US008884373B2

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Sato et al.

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(45) **Date of Patent: Nov. 11, 2014**

(54) **SEMICONDUCTOR DEVICE**

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(73) Assignee: **Panasonic Corporation**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 5 days.

(21) Appl. No.: **13/665,376**

(22) Filed: **Oct. 31, 2012**

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US 2013/0056832 A1 Mar. 7, 2013

Related U.S. Application Data

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(30) **Foreign Application Priority Data**

Mar. 25, 2011 (JP) 2011-068131

(51) **Int. Cl.**

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H01L 21/8238	(2006.01)
H01L 21/768	(2006.01)
H01L 27/11	(2006.01)
H01L 27/105	(2006.01)
H01L 21/285	(2006.01)

(52) **U.S. Cl.**

CPC .. ***H01L 21/823842*** (2013.01); ***H01L 21/76895*** (2013.01); ***H01L 27/1116*** (2013.01); ***H01L 27/1104*** (2013.01); ***H01L 27/105*** (2013.01); ***H01L 21/28518*** (2013.01); *Y10S 257/903* (2013.01)

USPC **257/369**; 257/392; 257/903; 257/E27.098

(58) **Field of Classification Search**

USPC 257/392, 903, E27.098, 369

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

2003/0107090	A1	6/2003	Kumeno	
2008/0036010	A1 *	2/2008	Tamaki et al.	257/372

FOREIGN PATENT DOCUMENTS

JP	6-275788	A	9/1994	
JP	8-017934	A	1/1996	
JP	2010-067912	*	3/2010	H01L 21/0238
JP	2010-067912	A	3/2010	

OTHER PUBLICATIONS

International Search Report issued in International Application No. PCT/JP2011/006167 oissued on Jan. 24, 2011.

* cited by examiner

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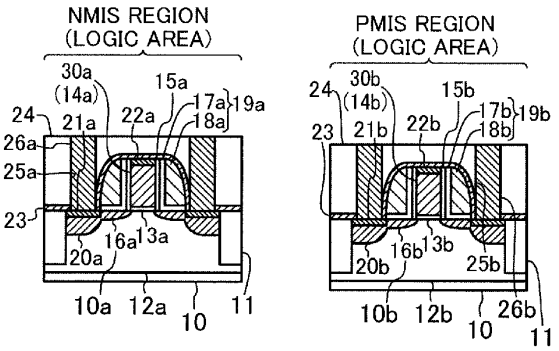
(57) **ABSTRACT**

A first dual-gate electrode includes a gate electrode located on a first active region and having a first silicon film of a first conductivity type and a gate electrode located on a second active region and having a first silicon film of a second conductivity type. A second dual-gate electrode includes a gate electrode located on a third active region and having a second silicon film of the first conductivity type and a gate electrode located on a fourth active region and having a second silicon film of the second conductivity type. At least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

14 Claims, 16 Drawing Sheets



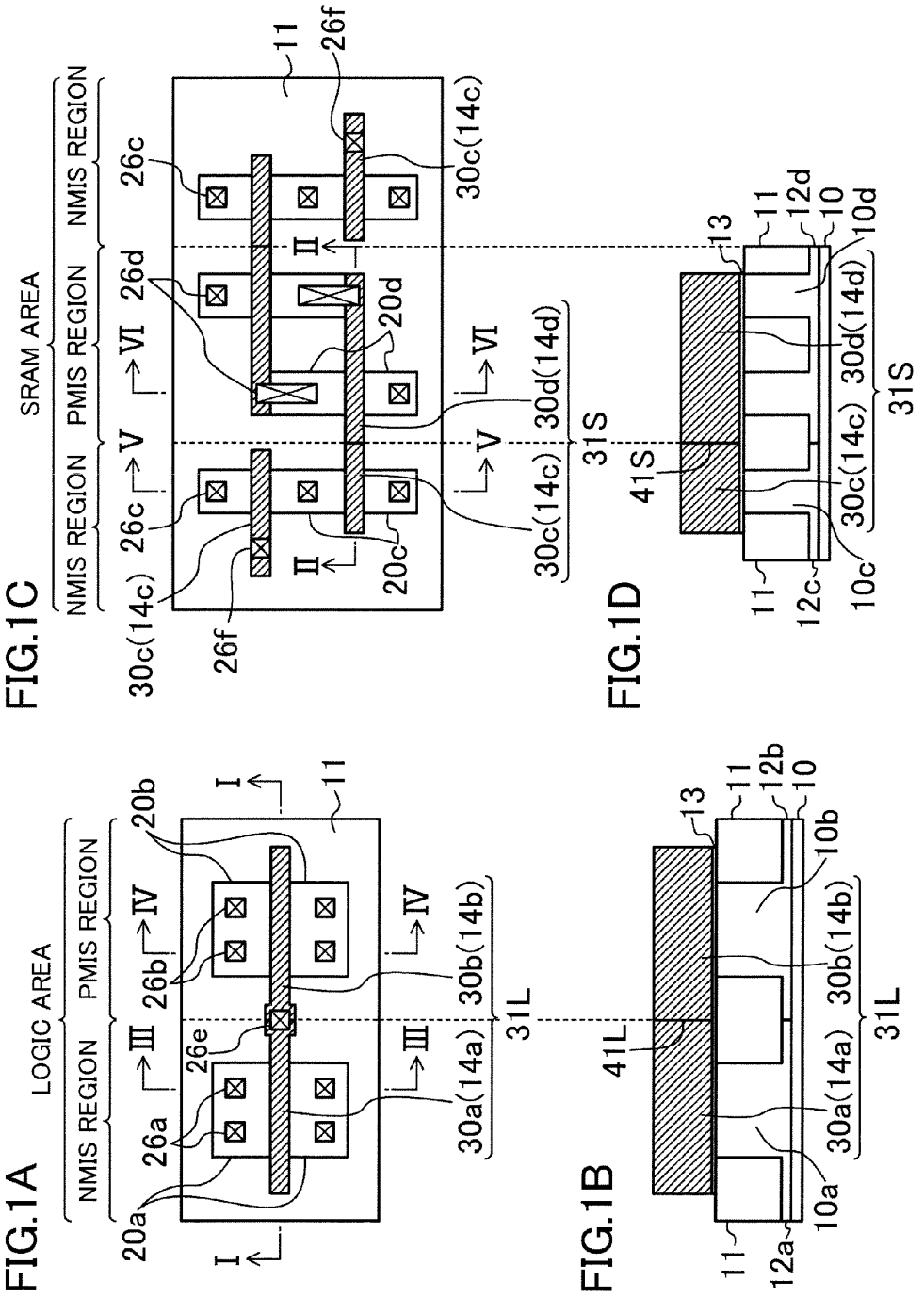


FIG.1A
LOGIC AREA
NMIS REGION
PMIS REGION
20a
26a
26e
26b
20b
III
IV
I
11
30a(14a)
30b(14b)
31L
FIG.1B
41L
13
11
12a
12b
10
10a
10b
FIG.1C
SRAM AREA
NMIS REGION
PMIS REGION
NMIS REGION
26c
26d
26f
30c(14c)
20c
20d
V
VI
II
30d(14d)
31S
FIG.1D
41S
12c
12d
10c
10d

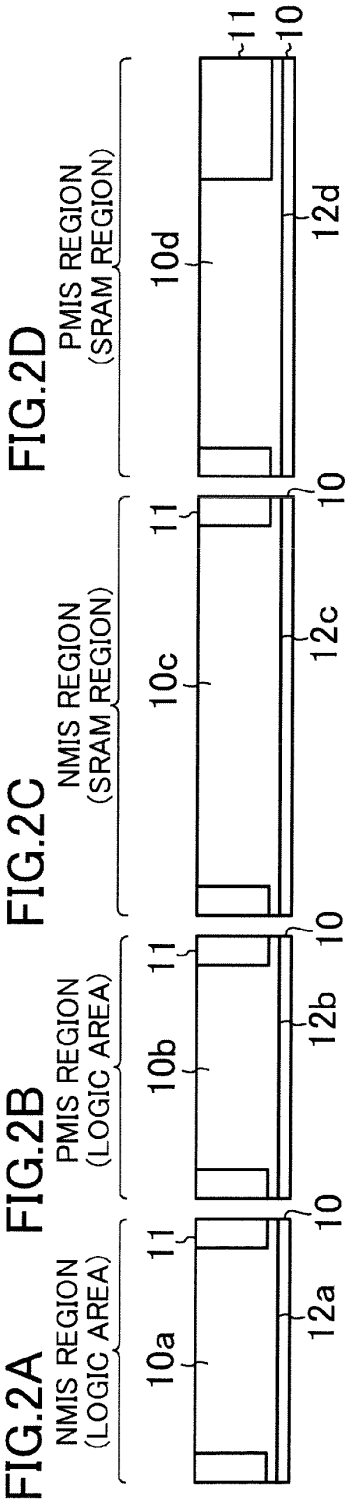


FIG.2A
NMIS REGION
(LOGIC AREA)
10a
11
12a
10
FIG.2B
PMIS REGION
(LOGIC AREA)
10b
11
12b
10
FIG.2C
NMIS REGION
(SRAM REGION)
10c
11
12c
10
FIG.2D
PMIS REGION
(SRAM REGION)
10d
11
12d
10

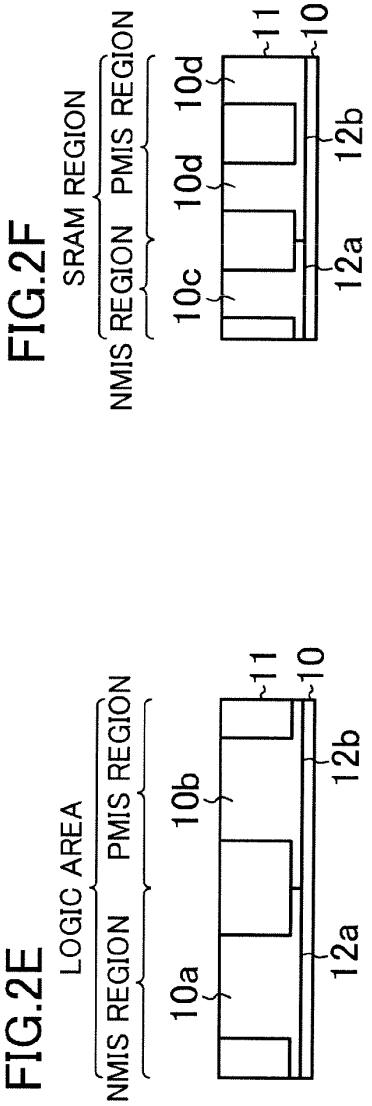


FIG.2E
LOGIC AREA
NMIS REGION
PMIS REGION
10a
10b
11
12a
12b
10
FIG.2F
SRAM REGION
NMIS REGION
PMIS REGION
10c
10d
10d
11
12a
12b
10

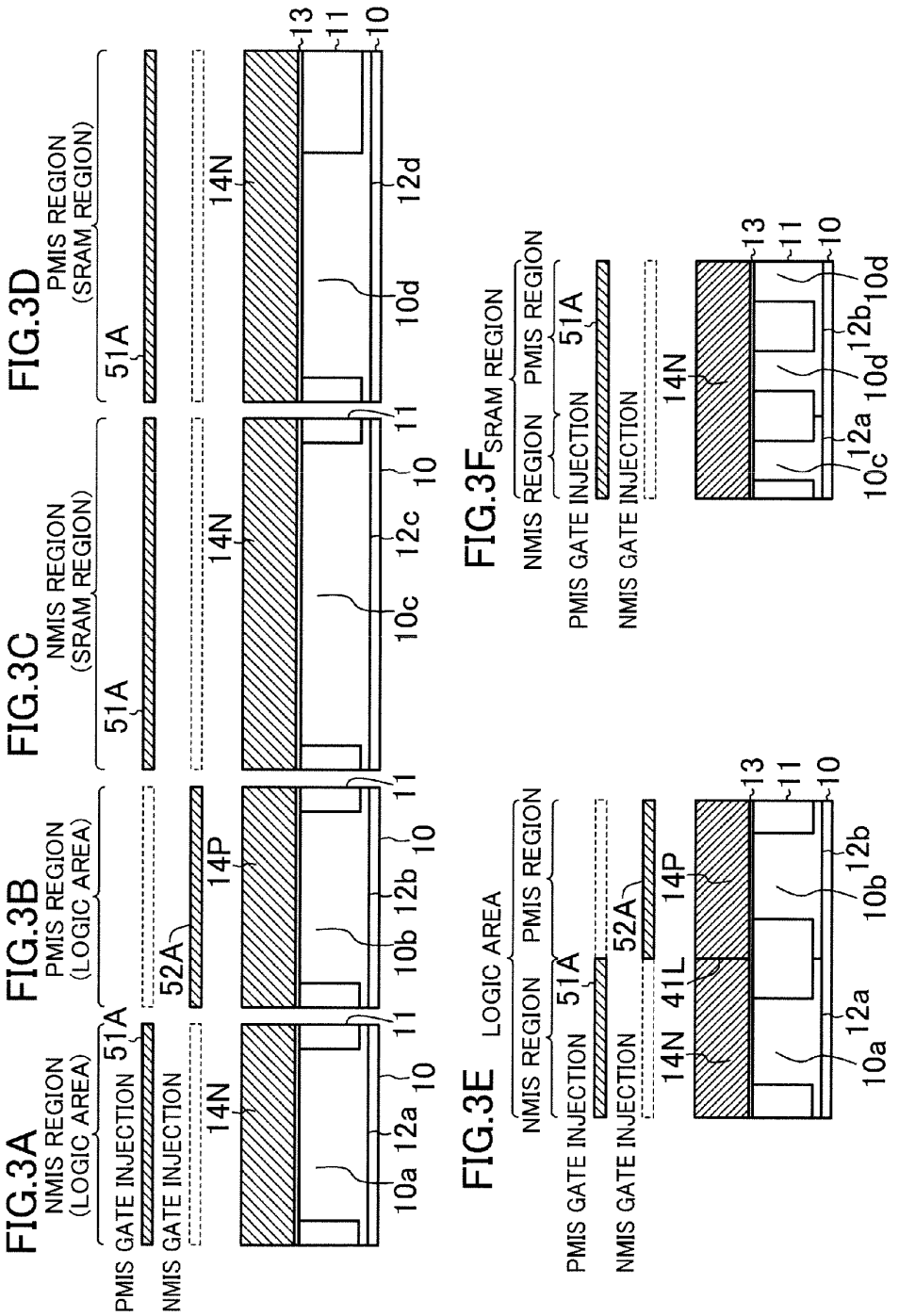


FIG.3A
NMIS REGION (LOGIC AREA)
PMIS GATE INJECTION
NMIS GATE INJECTION
51A
14N
10a
12a
10
11
FIG.3B
PMIS REGION (LOGIC AREA)
52A
14P
10b
12b
10
11
FIG.3C
NMIS REGION (SRAM REGION)
51A
14N
10c
12c
10
11
FIG.3D
PMIS REGION (SRAM REGION)
51A
14N
10d
12d
13
11
10
FIG.3E
LOGIC AREA
NMIS REGION
PMIS REGION
PMIS GATE INJECTION
NMIS GATE INJECTION
51A
52A
14N
41L
14P
10a
12a
10b
12b
13
11
10
FIG.3F
SRAM REGION
NMIS REGION
PMIS REGION
PMIS GATE INJECTION
NMIS GATE INJECTION
51A
14N
10c
12a
10d
12b
10d
13
11
10

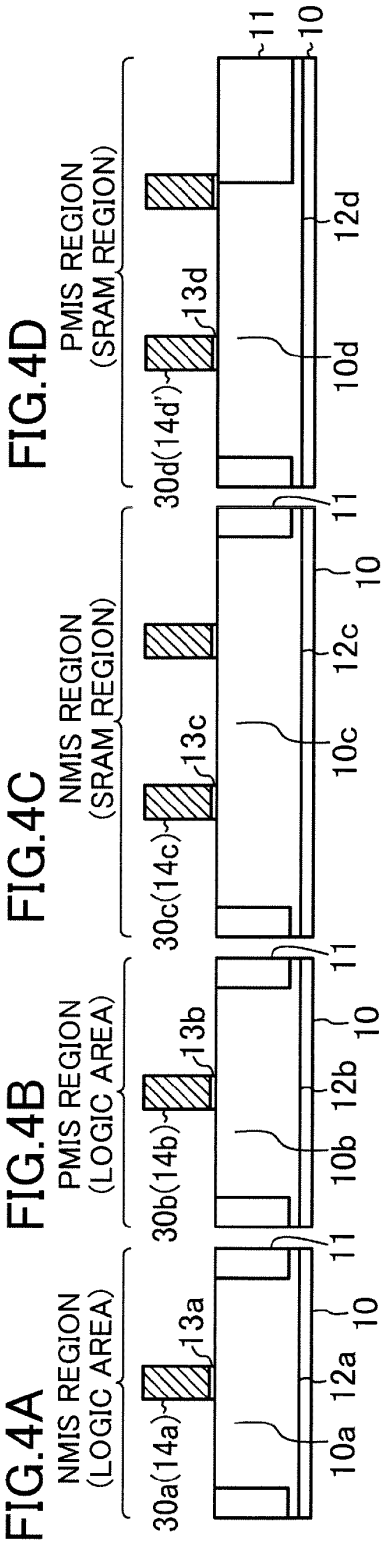


FIG.4A
NMIS REGION (LOGIC AREA)
30a(14a)
13a
10a
12a
10
11
FIG.4B
PMIS REGION (LOGIC AREA)
30b(14b)
13b
10b
12b
10
11
FIG.4C
NMIS REGION (SRAM REGION)
30c(14c)
13c
10c
12c
10
11
FIG.4D
PMIS REGION (SRAM REGION)
30d(14d')
13d
10d
12d
10
11

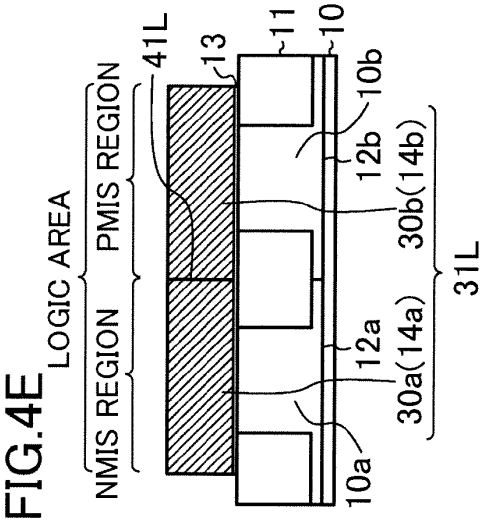


FIG.4E
LOGIC AREA
NMIS REGION
PMIS REGION
41L
13
10a
12a
30a(14a)
10b
12b
30b(14b)
10
11
31L

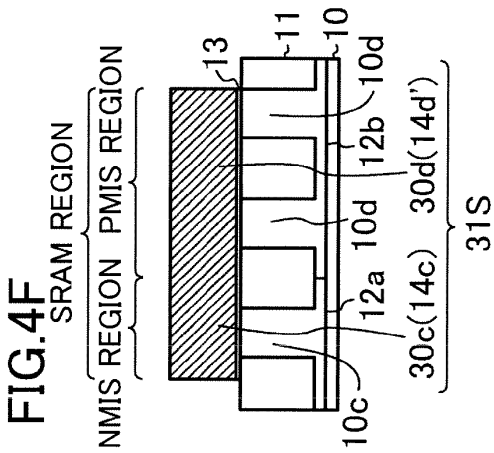


FIG.4F
SRAM REGION
NMIS REGION
PMIS REGION
13
10c
12a
30c(14c)
10d
12b
30d(14d')
10
11
31S

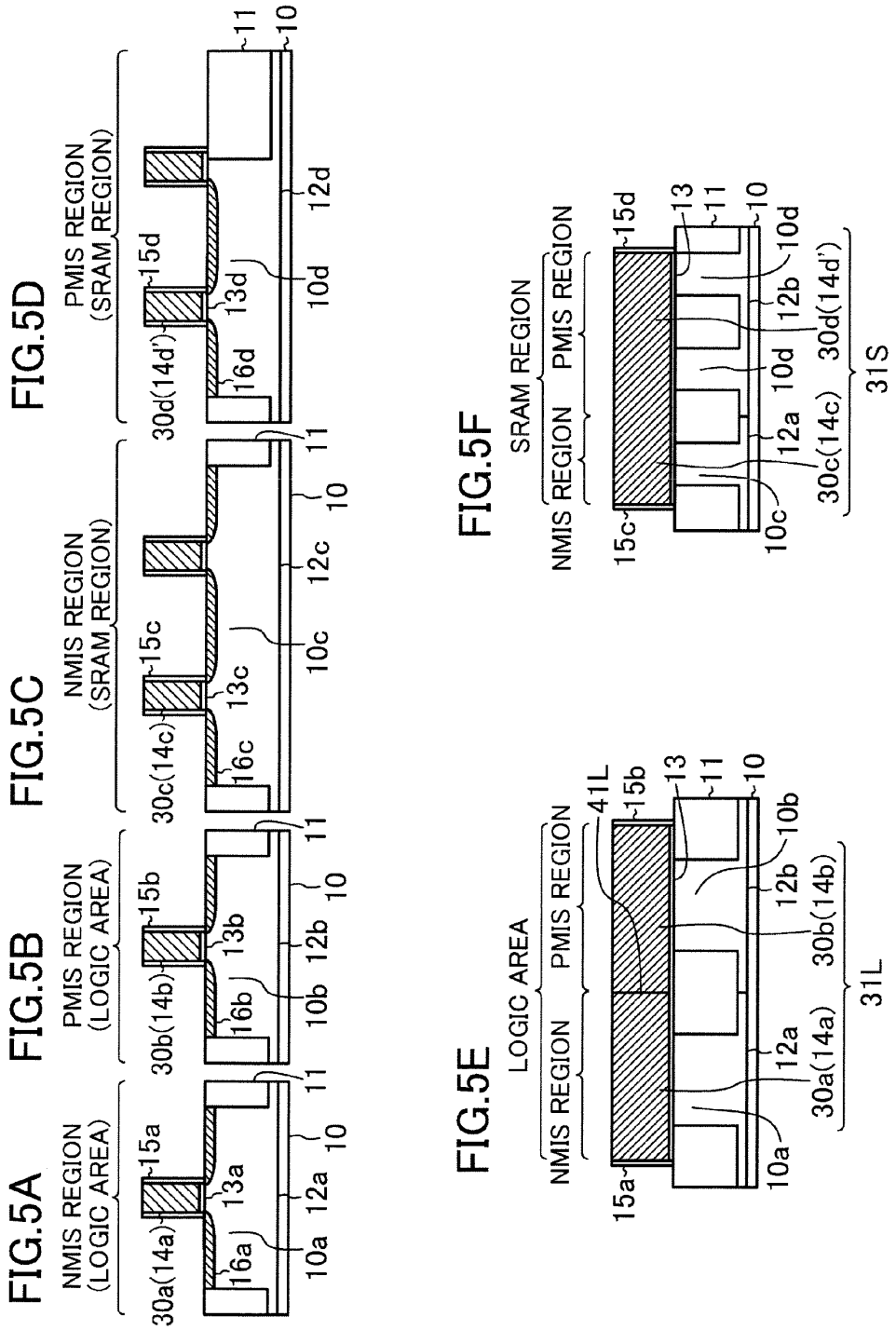


FIG.5A
NMIS REGION (LOGIC AREA)
30a(14a)
15a
16a
13a
10a
12a
10
11
FIG.5B
PMIS REGION (LOGIC AREA)
30b(14b)
15b
16b
13b
10b
12b
10
11
FIG.5C
NMIS REGION (SRAM REGION)
30c(14c)
15c
16c
13c
10c
12c
10
11
FIG.5D
PMIS REGION (SRAM REGION)
30d(14d')
15d
16d
13d
10d
12d
10
11
FIG.5E
LOGIC AREA
NMIS REGION
PMIS REGION
15a
41L
15b
10a
12a
30a(14a)
10b
12b
30b(14b)
13
11
10
31L
FIG.5F
SRAM REGION
NMIS REGION
PMIS REGION
15c
15d
10c
12a
10d
30c(14c)
12b
10d
30d(14d')
13
11
10
31S

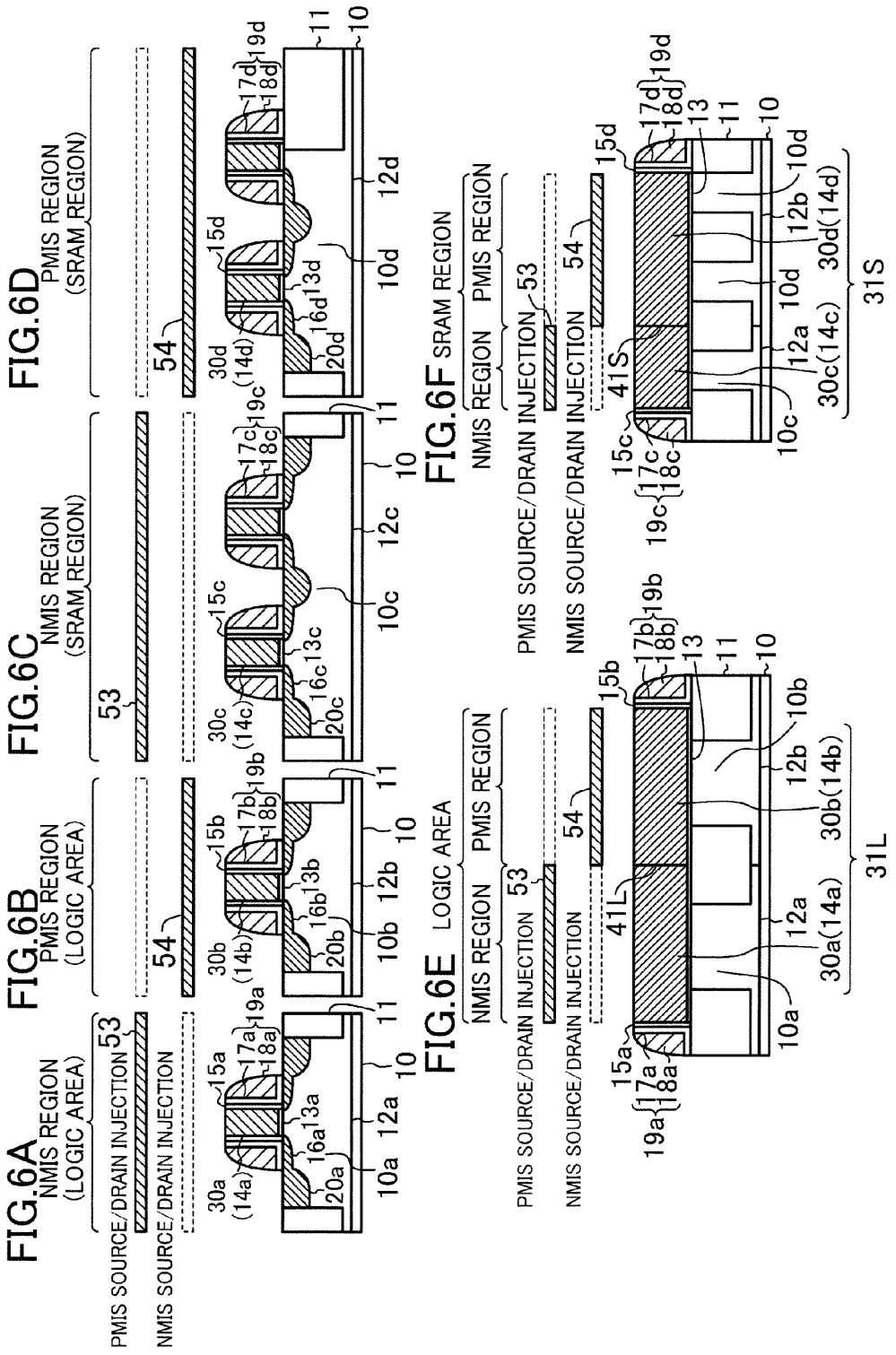


FIG.6A
NMIS REGION (LOGIC AREA)
PMIS SOURCE/DRAIN INJECTION
NMIS SOURCE/DRAIN INJECTION
FIG.6B
PMIS REGION (LOGIC AREA)
FIG.6C
NMIS REGION (SRAM REGION)
FIG.6D
PMIS REGION (SRAM REGION)
FIG.6E
LOGIC AREA
NMIS REGION
PMIS REGION
PMIS SOURCE/DRAIN INJECTION
NMIS SOURCE/DRAIN INJECTION
FIG.6F
SRAM REGION
NMIS REGION
PMIS REGION
PMIS SOURCE/DRAIN INJECTION
NMIS SOURCE/DRAIN INJECTION
31L
31S

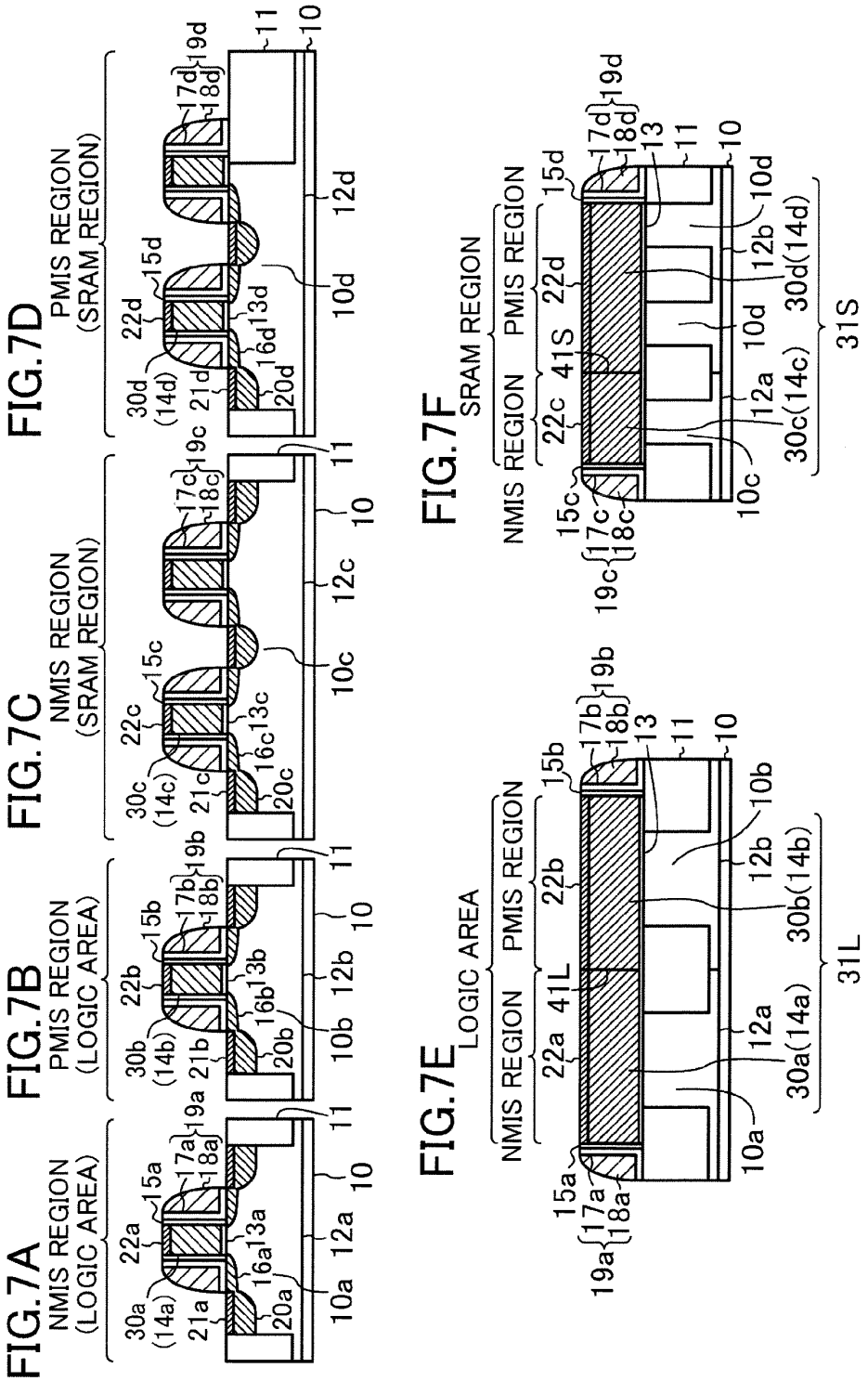


FIG.7A
NMIS REGION
(LOGIC AREA)
FIG.7B
PMIS REGION
(LOGIC AREA)
FIG.7C
NMIS REGION
(SRAM REGION)
FIG.7D
PMIS REGION
(SRAM REGION)
FIG.7E
LOGIC AREA
NMIS REGION
PMIS REGION
FIG.7F
SRAM REGION
NMIS REGION
PMIS REGION
31L
31S

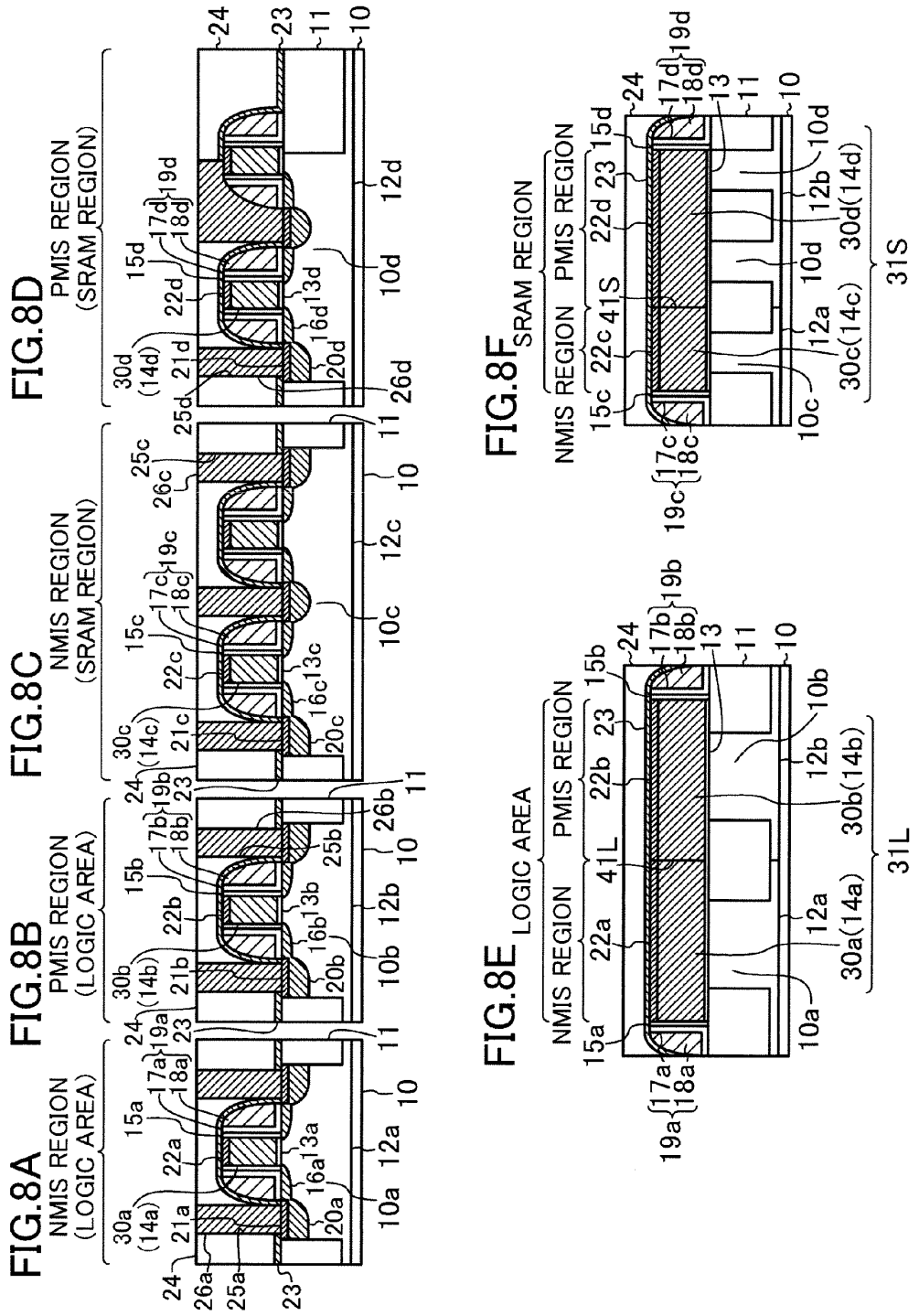


FIG.8A
NMIS REGION (LOGIC AREA)
FIG.8B
PMIS REGION (LOGIC AREA)
FIG.8C
NMIS REGION (SRAM REGION)
FIG.8D
PMIS REGION (SRAM REGION)
FIG.8E
LOGIC AREA
NMIS REGION
PMIS REGION
FIG.8F
SRAM REGION
NMIS REGION
PMIS REGION

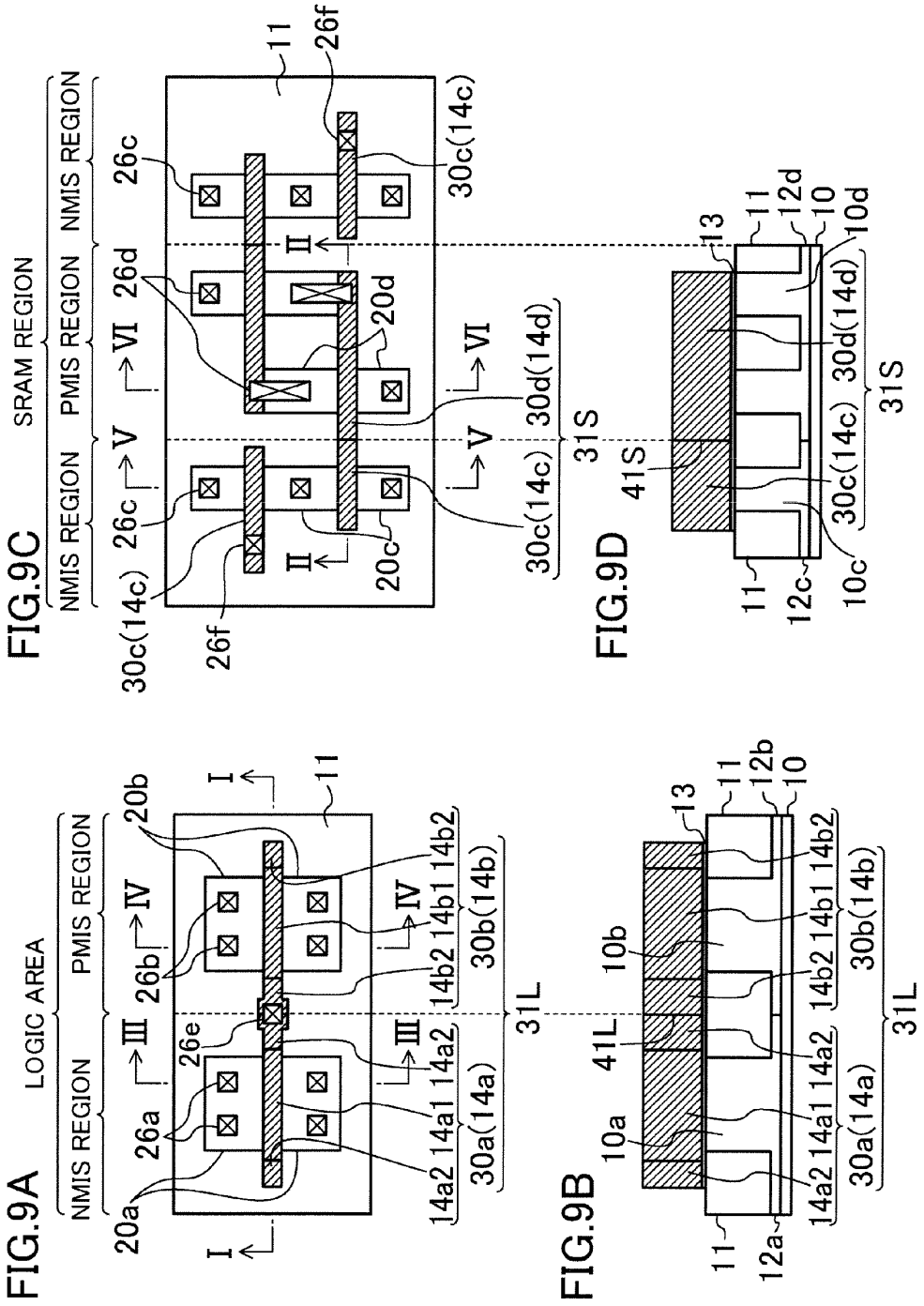


FIG.9A
LOGIC AREA
NMIS REGION
PMIS REGION
20a
26a
26e
26b
20b
III
IV
I
11
14a2 14a1 14a2
30a(14a)
14b2 14b1 14b2
30b(14b)
31L
FIG.9B
13
10a
41L
10b
11
12a
12b
10
FIG.9C
SRAM REGION
NMIS REGION
PMIS REGION
NMIS REGION
30c(14c)
26c
26d
26f
V
VI
II
20c
20d
30d(14d)
31S
41S
FIG.9D
12c
12d
10c
10d

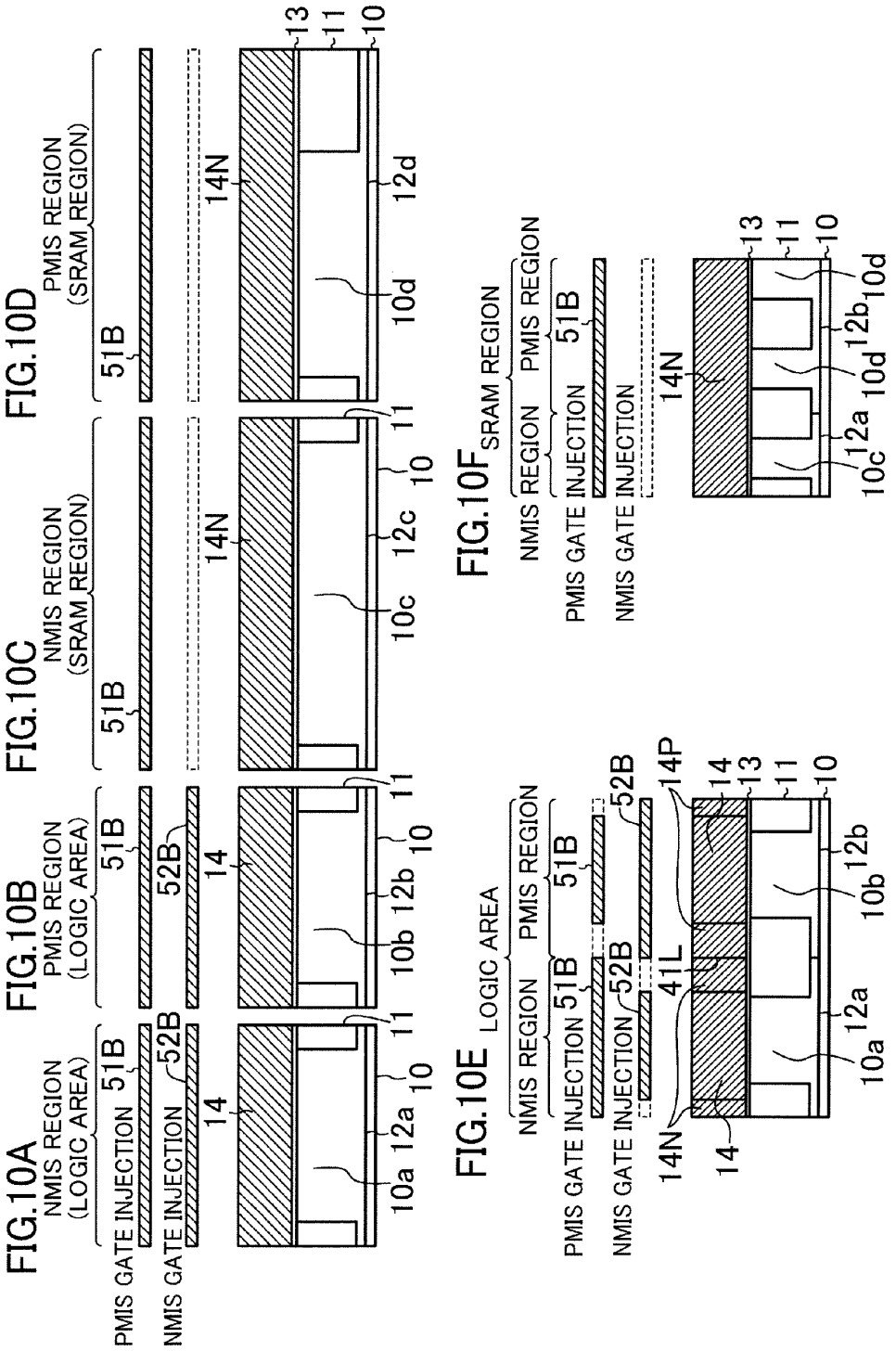


FIG.10A
NMIS REGION (LOGIC AREA)
PMIS GATE INJECTION
NMIS GATE INJECTION
51B
52B
14
10a
12a
10
11
FIG.10B
PMIS REGION (LOGIC AREA)
51B
52B
14
10b
12b
10
11
FIG.10C
NMIS REGION (SRAM REGION)
51B
14N
10c
12c
10
11
FIG.10D
PMIS REGION (SRAM REGION)
51B
14N
10d
12d
13
11
10
FIG.10E
LOGIC AREA
NMIS REGION
PMIS REGION
PMIS GATE INJECTION
NMIS GATE INJECTION
51B
52B
41L
14P
14N
14
13
11
10
10a
12a
10b
12b
FIG.10F
SRAM REGION
NMIS REGION
PMIS REGION
PMIS GATE INJECTION
NMIS GATE INJECTION
51B
14N
13
11
10
10c
12a
10d
12b
10d

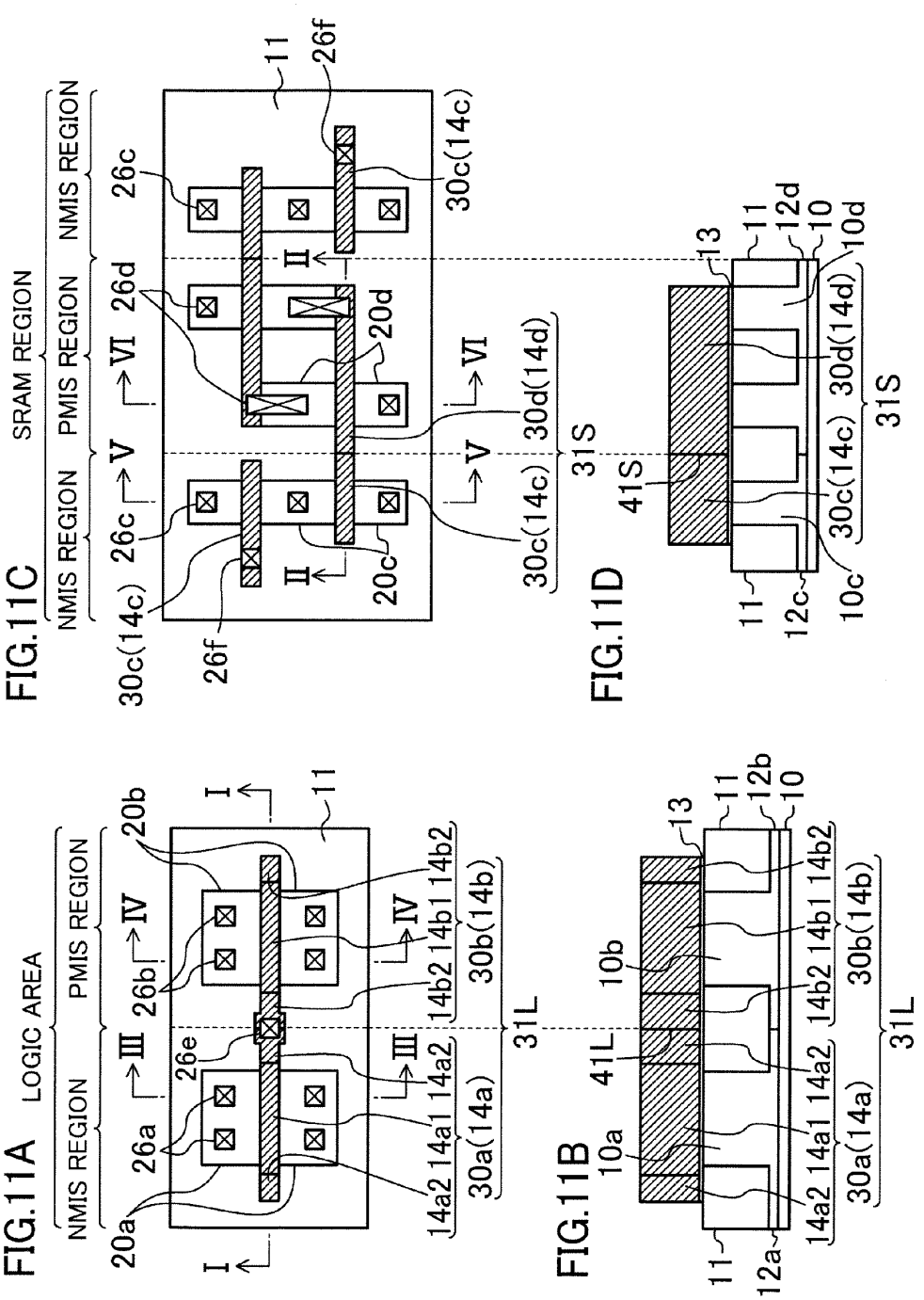


FIG.11A
LOGIC AREA
NMIS REGION
PMIS REGION
20a
26a
26b
20b
26e
I
III
IV
11
14a2 14a1 14a2
14b2 14b1 14b2
30a(14a)
30b(14b)
31L
FIG.11B
10a
10b
41L
13
11
12a
12b
10
FIG.11C
SRAM REGION
NMIS REGION
PMIS REGION
NMIS REGION
30c(14c)
26c
26d
26f
V
VI
II
20c
20d
30d(14d)
31S
FIG.11D
41S
12c
12d
10c
10d

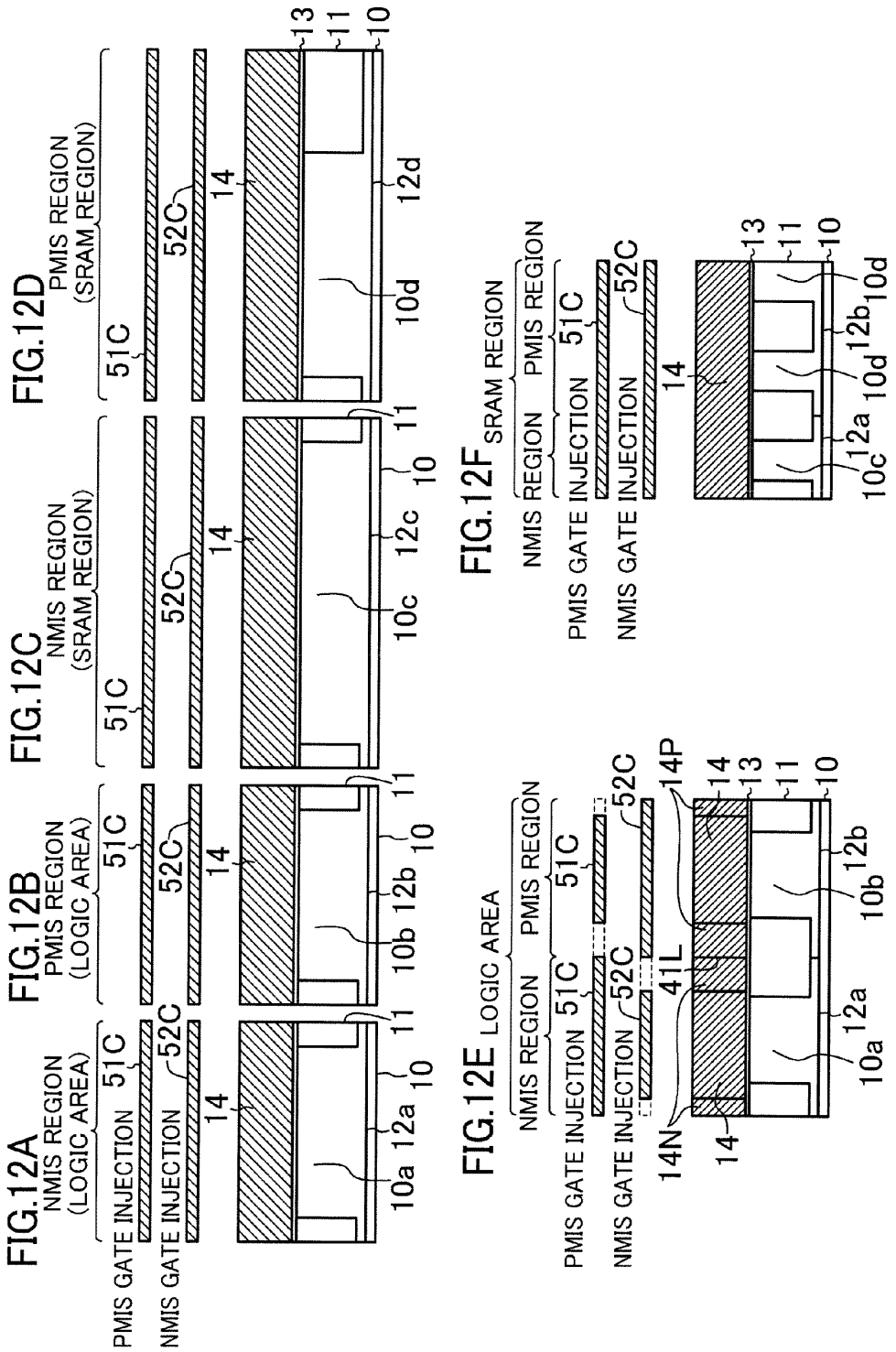


FIG.12A
NMIS REGION (LOGIC AREA)
PMIS GATE INJECTION
NMIS GATE INJECTION
51C
52C
14
10a
12a
10
11
FIG.12B
PMIS REGION (LOGIC AREA)
10b
12b
FIG.12C
NMIS REGION (SRAM REGION)
10c
12c
FIG.12D
PMIS REGION (SRAM REGION)
10d
12d
13
FIG.12E
LOGIC AREA
NMIS REGION
PMIS REGION
41L
14P
14N
FIG.12F
SRAM REGION

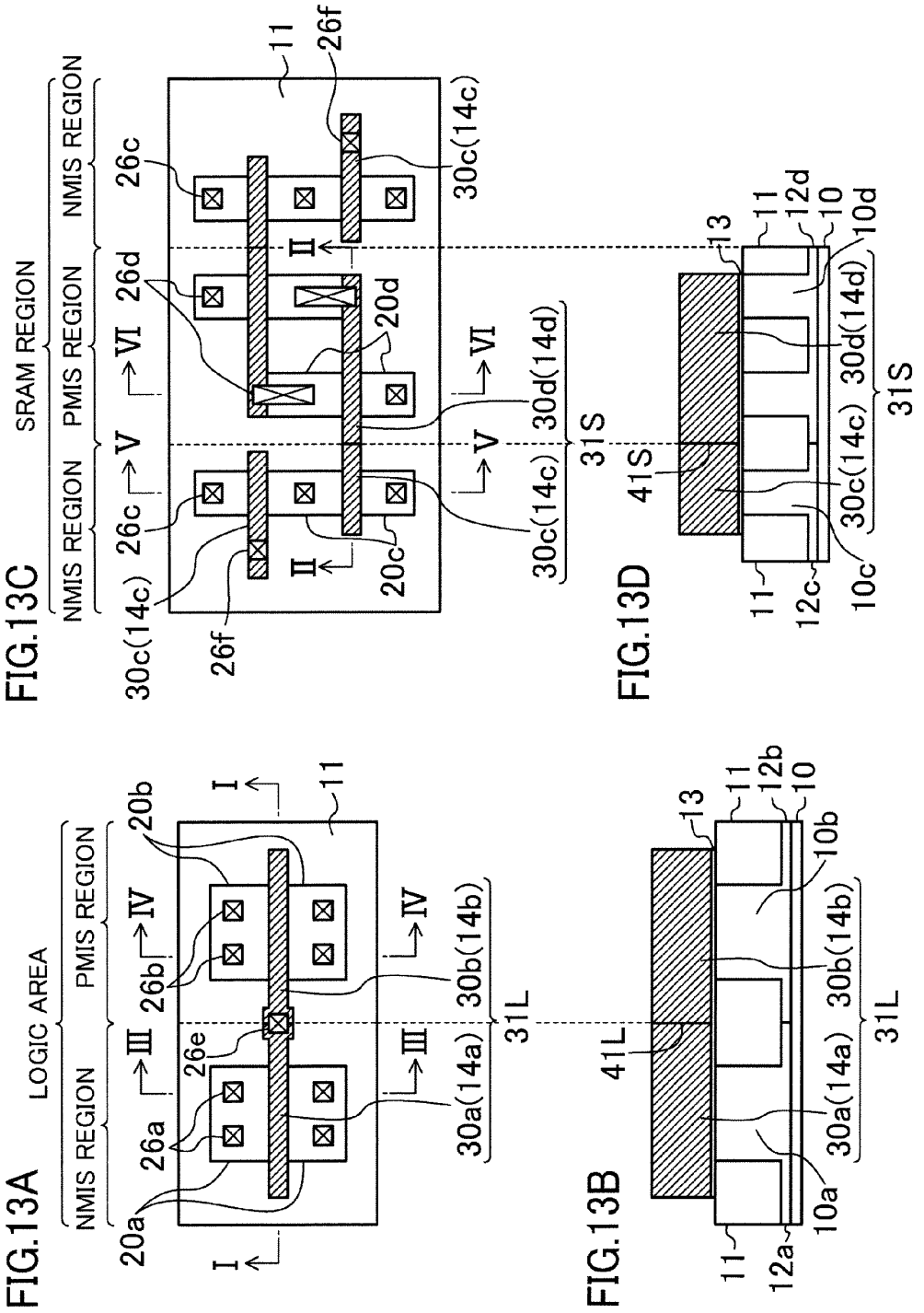


FIG.13A
LOGIC AREA
NMIS REGION
PMIS REGION
20a
26a
26e
26b
20b
I
III
IV
11
30a(14a)
30b(14b)
31L
FIG.13B
41L
13
11
12a
10a
12b
10
10b
FIG.13C
SRAM REGION
NMIS REGION
PMIS REGION
NMIS REGION
30c(14c)
26c
26d
26f
V
VI
II
20c
20d
30d(14d)
31S
FIG.13D
41S
12c
12d
10c
10d

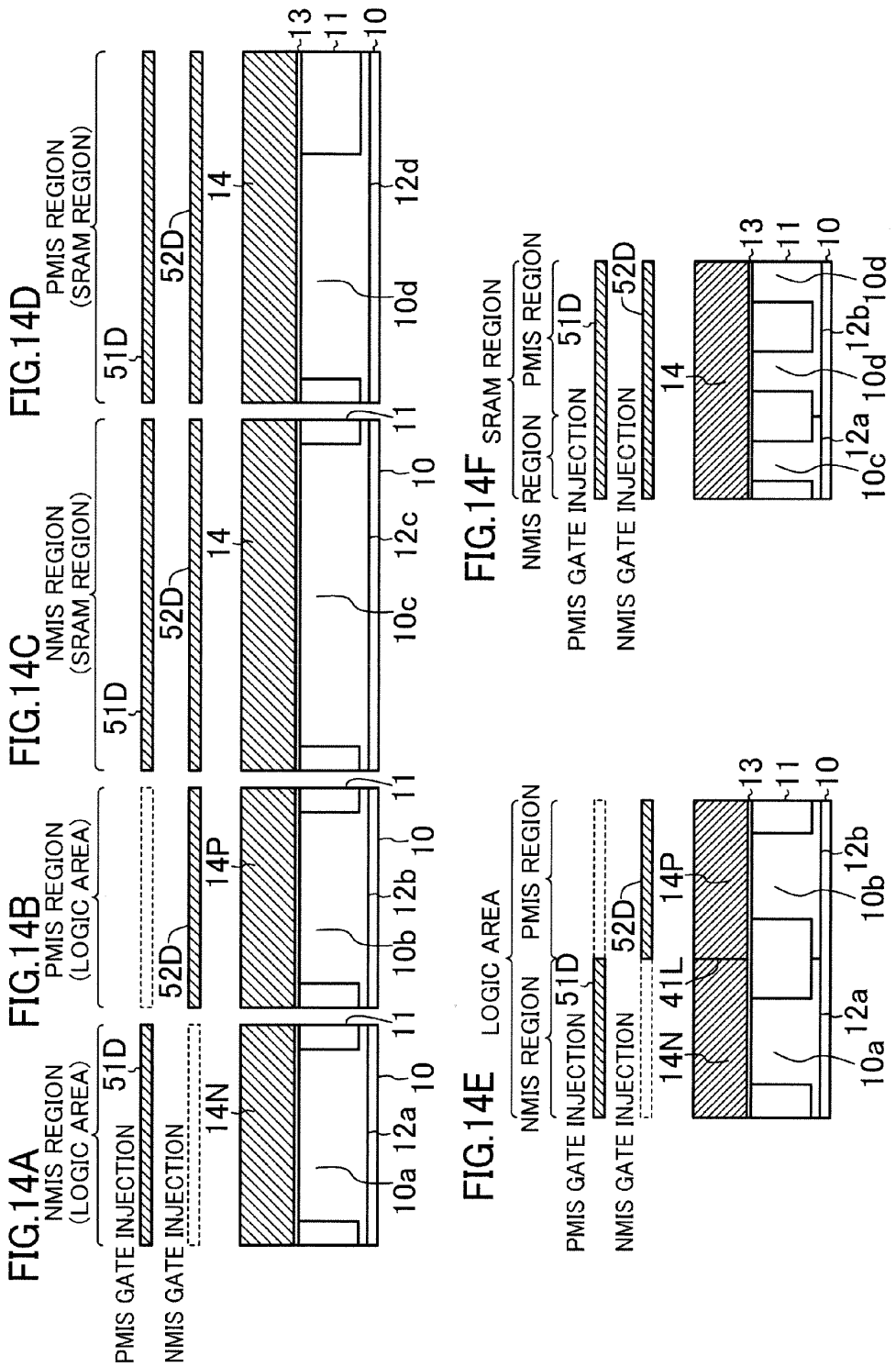


FIG.14A
NMIS REGION (LOGIC AREA)
PMIS GATE INJECTION
NMIS GATE INJECTION
51D
14N
10a
12a
10
11
FIG.14B
PMIS REGION (LOGIC AREA)
52D
14P
10b
12b
10
11
FIG.14C
NMIS REGION (SRAM REGION)
51D
52D
14
10c
12c
10
11
FIG.14D
PMIS REGION (SRAM REGION)
51D
52D
14
10d
12d
13
11
10
FIG.14E
LOGIC AREA
NMIS REGION
PMIS REGION
PMIS GATE INJECTION
NMIS GATE INJECTION
51D
52D
14N
41L
14P
10a
12a
10b
12b
13
11
10
FIG.14F
SRAM REGION
NMIS REGION
PMIS REGION
PMIS GATE INJECTION
NMIS GATE INJECTION
51D
52D
14
10c
12a
10d
12b
10d
13
11
10

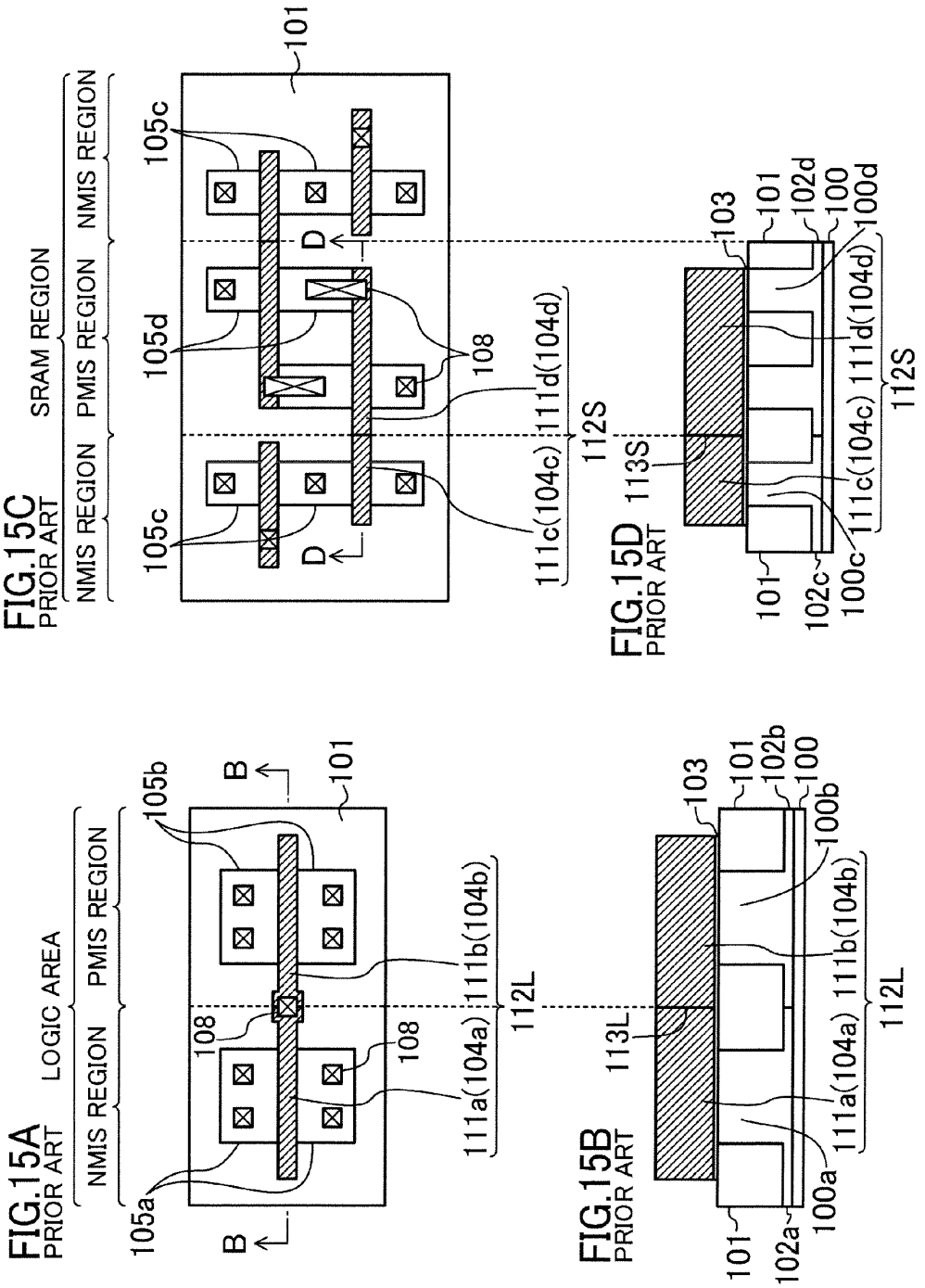


FIG.15A
PRIOR ART
LOGIC AREA
NMIS REGION
PMIS REGION
105a
105b
108
108
B
B
101
111a(104a)
111b(104b)
112L
FIG.15B
PRIOR ART
113L
103
101
102a
102b
100
100a
100b
111a(104a)
111b(104b)
112L
FIG.15C
PRIOR ART
SRAM REGION
NMIS REGION
PMIS REGION
NMIS REGION
105c
105d
105c
D
D
101
108
111c(104c)
111d(104d)
112S
FIG.15D
PRIOR ART
113S
103
101
102c
102d
100
100c
100d
111c(104c)
111d(104d)
112S

FIG.16A
PRIOR ART

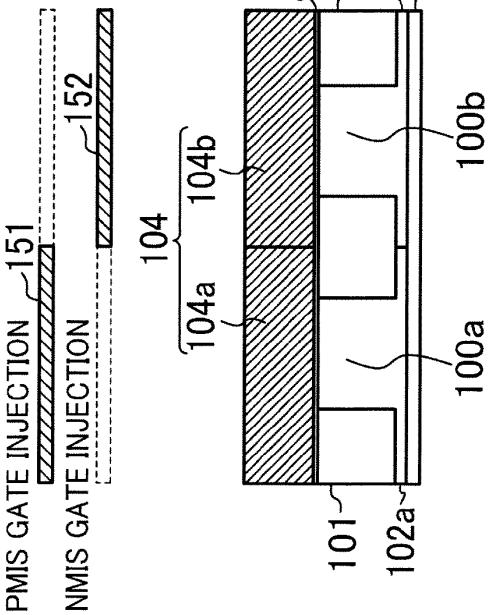
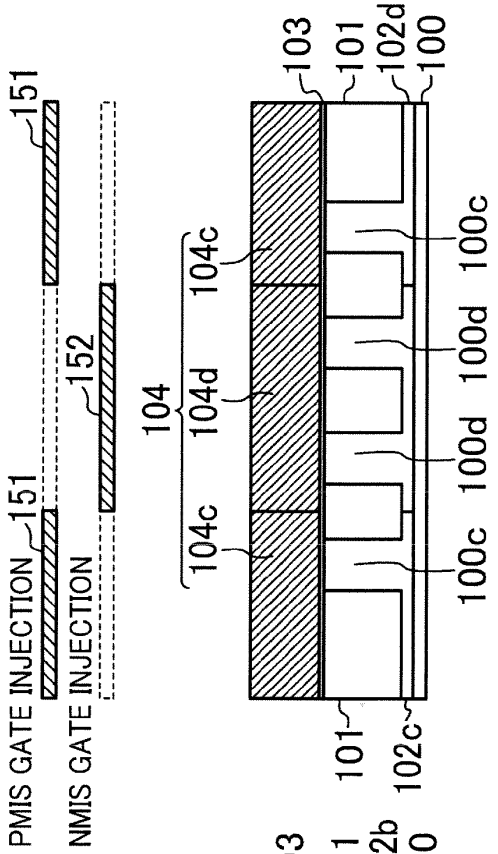


FIG.16B
PRIOR ART



SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This is a continuation of PCT International Application PCT/JP2011/006167 filed on Nov. 4, 2011, which claims priority to Japanese Patent Application No. 2011-068131 filed on Mar. 25, 2011. The disclosures of these applications including the specifications, the drawings, and the claims are hereby incorporated by reference in their entirety.

BACKGROUND

The present disclosure relates to semiconductor devices and methods for fabricating semiconductor devices, and more particularly to a semiconductor device having a complementary metal insulator semiconductor (CMIS) dual-gate structure and a method for fabricating such a semiconductor device.

The integration degree of semiconductor integrated circuits have been increased by miniaturizing CMIS devices with dual-gate structures. A CMIS device with a dual-gate structure generally refers to a device including a polysilicon film doped with an n-type impurity as a gate electrode of an n-channel metal insulator semiconductor field effect transistor (hereinafter referred to as an NMISFET) and also including a polysilicon film doped with a p-type impurity as a gate electrode of a p-channel MISFET (hereinafter referred to as a PMISFET) (see, for example, Japanese Patent Publication No. H06-275788). In a CMIS device with a dual-gate structure, a metal silicide layer is formed on a polysilicon gate electrode in order to connect an n-type polysilicon gate electrode and a p-type polysilicon gate electrode. In this structure, in the boundary between an n-type region and a p-type region in each of the polysilicon gate electrode, impurities in these regions are diffused from one region to the other through the metal silicide layer or the polysilicon film, resulting in a change in work function of the gate electrode, and thus, a variation in threshold voltage of each of the FETs.

As a conventional method for forming an n-type region and a p-type region in a polysilicon film for gate electrodes, ions of impurities are implanted into the polysilicon film for gate electrodes using a mask designed such that the boundary between the n-type region and the p-type region is located on an isolation between well regions (see, for example, Japanese Patent Publication No. H08-17934).

A conventional semiconductor device in which an n-type region and a p-type region are formed by implanting ions into gate electrodes of a transistor for a logic circuit and a transistor for a static random access memory (SRAM) circuit will be described with reference to the drawings.

FIG. **15**A is a plan view illustrating a logic area of a conventional semiconductor device. FIG. **15**B is a cross-sectional view taken along the line B-B (along the gate width) in FIG. **15**A. FIG. **15**C is a plan view illustrating an SRAM area of the conventional semiconductor device. FIG. **15**D is a cross-sectional view taken along the line D-D (along the gate width) in FIG. **15**C. In FIGS. **15**A-**15**D, sidewall spacers, a silicide layer, and an interlayer film, for example, are not shown for simplicity, and contacts are not shown in FIGS. **15**B and **15**D.

As illustrated in FIGS. **15**A-**15**D, each of the logic area and the SRAM area of the conventional semiconductor device has an NMIS region and a PMIS region. In the NMIS region in the logic area, a p-well region **102***a* is provided on a semiconductor substrate **100** and an active region **100***a* is surrounded by

an isolation region **101**. In the PMIS region in the logic area, an n-well region **102***b* is provided on the semiconductor substrate **100** and an active region **100***b* is surrounded by the isolation region **101**. In the NMIS region in the SRAM area, a p-well region **102***c* is provided on the semiconductor substrate **100**, and an active region **100***c* is surrounded by the isolation region **101**. In the PMIS region in the SRAM area, an n-well region **102***d* is provided on the semiconductor substrate **100**, and an active region **100***d* is surrounded by the isolation region **101**.

On the active region **100***a*, a gate electrode **111***a* including an n-type polysilicon film **104***a* is formed with a gate insulating film **103** interposed therebetween. On the active region **100***b*, a gate electrode **111***b* including a p-type polysilicon film **104***b* is formed with the gate insulating film **103** interposed therebetween. The gate electrode **111***a* and the gate electrode **111***b* are connected to each other at a PN boundary **113**L between the active region **100***a* and the active region **100***b* on the isolation region **101**, thereby forming a dual-gate electrode **112**L. N-type source/drain regions **105***a* are defined at both sides of the gate electrode **111***a* in the active region **100***a*. P-type source/drain regions **105***b* are defined at both sides of the gate electrode **111***b* in the active region **100***b*. A contact **108** is formed to be connected to the dual-gate electrode **112**L, the n-type source/drain regions **105***a*, and the p-type source/drain regions **105***b*.

On the active region **100***c*, a gate electrode **111***c* including an n-type polysilicon film **104***c* is formed with the gate insulating film **103** interposed therebetween. On the active region **100***d*, a gate electrode **111***d* including a p-type polysilicon film **104***d* is formed with gate insulating film **103** interposed therebetween. The gate electrode **111***c* and the gate electrode **111***d* are connected to each other at a PN boundary **1135** between the active region **100***c* and the active region **100***d* on the isolation region **101**, thereby forming a dual-gate electrode **112**S. N-type source/drain regions **105***c* are defined at both sides of the gate electrode **111***c* in the active region **100***c*. P-type source/drain regions **105***d* are defined at both sides of the gate electrode **111***d* in the active region **100***d*. A contact **108** is formed to be connected to the dual-gate electrode **112**S, the n-type source/drain regions **105***c*, and the p-type source/drain regions **105***d*.

FIGS. **16**A and **16**B are views schematically illustrating formation of a p-type region and an n-type region by implanting ions of impurities into a polysilicon film (before gate patterning) to be dual-gate electrodes **112**L and **112**S. In FIGS. **16**A and **16**B, components already shown in FIGS. **15**A-**15**D are denoted by the same reference characters.

As illustrated in FIGS. **16**A and **16**B, in gate injection for the PMIS regions, ions of a p-type impurity are implanted into the polysilicon film **104** using a mask pattern **151** covering the NMIS region in each of the logic area and the SRAM area, thereby forming p-type polysilicon films **104***b* and **104***d*. That is, the p-type polysilicon films **104***b* and **104***d* have substantially the same concentration of the p-type impurity. In gate injection for the NMIS regions, ions of an n-type impurity are implanted into the polysilicon film **104** using a mask pattern **152** covering the PMIS region of each of the logic area and the SRAM area, thereby forming n-type polysilicon films **104***a* and **104***c*. That is, the n-type polysilicon films **104***a* and **104***c* have substantially the same concentration of the n-type impurity. For simplicity, not resist patterns actually employed in ion implantation but mask patterns on photomasks for forming the resist patterns are schematically shown as the mask patterns **151** and **152**. The mask patterns **151** and **152** are designed such that the PN boundaries formed in the polysilicon film **104** are located between the active region **100***a* and

the active region **100***b* and between the active region **100***c* and the active region **100***d*, respectively, on the isolation region **101**.

Although not shown, in ion implantation for forming source/drain regions in each of the PMIS region and the NMIS region, mask patterns similar to the mask patterns **151** and **152** shown in FIGS. **16**A and **16**B are used.

In the gate injection illustrated in FIGS. **16**A and **16**B, the PN boundary formed in the polysilicon film **104** is located on a portion of the isolation region between the active regions. Thus, it is possible to reduce degradation of characteristics of FETs due to mutual diffusion of impurities between the n-type region and the p-type region in the polysilicon gate electrode.

SUMMARY

However, as the gate length decreases with miniaturization of devices, there arises the following problem in addition to the problem of mutual diffusion in the polysilicon film. Specifically, the difference in the etching speed of the polysilicon film between different types of ions serving as dopants relatively increases, thereby causing a variation in final gate length, and as a result, a variation in the threshold voltages of transistors arises. To solve the problem, especially in devices such as SRAMs which need to have their cell sizes reduced, it is necessary to reduce a variation in gate dimensions occurring near a PN boundary.

In addition, as in the conventional method described above, even if the PN boundary in the polysilicon gate electrode is located on a portion of the isolation region between the active regions, a small width of the isolation region especially in a device such as an SRAM makes the influence of mutual diffusion of impurities between the n-type region and the p-type region in the polysilicon gate electrode nonnegligible. Consequently, a variation occurs in the work functions of the gate electrodes to deteriorate transistor characteristics such as a variation in threshold voltage. As a result, failures in circuit operation often occurs.

It is therefore an object of the present disclosure to reduce a variation in transistor characteristics due to a variation in gate dimensions near a PN boundary and mutual diffusion of impurities in a semiconductor device with a CMIS dual-gate structure.

To achieve the object, a semiconductor device in an aspect of the present disclosure includes: a first dual-gate electrode; and a second dual-gate electrode, wherein the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type, the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type, the first active region and the second active region are isolated from each other with an isolation region interposed therebetween, the first gate electrode and the second gate electrode are connected to each other on the isolation region, and at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

In the semiconductor device, an isolation width between the first active region and the second active region may be larger than that between the third active region and the fourth active region.

In the semiconductor device, at least a portion of the first silicon film of the second conductivity type may have a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on each of the first active region and the isolation region may have a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the second active region may have a second-conductivity-type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the second active region may have a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region.

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the isolation region may have a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the isolation region may have a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the first conductivity type located on the third active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region.

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the second

active region may have a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the second active region may have a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region.

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the isolation region may have a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region, and a portion of the first silicon film of the second conductivity type located on the second active region may have a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, the first gate electrode may be a gate electrode of a first PMIS transistor, the second gate electrode may be a gate electrode of a first NMIS transistor, the third gate electrode may be a gate electrode of a second PMIS transistor, and the fourth gate electrode may be a gate electrode of a second NMIS transistor.

In the semiconductor device, each of the first gate electrode and the second gate electrode may be a gate electrode of a transistor for a logic circuit, and each of the third gate electrode and the fourth gate electrode may be a gate electrode of a transistor for an SRAM circuit.

A method for fabricating a semiconductor device in an aspect of the present disclosure is a method for forming a semiconductor device including a first dual-gate electrode including a first gate electrode located on a first active region and a second gate electrode located on a second active region and a second dual-gate electrode including a third gate electrode located on a third active region and a fourth gate electrode located on a fourth active region. The method for fabricating a semiconductor device includes the steps of: (a) forming a silicon film on the first active region, the second active region, the third active region, and the fourth active region; (b) introducing an impurity of a first conductivity type into the silicon film with portions of the silicon film located on the second active region, the third active region, and the fourth active region being covered with a first mask pattern; (c) introducing an impurity of a second conductivity type with a portion of the silicon film located on the first active region being covered with a second mask pattern; and (d) patterning the silicon film after steps (b) and (c), thereby forming the first gate electrode, the second gate electrode, the third gate electrode, and the fourth gate electrode including the silicon film on the first active region, the second active region, the third active region, and the fourth active region, respectively. In the method for fabricating a semiconductor device, step (b) and step (c) may be performed in any order.

In the method for fabricating a semiconductor device, the first mask pattern may expose a portion of the silicon film located on the first active region, and the second mask pattern may expose portions of the silicon film located on the second active region, the third active region, and the fourth active region.

In the method for fabricating a semiconductor device, the first active region and the second active region are electrically isolated from each other by an isolation region. In step (a), the silicon film may also be formed on the isolation region, the first mask pattern may cover a portion of the silicon film located on the first active region and expose a portion of the silicon film located on the isolation region, and the second mask pattern may cover a portion of the silicon film located on the second active region and expose portions of the silicon film located on the isolation region, the third active region, and the fourth active region. The first mask pattern and the second mask pattern do not need to expose a portion of the silicon film located on the isolation region. In other words, the first mask pattern and the second mask pattern may cover a portion of the silicon film located on the isolation region.

In the method for fabricating a semiconductor device, the first active region and the second active region may be electrically isolated from each other by an isolation region. In step (a), the silicon film may also be formed on the isolation region, the first mask pattern may cover a portion of the silicon film located on the first active region and expose a portion of the silicon film located on the isolation region, and the second mask pattern may cover portions of the silicon film located on the second active region, the third active region, and the fourth active region and expose a portion of the silicon film located on the isolation region.

In the method for fabricating a semiconductor device, the second mask pattern may cover portions of the silicon film located on the third active region and the fourth active region.

According to the present disclosure described above, it is possible to reduce a variation in transistor characteristics due to a variation in gate dimensions near a PN boundary and mutual diffusion of impurities in a semiconductor device with a CMIS dual-gate structure. Thus, the present disclosure is useful for semiconductor devices with CMIS dual-gate structures and methods for fabricating such semiconductor devices.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A is a plan view illustrating a logic area of a semiconductor device according to a first embodiment, FIG. **1**B is a cross-sectional view taken along the line I-I in FIG. **1**A, FIG. **1**C is a plan view illustrating an SRAM area of the semiconductor device of the first embodiment, and FIG. **1**D is a cross-sectional view taken along the line II-II in FIG. **1**C.

FIGS. **2**A-**2**F are cross-sectional views showing a process step of a method for fabricating a semiconductor device according to the first embodiment.

FIGS. **3**A-**3**F are cross-sectional views showing a process step of the method for fabricating a semiconductor device of the first embodiment.

FIGS. **4**A-**4**F are cross-sectional views showing a process step of the method for fabricating a semiconductor device of the first embodiment.

FIGS. **5**A-**5**F are cross-sectional views showing a process step of the method for fabricating a semiconductor device of the first embodiment.

FIGS. **6**A-**6**F are cross-sectional views showing a process step of the method for fabricating a semiconductor device of the first embodiment.

FIGS. **7**A-**7**F are cross-sectional views showing a process step of the method for fabricating a semiconductor device of the first embodiment.

FIGS. **8**A-**8**F are cross-sectional views showing a process step of the method for fabricating a semiconductor device of the first embodiment.

FIG. **9**A is a plan view illustrating a logic area of a semiconductor device according to a second embodiment, FIG. **9**B is a cross-sectional view taken along the line I-I in FIG. **9**A, FIG. **9**C is a plan view illustrating an SRAM area of the semiconductor device of the second embodiment, and FIG. **9**D is a cross-sectional view taken along the line II-II in FIG. **9**C.

FIGS. **10**A-**10**F are cross-sectional views showing a process step of a method for fabricating a semiconductor device according to the second embodiment.

FIG. **11**A is a plan view illustrating a logic area of a semiconductor device according to a third embodiment, FIG. **11**B is a cross-sectional view taken along the line I-I in FIG. **11**A, FIG. **11**C is a plan view illustrating an SRAM area of the semiconductor device of the third embodiment, and FIG. **11**D is a cross-sectional view taken along the line II-II in FIG. **11**C.

FIGS. **12**A-**12**F are cross-sectional views showing a process step of a method for fabricating a semiconductor device according to the third embodiment.

FIG. **13**A is a plan view illustrating a logic area of a semiconductor device according to a fourth embodiment, FIG. **13**B is a cross-sectional view taken along the line I-I in FIG. **13**A, FIG. **13**C is a plan view illustrating an SRAM area of the semiconductor device of the fourth embodiment, and FIG. **13**D is a cross-sectional view taken along the line II-II in FIG. **13**C.

FIGS. **14**A-**14**F are cross-sectional views showing a process step of a method for fabricating a semiconductor device according to the fourth embodiment.

FIG. **15**A is a plan view illustrating a logic area of a conventional semiconductor device, FIG. **15**B is a cross-sectional view taken along the line B-B in FIG. **15**A, FIG. **15**C is a plan view illustrating an SRAM area of the conventional semiconductor device, and FIG. **15**D is a cross-sectional view taken along the line D-D in FIG. **15**C.

FIGS. **16**A and **16**B are views schematically illustrating formation of p-type regions and n-type regions by implanting ions of an impurity into a polysilicon film (before gate patterning) to be a dual-gate electrode in a conventional method for fabricating a semiconductor device.

DETAILED DESCRIPTION

First Embodiment

A semiconductor device according to a first embodiment of the present disclosure will be described with reference to the drawings.

FIG. **1**A is a plan view illustrating a logic area of a semiconductor device according to the first embodiment. FIG. **1**B is a cross-sectional view taken along the line I-I (along the gate width) in FIG. **1**A. FIG. **1**C is a plan view illustrating an SRAM area of the semiconductor device of the first embodiment. FIG. **1**D is a cross-sectional view taken along the line II-II (along the gate width) in FIG. **1**C. In FIGS. **1**A-**1**D, sidewall spacers, a silicide layer, and an interlayer film, for example, are not shown for simplicity, and contacts are not shown in FIGS. **1**B and **1**D.

As illustrated in FIGS. **1**A-**1**D, the semiconductor device of this embodiment includes an area where a logic circuit is to be formed (hereinafter referred to as a logic area) and an area where an SRAM circuit is to be formed (hereinafter referred to as an SRAM area). Each of the logic area and the SRAM area includes a region where an NMISFET is to be formed (hereinafter referred to as an NMIS region) and a region where a PMISFET is to be formed (hereinafter referred to as a PMIS region). In the NMIS region in the logic area, a p-well region **12***a* is provided on a semiconductor substrate **10**, and an active region **10***a* is surrounded by an isolation region **11**. In the PMIS region in the logic area, an n-well region **12***b* is provided on the semiconductor substrate **10**, and an active region **10***b* is surrounded by the isolation region **11**. In the NMIS region in the SRAM area, a p-well region **12***c* is provided on the semiconductor substrate **10**, and an active region **10***c* is surrounded by the isolation region **11**. In the PMIS region in the SRAM area, an n-well region **12***d* is provided on the semiconductor substrate **10**, and an active region **10***d* is surrounded by the isolation region **11**.

On the active region **10***a*, a gate electrode **30***a* including an n-type silicon film **14***a* is formed with a gate insulating film **13** interposed therebetween. On the active region **10***b*, a gate electrode **30***b* including a p-type silicon film **14***b* is formed with the gate insulating film **13** interposed therebetween. The gate electrode **30***a* and the gate electrode **30***b* are connected to each other at a PN boundary **41**L between the active region **10***a* and the active region **10***b* on the isolation region **11**, thereby forming a dual-gate electrode **31**L. N-type source/drain regions **20***a* are defined at both sides of the gate electrode **30***a* in the active region **10***a*. P-type source/drain regions **20***b* are defined at both sides of the gate electrode **30***b* in the active region **10***b*. Contacts **26***a* and **26***b* are formed to be connected to the n-type source/drain regions **20***a* and the p-type source/drain regions **20***b*, and a contact **26***e* is formed to be connected to the dual-gate electrode **31**L.

On the active region **10***c*, a gate electrode **30***c* including an n-type silicon film **14***c* is formed with the gate insulating film **13** interposed therebetween. On the active region **10***d*, a gate electrode **30***d* including a p-type silicon film **14***d* is formed with the gate insulating film **13** interposed therebetween. The gate electrode **30***c* and the gate electrode **30***d* are connected to each other at a PN boundary **41**S between the active region **10***c* and the active region **10***d* on the isolation region **11**, thereby forming a dual-gate electrode **31**S, N-type source/drain regions **20***c* are defined at both sides of the gate electrode **30***c* in the active region **10***c*. P-type source/drain regions **20***d* are defined at both sides of the gate electrode **30***d* in the active region **10***d*. Contacts **26***c* and **26***d* are formed to be connected to the n-type source/drain regions **20***c* and the p-type source/drain regions **20***d*, and a contact **26***f* is formed to be connected to the gate electrode **30***c*.

A feature of this embodiment is that the p-type impurity concentration in the entire p-type silicon film **14***b* is higher than that in the entire p-type silicon film **14***d*.

The n-type impurity concentration of the n-type silicon film **14***a* is substantially equal to that of the n-type silicon film **14***c*. The width of the isolation region **11** (specifically a portion of the isolation region **11** between the active region **10***a* and the active region **10***b*) in the logic area is, for example, about 70 nm or more, whereas the width of the isolation region **11** (specifically a portion of the isolation region **11** between the active region **10***c* and the active region **10***d*) in the SRAM area is, for example, about 30-60 nm.

A method for fabricating a semiconductor device according to the first embodiment will be described hereinafter with reference to the drawings.

FIGS. **2**A-**2**F, **3**A-**3**F, **4**A-**4**F, **5**A-**5**F, **6**A-**6**F, **7**A-**7**F, and **8**A-**8**F are cross-sectional views illustrating process steps of a method for fabricating a semiconductor device according to the first embodiment. FIGS. **2**A, **3**A, **4**A, **5**A, **6**A, **7**A, and **8**A illustrate cross-sectional structures taken along the line III-III (along the gate length) in FIG. **1**A in respective process steps.

FIGS. **2**B, **3**B, **4**B, **5**B, **6**B, **7**B, and **8**B illustrate cross-sectional structures taken along the line IV-IV (along the gate length) in FIG. **1**A in the respective process steps. FIGS. **2**C, **3**C, **4**C, **5**C, **6**C, **7**C, and **8**C illustrate cross-sectional structures taken along the line V-V (along the gate length) in FIG. **1**C in the respective process steps. FIGS. **2**D, **2**D, **3**D, **4**D, **5**D, **6**D, **7**D, and **8**D illustrate cross-sectional structures taken along the line VI-VI (along the gate length) in FIG. **1**C in the respective process steps. FIGS. **2**E, **3**E, **4**E, **5**E, **6**E, **7**E, and **8**E illustrate cross-sectional structures taken along the line I-I (along the gate width) in FIG. **1**A in the respective process steps. FIGS. **2**F, **3**F, **4**F, **5**F, **6**F, **7**F, and **8**F illustrate cross-sectional structures taken along the line II-II (along the gate width) in FIG. **1**C in the respective process steps.

First, as illustrated in FIGS. **2**A-**2**F, an isolation region **11** formed by filling a trench with an insulating film is selectively formed in an upper portion of a semiconductor substrate **10** of, for example, p-type silicon by a method such as shallow trench isolation (STI). Accordingly, in the NMIS region in the logic area, an active region **10***a* is formed in a portion of the semiconductor substrate **10** surrounded by the isolation region **11**. In the PMIS region in the logic area, an active region **10***b* is formed in a portion of the semiconductor substrate **10** surrounded by the isolation region **11**. In the NMIS region in the SRAM area, an active region **10***c* is formed in a portion of the semiconductor substrate **10** surrounded by the isolation region **11**. In the PMIS region in the SRAM area, an active region **10***d* is formed in a portion of the semiconductor substrate **10** surrounded by the isolation region **11**. Thereafter, a p-type impurity such as boron (B) is implanted into each of the NMIS regions of the semiconductor substrate **10** by, for example, lithography and ion implantation. Subsequently, an n-type impurity such as phosphorus (P) is implanted into each of the PMIS regions of the semiconductor substrate **10** by, for example, lithography and ion implantation. Then, the semiconductor substrate **10** is subjected to heat treatment at 850° C. for 30 seconds, for example, thereby forming a p-well region **12***a* on the semiconductor substrate **10** in the NMIS region in the logic area, an n-well region **12***b* on the semiconductor substrate **10** in the PMIS region in the logic area, a p-well region **12***c* on the semiconductor substrate **10** in the NMIS region in the SRAM area, and an n-well region **12***d* on the semiconductor substrate **10** in the PMIS region in the SRAM area.

Next, as illustrated in FIGS. **3**A-**3**F, the surface of the semiconductor substrate **10** is cleaned with diluted hydrogen fluoride, and then a gate insulating film **13** of a silicon dioxide film with a thickness of, for example, about 2 nm is formed by in-situ steam generation (ISSG) oxidation on the active regions **10***a*, **10***b*, **10***c*, and **10***d*. Thereafter, the semiconductor substrate **10** is subjected to, for example, a nitrogen plasma process, thereby nitriding the surface of the gate insulating film **13** to form a nitrided layer (not shown). Then, annealing is performed, thereby removing nitrogen atoms with weak bonds from the nitrided layer. Subsequently, a silicon film **14** of, for example, polysilicon with a thickness of about 100 nm is deposited by, for example, chemical vapor deposition (CVD) over the gate insulating film **13**.

Then, as illustrated in FIGS. **3**A-**3**F, with a mask pattern **51**A covering the entire NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the entire PMIS region in the logic area, ions of a p-type impurity such as boron (B) are implanted into the silicon film **14** at a dose of 4×10^{15} cm^{-2}, thereby forming a p-type silicon film **14**P. Thereafter, with a mask pattern **52**A covering the entire PMIS region in the logic area and exposing the entire NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area), ions of an n-type impurity such as phosphorus (P) are implanted into the silicon film **14** at a dose of 3×10^{15} cm^{-2}, thereby forming an n-type silicon film **14**N. That is, as a feature of this embodiment, ions of the n-type impurity are implanted in the gate injection for the PMIS region in the SRAM area.

Formation of the p-type silicon film **14**P and formation of the n-type silicon film **14**N may be performed in any order. In FIGS. **3**A-**3**F, not resist patterns formed on the semiconductor substrate **10** by photolithography but mask patterns on photomasks for forming these resist patterns are schematically shown as the mask patterns **51**A and **52**A for simplicity. The mask patterns **51**A and **52**A are designed such that the PN boundary **41**L between the p-type silicon film **14**P and the n-type silicon film **14**N is located on a portion of the isolation region **11** between the active region **10***a* and the active region **10***b*.

After formation of the p-type silicon film **14**P and the n-type silicon film **14**N, the semiconductor substrate **10** is subjected to heat treatment at 850° C. for 30 seconds, for example, thereby uniformizing a profile (specifically a profile vertical to the principal surface of the substrate, hereinafter referred to as a vertical profile) of an impurity implanted in the form of ions into each of the p-type silicon film **14**P and the n-type silicon film **14**N.

Thereafter, a resist pattern (not shown) having a gate shape is formed by photolithography on the silicon film **14**, and then using the resist pattern as a mask, the silicon film **14** is patterned by dry etching. In this manner, as illustrated in FIGS. **4**A-**4**F, a gate electrode **30***a* including an n-type silicon film **14***a* is formed on the active region **10***a* with a gate insulating film **13***a* interposed therebetween, a gate electrode **30***b* including a p-type silicon film **14***b* is formed on the active region **10***b* with a gate insulating film **13***b* interposed therebetween, a gate electrode **30***c* including an n-type silicon film **14***c* is formed on the active region **10***c* with a gate insulating film **13***c* interposed therebetween, and a gate electrode **30***d* including an n-type silicon film **14***d* is formed on the active region **10***d* with a gate insulating film **13***d* interposed therebetween. The gate electrode **30***a* and the gate electrode **30***b* are connected to each other at the PN boundary **41**L between the active region **10***a* and the active region **10***b* on the isolation region **11**, thereby forming a dual-gate electrode **31**L. The gate electrode **30***c* and the gate electrode **30***d* are connected to each other on a portion of the isolation region **11** between the active region **10***c* and the active region **10***d*, thereby forming a dual-gate electrode **31**S. At the end of the process step shown in FIGS. **4**A-**4**F, no PN boundary is formed in the dual-gate electrode **31**S.

Subsequently, an insulating film for offset spacers of, for example, a silicon dioxide film with a thickness of 8 nm is deposited by, for example, CVD over the entire surface of the semiconductor substrate **10**, and then the insulating film for offset spacers is subjected to anisotropic etching. In this manner, as illustrated in FIGS. **5**A-**5**F, offset spacers **15***a* are formed on side surfaces of the gate insulating film **13***a* and the gate electrode **30***a*, offset spacers **15***b* are formed on side surfaces of the gate insulating film **13***b* and the gate electrode **30***b*, offset spacers **15***c* are formed on side surfaces of the gate insulating film **13***c* and the gate electrode **30***c*, and offset spacers **15***d* are formed on side surfaces of the gate insulating film **13***d* and the gate electrode **30***d*.

Then, a resist pattern (not shown) exposing each NMIS region and covering each PMIS region is formed on the semiconductor substrate **10**, and then, using the resist pattern and

the gate electrodes **30***a* and **30***c* as masks, ions of an n-type impurity such as arsenic (As) are implanted. With this process, as illustrated in FIGS. **5**A-**5**D, n-type source/drain regions (e.g., lightly doped drain (LDD) regions or extension regions) **16***a* and **16***c* having relatively shallow junction depths are defined in a self-aligned manner in portions of the active region **10***a* below the sides of the gate electrode **30***a* and in portions of the active region **10***c* below the sides of the gate electrode **30***c*. Subsequently, a resist pattern (not shown) covering each NMIS region and exposing each PMIS region is formed on the semiconductor substrate **10**, and using the resist pattern and the gate electrodes **30***b* and **30***d* as masks, ions of a p-type impurity such as BF_2 are implanted. With this process, as illustrated in FIGS. **5**A-**5**D, p-type source/drain regions (e.g., LDD regions or extension regions) **16***b* and **16***d* having relatively shallow junction depths are defined in a self-aligned manner in portions of the active region **10***b* below the sides of the gate electrode **30***b* and portions of the active region **10***d* below the sides of the gate electrode **30***d*.

Formation of the n-type source/drain regions **16***a* and **16***c* and formation of the p-type source/drain regions **16***b* and **16***d* may be performed in any order.

Then, a first insulating film of, for example, a silicon dioxide film with a thickness of about 10 nm and a second insulating film of, for example, a silicon nitride film with a thickness of about 30 nm are deposited in this order by, for example, CVD over the entire surface of the semiconductor substrate **10**, and then the first insulating film and the second insulating film are subjected to anisotropic etching. In this manner, as illustrated in FIGS. **6**A-**6**F, sidewall spacers **19***a* are formed on side surfaces of the gate electrode **30***a* with the offset spacers **15***a* interposed therebetween, sidewall spacers **19***b* are formed on side surfaces of the gate electrode **30***b* with the offset spacers **15***b* interposed therebetween, sidewall spacers **19***c* are formed on side surfaces of the gate electrode **30***c* with the offset spacers **15***c* interposed therebetween, and sidewall spacers **19***d* are formed on side surfaces of the gate electrode **30***d* with the offset spacers **15***d* interposed therebetween. Each of the sidewall spacers **19***a* includes an inner sidewall **17***a* having an L shape in cross section and made of the first insulating film and an outer sidewall **18***a* located on the inner sidewall **17***a* and made of the second insulating film. Each of the sidewall spacers **19***b* includes an inner sidewall **17***b* having an L shape in cross section and made of the first insulating film and an outer sidewall **18***b* located on the inner sidewall **17***b* and made of the second insulating film. Each of the sidewall spacers **19***c* includes an inner sidewall **17***c* having an L shape in cross section and made of the first insulating film and an outer sidewall **18***c* located on the inner sidewall **17***c* and made of the second insulating film. Each of the sidewall spacers **19***d* includes an inner sidewall **17***d* having an L shape in cross section and made of the first insulating film and an outer sidewall **18***d* located on the inner sidewall **17***d* and made of the second insulating film.

Subsequently, as illustrated in FIGS. **6**A-**6**F, using a mask pattern **53** covering the entire NMIS region in the logic area and the entire NMIS region in the SRAM area, the gate electrode **30***b*, the offset spacers **15***b*, and the sidewall spacers **19***b* in the active region **10***b*, and the gate electrode **30***d*, the offset spacers **15***d*, and the sidewall spacers **19***d* in the active region **10***d* as mask, ions of a p-type impurity such as boron (B) are implanted into the active region **10***b* and the active region **10***d* at a dose of 5×10^{15} cm^{-2}. In this manner, p-type source/drain regions **20***b* having a junction depth deeper than that of the shallow p-type source/drain regions **16***b* and connected to the p-type source/drain regions **16***b* are defined in a self-aligned manner below the outer sides of the sidewall spacers **19***b* in the active region **10***b*, and p-type source/drain regions **20***d* having a junction depth deeper than that of the shallow p-type source/drain regions **16***d* and connected to the p-type source/drain regions **16***d* are defined in a self-aligned manner below the outer sides of the sidewall spacers **19***d* in the active region **10***d*. In this process step, the p-type impurity is also implanted into the p-type silicon film **14***b* forming the gate electrode **30***b* and the n-type silicon film **14***d*' forming the gate electrode **30***d*, thereby increasing the p-type impurity concentration of the p-type silicon film **14***b* and changing the n-type silicon film **14***d*' into the p-type silicon film **14***d*. In this manner, a PN boundary **41**S between the n-type silicon film **14***c* (the gate electrode **30***c*) and the p-type silicon film n **14***d* (the gate electrode **30***d*) is formed in the dual-gate electrode **31**S. At this time, the p-type impurity concentration of the p-type silicon film **14***b* is higher than that of the p-type silicon film **14***d*.

Thereafter, as illustrated in FIGS. **6**A-**6**F, using a mask pattern **54** covering the entire PMIS region in the logic area and the entire PMIS region in the SRAM area, the gate electrode **30***a*, the offset spacers **15***a*, and the sidewall spacers **19***a* in the active region **10***a*, and the gate electrode **30***c*, the offset spacers **15***c*, and the sidewall spacers **19***c* in the active region **10***c* as masks, ions of an n-type impurity such as arsenic (As) are implanted into the active region **10***a* and the active region **10***c* at a dose of 4×10^{15} to 5×10^{15} cm^{-2}. In this manner, n-type source/drain regions **20***a* having a junction depth deeper than that of the shallow n-type source/drain regions **16***a* and connected to the n-type source/drain regions **16***a* are defined in a self-aligned manner below the outer sides of the sidewall spacers **19***a* in the active region **10***a*, and n-type source/drain regions **20***c* having a junction depth deeper than that of the shallow n-type source/drain regions **16***c* and connected to the n-type source/drain regions **16***c* are defined in a self-aligned manner below the outer sides of the sidewall spacers **19***c* in the active region **10***c*.

Formation of the p-type source/drain regions **20***b* and **20***d* and formation of the n-type source/drain regions **20***a* and **20***c* may be performed in any order. In FIGS. **6**A-**6**F, not resist patterns formed by photolithography on the semiconductor substrate **10** but mask patterns on photomasks for forming the resist patterns are schematically shown as the mask patterns **53** and **54** for simplicity. The mask patterns **53** and **54** are designed such that the location (i.e., on a portion of the isolation region **11** between the active region **10***a* and the active region **10***b*) of the PN boundary **41**L between the p-type silicon film **14***a* (the gate electrode **30***a*) and the n-type silicon film **14***b* (the gate electrode **30***b*) is not changed and that the PN boundary **41**S between the p-type silicon film **14***c* (the gate electrode **30***c*) and the n-type silicon film **14***d* (the gate electrode **30***d*) is located on a portion of the isolation region **11** between the active region **10***c* and the active region **10***d*.

After formation of the n-type source/drain regions **20***a* and **20***c* and the p-type source/drain regions **20***b* and **20***d*, the semiconductor substrate **10** is subjected to heat treatment, thereby activating the impurities implanted into the n-type source/drain regions **20***a* and **20***c* and the p-type source/drain regions **20***b* and **20***d*.

Then, natural oxide films (not shown) on the surfaces of the deep n-type source/drain regions **20***a* and **20***c* and the deep p-type source/drain regions **20***b* and **20***d* are removed, and then a metal film (not shown) of, for example, nickel with a thickness of about 10 nm is deposited by, for example, sputtering over the entire surface of the semiconductor substrate **10**. Thereafter, first rapid thermal annealing (RTA) is performed on the semiconductor substrate **10** at, for example,

320° C. in, for example, a nitrogen atmosphere, thereby causing silicon (Si) in surface portions of the deep n-type source/drain regions **20***a* and **20***c* and the deep p-type source/drain regions **20***b* and **20***d* and nickel (Ni) in the metal film to react with each other. In this manner, as illustrated in FIGS. **7**A-**7**F, metal silicide layers **21***a*-**21***d* of nickel silicide are formed on the deep n-type source/drain regions **20***a* and **20***c* and the deep p-type source/drain regions **20***b* and **20***d*. In this process step, Si in surface portions of the n-type silicon films **14***a* and **14***c* constituting the gate electrode **30***a* and **30***c* and the p-type silicon films **14***b* and **14***d* constituting the gate electrodes **30***b* and **30***d* also reacts with Ni in the metal film, thereby forming metal silicide layers **22***a*-**22***d* of nickel silicide on the gate electrodes **30***a*-**30***d*. Subsequently, the semiconductor substrate **10** is immersed in an etchant of a mixed solution of, for example, sulfuric acid and a hydrogen peroxide solution, thereby removing unreacted portions of the metal film remaining on, for example, the isolation region **11**, the offset spacers **15***a*-**15***d*, and the sidewall spacers **19***a*-**19***d*. Then, second RTA is performed at a temperature (e.g., 550° C.) higher than that in the first RTA, thereby stabilizing the silicide content in each of the metal silicide layers **21***a*-**21***d* and the metal silicide layers **22***a*-**22***d*.

Thereafter, as illustrated in FIGS. **8**A-**8**F, an insulating film **23** of, for example, a silicon nitride film a thickness of about 20 nm is deposited by, for example, plasma CVD over the entire surface of the semiconductor substrate **10**. Then, an interlayer insulating film **24** of, for example, a silicon dioxide film is deposited by, for example, CVD over the insulating film **23**. Subsequently, the surface of the interlayer insulating film **24** is planarized by, for example, chemical mechanical polishing (CMP). Then, as in a method for fabricating a semiconductor device with a general MIS transistor, a resist film (not shown) having a contact hole pattern is formed on the interlayer insulating film **24**, and using the resist film as a mask, contact holes **25***a*-**25***d* are formed by dry etching in the insulating film **23** and the interlayer insulating film **24** such that the contact holes **25***a*-**25***d* reach the upper surfaces of the metal silicide layers **21***a*-**21***d*, respectively. In this process step, a two-step etching process in which etching is temporarily stopped when the insulating film **23** is exposed is employed, thereby reducing the amount of overetching of the metal silicide layers **21***a*-**21***d*. Thereafter, a barrier metal film (not shown) as a stack of, for example, a titanium film and a titanium nitride film is formed by, for example, sputtering or CVD on each of the bottoms and side surfaces of the contact holes **25***a*-**25***d*. Subsequently, a tungsten film, for example, is deposited by CVD over the interlayer insulating film **24** to fill the contact holes **25***a*-**25***d*, and then portions of the tungsten film located outside the contact holes **25***a*-**25***d* are removed by, for example, CMP. In this manner, contacts **26***a*-**26***d* in each of which the tungsten film is buried with the barrier metal film interposed between the contact hole and the tungsten film are formed in the contact holes **25***a*-**25***d*. Thereafter, metal interconnects (not shown) electrically connected to the contacts **26***a*-**26***d* are formed on the interlayer insulating film **24**.

In the foregoing manner, the semiconductor device of this embodiment, i.e., the semiconductor device including: an NMISFET located in the logic area and including the gate electrode **30***a* having the n-type silicon film **14***a*; a PMISFET located in the logic area and including the gate electrode **30***b* having the p-type silicon film **14***b*; an NMISFET located in the SRAM area and including the gate electrode **30***c* having the n-type silicon film **14***c*; and a PMISFET located in the SRAM area and including the gate electrode **30***d* having the p-type silicon film **14***d*, can be fabricated.

In this embodiment, in forming the gate electrodes **30***a*-**30***d* by dry-etching the silicon film **14**, substantially only the n-type impurity is present in portions of the silicon film **14** constituting the gate electrodes **30***c* and **30***d* in the SRAM area susceptible to the influence of mutual diffusion of the impurities because of a small width of the isolation region **11** (specifically a portion of the isolation region **11** between the active region **10***c* and the active region **10***d*). Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film **14** caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode **30***c* of the NMISFET and the gate electrode **30***d* of the PMISFET, thereby reducing variations in transistor characteristics due to variations in gate length. In addition, in dry-etching the silicon film **14**, it is necessary to uniformize the vertical profile of an impurity implanted into the silicon film **14** beforehand by annealing. However, in this embodiment, since substantially only an n-type impurity is present in a portion of the silicon film **14** located in the SRAM area at the time when the silicon film **14** is etched, the influence of mutual diffusion (specifically diffusion in the direction parallel to the principal surface of the substrate) of the impurities due to the annealing is substantially negligible. As a result, variations in transistor characteristics can be further reduced.

In this embodiment, in an a portion of the silicon film **14** constituting the gate electrode **30***d* of the PMIS region in the SRAM area, the n-type impurity is implanted in the gate injection, whereas the p-type impurity is implanted in source/drain implantation. Accordingly, to form the PMISFET in the SRAM area as a surface channel type, the n-type impurity concentration in the gate injection is preferably lower than the p-type impurity concentration in the source/drain implantation. In this case, as a feature of this embodiment, the p-type impurity concentration of the p-type silicon film **14***b* constituting the gate electrode **30***b* in the PMIS region in the logic area is higher than that of the p-type silicon film **14***d* in constituting the gate electrode **30***d* in the PMIS region in the SRAM area.

In this embodiment, gate injection of the n-type impurity is performed on the NMIS region and the PMIS region in the SRAM area, and then source/drain implantation of the p-type impurity is performed, thereby reversing the conductivity type of a portion of the silicon film **14** constituting the gate electrode **30***d* in the PMIS region in the SRAM area to the p-type. Alternatively, the conductivity type of a portion of the silicon film **14** constituting the gate electrode **30***c* in the NMIS region in the SRAM area may be reversed to the n-type by performing gate injection of the p-type impurity on the NMIS region and the PMIS region in the SRAM area and then performing source/drain implantation of the n-type impurity.

Second Embodiment

A semiconductor device according to a second embodiment of the present disclosure will be described hereinafter with reference to the drawings.

FIG. **9**A is a plan view illustrating a logic area of the semiconductor device of the second embodiment. FIG. **9**B is a cross-sectional view taken along the line I-I (along the gate width) in FIG. **9**A. FIG. **9**C is a plan view illustrating an SRAM area of the semiconductor device of the second embodiment. FIG. **9**D is a cross-sectional view taken along the line II-II (along the gate width) in FIG. **9**C. In FIGS. **9**A-**9**D, sidewall spacers, a silicide layer, and an interlayer film, for example, are not shown for simplicity, and contacts are not shown in FIGS. **9**B and **9**D. In FIGS. **9**A-**9**D, compo-

nents already shown in FIGS. **1**A-**1**D for the first embodiment are denoted by the same reference characters, and descriptions thereof will not be repeated and only different characteristics will be described hereinafter.

The second embodiment is different from the first embodiment in the following aspects. As illustrated in FIGS. **9**A and **9**B, a dual-gate electrode **31**L in a logic area includes: a gate electrode **30***a* located in an NMIS region and including an n-type silicon film **14***a***1** provided on an active region **10***a* and a portion of an isolation region **11** near the active region **10***a* and an n-type silicon film **14***a***2** provided on portions of the isolation region **11** at both ends of the n-type silicon film **14***a***1**; and a gate electrode **30***b* located on a PMIS region and including a p-type silicon film **14***b***1** provided on an active region **10***b* and a portion of the isolation region **11** near the active region **10***b* and a p-type silicon film **14***b***2** provided on portions of the isolation region **11** at both ends of the p-type silicon film **14***b***1**.

The configuration of the SRAM area illustrated in FIGS. **9**C and **9**D including the structure of a dual-gate electrode **31**S is the same as that in the SRAM area of the first embodiment illustrated in FIGS. **1**C and **1**D. Specifically, in the same manner as in the first embodiment, the dual-gate electrode **31**S includes a gate electrode **30***c* located on an NMIS region and including an n-type silicon film **14***c* and a gate electrode **30***d* located on a PMIS region and including a p-type silicon film **14***d*.

A feature of this embodiment is that the p-type silicon film **14***b***1** has a p-type impurity concentration lower than that of the p-type silicon film **14***b***2**. In addition, each of the p-type silicon film **14***b***1** and the p-type silicon film **14***b***2** has a p-type impurity concentration higher than that of the p-type silicon film **14***d*. The n-type silicon film **14***a***1** has an n-type impurity concentration lower than that of each of the n-type silicon film **14***a***2** and the n-type silicon film **14***c*. The n-type silicon film **14***a***2** has an n-type impurity concentration substantially equal to that of the n-type silicon film **14***c*.

A method for fabricating a semiconductor device according to the second embodiment will be described hereinafter with reference to the drawings. The method for fabricating a semiconductor device of this embodiment is different from that of the first embodiment only in the location of gate injection in the logic area (see FIGS. **10**A-**10**F).

FIGS. **10**A-**10**F are cross-sectional views illustrating a process step of the method for fabricating a semiconductor device of the second embodiment. FIG. **10**A illustrates a cross-sectional structure in the process step taken along the line III-III (along the gate length) in FIG. **9**A. FIG. **10**B illustrates a cross-sectional structure in the process step taken along the line IV-IV (along the gate length) in FIG. **9**A. FIG. **10**C illustrates a cross-sectional structure in the process step taken along the line V-V (along the gate length) in FIG. **9**C. FIG. **10**D illustrates a cross-sectional structure in the process step taken along the line VI-VI (along the gate length) in FIG. **9**C. FIG. **10**E illustrates a cross-sectional structure in the process step taken along the line I-I (along the gate width) in FIG. **9**A. FIG. **10**F illustrates a cross-sectional structure in the process step taken along the line II-II (along the gate width) in FIG. **9**C.

In this embodiment, first, the same process step as that of the first embodiment illustrated in FIGS. **2**A-**2**F is performed. Thereafter, as illustrated in FIGS. **10**A-**10**F, the surface of a semiconductor substrate **10** is cleaned with, for example, diluted hydrogen fluoride, and then a gate insulating film **13** of, for example, a silicon dioxide film with a thickness of about 2 nm is deposited by, for example, ISSG oxidation on the active regions **10***a*, **10***b*, **10***c*, and **10***d*. Subsequently, the semiconductor substrate **10** is subjected to, for example, a nitrogen plasma process, thereby nitriding the surface of the gate insulating film **13** to form a nitrided layer (not shown). Then, annealing is performed, thereby removing nitrogen atoms with weak bonds from the nitrided layer. Subsequently, a silicon film **14** of, for example, polysilicon with a thickness of about 100 nm is deposited by, for example, CVD over the gate insulating film **13**.

Then, as illustrated in FIGS. **10**A-**10**F, with a mask pattern **51**B covering the entire NMIS region and the active region **10***b* in the PMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the isolation region **11** in the PMIS region in the logic area, ions of a p-type impurity such as boron (B) are implanted into the silicon film **14** at a dose of 4×10^{15} cm^{-2}, thereby forming a p-type silicon film **14**P on a portion of the isolation region **11** in the PMIS region in the logic area. In this process step, the length (e.g., about 50 nm) of a portion of the isolation region **11** covered with the mask pattern **51**B near the active region **10***b* in the PMIS region in the logic area is determined in consideration of the influence of mutual diffusion of the impurities. Thereafter, with a mask pattern **52**B covering the entire PMIS region and the active region **10***a* in the NMIS region in the logic area and exposing the isolation region **11** in the NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area), ions of an n-type impurity such as phosphorus (P) are implanted into the silicon film **14** at a dose of 3×10^{15} cm^{-2}, thereby forming an n-type silicon film **14**N on a portion of the isolation region **11** located in the NMIS region in the logic area and the entire SRAM area. In this process step, the length (e.g., about 50 nm) of a portion of the isolation region **11** covered with the mask pattern **51**B near the active region **10***a* in the NMIS region in the logic area is determined in consideration of the influence of mutual diffusion of the impurities. That is, in this embodiment, ions of the n-type impurity are implanted in gate injection for the PMIS region in the SRAM area in the same manner as in the first embodiment.

Formation of the p-type silicon film **14**P and formation of the n-type silicon film **14**N may be performed in any order. In FIGS. **10**A-**10**F, not resist patterns formed on the semiconductor substrate **10** by photolithography but mask patterns on photomasks for forming these resist patterns are schematically shown as the mask patterns **51**B and **52**B for simplicity. The mask patterns **51**B and **52**B are designed such that a PN boundary **41**L between the p-type silicon film **14**P and the n-type silicon film **14**N is located on a portion of the isolation region **11** between the active region **10***a* and the active region **10***b*.

After formation of the p-type silicon film **14**P and the n-type silicon film **14**N, the semiconductor substrate **10** is subjected to heat treatment at 850° C. for 30 seconds, for example, thereby uniformizing a vertical profile of an impurity implanted as ions into each of the p-type silicon film **14**P and the n-type silicon film **14**N.

Thereafter, process steps similar to the process step (gate patterning) illustrated in FIGS. **4**A-**4**F, the process step (formation of offset spacers and shallow source/drain regions) illustrated in FIGS. **5**A-**5**F, the process step (formation of sidewall spacers and deep source/drain regions) illustrated in FIGS. **6**A-**6**F, the process step (formation of a silicide layer) illustrated in FIGS. **7**A-**7**F, and the process step (formation of an interlayer insulating film and a contact silicide layer) illustrated in FIGS. **8**A-**8**F of the first embodiment are performed in order.

In the foregoing manner, the semiconductor device of this embodiment, i.e., the semiconductor device including: an NMISFET located in the logic area and including the gate electrode **30***a* having the n-type silicon films **14***a***1** and **14***a***2**; a PMISFET located in the logic area and including the gate electrode **30***b* having the p-type silicon films **14***b***1** and **14***b***2**; an NMISFET located in the SRAM area and including the gate electrode **30***c* having the n-type silicon film **14***c*; and a PMISFET located in the SRAM area and including the gate electrode **30***d* having the p-type silicon film **14***d*, can be fabricated.

In this embodiment, in forming the gate electrodes **30***a*-**30***d* by dry-etching the silicon film **14**, substantially only the n-type impurity is present in portions of the silicon film **14** constituting the gate electrodes **30***c* and **30***d* in the SRAM area susceptible to the influence of mutual diffusion of the impurities because of a small width of the isolation region **11** (specifically a portion of the isolation region **11** between the active region **10***c* and the active region **10***d*). Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film **14** caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode **30***c* of the NMISFET and the gate electrode **30***d* of the PMISFET, thereby reducing variations in transistor characteristics due to variations in gate length. In addition, in dry-etching the silicon film **14**, it is necessary to uniformize the vertical profile of an impurity implanted into the silicon film **14**. However, in this embodiment, since substantially only the n-type impurity is present in a portion of the silicon film **14** located in the SRAM area at the time when the silicon film **14** is etched in the same manner as in the first embodiment, the influence of mutual diffusion (specifically diffusion in the direction parallel to the principal surface of the substrate) of the impurities due to the annealing is substantially negligible. As a result, variations in transistor characteristics can be further reduced.

In this embodiment, in forming the gate electrodes **30***a*-**30***d* by dry-etching the silicon film **14**, substantially no impurities are implanted into portions of the silicon film **14** at least on the active regions **10***a* and **10***b* in the logic area. Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film **14** caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode **30***a* of the NMISFET and the gate electrode **30***b* of the PMISFET, thereby reducing variations in transistor characteristics due to variations in gate length.

In addition, in this embodiment, in a portion of the silicon film **14** constituting the gate electrode **30***d* in the PMIS region in the SRAM area, the n-type impurity is implanted in the gate injection, whereas the p-type impurity is implanted in source/drain implantation. Accordingly, to form the PMISFET in the SRAM area as a surface channel type, the n-type impurity concentration in the gate injection is preferably lower than the p-type impurity concentration in the source/drain implantation, as in the first embodiment. In this case, as a feature of this embodiment, the p-type impurity concentration of each of the p-type silicon films **14***b***1** and **14***b***2** constituting the gate electrode **30***b* in the PMIS region in the logic area is higher than that of the p-type silicon film **14***d* in constituting the gate electrode **30***d* in the PMIS region in the SRAM area.

Further, in this embodiment, the n-type silicon film **14***a***1** on the active region **10***a* formed in the logic area has an n-type impurity concentration lower than that of the n-type silicon film **14***a***2** on a portion of the isolation region **11** formed in the logic area, and the p-type silicon film **14***b***1** on the active region **10***b* formed in the logic area has a p-type impurity concentration lower than that of the p-type silicon film **14***b***2** on a portion of the isolation region **11** formed in the logic area. Accordingly, although the gate electrodes **30***a* and **30***b* on the active regions **10***a* and **10***b* formed in the logic area have high resistances, metal silicide layers **22***a* and **22***b* are formed on the gate electrodes **30***a* and **30***b*, and the gate electrodes **30***a* and **30***b* (i.e., gate lines) on portions of the isolation region **11** formed in the logic area have high impurity concentrations similar to those in the first embodiment. In this manner, a delay of the circuit speed due to increase in resistance of the gate electrodes **30***a* and **30***b* on the active regions **10***a* and **10***b* can be reduced. Since no impurities are implanted into portions of the silicon film **14** constituting the gate electrodes **30***a* and **30***b* on the active regions **10***a* and **10***b* in gate injection in this embodiment, an impurity in an amount necessary for preventing formation of depletion in the final structure needs to be implanted in source/drain implantation. In a case where a delay of the circuit speed due to an increase in resistance of the gate electrodes **30***a* and **30***b* on the active regions **10***a* and **10***b* has a small influence, an impurity does not need to be implanted into portions the silicon film **14** constituting the gate electrodes **30***a* and **30***b* on portions of the isolation region **11** formed in the logic area in gate injection.

In this embodiment, gate injection of the n-type impurity is performed on the NMIS region and the PMIS region in the SRAM area, and then source/drain implantation of the p-type impurity is performed, thereby reversing the conductivity type of a portion of the silicon film **14** constituting the gate electrode **30***d* in the PMIS region in the SRAM area to the p-type. Alternatively, the conductivity type of a portion of the silicon film **14** constituting the gate electrode **30***c* in the NMIS region in the SRAM area may be reversed to the n-type by performing gate injection of an p-type impurity on the NMIS region and the PMIS region in the SRAM area and then performing source/drain implantation of an n-type impurity.

Third Embodiment

A semiconductor device according to a third embodiment of the present disclosure will be described hereinafter with reference to the drawings.

FIG. **11**A is a plan view illustrating a logic area of the semiconductor device of the third embodiment. FIG. **11**B is a cross-sectional view taken along the line I-I (along the gate width) in FIG. **11**A. FIG. **11**C is a plan view illustrating an SRAM area of the semiconductor device of the third embodiment. FIG. **11**D is a cross-sectional view taken along the line II-II (along the gate width) in FIG. **11**C. In FIGS. **11**A-**11**D, sidewall spacers, a silicide layer, and an interlayer film, for example, are not shown for simplicity, and contacts are not shown in FIGS. **11**B and **11**D. In FIGS. **11**A-**11**D, components already shown in FIGS. **1**A-**1**D for the first embodiment are denoted by the same reference characters, and descriptions thereof will not be repeated and only different characteristics will be described hereinafter.

The third embodiment is different from the first embodiment in the following aspects. As illustrated in FIGS. **11**A and **11**B, in the same manner as in the second embodiment illustrated in FIGS. **9**A and **9**B, a dual-gate electrode **31**L includes: a gate electrode **30***a* located in an NMIS region and including an n-type silicon film **14***a***1** provided on an active region **10***a* and a portion of the isolation region **11** near the active region **10***a* and an n-type silicon film **14***a***2** provided on portions of the isolation region **11** at both ends of the n-type silicon film **14***a***1**; and a gate electrode **30***b* located on a PMIS region and including a p-type silicon film **14***b***1** provided on an active region **10***b* and a portion of the isolation region **11**

near the active region **10***b* and a p-type silicon film **14***b***2** provided on portions of the isolation region **11** at both ends of the p-type silicon film **14***b***1**.

The configuration of an SRAM area illustrated in FIGS. **11**C and **11**D including the structure of a dual-gate electrode **31**S is basically the same as that in the SRAM area of the first embodiment illustrated in FIGS. **1**C and **1**D. Specifically, in the same manner as in the first embodiment, the dual-gate electrode **31**S includes a gate electrode **30***c* located in an NMIS region and including an n-type silicon film **14***c* and a gate electrode **30***d* located in a PMIS region and including a p-type silicon film **14***d*. However, in this embodiment, the n-type impurity concentration of the n-type silicon film **14***c* and the p-type impurity concentration of the p-type silicon film **14***d* are lower than those in the first embodiment.

A feature of this embodiment is that the p-type silicon film **14***b***2** has a p-type impurity concentration higher than that of the p-type silicon film **14***d* and that the p-type silicon film **14***b***1** has a p-type impurity concentration substantially equal to that of the p-type silicon film **14***d*. Specifically, the p-type silicon film **14***b***1** has a p-type impurity concentration lower than that of the p-type silicon film **14***b***2**. The n-type silicon film **14***a***1** has an n-type impurity concentration substantially equal to that of the n-type silicon film **14***c*. The n-type silicon film **14***a***1** has an n-type impurity concentration lower than that of the n-type silicon film **14***a***2**. Specifically, the n-type silicon film **14***a***2** has an n-type impurity concentration lower than that of the n-type silicon film **14***c*.

A method for fabricating a semiconductor device according to the third embodiment will be described hereinafter with reference to the drawings. The method for fabricating a semiconductor device of this embodiment is different from that of the first embodiment only in the location of gate injection in each of the logic area and the SRAM area (see FIGS. **12**A-**12**F).

FIGS. **12**A-**12**F are cross-sectional views illustrating a process step of the method for fabricating a semiconductor device of the third embodiment. FIG. **12**A illustrates a cross-sectional structure in the process step taken along the line III-III (along the gate length) in FIG. **11**A. FIG. **12**B illustrates a cross-sectional structure in the process step taken along the line IV-IV (along the gate length) in FIG. **11**A. FIG. **12**C illustrates a cross-sectional structure in the process step taken along the line V-V (along the gate length) in FIG. **11**C. FIG. **12**D illustrates a cross-sectional structure in the process step taken along the line VI-VI (along the gate length) in FIG. **11**C. FIG. **12**E illustrates a cross-sectional structure in the process step taken along the line I-I (along the gate width) in FIG. **11**A. FIG. **12**F illustrates a cross-sectional structure in the process step taken along the line (along the gate width) in FIG. **11**C.

In this embodiment, first, the same process step as that of the first embodiment illustrated in FIGS. **2**A-**2**F is performed. Thereafter, as illustrated in FIGS. **12**A-**12**F, the surface of a semiconductor substrate **10** is cleaned with, for example, diluted hydrogen fluoride, and then a gate insulating film **13** of, for example, a silicon dioxide film with a thickness of about 2 nm is deposited by, for example, ISSG oxidation on the active regions **10***a*, **10***b*, **10***c*, and **10***d*. Subsequently, the semiconductor substrate **10** is subjected to, for example, a nitrogen plasma process, thereby nitriding the surface of the gate insulating film **13** to form a nitrided layer (not shown). Then, annealing is performed, thereby removing nitrogen atoms with weak bonds from the nitrided layer. Subsequently, a silicon film **14** of, for example, polysilicon with a thickness of about 100 nm is deposited by, for example, CVD over the gate insulating film **13**.

Then, as illustrated in FIGS. **12**A-**12**F, with a mask pattern **51**C covering the entire NMIS region and the active region **10***b* in the PMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the isolation region **11** in the PMIS region in the logic area, ions of a p-type impurity such as boron (B) are implanted into the silicon film **14** at a dose of 4×10^{15} cm^{-2}, thereby forming a p-type silicon film **14**P on a portion of the isolation region **11** in the PMIS region in the logic area. In this process step, the length (e.g., about 50 nm) of a portion of the isolation region **11** covered with the mask pattern **51**C near the active region **10***b* in the PMIS region in the logic area is determined in consideration of the influence of mutual diffusion of the impurities. Thereafter, with a mask pattern **52**C covering the entire PMIS region and the active region **10***a* in the NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the isolation region **11** in the NMIS region in the logic area, ions of an n-type impurity such as phosphorus (P) are implanted into the silicon film **14** at a dose of 3×10^{15} cm^{-2}, thereby forming an n-type silicon film **14**N on a portion of the isolation region **11** located in the NMIS region in the logic area. In this process step, the length (e.g., about 50 nm) of a portion of the isolation region **11** covered with the mask pattern **52**C near the active region **10***a* in the NMIS region in the logic area is determined in consideration of the influence of mutual diffusion of the impurities. That is, in this embodiment, no gate injection is performed on any of the NMIS region and PMIS region in the SRAM area, unlike the first and second embodiments.

Formation of the p-type silicon film **14**P and formation of the n-type silicon film **14**N may be performed in any order. In FIGS. **12**A-**12**F, not resist patterns formed on the semiconductor substrate **10** by photolithography but mask patterns on photomasks for forming these resist patterns are schematically shown as the mask patterns **51**C and **52**C for simplicity. The mask patterns **51**C and **52**C are designed such that a PN boundary **41**L between the p-type silicon film **14**P and the n-type silicon film **14**N is located on a portion of the isolation region **11** between the active region **10***a* and the active region **10***b*.

After formation of the p-type silicon film **14**P and the n-type silicon film **14**N, the semiconductor substrate **10** is subjected to heat treatment at, for example, 850° C. for 30 seconds, thereby uniformizing a vertical profile of an impurity implanted as ions into each of the p-type silicon film **14**P and the n-type silicon film **14**N.

Thereafter, process steps similar to the process step (gate patterning) illustrated in FIGS. **4**A-**4**F and the process step (formation of offset spacers and shallow source/drain regions) illustrated in FIGS. **5**A-**5**F, the process step (formation of sidewall spacers and deep source/drain regions) illustrated in FIGS. **6**A-**6**F, the process step (formation of a silicide layer) illustrated in FIGS. **7**A-**7**F, and the process step (formation of an interlayer insulating film and a contact silicide layer) illustrated in FIGS. **8**A-**8**F of the first embodiment are performed in order.

In the foregoing manner, the semiconductor device of this embodiment, i.e., the semiconductor device including: an NMISFET located in the logic area and including the gate electrode **30***a* having the n-type silicon films **14***a***1** and **14***a***2**; a PMISFET located in the logic area and including the gate electrode **30***b* having the p-type silicon films **14***b***1** and **14***b***2**; an NMISFET located in the SRAM area and including the gate electrode **30***c* having the n-type silicon film **14***c*; and a

PMISFET located in the SRAM area and including the gate electrode **30***d* having the p-type silicon film **14***d*, can be fabricated.

In this embodiment, in forming the gate electrodes **30***a*-**30***d* by dry-etching the silicon film **14**, no impurities are implanted into portions of the silicon film **14** constituting the gate electrodes **30***c* and **30***d* in the SRAM area susceptible to the influence of mutual diffusion of the impurities because of a small width of the isolation region **11** (specifically a portion of the isolation region **11** between the active region **10***c* and the active region **10***d*). Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film **14** caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode **30***c* of the NMISFET and the gate electrode **30***d* of the PMISFET, thereby reducing variations in transistor characteristics due to variations in gate length. In addition, in dry-etching the silicon film **14**, it is necessary to uniformize the vertical profile of an impurity implanted into the silicon film **14** beforehand by annealing. However, in this embodiment, since substantially no impurities are implanted into a portion of the silicon film **14** located in the SRAM area at the time when the silicon film **14** is etched, the influence of mutual diffusion (specifically diffusion in the direction parallel to the principal surface of the substrate) of the impurities due to the annealing is substantially negligible. As a result, variations in transistor characteristics can be further reduced.

In this embodiment, in forming the gate electrodes **30***a*-**30***d* by dry-etching the silicon film **14**, substantially no impurities are implanted into portions of the silicon film **14** at least on the active regions **10***a* and **10***b* in the logic area. Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film **14** caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode **30***a* of the NMISFET and the gate electrode **30***b* of the PMISFET, thereby reducing variations in transistor characteristics due to variations in gate length.

In addition, in this embodiment, the n-type silicon film **14***a***1** on the active region **10***a* formed in the logic area has an n-type impurity concentration lower than that of the n-type silicon film **14***a***2** on a portion of the isolation region **11** formed in the logic area, and the p-type silicon film **14***b***1** on the active region **10***b* formed in the logic area has a p-type impurity concentration lower than that of the p-type silicon film **14***b***2** on a portion of the isolation region **11** formed in the logic area. Accordingly, although the gate electrodes **30***a* and **30***b* on the active regions **10***a* and **10***b* formed in the logic area have high resistances, metal silicide layers **22***a* and **22***b* are formed on the gate electrodes **30***a* and **30***b*, and the gate electrodes **30***a* and **30***b* (i.e., gate lines) on portions of the isolation region **11** formed in the logic area have high impurity concentrations similar to those in the first embodiment. In this manner, a delay of the circuit speed due to increase in resistance of the gate electrodes **30***a* and **30***b* on the active regions **10***a* and **10***b* can be reduced. Since no impurities are implanted into the silicon film **14** constituting the gate electrodes **30***a* and **30***b* on the active regions **10***a* and **10***b* in gate injection in this embodiment, an impurity in an amount necessary for preventing formation of depletion in the final structure needs to be implanted in source/drain implantation. In a case where a delay of the circuit speed due to an increase in resistance of the gate electrodes **30***a* and **30***b* on the active regions **10***a* and **10***b* has a small influence, an impurity does not need to be implanted into portions of the silicon film **14** constituting the gate electrodes **30***a* and **30***b* on portions of the isolation region **11** formed in the logic area in gate injection.

Further, in this embodiment, no impurities are implanted into portions of the silicon film **14** constituting the gate electrodes **30***c* and **30***d* in the SRAM area in gate injection, i.e., impurities are implanted into portions of the silicon film **14** constituting the gate electrodes **30***c* and **30***d* only in source/drain implantation. Thus, the gate electrodes **30***c* and **30***d* have resistances higher than those of the gate electrodes **30***a* and **30***b* in the logic area. However, since transistors for SRAM circuits do not need to operate at high speed, unlike transistors for logic circuits, the influence of, for example, a delay of the circuit speed due to increase in resistance of the gate electrodes **30***c* and **30***d* is small.

Fourth Embodiment

A semiconductor device according to a fourth embodiment of the present disclosure will be described hereinafter with reference to the drawings.

FIG. **13**A is a plan view illustrating a logic area of the semiconductor device of the fourth embodiment. FIG. **13**B is a cross-sectional view taken along the line I-I (along the gate width) in FIG. **13**A. FIG. **13**C is a plan view illustrating an SRAM area of the semiconductor device of the fourth embodiment. FIG. **13**D is a cross-sectional view taken along the line II-II (along the gate width) in FIG. **13**C. In FIGS. **13**A-**13**D, sidewall spacers, a silicide layer, and an interlayer film, for example, are not shown for simplicity, and contacts are not shown in FIGS. **13**B and **13**D. In FIGS. **13**A-**13**D, components already shown in FIGS. **1**A-**1**D for the first embodiment are denoted by the same reference characters, and descriptions thereof will not be repeated and only different characteristics will be described hereinafter.

The configuration of the logic area illustrated in FIGS. **13**A and **13**B including the structure of a dual-gate electrode **31**L is the same as that of the logic area of the first embodiment illustrated in FIGS. **1**A and **1**B. Specifically, in the same manner as in the first embodiment, the dual-gate electrode **31**L includes a gate electrode **30***a* located in an NMIS region and including an n-type silicon film **14***a* and a gate electrode **30***b* located in a PMIS region and including a p-type silicon film **14***b*.

On the other hand, the configuration of the SRAM area illustrated in FIGS. **13**C and **13**D including the structure of a dual-gate electrode **31**S is basically the same as that in the SRAM area of the first embodiment illustrated in FIGS. **1**C and **1**D. Specifically, in the same manner as in the first embodiment, the dual-gate electrode **31**S includes a gate electrode **30***c* located on an NMIS region and including an n-type silicon film **14***c* and a gate electrode **30***d* located on a PMIS region and including a p-type silicon film **14***d*. However, in this embodiment, the n-type impurity concentration of the n-type silicon film **14***c* and the p-type impurity concentration of the p-type silicon film **14***d* are lower than those in the first embodiment.

A feature of this embodiment is that the p-type silicon film **14***b* has a p-type impurity concentration higher than that of the p-type silicon film **14***d* and that the n-type silicon film **14***a* has an n-type impurity concentration higher than that of the n-type silicon film **14***c*.

A method for fabricating a semiconductor device according to the fourth embodiment will be described hereinafter with reference to the drawings. The method for fabricating a semiconductor device of this embodiment is different from that of the first embodiment only in the location of gate injection in the SRAM area (see FIGS. **14**A-**14**F).

FIGS. **14**A-**14**F are cross-sectional views illustrating a process step of the method for fabricating a semiconductor device of the fourth embodiment. FIG. **14**A illustrates a cross-sectional structure in the process step taken along the line III-III (along the gate length) in FIG. **13**A. FIG. **14**B illustrates a cross-sectional structure in the process step taken along the line IV-IV (along the gate length) in FIG. **13**A. FIG. **14**C illustrates a cross-sectional structure in the process step taken along the line V-V (along the gate length) in FIG. **13**C. FIG. **14**D illustrates a cross-sectional structure in the process step taken along the line VI-VI (along the gate length) in FIG. **13**C. FIG. **14**E illustrates a cross-sectional structure in the process step taken along the line I-I (along the gate width) in FIG. **13**A. FIG. **14**F illustrates a cross-sectional structure in the process step taken along the line II-II (along the gate width) in FIG. **13**C.

In this embodiment, first, the same process step as that of the first embodiment illustrated in FIGS. **2**A-**2**F is performed. Thereafter, as illustrated in FIGS. **14**A-**14**F, the surface of a semiconductor substrate **10** is cleaned with, for example, diluted hydrogen fluoride, and then a gate insulating film **13** of, for example, a silicon dioxide film with a thickness of about 2 nm is deposited by, for example, ISSG oxidation on the active regions **10***a*, **10***b*, **10***c*, and **10***d*. Subsequently, the semiconductor substrate **10** is subjected to, for example, a nitrogen plasma process, thereby nitriding the surface of the gate insulating film **13** to form a nitrided layer (not shown). Then, annealing is performed, thereby removing nitrogen atoms with weak bonds from the nitrided layer. Subsequently, a silicon film **14** of, for example, polysilicon with a thickness of about 100 nm is deposited by, for example, CVD over the gate insulating film **13**.

Then, as illustrated in FIGS. **14**A-**14**F, with a mask pattern **51**D covering the entire NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the entire PMIS region in the logic area, ions of a p-type impurity such as boron (B) are implanted into the silicon film **14** at a dose of 4×10^{15} cm^{-2}, thereby forming a p-type silicon film **14**P in the entire PMIS region in the logic area. Thereafter, with a mask pattern **52**D covering the entire PMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the entire NMIS region in the logic area, ions of an n-type impurity such as phosphorus (P) are implanted into the silicon film **14** at a dose of 3×10^{15} cm^{-2}, thereby forming an n-type silicon film **14**N in the entire NMIS region in the logic area. That is, in this embodiment, no gate injection is performed on any of the NMIS region and the PMIS region in SRAM area, as in the third embodiment.

Formation of the p-type silicon film **14**P and formation of the n-type silicon film **14**N may be performed in any order. In FIGS. **14**A-**14**F, not resist patterns formed on the semiconductor substrate **10** by photolithography but mask patterns on photomasks for forming these resist patterns are schematically shown as the mask patterns **51**D and **52**D for simplicity. The mask patterns **51**D and **52**D are designed such that a PN boundary **41**L between the p-type silicon film **14**P and the n-type silicon film **14**N is located on a portion of the isolation region **11** between the active region **10***a* and the active region **10***b*.

After formation of the p-type silicon film **14**P and the n-type silicon film **14**N, the semiconductor substrate **10** is subjected to heat treatment at, for example, 850° C. for 30 seconds, thereby uniformizing a vertical profile of an impurity implanted in the form of ions into each of the p-type silicon film **14**P and the n-type silicon film **14**N.

Thereafter, process steps similar to the process step (gate patterning) illustrated in FIGS. **4**A-**4**F, the process step (formation of offset spacers and shallow source/drain regions) illustrated in FIGS. **5**A-**5**F, the process step (formation of sidewall spacers and deep source/drain regions) illustrated in FIGS. **6**A-**6**F, the process step (formation of a silicide layer) illustrated in FIGS. **7**A-**7**F, and the process step (formation of an interlayer insulating film and a contact silicide layer) illustrated in FIGS. **8**A-**8**F of the first embodiment are performed in order.

In the foregoing manner, the semiconductor device of this embodiment, i.e., the semiconductor device including: an NMISFET located in the logic area and including the gate electrode **30***a* having the n-type silicon film **14***a*; a PMISFET located in the logic area and including the gate electrode **30***b* having the p-type silicon film **14***b*; an NMISFET located in the SRAM area and including the gate electrode **30***c* having the n-type silicon film **14***c*; and a PMISFET located in the SRAM area and including the gate electrode **30***d* having the p-type silicon film **14***d*, can be fabricated.

In this embodiment, in forming the gate electrodes **30***a*-**30***d* by dry-etching the silicon film **14**, no impurities are implanted into portions of the silicon film **14** constituting the gate electrodes **30***c* and **30***d* in the SRAM area susceptible to the influence of mutual diffusion of the impurities because of a small width of the isolation region **11** (specifically a portion of the isolation region **11** between the active region **10***c* and the active region **10***d*). Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film **14** caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode **30***c* of the NMISFET and the gate electrode **30***d* of the PMISFET, thereby reducing variations in transistor characteristics due to variations in gate length. In addition, in dry-etching the silicon film **14**, it is necessary to uniformize the vertical profile of an impurity implanted into the silicon film **14** beforehand by annealing. However, in this embodiment, since no impurities are implanted into a portion of the silicon film **14** located in the SRAM area at the time when the silicon film **14** is etched, the influence of mutual diffusion (specifically diffusion in the direction parallel to the principal surface of the substrate) of the impurities due to the annealing is substantially negligible. As a result, variations in transistor characteristics can be further reduced.

In this embodiment, no impurities are implanted into portions of the silicon film **14** constituting the gate electrodes **30***c* and **30***d* in the SRAM area in gate injection, i.e., impurities are implanted into portions of the silicon film **14** constituting the gate electrodes **30***c* and **30***d* only in source/drain implantation. Thus, the gate electrodes **30***c* and **30***d* have resistances higher than those of the gate electrodes **30***a* and **30***b* in the logic area. However, since transistors for SRAM circuits do not need to operate at high speed, unlike transistors for logic circuits, the influence of, for example, a delay of the circuit speed due to increase in resistance of the gate electrodes **30***c* and **30***d* is small.

In the first through fourth embodiments, a silicon oxynitride film is used as a gate insulating film and a polysilicon electrode is used as a gate electrode, as examples. However, the present disclosure is not limited to these embodiments. Alternatively, the gate insulating film material may be a high-k material (e.g., an insulating material having a relative dielectric constant of 8 or more) typified by metal oxide such as alumina (Al_2O_3), hafnium oxide (HfO_2), or hafnium silicate ($HfSiO_x$), and the gate electrode structure may be a metal-inserted poly-silicon stack (MIPS) structure including

a metal film of, for example, titanium nitride (TiN) or tantalum nitride (TaN) between the gate insulating film and the polysilicon film in addition to the polysilicon film. In such a case, advantages similar to those of the foregoing embodiments can be obtained. In the MIPS structure, the threshold voltage of a transistor is adjusted mainly by using the work function. This adjustment is determined by a combination of a high-k gate insulating film material and a metal film material. Specifically, the adjustment of the threshold voltage between the NMISFET and the PMISFET may be performed either by changing metal film materials while using the same high-k gate insulating film material or by changing high-k gate insulating film materials while using the same metal film material. Since formation of depletion in the gate electrode is reduced in the MIPS structure, the impurity concentration in the polysilicon film only needs to be set in consideration of gate resistance (resistance of a bulk region, resistance of a silicide/polysilicon interface, resistance of a polysilicon/metal interface). When each of the interface resistances has a sufficiently low resistance, gate resistance is low in a MIPS structure using a metal film.

In the first and second embodiments, to form the PMISFET in the SRAM area as a surface channel type, the n-type impurity concentration in gate injection is preferably lower than the p-type impurity concentration in source/drain implantation. However, in the case of employing an MIPS structure, in view of reducing the resistance of the silicon film and the interface resistances mentioned above, the n-type impurity concentration in gate injection may be higher than the p-type impurity concentration in source/drain implantation. Alternatively, no source/drain implantation may be performed on the silicon films constituting the gate electrodes in the SRAM area. In other words, only gate injection of an n-type impurity may be performed on the silicon films constituting the gate electrodes in the SRAM area. This process changes all the silicon films constituting the gate electrodes of the CMISFETs in the SRAM area into n-type silicon films. In this case, only gate injection of an n-type impurity may be performed on the silicon films constituting the gate electrodes in the logic area, without performing source/drain implantation. This process also changes all the silicon films constituting the gate electrodes of the CMISFET in the logic area into n-type silicon films.

In the third and fourth embodiments, no gate injection is performed on the silicon films constituting the gate electrodes in the SRAM area. However, in the case of employing an MIPS structure, gate injection does not need to be performed on the silicon films constituting the gate electrodes in the SRAM area and the logic area. In other words, only source/drain implantation may be performed on the silicon films constituting the gate electrodes in the SRAM area and the logic area.

The first through fourth embodiments are directed to semiconductor device including logic circuits and SRAM circuits. However, the present disclosure is not limited to these embodiments. For example, in the case of including input/output circuits instead of the logic circuits, the dual-gate electrodes for logic circuits of the above embodiments are applicable. Specifically, the two types of dual-gate electrodes described in each of the above embodiments can be selectively used depending on the width of the isolation region between a pair of active regions where CMISFETs are to be formed. Specifically, the dual-gate electrodes for logic circuits described in the above embodiments may be used for CMISFETs with a relatively wide isolation region, whereas the dual-gate electrodes for SRAM circuits described in the above embodiments may be used for CMISFETs with a relatively narrow isolation region.

What is claimed is:

1. A semiconductor device, comprising:

a first dual-gate electrode; and

a second dual-gate electrode being separated from the first dual-gate electrode, wherein

the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type,

the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type,

the first active region and the second active region are isolated from each other with an isolation region interposed therebetween,

the first gate electrode and the second gate electrode are connected to each other on the isolation region, and

at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

2. The semiconductor device of claim **1**, wherein an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region.

3. The semiconductor device of claim **1**, wherein at least a portion of the first silicon film of the second conductivity type has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

4. The semiconductor device of claim **1**, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

5. The semiconductor device of claim **1**, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region.

6. The semiconductor device of claim **1**, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

7. The semiconductor device of claim **1**, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region.

8. The semiconductor device of claim **1**, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity

concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region.

9. The semiconductor device of claim **1**, wherein a portion of the first silicon film of the first conductivity type located on the isolation region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

10. The semiconductor device of claim **1**, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the first conductivity type located on the third active region.

11. The semiconductor device of claim **1**, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

12. The semiconductor device of claim **1**, wherein

a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region, and

a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

13. The semiconductor device of claim **1**, wherein

the first gate electrode is a gate electrode of a first PMIS transistor,

the second gate electrode is a gate electrode of a first NMIS transistor,

the third gate electrode is a gate electrode of a second PMIS transistor, and

the fourth gate electrode is a gate electrode of a second NMIS transistor.

14. The semiconductor device of claim **1**, wherein

each of the first gate electrode and the second gate electrode is a gate electrode of a transistor for a logic circuit, and

each of the third gate electrode and the fourth gate electrode is a gate electrode of a transistor for an SRAM circuit.

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