IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Advanced Integrated Circuit Process LLC,

Patent Owner.

_____

IPR2025-01210

U.S. Patent No. 7,632,751

_____

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,632,751

TABLE OF CONTENTS

EXHIBIT LIST v

LIST OF CHALLENGED CLAIMS viii

I. RELIEF REQUESTED 1

II. STATE OF THE ART 1

A. Interconnects and Dual Damascene 2

B. Dummy Structures for Reducing Stress-Induced Voiding, and Improving Strength 4

III. THE ’751 PATENT 6

A. Overview 6

B. Prosecution History 8

C. Claim Construction 8

IV. ORDINARY SKILL 8

V. PRIOR ART 9

VI. DETAILED EXPLANATION OF GROUNDS 9

A. GROUNDS 1A/1B: Watanabe anticipates (Ground 1A) and renders obvious (Ground 1B) Claims 1-2, 5-8, 10-13, 18, and 20 9

1. Watanabe 10

2. Claim 1 14

3. Claim 2 28

4. Claim 5 32

5. Claim 6 33

6. Claim 7 35

7. Claim 8 37

8. Claim 10 38

9. Claim 11 40

10. Claim 12 42

11. Claim 13 44

12. Claim 18 46

13. Claim 20 46

B. GROUND 2: Watanabe combined with Kamoshima renders Claims 3-4 and 15-16 unpatentable 50

1. Kamoshima 50

2. Claim 3 51

3. Claim 4 55

4. Claim 15 56

5. Claim 16 56

C. GROUND 3: Watanabe combined with Kamoshima and Fukazawa renders Claim 17 unpatentable 57

1. Fukazawa 57

2. Claim 17 58

D. GROUND 4: Watanabe combined with Iizuka renders Claim 9 unpatentable 62

1. Iizuka 62

2. Claim 9 62

E. GROUND 5: Hasunuma anticipates Claims 1, 5-6, 9, 11-14, and 18-19 64

1. Hasunuma 64

2. Claim 1 66

3. Claim 5 72

4. Claim 6 72

5. Claim 9 73

6. Claim 11 75

7. Claim 12 76

8. Claim 13 77

9. Claim 14 79

10. Claim 18 80

11. Claim 19 81

F. GROUND 6: Hasunuma combined with Kurashima renders Claims 2 and 20 obvious 83

1. Kurashima 83

2. Claim 2 85

3. Claim 20 90

G. GROUND 7: Hasunuma combined with Watanabe renders Claims 2, 8, and 10 unpatentable 94

1. Claim 2 94

2. Claim 8 95

3. Claim 10 97

H. GROUND 8: Aoyagi renders obvious Claims 1, 3-4, 7, 14-16, and 19 100

1. Aoyagi 100

2. Claim 1 104

3. Claim 3 112

4. Claim 4 115

5. Claim 7 116

6. Claim 14 117

7. Claim 15 118

8. Claim 16 120

9. Claim 19 121

I. GROUND 9: Aoyagi combined with Fukazawa renders Claim 17 unpatentable 124

1. Claim 17 124

VII. GROUNDS FOR STANDING 130

VIII. MANDATORY NOTICES AND FEES 130

A. Real Party-In-Interest 130

B. Related Matters 130

C. Counsel and Service Information 131

D. Payment of Fees 131

IX. CONCLUSION 132

EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 7,632,751
1002	File History of U.S. Patent No. 7,632,751 ("'751 File History")
1003	Declaration of Dr. Reinhold Dauskardt
1004	U.S. Patent Publication No. 2003/0116852 to Watanabe et al. ("Watanabe")
1005	U.S. Patent Publication No. 2004/0113238 to Hasunuma et al. ("Hasunuma")
1006	U.S. Patent Publication No. 2001/0019180 to Aoyagi et al. ("Aoyagi")
1007	U.S. Patent No. 6,717,267 to Kunikiyo ("Kunikiyo")
1008	U.S. Patent No. 5,250,465 to Iizuka et al. ("Iizuka")
1009	U.S. Patent Publication No. 2004/0173905 to Kamoshima et al. ("Kamoshima")
1010	JP2002299437 ("Fukazawa") and Certified Translation of Fukazawa with Certification of Translation
1011	U.S. Patent No. 7,042,099 to Kurashima ("Kurashima")
1012	P. Andricacos, "Copper On-Chip Interconnections," *Interface*, *The Electrochemical Society*, pp. 32-37, 1999
1013	U.S. Patent No. 5,885,857 to Yamaha et al. ("Yamaha")
1014	U.S. Patent Publication No. 2003/0005399 to Igarashi ("Igarashi")

1015	U.S. Patent No. 6,717,268 to Hau-Riege ("Hau-Riege")
1016	U.S. Patent No. 6,468,894 to Yang ("Yang")
1017	U.S. Patent No. 6,022,808 to Nogami ("Nogami")
1018	Reserved
1019	Kaanta et al., "Dual Damascene: A ULSI Wiring Technology," *VMIC Conference*, IEEE, Jun. 11-12, 1991, pp. 144-152
1020	U.S. Patent No. 5,032,890 to Ushiku ("Ushiku")
1021	Reserved
1022	U.S. Patent No. 6,582,976 to Watanabe ("Watanabe'976")
1023	S. Middleman et al., *Process Engineering Analysis in Semiconductor Device Fabrication*, pp. 260-61 (excerpted), McGraw-Hill, 1993 ("Middleman")
1024	U.S. Patent No. 6,156,660 to Liu et al. ("Liu")
1025	U.S. Patent No. 5,798,298 to Yang ("Yang 2")
1026	T. I. Bao et al., "90 nm Generation Cu/CVD Low-k (k < 2.5) Interconnect Technology," *Digest. International Electron Devices Meeting*, San Francisco, CA, USA, 2002, pp. 583-586
1027	A. Loke, "Process Integration Issues of Low-Permittivity Dielectrics With Copper for High-Performance Interconnects, Dissertation," Stanford University (1999)
1028	K.N. Tu, "Recent advances on electromigration in very-large-scale-integration of interconnects," *Applied Physics Review – Focused Review*, *Journal of Applied Physics*, Vol. 94, No. 9, pp. 5451-5473 (November 1, 2003)

1029	T. C. Huang, et al., "Numerical Modeling and Characterization of the Stress Migration Behaviour Upon Various 90 nanometer Cu/Low k Interconnects," *Proceedings of the IEEE 2003 International Interconnect Technology Conference (Cat. No.03TH8695)*, Burlingame, CA, USA, 2003 (added to IEEE Xplore 8-11-2003), pp. 207-209
1030	Reserved
1031	Reserved
1032	JP2000012688 to Nasu ("Nasu") and Certified Translation of Nasu with Certification of Translation
1033	U.S. Patent Publication No. 2001/0030365 to Otsuka et al. ("Otsuka")
1034	Wolf, Stanley, *Silicon Processing for the VLSI Era: Deep-Submicron Process Technology*, Lattice Press, 2002 (excerpted) ("Wolf")
1035	U.S. Patent No. 6,858,944 to Huang et al. ("Huang")
1036	Reserved
1037	Reserved
1038	U.S. Patent No. 6,215,189 to Toyoda et al. ("Toyoda")
1039	U.S. Patent No. 6,238,850 to Bula et al. ("Bula")

LIST OF CHALLENGED CLAIMS

Claim Element	Claim Language
1[pre]	A method for fabricating a semiconductor device comprising the steps of:
1[a]	(a) forming a first interconnect on a semiconductor substrate;
1[b]	(b) forming a first insulating film on the first interconnect;
1[c]	(c) forming in the first insulating film, a via hole connected to the first interconnect, a dummy hole which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench connected to the via hole and the dummy hole; and
1[d]	(d) depositing a conductive material in the via hole, the dummy hole and the interconnect trench, thereby forming a via, a dummy via and a second interconnect.
2[a]	The method of claim 1, wherein in the step (a) a first dummy interconnect is simultaneously formed on the semiconductor substrate, and
2[b]	in the step (c) the dummy hole is connected to the first dummy interconnect.
3[a]	The method of claim 1, wherein in the step (c) the interconnect trench is comprised of a first interconnect trench portion and a second interconnect trench portion whose width is smaller than that of the first interconnect trench portion and which branches from the first interconnect trench portion, and
3[b]	the via hole and the dummy hole are connected to the interconnect trench.

4	The method of claim 3, wherein in the step (c) the dummy hole is connected to the branch point between the first and second interconnect trench portions or to the interconnect trench near the branch point.
5	The method of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO_2 film.
6	The method of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode.
7	The method of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect.
8	The method of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect.
9	The method of claim 1, wherein the via and the dummy via are substantially circular in a plan view.
10	The method of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square.
11	The method of claim 1, wherein the first interconnect and the second interconnect extend in a same direction.

12	The method of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends.
13	The method of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less.
14	The method of claim 1, wherein a bottom of the dummy via is located deeper than a bottom of the via.
15[a]	The method of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion, and
15[b]	the via is connected to the second interconnect portion.
16	The method of claim 15, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions.
17[a]	The method of claim 15, wherein the dummy via is substantially rectangular in a plan view, and
17[b]	a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction.
18	The method of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film.

19	The method of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film.
20	The method of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film.

I. RELIEF REQUESTED

Applying the following grounds, Petitioner petitions for *Inter Partes* Review ("IPR") of U.S. Patent No. 7,632,751 ("the '751 patent") and cancellation of claims 1-20:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A/1B	1-2, 5-8, 10-13, 18, 20	102/103	Watanabe
2	3-4, 15-16	103	Watanabe, Kamoshima
3	17	103	Watanabe, Kamoshima, Fukazawa
4	9	103	Watanabe, Iizuka
5	1, 5-6, 9, 11-14, 18-19	102	Hasunuma
6	2, 20	103	Hasunuma, Kurashima
7	2, 8, 10	103	Hasunuma, Watanabe
8	1, 3-4, 7, 14-16, 19	103	Aoyagi
9	17	103	Aoyagi, Fukazawa

This petition is supported by the declaration of Dr. Reinhold Dauskardt, an expert in the field of interconnect technology. TSMC-1003, ¶¶1-39.

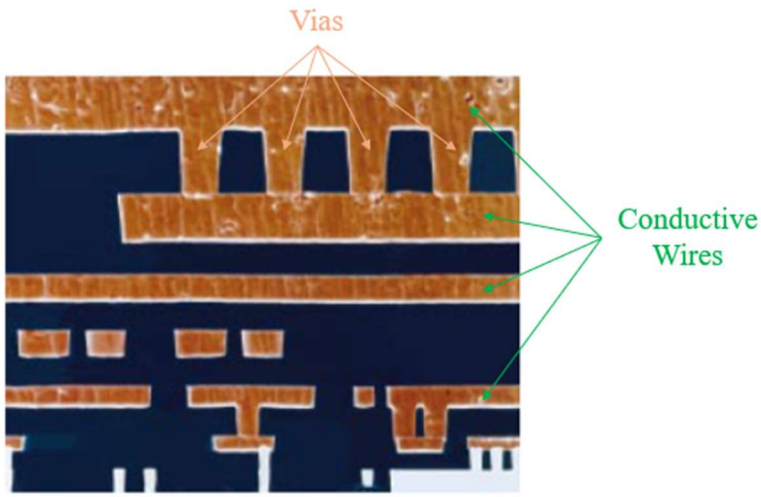
II. STATE OF THE ART

The '751 patent describes the use of dummy structures to reduce stress migration and void formation in interconnect structures. Such dummy structures,

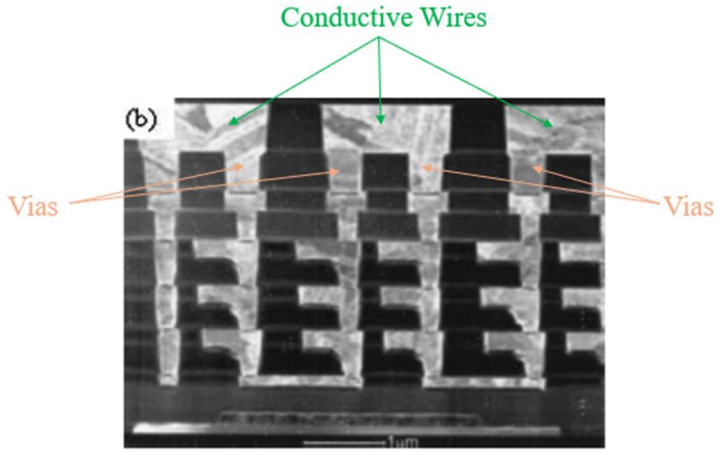
for the same purposes, and associated methods of manufacturing interconnect structures were already known. *Id*., ¶¶40-46.

A. Interconnects and Dual Damascene

Semiconductor chips have multiple levels of conductive wires ("interconnects") for controlling chip operation, with vias connecting wires between different levels when needed; such interconnect structures are commonly made of aluminum or copper. TSMC-1015, 1:13-24; *see also* TSMC-1012, 32; TSMC-1017, 2:53-58. Exemplary interconnect structures are shown below:



TSMC-1012, 32



TSMC-1028, 5452

Dual damascene is a manufacturing process where patterns of trenches and underlying via holes are filled with conductive metal(s) to simultaneously form the interconnects on a given level and the vias below that level. TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract; TSMC-1034, 671-76. This process is illustrated below:

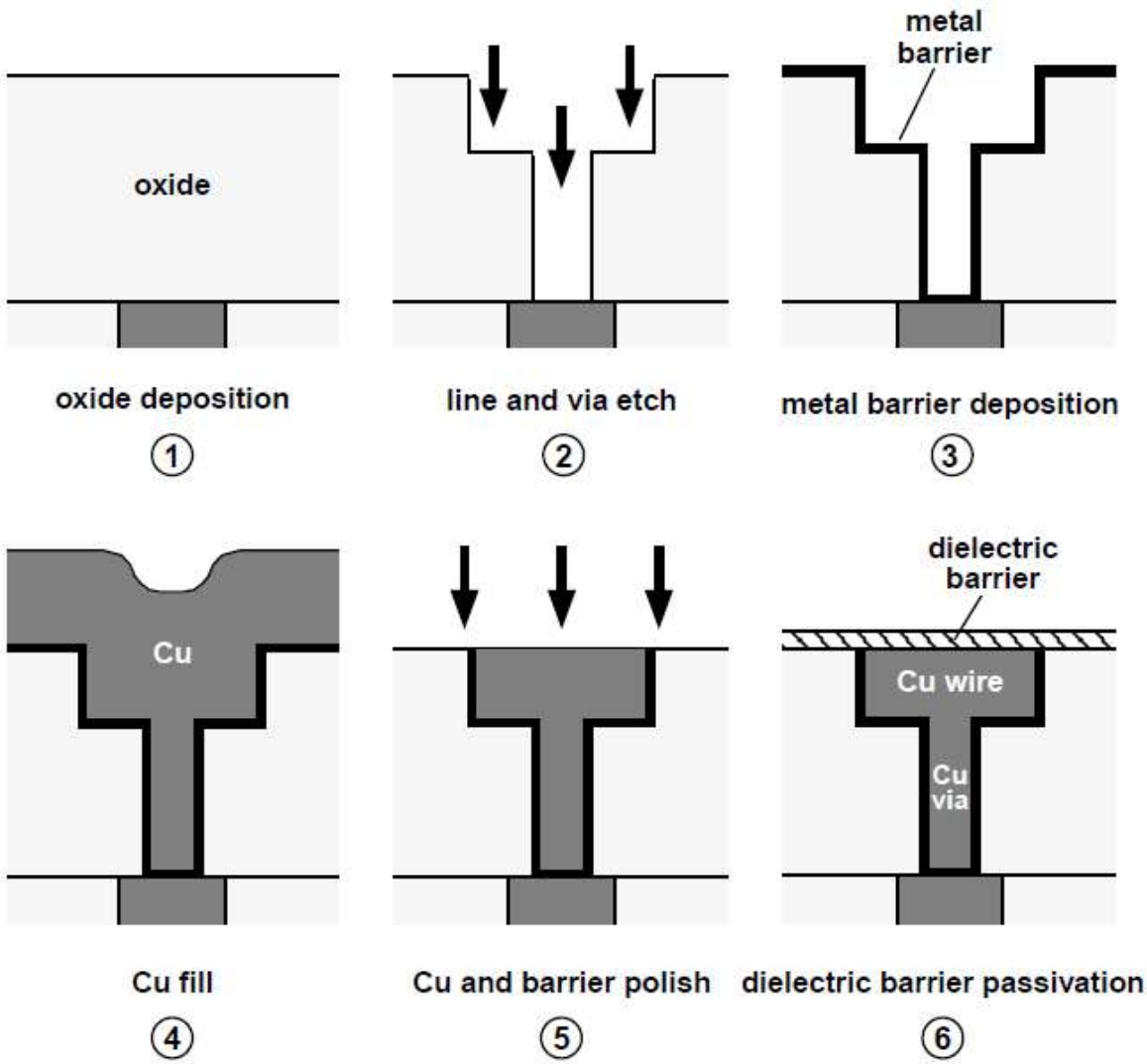


Figure 2-5 Simplified dual-Damascene process flow for fabricating Cu interconnects.

TSMC-1027, 25. Steps ④→⑤ are typically performed using chemical mechanical polishing ("CMP"). TSMC-1034, 322-24, 675.

B. Dummy Structures for Reducing Stress-Induced Voiding, and Improving Strength

Stress migration and electromigration involve the movement of metal atoms and vacancies within the interconnect structure; because vacancies tend to

aggregate in/under vias, voids can form and cause electrical disconnects. TSMC-1029, 207; TSMC-1028, 5455-56, 5458-59; TSMC-1015, 1:32-37, 2:61-63. In addition, insulating films, especially low k materials, can have lower mechanical strength and poorer adhesion that make them susceptible to damage, for example during CMP. TSMC-1016, 1:53-2:7; TSMC-1026, 583.

As replete in the art, dummy structures have been used well before the '751 patent for addressing these problems. For example, dummy vias have been added near active vias to arrest stress-induced vacancy migration and void formation. TSMC-1029, Abstract, 208; TSMC-1015, 2:64-3:14. Dummy structures have been known to address electromigration reliability concerns, including dummy plugs that act as reservoirs for metallic ions and reduce mechanical stress caused by electromigration. *See* TSMC-1015, 1:66-2:11; TSMC-1032, ¶¶[0012]-[0016]. Migrating vacancies/microvoids get distributed between vias and dummy vias, reducing their concentration in/under the vias. TSMC-1029, 208; TSMC-1009, ¶[0088]. Dummy vias were also well-known to improve mechanical strength, such as to prevent damage during CMP. TSMC-1016, 4:42-47; TSMC-1026, 584-85.

Similar to dummy vias, dummy wirings also improve mechanical properties, helping adhesion across multiple insulating layers and leading to improved planarization after CMP by reducing dishing. TSMC-1020, Abstract; TSMC-1024, 2:55-58; TSMC-1025, Abstract; TSMC-1026, 584-85. Connecting dummy wirings

to dummy vias was well-known to increase the mechanical strength of the combined insulating layer and upper-level wiring, as well as enhance the durability of multi-layered insulating films during CMP and other manufacturing steps. TSMC-1011, 8:35-54.

III. THE '751 PATENT

A. Overview

As Dr. Dauskardt explains (TSMC-1003, ¶¶47-51), the '751 patent relates to a method of fabricating a semiconductor device having multilevel interconnection structures. TSMC-1001, 6:22-7:43. A first interconnect 102A (and optionally a dummy interconnect 102B) is formed in insulating film 101. *Id.*, 11:21-26, Figs. 1A, 2B. After forming intermediate insulating layers 103-105, interconnect trench 107, via hole 106A and dummy via hole 110B are formed therein, followed by deposition of barrier film 108/copper film 109 in holes 106A, 106B and trench 107 to form via 110A, dummy via 110B, and second interconnect 111 in a dual damascene process. *Id.*, 11:1-11:37, Figs. 1B-1C, 2A-2B.

FIG. 1B

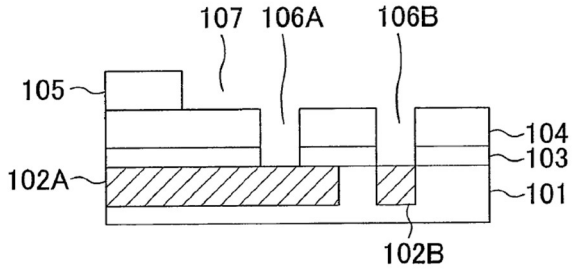
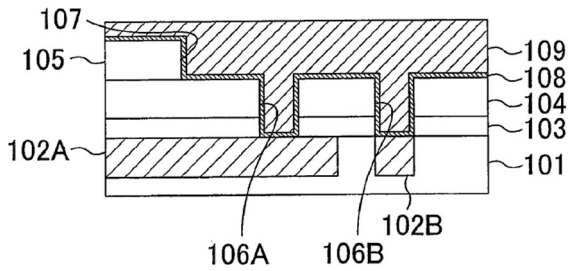
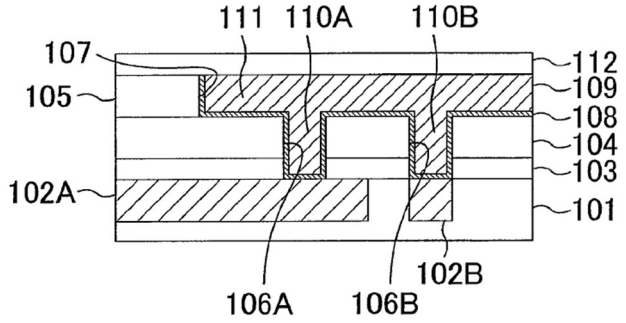


FIG. 1C



Via 110A connects first interconnect 102A and second interconnect 111. *Id.*, 11:31-37. Dummy via 110B connects dummy interconnect 102B and second interconnect 111, but is not connected to first interconnect 102A. *Id.*, 11:31-37; Figs. 2A-2B.

FIG. 2B



First interconnect 102A, via 110A and second interconnect 111 constitute part of a closed circuit during device operation, while neither dummy interconnect 102B nor dummy via 110B does. *Id.*, 10:40-44. That is, the device remains operable even if dummy interconnect 102B and dummy via 110B are omitted. *Id.*, 10:44-48.

According to the ’751 patent, vacancies in copper film 109 of second interconnect 111 are divided and flow into via 110A and dummy via 110B, reducing the total vacancies flowing into via 110A and thereby reducing the associated stress gradient to via 110A. *Id.*, 11:47-54. The ’751 patent says this suppresses occurrences of voids in via hole 106A. *Id.*, 11:57-62.

B. Prosecution History

The ’751 application claims priority to a U.S. application filed December 2, 2004, and a Japanese application filed December 3, 2003.

During prosecution, a first action Notice of Allowance issued, with the following reasons for allowance:

> Claim 27 [issued claim 1] recites…forming a dummy hole which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench connected to the via hole and the dummy hole. These limitations…are neither taught nor suggested in the prior art.

TSMC-1002, 166.

C. Claim Construction

The Board construes claims under the standard in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). For purposes of this proceeding, Petitioner does not believe that any claim terms need construction to resolve the unpatentability issues presented in this Petition. TSMC-1003, ¶52.

IV. ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. TSMC-1003, ¶37. Additional graduate education could substitute for work

experience, and additional work experience/training could substitute for formal education. *Id*.

V. PRIOR ART[1]

Reference	Filed	Published	Pre-AIA Prior Art Qualification
Watanabe	12/4/2002 (USPTO)	6/26/2003	§§102(a),(b),(e)
Hasunuma	9/3/2003 (USPTO)	6/17/2004	§102(e)
Aoyagi	3/20/2001 (USPTO)	9/6/2001	§§102(a),(b),(e)
Kurashima	8/14/2003 (USPTO)	5/9/2006	§102(e)
Iizuka	1/24/1992 (USPTO)	10/5/1993	§§102(a),(b),(e)
Kamoshima	9/9/2003 (USPTO)	9/9/2004	§102(e)
Fukazawa	3/29/2001 (JPO)	10/11/2002	§§102(a),(b)

VI. DETAILED EXPLANATION OF GROUNDS

A. GROUNDS 1A/1B: Watanabe anticipates (Ground 1A) and renders obvious (Ground 1B) Claims 1-2, 5-8, 10-13, 18, and 20

Watanabe anticipates and renders obvious claims 1-2, 5-8, 10-13, 18, and 20. TSMC-1003, ¶¶94-187.

[1] All references are prior art regardless of any priority claim to the Japanese application filed December 3, 2003. Petitioner does not acquiesce that any claims are so entitled.

C. Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3) and 42.10(a), Petitioner provides the following counsel and service information. Pursuant to 37 C.F.R. §42.10(b), a Power of Attorney accompanies this Petition.

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Petitioner consents to electronic service directed to the following email address: Foley_TSMC_751_IPR2025-01210@foley.com.

D. Payment of Fees

The Office is authorized to charge fees for this Petition to Deposit Account No. 19-0741. Any additional fees that might be due are also authorized.

IX. CONCLUSION

Petitioner requests IPR be instituted for the Challenged Claims.

Date: July 15, 2025

Respectfully submitted,

By: ___*/Nicholas Lagerwall/*_____

Nicholas Lagerwall
Reg. No. 63,272
FOLEY & LARDNER LLP
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION, TYPEFACE REQUIREMENTS, AND TYPE STYLE REQUIREMENTS

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,975 words, as counted using the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. §42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. §42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman.

Date: July 15, 2025

By: __*/Nicholas Lagerwall/*_

Nicholas Lagerwall
Reg. No. 63,272
FOLEY & LARDNER LLP
Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on July 15, 2025, true and correct copies of the foregoing document and supporting materials were served in its entirety on the Patent Owner at the following address of record listed on the USPTO's Patent Center via overnight service:

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Szymon M. Gurda
903 Commerce Dr.
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Courtesy copies of the same documents were served electronically on prosecution counsel and Patent Owner's litigation counsel by email at the following addresses:

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