UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

IPR2025-01212
U.S. Patent 7,439,623

PETITIONER'S OPPOSITION TO PATENT OWNER'S DISCRETIONARY DENIAL REQUEST

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I. Introduction

A core purpose of the PTAB under the American Invents Act (AIA) is to strengthen the integrity of the U.S. patent system by ensuring only valid and properly granted patents remain in force. The challenged patent, U.S. Patent 7,439,623 issued as a result of material error by the Examiner. Specifically, among other errors, the Examiner overlooked ***two cited*** references (among only eight total) disclosing the allegedly novel feature of claim 1, and missed ***at least two other references*** teaching the same feature and falling directly within the subclasses the Examiner searched. Indeed, all four of these references anticipate claim 1. As in prior cases with similar examination errors, the Petition should be instituted to correct these errors.

The Petition's merits are exceedingly strong with many §102 references and an additional single-reference §103 reference disclosing all limitations of many challenged claims, including the limitation that led to the '623 patent's allowance.

The settled interests of TSMC outweigh any settled interests of AICP, warranting a merits determination. TSMC's settled expectations are strong due to the lack of any evidence of commercialization, licensing, or marking in the "technology space" where the '623 patent is now asserted. For more than a decade after the '623 patent's issuance, TSMC manufactured the accused chips without incident, including for American customers who integrate those chips into their products.

Institution is warranted and is an efficient use of Board resources in view of

the *Fintiv* factors. First, TSMC has proffered an extraordinarily broad stipulation removing absolutely any overlap between the IPR and parallel litigation by foregoing all §§102 and 103 prior art challenges upon institution. Instituting TSMC's Petition provides a true alternative to adjudicate invalidity, and the Board, with its specialized resources and efficient processes, is best suited to do so. Second, a final written decision ("FWD") is more likely than not to issue before trial. Although the trial date is currently scheduled a few months before the statutory due date for the FWD, the official U.S. Courts trial statistics suggest trial would occur **over 3 months <u>after</u>** the FWD. This fact, combined with the uncertainty due to the current shutdown of the Federal Government, counsels against discretionary denial.

Finally, compelling economic, national security, and other public interest considerations all make IPR of this patent a compelling use of the Office's resources. Despite AICP's allegations to the contrary, its complaint seeks an injunction against TSMC and this requested remedy has not been withdrawn. For the '623 patent alone, AICP alleges infringement by TSMC's 3nm, 4nm, 5nm, 6nm, 7nm, 10nm, 12nm, and 16nm process nodes. And AICP's allegations under the asserted patents collectively involve TSMC's FinFET process nodes and/or 28nm and 22nm process nodes. It is implausible that such a wide ranging infringement campaign would not impact U.S. national security and public interests. TSMC, a trusted foundry and the world's largest chip maker (reportedly providing around 90% of the world's advanced chips)

(*see* TSMC-1049), is vital to the U.S. supply chain with a wide range of applications, including AI (e.g., NVIDIA's AI supercomputers) and military/defense applications (e.g., the F-35 stealth fighter). Given TSMC's vital and strategic contribution in the U.S. supply chain, the Administration has a heightened interest in ensuring the error in issuing this patent is corrected.

II. Institution Is Warranted in View of the Material Errors by the Examiner and Strong Technical Merits of the Petition

The merits here are particularly strong which, combined with the clear errors made during prosecution, warrant institution to correct those mistakes. Even AICP has conceded that where a reference before the Examiner teaches the very "claimed features that the patent examiner indicated were not taught," institution is appropriate to address such examiner error. (Paper-10, 20 (citing *Taiwan Semiconductor Mfg. Co. Ltd. v. Marlin Semiconductor Ltd*., IPR2025-00847, Paper-15 [sic: Paper-11], 3-4 (Sept. 3, 2025)).) This is precisely what occurred during examination of the '623 patent, where the Examiner overlooked: (a) two ***cited*** references, Kunikiyo and Nasu, that disclose the allegedly novel features of claim 1; and (b) at least two other references that disclose the same feature (and anticipate numerous '623 claims) that should have been found under the Examiner's reported search. These material errors, collectively involving ***numerous different §102 references***, warrant institution.

A. The Examiner Materially Erred by Overlooking Disclosures in Both Kunikiyo and Nasu, which Were Cited During Prosecution

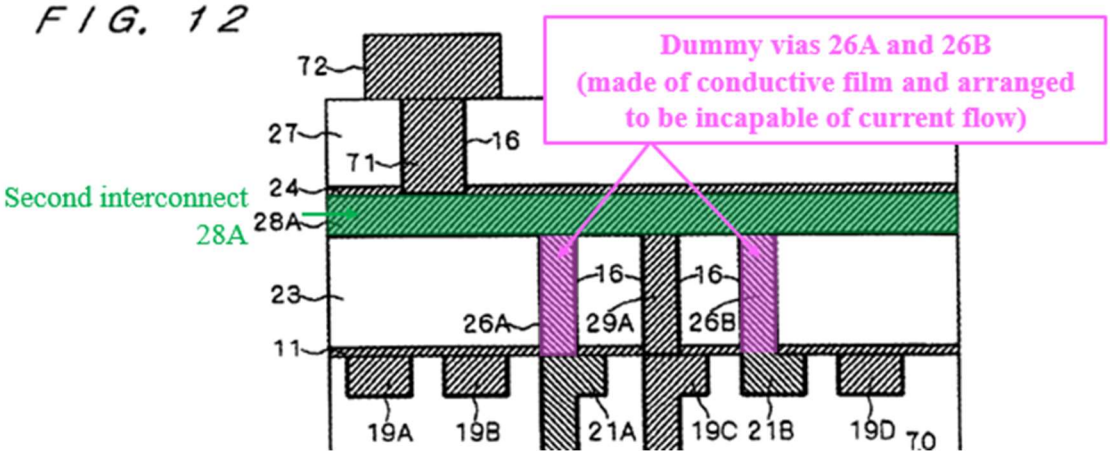
The Examiner allowed the claims because the "cited prior art" allegedly did not disclose a "dummy via" made of conductive film and arranged so as to be incapable of having current flow therethrough. (TSMC-1002, 331, 355.) Yet, Kunikiyo (TSMC-1007) and Nasu (TSMC-1032) were before the Examiner during prosecution, and both teach precisely this feature, and indeed, all of claim 1's limitations.

First, Kunikiyo's Figure 12 embodiment discloses a semiconductor substrate having the claimed first and second interconnects separated by an insulating film and connected by a via. (*See* Pet., 124-30 (noting first interconnect 19C, second interconnect 28A, via 29A, and insulating film 23 all on substrate 1).) Critically, Kunikiyo teaches dummy vias 26A and 26B made of conductive film (copper) connected at one end to the second interconnect forming a dual damascene structure (*see* TSMC-1003, ¶¶488-500), while not connected to another active circuit element or wiring at the other end[1] (Pet., 131-35), as seen below[2]:

[1] Kunikiyo's dummy vias 26A and 26B are connected at their lower ends to dummy interconnects 21A and 21B located on/in second insulating film 10 in Figure 12, just like dummy interconnect 102B of the '623 patent as shown in Figure 2B below, thereby disclosing the additional limitations of claim 2. (Pet., 135-39.)

[2] All color annotations added unless otherwise indicated.

FIG. 12

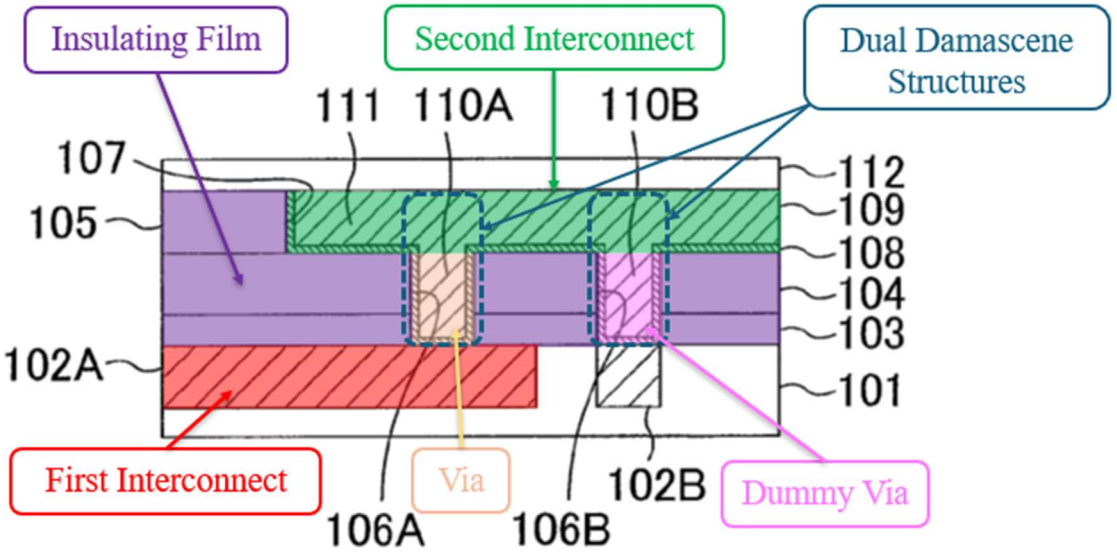


Just like the '623 patent's dummy vias, Kunikiyo's dummy vias terminate at a dummy interconnect in the underlying insulating film(s) at an electrical "dead-end" and do not contribute to the function of Kunikiyo's MOSFET device. (*Id.*, 132-33; TSMC-1007, 20:29-37, 25:54-26:9.) Thus, they are "arranged so as to be incapable of having current flow therethrough"—the exact feature relied on for allowance.

Moreover, Kunikiyo's Figure 12 embodiment discloses all limitations of claim 1. For context, claim 1 and Figure 2B of the '623 patent are shown below:

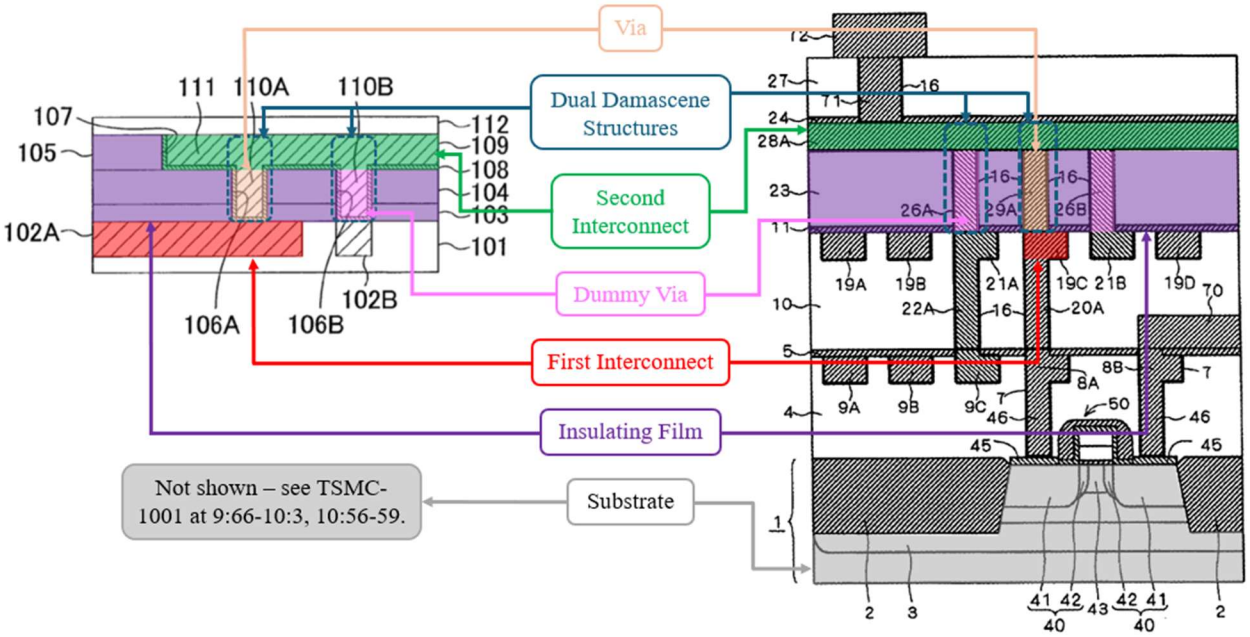
'623 Patent – Claim 1
1. A semiconductor device comprising:
a semiconductor substrate; a first interconnect formed on the semiconductor substrate; a first insulating film formed on the first interconnect; a second interconnect formed on the first insulating film; a via formed through the first insulating film and connecting between the first and second interconnects; and a dummy via connected to the second interconnect,
wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough;
the second interconnect and the via form a dual damascene structure, and

the second interconnect and the dummy via from a dual damascene structure.



'623 Patent (TSMC-1001), Fig. 2B

As seen below, Kunikiyo's Figure 12 embodiment discloses **all** claim 1 limitations:

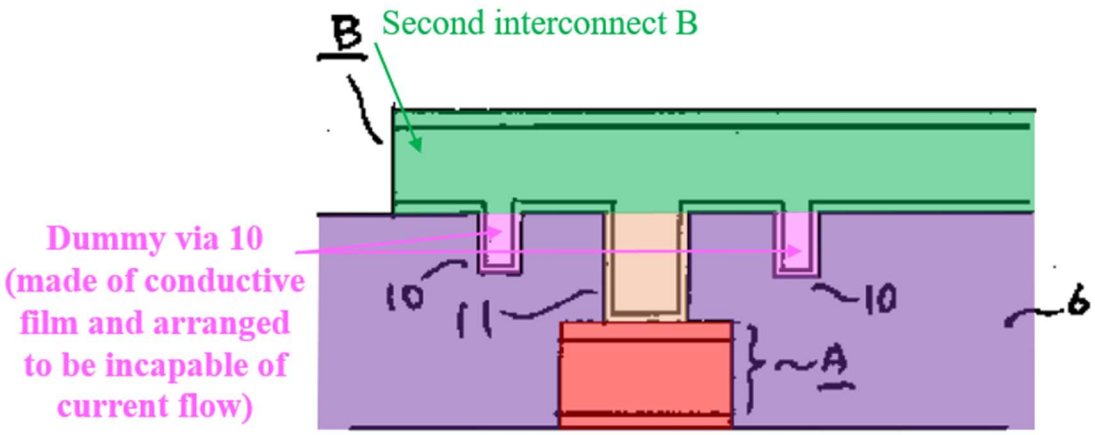


'623 Pat., Fig. 2B

Kunikiyo (TSMC-1007), Fig. 12

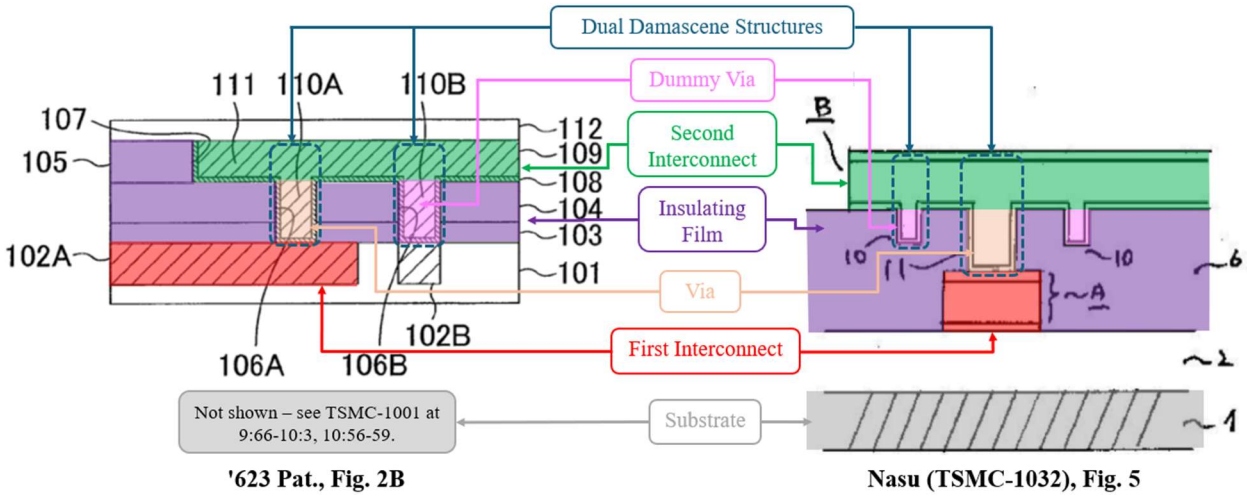
(*See generally* Pet., 124-35.) The Examiner did not rely or comment on Kunikiyo during prosecution.

Second, the Examiner also failed to appreciate the teachings of Nasu (JP2000-012688), another reference cited on the face of the '623 patent. Like Kunikiyo, Nasu also discloses dummy vias 10 (made of conductive film 13) connected to second interconnect B at one end but not connected to another active element at the other end (and thus arranged to be incapable of current flow), as well as all other limitations of claim 1[3]:



Nasu (TSMC-1032), Fig. 5 (excerpted)

[3] Damascene processes were well-known at the time for forming interconnects from copper. (TSMC-1012, 32-33; TSMC-1015, 1:7-24; TSMC-1034, 671-76.) Because Nasu discloses copper interconnects (*see* TSMC-1032, ¶¶[0012], [0016], [0033]), it was obvious to form Nasu's interconnect, via, and dummy vias as "dual damascene structures." (*See* Pet., 2-4, 20-22, 85-86, 106-08, 116-18, 133-35.)



'623 Pat., Fig. 2B — Nasu (TSMC-1032), Fig. 5

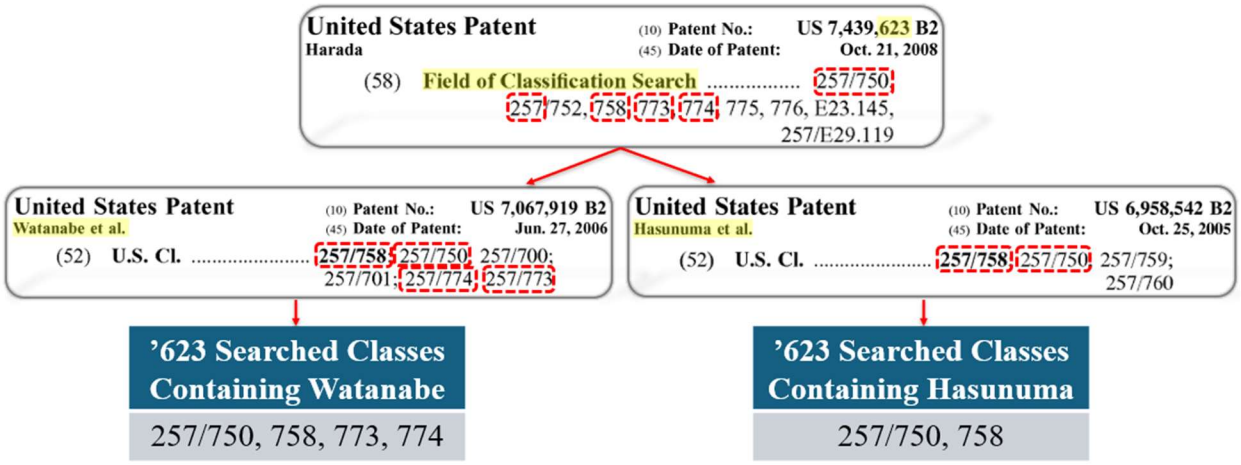
(*See* TSMC-1032, ¶¶[0022]-[0023], [0025]-[0028], [0033]; Fig. 5.)

The Examiner overlooked the foregoing disclosures in Kunikiyo and Nasu, and allowed the '623 patent solely because of the dummy via limitation. The '623 patent cites only eight total prior art references on its face. (TSMC-1001, 1.) **Fully one quarter of these** disclose the exact feature relied on in allowing the claims, while also anticipating claim 1. This manifest error warrants institution.

B. The Examiner Materially Erred by Missing Two More References Falling in the Searched Subclasses, Which Disclose All Limitations of Numerous Claims, including the Limitation Leading to '623 Patent Allowance

The '623 patent's primary U.S. Classification is **257/758**. (TSMC-1001, 1; TSMC-1002, 363.) In June 2008, the Examiner conducted a search within this **257/758** classification (TSMC-1002, 364), which should have uncovered two more anticipatory patents corresponding to Watanabe and Hasunuma, since they likewise have the same **257/758** primary classification and several secondary classifications

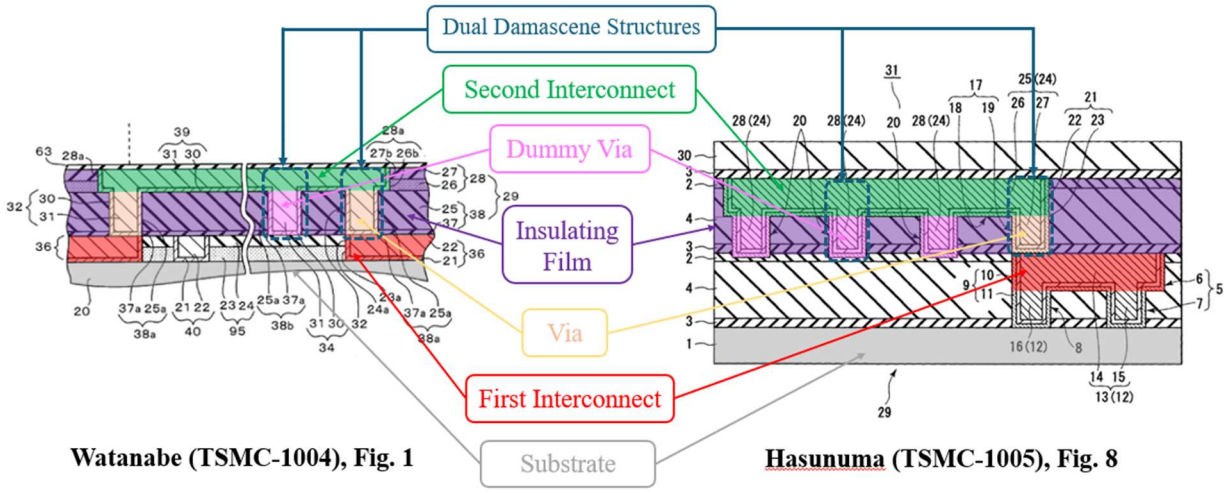
within the alleged search, and were issued years before the Examiner's search:



(*See* TSMC-1067 (Watanabe), 1 (issued June 2006); TSMC-1068 (Hasunuma), 1 (issued October 2005).)[4]

As detailed in the Petition, both Watanabe and Hasunuma expressly disclose all limitations of claim 1 (and many dependent claims)—including the allegedly novel "dummy via" arranged to be incapable of having current flow therethrough, as illustrated below:

[4] TSMC-1067 and TSMC-1068 are the issued patents corresponding to the Watanabe and Hasunuma publications, respectively, used in the Petition.



Watanabe (TSMC-1004), Fig. 1 **Hasunuma (TSMC-1005), Fig. 8**

(*See* Pet., 9-56 (Watanabe), 77-97 (Hasunuma).) Yet, inexplicably, the Examiner missed both Watanabe[5] and Hasunuma despite those references being found in the very subclasses that the '623 Examiner searched, and even sharing the same primary class/subclass as the '623 patent.

In sum, the Examiner failed to consider at least four different references disclosing the allegedly novel feature relied upon for allowance. Two references (Kunikiyo and Nasu) anticipate claim 1 and were among only eight total references listed on the face of the '623 patent, while two more §102 references (Watanabe and Hasunuma) clearly should have been located given that their primary classifications matched the primary classification of the '623 patent that the Examiner searched.

[5] Watanabe's JP counterpart (JP2003-197623) was cited in a search report in January 2007 as an "X" category reference against a Japanese counterpart application. (TSMC-1069, 33-35.) This reference was not disclosed to the U.S. Examiner.

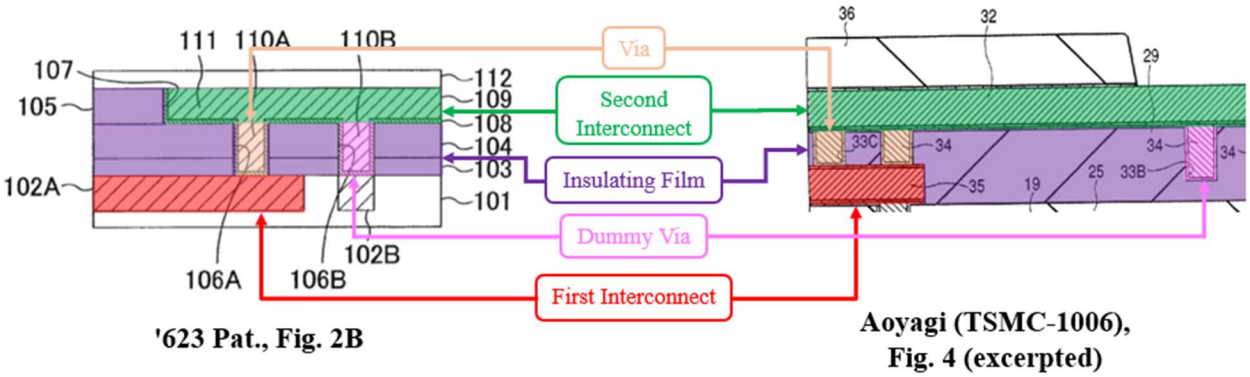
The severity of the Examiner's errors here—overlooking key disclosures in ***multiple cited*** references of the alleged point of novelty and ***multiple other*** §102 references—exceeds other errors found to justify referral. As AICP admits (Paper-10, 20), such significant Examiner error—overlooking features that are clearly disclosed in cited prior art references and highly relevant to the reason for allowing the claims of the '623 patent—weighs heavily against discretionary denial and far outweighs any settled expectations AICP may have acquired with its recent purchase of the asserted patents. *See, e.g.*, *TSMC v. Marlin*, IPR2025-00847, Paper-11, 3-4 (referring, despite challenged patent being in force for 15 years, because the "Office erred in a manner material to the patentability of the challenged claims during patent examination" by "overlook[ing] certain teachings in" a reference from prosecution "that appear to disclose the claimed features that the patent examiner indicated were not taught by the prior art of record, including" the reference); *Samsung Elecs. v. Wilus Inst. of Standards and Tech.*, IPR2025-00935, Paper-12, 3 (Sept. 26, 2025) (referring in part based on examiner error by "overlook[ing] certain teachings" in reference cited on IDS "that appear to disclose features of the challenged claims… thus demonstrating that the Office erred in a manner material to the patentability of the claims"); *Freightcar Am., Inc. v. Nat'l Steel Car Ltd.*, IPR2025-01046, Paper-20, 2-3 (Oct. 10, 2025) (referring petition for a 13-year old patent, based on examiner

error where "examiner overlooked certain teachings of" a reference cited in an IDS "that appear[s] to disclose the allowable features").

C. Kunikiyo, Watanabe, Hasunuma, and Aoyagi (§102 or Single-Reference §103) Disclose All Limitations of Numerous Claims, Including the Missing Limitation Leading to '623 Patent Allowance

The Petition's merits are strong, well-supported, and well-reasoned, and the invalidity positions are straightforward. TSMC presents three §102 references and one single-reference §103 ground against the sole independent claim and numerous dependent claims. (*See* Pet., 1.)

As discussed above in sections II.A and II.B, each of Kunikiyo, Watanabe, and Hasunuma is a §102 reference against claim 1, along with many dependent claims of the '623 patent. (*Id.*, 9-56 (Watanabe), 77-97 (Hasunuma), 124-44 (Kunikiyo).) Moreover, a fourth reference Aoyagi (TSMC-1006) is used for a single-reference §103 ground against claim 1 (and numerous dependent claims), including disclosing a dummy via arranged to be incapable of having current flow therethrough:



(*See id.*, 104-22.)

III. Institution Is Warranted Because the Settled Expectations of TSMC and Others Outweigh AICP's Alleged Expectations

TSMC's settled expectations outweigh AICP's alleged expectations. First, TSMC and its customers have settled expectations that the '623 patent would not apply due to the prior owner's inaction over 16 years since the '623 patent issued, and indeed, not until just before the '623 patent expired. The accused 16nm FinFET products entered volume production in 2014. (TSMC-1070.) For over a decade thereafter, TSMC invested billions of dollars in fabrication facilities to manufacture millions of wafers per year using the accused technology, and its customers similarly invested significant resources into designs based on that technology. During this time, the prior owner of the '623 patent remained silent and inactive, up to the cusp of expiration. TSMC's continuous manufacturing and extensive investments for over a decade before enforcement show that TSMC and its customers relying on its accused technology all have settled expectations that the patent would not apply. Other analyses of a property owner's extended periods of inaction routinely find the equities favor innocent actors such as TSMC. *See* Restatement (First) of Prop. § 459 cmt. a (1993) ("Through lapse of time old rights become obscure. A long continued use raises reasonable expectations of its continuance."); *Anaheim Gardens, L.P. v. United States*, 953 F.3d 1344, 1350-51 (Fed. Cir. 2020); *Nordlinger v. Hahn*, 505 U.S. 1, 12-13 (1992) ("[A]n existing owner rationally may be thought to have vested

expectations in his property or home that are more deserving of protection than the anticipatory expectations of a new owner at the point of purchase.").

Second, AICP has not presented any evidence that the '623 patent was ever "commercialized, asserted, marked, licensed, or otherwise applied" in the same "particular technology space" where it now seeks to assert it, weighing against any claim by AICP of "settled expectations." *Intel Corp. v. Proxense LLC*, IPR2025-00327, Paper-12, 2-3 (June 26, 2025). Indeed, the '623 patent appears to have been asserted for the first time only after AICP acquired it well over a decade after issuance. TSMC-1041. When AICP acquired patents (like the '623 patent) that had never been asserted, with the intention of asserting them, the only reasonable expectation is that their validity would be challenged. *See Anaheim Gardens*, 953 F.3d at 1350-51 ("timing" of a property purchase and "knowledge of the purchaser" are relevant in determining whether purchaser had reasonable investment-backed expectations); *Celgene Corp. v. Peter*, 931 F.3d 1342, 1361-63 (Fed. Cir. 2019) (patent owners know their patents may be subject to post-issuance reconsideration proceedings).

There is no evidence in the record that the '623 patent was licensed, let alone licensed in TSMC's particular technology space. In response to TSMC's request to produce any license to the '623 patent in Patent Owner's possession, AICP produced nothing more than the PPA (EX2026) and responded "AICP is not withholding production of any documents in its possession that are responsive to this request."

(TSMC-1064, 1.) AICP has also not produced any evidence of marking or commercialization of the '623 patent.

AICP's supposed "rel[iance] on the fact that no party had ever challenged" the '623 patent (Paper-10, 20) ignores that no one previously attempted to publicly assert, commercialize, or mark products with the '623 patent. So, the public's "settled expectations" are at least as strong as any expectations of the previous owner.

Third, AICP's primary argument for discretionary denial is that "[t]hree of the Four Patents…are ***expired***," and a majority of challenged claims "are both ***unasserted and expired***" (Paper-10, 1, 3-8 (emph. in orig.)) is meritless. The '751 and '572 patents expired **prior to filing of the complaint**, which AICP admits. (*Id*., 3-4). The '623 patent expired within a few months of AICP's assertion. Yet AICP argues that, for discretionary denial analysis, the '623 patent should be treated as expired. *Id*., 1, 3-4, 7-8 (in arguing for discretionary denial, repeatedly stating that '623 patent is expired). If so, then AICP's stance demonstrates that TSMC has a settled expectation that it would not be sued on this expired patent because neither AICP nor any previous patent owner asserted the '623 patent in any proceeding against anyone else before its complaint against TSMC. The '623 patent having expired is not a reason by itself to deny institution. *See Google v. Sandpiper CDN,* IPR2025-00806, Paper-13, 2 (Sept. 12, 2025) (referring, despite patent being "in force for many years," where patent expired prior to assertion); *Apple v. Allani*,

IPR2025-00856, Paper-11, 3 (Sept. 5, 2025) (referring, despite strong settled expectations from Patent Owner based on patent age, due in part to patent expiring before assertion).

AICP further contends "there is nothing 'cost-effective' about using limited public resources to adjudicate the validity of expired patents." (Paper-10, 1.) But AICP sued TSMC in district court claiming infringement of these expired patents and AICP's suit will require expenditure of limited public resources to address validity of these expired patents somewhere. The only question is whether addressing the patents' invalidity will occur in district court or the PTAB. As AICP itself says, "Congress created IPRs to provide a '***quick*** and ***cost effective alternative***[] to litigation.'" (*Id*. (emph. in orig.).) And that is why IPR should be instituted for all four patents.

AICP further faults TSMC for challenging "unasserted" claims. AICP is wrong. Indeed, TSMC filed the majority of its current IPRs before AICP served its infringement contentions—i.e., before there was any identifiable group of "asserted" versus "unasserted" claims. (*Compare* EX2004, 5 (contentions served on July 16, 2025) *with* IPR2025-01210, Paper-1 (filed July 15, 2025); IPR2025-1302, Paper-2 (filed July 15, 2025); IPR2025-01305, Paper-1 (filed July 15, 2025).) Since AICP did not identify asserted claims in its complaint, its position would require a petitioner to wait to file until after receiving infringement contentions, a fact which

AICP uses as a reason for denial under *Fintiv.* Moreover, AICP has made no representations that it will not add claims to the pending litigation. TSMC however stipulates that if AICP provides a covenant not to sue TSMC and its customers on the non-asserted claims, TSMC would seek authorization to withdraw challenges against such claims. And AICP's argument ignores that under *Fintiv* Factor 4, "additional challenged claims not at issue in the district court … weigh[] against exercising discretion to deny institution." *Samsung Display Co. Ltd. v. Pictiva Displays Int'l Ltd.*, IPR2024-01222, Paper-12, 8 (Mar. 6, 2025).

In sum, the settled expectations of TSMC, its customers, and the public, spanning over a decade, cannot be overridden merely based on AICP's acquisition of the '623 patent. AICP acquired it subject to prior third-party expectations, which were reasonable in view of the prior owner's inaction.

IV. Institution Is Warranted by the Other *Fintiv* Factors

TSMC acted diligently by filing its Petition less than four months after the Complaint was filed. The *Fintiv* factors demonstrate it is an efficient use of Office resources to consider the merits of the Petition and therefore weigh against denial.

Fintiv* Factor 4 Weighs Heavily Against Discretionary Denial.** TSMC proffered an extraordinarily broad stipulation, offering to remove ***all invalidity grounds under Sections 102 and 103, involving any type of legally recognized prior art in the parallel litigation, if TSMC's Petition is instituted, making the Board a true

alternative venue for invalidity. (*See* TSMC-1040, 1-2.) This stipulation weighs heavily against discretionary denial. *See, e.g.*, *Tesla, Inc. v. U.S. Sec'y of the Navy*, IPR2025-00341, Paper-12, 2 (June 13, 2025); *Tesla, Inc. v. Intell. Ventures II*, IPR2025-00339, Paper-10, 2 (June 13, 2025). It ensures this IPR, if instituted, is a true alternative for this phase of the litigation.

***Fintiv* Factor 2 Weighs Against Discretionary Denial:** Based on the current U.S. Courts time-to-trial statistics, it is unclear whether a FWD will issue after the District Court trial occurs, rendering Factor 2 at least neutral. The projected FWD due date is February 8, 2027, while the district court's currently scheduled trial date is November 16, 2026 (*see* EX2027). But the latest time-to-trial statistics from the U.S. Courts suggest trial will not begin until May 2027. (*See* TSMC-1042 (median time to trial in E.D. Texas of 25.9 months), 35.) Such considerations neither favor nor counsel against discretionary denial. *See Tanklogix v. Sitepro*, IPR2025-00761, Paper-10, 2 (Sept. 3, 2025) (finding factor 2 neutral where FWD expected after district court's scheduled trial but before trial date suggested by time-to-trial statistics).

Here, it is more likely than not the Board will issue its FWD before trial begins. Looking specifically at Judge Gilstrap's ***patent jury trials*** over the past year—the most relevant comparator pool—the median time to trial is 25.5 months, consistent with the latest statistics from the U.S. Courts. That would place the trial date for the litigation around May 18, 2027, over three months later than the projected

February 8, 2027 statutory deadline. (*See* TSMC-1043, 4.) AICP, however, ignores this evidence and misleadingly cites non-analogous data associated with all trials before Judge Gilstrap to imply the associated patent trial is likely to occur prior to the FWD. (Paper-10, 12.) AICP further suggests that because the trial date has not changed in the case's first 5 months, the only reasonable assumption is it will never change. (*Id*.) These citations and suggestions fly in the face of common sense and overwhelming evidence of recent delays in Judge Gilstrap's original scheduled patent trials. (*See, e.g.*, TSMC-1044 (moving Oct. 3 trial to Oct. 27); TSMC-1045 (same); TSMC-1046 (delaying Nov. jury trial without explanation); TSMC-1047 (same); TSMC-1048 (same).) Moreover, the uncertain duration of the current U.S. government shutdown may impact the trial date.

***Fintiv* Factor 3 Weighs Against Discretionary Denial:** Based on the current schedule, at the time of institution ("DI"), the District Court case will still be in its early stages—prior to the initial exchange of claim constructions, two months before any claim construction briefing, over three months before the *Markman* hearing, almost five months before close of fact discovery, and six months before close of expert discovery and dispositive motions. (*See* EX2027, 3-5.) AICP points only to the parties' early invalidity and infringement contentions. (*See* Paper-10, 13-14.) That is not enough as the minimal investment by the parties and the Court weighs against discretionary denial. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper-11, 10 (Mar.

20, 2020); *Am. Airlines, Inc., et al. v. Intell. Ventures I, LLC*, IPR2025-00786, Paper-12, 2-3 (Aug. 29, 2025) (referring, despite patent being in force for 18 years, where "little investment in the district court" proceeding).

***Fintiv* Factor 1 Weighs Against Discretionary Denial:** As AICP admits, TSMC's previous motion to stay was denied without prejudice, and TSMC can renew after institution. (Paper-10, 9.) As discussed above, the DI occurs at an early stage of the case, before opening claim construction briefs are even due. (*Id.*, 10.) Stay motions after institution are generally granted on timelines like this. *See, e.g.*, *Resonant Sys., Inc. v. Samsung Elecs. Co.*, No. 2:22-CV-00423-JRG, 2024 WL 1021023, *2-4 (E.D. Tex. Mar. 8, 2024) (granting stay with claim construction briefing underway, close of fact discovery two months away, and IPR filed three months after infringement contentions). AICP's argument that the district court would only stay the case if TSMC's IPR petitions are instituted against all asserted patents requires the circular assumption some will not be—a poor and speculative assumption.

***Fintiv* Factor 5 Is At Least Neutral:** As AICP notes, "factor 5 generally follows factor 2" and therefore weighs against denial here. (Paper-10, 15.)

***Fintiv* Factor 6 Weighs Against Denial.** The district court case here is complex, involving the assertion of 28 claims across four patents. (Paper-10, 1.) The underlying technology is also complex, involving technologically complicated aspects of semiconductor design and manufacture; trained PTAB judges would be

better suited than a lay jury to assess validity. The complexity of the case and technology both weigh ***against*** discretionary denial. *See, e.g.*, *Navy*, IPR2025-00341, Paper-12, 2-3 ("[T]he complex and diverse litigation proceeding tip[s] the balance against discretionary denial.").

AICP contends that under *Fintiv* Factor 6 "foreign third-party discovery in Japan weighs in favor of discretionary denial" because the Petition "relies on four references that TSMC concedes are prior art, if at all, only under § 102(e)." (Paper-10, 16.) AICP's argument strains credibility because AICP did not identify a priority date earlier than the filing date of US 2004/0173905 (September 9, 2003) or other cited references, had ample opportunity to obtain such information before asserting the patent (EX2026, 5), and only speculates such evidence exists.

V. Review Is an Appropriate Use of Office Resources in View of the Compelling National Security, Economic, and Public Interest Considerations

Compelling economic, national security, and other public interest considerations all make *inter partes* review of this patent an appropriate use of the Office's resources—indeed, a compelling one.

Vital U.S. economic and national security interests and TSMC's unprecedented $165 billion investment to onshore advanced semiconductor manufacturing in the U.S. (TSMC-1055), however, are threatened by AICP's infringement allegations seeking to enjoin chips made using TSMC's 22, 28nm process technologies ('373 patent) and TSMC's 3-16nm process technologies ('572, '751, '623 patents).

A. Discretionary Denial Would Harm Compelling U.S. National Security and Public Interests

As Secretary Lutnick explained in April 2025, "national security" is the "key" reason to "bring semiconductors home." (TSMC-1050, 3.) That has been a key principle of President Trump's agenda: "Our national security depends on bringing our supply chain home. This is especially true when we are dealing with critical technology, computer chips that are not only important to our civilian world … but also to our military." (TSMC-1051, 40; *see also* TSMC-1052; TSMC-1053.)

TSMC makes semiconductors for a wide range of "military-grade" devices used by the Department of Defense. (TSMC-1056, 5; TSMC-1057, 59 ("U.S. Department of Defense rel[ies] heavily on Taiwan foundries (particularly TSMC) to manufacture the computer chips needed for their products."); TSMC-1058, 2-3 (TSMC is world's leading manufacturer of radar system chips).) Indeed, TSMC's 28nm to 3nm technologies power widespread military/defense applications like avionics, missile guidance, radar systems, radar electronic warfare, radiation-hardened systems, power systems, imaging for defense and aerospace, and secure communications. The U.S. Air Force estimates "90% of its precision-guided munitions rely on TSMC chips." (TSMC-1054, 4.)

AICP incorrectly argues that these national security concerns should be disregarded if TSMC cannot specifically identify the affected military products. (Paper-10, 18-19.) Although TSMC's has a multi-level supply chain has no direct supply

relationship with the U.S. government, multiple third-party sources confirm that TSMC's products and processes, including those accused by AICP, are essential to a wide array of U.S. military hardware. Given the nature of the industry (and the heightened difficulty of obtaining public documentation of the military's use of specific chips), TSMC has provided adequate evidence of the importance of the accused process nodes for national security.

B. Discretionary Denial Would Harm U.S. Leadership in AI and High-Tech Races, Harming Public Interests Like Healthcare

AI is critical to U.S. leadership. Early in 2025, the President issued an executive order stating: "It is the policy of the United States to sustain and enhance America's global AI dominance in order to promote human flourishing, economic competitiveness, and national security." (TSMC-1073, 1; *see also* TSMC-1074 (July 2025 AI Action Plan), 21 ("Advanced AI compute is essential to the AI era, enabling both economic dynamism and novel military capabilities.").)

A 2024 report by the bi-partisan U.S.-China Economic and Security Review Commission explains the fierce U.S.-China competition, which will "shape the rapidly evolving global technological landscape" and could "transform society, create new industries … and alter the character of warfare." (TSMC-1075, 9.) The country that "secures a lead in key technologies—particularly those with first mover advantages—will tip the balance of power in its favor…." (*Id.*) China is making rapid AI advancements, one such key technology, for economic growth and military

applications. (*Id*., 10-11.)

TSMC is an important part of the American AI-dominance strategy. (*See* TSMC-1076 (Ansys collaboration); TSMC-1077 (Cadence collaboration).) TSMC, the world's largest contract chipmaker, offers the most advanced semiconductor processes. TSMC is a global AI technology leader "steering" the AI wave for tech giants, producing "advanced processors that Nvidia, AMD[] and Apple[] rely on to bring Al to life." (TSMC-1078, 2.)

AICP asserts the '751/'623/'572 patents against chips manufactured by TSMC essential to American AI dominance. These include chips driving AI systems, e.g., NVIDIA's H100 manufactured with TSMC's 4nm process (TSMC-1079, 2), and NVIDIA's latest B100 and B200 chips that can only be manufactured using TSMC's world-leading 3 nm process. (*Id*.)

Healthcare is one of the key areas fueling the projected 30% compound annual growth rate of the AI semiconductor market, where the demand for "advanced chips—TSMC's specialty—will continue to surge." (TSMC-1080, 5.) For example, the Mayo Clinic uses AI supercomputers for medical research that are powered by Cerebras chips, which are "[b]uilt on TSMC 7nm"—one of the very process nodes that AICP alleges infringes. (TSMC-1081, 2.) These same TSMC-manufactured chips were used in a massive scientific study to analyze the COVID-19 virus, a project nominated for a Gordon Bell Special Prize for its contribution to public health.

(TSMC-1082, 1.)

TSMC-built chips also power the vast majority of electronic devices in the world, including smartphones, laptops, computer servers and other devices used in cars and consumer goods. (TSMC-1063, 2.) TSMC enables innovations by its customers, including Apple, NVIDIA, AMD, Broadcom, Microsoft, Amazon, and Tesla, and many others, securing U.S. leadership in high-tech competition.

Given the extraordinarily broad impact of TSMC's technology on U.S. economy and national security, review is an appropriate use of the Board's resources.

VI. Conclusion

For the foregoing reasons, this Petition should be instituted.

Date: October 28, 2025

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

Pursuant to the Board's email dated October 16, 2025, granting Petitioner's request to expand the page limit by 5 pages (*see* Exhibit 3101), the undersigned hereby certifies that this brief complies with the authorized type-volume limitation because this brief does not exceed 25 pages.

Date: October 28, 2025

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CERTIFICATE OF SERVICE

The undersigned herby certifies, in accordance with 37 C.F.R. § 42.205, that the foregoing **Petitioner's Opposition to Patent Owner's Discretionary Denial Request** was served on October 28, 2025, via e-mail directed to counsel of record for Patent Owner at the following:

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