8585976

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United States Patent and Trademark Office

March 27, 2025

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APPLICATION NUMBER: ***16/698,935***
FILING DATE: ***November 27, 2019***
PATENT NUMBER: ***10877233***
ISSUE DATE: ***December 29, 2020***

Certified by

ACTING DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

PTO/AIA/80 (07-12)
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

■ Practitioners associated with Customer Number: 63467

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

■ The address associated with Customer Number: 63467

OR

☐

Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address: Credo Technology Group Limited, Ugland House, Grand Cayman Ky1-1104, Cayman Islands

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	2-9-2018
Name	Adam Thorngate-Gottlund	Telephone	408-664-9329 x127
Title	General Counsel		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	
Filing Date	
First Named Inventor	Yifei DAI, et al
Title	ACTIVE ETHERNET CABLE WITH PRESET PRE-EQUALIZATION
Art Unit	
Examiner Name	
Attorney Docket Number	20160.0038.NPUS00

SIGNATURE of Applicant or Patent Practitioner

Signature	/Dan Krueger/	Date (Optional)	11/27/2019
Name	Dan Krueger	Registration Number	42771
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Credo Technology Group Limited		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Credo Technology Group Limited

Application No./Patent No.: _____ Filed/Issue Date: _____

Titled: ACTIVE ETHERNET CABLE WITH PRESET PRE-EQUALIZATION

Credo Technology Group Limited, a limited company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

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STATEMENT UNDER 37 CFR 3.73(c)

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5. From: _____ To: _____

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Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Dan Krueger/	11/27/2019
Signature	Date
Daniel J. Krueger	42,771
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	2019-11-22
	First Named Inventor	Yifei DAI
	Art Unit	
	Examiner Name	
	Attorney Docket Number	20160.0038.NPUS00

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	9322704	B1	2016-04-26	Neveux	
	2	7401985	B2	2008-07-22	Aronson, et al	

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	1	2018161273	WO	A1	2018-09-13	Credo Technology Group Ltd.		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2019-11-22
	First Named Inventor	Yifei DAI
	Art Unit	
	Examiner Name	
	Attorney Docket Number	20160.0038.NPUS00

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Rumer, B. (2001, February 1). Fighting Jitter in Fibre-Channel Designs. EE Times. Retrieved January 23, 2019, from https://www.eetimes.com/document.asp?doc_id=1277249#.	
	2	Management Data Input/Output. (2018, November 25). Wikiepedia. Retrieved January 23, 2019, from https://en.wikipedia.org/wiki/Management_Data_Input/Output.	
	3	QSFP-DD MSA - QSFP-DD Hardware Specification for QSFP Double Density 8X Pluggable Transceiver Rev 4.0 Candidate. August 15, 2018.	
	4	40 Gigabit Ethernet, 40G QSFP+, 40GBASE-LR4, 40G-BASE-SR4, CFP module, CXP Transceiver, MPO MTP Fiber on May 25, 2015 [http://www.cables-solutions.com/guide-to-40-gigabit-ethernet-options.html]	
	5	IEEE P802.3cd/D1.2, 3rd February 2017 (Amendment of IEEE Std 802.3-2015 as amended) IEEE Draft Standard for Ethernet Amendment: Media Access Control Parameters for 50 Gb/s, 100 Gb/s and 200 Gb/s Operation.	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2019-11-22
	First Named Inventor	Yifei DAI
	Art Unit	
	Examiner Name	
	Attorney Docket Number	20160.0038.NPUS00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Dan Krueger/	Date (YYYY-MM-DD)	2019-11-27
Name/Print	Dan Krueger	Registration Number	42771

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 September 2018 (13.09.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/161273 A1

(51) International Patent Classification:
H04L 12/24 (2006.01)

(21) International Application Number:
PCT/CN2017/075961

(22) International Filing Date:
08 March 2017 (08.03.2017)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **CREDO TECHNOLOGY GROUP LTD.**; P.O. Box 309, Ugland House, Grand Cayman 1104 (KY).

(72) Inventors: **DAI, Yifei**; Room 508, No. 510 Chifeng Road, Hongkou District, Shanghai 200092 (CN). **QIAN, Haoli**; 48617 Tonopah Ct., Fremont, California 94539 (US). **TWOMBLY, Jeff**; 13621 Burke Road, Los Altos Hills, California 94022 (US).

(74) Agent: **SHANGHAI PATENT & TRADEMARK LAW OFFICE, LLC**; 435 Guiping Road, Shanghai 200233 (CN).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: ETHERNET LINK EXTENSION METHOD AND DEVICE

(57) Abstract: Ethernet link extension methods and devices provide, in one illustrative embodiment, an Ethernet link extender with physical medium attachment (PMA) circuits each having a transmitter and receiver that communicate with a respective node in a sequence of communication phases. The sequence includes at least an auto-negotiation phase and a subsequent training phase, the phases occurring simultaneously for both PMA circuits. In the auto-negotiation phase, the PMA circuits operate in a pass-through mode, rendering the extender transparent to the two nodes. In the training phase, the PMA circuits operate independently, sending training frames to their respective nodes based in part on received back-channel information and locally-determined training status information. The training phases may be prolonged if needed to provide a simultaneous transition to a frame-forwarding phase of the sequence.

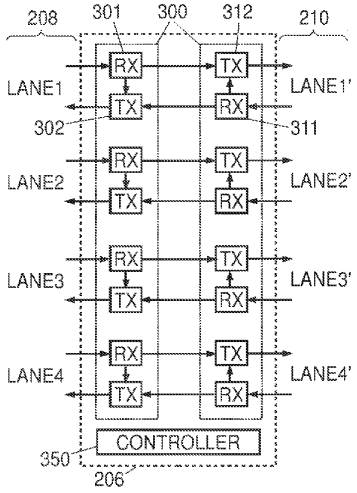


FIG. 3

WO 2018/161273 A1

ETHERNET LINK EXTENSION METHOD AND DEVICE

BACKGROUND

[0001] The Institute of Electrical and Electronics Engineers (IEEE) Standards Associations publishes an IEEE Standard for Ethernet, IEEE Std 802.3-2015, which will be familiar to those of ordinary skill in the art to which this application pertains. This standard provides a common media access control specification for local area network (LAN) operations at selected speeds from 1 Mb/s to 100 Gb/s over coaxial cable, twisted wire pair cable, fiber optic cable, and electrical backplanes. To support shared access on multisegment networks, the standard provides for the use of repeaters at operational speeds up to 1000 Mb/s. Operation at higher speeds appears contemplated solely for point-to-point communication links of an inconveniently limited length. The length limits are imposed by the existence of channel non-idealities such as dispersion and additive noise.

[0002] This choice to support only point-to-point links enables the protocol to include auto-negotiation and training phases for optimizing high-speed communications. The auto-negotiation phase enables the end nodes to exchange information about their capabilities, and the training phase enables the end nodes to adapt both transmit-side and receive-side equalization filters in a fashion that combats the channel non-idealities. Both phases are governed by strict timing requirements, and they each fail to account for any intermediate devices or filters.

[0003] At least in principle, link extenders, also known as signal reconditioners, retimers, or repeaters, are well known. Ideally such devices operate solely as conduits between the link's end nodes, supporting standard-compliant network operations without appearing as additional nodes in the network. We are not aware of any existing link extension methods or devices that can satisfactorily achieve this ideal for Ethernet links operating at 10 Gb/s or above.

SUMMARY

[0004] Accordingly, there are disclosed herein a Ethernet link extension methods and devices. In one illustrative embodiment, an Ethernet link extender includes physical medium attachment (PMA) circuits each having a transmitter and receiver that communicate with a respective node

Marvell Semiconductor, Inc. - Ex. 1002, Page 000012

in a sequence of communication phases, the sequence including at least an auto-negotiation phase and a subsequent training phase, the phases occurring simultaneously for both PMA circuits. In the auto-negotiation phase, the PMA circuits operate in a pass-through mode, rendering the extender transparent to the two nodes. In the training phase, the PMA circuits operate independently, sending training frames to their respective nodes based in part on received back-channel information and locally-determined training status information.

[0005] An illustrative Ethernet link extension method includes a first communications phase for auto-negotiation and a subsequent communications phase for training for use by a first PMA circuit that communicates with a first node and a second PMA circuit that communicates with a second node. In the first phase, the transmitter of the second PMA circuit is coupled to the receiver of the first PMA circuit to retransmit communications received from the first node, and the transmitter of the first PMA circuit is coupled to the receiver of the second PMA circuit to retransmit communications received from the second node. In the second phase, training controllers in each PMA circuit generate training frames for the respective transmitter to send to the respective node, the frames being based in part on received back-channel information and locally-generated training status information from their respective receivers.

[0006] Each of the foregoing embodiments may be implemented individually or in combination, and may be implemented with any one or more of the following features in any suitable combination: (1) the transmitter of the second PMA circuit is coupled to the receiver of the first PMA circuit during the auto-negotiation phase via an on-chip analog signal line. (2) the transmitter of the second PMA circuit is coupled to the receiver of the first PMA circuit during the auto-negotiation phase via a digital signal bus between an analog-to-digital converter and a digital-to-analog converter. (3) the transmitter of the first PMA circuit and the transmitter of the second PMA circuit each include a transmit filter adapted in accordance with back-channel information received from the first and second nodes, respectively, during the training phase. (4) the receiver of the first PMA circuit and the receiver of the second PMA circuit each include a filter adaptation circuit that generates filter coefficient updates and detects filter convergence. (5) at least one of the transmitter of the first PMA circuit and the transmitter of the second PMA circuit includes a training controller providing back-channel information to at least one of

Marvell Semiconductor, Inc. - Ex. 1002, Page 000013

the first and second nodes. (6) the training controller confirms filter convergence only when filter converge is detected by both the receiver of the first PMA circuit and the receiver of the second PMA circuit. (7) the receiver of the first PMA circuit and the receiver of the second PMA circuit each include detector. (8) the extender initiates a training phase when either of the detectors detects an end of the auto-negotiation phase. (9) the detectors monitor spectra of received signals for high-frequency content indicative of training frames. (10) the detectors decode information from auto-negotiation frames to detect said end. (11) each of the first PMA circuit and the second PMA circuit include multiple transmitter-receiver pairs to support multiple communication lanes between the first and second nodes. (12) coupling of the transmitter of the second PMA circuit to the receiver of the first PMA circuit during the auto-negotiation phase includes: (a) digitizing communications received from the first node to obtain received signal samples; (b) conveying the received signal samples on a bus to the transmitter of the second PMA circuit; and (c) converting the received signal samples into an analog electrical transmit signal. (13) adapting a transmit filter in each of the transmitter of the first PMA circuit and the transmitter of the second PMA circuit in accordance with back-channel information received from the first and second nodes, respectively, during the training phase. (14) generating filter coefficient updates and detecting filter convergence with a filter adaptation circuit in each of the receiver of the first PMA circuit and the receiver of the second PMA circuit. (15) providing back-channel information to the first and second nodes with a training controller in each of the transmitter of the first PMA circuit and the transmitter of the second PMA circuit. (16) confirming filter convergence with each of the training controllers only when filter converge is detected by both the receiver of the first PMA circuit and the receiver of the second PMA circuit. (17) initiating the training phase when either, but before both, the receiver of the first PMA circuit and the receiver of the second PMA circuit detects an end of the auto-negotiation phase. (18) monitoring spectra of received signals for high-frequency content to detect said end of the auto-negotiation phase. (19) decoding information from auto-negotiation frames to detect said end.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000014

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] In the drawing:

[0008] Fig. 1 shows an illustrative communications network.

[0009] Fig. 2 is a block diagram of an illustrative extended Ethernet link.

[0010] Fig. 3 is a block diagram of an illustrative Ethernet link extender.

[0011] Fig. 4 is a block diagram of an illustrative PMA circuit receiver.

[0012] Fig. 5 is a block diagram of an illustrative PMA circuit transmitter.

[0013] Fig. 6 is a flowchart of an illustrative Ethernet link extension method.

[0014] It should be understood, however, that the specific embodiments given in the drawings and detailed description do not limit the disclosure. On the contrary, they provide the foundation for one of ordinary skill to discern the alternative forms, equivalents, and modifications that are encompassed in the scope of the appended claims.

DETAILED DESCRIPTION

[0015] The disclosed apparatus and methods are best understood in the context of the larger environments in which they operate. Accordingly, Fig. 1 shows an illustrative communications network 100 including mobile devices 102 and computer systems 104A-C coupled via a routing network 106. The routing network 106 may be or include, for example, the Internet, a wide area network, or a local area network. In Fig. 1, the routing network 106 includes a network of equipment items 108, such as switches, routers, and the like. The equipment items 108 are connected to one another, and to the computer systems 104A-C, via point-to-point communication links 110 that transport data between the various network components. At least some of the links 110 in network 106 are high-speed Ethernet links operating in compliance with the IEEE Std 802.3-2015 at 10 Gb/s or more .

[0016] Fig. 2 is a block diagram of an illustrative high-speed Ethernet link that may be representative of one or more links 110 in Fig. 1. The illustrated embodiment includes a first node 202 (“Node A”) in communication with a second node 204 (“Node B”) via an Ethernet link extender 206. Nodes A & B can each be, for example, any one of equipment items 108, computer systems 104A-C, or other sending/receiving devices having high-speed Ethernet ports

Marvell Semiconductor, Inc. - Ex. 1002, Page 000015

and separated by a distance greater than the point-to-point link length limitations imposed by the standard. The nodes can also be integrated circuit (IC) chips in a switch or other telecommunications system. The illustrated link includes four bidirectional communication lanes 208 extending from Node A to the extender 206 and four communication lanes 210 extending from Node B to the extender 206. Each bidirectional lane represents two unidirectional lanes operating in opposite directions. In accordance with the standard, these unidirectional or bidirectional lanes may be transported by different twisted wire pairs, electrical back-plane traces, copper transmission lines, or optical fibers, or they may be multiplexed onto shared electrical/optical conductors.

[0017] The Ethernet standard specifies the node operations in terms of the hierarchical layers of the Open Systems Interconnection (OSI) model, focusing in particular on the lowermost "physical" layer, which provides the electrical and physical specifications of the connections between the nodes and the communications medium (e.g., pin layouts, line impedances, signal voltages & timing), arrangements of the communications medium (e.g., the network topology), and the electrical and physical specifications for the communications medium itself (e.g., conductor arrangements in copper or fiber optic cable, limitations on attenuation, propagation delay, signal skew). The physical layer is responsible for transmission and reception of raw bit streams over the communications medium, employing simplex, half duplex, or full duplex modes.

[0018] Depending on the applicable clauses, the Ethernet standard divides the physical layer into at least three sublayers: the physical medium dependent (PMD) sublayer, the physical medium attachment (PMA) sublayer, and the physical coding sublayer (PCS). The PMD sublayer specifies the transceiver conversions between transmitted/received channel signals and the corresponding bit (or digital symbol) streams. The PMA sublayer operation varies between clauses, but generally specifies (potential) lane remapping, symbol encoding/decoding, framing, and octet/symbol synchronization. In practice, the delineation between PMD and PMA sublayers may be uncertain and the two sublayers more properly regarded as a combined sublayer. The PCS sublayer provides scrambling/descrambling, data encoding/decoding, block and symbol redistribution, alignment marker insertion/removal, and block-level lane

Marvell Semiconductor, Inc. - Ex. 1002, Page 000016

synchronization and deskew. An optional forward error correction (FEC) sublayer may reside between the PMA and PCS sublayers to provide, e.g., Reed-Solomon coding/decoding that distributes data blocks with controlled redundancy across the lanes. If present, the FEC sublayer provides at least some of the functionality otherwise allocated to the PCS sublayer, e.g., encoding/decoding, alignment marker insertion/removal, and block-level lane synchronization and deskew.

[0019] The circuitry associated with each sublayer (and each of the higher layers in the OSI model) adds to the areal and power requirements of the protocol stack for each device's Ethernet connection, and exacerbates the communications link latency. While this situation is largely unavoidable for the nodes, it is singularly undesirable to impose these penalties on every link extender in the system. The following Ethernet link extender devices and methods seek to exclude any circuitry for implementing the PCS sublayer and any higher layers of the OSI model. At least some of the disclosed extender devices and methods limit their circuitry to only that necessary to implement the PMD and PMA sublayers of the Ethernet standard. As described below, this ideal is achievable by enabling the extender to switch between transparent and opaque modes at different phases of the link establishment process. As a result, the Ethernet link's end nodes (Nodes A & B) conduct standard-compliant operations in ignorance of any intermediate extender devices which may be present, thereby overcoming the link length limitations otherwise imposed by the standard.

[0020] Fig. 3 is a high-level block diagram of an illustrative extender 206 having two PMA circuits 300, one for communicating with Node A via communication lanes 208, and one for communicating with Node B via communication lanes 210. The PMA circuits 300 each have a transceiver for each communication lane, yielding four transmitter-receiver pairs within each PMA circuit. For example, receiver 301 and transmitter 302 communicate with Node A via Lane 1, while receiver 311 and transmitter 312 communicate with Node B via Lane 1'. Lanes 2-4 and 2'-4' are similarly supported. An integrated controller 350 provides chip-level support functions (e.g., voltage regulation, clock generation, MDIO/I2C bus interface for programming and testing) and a firmware-programmed microcontroller having registers for coordinating and controlling the operations of the PMA circuits 300.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000017

[0021] In the normal operating phase, i.e., after the link has been established and data is being conveyed between the nodes, extender 300 operates as follows. Receiver 301 receives via Lane 1 a channel signal from Node A, converts the channel signal into digital receive signal, or more precisely, a frame- and symbol-synchronized bit stream representing the data conveyed via Lane 1. Receiver 301 provides this digital receive signal to transmitter 312, which converts it into a channel signal transmitted to Node B via Lane 1'. The signal-to-noise ratio of the transmitted channel signal on Lane 1' is thereby enhanced relative to the signal-to-noise ratio of the received channel signal on Lane 1. Receiver 311 and transmitter 302 perform the same operations for communications from Node B to Node A. The remaining transmitters and receivers operate similarly for the remaining communications lanes. Note that it may advantageously simplify implementation if the communication lanes are enabled to operate independently in the described fashion.

[0022] To get to the normal operating phase, however, the standard requires that the link pass through an auto-negotiation phase and a subsequent training phase. The auto-negotiation phase enables the end nodes to exchange information about their capabilities, and the training phase enables the end nodes to adapt both transmit-side and receive-side equalization filters in a fashion that combats the channel non-idealities. Both phases are governed by strict timing requirements, and the standard fails to account for the possibility of any intermediate devices or filters.

[0023] The standard specifies that the end nodes initiate the setup of each communications lane by transmitting and receiving frames of auto-negotiation information regarding the respective capabilities of both nodes, acknowledgements of received information, and the results of an arbitration process to select an optimal set of communications parameters given the nodes' respective capabilities. To comply with the standard, the extender, being initially ignorant of the respective capabilities of the end nodes, must force multiple rounds of auto-negotiation to assure an optimal set of communications parameters is chosen by the nodes. (The extender would implement PMA and PCS sublayers that enter a first round of auto-negotiation with each end node to determine their respective capabilities, then enter a second round in which the extender masquerades itself to each end node as the other end node. Note

Marvell Semiconductor, Inc. - Ex. 1002, Page 000018

that additional rounds would also be required if more than one extender is present. In the meantime, the timing limitations on the training phase may cause a link failure.)

[0024] Preferably, then, the extender does not participate in the auto-negotiation process, instead operating in a pass through ("transparent") mode to retransmit the auto-negotiation frames received from each node to the other. In at least some "packet-sniffing" embodiments, the controller 350 monitors the contents of the auto-negotiation frames received on each lane, determining from the embedded control codes for each lane when the selection process is complete and the auto-negotiation phase is concluded. (Rather than treating the communications lanes independently, some alternative embodiments conduct the auto-negotiation process on only the first lane and apply the negotiated communications parameters to all communications lanes. A subsequent failure on any one lane triggers a restart of the auto-negotiation process for all lanes.)

[0025] Notably, however, the auto-negotiation frames are formed from low-rate channel symbols having a large separation (in signal space) even after accounting for channel attenuation and the use of untrained equalization filters. These frames accordingly are not subject to the same link length limitation and can be accurately decoded a significantly greater distances. Accordingly, other "non-decoding" embodiments of extender 206 merely pass along the channel signal waveforms conveying the auto-negotiation frames without timing recovery, demodulation, and/or decoding. Amplification and filtering may be provided, or in some cases, analog-to-digital conversion followed by digital-to-analog conversion at a resolution suitable to pass along the waveform with adequate fidelity. Such embodiments may monitor the spectral content and/or other characteristics of the received channel signals to detect when the auto-negotiation phase is concluded. (For example, the training frames will have high-frequency spectral content that is absent from the auto-negotiation frames.)

[0026] The packet-sniffing embodiments can determine the negotiated operating parameters from the embedded control codes, while the non-decoding extender embodiments can determine the negotiated operating parameters from the spectral characteristics of the training frames. If the negotiated operating parameters are within the extender's capabilities, the extender configures the receivers and transmitters accordingly and commences the training

Marvell Semiconductor, Inc. - Ex. 1002, Page 000019

phase. For 10GBASE-KR, the training phase details can be found in IEEE Std 802.3 clause 72. For 100GBASE-KP4, the details are in IEEE 802.3 clause 94. If the auto-negotiation phase is successful, the end nodes remain unaware of any intervening link extenders during the auto-negotiation phase. However, if the end nodes negotiate a speed that cannot be supported, at least some link extender embodiments treat this situation as an error condition and temporarily disable the transmitters, thereby aborting the link setup process.

[0027] The auto-negotiation phase is followed by a subsequent training phase, in which each end node transmits and receives frames of training information. The frames include broadband training sequences that the other node can employ to adapt its receive filters, training status information, and back-channel information used by the receiving node to adjust its transmit filters. The standard link length limitations apply to the training sequences, and in any event, the extender's transmit and receive filters should also be trained. Accordingly, the extender participates in the training phase, masquerading itself as an end node on each communication lane. Thus, for example, receiver 301 and transmitter 302 participate in the training phase with Node A, while at the same time receiver 311 and transmitter 312 participate in the training phase with Node B. Other than the simultaneous nature of the training phases, the Node A and Node B training occur independently of each other. If the training occurs more quickly on the Node A link than on the Node B link (or vice versa), the extender may prolong the training process on the sufficiently trained link until the training for both links is completed, so that the Node A and Node B training phases conclude at substantially the same time.

[0028] As previously noted, some extender embodiments coordinate the operations of all lanes, so that the training phase for all lanes begins and ends at the same time. Other embodiments enable the lanes to operate independently, and for each lane provide coordination of the Node A and Node B links. As the training phase for each lane (or for all lanes) concludes, the extender places the lanes in a normal-operations mode, which may alternatively be referred to as the frame-forwarding phase. In the frame-forwarding phase, the extender recovers the symbols or bits from each frame received on a given lane from an end node and retransmits them as a regenerated frame on the corresponding lane to the other end node. The extender can thus convey data between the end nodes with very small latency and low power overhead.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000020

[0029] Fig. 4 shows an illustrative receiver 301 suitable for use in the PMA circuits 300. The channel input (CH_IN) node receives an analog electrical signal from a transducer (e.g., a photodiode) or directly from the channel lane conductor and supplies it to a low noise amplifier (LNA) 402. The LNA 402 provides a high input impedance to minimize channel loading and amplifies the received electrical signal to drive the input of a continuous time linear equalizer (CTLE) filter 404. During normal operations, CTLE 404 provides continuous time filtering to shape the signal spectrum in an adaptive fashion to reduce the length of the channel impulse response while minimizing leading inter-symbol interference (ISI). A decision feedback equalizer (DFE) 406 operates on the filtered signal to correct for trailing ISI and detect each transmitted channel bit or symbol, thereby producing a demodulated digital data stream. Some embodiments employ oversampling. A clock and data recovery (CDR) circuit 408 extracts a clock signal from the filtered signal and/or the digital data stream and supplies it to DFE 406 to control timing of the symbol detection. A serial-to-parallel circuit 410 groups the digital data stream bits or symbols into blocks to enable the use of lower clock rates for subsequent on-chip operations. During normal operations, multiplexer 412 places the blocks on the digital receive bus (RXD) for retransmission to the remote end node by a transmitter (e.g., transmitter 312).

[0030] During the auto-negotiation phase, the illustrated LNA 402 supplies the amplified receive signal to an analog-to-digital converter (ADC) 420. ADC 420 digitizes the receive signal, optionally with a sampling rate and resolution to provide adequate reconstruction without requiring timing recovery. The multiplexer 412 places the digital samples of the receive signal on the RXD bus for retransmission on another link. A detector 422 monitors the receive signal for the end of the auto-negotiation phase and/or the beginning of the training phase frames. Alternatively, the auto-negotiation phase signals may be passed through the normal operations signal path (402-404-406-410) with untrained (default) filters and a packet information extractor 442 employed to monitor the contents of the auto-negotiation frames for detecting the end of the auto-negotiation phase.

[0031] During the training phase, LNA 402 supplies the received signal to CTLE filter 404, DFE 406, and S2P circuit 410. A filter adaptation circuit 440 measures an error between the input and output of a decision element in DFE 406, employing that error in accordance with well-

Marvell Semiconductor, Inc. - Ex. 1002, Page 000021

known techniques from the literature on adaptive filtering to determine adjustments for the coefficients in CTLE filter 404, DFE 406, and a transmit filter 506 (discussed further below), and to determine whether convergence has been achieved. The locally-generated information (LOCAL_INFO) including the transmit filter coefficient adjustments and the convergence status are provided to the local transmitter (e.g., transmitter 302). As discussed below, the local transmitter communicates the transmit filter adjustments and the convergence status via a back-channel to the local end node. In that vein, the received signal includes back-channel information *from* the local end node. A packet information extractor 442 detects the back-channel information (BACK_INFO) and passes it to the local transmitter (e.g., transmitter 302). Once convergence is achieved, receiver 301 is ready to begin normal operations.

[0032] Fig. 5 shows an illustrative transmitter 302 suitable for use in the PMA circuits 300. During normal operations, demultiplexer 502 and multiplexer 503 supply blocks of channel bits or symbols from the remote end node conveyed by the RXD bus to the parallel to serial (P2S) circuit 504. P2S circuit converts the blocks into a digital data stream. A transmit filter 506, also called a pre-emphasis filter, converts the digital data stream into an analog electrical signal with spectral shaping to combat channel degradation. Driver 508 amplifies the analog electrical signal to drive the channel output (CH_OUT) node.

[0033] During the auto-negotiation phase, illustrated demultiplexer 502 directs digital samples of the received auto-negotiation signals received from the remote end node and conveyed via the RXD bus to a digital-to-analog converter (DAC) 520. DAC 520 converts the digital samples into an analog electrical signal that reproduces the received auto-negotiation signals. Driver 508 amplifies the analog electrical signal to drive the channel output (CH_OUT) node. If the ADC path is omitted from receiver (Fig. 4), the DAC path may also be omitted from the transmitter. The normal operations path may be employed with an untrained (default) transmit filter. As another alternative, a switchable on-chip analog signal line may couple LNA 402 for a local end node to the driver 508 for a remote end node.

[0034] During the training phase, multiplexer 503 obstructs information from the RXD bus, instead supplying P2S circuit 504 with training frames from a training controller 540. The training controller 540 generates the training frames based on the convergence status and

Marvell Semiconductor, Inc. - Ex. 1002, Page 000022

transmit filter coefficient adjustments (LOCAL_INFO) received from the local receiver (e.g., receiver 301). Note that even after the local receiver indicates filter convergence has occurred, the training controller 540 may prolong the training phase to coordinate training phase timing with the receiver for the remote end node (e.g., receiver 311). The training frames further include training sequences as specified by the relevant portions of the IEEE Std 802.3.

[0035] The training controller 540 further accepts the back-channel information (BACK_INFO) extracted by the local receiver from received training frames sent by the local end node. The training controller applies the corresponding adjustments to the coefficients of transmit filter 506. Upon conclusion of the training phase, multiplexer 503 begins forwarding RXD blocks to the P2S circuit 504.

[0036] Fig. 6 is a flowchart of an illustrative Ethernet link extension method. It begins in block 602 with a technician or user connecting end nodes of an Ethernet link via an intermediate link extender. When each end node powers up, or periodically thereafter, it initiates an auto-negotiation phase to set up the link. In block 604, the extender conceals itself during the auto-negotiation phase, transparently passing the signals received from each end node to the other end node. The signals may be passed through the extender as analog signals; as analog-to-digital and digital-to-analog converted waveforms, or as demodulated and remodulated data frames. In other words, a transmitter of a second PMA (physical medium attachment) circuit is coupled to a receiver of a first PMA circuit to retransmit communications received from a first node; and a transmitter of the first PMA circuit is coupled to a receiver of the second PMA circuit to retransmit communications received from the second node.

[0037] During the auto-negotiation phase, the extender monitors the received signals until, in block 606, the end of the auto-negotiation phase is detected. As discussed previously, the extender may perform this detection by decoding information from the auto-negotiation frames exchanged between the end nodes and/or by monitoring the spectra for high-frequency content typical of training sequences. Having detected the end of the auto-negotiation phase from either end node on a given lane, the extender initiates the training phase on that lane for both end nodes simultaneously in block 608. Training controllers for each of the first and second PMA circuits generate training frames for transmission by the transmitter of the

Marvell Semiconductor, Inc. - Ex. 1002, Page 000023

respective PMA circuit based in part on back-channel information and training status information from the local receiver of the respective PMA circuit.

[0038] The training phase is performed concurrently for both end nodes, prolonged if necessary until the links are trained for both end nodes in block 610, indicating that the training phase can be concluded for both. The extender then signals the end of the training phase on that lane to both end nodes and enters the frame-forwarding phase in block 612.

[0039] In the frame-forwarding phase of block 612, the extender demodulates the channel data frames to extract the channel bits or symbols from each end node. The channel bits or symbols are then remodulated for transmission to the other end node, obviating any need for a PCS sublayer and thereby minimizing latency and power consumption with minimal impairment to link robustness. In some extender embodiments, the extender monitors the equalization error levels, or performs checksum calculations to detect errors. If a fault is detected, in block 614 the extender temporarily disables the transmitters for that lane to force re-initiation of the link, and the method then repeats beginning with block 604.

[0040] Numerous alternative forms, equivalents, and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. For example, the foregoing description focuses on implementations employing only one link extender between end nodes, but the disclosed principles would still apply if multiple extenders are provided in sequence between the end nodes. It is intended that the claims be interpreted to embrace all such alternative forms, equivalents, and modifications that are encompassed in the scope of the appended claims.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000024

CLAIMS

What is claimed is:

1. An Ethernet link extender that comprises:

a first PMA (physical medium attachment) circuit having a transmitter and a receiver that communicate in a sequence of phases with a first node, the sequence including at least an auto-negotiation phase and a subsequent training phase; and

a second PMA circuit having a transmitter and a receiver that communicate in said sequence of phases with a second, different node, the phases in said sequence being simultaneous for the first and second PMA circuits,

the transmitter of the second PMA circuit being coupled to the receiver of the first PMA circuit during the auto-negotiation phase to retransmit communications received from the first node,

the transmitter of the first PMA circuit being coupled to the receiver of the second PMA circuit during the auto-negotiation phase to retransmit communications received from the second node, and

the first and second PMA circuits each including a respective training controller that, during the training phase, generates training frames for transmission by the transmitter of the respective PMA circuit based in part on back-channel information and training status information from the receiver of the respective PMA circuit.

2. The extender of claim 1, wherein said coupling of the transmitter of the second PMA circuit to the receiver of the first PMA circuit during the auto-negotiation phase is via an on-chip analog signal line.

3. The extender of claim 1, wherein said coupling of the transmitter of the second PMA circuit to the receiver of the first PMA circuit during the auto-negotiation phase is via a digital signal bus between an analog-to-digital converter and a digital-to-analog converter.

4. The extender of claim 1, wherein the transmitter of the first PMA circuit and the transmitter of the second PMA circuit each include a transmit filter adapted in accordance with back-channel information received from the first and second nodes, respectively, during the training phase.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000025

5. The extender of claim 1, wherein the receiver of the first PMA circuit and the receiver of the second PMA circuit each include a filter adaptation circuit that generates filter coefficient updates and detects filter convergence.

6. The extender of claim 5, wherein at least one of the transmitter of the first PMA circuit and the transmitter of the second PMA circuit includes a training controller providing back-channel information to at least one of the first and second nodes, and wherein the training controller confirms filter convergence only when filter converge is detected by both the receiver of the first PMA circuit and the receiver of the second PMA circuit.

7. The extender of claim 1, wherein the receiver of the first PMA circuit and the receiver of the second PMA circuit each include detector, and wherein the extender initiates a training phase when either of the detectors detects an end of the auto-negotiation phase.

8. The extender of claim 7, wherein the detectors monitor spectra of received signals for high-frequency content indicative of training frames.

9. The extender of claim 7, wherein the detectors decode information from auto-negotiation frames to detect said end.

10. The extender of claim 1, wherein each of the first PMA circuit and the second PMA circuit include multiple transmitter-receiver pairs to support multiple communication lanes between the first and second nodes.

11. An Ethernet link extension method that comprises,

in a first communications phase for auto-negotiation:

coupling a transmitter of a second PMA (physical medium attachment) circuit to a receiver of a first PMA circuit to retransmit communications received from a first node; and

coupling a transmitter of the first PMA circuit to a receiver of the second PMA circuit to retransmit communications received from a second node; and

in a subsequent communications phase for training:

generating, with a respective training controller for each of the first and second PMA circuits, training frames for transmission by the transmitter of the respective PMA circuit

Marvell Semiconductor, Inc. - Ex. 1002, Page 000026

based in part on back-channel information and training status information from the receiver of the respective PMA circuit.

12. The method of claim 11, wherein said coupling of the transmitter of the second PMA circuit to the receiver of the first PMA circuit during the auto-negotiation phase is via an on-chip analog signal line.

13. The method of claim 11, wherein said coupling of the transmitter of the second PMA circuit to the receiver of the first PMA circuit during the auto-negotiation phase includes:

digitizing communications received from the first node to obtain received signal samples;

conveying the received signal samples on a bus to the transmitter of the second PMA circuit; and

converting the received signal samples into an analog electrical transmit signal.

14. The method of claim 1, further comprising adapting a transmit filter in each of the transmitter of the first PMA circuit and the transmitter of the second PMA circuit in accordance with back-channel information received from the first and second nodes, respectively, during the training phase.

15. The method of claim 11, further comprising generating filter coefficient updates and detecting filter convergence with a filter adaptation circuit in each of the receiver of the first PMA circuit and the receiver of the second PMA circuit.

16. The method of claim 15, further comprising:

providing back-channel information to the first and second nodes with a training controller in each of the transmitter of the first PMA circuit and the transmitter of the second PMA circuit; and

confirming filter convergence with each of the training controllers only when filter converge is detected by both the receiver of the first PMA circuit and the receiver of the second PMA circuit.

17. The method of claim 11, initiating the training phase when either, but before both, the receiver of the first PMA circuit and the receiver of the second PMA circuit detects an end of the auto-negotiation phase.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000027

18. The method of claim 17, further comprising monitoring spectra of received signals for high-frequency content to detect said end of the auto-negotiation phase.

19. The method of claim 17, further comprising decoding information from auto-negotiation frames to detect said end.

20. The method of claim 11, wherein each of the first PMA circuit and the second PMA circuit include multiple transmitter-receiver pairs to support multiple communication lanes between the first and second nodes.

21. An Ethernet link extension method that comprises,

in a first communications phase for auto-negotiation:

coupling a transmitter of a second PMA (physical medium attachment) circuit to a receiver of a first PMA circuit to retransmit channel signal waveforms received from a first node;

coupling a transmitter of the first PMA circuit to a receiver of the second PMA circuit to retransmit channel signal waveforms received from a second node; and

monitoring spectra of the channel signal waveforms received from at least one of the first and second nodes to detect an end of the auto-negotiation phase; and

in a subsequent frame-forwarding phase:

demodulating communications received from the first node by the receiver of the first PMA circuit to obtain a first digital channel symbol or bit stream;

conveying the first digital channel symbol or bit stream to the transmitter of the second PMA circuit for transmission to the second node;

demodulating communications received from the second node by the receiver of the second PMA circuit to obtain a second digital channel symbol or bit stream; and

conveying the second digital channel symbol or bit stream to the transmitter of the first PMA circuit for transmission to the first node.

22. The method of claim 21, wherein said coupling of the transmitter of the second PMA circuit to the receiver of the first PMA circuit during the first communications phase is via an on-chip

Marvell Semiconductor, Inc. - Ex. 1002, Page 000028

analog signal line.

23. The method of claim 21, wherein said coupling of the transmitter of the second PMA circuit to the receiver of the first PMA circuit during the first communications phase includes:

digitizing channel signal waveforms received from the first node to obtain received signal samples;

conveying the received signal samples on a bus to the transmitter of the second PMA circuit; and

converting the received signal samples into an analog electrical transmit signal.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000029

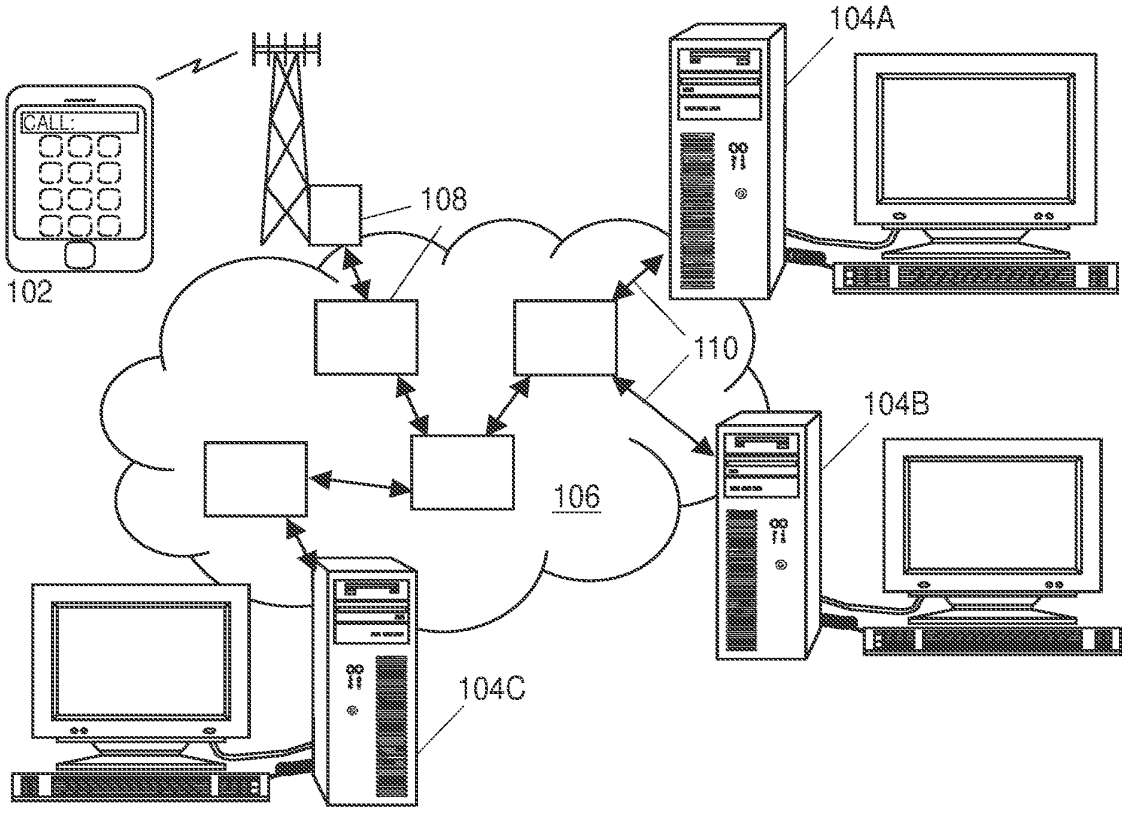


FIG. 1

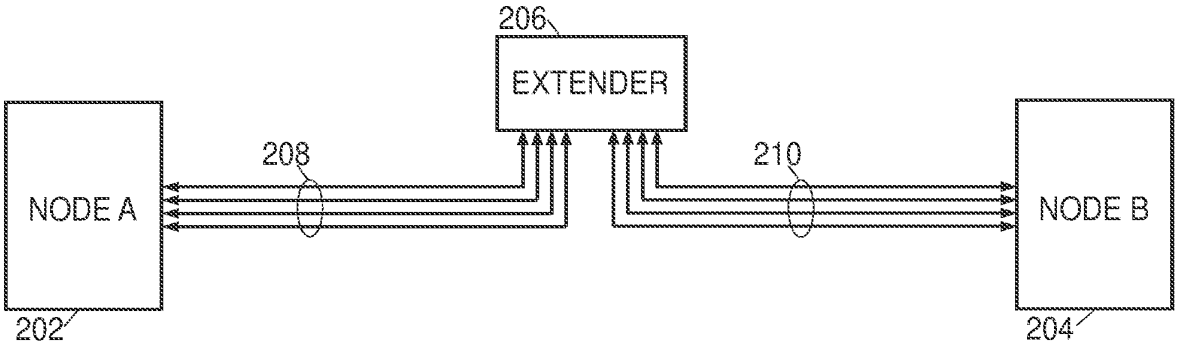


FIG. 2

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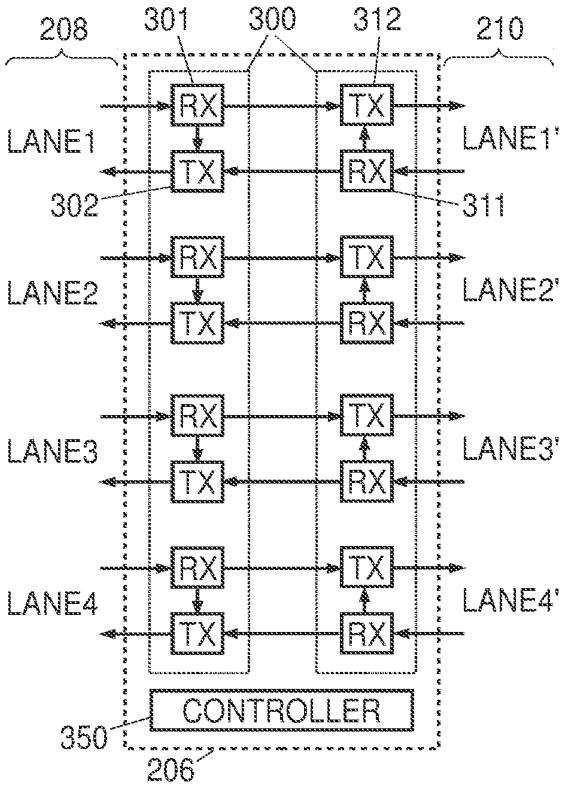


FIG. 3

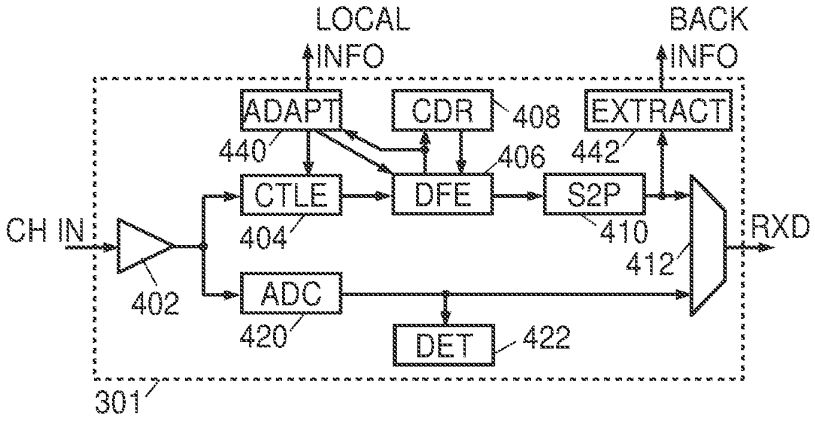


FIG. 4

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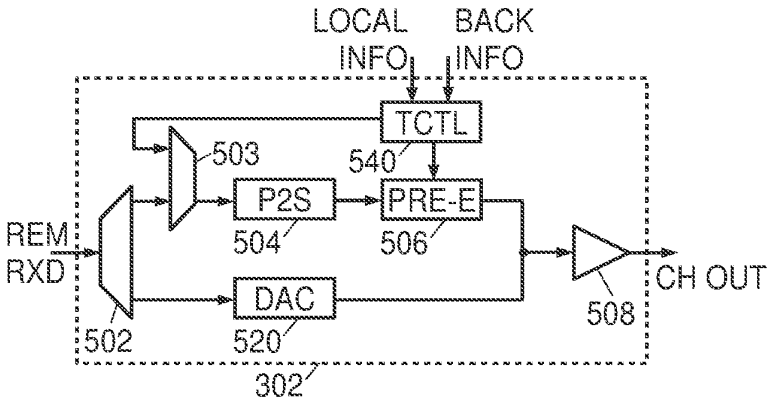


FIG. 5

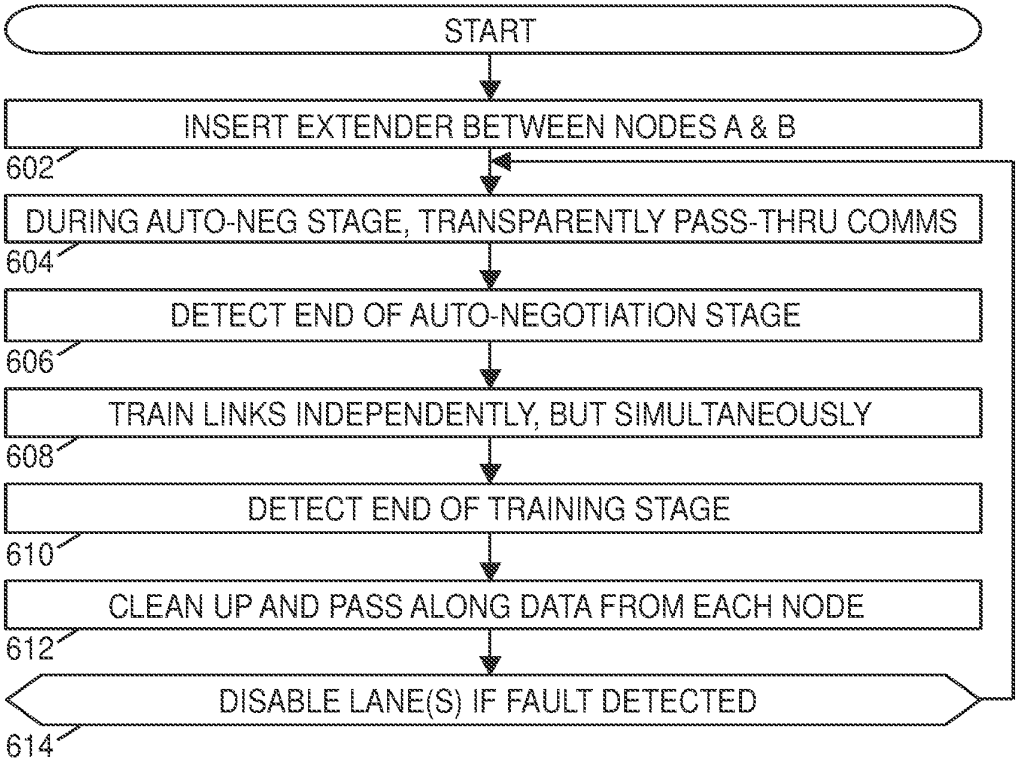


FIG. 6

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2017/075961

A. CLASSIFICATION OF SUBJECT MATTER

H04L 12/24(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, WPI, EPODOC, IEEE: 802.3, ethernet, extend+, PMA, physical medium attachment, auto w negotiation, training, data, phase, back w channel, modulat+, convey+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014146833 A1 (LUSTED, KENT C. ET AL.) 29 May 2014 (2014-05-29) abstract, description, paragraphs [0042]-[0059], [0098]-[0104], [0119]-[0122] and figure 1	1-23
X	US 2014086264 A1 (LUSTED, KENT C. ET AL.) 27 March 2014 (2014-03-27) abstract, description, paragraphs [0041]-[0054], [0099]-[0107], [0119]-[0122] and figure 1	1-23
X	US 2013343400 A1 (LUSTED, KENT C. ET AL.) 26 December 2013 (2013-12-26) abstract, description, paragraphs [0036]-[0049], [0082] and figure 1	1-23
A	CN 1941649 A (BROADCOM CORPORATION) 04 April 2007 (2007-04-04) the whole document	1-23
A	LAN/MAN Standards Committee of the IEEE Computer Society. "IEEE Standard for Ethernet" *IEEE Std 802.3™-2015*, 03 September 2015 (2015-09-03), the whole document	1-23

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

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PCT/CN2017/075961

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2014146833	A1	29 May 2014	JP	2014107869	A	09 June 2014
				DE	202013105453	U1	06 November 2014
US	2014086264	A1	27 March 2014	JP	2014068345	A	17 April 2014
				DE	202013104344	U1	20 February 2014
US	2013343400	A1	26 December 2013	WO	2013191912	A1	27 December 2013
				CN	104322014	A	28 January 2015
				CA	2908681	A1	27 December 2013
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				US	2013243011	A1	19 September 2013
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				US	2007076722	A1	05 April 2007
				US	2011205934	A1	25 August 2011
				DE	602006003500	E	18 December 2008

Marvell Semiconductor, Inc. - Ex. 1002, Page 000034

EE Times

Marvell Semiconductor, Inc. - Ex. 1002, Page 000035

DESIGNLINES | MILITARY & AEROSPACE DESIGNLINE

Fighting Jitter in Fibre-Channel Designs

Fighting Jitter in Fibre-Channel Designs

By **Bob Rumer**, 02.01.01 0

Routing multiple serial signals can be a daunting task during the development of fibre channel systems. Fortunately, digitalrepeaters and retimer ICs can clean up signals and counteract jitter in order to ensure spec compliance.

Storage area networking (SAN) and network attached storage (NAS) have garnered a great deal of attention in the communication market as the demand for sophisticated e-commerce and mission-critical systems has exploded over the past year. Estimates of future growth optimistically point to widespread deployment of these systems to distribute databases, Web pages, streaming video, and movies-on-demand.

A chief concern of designers of SAN and NAS equipment is, of course, fast access to files. Merely locating audio clips, video clips, and large databases is not enough; fast access and loading of the data is critical. To this end, fibre channel has emerged as a fast and reliable method for making SAN and NAS equipment a reality.

Fibre channel uses high-speed serial links at either 1.0625- or 2.125-Gbps data rates to link servers, switches, routers, disk arrays, tape systems, and RAID controllers into complex, redundantly interconnected networks which allow user access to data in the presence of component failures. Fibre channel-derived SAN architectures are now being deployed in increasingly complex and creative ways to solve serious data availability issues which, to-date, have been unsolvable. Designers implementing these systems must ensure physical layer interoperability in order to reliably deliver future scaleability to users.

Unfortunately, designing robust gigabit speed serial links is typically viewed as a black art beyond the skill of most system architects. The most challenging area is jitter, which can adversely affect the reliability of data transfer through the link. As you'll see, repeaters and retimers can be used to mitigate these difficulties and, with care, provide signals that comply with all jitter-related industry specifications. To better illustrate the impact of repeaters and retimers, let's start with a more detailed look at the physical layer of fibre channel links.

Speeding the connection

At the transmit source of a fibre channel architecture, 8 b of raw data are encoded into a 10-b character using the 8B/10B encoding scheme. This encoding scheme provides the encoded data with several critical properties of value in serial data communications. 10-b data is serialized and transmitted through a high-speed, differential output buffer, onto copper cable or into an optical transceiver for conversion to light. This is done with an output buffer that uses either positive emitter coupled logic (PECL) or current mode logic (CML).

At the other end of the fibre channel link, high-speed differential data from the copper cable or output of an optical transceiver is input to a high-speed, differential input buffer that drives a clock and data recovery (CDR) unit. This CDR extracts a bit-rate clock from the serial data, samples the data, then deserializes and

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Management Data Input/Output

Management Data Input/Output (MDIO), also known as **Serial Management Interface (SMI)** or **Media Independent Interface Management (MIIM)**, is a serial bus defined for the Ethernet family of IEEE 802.3 standards for the Media Independent Interface, or **MII**. The MII connects Media Access Control (MAC) devices with Ethernet physical layer (PHY) circuits. The MAC device controlling the MDIO is called the Station Management Entity (SME).

Contents

Relationship with MII
Electrical specification
Bus timing (clause 22)
MDIO Packet Format (clause 22)
Commands
References

Relationship with MII

MII has two signal interfaces:

- A Data interface to the Ethernet MAC, for sending and receiving Ethernet frame data.
- A PHY management interface, MDIO, used to read and write the control and status registers of the PHY in order to configure each PHY before operation, and to monitor link status during operation.

Electrical specification

The MDIO interface is implemented by two signals:

- MDC clock: driven by the MAC device to the PHY.
- MDIO data: bidirectional, the PHY drives it to provide register data at the end of a read operation.

The bus only supports a single MAC as the master, and can have up to 32 PHY slaves.

The MDC can be periodic, with a minimum period of 400 ns, which corresponds to a maximum frequency of 2.5 MHz. Newer chips, however, allow faster accesses.

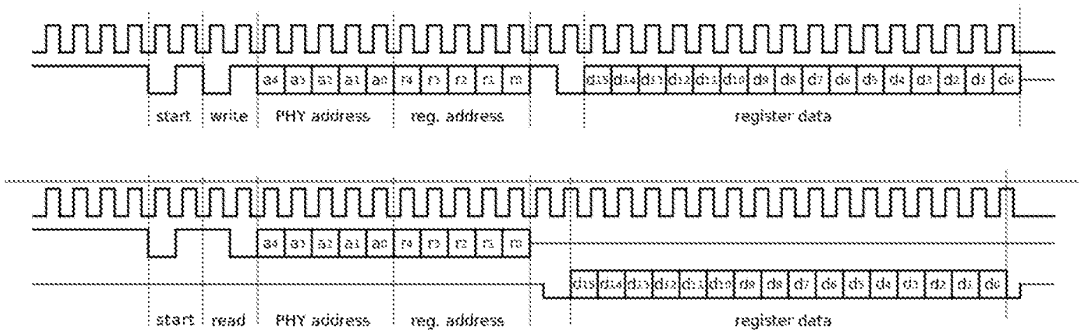
The MDIO requires a specific pull-up resistor of 1.5 kΩ to 10 kΩ, taking into account the total worst-case leakage current of 32 PHYs and one MAC.

Bus timing (clause 22)

Before a register access, PHY devices generally require a preamble of 32 ones to be sent by the MAC on the MDIO line. The access consists of 16 control bits, followed by 16 data bits. The control bits consist of 2 start bits, 2 access type bits (read or write), the PHY address (5 bits), the register address (5 bits), and 2 "turnaround" bits.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000038

During a write command, the MAC provides address and data. For a read command, the PHY takes over the MDIO line during the turnaround bit times, supplies the MAC with the register data requested, then releases the MDIO line.



When the MAC drives the MDIO line, it has to guarantee a stable value 10 ns (setup time) before the rising edge of the clock MDC. Further, MDIO has to remain stable 10 ns (hold time) after the rising edge of MDC.

When the PHY drives the MDIO line, the PHY has to provide the MDIO signal between 0 and 300 ns after the rising edge of the clock.[1] Hence, with a minimum clock period of 400 ns (2.5 MHz maximum clock rate) the MAC can safely sample MDIO during the second half of the low cycle of the clock.

MDIO Packet Format (clause 22)

	MDIO Packet Format																															
Bit:	**0**	**1**	**2**	**3**	**4**				**8**	**9**				**13**	**14**	**15**	**16**															**31**
0	PRE_32																															
32	ST		OP		PA5				RA5					TA	D16																	

PRE_32

The first field in the MDIO header is the Preamble. During the preamble, the MAC sends 32 bits, all '1', on the MDIO line.

ST

The Start field consists of 2 bits and always contains the combination '01'.

OP

The Opcode consists of 2 bits. There are two possible opcodes, read '10' or write '01'.

PA5

5 bits, PHY address.

RA5

The Register Address field indicates the register to be written to or read from. It is 5 bits long.

TA

Marvell Semiconductor, Inc. - Ex. 1002, Page 000039

The turn-around field is 2 bits long. When data is being written to the PHY, the MAC writes '10' to the MDIO line. When data is being read, the MAC releases the MDIO line.

D16

16 bits, data. This can be sent by either the SME or the PHY, depending on the value of the OP field.

Z

Tristate MDIO.

Commands

IEEE 802.3 Part [2] use different opcodes and start sequences. Opcodes 00(set address) and 11(read)/01(write) /10(read increment) are used as two serial transactions to read and write registers.

References

1. "IEEE 802.3 Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method and Physical Layer specification" (http://standards.ieee.org/getieee802/download/802.3-2008_section2.pdf) (PDF). IEEE. Retrieved February 29, 2012.
2. "IEEE 802.3 Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method and Physical Layer specification" (http://standards.ieee.org/getieee802/download/802.3-2008_section2.pdf) (PDF). IEEE. Retrieved February 29, 2012.

[1]

1. http://www.ieee802.org/3/efm/public/nov02/oam/pannell_oam_1_1102.pdf

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000040

QSFP-DD MSA

QSFP-DD Hardware Specification

for

QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER

Rev 4.0 Candidate August 15, 2018

Abstract: This specification defines: the electrical and optical connectors, electrical signals and power supplies, mechanical and thermal requirements of the pluggable QSFP Double Density (QSFP-DD) module, connector and cage system. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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Intel
Juniper Networks
Lumentum
Luxtera
Mellanox
Molex LLC
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Sicoya
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Spirent
Sumitomo Electric
US Conec
Xilinx
Yamaichi

Change History:

Revision	Date	Changes
1.0	Sept 19 2016	First public release
2.0	March 13 2017	Second public release
3.0	Sept 19 2017	Third public release
4.0	Aug 14 2018	Fourth public release, Additions to thermal section 6, synchronous clocking section 4.4, Mechanical updates

Foreword

The development work on this specification was done by the QSFP-DD MSA, an industry group. The membership of the committee since its formation in Feb 2016 has included a mix of companies which are leaders across the industry.

CONTENTS

1 Scope 7
1.1 Description of Sections *7*
2 References 7
2.1 Industry Documents *7*
2.2 Sources *8*
3 Introduction 8
3.1 Objectives *8*
3.2 Applications *9*
4 Electrical Specification 9
4.1 Electrical Connector *9*
4.1.1 Low Speed Electrical Hardware Signals 16
4.1.2 Low Speed Electrical Specification 17
4.1.3 Timing for soft control and status functions 18
4.1.4 High Speed Electrical Specification 21

DRAFT

Marvell Semiconductor, Inc. - Ex. 1002, Page 000043

4.2 Power Requirements *22*
4.2.1 Power Classes and Maximum Power Consumption 22
4.2.2 Host Board Power Supply Filtering 22
4.2.3 Module Power Supply Specification 23
4.2.4 Host Board Power Supply Noise Output 24
4.2.5 Module Power Supply Noise Output 24
4.2.6 Module Power Supply Noise Tolerance 24
4.3 ESD *26*
4.4 Clocking Considerations *26*
4.4.1 Data Path Description 26
4.4.2 Tx Clocking Considerations 26
4.4.3 Rx Clocking Considerations 26
5 Mechanical and Board Definition 27
5.1 Introduction *27*
5.2 Datums, Dimensions and Component Alignment *28*
5.3 Module Mechanical Dimensions *31*
5.4 Module Flatness and Roughness *37*
5.5 Module paddle card dimensions *38*
5.6 Module Extraction and Retention Forces *41*
5.7 2x1 Electrical Connector Mechanical *42*
5.7.1 2x1 Connector and Cage host PCB layout 46
5.8 Surface Mount Electrical Connector Mechanical *49*
5.8.1 Surface mount connector and cage host PCB layout 55
5.9 Module Color Coding and Labeling *57*
5.10 Optical Interface *58*
5.10.1 MPO Optical Cable connections 59
5.10.2 Dual LC Optical Cable connection 61
5.10.3 Dual CS Optical Cable connection 61
5.10.4 Electrical data input/output to optical port mapping 62
6 Environmental and Thermal 62
6.1 Thermal Requirements *62*
6.2 Thermal Requirements – tighter controlled environments *63*
6.3 External Case and Handle Touch Temperature *63*
7 Management Interface 63
7.1 SCL, SDA and ModSEL Timing Specification *64*
7.1.1 Introduction 64
7.1.2 Management Interface Timing Specification 64
7.1.3 Serial Interface Protocol 65
Appendix A: Informative overall module length with elastomeric handle attached to module latches *67*

Marvell Semiconductor, Inc. - Ex. 1002, Page 000044

Table 1- Pad Function Definition..... 12
Table 2- Low Speed Control and Sense Signals..... 18
Table 3- Timing for QSFP-DD soft control and status functions..... 19
Table 4- I/O Timing for Squelch & Disable..... 20
Table 5- Power Classes..... 22
Table 6- Power Supply specifications, Instantaneous, sustained and steady state current limits..... 25
Table 7- Datums..... 29
Table 8- Module flatness specifications..... 37
Table 9- Insertion, Extraction and Retention Forces..... 41
Table 10- Electrical Signal to Optical Port Mapping..... 62
Table 11- Temperature Range Class of operation..... 62
Table 12- Temperature Range Classes for Tighter Controlled Applications..... 63
Table 13- Management Interface timing parameters..... 66

DRAFT

Marvell Semiconductor, Inc. - Ex. 1002, Page 000045

Figure 1: Application Reference Model..... 9
Figure 2: Module pad layout..... 11
Figure 3: Example QSFP-DD Host Board Schematic For Optical Modules..... 14
Figure 4: Example QSFP-DD Host Board Schematic for active copper cables..... 15
Figure 5: Example QSFP-DD Host Board Schematic for passive copper cables..... 16
Figure 6: Recommended Host Board Power Supply Filtering..... 23
Figure 7: Instantaneous and sustained peak currents for Icc Host (see Fig. 6)..... 24
Figure 8: 2x1 stacked cage and module..... 27
Figure 9: Press fit cage for surface mount (SMT) connector..... 27
Figure 10: Type 1 Pluggable module..... 28
Figure 11: Type 2 Pluggable module..... 28
Figure 12: 2X1 stacked connector/cage datum descriptions..... 30
Figure 13: Surface mount connector/cage datum descriptions..... 31
Figure 14: Type 1 Module..... 32
Figure 15: Type 2 Module..... 32
Figure 16: Drawing of module..... 34
Figure 17: Detailed dimension of module..... 36
Figure 18: Module paddle card dimensions..... 39
Figure 19: Module pad dimensions..... 40
Figure 20: Integrated connector in 2x1 stacked cage..... 42
Figure 21: 2x1 stacked cage..... 43
Figure 22: 2x1 stacked cage dimensions..... 44
Figure 23: Connector pins in 2x1 stacked cage as viewed from the front..... 45
Figure 24: 2x1 Bezel Opening..... 45
Figure 25: 2X1 host board connector contacts..... 46
Figure 26: 2X1 Host PCB Mechanical Layout..... 48
Figure 27: SMT connector in 1xn cage..... 49
Figure 28: SMT 1x1 Cage Design..... 51
Figure 29: SMT 1x1 Connector Design..... 53
Figure 30: SMT 1x1 bezel opening..... 54
Figure 31: SMT Host PCB Mechanical Layout..... 55
Figure 32: SMT Connector and Host PCB Pin Numbers..... 56
Figure 33: Optical Media Dependent Interface port assignments..... 58
Figure 34: MPO-12 Single Row optical patch cord and module receptacle..... 59
Figure 35: MPO-16 Single Row optical patchcord and module receptacle..... 60
Figure 36: MPO-12 Two Row optical patchcord and module receptacle..... 60
Figure 37: Dual LC optical patchcord and module receptacle..... 61
Figure 38: Dual CS connector module receptacle (in support of breakout applications)... 61
Figure 39: QSFP-DD Timing Diagram..... 64
Figure 40: SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times... 65
Figure 41: Informative overall module length with handle for Type 1 module..... 67
Figure 42: Informative overall module length with handle for Type 2 module..... 67

Marvell Semiconductor, Inc. - Ex. 1002, Page 000046

QSFP-DD 8X Pluggable Transceiver

1 Scope

The scope of this specification is the definition of a high density 8-channel (8x) module, cage and connector system. QSFP-DD supports up to 400 Gb/s in aggregate over an 8 x 50 Gb/s electrical interface. The cage and connector design provides backwards compatibility to QSFP28 modules which can be inserted into a QSFP-DD port and connected to 4 of the 8 electrical channels.

1.1 Description of Sections

Section 1 Scope and Purpose

Section 2 Referenced and Related Standards and SFF Specifications

Section 3 Introduction

Section 4 Electrical specifications

Section 5 Mechanical specifications and printed circuit board recommendations

Section 6 Environmental and thermal considerations

Section 7 Management Interface

2 References

2.1 Industry Documents

The following documents are relevant to this Specification:

- GR-253-CORE
- IEEE Std 802.3™-2018
- IEEE Std 802.3cd
- InfiniBand Architecture Specifications
- FC-PI-6p
- FC-PI-7
- ANSI/TIA-568.3
- TIA-604-5 (FOCIS 5)
- TIA-604-10 (FOCIS 10)
- TIA-604-18 (FOCIS 18)
- IEC 61754-7-1
- ANSI/ESDA/JDEC JS001
- EN6100-4-2
- Common Management Interface Specification for 8X/16X Pluggable Transceivers
- GR63 Section 4.1.7 (Touch Temperature Reference)
- UL 60950-1 Section 4.5.4 (Touch Temperature Reference)
- IEC 31300-3-35
- EIA-964 Specification for QSFP+ 10 Gb/s Pluggable Transceiver
- Keysight Application Brief 5991-2778EN: Methods for characterizing and tuning DC inrush current

SFF Specifications

- SFF-8636 Management Interface for Cabled Environments
- SFF-8472 Diagnostic Monitoring Interface for Optical Transceivers
- SFF-8661 QSFP+ 4X Pluggable Module
- SFF-8679 QSFP28 4X Base Electrical Specification

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000047

CS optical connector specification

- CS-01242017 Revision 1.0 (Can be found at www.QSFP-DD.com)

2.2 Sources

This document can be obtained via the www.QSFP-DD.com web site.

3 Introduction

This Specification covers the following items:

a) Electrical interfaces including pad assignments for data, control, status and power supplies and host PCB layout requirements.

b) Optical interfaces (including optical receptacles and mating fiber plugs for multimode and single-mode duplex and parallel fiber applications). Breakout cable applications are also specified. Optical signaling specifications are not included in this document but are defined in the applicable industry standards.

c) Mechanical specifications including dimensions and tolerances for the connector, cage and module system. Includes details of the requirements for correct mating of the module and host sides of the connector.

d) Thermal requirements

e) Electrostatic discharge (ESD) requirements by reference to industry standard limits and test methods.

This Specification does not cover the following items:

a) Electromagnetic interference (EMI) protection. EMI protection is the responsibility of the implementers of the cages and modules.

b) Memory map definition, which can be found in the 'Common Management Interface Specification for 8x/16x pluggable transceivers' (see www.QSFP-DD.com).

3.1 Objectives

Electrical signal contact and channel assignments, electrical and power requirements defined in Section 4 and optical lane assignments defined in Section 5 ensure that the pluggable modules and cable assemblies are functionally interchangeable. Dimensions, mounting and insertion requirements defined in Section 5 for the bezel, optical module, cable plug, cage and connector system on a circuit board ensure that these products are mechanically interchangeable.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000048

3.2 Applications

This specification defines a common solution for combined eight-channel ports that support Ethernet and/or InfiniBand and/or Fibre Channel requirements. The QSFP-DD interface can support pluggable modules or direct attach cables based on multimode fiber, single mode fiber or copper wires.
An application reference Model, shown in Figure 1, shows the high-speed data interface between an ASIC and the QSFP-DD module.

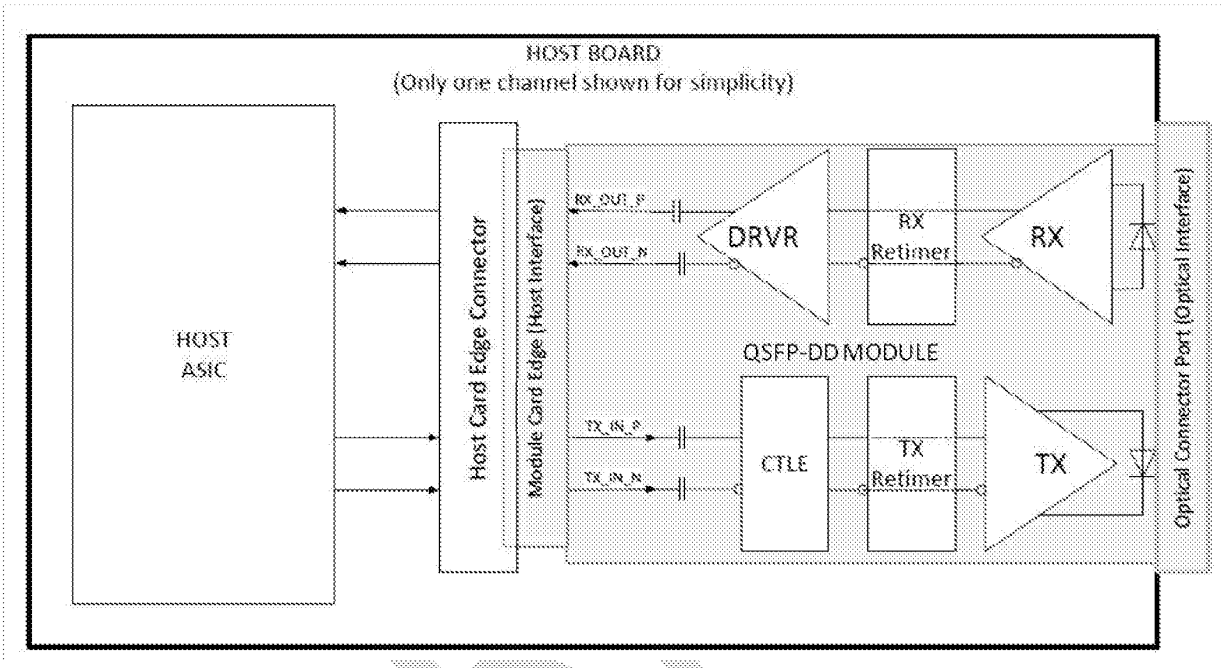


Figure 1: Application Reference Model

Note: For high speed electrical signals the compliance board methodology of IEEE and OIF should be used. Measurements taken with QSFP-DD compliance boards should be corrected for any difference between the loss of these compliance boards and the loss of the compliance boards specified in the standard.

4 Electrical Specification

This section contains signal definitions and requirements that are specific to the QSFP-DD module. High-speed signal requirements including compliance points for electrical measurements are defined in the applicable industry standard.

4.1 Electrical Connector

The QSFP-DD module edge connector consists of a single paddle card with 38 pads on the top and 38 pads on the bottom of the paddle card for a total of 76 pads. The pads are defined in such a manner so as to accommodate insertion of a QSFP module into a QSFP-DD receptacle. The legacy signal locations are deeper on the paddlecard, so that legacy QSFP module pads only connect to the longer row of connector pins, leaving the short row of connector pins unconnected in a QSFP application.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000049

The pads are designed for a sequenced mating:

First mate – ground pads
Second mate – power pads
Third mate – signal pads

Because the QSFP-DD module has 2 rows of pads, the additional QSFP-DD pads will have an intermittent connection with the legacy QSFP pins in the connector during the module insertion and removal. The 'legacy' QSFP pads have a 'B' label shown in Table 1 to designate them as the second row of module pads to contact the QSFP-DD connector. The additional QSFP-DD pads have an 'A' label in Table 1 to designate them as the first row of module pads to contact the QSFP-DD connector. The additional QSFP-DD pads have first, second and third mate to the connector pins for both insertion and removal. Each of the first, second and third mate connections of the legacy QSFP pads and the respective additional QSFP-DD pads are simultaneous.

Figure 2 shows the signal symbols and pad numbering for the QSFP-DD module edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 76 pads intended for high speed signals, low speed signals, power and ground connections. Table 1 provides more information about each of the 76 pads. Figure 18 and Figure 19 show pad dimensions. The connector can be integrated into a 2x1 stacked configuration with 2 ports as illustrated in Figure 8 or a surface mount configuration as shown in Figure 9.

For EMI protection the signals from the host connector should be shut off when the QSFP-DD module is not present. Standard board layout practices such as connections to Vcc and GND with vias, use of short and equal-length differential signal lines are recommended. The chassis ground (case common) of the QSFP-DD module should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000050

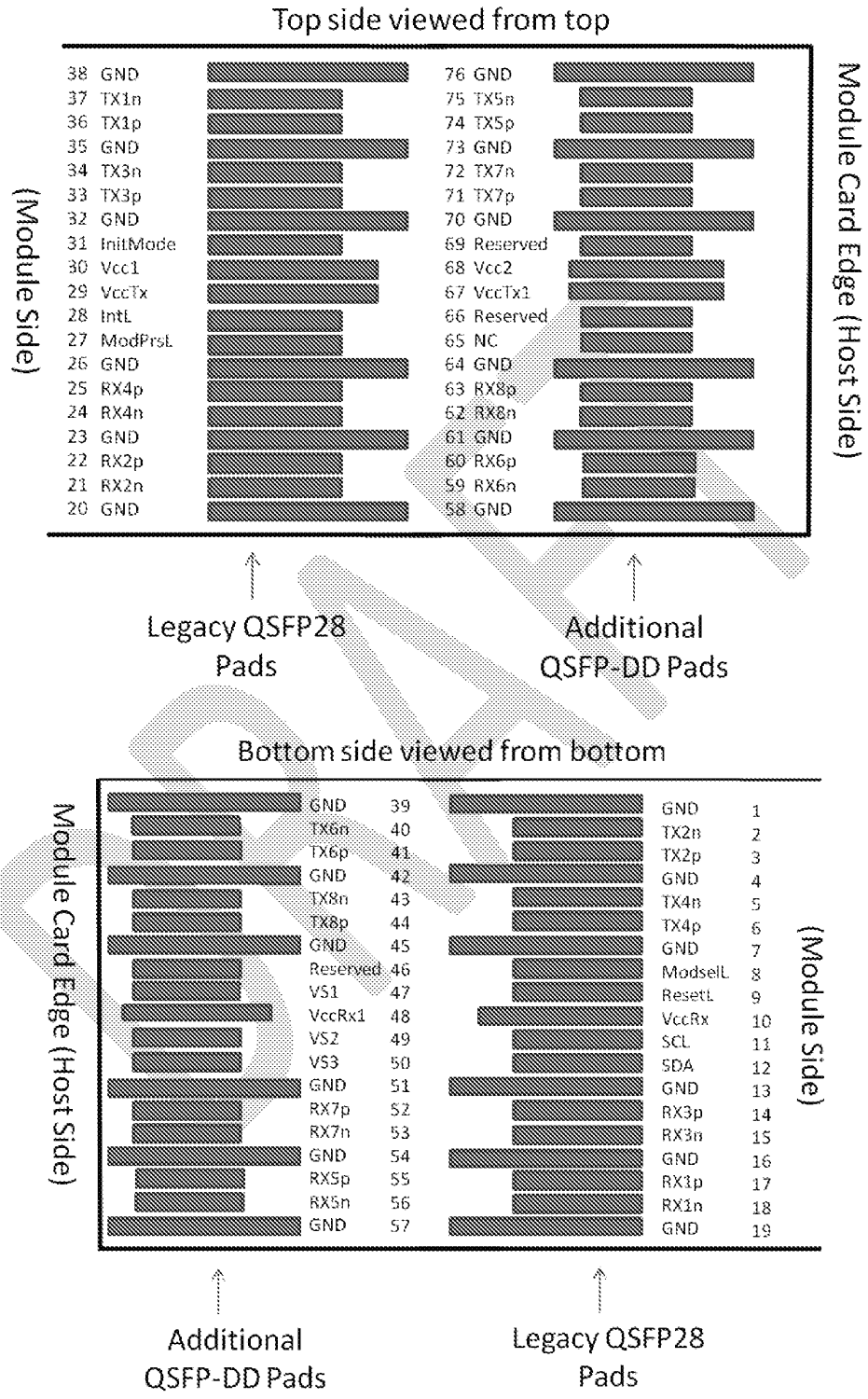


Figure 2: Module pad layout

Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Marvell Semiconductor, Inc. - Ex. 1002, Page 000052

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000053

Figure 3, Figure 4 and Figure 5 show examples of QSFP-DD host PCB schematics with connections to CDR and control ICs. An 8 wide electrical/optical interface is shown. Note alternate electrical/optical interfaces are supported using optical multiplexing (WDM) or electrical multiplexing.

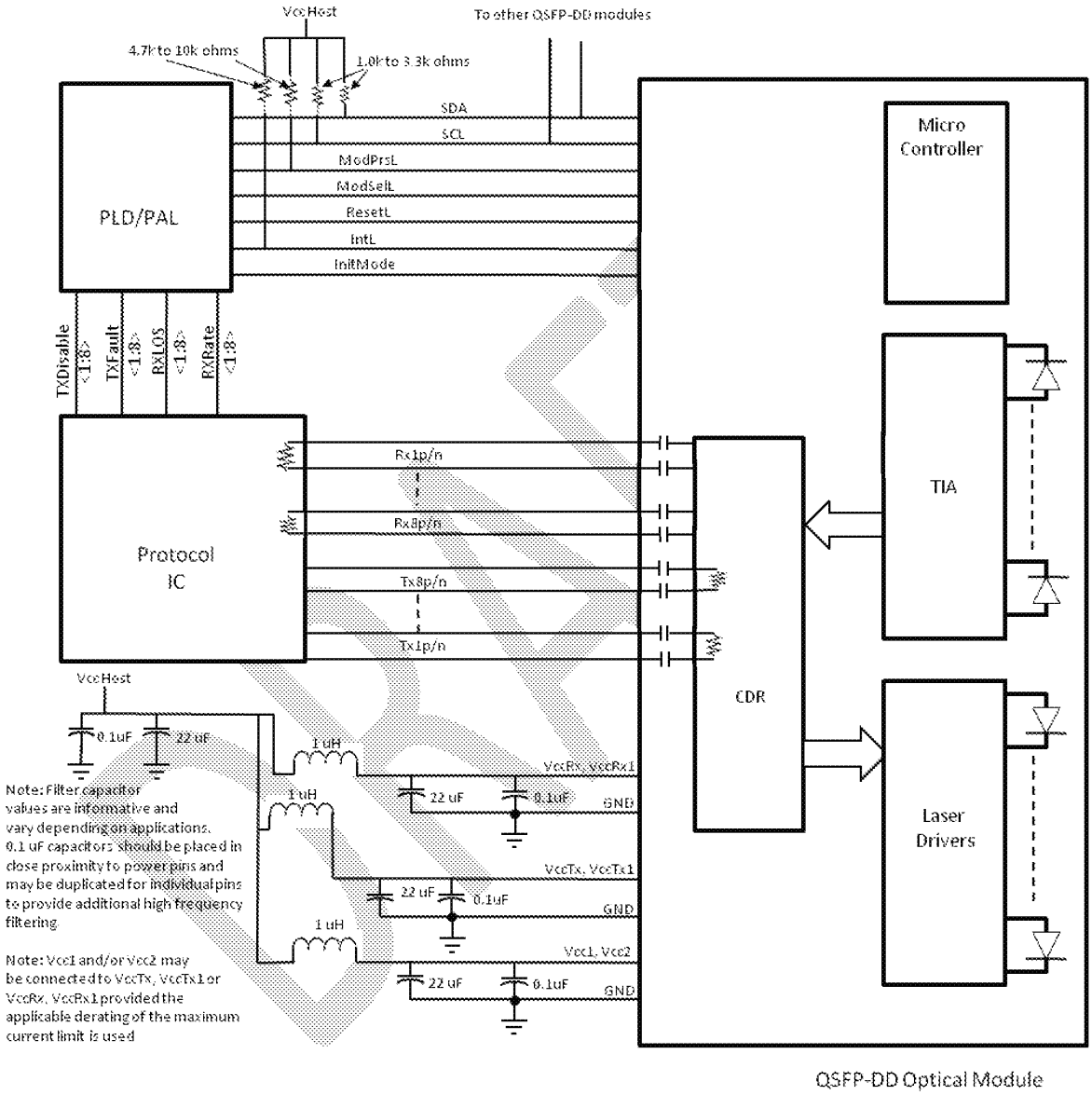


Figure 3: Example QSFP-DD Host Board Schematic For Optical Modules

Marvell Semiconductor, Inc. - Ex. 1002, Page 000054

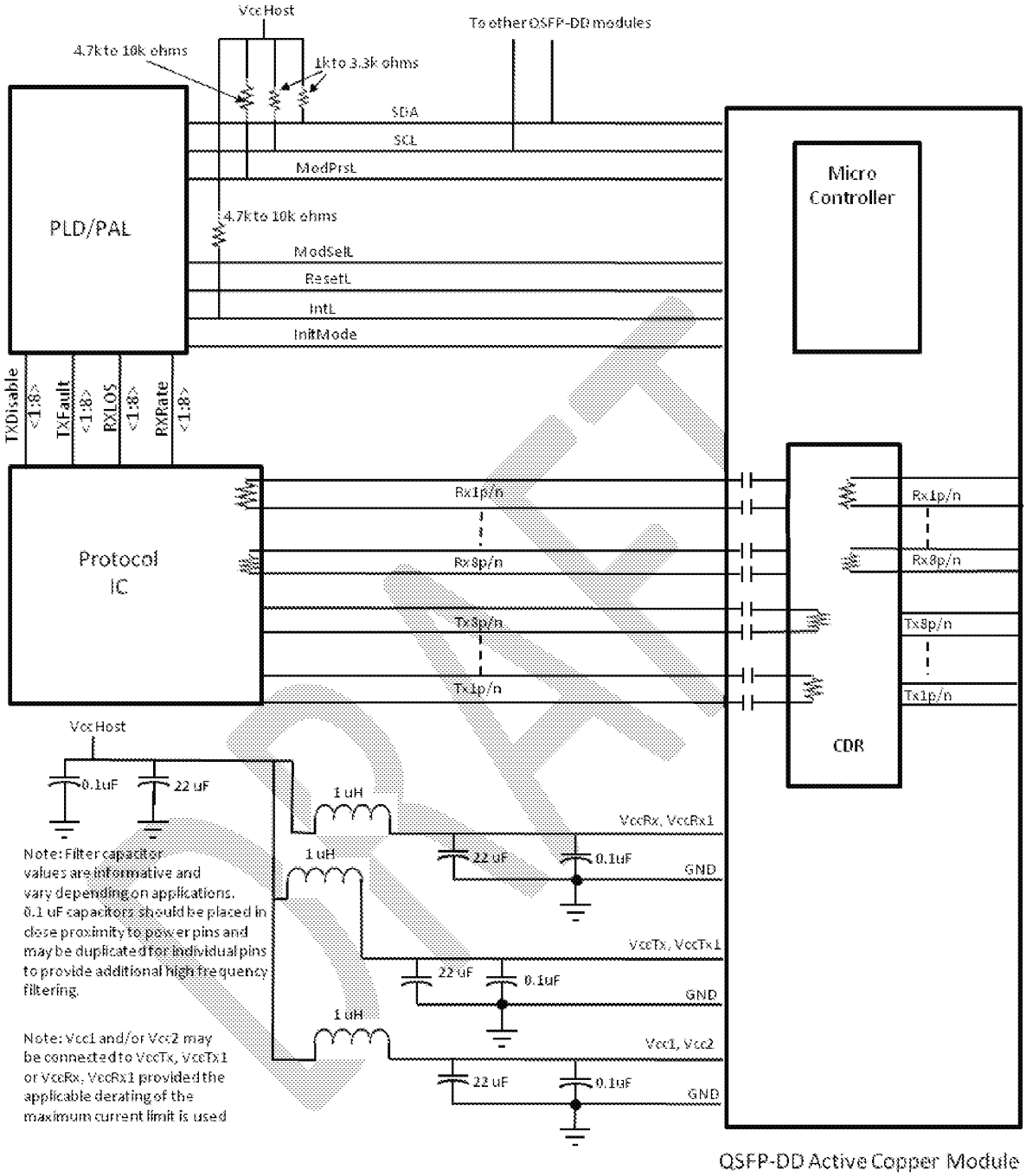


Figure 4: Example QSFP-DD Host Board Schematic for active copper cables

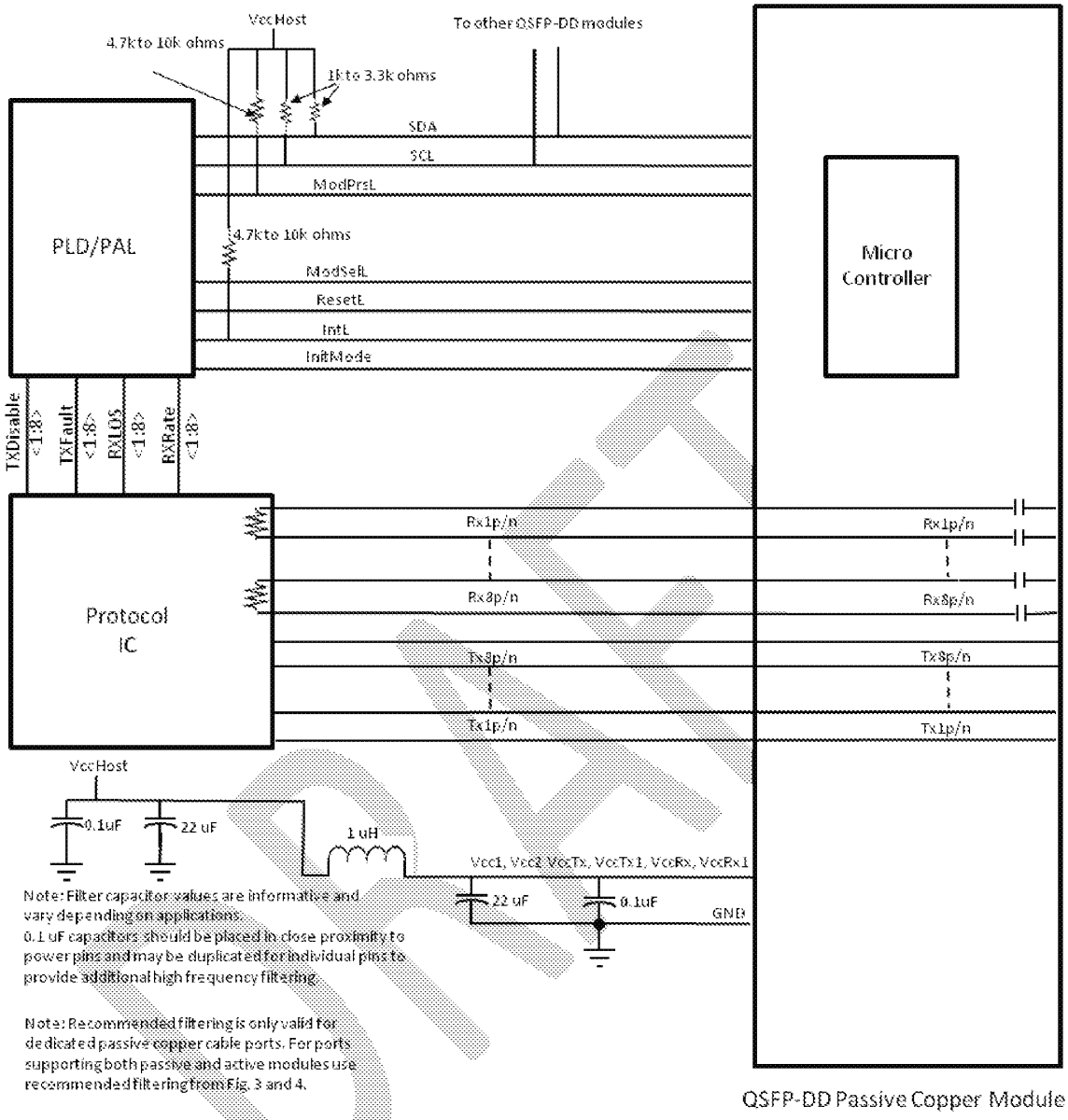


Figure 5: Example QSFP-DD Host Board Schematic for passive copper cables

4.1.1 Low Speed Electrical Hardware Signals

In addition to the 2-wire serial interface the module has the following low speed signals for control and status:

- ModSelL
- ResetL
- InitMode
- ModPrsL
- IntL

Marvell Semiconductor, Inc. - Ex. 1002, Page 000056

4.1.1.1 ModSelL

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module (see Table 2). When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4.1.1.2 ResetL

The ResetL signal shall be pulled to Vcc in the module (see Table 2). A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 3) initiates a complete module reset, returning all user module settings to their default state.

4.1.1.3 InitMode

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module (see Table 2). The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP-DD Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

4.1.1.4 ModPrsL

ModPrsL must be pulled up to Vcc Host on the host board and pulled low in the module (see Table 2). The ModPrsL is asserted "Low" when the module is inserted. The ModPrsL is deasserted "High" when the module is physically absent from the host connector due to the pull-up resistor on the host board.

4.1.1.5 IntL

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board (see Table 2). When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read.

4.1.2 Low Speed Electrical Specification

Low speed signaling other than the SCL and SDA interface is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs (see Table 2). The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

Note: Timing diagrams for SCL and SDA are shown in Section 7.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000057

The QSFP-DD low speed electrical specifications are given in Table 2. This specification ensures compatibility between host bus masters and the 2-wire interface.

Table 2- Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3mA for fast mode, 20ma for Fast-mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400kHz clock rate use 3.0 k Ohms Pullup resistor, max. For 1000kHz clock rate refer to Figure 40
			200	pF	For 400kHz clock rate use 1.6 k Ohms pullup resistor, max. For 1000kHz clock rate refer to Figure 40.
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
	|Iin|		360	uA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	10k ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

4.1.3 Timing for soft control and status functions

Timing for QSFP-DD soft control and status functions are described in Table 3.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000058

Table 3- Timing for QSFP-DD soft control and status functions

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[1], hot plug or rising edge of reset until completion of the MgmtInit State
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Deassert Time (optional fast mode)	toff_losf		3	ms	Time from Rx LOS condition absent to negation of Rx LOS status bit.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[3] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[3] until associated IntL operation resumes
Module Select Wait Time DataPathDeinit Max Duration DataPathInit Max Duration ModulePwrDn Max Duaration	ModSelL Wait Time DataPathDeinit_MaxDuration DataPathInit_MaxDuration ModulePwrDn_MaxDuration				See CMIS Table 40
Note 1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 6.					
Note 2. Measured from the rising edge of SDA in the stop bit of the read transaction					
Note 3. Measured from the rising edge of SDA in the stop bit of the write transaction					
Note 4. Rx LOS condition is defined at the optical input by the relevant standard					

Marvell Semiconductor, Inc. - Ex. 1002, Page 000059

Squelch and disable timings are defined in Table 4.

Table 4- I/O Timing for Squelch & Disable

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached. See Subsection 4.1.4.1.
Rx Squelch Deassert Time	toff_Rxsq	15	ms	Time from resumption of Rx input signals until normal Rx output condition is reached. See subsection 4.1.4.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached. See subsection 4.1.4.2.
Tx Squelch Deassert Time	toff_Txsq	400	ms	Time from resumption of Tx input signals until normal Tx output condition is reached. See subsection 4.1.4.2.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence [1] until optical output falls below 10% of nominal
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Tx Disable Deassert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled
Note 1: Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction				

Marvell Semiconductor, Inc. - Ex. 1002, Page 000060

4.1.4 High Speed Electrical Specification

For detailed electrical specifications see the appropriate specification, e.g. IEEE Std 802.3-2018 Annex 86A, Annex 120E or Annex 120C, FC-PI-6, FC-PI-7, OIF-CEI-28G-VSR, OIF-CEI-56G-VSR or the InfiniBand specification. Partial or complete squelch specifications may be provided in the appropriate specification. Where squelch is not fully defined by the appropriate specification, the recommendations of the following subsections 4.1.4.1 and 4.1.4.2 may be used.

4.1.4.1 Rx(n)(p/n)

Rx(n)(p/n) are QSFP-DD module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the QSFP-DD module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or the relevant standard, whichever is less.

Output squelch for loss of optical input signal, hereafter RX Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, then the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output as shown in Section 5.10.4. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp.

In normal operation the default case has RX Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface.

4.1.4.2 Tx(n)(p/n)

Tx(n)(p/n) are QSFP-DD module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP-DD optical module. The AC coupling is implemented inside the QSFP-DD optical module and not required on the Host board.

Output squelch for loss of electrical signal, hereafter Tx Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 70 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel, the loss of any of the incoming electrical input channels causes the optical output channel to be squelched.

For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch is an optional function. If TX squelch is implemented, the disable squelch must be provided.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000061

4.2 Power Requirements

The power supply has six designated pins, VccTx, VccTx1, Vcc1, Vcc2, VccRx, VccRx1 in the connector. Vcc1 and Vcc2 are used to supplement VccTx, VccTx1, VccRx or VccRx1 at the discretion of the module vendor. Power is applied concurrently to these pins.

A host board together with the QSFP-DD module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All power supply requirements in Table 6 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

4.2.1 Power Classes and Maximum Power Consumption

There are two power modes; Low Power Mode and High Power Mode, and eight power classes, Class 1 - Class 8. Module power modes are defined in Table 6 and power classes are defined in Table 5.

Since a wide range of module power classes exist, to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to accommodate only low power consumption modules, it is recommended that the host implement the state machine defined in the QSFP-DD Management Interface Specification and identify the power class of the module before allowing the module to go into high power mode.

Table 5- Power Classes

Power Class	Max Power (W)
1	1.5
2	3.5
3	7.0
4	8.0
5	10
6	12
7	14
8	>14

In general, the higher power classification levels are associated with higher data rates and longer reaches. The system designer is responsible for ensuring that the maximum case temperature does not exceed the case temperature requirements.

4.2.2 Host Board Power Supply Filtering

The host board should use the power supply filtering equivalent to that shown in Figure 6.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000062

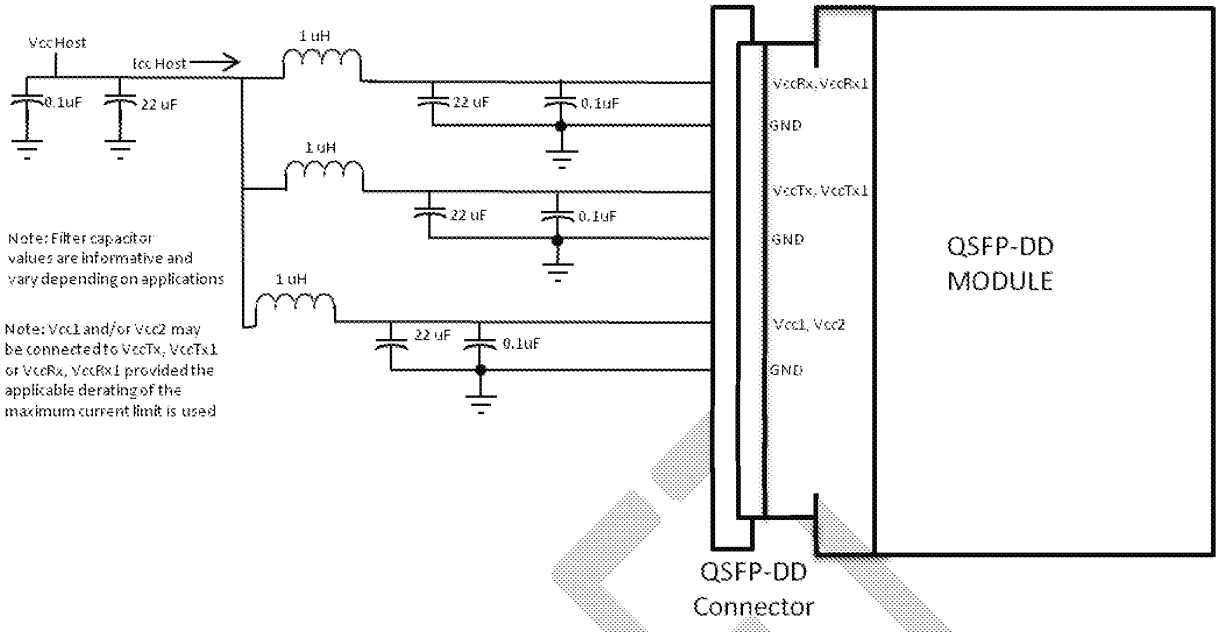


Figure 6: Recommended Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Card Edge Connector. It is recommended that the 22 uF capacitors each have an equivalent series resistance of 0.22 ohm.

The specifications for the power supply are shown in Table 6. The limits in Table 6 apply to the combined current that flows through all inductors in the power supply filter (represents ICC host in Figure 6). The test method for measuring inrush current can be found in SFF-8431. Keysight Technologies application brief 5991-2778EN provides useful guidance.

4.2.3 Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP-DD modules shall power up in Low Power Mode if InitMode is asserted. If InitMode is not asserted the module will proceed to High Power Mode without host intervention. Figure 7 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 6.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000063

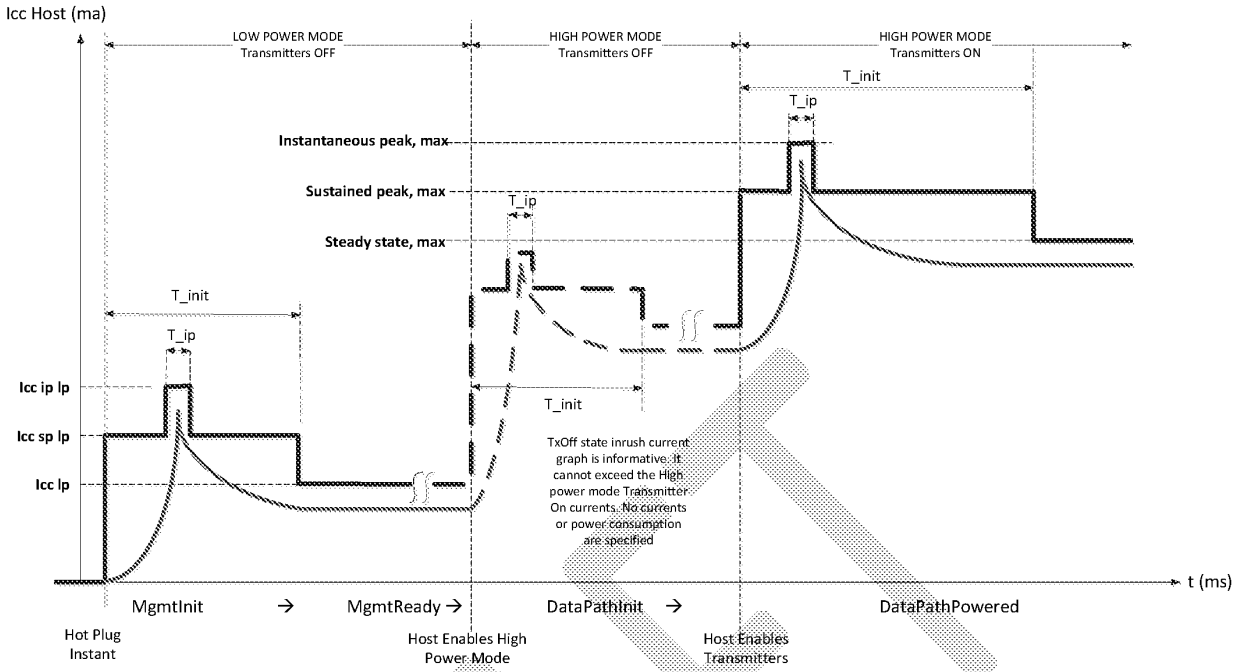


Figure 7: Instantaneous and sustained peak currents for Icc Host (see Fig. 6)

4.2.4 Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the value in Table 6 when tested by the methods of SFF-8431, section D.17.1 with the exception that 4.7uH iin SFF-8431 Figure 56 is replaced with 1 uH and the ESR of the .22uF capacitor (0.5 ohm) is replace with 0.22 ohm.

4.2.5 Module Power Supply Noise Output

The QSFP-DD module shall generate less than the value in Table 6 when tested by the methods of SFF-8431, section D.17.2. Note: The series resistor specified in D.17 Figure 56 may need to be reduced for high power modules.

4.2.6 Module Power Supply Noise Tolerance

The QSFP-DD module shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 6, swept from 10 Hz to 10 MHz according to the methods of SFF-8431, section D.17.3. This emulates the worst case noise output of the host.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000064

Table 6- Power Supply specifications, Instantaneous, sustained and steady state current limits

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccTx1, VccRx, VccRx1, Vcc1 & Vcc2 including ripple, droop and noise below 100kHz[1]		3.135	3.3	3.465	V
Host RMS noise output 10 Hz-10 MHz				25	mV
Module RMS noise output 10 Hz - 10 MHz				15	mV
Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak)	$PSNR_{mod}$			66	mV
Module inrush - instantaneous peak duration[2]	T_ip			50	µs
Module inrush - initialization time[2]	T_init			500	ms
Low Power Mode					
Power Consumption	P_lp			1.5	W
Instantaneous peak current at hot plug	Icc_ip_lp	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_lp	-	-	495	mA
Steady state current	Icc_lp	See Note 3			mA
High Power Mode Power Class 1 module					
Power Consumption	P_1			1.5	W
Instantaneous peak current	Icc_ip_1	-	-	600	mA
Sustained peak current	Icc_sp_1	-	-	495	mA
Steady state current	Icc_1	See Note 3			mA
High Power Mode Power Class 2 module					
Power Consumption	P_2			3.5	W
Instantaneous peak current	Icc_ip_2	-	-	1400	mA
Sustained peak current	Icc_sp_2	-	-	1155	mA
Steady state current	Icc_2	See Note 3			mA
High Power Mode Power Class 3 module					
Power Consumption	P_3			7	W
Instantaneous peak current	Icc_ip_3	-	-	2800	mA
Sustained peak current	Icc_sp_3	-	-	2310	mA
Steady state current	Icc_3	See Note 3			mA
High Power Mode Power Class 4 module					
Power Consumption	P_4			8	W
Instantaneous peak current	Icc_ip_4	-	-	3200	mA
Sustained peak current	Icc_sp_4	-	-	2640	mA
Steady state current	Icc_4	See Note 3			mA
High Power Mode Power Class 5 module					
Power Consumption	P_5			10	W
Instantaneous peak current	Icc_ip_5	-	-	4000	mA
Sustained peak current	Icc_sp_5	-	-	3300	mA
Steady state current	Icc_5	See Note 3			mA
High Power Mode Power Class 6 module					
Power Consumption	P_6			12	W
Instantaneous peak current	Icc_ip_6	-	-	4800	mA
Sustained peak current	Icc_sp_6	-	-	3960	mA
Steady state current	Icc_6	See Note 3			mA
High Power Mode Power Class 7 module					
Power Consumption	P_7			14	W
Instantaneous peak current	Icc_ip_7	-	-	5600	mA
Sustained peak current	Icc_sp_7	-	-	4620	mA
Steady state current	Icc_7	See Note 3			mA
High Power Mode Power Class 8 module					
Power Consumption	P_8[4]			>14	W
Instantaneous peak current	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current	Icc_sp_8	-	-	P_8/3.03	A
Steady state current	Icc_8	-	-	6	A

Note 1: Measured at VccTx, VccTx1, VccRx, VccRx1, Vcc1 and Vcc2
Note 2: T_ip and T_init are test conditions for measuring inrush current and not characteristics of the module
Note 3: The module must stay within its declared power class.
Note 4: User must read management register for maximum power consumption

Marvell Semiconductor, Inc. - Ex. 1002, Page 000065

4.3 ESD

Where ESD performance is not otherwise specified, e.g. in the InfiniBand specification, the QSFP-DD module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case. All the QSFP-DD module and host pins including high speed signal pins shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001.

4.4 Clocking Considerations

4.4.1 Data Path Description

Within a module, host electrical and module media lanes are grouped together into a logical concept called a data path. A data path is intended to represent a group of lanes that will be powered up or down and initialized together. Some examples include a 100GAUI-4 to 100GBASE-SR4 module implementation, where the data path would include four host electrical lanes and four module media lanes, or a 400GAUI-8 to 400GBASE-DR4 module implementation, where the data path would include eight host electrical lanes and four module media lanes.

4.4.2 Tx Clocking Considerations

Within a given Tx data path the host is responsible for ensuring that all electrical lanes delivered to the module are frequency synchronous (sourced from the same clock domain). If a module supports multiple Tx data paths running concurrently, the different Tx data paths can either all be in a single clock domain or separate clock domains. The module advertises which of these two modes it supports via the management registers.

If the module supports multiple Tx data paths running concurrently in a single clock domain, the module shall ensure that active Tx data paths continue to operate undisturbed even as other Tx data paths (and their associated Tx input lanes) are enabled/disabled by the host.

4.4.3 Rx Clocking Considerations

Within a given Rx data path all lanes received on the module media interface are required to be frequency synchronous (sourced from the same clock domain). If a module supports multiple Rx data paths running concurrently, the module shall allow the different Rx data paths to be asynchronous from each other (sourced from separate clock domains).

Marvell Semiconductor, Inc. - Ex. 1002, Page 000066

5 Mechanical and Board Definition

5.1 Introduction

The cages and modules defined in this section are illustrated in Figure 8 (2x1 stacked cage), Figure 9 (surface mount cage}, Figure 10 (Type 1 pluggable module) and Figure 11 (Type 2 pluggable module). All Pluggable modules and direct attach cable plugs (both Type 1 and Type 2) must mate to the connectors and cages defined in this specification. The Type 2 module allows an additional extension of the module outside of the cage to allow for flexibility in module design. Heat sink/clip thermal designs are application specific and not specifically defined by this specification. See Appendix A for informative recommendations on overall module length including handle.

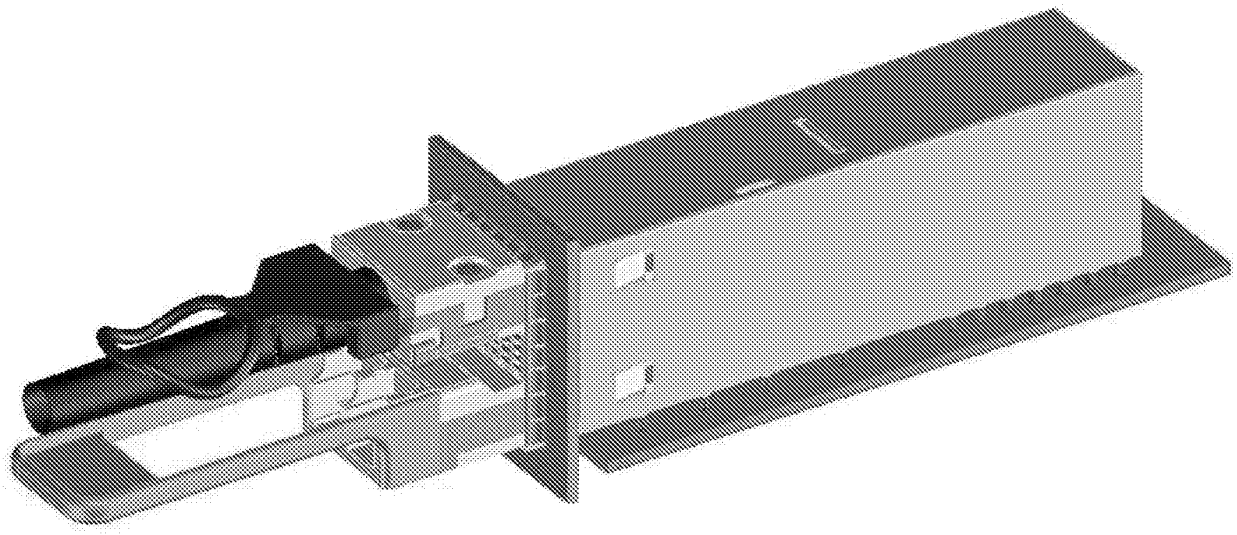


Figure 8: 2x1 stacked cage and module

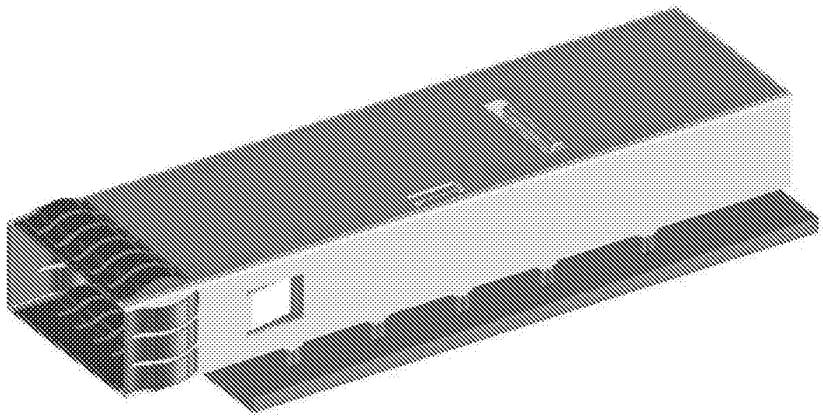


Figure 9: Press fit cage for surface mount (SMT) connector

Marvell Semiconductor, Inc. - Ex. 1002, Page 000067

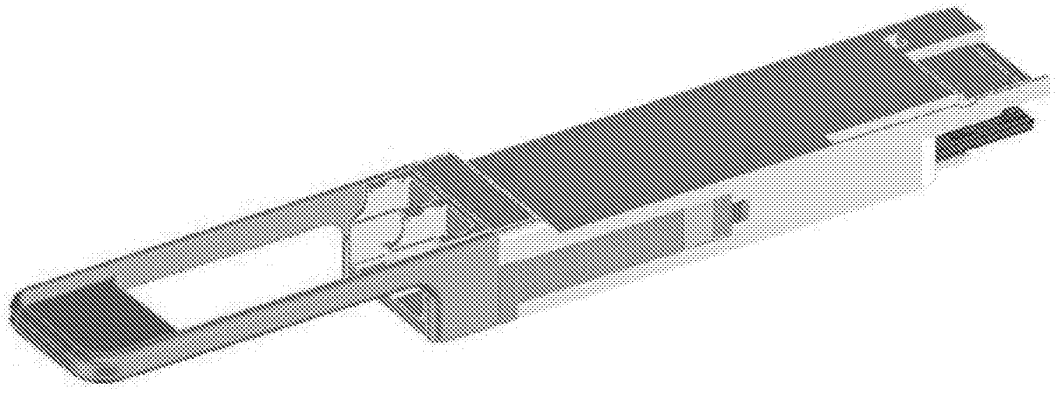


Figure 10: Type 1 Pluggable module

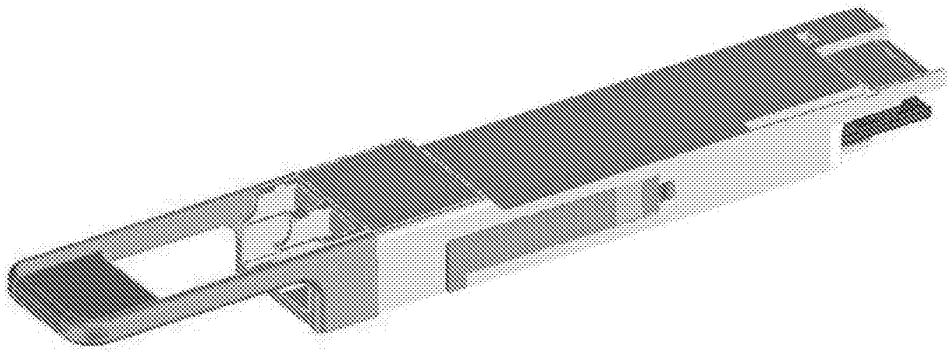


Figure 11: Type 2 Pluggable module

5.2 Datums, Dimensions and Component Alignment

A listing of the datums for the various components is contained in Table 7. The alignments of some of the datums are noted. In order to reduce the complexity of the drawings, all dimensions are considered centered unless otherwise specified. Dimensions and tolerancing conform to ASME Y14.5-2009. All dimensions are in millimeters.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000068

Table 7- Datums

Datum	Description
A	Host Board Top Surface
B	Inside surface of bezel
C	**Distance between Connector terminal thru holes on host board
D	*Hard stop on module
E	**Width of module
F	Height of module housing
G	**Width of module pc board
H	Leading edge of signal contact pads on module pc board
J	Top surface of module pc board
K	*Host board thru hole #1 to accept connector guide post
L	*Host board thru hole #2 to accept connector guide post
M	**Width of bezel cut out
P	Vertical Center line of internal surface of cage
S	Seating plane of cage on host board
T	*Hard stop on cage
AA	**Connector slot width
BB	Seating plane of connector on host board
DD	Top surface of module housing
EE	Centerline of module opening to locate paddle card Datum H
FF	Centerline of upper port cage height
GG	Centerline of lower port cage height
EE	Primary Datum hole for 2x1 Host PCB
*Datums D and T are aligned when assembled (see Figure 12 and Figure 13) **Centerlines of datums AA, C, E, G, M are aligned on the same vertical plane	

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000069

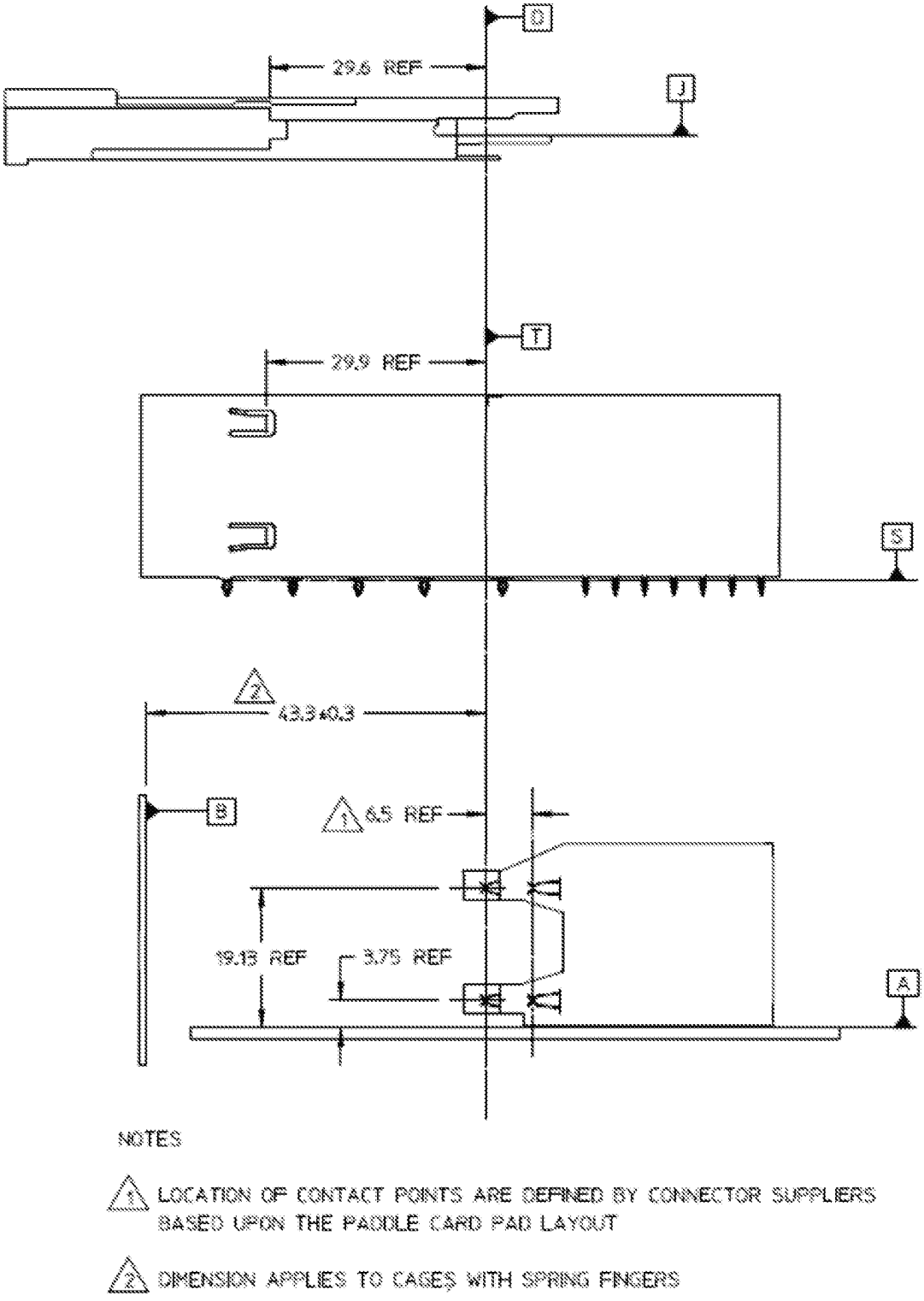


Figure 12: 2X1 stacked connector/cage datum descriptions

Marvell Semiconductor, Inc. - Ex. 1002, Page 000070

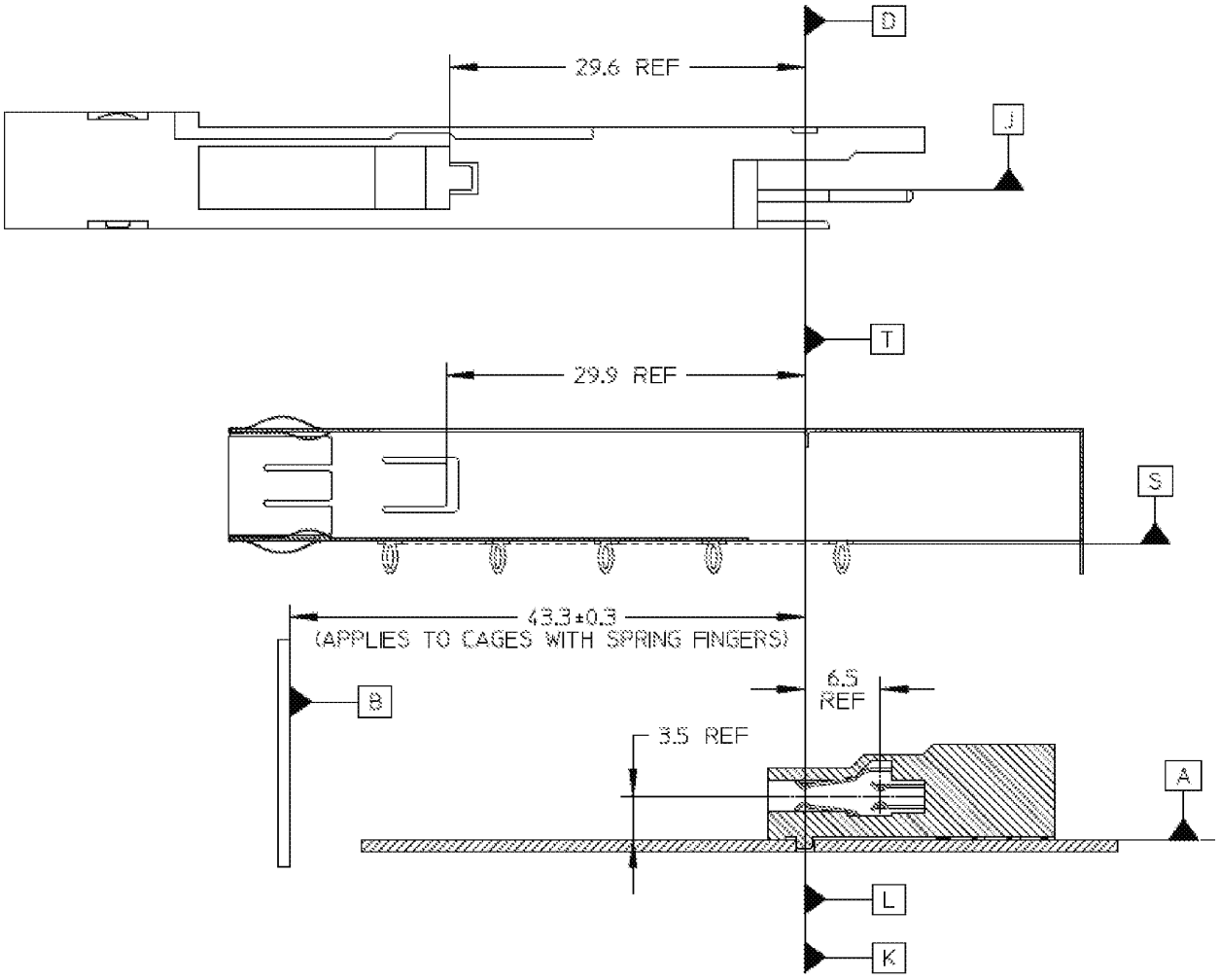


Figure 13: Surface mount connector/cage datum descriptions

5.3 Module Mechanical Dimensions

The mechanical outline for the Type 1 module is shown in Figure 14 and the Type 2 module is shown in Figure 15. The module shall provide a means to self-lock with either the 2x1 stacked cage or SMT cage upon insertion. The module package dimensions are defined in Figure 16 and Figure 17. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions per Note 4 in Figure 16. Note: All dimensions are in mm.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000071

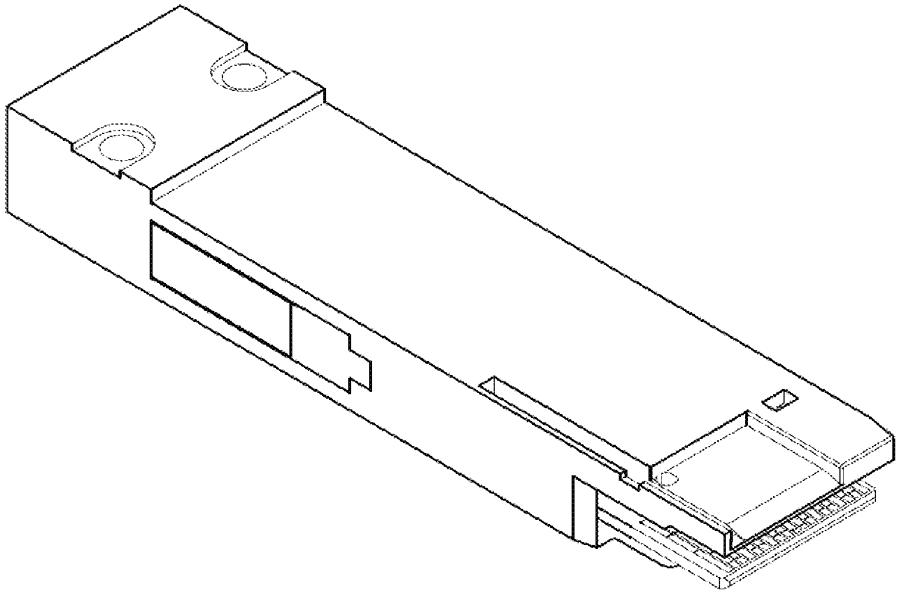


Figure 14: Type 1 Module

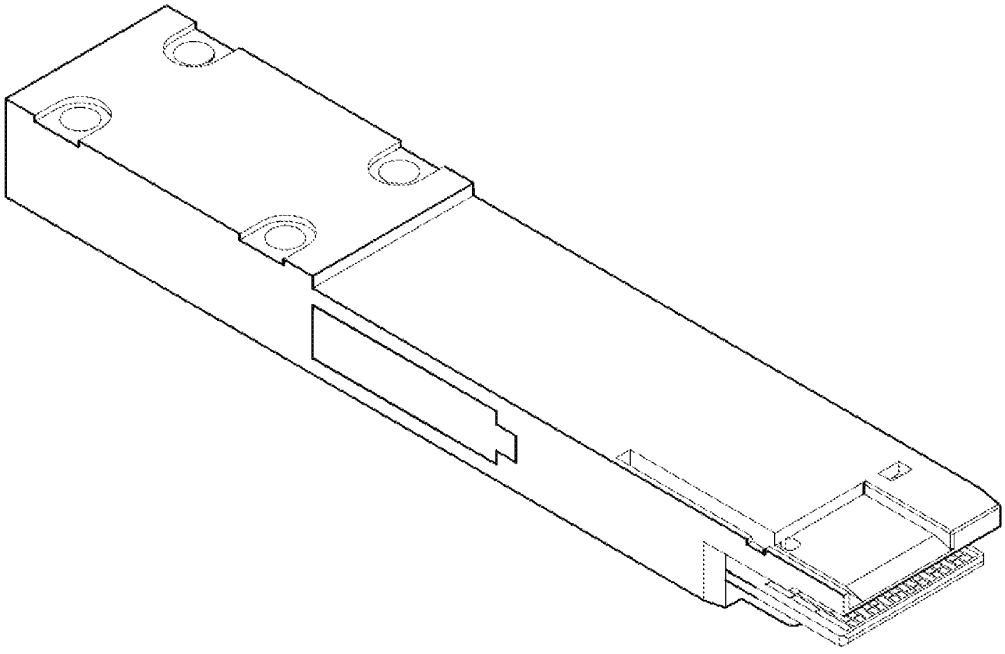


Figure 15: Type 2 Module

Marvell Semiconductor, Inc. - Ex. 1002, Page 000072

NOTES APPLY TO MODULE DRAWINGS :

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. UNLESS OTHERWISE SPECIFIED, SHARP CORNERS AND EDGES ARE NOT ALLOWED. ROUND OFF ALL EDGES AND CORNERS TO A MINIMUM RADUS OF 0.10 MM.

4 DIMENSION DEFINES ENLARGED SECTION OF TRANSCEIVER THAT EXTENDS OUTSIDE OF CAGE TO ACCOMMODATE MATING PLUG AND ACTUATOR MECHANISM.

5 SURFACES ON ALL 4 SIDES OF THE 12.4 MIN DIMENSION TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.

6 DIMENSION APPLIES TO LATCH MECHANISM.

7 DIMENSION APPLIES TO THE LOCATION OF THE EDGE OF THE MODULE BOARD PAD. DATUM H. CONTACTS 21, 22, 36 AND 37 ARE VISIBLE.

8 DIMENSION TO INCLUDE BAIL TRAVEL.

9 DIMENSIONS APPLY TO OPENINGS IN THE HOUSING.

10 OPTIONAL FEATURE TO AID INSPECTION OF DIMENSIONS FROM DATUM D.

11 FLATNESS AND SURFACE ROUGHNESS (Ra) APPLIES FOR INDICATED LENGTH AND MIN WIDTH OF 13 MM. SURFACE TO BE THERMALLY CONDUCTIVE. SEE SECTION 5.4 TABLE 8 FOR FLATNESS AND ROUGHNESS REQUIREMENTS.

12 HIGHER WATTAGE MODULES MAY REQUIRE ADDITIONAL SPACE FOR COOLING.

13 BLOCKING FEATURE IS CRITICAL TO APPLICATION FUNCTION. A RADIUS OF 0.1 ± 0.05 MM IS REQUIRED ON THE LEADING EDGES OF THIS FEATURE.

1

Marvell Semiconductor, Inc. - Ex. 1002, Page 000073

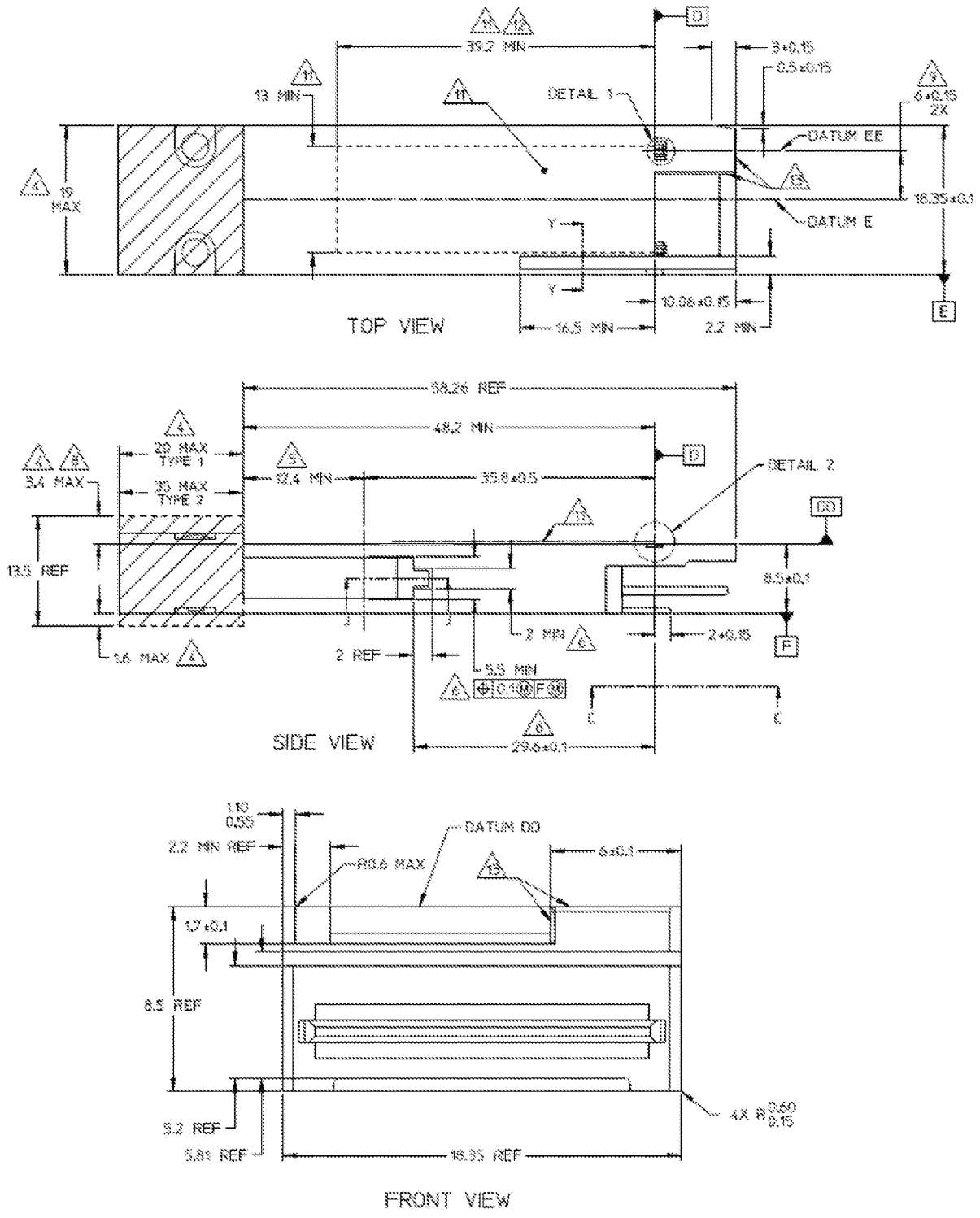
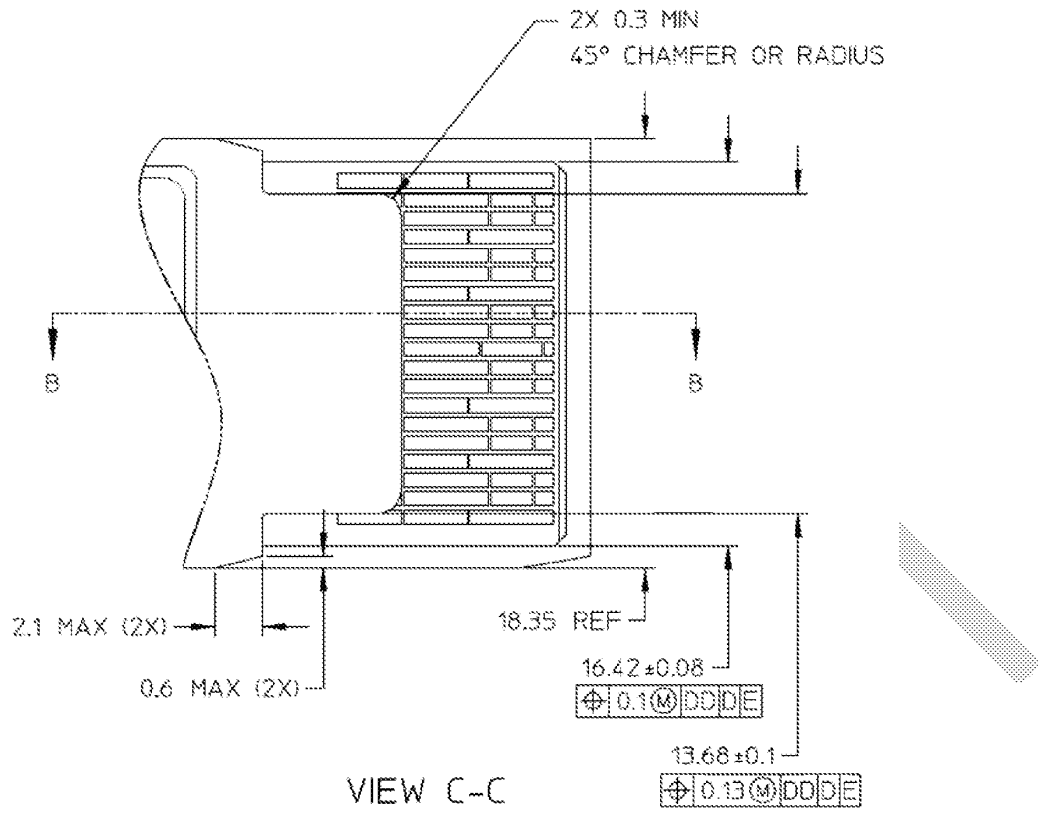
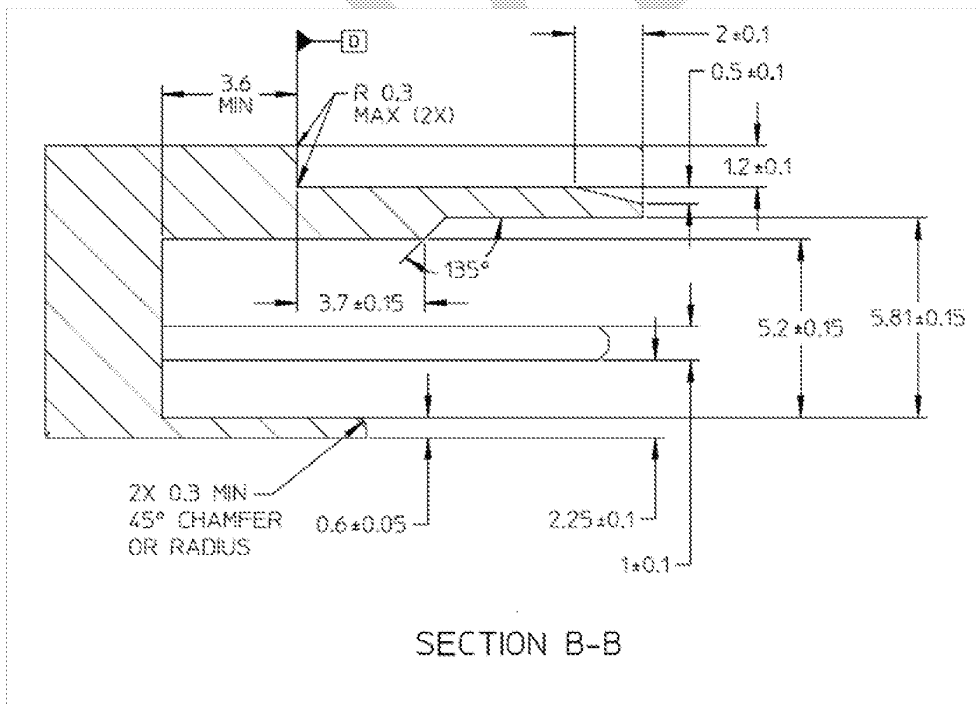


Figure 16: Drawing of module



VIEW C-C



SECTION B-B

Marvell Semiconductor, Inc. - Ex. 1002, Page 000075

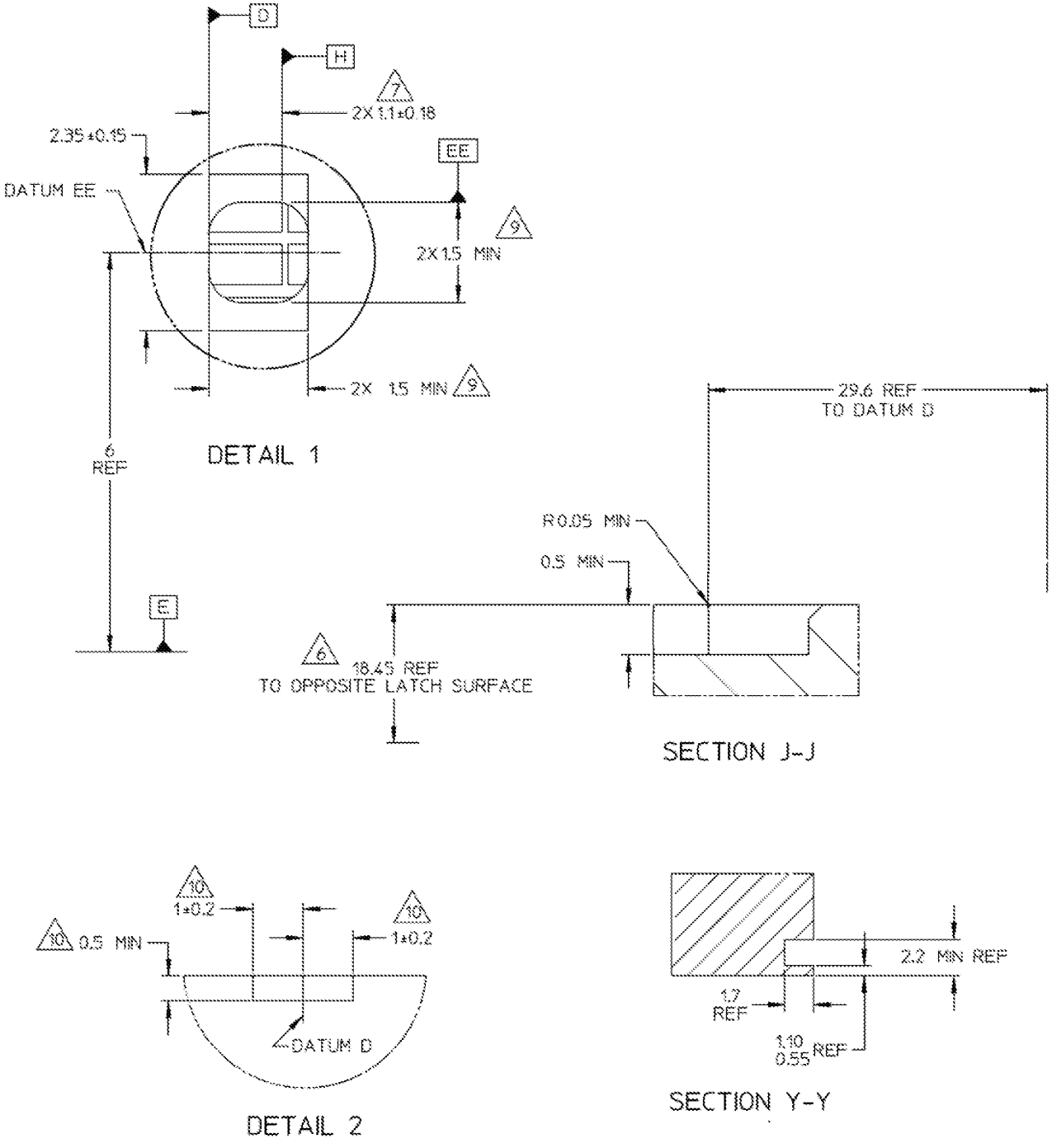


Figure 17: Detailed dimension of module

Marvell Semiconductor, Inc. - Ex. 1002, Page 000076

5.4 Module Flatness and Roughness

Module flatness and roughness are specified to improve module thermal characteristics when used with a riding heat sink. Relaxed specifications are used for lower power modules to reduce cost. The module flatness and roughness specifications apply to the specified heat sink contact area as specified in Figure 16. Specifications for Module flatness and surface roughness are shown in Table 8 (see Figure 16 note 11).

Table 8- Module flatness specifications

Power Class	Module Flatness (mm)	Surface Roughness (Ra,µm)
1	0.075	1.6
2	0.075	1.6
3	0.075	1.6
4	0.075	1.6
5	0.050	0.8
6	0.050	0.8
7	0.050	0.8
8	0.050	0.8

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000077

5.5 Module paddle card dimensions

Notes for Module Paddle Card Drawings (Figures 18 and 19):

1. Pre-wipe pads (shaded area) on module card host side are optional
2. A single split in the pre-wipe signal pad is optional, and if implemented, the resulting 2 pads shall be separated with a gap of 0.13 +/- 0.05
3. Dimensioning and tolerancing conform to ASME Y14.5-2009
4. All dimensions are in millimeters
5. No solder mask within 0.05 mm of all defined contact pad edges.
6. No solder mask between end contacts and the sides of the paddle card
7. Datum H is established with Datum Target points at the leading edge of the outer most signal contact pads to be re-established on each side
8. Dimension applies from the first set of signal pads to the second set of signal pads
9. Dimension applies from the first set of signal pads to the second set of signal pads
10. Dimension and tolerance applies to all power pads on both top and bottom side of paddle card
11. Dimension and tolerance applies to all power pads on both top and bottom side of paddle card
12. Dimension and tolerance applies to all power pads on both top and bottom side of paddle card
13. A zero gap is allowed for a continuous pad option
14. Applies to all signal pad to pad spacing
15. Pre-wipe pads (shaded area) are required except in continuous power or groundpad designs
16. Paddle card thickness is measured over pads vias must not be proud of the pad surface
17. Minimum dimension required for mating sequence between signal and ground pads
18. Component keep out area measured from Datum H
19. Contact pad plating

    0.38 micrometers minimum gold over

    1.27 micrometers minimum nickel

    Alternate contact pad plating

    0.05 micrometers minimum gold over

    0.30 micrometers minimum palladium over

    1.27 micrometers minimum nickel

Marvell Semiconductor, Inc. - Ex. 1002, Page 000078

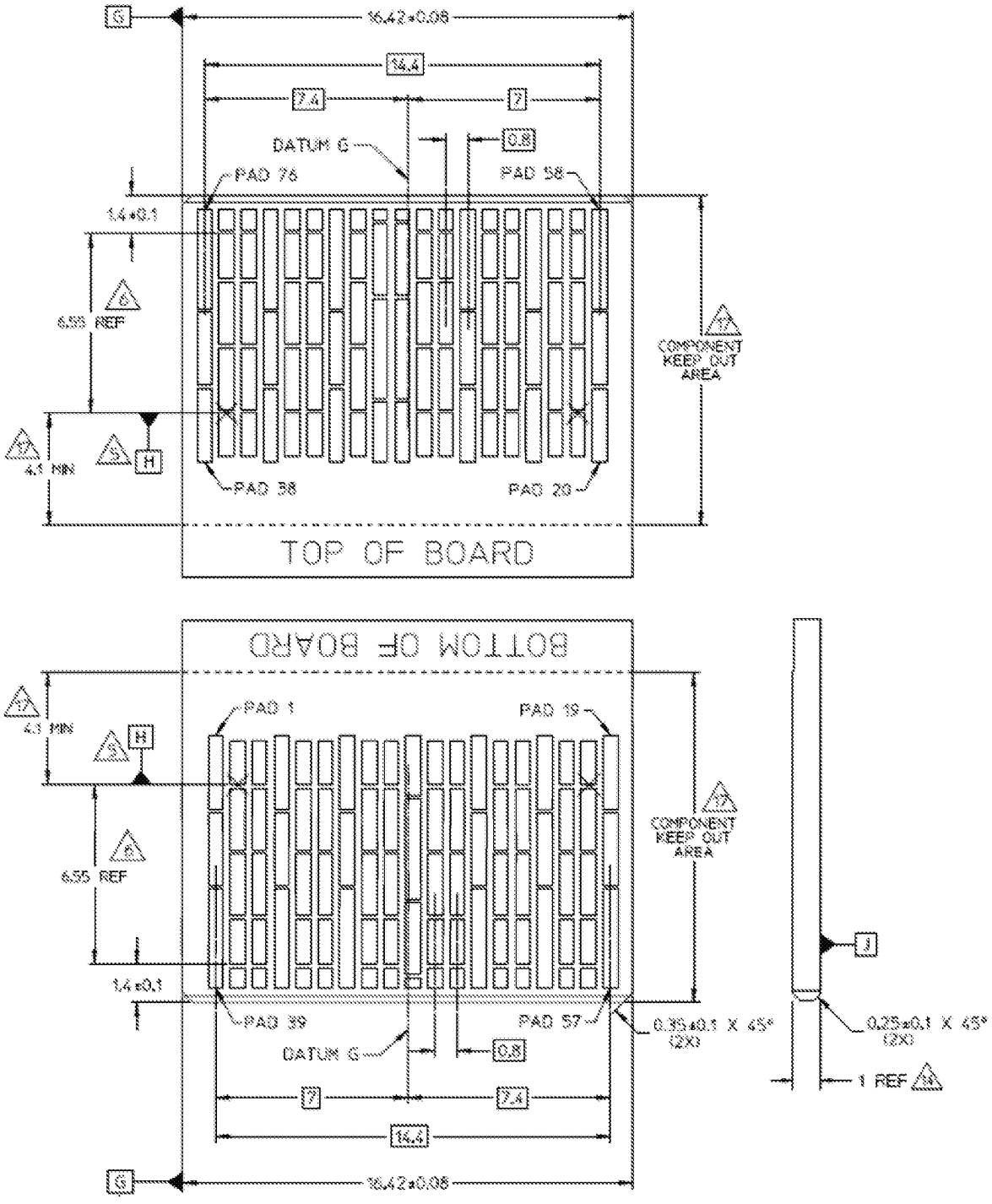


Figure 18: Module paddle card dimensions

Marvell Semiconductor, Inc. - Ex. 1002, Page 000079

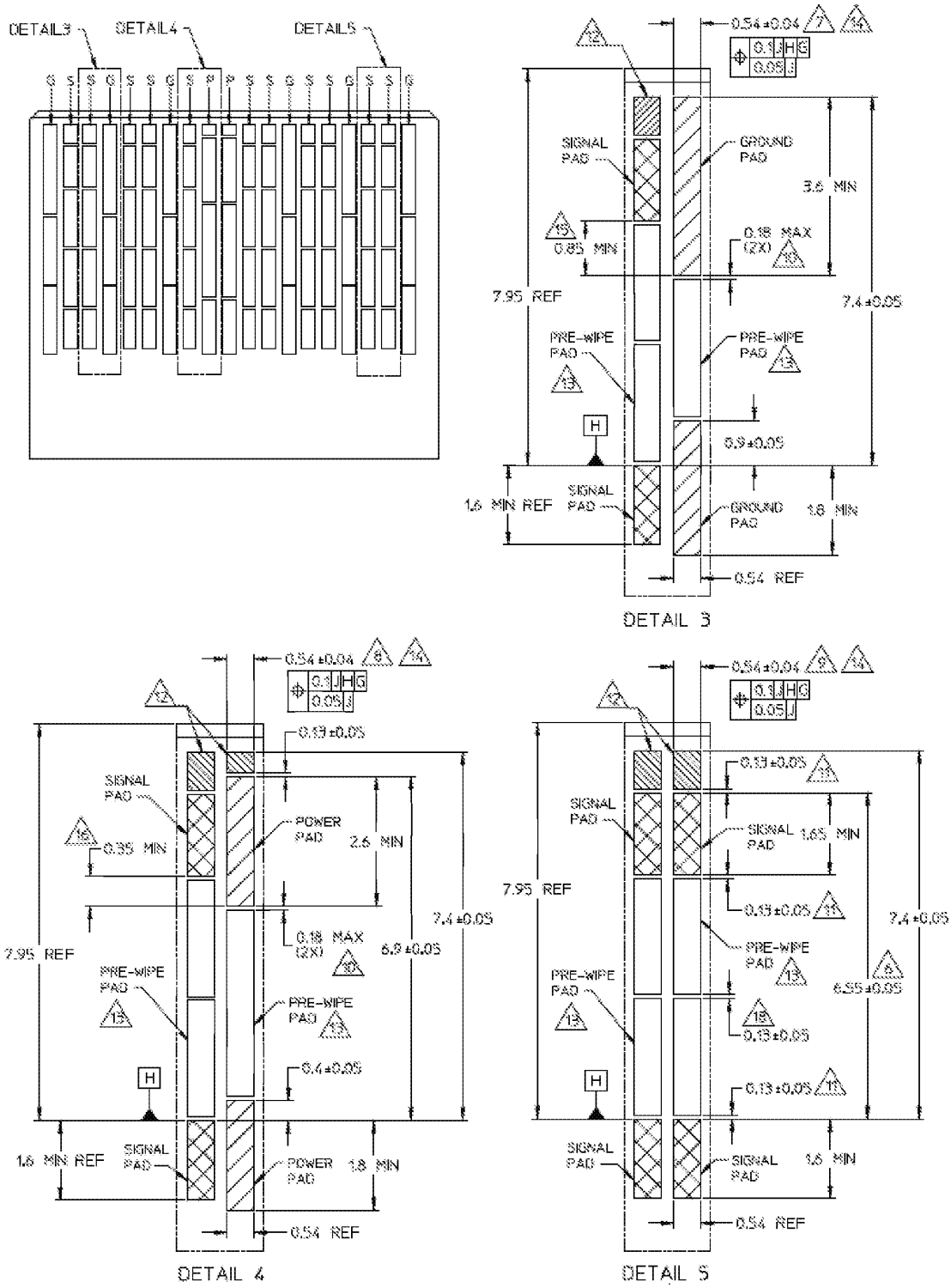


Figure 19: Module pad dimensions

Marvell Semiconductor, Inc. - Ex. 1002, Page 000080

5.6 Module Extraction and Retention Forces

The requirements for insertion forces, extraction forces and retention forces are specified in Table 9. The QSFP-DD cage and module are designed to ensure that excessive force applied to a cable does not damage the QSFP-DD cage or host connector. If any part is damaged by excessive force, it should be the cable or media module and not the cage or host connector which is part of the host system. The contact pad plating shall meet the requirements of Section 5.5.

Table 9- Insertion, Extraction and Retention Forces

Measurement	Min	Max	Units	Comments
QSFP module insertion	0	40	N	
QSFP-DD module insertion	0	90	N	
QSFP module extraction	0	30	N	
QSFP-DD module extraction	0	50	N	
QSFP module retention	90	N/A	N	No damage to module below 90N with latch engaged
QSFP-DD module retention	90	N/A	N	No damage to module below 90N with latch engaged
Cage retention (Latch strength)	125	N/A	N	No damage to latch below 125N
Cage retention in Host Board	114	N/A	N	Force to be applied in a vertical direction, no damage to cage
Insertion/removal cycles, connector/ cage	100	N/A	Cycles	Number of cycles for the connector and cage with multiple modules.
Insertion/removal cycles, QSFP-DD module	50	N/A	Cycles	Number of cycles for an individual module.
Note: Insertion, extraction and retention forces apply with or without the presence of a riding heat sink.				

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000081

5.7 2x1 Electrical Connector Mechanical

The QSFP-DD Connector is a 76-contact, right angle connector. The integrated connector in a 2x1 stacked cage is shown in Figure 20 with detailed drawings in Figure 21, Figure 22 and Figure 23. Recommendations for the 2x1 stacked cage bezel opening are shown in Figure 24.

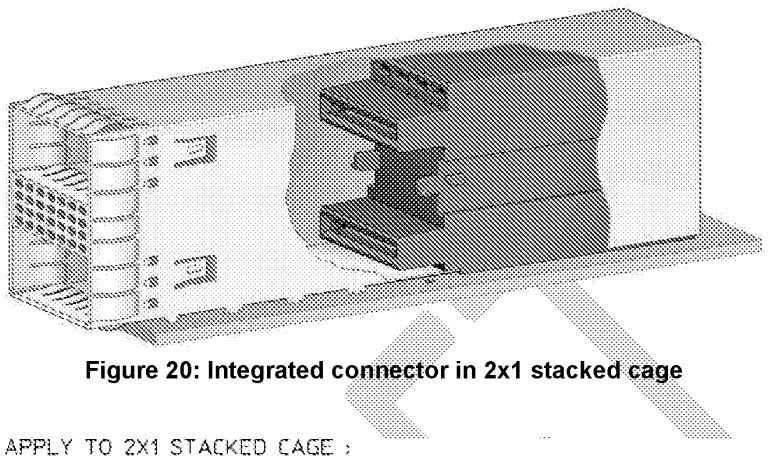


Figure 20: Integrated connector in 2x1 stacked cage

NOTES APPLY TO 2X1 STACKED CAGE :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS FROM INSIDE SURFACES OF SPRING FINGERS WHEN FULLY DEPRESSED
4. CONNECTOR REMOVED FOR DRAWING CLARITY.
5. APPLIES TO ALL SPRING FINGERS ON ALL SIDES.
6. EXTERNAL CAGE DIMENSIONS. DOES NOT INCLUDE FOLDING TABS.
7. LENGTH OF CAGE AND SIGNAL TAILS.
8. PRESS FIT CAGE PINS APPLY TO RIGHT SIDE OF CAGE.
9. PRESS FIT CAGE PINS APPLY TO LEFT SIDE TO CAGE.
10. PRESS FIT PIN OFFSET BETWEEN RIGHT AND LEFT SIDE OF CAGE.
11. DIMENSIONS INCLUDES BACKCOVER.
12. SIZE AND POSITION OF CAGE AND CONNECTOR PRESS FIT PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FOOTPRINT LAYOUT
13. CAVITY FOR HEAT SINK IS OPTIONAL
14. CONTACT PIN DIMENSION MEASURED FROM DATUM T
15. CONTACT PIN DIMENSION MEASURED FROM DATUM T1

Marvell Semiconductor, Inc. - Ex. 1002, Page 000082

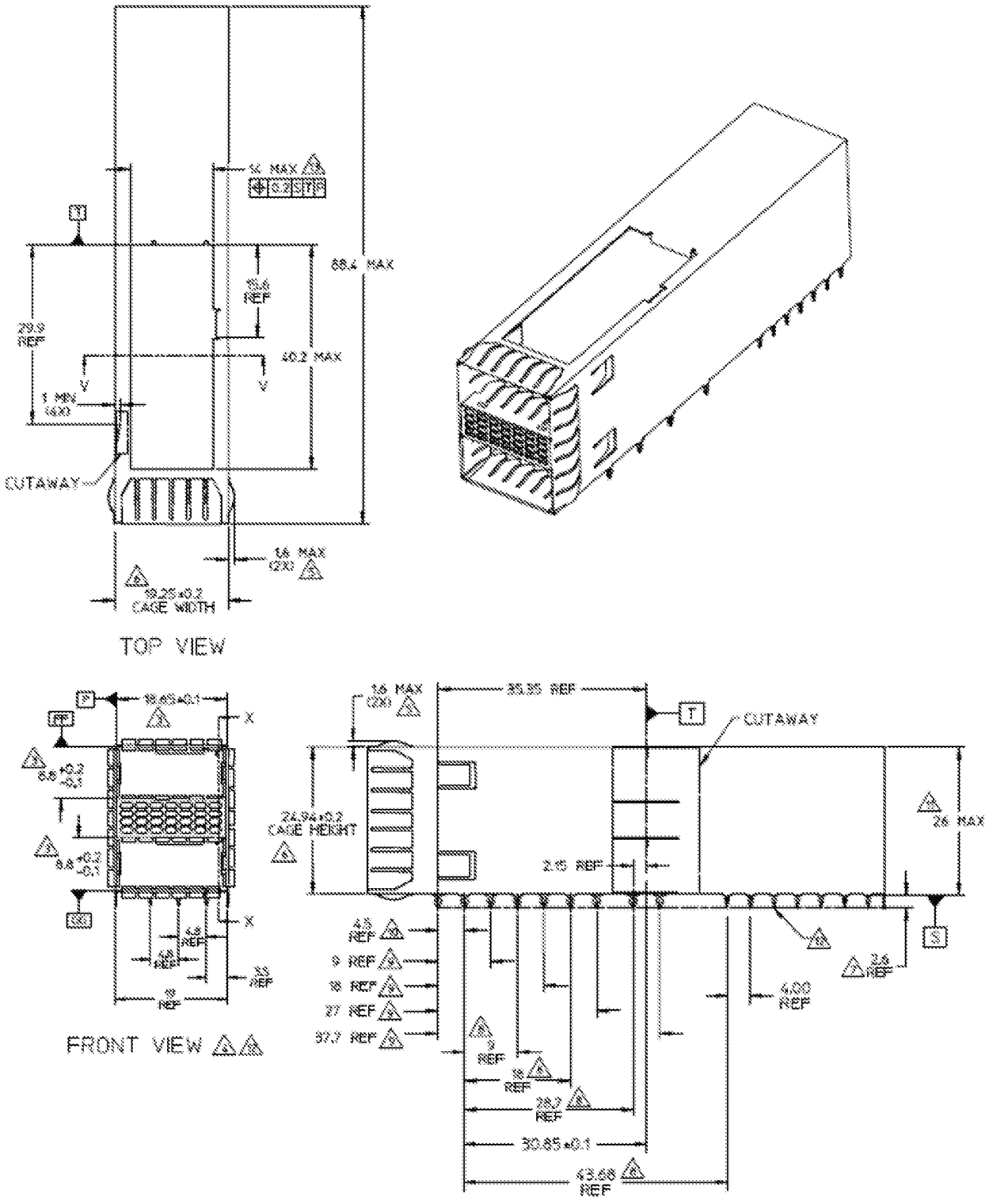


Figure 21: 2x1 stacked cage

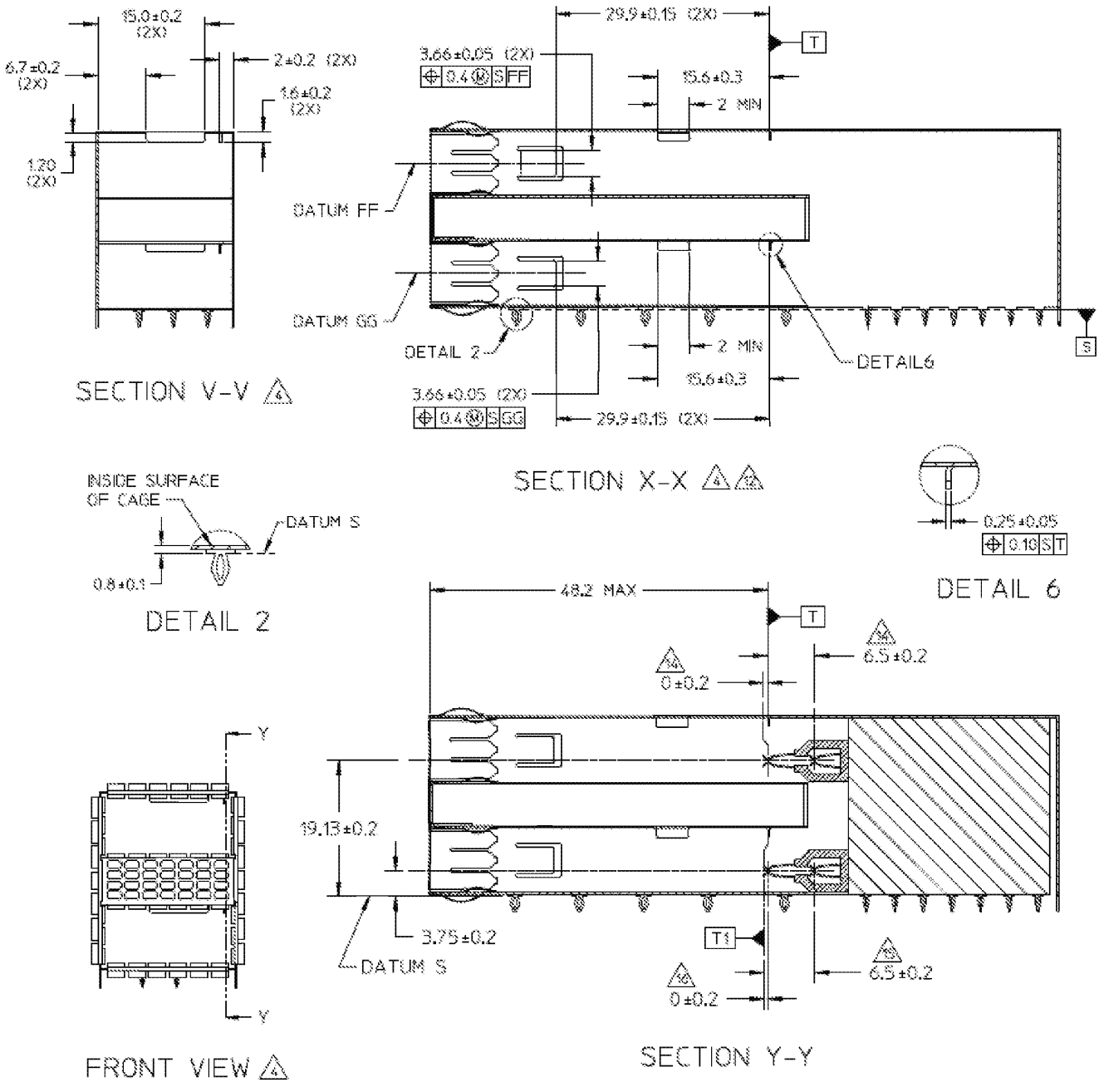


Figure 22: 2x1 stacked cage dimensions

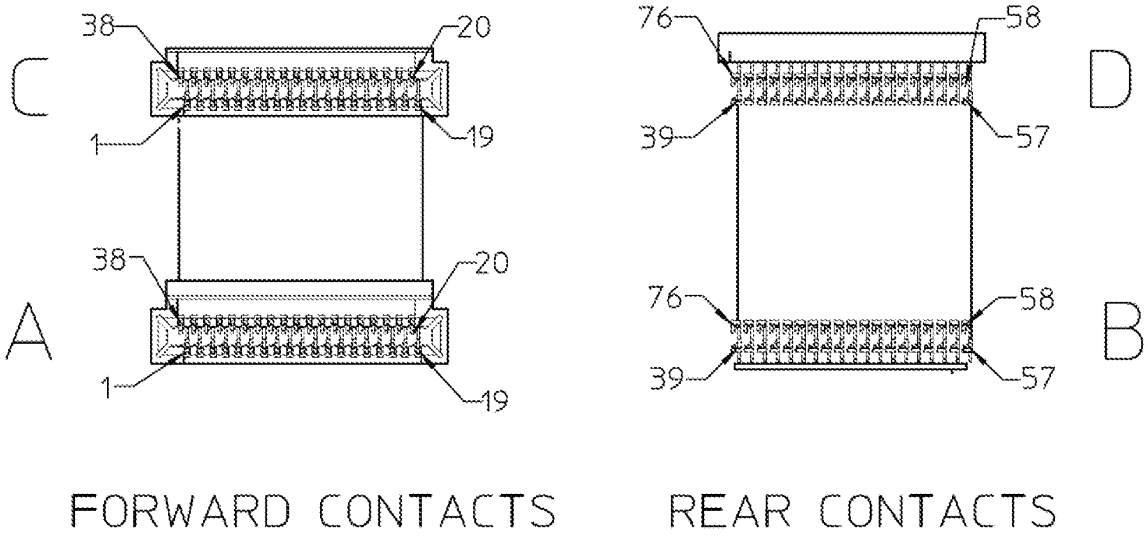


Figure 23: Connector pins in 2x1 stacked cage as viewed from the front

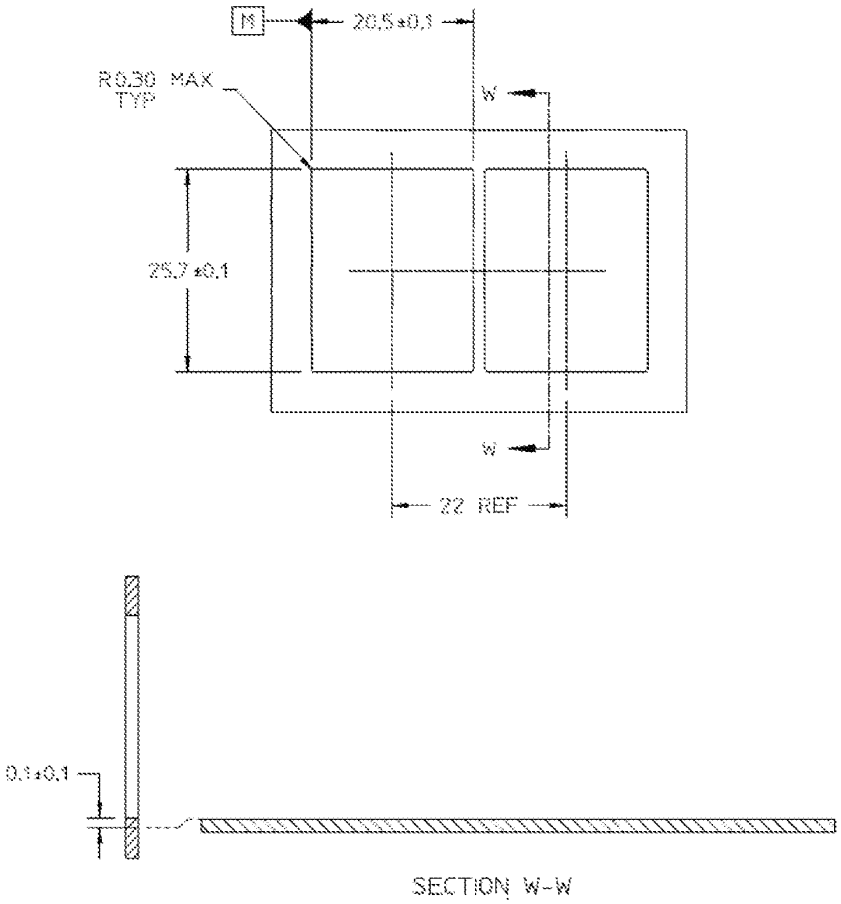


Figure 24: 2x1 Bezel Opening

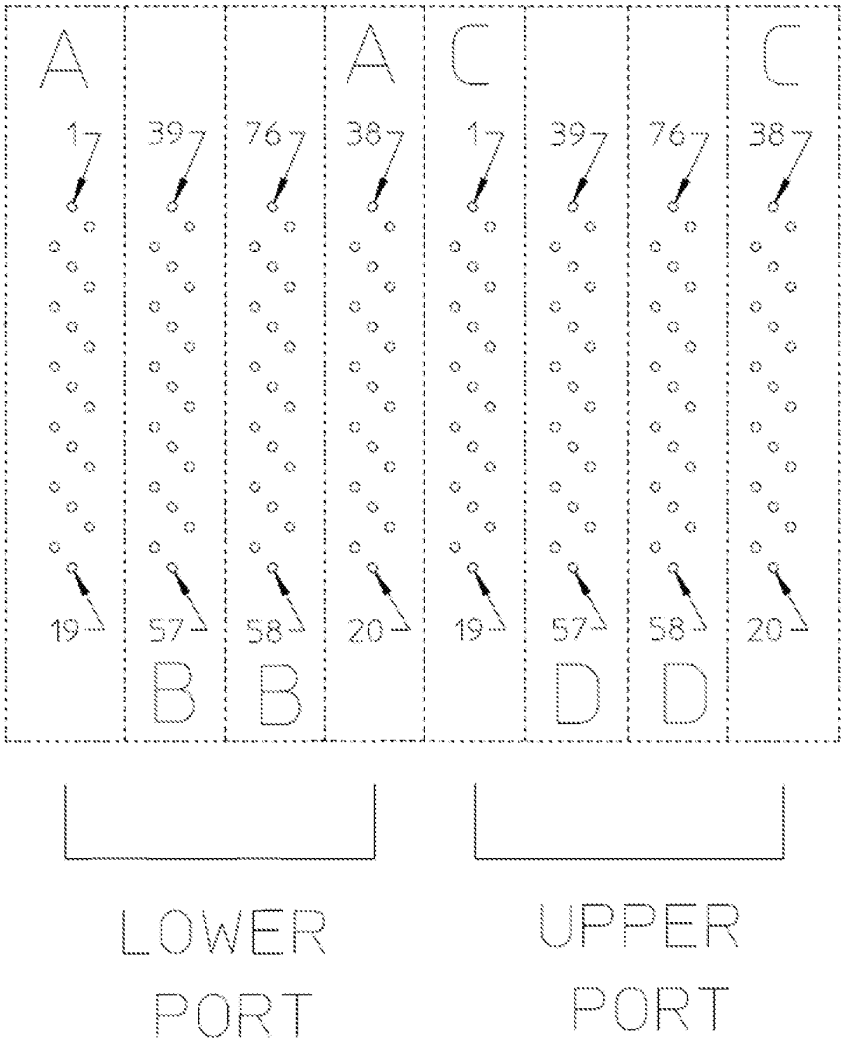


Figure 25: 2X1 host board connector contacts

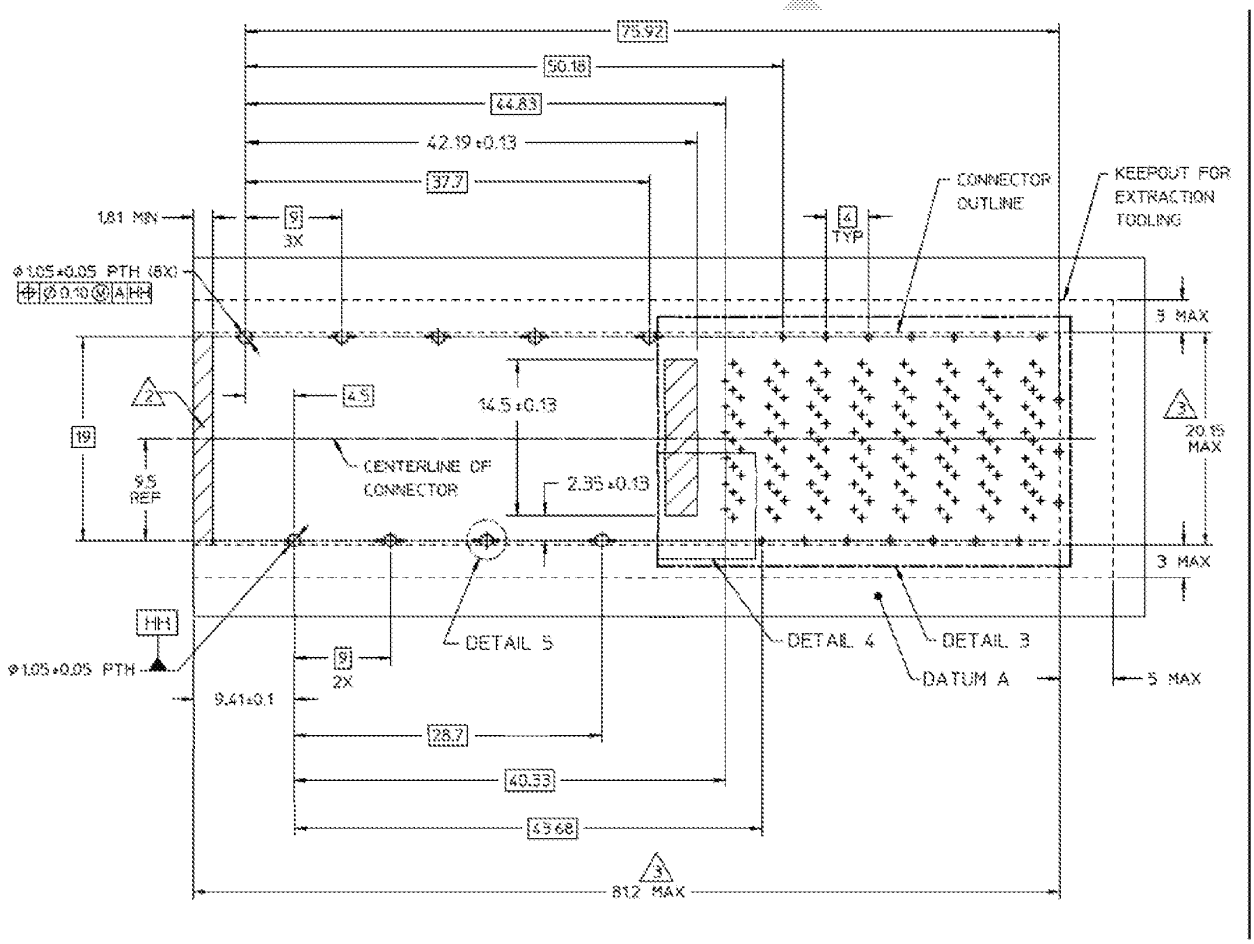
5.7.1 2x1 Connector and Cage host PCB layout

A typical host board mechanical layout for attaching the QSFP-DD 2x1 Connector and Cage system is shown in Figure 25 and Figure 26. Location of the pattern on the host board is application specific. To achieve 25-50 Gbps performance pad dimensions and associated tolerances must be adhered to and attention paid to the host board layout.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000086

Notes for Host PCB (Figure 26):

1. The entire area under the connector (outside dashed lines) is to be considered a keep out area for components
2. Hatched area represent zones on the PCB that come in contact with or are in close proximity to the plastic housing or the connector cage. Indicated areas to be considered trace free.
3. Dimension applies to connector outline



Marvell Semiconductor, Inc. - Ex. 1002, Page 000087

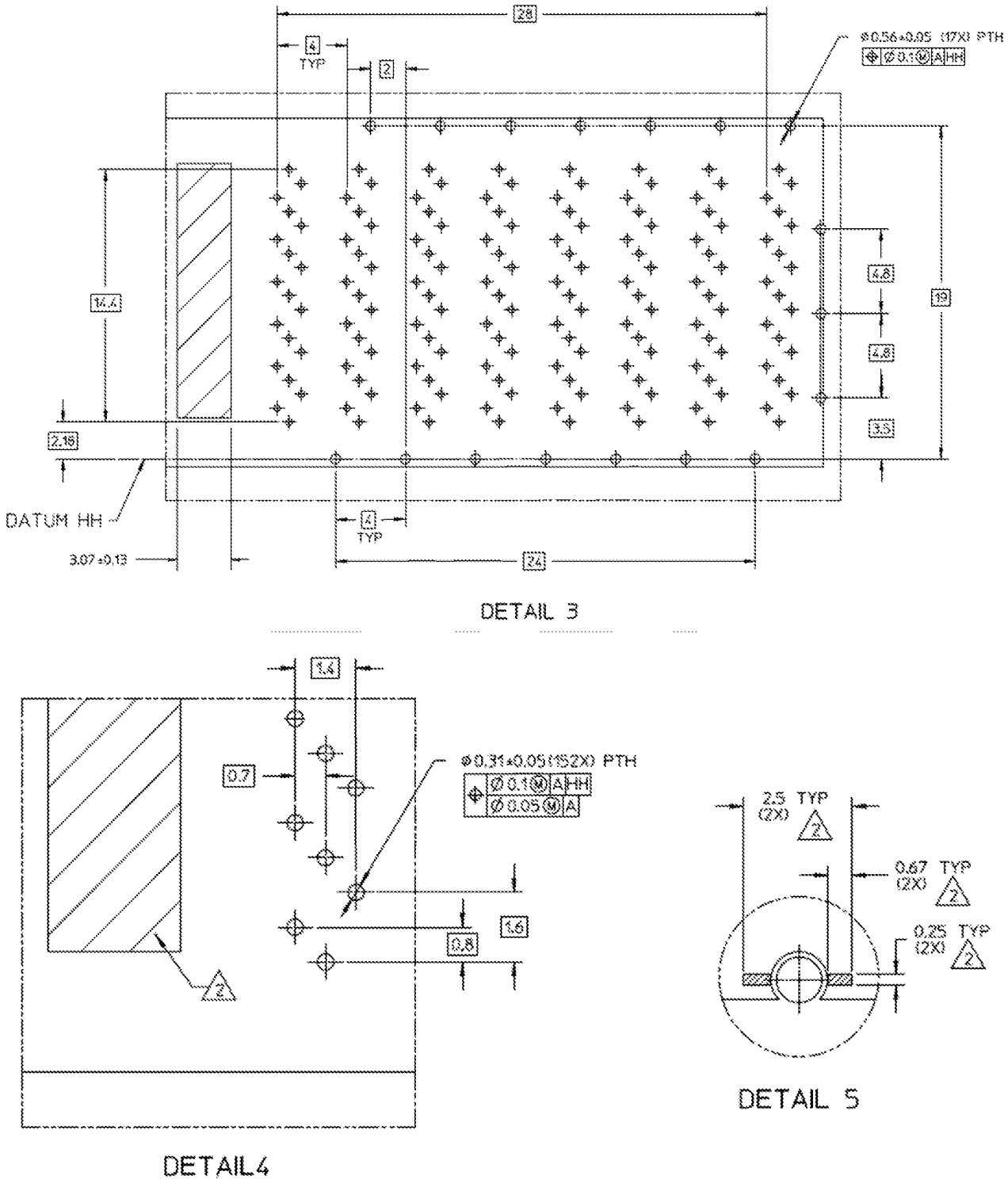


Figure 26: 2X1 Host PCB Mechanical Layout

5.8 Surface Mount Electrical Connector Mechanical

The QSFP-DD Connector is a 76-contact, right angle connector. The SMT connector in a 1xn cage is shown in Figure 27 with detailed drawings in Figure 28 and Figure 29. Recommendations for the SMT cage bezel opening are shown in Figure 30.

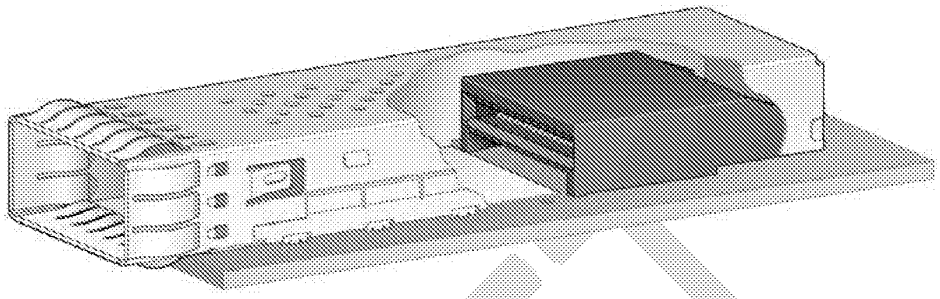


Figure 27: SMT connector in 1xn cage

NOTES APPLY TO SMT 1 X N CAGE DRAWINGS :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. DIMENSIONS FROM INSIDE SURFACES OF SPRING FINGERS WHEN FULLY DEPRESSED.

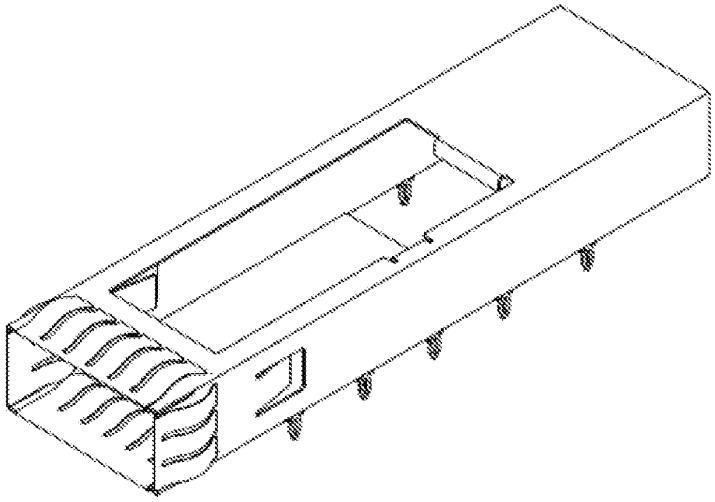
4. CAVITY FOR HEAT SINK IS OPTIONAL.

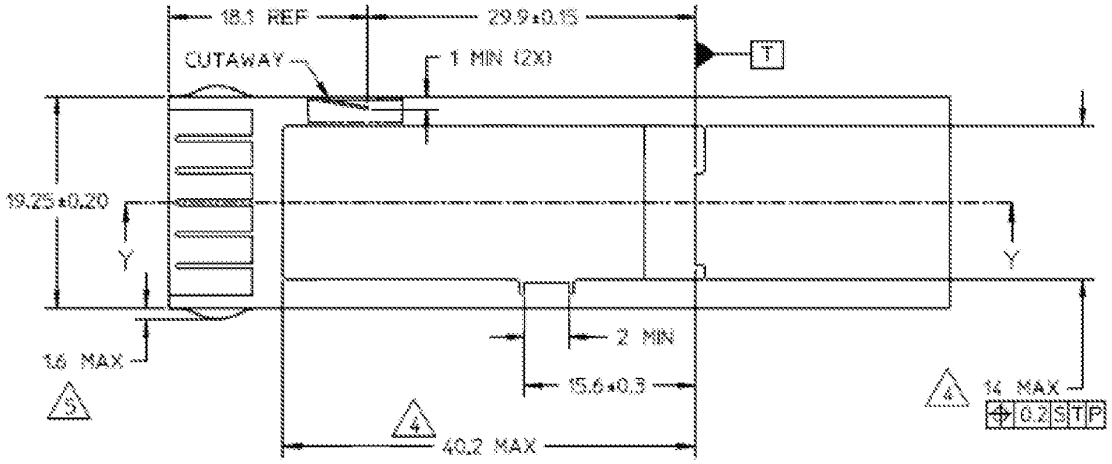
5. APPLIES TO ALL SPRING FINGERS ON ALL SIDES.

6. DATUM S IS DEFINED BY SEATING PLANE ON HOST BOARD.

7. SIZE OF CAGE PRESS FIT PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FOOTPRINT LAYOUT.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000089




18.1 REF
29.9±0.15
CUTAWAY
1 MIN (2X)
T
19.25±0.20
Y
Y
1.6 MAX
2 MIN
15.6±0.3
40.2 MAX
14 MAX
0.2 S T P

TOP VIEW

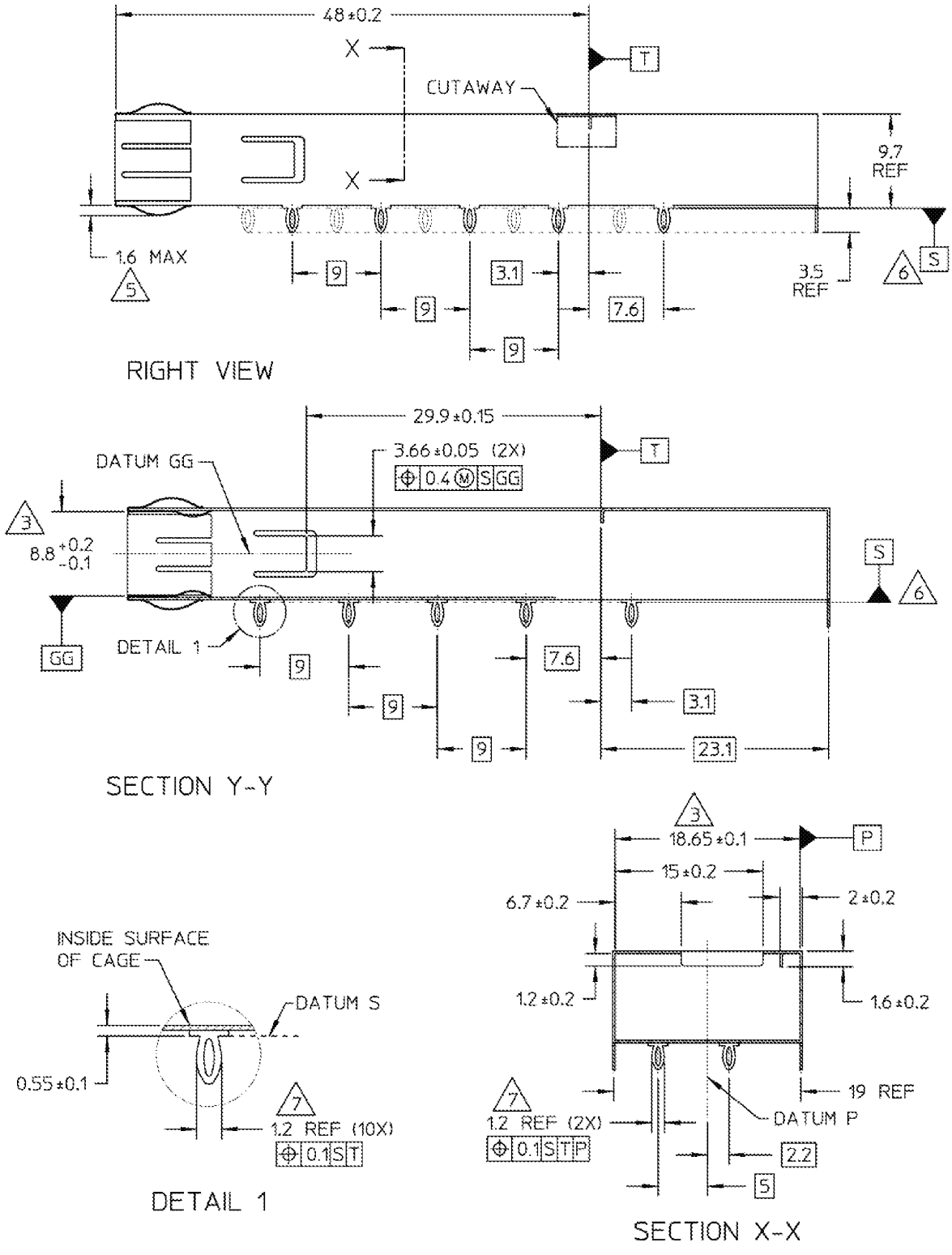
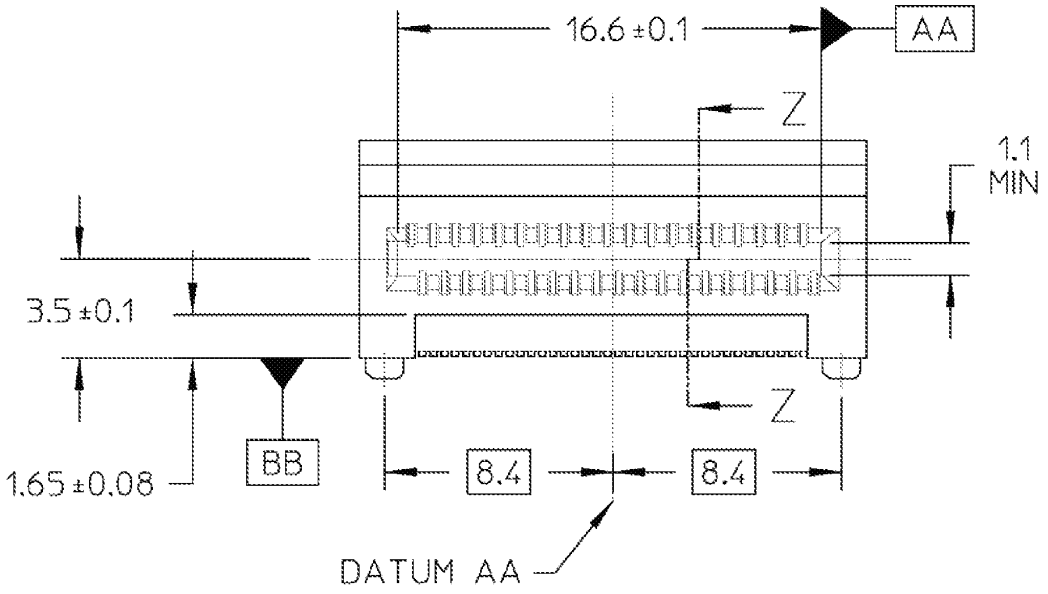
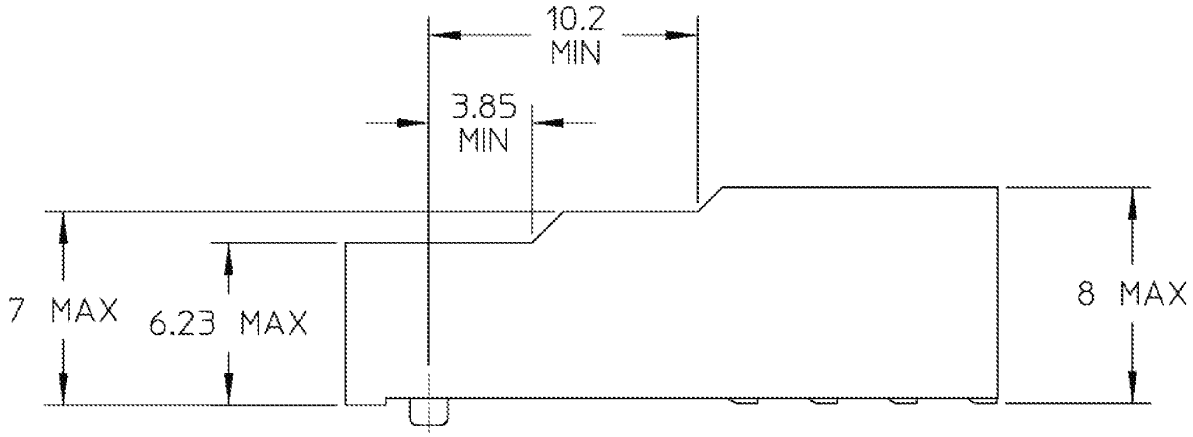


Figure 28: SMT 1x1 Cage Design

Marvell Semiconductor, Inc. - Ex. 1002, Page 000091



FRONT VIEW



SIDE VIEW

Marvell Semiconductor, Inc. - Ex. 1002, Page 000092

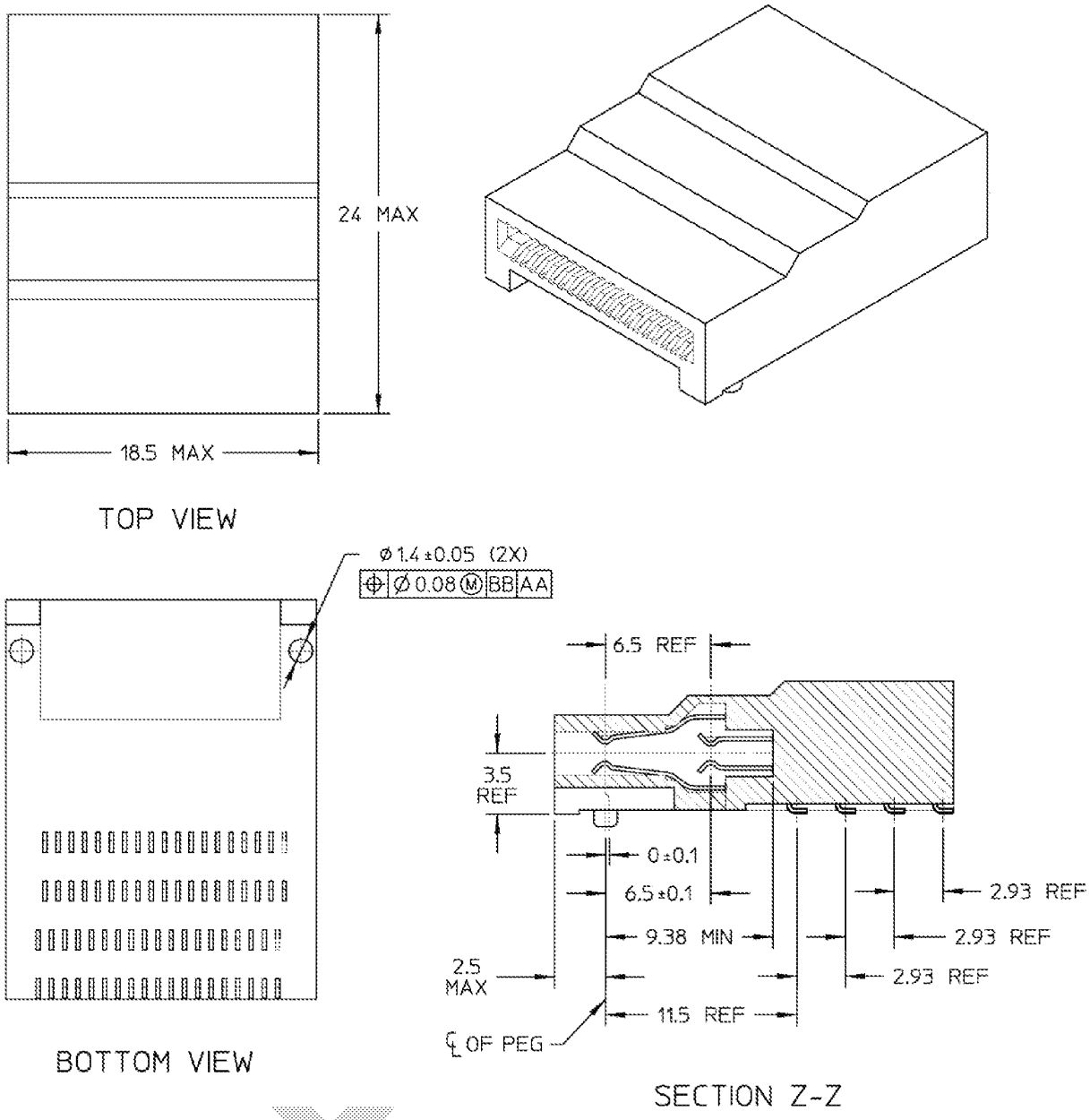


Figure 29: SMT 1x1 Connector Design

Note: Contact Pin Dimension Measured from Datum T

Marvell Semiconductor, Inc. - Ex. 1002, Page 000093

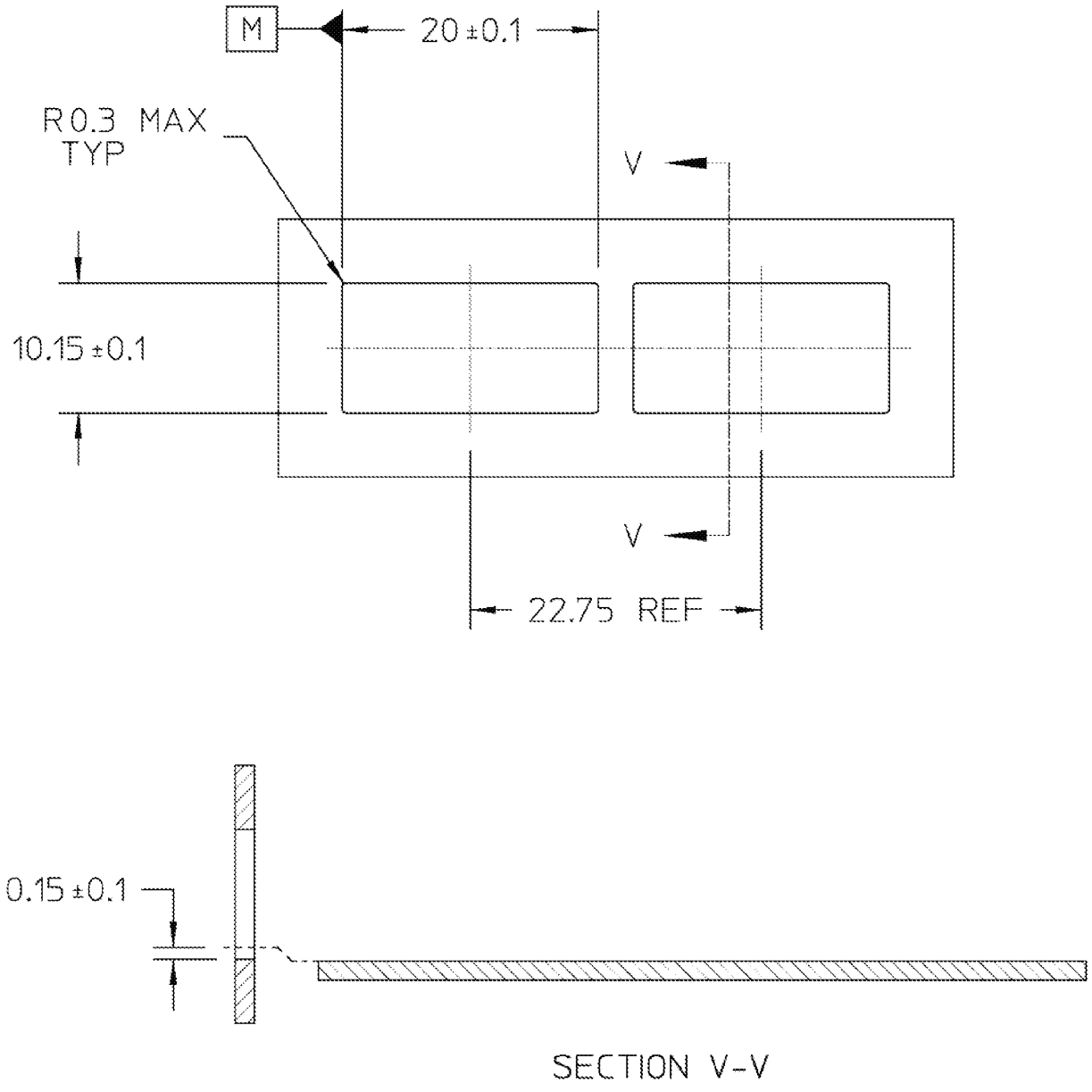


Figure 30: SMT 1x1 bezel opening

Marvell Semiconductor, Inc. - Ex. 1002, Page 000094

5.8.1 Surface mount connector and cage host PCB layout

A typical host board mechanical layout for attaching the QSFP-DD surface mount Connector and Cage System is shown in Figure 31 and Figure 32. Location of the pattern on the host board is application specific.

To achieve 25-50 Gbps performance pad dimensions and associated tolerances must be adhered to and attention paid to the host board layout.

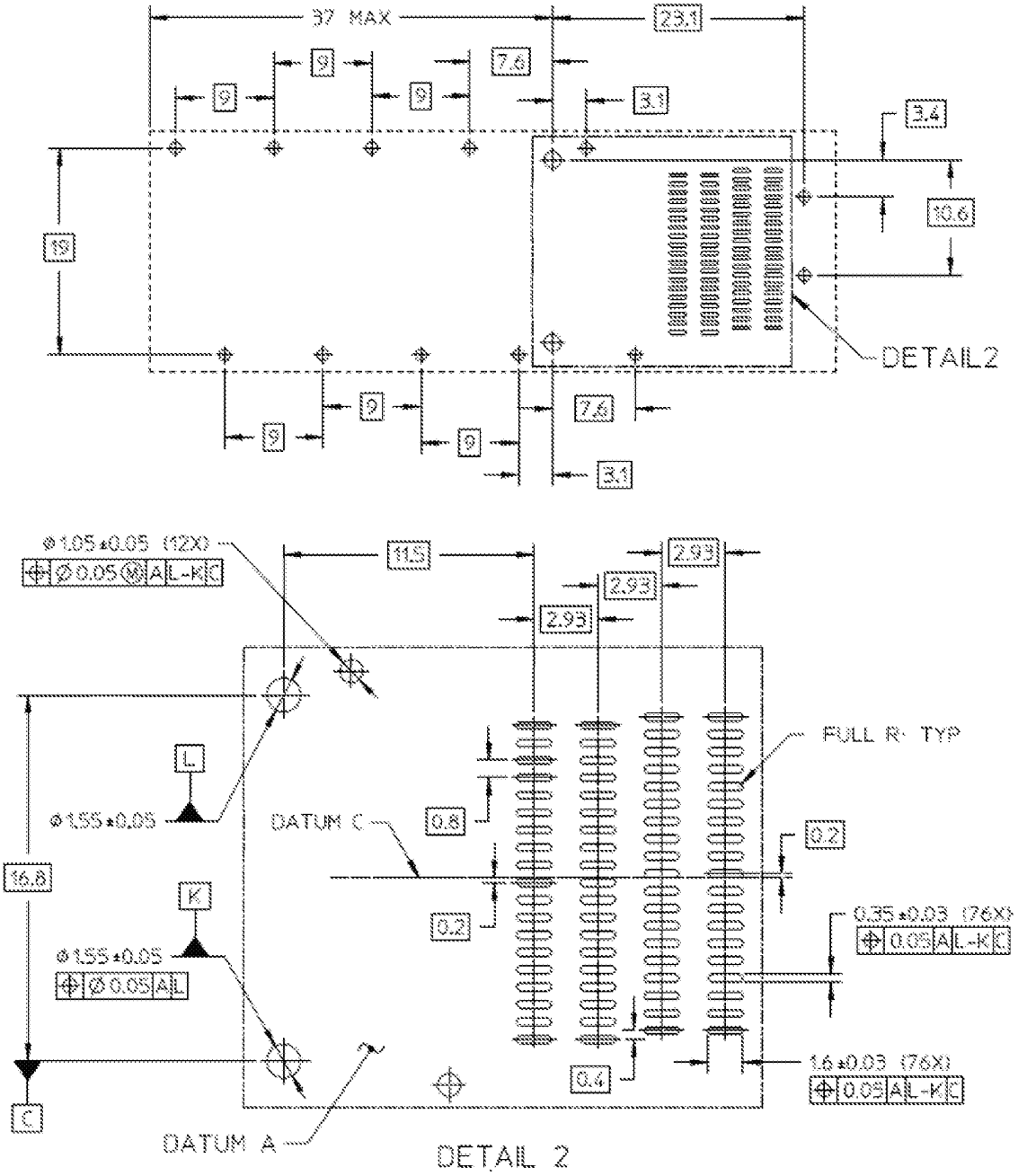


Figure 31: SMT Host PCB Mechanical Layout

Marvell Semiconductor, Inc. - Ex. 1002, Page 000095

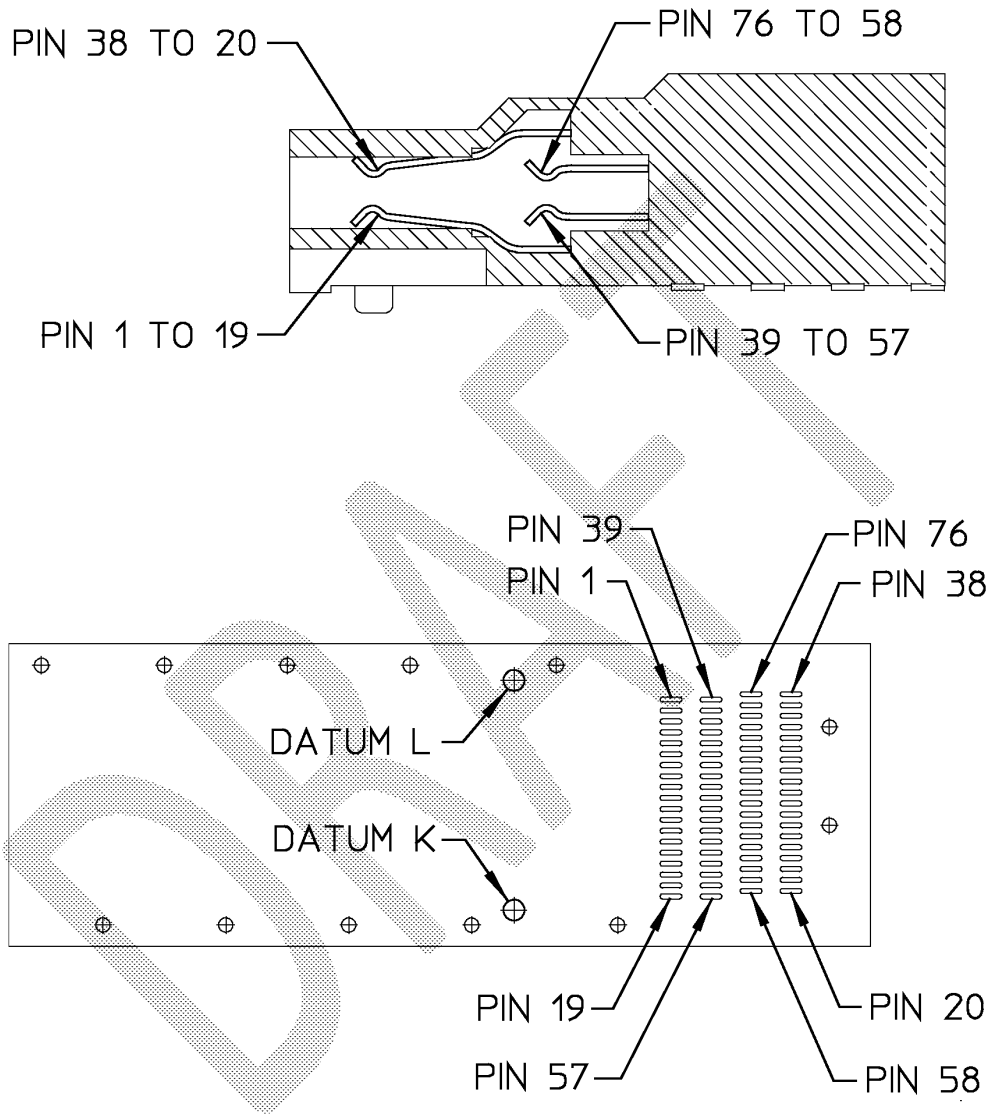


Figure 32: SMT Connector and Host PCB Pin Numbers

Marvell Semiconductor, Inc. - Ex. 1002, Page 000096

5.9 Module Color Coding and Labeling

An exposed feature of the QSFP-DD module (a feature or surface extending outside of the bezel) shall be color coded as follows:

- Beige for 850nm
- Blue for 1310nm
- White for 1550nm

Each QSFP-DD module shall be clearly labeled. The complete labeling need not be visible when the QSFP-DD module is installed and the bottom of the device is the recommended location for the label. Labeling shall include:

- Appropriate manufacturing and part number identification
- Appropriate regulatory compliance labeling
- A manufacturing traceability code

The label should also include clear specification of the external port characteristics such as:

- Optical wavelength
- Required fiber characteristics
- Operating data rate
- Interface standards supported
- Link length supported
- Connector Type

If required to comply with Section 6.3, a label must be applied to the top external surface of the module case, warning of high touch temperature.

The labeling shall not interfere with the mechanical, thermal or EMI features.

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000097

5.10 Optical Interface

The QSFP-DD optical interface port shall be either a male MPO receptacle (see Figure 34, Figure 35 and Figure 36), a dual LC (see Figure 37) or a CS connector (see Figure 38). The recommended location and numbering of the optical ports for each of the Media Dependent Interfaces is shown in Figure 33. The transmit and receive optical lanes shall occupy the positions depicted in Figure 33 when looking into the MDI receptacle with the connector keyway feature on top.

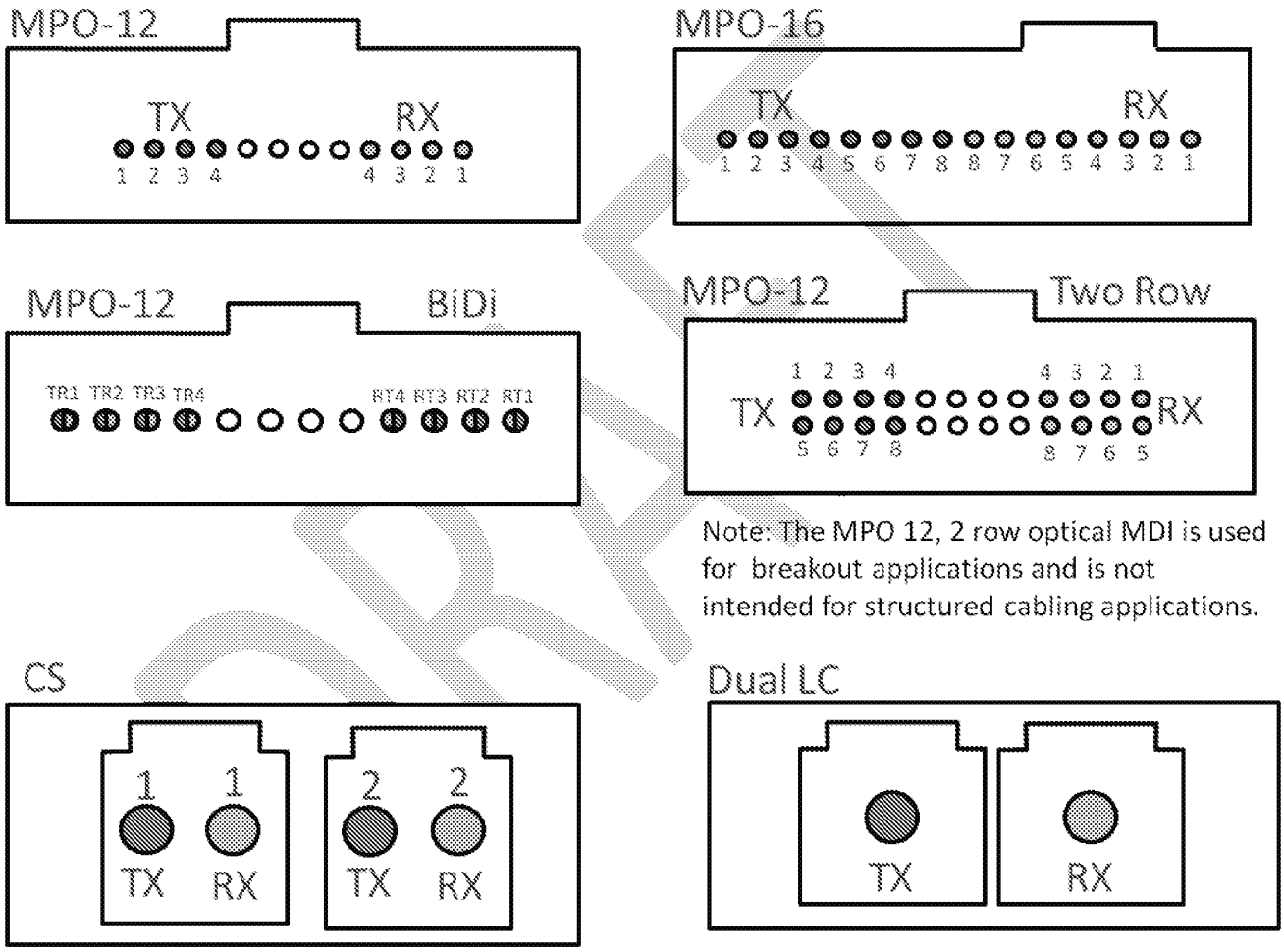


Figure 33: Optical Media Dependent Interface port assignments

Marvell Semiconductor, Inc. - Ex. 1002, Page 000098

5.10.1 MPO Optical Cable connections

The optical plug and receptacle for the MPO-12 connector is specified in TIA-604-5 and shown in Figure 34 (MPO-12 Single Row)and Figure 36 (MPO-12 Two Row). The optical plug and receptacle for the MPO-16 connector is specified in TIA-604-18 and shown in Figure 35 (MPO-16 Single Row). Note: This specification uses the terms MPO-12 in place of the TIA term MP0 and MPO-12 Two Row in place of the TIA term MPO Two Row.

Aligned keys are used to ensure alignment between the modules and the patchcords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top. Note: Two alignment pins are present in each receptacle.

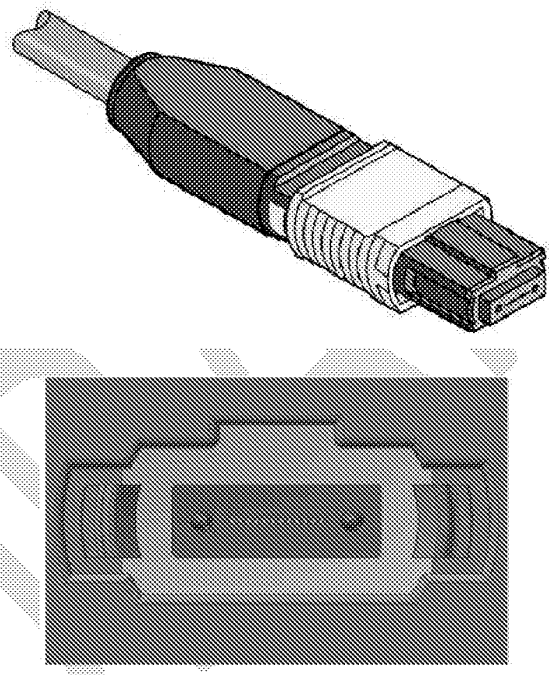


Figure 34: MPO-12 Single Row optical patch cord and module receptacle

Marvell Semiconductor, Inc. - Ex. 1002, Page 000099

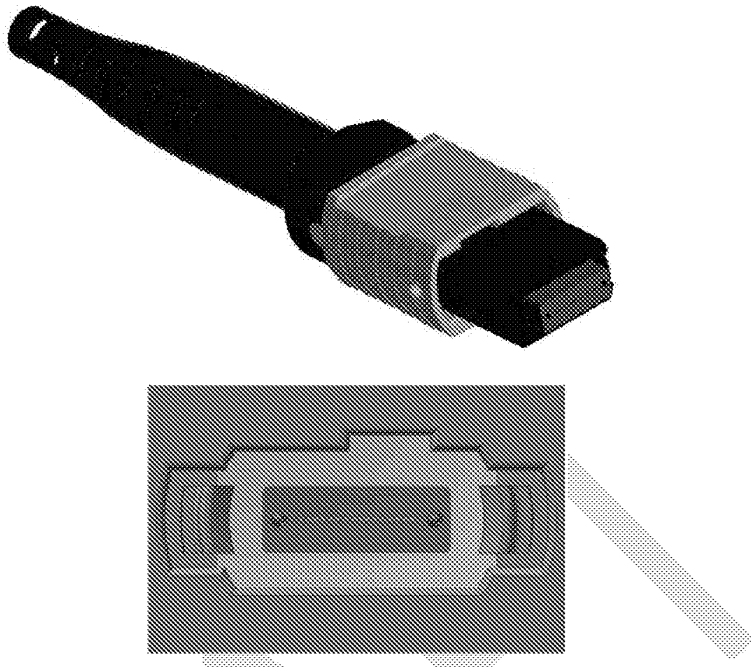


Figure 35: MPO-16 Single Row optical patchcord and module receptacle

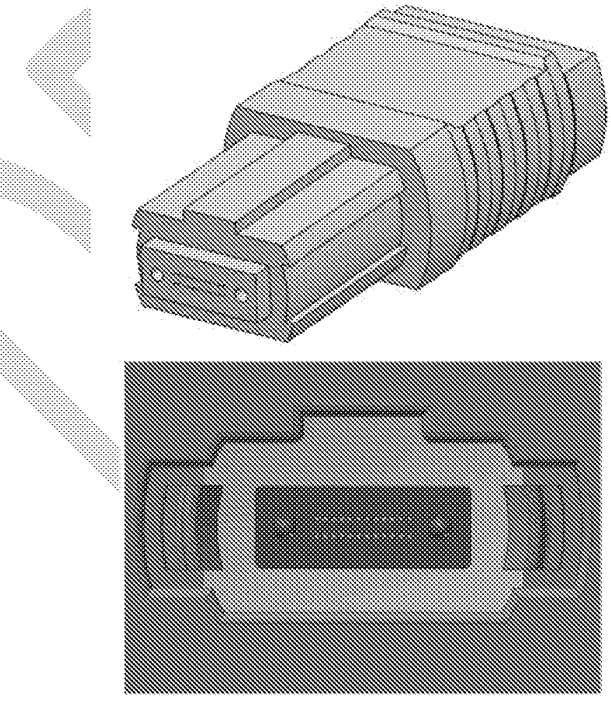


Figure 36: MPO-12 Two Row optical patchcord and module receptacle

5.10.2 Dual LC Optical Cable connection

The Dual LC optical patchcord and module receptacle is specified in TIA-604-10 and shown in Figure 37.

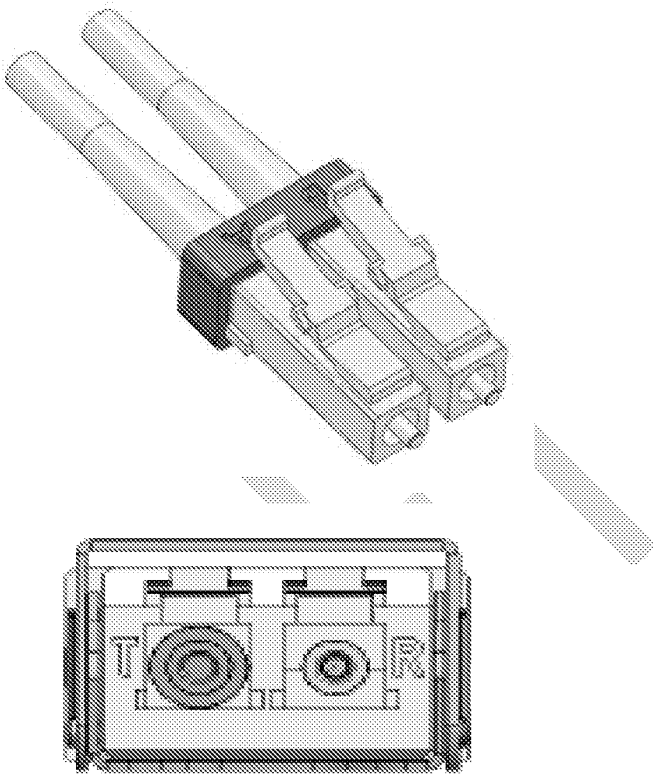


Figure 37: Dual LC optical patchcord and module receptacle

5.10.3 Dual CS Optical Cable connection

The Dual CS optical receptacle for a QSFP-DD module is specified in CS-01242017 (see Industry Documents) and shown in Figure 38.

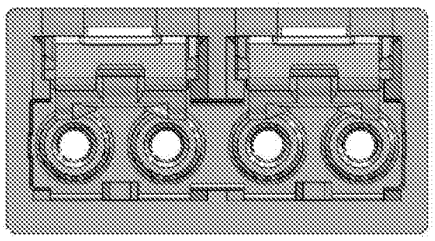


Figure 38: Dual CS connector module receptacle (in support of breakout applications)

Marvell Semiconductor, Inc. - Ex. 1002, Page 000101

5.10.4 Electrical data input/output to optical port mapping

Table 10 defines the mapping of electrical TX data inputs and RX data outputs to optical ports. Note that there is no defined mapping of electrical input/output to optical wavelengths for WDM applications.

Table 10- Electrical Signal to Optical Port Mapping

Electrical Signal	Optical Port Type (see Figure 33)				
	LC	CS or MPO-12	MPO-12	MPO-12 (two row) MPO-16	MPO-12 BiDi
	1 TX fiber 1 RX fiber[1]	2 TX fibers 2 RX fibers[1]	4 TX fibers 4 RX fibers[1]	8 TX fibers 8 RX fibers[1]	8 Tx (Rx) fibers[2]
Tx1	TX-1	TX-1	TX-1	TX-1	TR1
Tx2				TX-2	RT1
Tx3			TX-2	TX-3	TR2
Tx4				TX-4	RT2
Tx5		TX-2	TX-3	TX-5	TR3
Tx6				TX-6	RT3
Tx7			TX-4	TX-7	TR4
Tx8				TX-8	RT4
Rx1	RX-1	RX-1	RX-1	RX-1	RT1
Rx2				RX-2	TR1
Rx3			RX-2	RX-3	RT2
Rx4				RX-4	TR2
Rx5		RX-2	RX-3	RX-5	RT3
Rx6				RX-6	TR3
Rx7			RX-4	RX-7	RT4
Rx8				RX-8	TR4
Note 1: TX-n or RX-n where n is the optical port number as defined in Figure 33					
Note 2: TRn or RTn where n is the optical port number as defined in Figure 33					

6 Environmental and Thermal

QSFP-DD is designed to allow for up to 36 modules; stacked, ganged and/or belly-to-belly in a 1U 19" rack, with the appropriate thermal design for cooling/airflow.
The equipment supplier is responsible for controlling the module case temperature to the specified range. The module supplier is responsible for defining a point on the module case where the temperature is measured. This should be a point connected to an internal component with the least thermal margin, e.g. a laser diode. It is recommended that the defined point on the module case be behind the equipment faceplate in order to enable in-system monitoring.

6.1 Thermal Requirements

The module case temperature may be within one or more of the case temperatures ranges defined in Table 11. The temperature ranges are applicable between 60m below sea level and 1800m above sea level, utilizing the host systems designed airflow. For further information see *Telcordia GR-63-CORE, Issue 4, April 2012, NEBS™ Requirements: Physical Protection*.

Table 11- Temperature Range Class of operation

Class	Module Case Temperature
Standard	0°C through 70°C
Extended	-5°C through 85°C
Industrial	-40°C through 85°C

Marvell Semiconductor, Inc. - Ex. 1002, Page 000102

6.2 Thermal Requirements – tighter controlled environments

The classes in Table 12 are intended for tighter controlled environments, e.g. data center environments as described in *"Thermal guidelines for data processing environments", fourth Ed., ASHRAE, 2015.* The four classes correspond to different ranges of equipment intake air temperature.

Table 12- Temperature Range Classes for Tighter Controlled Applications

Class	Module Functional Case Temperature[1]	Module Performance Case Temperature[1]
A1	15°C to 62°C	25°C to 62°C
A2	10°C to 65°C	20°C to 65°C
A3	5°C to 70°C	15°C to 70°C
A4	5°C to 75°C	15°C to 75°C
Note 1: Functional includes all features available in Low Power Mode. Performance means all specifications are met in high power mode.		

6.3 External Case and Handle Touch Temperature

For all power classes, all module case and handle surfaces outside of the cage must comply with applicable touch temperature requirements. If the module case temperature will exceed applicable short-term touch temperature limits, a means must be provided to prevent contact with the case during unlatching and removal. Figure 10, Figure 11 and Appendix A show typical handles used to unlatch and remove the module, thereby limiting contact with the module case. Handles are typically low thermal conductivity elastomer and allow for a higher touch temperature. For more information see "*IEC/UL 60950-1* Requirements for Information Technology Equipment" and "*Telcordia GR-63-CORE, Issue 4, April 2012, NEBS™ Requirements: Physical Protection*".

7 Management Interface

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. The memory map for QSFP-DD is found in the 'Common Management Interface Specification for 8x/16x pluggable transceivers'. (see www.QSFP-DD.com) Some timing requirements are critical, especially for a multi-channel device, so the interface speed may optionally be increased. Byte 00h on the Lower Page or Address 128 Page 00h is used to indicate the use of the QSFP-DD memory map rather than the QSFP memory map. When a legacy QSFP28 module is inserted into a QSFP-DD port the legacy QSFP memory map (i.e. SFF-8636) must be used. This case is outside the scope of this document.

In some applications, muxing or demuxing may occur in the module. In this specification, all references to channel numbers are based on the electrical connector interface channels, unless otherwise indicated. In cases where a status or control aspect is applicable only to channels after muxing or demuxing has occurred, the status or control is intended to apply to all channels in the mux group, unless otherwise indicated.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000103

7.1 SCL, SDA and ModSEL Timing Specification

7.1.1 Introduction

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. Detailed electrical specifications are given in section 4.1.2. Nomenclature for all registers more than 1 bit long is MSB-LSB.

7.1.2 Management Interface Timing Specification

The timing requirements are shown in Figure 39 and specified in Table 13. QSFP-DD is positioned to leverage 2-wire timing (Fast Mode devices) to align the use of related cores on host ASICs. The default clock rate is a maximum of 400 kHz with an option to support up to a maximum of 1 MHz. This subsection closely follows the QSFP SFF-8636 specification.

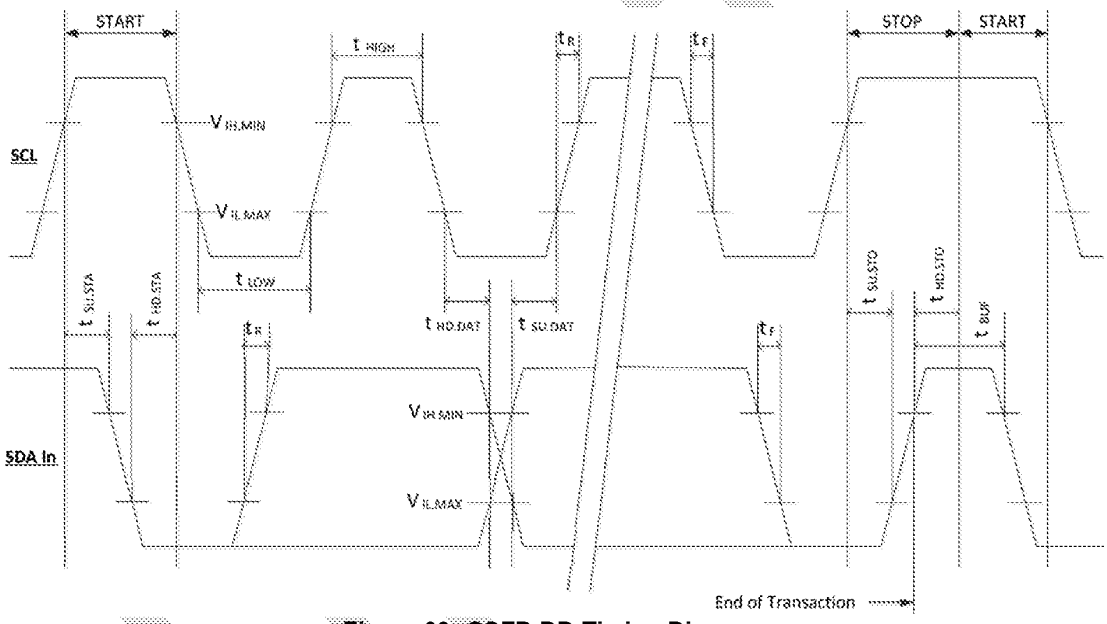


Figure 39: QSFP-DD Timing Diagram

The 2-wire serial interface address of the QSFP-DD module is 1010000X (A0h). In order to allow access to multiple QSFP-DD modules on the same 2-wire serial bus, the QSFP-DD includes a module select pad, ModSelL. This input (which is pulled high, deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.
Before initiating a 2-wire serial bus communication, the host shall provide setup time on the ModSelL line of all modules on the 2-wire bus. The host shall not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement is satisfied.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000104

7.1.3 Serial Interface Protocol

7.1.3.1 Management Timing Parameters

The timing parameters for the 2-Wire interface to the QSFP-DD module and the QSFP-DD memory transaction timings are shown in Table 13. Tradeoffs between pull-up resistor values, bus capacitance and rise time are shown in Figure 40.

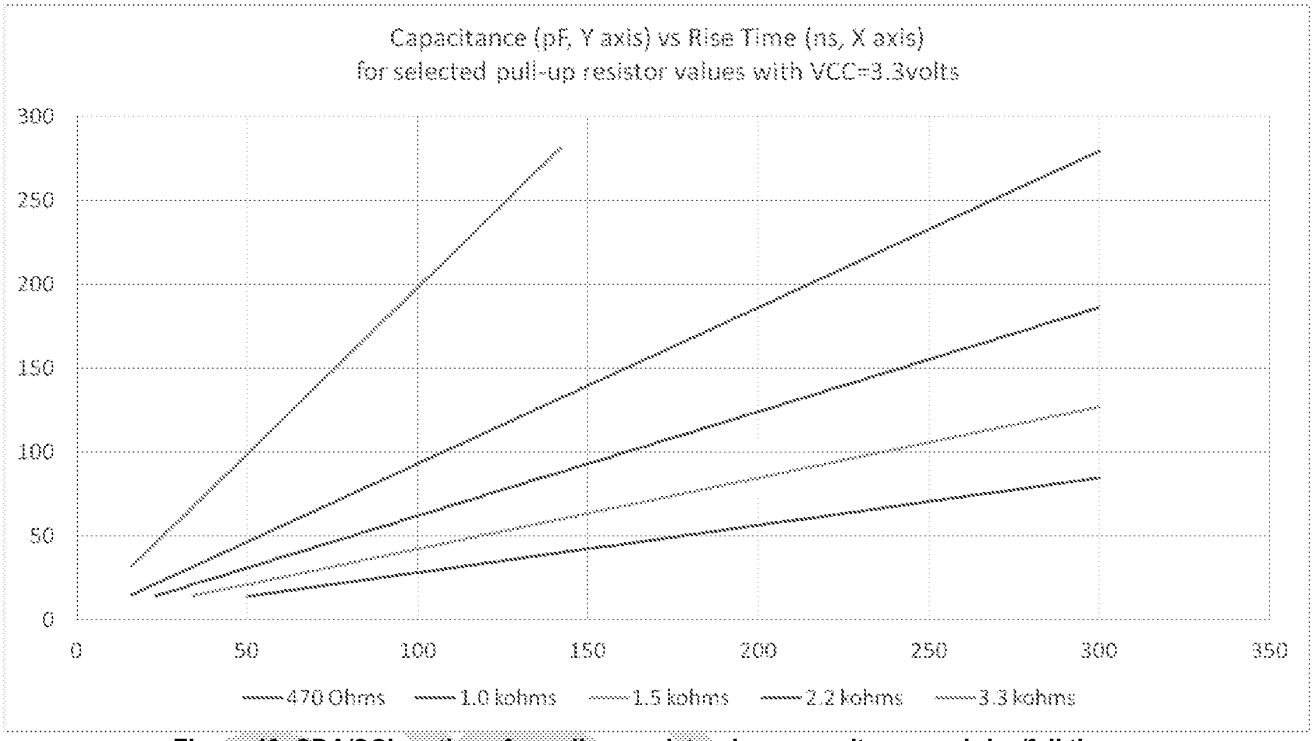


Figure 40: SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000105

Table 13- Management Interface timing parameters

		Fast Mode (400 KHz)		Fast Mode Plus (1 MHz)			
Parameter	Symbol	Min	Max	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	0	1000	KHz	
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		1		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	tR		300		120	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	tF		300		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		0.26		µs	
STOP Hold Time	tHD.STO	0.6		0.26		us	
Aborted sequence – bus release	Deselect_Abort	2		2		ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time	tSU.ModSelL	2		2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host initiated serial bus sequence.
ModSelL Hold Time[1]	tHD.ModSelL	2		2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module select status.
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500		500	us	Maximum time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write to non-volatile registers	tWR		80		80	ms	Complete Write of up to 8 Bytes
Endurance (Write Cycles)		50K			50k	cycles	Module Case Temperature = 70^0 C
Note 1: When the host has determined that module is QSFP-DD, the management registers can be read to determine alternate supported ModSelL set up and hold times.							

Marvell Semiconductor, Inc. - Ex. 1002, Page 000106

Appendix A: Informative overall module length with elastomeric handle attached to module latches

Figure 41 and Figure 42 show flexible elastomeric handles attached to the module latches. Handle ends for Types 1 and Type 2 modules should be aligned independent of module case extension. Type 1 modules should meet the overall length of 118mm maximum per Figure 41 with a handle length of approximately 50mm. Type 2 modules should comply with Figure 42 and have reduced handle length equal to the module case length extension

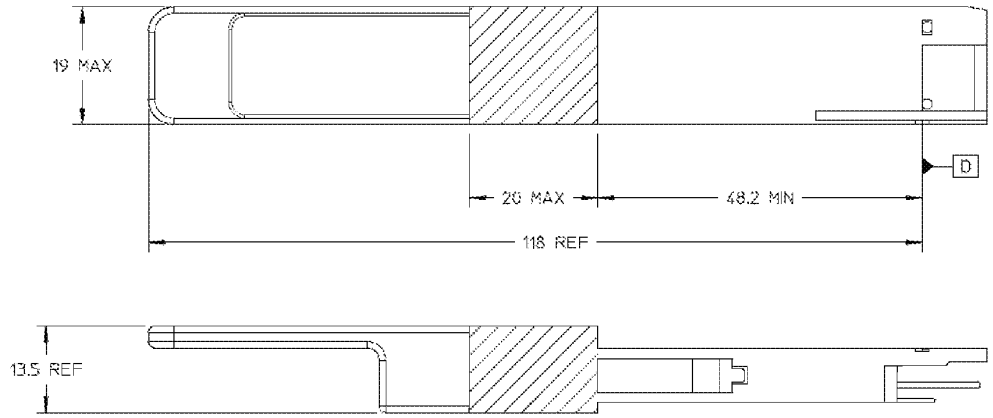


Figure 41: Informative overall module length with handle for Type 1 module

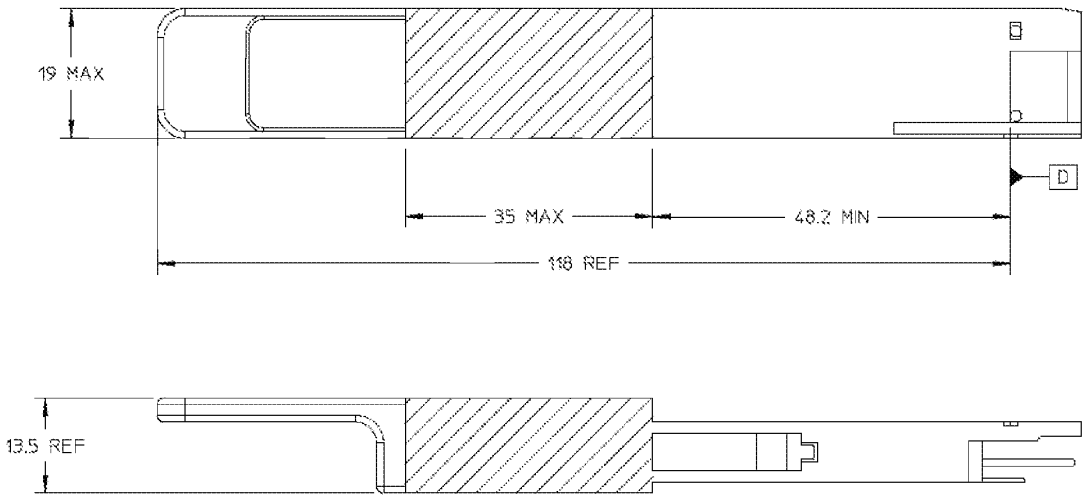


Figure 42: Informative overall module length with handle for Type 2 module

Marvell Semiconductor, Inc. - Ex. 1002, Page 000107

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End of Document

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000108

Fiber Optic Cabling Solutions

The largest solutions of pre-terminated fiber optics, including multimode and single-mode patch cords, MTP/MPO fiber trunks and harnesses, plug-n-play modules/cassettes and fiber enclosures.

40 Gigabit Ethernet Options Guideline



When the IEEE introduced the 802.3ba Ethernet standard, this was in response to the increasing bandwidth demands facing data centers, paving the way for the introduction of 40Gb/s and 100Gb/s Ethernet operations. Believe it or not, the 40 Gigabit Ethernet era is already upon us. This text put together a brief overview of the current 40 Gigabit Ethernet optics types and form factors to aid in planning for future high-performance Ethernet needs.

40 Gigabit Ethernet Standards

The IEEE 802.3ba introduced the 40 Gigabit and 100 Gigabit Ethernet standards in 2010. 802.3ba is the designation given to the higher speed Ethernet task force which completed its work to modify the 802.3 standard to support speeds higher than 10 Gbit/s. This was the first time two different Ethernet speeds were specified in a single standard. The table below gives detailed specifications for 40 Gigabit Ethernet standards.

Name	Medium	Specified distance
40GBASE-CR4	twinax copper cable	7 m
40GBASE-SR4	Multimode fiber	OM3 100m/OM4 125m
40GBASE-LR4	Singlemode fiber	10 km
40GBASE-ER4	Singlemode fiber	40 km
40GBASE-FR	Singlemode fiber	2 km
40GBASE-KR4	Backplane	1 m
40GBASE-T	Cat.8 twisted pair	30 m

40 Gigabit Ethernet QSFPTransceiver Options

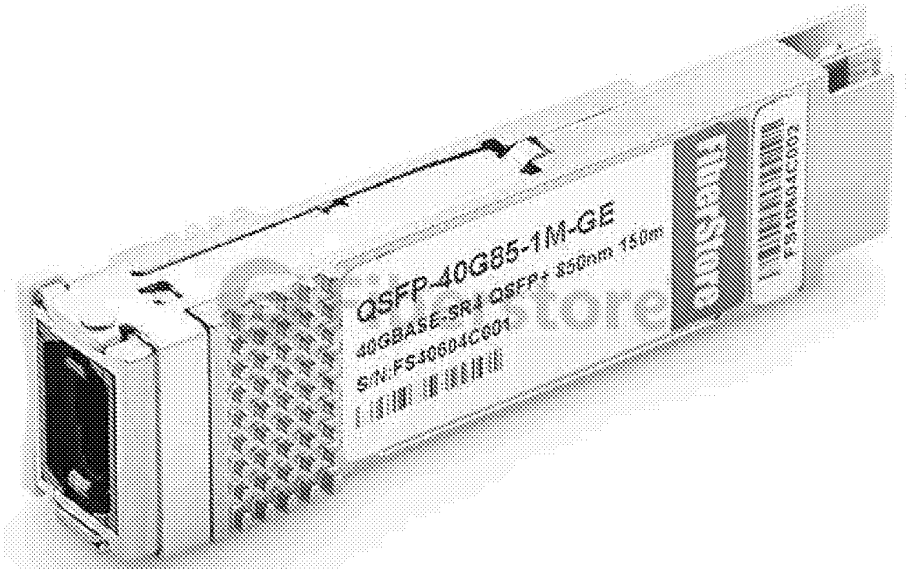
As with any new generation of technology, one design goal was to leverage as much existing technology as possible. By minimizing the number of new interfaces, the interfaces become less expensive and take

Marvell Semiconductor, Inc. - Ex. 1002, Page 000109

advantage of volume production and simplicity. To meet this design goal, there are three media modules will be used in the first generation of 40 Gigabit Ethernet: QSFP, CXP and CFP.

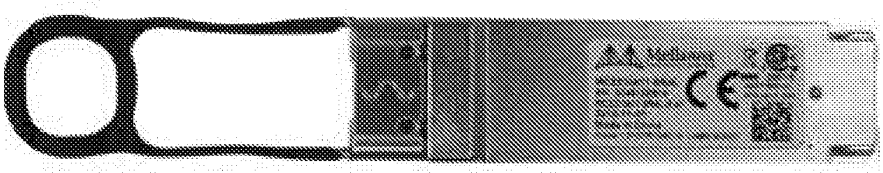
- QSFP

  The Quad Small-Form-Factor Pluggable (QSFP) is similar in size to the CXP and provides four transmit and four receive lanes to support 40 Gigabit Ethernet applications for multimode fiber and copper today and may serve single-mode in the future. Another future role for the QSFP may be to serve 100 Gigabit Ethernet when lane rates increase to 25 Gbps.



- CXP

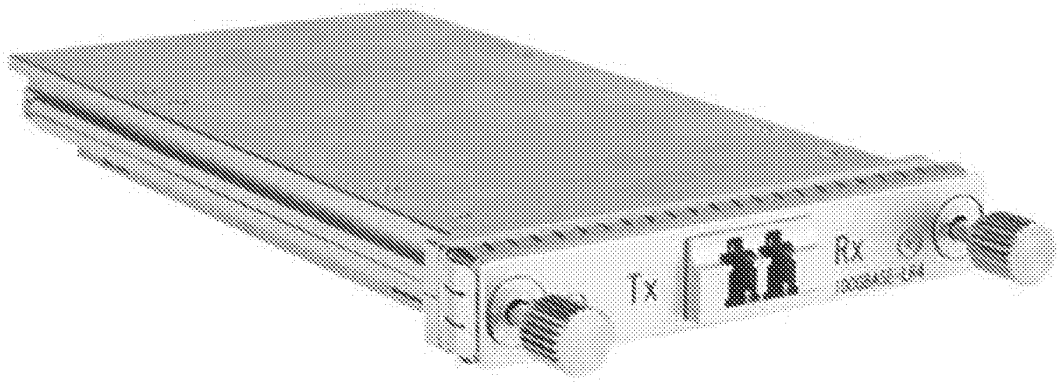
  The CXP transceiver features 12 transmit and 12 receive 10-Gbps lanes to support one 100 Gigabit Ethernet port, or up to three 40 Gigabit Ethernet ports. It can achieve rates up to 120 Gbps of pluggable data over 12 lanes in one assembly while enhanced-footprint connectors transmit signals over 10 lanes for up to 100 Gbps.



Marvell Semiconductor, Inc. - Ex. 1002, Page 000110

- CFP

  The C Form-Factor Pluggable (CFP) is a new media module that was designed for longer-reach applications, with up to 24 watts of power dissipation. Its dense electrical connectors and integrated, riding heat sink enable a range of interfaces. This module is used for 40GBASE-SR4, 40GBASE-LR4.



40GbE Cabling Options

The most common 40GbE cable is the QSFP+ Cable. Such as QSFP direct attach copper cable (DAC) and QSFP active optical cable (AOC). Besides, the MPO/MTP cable is considered the best solution for 40GbE. Since MPO/MTP connectors have either 12 fibres or 24 fibres array, which can allow data transmission across multiple fibres simultaneously.

- Direct Attach Copper Cable

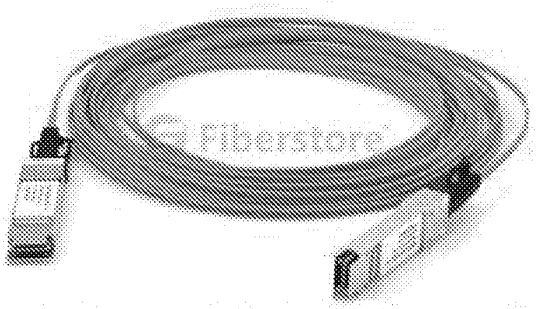
Transmitting 40 GbE over short distances of parallel coaxial copper cabling (also referred to as twinax cabling) is accomplished using a special cabling assembly with four lanes of coaxial cabling (eight pairs). Four pairs each transmit 10 Gbps in one direction and four transmit 10 Gbps in the other direction for a total data rate of 40 Gbps. The two common DACs used in 40g Ethernet are QSFP to QSFP and QSFP to 4 SFP+ copper direct-attach cables.



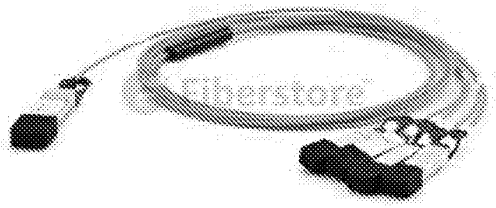
- Active Optical Cable

Marvell Semiconductor, Inc. - Ex. 1002, Page 000111

In the market, there are two common 40g fiber cable: QSFP to 4 SFP+ breakout AOC and QSFP to QSFP AOC. The former is a 4×10 Gb/s parallel active optical cable which transmits four separate streams of 10 Gb/s data over ribbon cables in a point-to-multipoint configuration. The cable contains a QSFP+ module on one end and four separate SFP+ modules at the other ends. The latter is a 40 Gb/s parallel active optical cable which transmits error-free parallel 4×10 Gb/s data over multimode fiber (MMF) ribbon cables.



QSFP to QSFP AOC



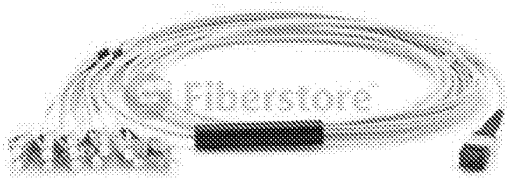
QSFP to 4 SFP+ Breakout AOC

- MPO/MTP Cable

Current multi-mode optics standards for 40GbE optics use multiple 10Gbps lasers, simultaneously transmitting across multiple fiber strands to achieve high data rates. Because of the multi-lane nature of these optics, 40GbE multi-mode optics use a different style of fiber cabling, known as MPO or MTP cabling. As with 10GbE optics over multi-mode fiber, an OM3 or OM4 grade MMF is needed to be able to cover longer distances. For 40g Ethernet, we can use 8 fibers MPO/MTP harness cables or 12 fibers MPO/MTP trunk cables. The former is to directly connect a QSFP port to other 4 SFP+ ports. The latter is to directly connect one QSFP port to another QSFP port.



MPO/MTP Trunk Cable



MPO/MTP Harness Cable

Related articles:

40G Network Connectivity Solutions
MTP Fiber Cable Solutions
Three Types MTP Harness Cables Used in Today's Data Center

Marvell Semiconductor, Inc. - Ex. 1002, Page 000112

This entry was posted in QSFP+ Transceiver and tagged 40 Gigabit Ethernet, 40G QSFP+, 40GBASE-LR4, 40GBASE-SR4, CFP module, CXP Transceiver, MPO MTP Fiber on May 25, 2015 [http://www.cables-solutions.com/guide-to-40-gigabit-ethernet-options.html] by Alice.Gui.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000113

IEEE P802.3cd™/D1.2

Draft Standard for Ethernet Amendment: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation

Prepared by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

This draft is an amendment of IEEE Std 802.3-2015 as amended by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, IEEE Std 802.3bp-2016, IEEE Std 802.3br-2016, IEEE Std 802.3bn-2016, IEEE Std 802.3bz-2016, and [many others]. This amendment defines IEEE 802.3 Media Access Control (MAC) parameters, Physical Layer specifications, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s. Draft D1.2 is prepared for Task Force review. This draft expires 6 months after the date of publication or when the next version is published, whichever comes first.

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Abstract: This amendment to IEEE Std 802.3-2015 adds Clause 131 through Clause 140 and Annex 135A through Annex 136C. This amendment includes IEEE 802.3 Media Access Control (MAC) parameters, Physical Layer specifications, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

Keywords: 50GAUI-1, 50GAUI-2, 50GBASE-CR, 50GBASE-KR, 50GBASE-FR, 50GBASE-LR, 50GBASE-SR, 50 Gigabit Ethernet, 50GMII, 100GAUI-2, 100GAUI-4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100 Gigabit Ethernet, 200GBASE-CR4, 200GBASE-KR4, 200GBASE-SR4, 200 Gigabit Ethernet, Energy Efficient Ethernet (EEE), Ethernet, forward error correction (FEC), IEEE 802.3™, IEEE Std 802.3cd™, LAUI-2, MMF, SMF.

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Introduction

This introduction is not part of IEEE Std 802.3cd-20xx, IEEE Draft Standard for Ethernet. Amendment: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the date of IEEE Std 802.3cd-20xx publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines ser-

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vices and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw™-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by™-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq™-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bp™-2016

Amendment 4—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 97 and Clause 98. This amendment adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable in automotive and other applications not utilizing the structured wiring plant.

IEEE Std 802.3br™-2016

Amendment 5—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 99. This amendment adds a MAC Merge sublayer and a MAC Merge Service Interface to support for Interspersing Express Traffic over a single link.

IEEE Std 802.3bn™-2016

Amendment 6—This amendment adds the Physical Layer specifications and management parameters for symmetric and/or asymmetric operation of up to 10 Gb/s on point-to-multipoint Radio Frequency (RF) distribution plants comprising either amplified or passive coaxial media. It also extends the operation of Ethernet Passive Optical Networks (EPON) protocols, such as Multipoint Control Protocol (MPCP) and Operation Administration and Management (OAM).

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IEEE Std 802.3bz™-2016

Amendment 7—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 125 and Clause 126. This amendment adds new rates of 2.5 Gb/s and 5 Gb/s and new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bu™-201x

Amendment 8—This amendment includes changes to IEEE Std 802.3-2015 to define a methodology for the provision of power via a single twisted pair to connected Data Terminal Equipment (DTE) with IEEE 802.3 single twisted-pair interfaces.

IEEE Std 802.3bv™-201x

Amendment 9—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 115 and Annex 115A. This amendment adds point-to-point 1000 Mb/s Physical Layer (PHY) specifications and management parameters for operation on duplex plastic optical fiber (POF) targeting use in automotive, industrial, home-network, and other applications.

IEEE Std 802.3bs™-201x

This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 116 through Clause 124 and Annex 119A through Annex 120E. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 200 Gb/s and 400 Gb/s.

IEEE Std 802.3[others]™-201x

This amendment includes…

IEEE Std 802.3cd™-201x

This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 131 through Clause 140 and Annex 135A through Annex 136C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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Contents

1. Introduction 36

1.1 Overview 36
1.1.3 Architectural perspectives 36
1.1.3.2 Compatibility interfaces 36
1.3 Normative references 36
1.4 Definitions 37
1.5 Abbreviations 38

4. Media Access Control 39

4.4 Specific implementations 39
4.4.2 MAC parameters 39

30. Management 40

30.3 Layer management for DTEs 40
30.3.2 PHY device managed object class 40
30.3.2.1 PHY device attributes 40
30.3.2.1.2 aPhyType 40
30.3.2.1.3 aPhyTypeList 40
30.3.2.1.5 aSymbolErrorDuringCarrier 40
30.5 Layer management for medium attachment units (MAUs) 40
30.5.1 MAU managed object class 40
30.5.1.1 MAU attributes 40
30.5.1.1.2 aMAUType 40
30.5.1.1.4 aMediaAvailable 41
30.5.1.1.11 aBIPErrorCount 42
30.5.1.1.12 aLaneMapping 42
30.5.1.1.15 aFECAbility 42
30.5.1.1.17 aFECCorrectedBlocks 42
30.5.1.1.18 aFECUncorrectableBlocks 43
30.5.1.1.26 aRSFECBIPErrorCount 43
30.5.1.1.27 aRSFECLaneMapping 43
30.6 Management for link Auto-Negotiation 44
30.6.1 Auto-Negotiation managed object class 44
30.6.1.1 Auto-Negotiation attributes 44
30.6.1.1.5 aAutoNegLocalTechnologyAbility 44

45. Management Data Input/Output (MDIO) Interface 45

45.2 MDIO Interface Registers 45
45.2.1 PMA/PMD registers 45
45.2.1.1 PMA/PMD control 1 register (Register 1.0) 46
45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2) 46
45.2.1.2 PMA/PMD status 1 register (Register 1.1) 47
45.2.1.2.3 Fault (1.1.7) 47
45.2.1.4 PMA/PMD speed ability (Register 1.4) 48
45.2.1.4.6a 50G capable (1.4.3) 48
45.2.1.6 PMA/PMD control 2 register (Register 1.7) 48
45.2.1.6.3 PMA/PMD type selection (1.7.6:0) 50

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000127

45.2.1.7 PMA/PMD status 2 register (Register 1.8) 51
45.2.1.7.4 Transmit fault (1.8.11) 51
45.2.1.7.5 Receive fault (1.8.10) 51
45.2.1.8 PMD transmit disable register (Register 1.9) 52
45.2.1.14b1 50G PMA/PMD extended ability (Register 1.20) 53
45.2.1.14b1.1 50G PMA remote loopback ability (1.20.15) 53
45.2.1.14b1.2 50GBASE-LR ability (1.20.4) 53
45.2.1.14b1.3 50GBASE-FR ability (1.20.3) 53
45.2.1.14b1.4 50GBASE-SR ability (1.20.2) 54
45.2.1.14b1.5 50GBASE-CR ability (1.20.1) 54
45.2.1.14b1.6 50GBASE-KR ability (1.20.0) 54
45.2.1.14f1 PMA/PMD extended ability 2 (Register 1.25) 54
45.2.1.14f1.1 50G extended abilities (1.25.0) 54
45.2.1.101 RS-FEC control register (Register 1.200) 55
45.2.1.101.aa Four-lane PMD (1.200.3) 55
45.2.1.102 RS-FEC status register (Register 1.201) 55
45.2.1.102.1 PCS align status (1.201.15) 56
45.2.1.102.2 RS-FEC align status (1.201.14) 56
45.2.1.102.5 FEC AM lock 1 (1.201.9) 56
45.2.1.102.6 FEC AM lock 0 (1.201.8) 56
45.2.1.102.6a FEC optional states supported (1.201.7) 56
45.2.1.108 RS-FEC BIP error counter lane 0 (Register 1.230) 56
45.2.1.116d 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register (Register 1.500) 57
45.2.1.116d.1 Request flag (1.500.15) 58
45.2.1.116d.2 Post-cursor request (1.500.14:12) 58
45.2.1.116d.3 Pre-cursor request (1.500.11:10) 58
45.2.1.116d.4 Post-cursor remote setting (1.500.9:7) 58
45.2.1.116d.5 Pre-cursor remote setting (1.500.6:5) 59
45.2.1.116d.6 Post-cursor local setting (1.500.4:2) 59
45.2.1.116d.7 Pre-cursor local setting (1.500.1:0) 59
45.2.1.116e 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 1 through lane 15 registers (Registers 1.501 through 1.515) 59
45.2.1.116f 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register (Register 1.516) 59
45.2.1.116f.1 Request flag (1.516.15) 59
45.2.1.116f.2 Post-cursor request (1.516.14:12) 61
45.2.1.116f.3 Pre-cursor request (1.516.11:10) 61
45.2.1.116f.4 Post-cursor remote setting (1.516.9:7) 61
45.2.1.116f.5 Pre-cursor remote setting (1.516.6:5) 61
45.2.1.116f.6 Post-cursor local setting (1.516.4:2) 61
45.2.1.116f.7 Pre-cursor local setting (1.516.1:0) 61
45.2.1.116g 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 15 registers (Registers 1.517 through 1.531) 62
45.2.1.116h PMA precoder control down Tx (Register 1.600) 62
45.2.1.116h.1 PMA precoder down Tx enable lane 3 (1.600.3) 62
45.2.1.116h.2 PMA precoder down Tx enable lane 2 (1.600.2) 62
45.2.1.116h.3 PMA precoder down Tx enable lane 1 (1.600.1) 62
45.2.1.116h.4 PMA precoder down Tx enable lane 0 (1.600.0) 62
45.2.1.116i PMA precoder control down Rx (Register 1.601) 62
45.2.1.116i.1 PMA precoder down Rx enable lane 3 (1.601.3) 63
45.2.1.116i.2 PMA precoder down Rx enable lane 2 (1.601.2) 63

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This is an unapproved IEEE Standards draft, subject to change.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000128

45.2.1.116i.3 PMA precoder down Rx enable lane 1 (1.601.1) 63
45.2.1.116i.4 PMA precoder down Rx enable lane 0 (1.601.0) 63
45.2.1.116j PMA precoder control up Tx (Register 1.602) 63
45.2.1.116j.1 PMA precoder up Tx enable lane 1 (1.602.1) 64
45.2.1.116j.2 PMA precoder up Tx enable lane 0 (1.602.0) 64
45.2.1.116k PMA precoder control up Rx (Register 1.603) 64
45.2.1.116k.1 PMA precoder up Rx enable lane 1 (1.603.1) 64
45.2.1.116k.2 PMA precoder up Rx enable lane 0 (1.603.0) 64
45.2.1.116l PMA precoder request status (Register 1.604) 64
45.2.1.116l.1 PMA precoder request status lane 1 (1.604.1) 65
45.2.1.116l.2 PMA precoder request status lane 0 (1.604.0) 65
45.2.1.116m PMA precoder request down (Register 1.605) 65
45.2.1.116m.1 PMA precoder request down lane 1 (1.605.1) 65
45.2.1.116m.2 PMA precoder request down lane 0 (1.605.0) 65
45.2.1.116n PMA precoder request up (Register 1.606) 65
45.2.1.116n.1 PMA precoder request up lane 1 (1.606.1) 66
45.2.1.116n.2 PMA precoder request up lane 0 (1.606.0) 66
45.2.1.118a BASE-R PAM4 PMD training LP control registers, lanes 0 through 3 (Register 1.1120 through 1.1123) 66
45.2.1.119a BASE-R PAM4 PMD training LP status registers, lanes 0 through 3 (Register 1.1220 through 1.1223) 67
45.2.1.120a BASE-R PAM4 PMD training LD control registers, lanes 0 through 3 (Register 1.1320 through 1.1323) 68
45.2.1.121a BASE-R PAM4 PMD training LD status registers, lanes 0 through 3 (Register 1.1420 through 1.1423) 69
45.2.1.124 PRBS pattern testing control (Register 1.1501) 70
45.2.3 PCS registers 70
45.2.3.1 PCS control 1 register (Register 3.0) 70
45.2.3.2 PCS status 1 register (Register 3.1) 71
45.2.3.2.7 PCS receive link status (3.1.2) 71
45.2.3.4 PCS speed ability (Register 3.4) 71
45.2.3.4.5a 50G capable (3.4.5) 71
45.2.3.6 PCS control 2 register (Register 3.7) 72
45.2.3.7 PCS status 2 register (Register 3.8) 72
45.2.3.7.3ab 50GBASE-R capable (3.8.8) 73
45.2.3.9 EEE control and capability 1 (Register 3.20) 73
45.2.3.9.a 50GBASE-R EEE fast wake supported (3.20.14) 73
45.2.3.13 BASE-R and MultiGBASE-T PCS status 1 register (Register 3.32) 73
45.2.3.13.1 BASE-R and MultiGBASE-T receive link status (3.32.12) 73
45.2.3.13.4 BASE-R and MultiGBASE-T PCS high BER (3.32.1) 74
45.2.3.13.5 BASE-R and MultiGBASE-T PCS block lock (3.32.0) 74
45.2.3.14 BASE-R and MultiGBASE-T PCS status 2 register (Register 3.33) 74
45.2.3.14.1 Latched block lock (3.33.15) 74
45.2.3.14.2 Latched high BER (3.33.14) 74
45.2.3.14.3 BER(3.33.13:8) 75
45.2.3.14.4 Errored blocks (3.33.7:0) 75
45.2.3.17 BASE-R PCS test-pattern control register (Register 3.42) 75
45.2.7 Auto-Negotiation registers 75
45.2.7.12 Backplane Ethernet, BASE-R copper status (Register 7.48) 76
45.2.7.12.2 Negotiated Port Type (7.48.1, 7.48.2, 7.48.3, 7.48.5, 7.48.6, 7.48.8, 7.48.9, 7.48.10, 7.48.11, 7.48.12, 7.48.13, 7.48.14, 7.48.15, 7.49.0, 7.49.1, 7.49.2) 76
45.2.7.12a Backplane Ethernet, BASE-R copper status 2 (Register 7.49) 76
45.2.7.12a.1 Negotiated Port Type 76

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This is an unapproved IEEE Standards draft, subject to change.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000129

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) interface 77
45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface 77
45.5.3.3 PMA/PMD management functions 77

69. Introduction to Ethernet operation over electrical backplanes 78

69.1 Overview 78
69.1.1 Scope 78
69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model 78
69.2 Summary of Backplane Ethernet Sublayers 80
69.2.1 Reconciliation sublayer and media independent interfaces 80
69.2.3 Physical Layer signaling systems 80
69.3 Delay constraints 82
69.5 Protocol implementation conformance statement (PICS) proforma 82

73. Auto-Negotiation for backplane and copper cable assembly 83

73.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model 83
73.3 Functional specifications 83
73.5 DME transmission 84
73.5.1 DME electrical specifications 84
73.6 Link codeword encoding 84
73.6.4 Technology Ability Field 84
73.7 Receive function requirements 85
73.7.1 DME page reception 85
73.7.6 Priority Resolution function 86
73.10 State diagrams and variable definitions 86
73.10.1 State diagram variables 86
73.10.2 State diagram timers 87
73.11 Protocol implementation conformance statement (PICS) proforma for Clause 73, Auto-Negotiation for backplane and copper cable assembly 89
73.11.4 PICS proforma tables for Auto-Negotiation for backplane and copper cable assembly 89
73.11.4.3 Link codeword encoding 89
73.11.4.7 State diagrams and variable definitions 89

78. Energy-Efficient Ethernet (EEE) 90

78.1 Overview 90
78.1.4 PHY types optionally supporting EEE 90
78.5 Communication link access latency 91

80. Introduction to 40 Gb/s and 100 Gb/s networks 92

80.1 Overview 92
80.1.3 Relationship of 40 Gigabit and 100 Gigabit Ethernet to the ISO OSI reference model 92
80.1.4 Nomenclature 93
80.1.5 Physical Layer signaling systems 93
80.2 Summary of 40 Gigabit and 100 Gigabit Ethernet sublayers 95
80.2.1 Physical Coding Sublayer (PCS) 95
80.2.3 Forward Error Correction (FEC) sublayers 95
80.2.4 Physical Medium Attachment (PMA) sublayer 95
80.2.5 Physical Medium Dependent (PMD) sublayer 96
80.2.6 Auto-Negotiation 96

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000130

80.4 Delay constraints 97
80.5 Skew constraints 98

82. Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R 101

82.6 Auto-Negotiation 101
82.7 Protocol implementation conformance statement (PICS) proforma for Clause 82, Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R 101
82.7.4 PICS Proforma Tables for PCS, type 40GBASE-R and 100GBASE-R 101
82.7.4.5 Test-pattern modes 101
82.7.4.7 Management 101
82.7.4.11 Auto-Negotiation for Backplane Ethernet functions 102

90. Ethernet support for time synchronization protocols 103

90.1 Introduction 103

91. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs 104

91.5 Functions within the RS-FEC sublayer 104
91.5.2 Transmit function 104
91.5.2.6 Alignment marker mapping and insertion 104
91.5.2.7 Reed-Solomon encoder 104
91.5.3 Receive function 105
91.5.3.1 Alignment lock and deskew 105
91.5.3.3 Reed-Solomon decoder 106
91.5.4 Detailed functions and state diagrams 106
91.5.4.2 State variables 106
91.5.4.2.1 Variables 106
91.5.4.2.3 Counters 106
91.6 RS-FEC MDIO function mapping 107
91.6.2a four_lane_pmd 107
91.6.5a FEC_optional_states 107
91.7 Protocol implementation conformance statement (PICS) proforma for Clause 91, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs 108
91.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs 108
91.7.4.1 Transmit function 108
91.7.4.3 State diagrams 108

116. Introduction to 200 Gb/s and 400 Gb/s networks 109

116.1 Overview 109
116.1.2 Relationship of 200 Gigabit and 400 Gigabit Ethernet to the ISO OSI reference model 109
116.1.3 Nomenclature 109
116.1.4 Physical Layer signaling systems 109
116.2 Summary of 200 Gigabit and 400 Gigabit Ethernet sublayers 111
116.2.5 Physical Medium Dependent (PMD) sublayer 111
116.4 Delay constraints 111

119. Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R 112

119.6 Auto-Negotiation 112

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000131

119.7 Protocol implementation conformance statement (PICS) proforma for Clause 119, Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R ... 112
119.7.4 PICS proforma tables for Physical Coding Sublayer (PCS) 64B/66B, type 200GBASE-R and 400GBASE-R ... 112
119.7.4.12 Auto-Negotiation for Backplane Ethernet functions ... 112

120. Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R ... 113

120.5 Functions within the PMA ... 113
120.5.7 PAM4 Encoding ... 113
120.5.7.1 Gray coding for PAM4 encoded lanes ... 113
120.5.7.2 Precoding for PAM4 encoded lanes ... 113
120.6 PMA MDIO function mapping ... 114
120.7 Protocol implementation conformance statement (PICS) proforma for Clause 120, Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R ... 115
120.7.7 Encoding ... 115

131. Introduction to 50 Gb/s networks ... 116

131.1 Overview ... 116
131.1.1 Scope ... 116
131.1.2 Relationship of 50 Gigabit Ethernet to the ISO OSI reference model ... 116
131.1.3 Nomenclature ... 117
131.1.4 Physical Layer signaling systems ... 117
131.2 Summary of 50 Gigabit Ethernet sublayers ... 118
131.2.1 Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) ... 118
131.2.2 Physical Coding Sublayer (PCS) ... 119
131.2.3 Forward Error Correction (FEC) sublayer ... 119
131.2.4 Physical Medium Attachment (PMA) sublayer ... 119
131.2.5 Physical Medium Dependent (PMD) sublayer ... 119
131.2.6 Management interface (MDIO/MDC) ... 119
131.2.7 Management ... 119
131.3 Service interface specification method and notation ... 119
131.3.1 Inter-sublayer service interface ... 120
131.3.2 Instances of the Inter-sublayer service interface ... 120
131.3.3 Semantics of inter-sublayer service interface primitives ... 120
131.4 Delay constraints ... 122
131.5 Skew constraints ... 122
131.6 State diagrams ... 125
131.7 Protocol implementation conformance statement (PICS) proforma ... 125

132. Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation ... 127

132.1 Overview ... 127
132.1.1 Summary of major concepts ... 127
132.1.2 Application ... 127
132.1.3 Rate of operation ... 127
132.1.4 Delay constraints ... 128
132.1.5 Allocation of functions ... 129
132.1.6 50GMII structure ... 129
132.1.7 Mapping of 50GMII signals to PLS service primitives ... 129
132.2 50GMII data stream ... 129
132.3 50GMII functional specifications ... 129
132.4 LPI assertion and detection ... 129

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This is an unapproved IEEE Standards draft, subject to change.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000132

132.5 Protocol implementation conformance statement (PICS) proforma for Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation 130
132.5.1 Introduction 130
132.5.2 Identification 130
132.5.2.1 Implementation identification 130
132.5.2.2 Protocol summary 130
132.5.2.3 Major capabilities/options 131
132.5.3 PICS proforma Tables for Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation 131
132.5.3.1 General 131
132.5.3.2 Mapping of PLS service primitives 131

133. Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R 132

133.1 Overview 132
133.1.1 Scope 132
133.1.2 Relationship of 50GBASE-R to other standards 132
133.1.3 Summary of 50GBASE-R sublayers 132
133.1.3.1 Physical Coding Sublayer (PCS) 132
133.1.4 Inter-sublayer interfaces 132
133.1.4.1 PCS service interface (50GMII) 133
133.1.4.2 Forward Error Correction (FEC) or Physical Medium Attachment (PMA) service interface 133
133.1.5 Functional block diagram 133
133.2 Physical Coding Sublayer (PCS) 134
133.2.1 Functions within the PCS 134
133.2.2 Alignment marker insertion 135
133.2.3 PCS lane deskew 136
133.2.4 Detailed functions and state diagrams 136
133.3 Delay constraints 136
133.4 Auto-Negotiation 136
133.5 Protocol implementation conformance statement (PICS) proforma for Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R 137
133.5.1 Introduction 137
133.5.2 Identification 137
133.5.2.1 Implementation identification 137
133.5.2.2 Protocol summary 137
133.5.3 Major capabilities/options 138
133.5.4 PICS Proforma Tables for Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R 138
133.5.4.1 Coding rules 138
133.5.4.2 Scrambler and Descrambler 139
133.5.4.3 Deskew and Reordering 139
133.5.4.4 Alignment Markers 139
133.5.4.5 Test-pattern modes 139
133.5.4.6 Bit order 140
133.5.4.7 Management 140
133.5.4.8 State diagrams 140
133.5.4.9 Loopback 141
133.5.4.10 Delay constraints 141
133.5.4.11 Auto-Negotiation for Backplane Ethernet functions 141

134. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs 142

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000133

134.1 Overview ... 142
134.1.1 Scope ... 142
134.1.2 Position of RS-FEC in the 50GBASE-R sublayers ... 142
134.2 FEC service interface ... 142
134.3 PMA compatibility ... 143
134.4 Delay constraints ... 144
134.5 Functions within the RS-FEC sublayer ... 144
134.5.1 Functional block diagram ... 144
134.5.2 Transmit function ... 144
134.5.2.1 PCS Lane block synchronization ... 144
134.5.2.2 PCS Alignment lock and deskew ... 144
134.5.2.3 PCS Lane reorder ... 144
134.5.2.4 Alignment marker removal ... 144
134.5.2.5 64B/66B to 256B/257B transcoder ... 145
134.5.2.6 Alignment marker mapping and insertion ... 146
134.5.2.7 Reed-Solomon encoder ... 147
134.5.2.8 Symbol distribution ... 147
134.5.2.9 Transmit bit ordering ... 147
134.5.3 Receive function ... 147
134.5.3.1 Alignment lock and deskew ... 147
134.5.3.2 FEC Lane reorder ... 149
134.5.3.3 Reed-Solomon decoder ... 149
134.5.3.4 Alignment marker removal ... 149
134.5.3.5 256B/257B to 64B/66B transcoder ... 150
134.5.3.6 Block distribution ... 150
134.5.3.7 Alignment marker mapping and insertion ... 150
134.5.3.8 Receive bit ordering ... 151
134.5.4 Detailed functions and state diagrams. ... 151
134.5.4.1 State diagram conventions ... 151
134.5.4.2 State variables ... 151
134.5.4.2.1 Variables ... 151
134.5.4.2.2 Functions ... 153
134.5.4.2.3 Counters ... 153
134.5.4.3 State diagrams ... 153
134.6 RS-FEC MDIO function mapping ... 153
134.6.1 FEC_bypass_indication_enable ... 153
134.6.2 FEC_bypass_indication_ability ... 153
134.6.3 hi_ser ... 154
134.6.4 amps_lock<*x*> ... 154
134.6.5 fec_align_status ... 155
134.6.6 FEC_corrected_cw_counter ... 155
134.6.7 FEC_uncorrected_cw_counter ... 155
134.6.8 FEC_lane_mapping<*x*> ... 155
134.6.9 FEC_symbol_error_counter_*i* ... 155
134.6.10 align_status ... 155
134.6.11 BIP_error_counter_*i* ... 155
134.6.12 lane_mapping<*x*> ... 155
134.6.13 block_lock<*x*> ... 156
134.6.14 am_lock<*x*> ... 156
134.7 Protocol implementation conformance statement (PICS) proforma for Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs ... 156
134.7.1 Introduction ... 156
134.7.2 Identification ... 156
134.7.2.1 Implementation identification ... 156

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000134

134.7.2.2 Protocol summary ... 157
134.7.3 Major capabilities/options ... 157
134.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs ... 157
134.7.4.1 Transmit function ... 157
134.7.4.2 Receive function ... 158
134.7.4.3 State diagrams ... 159
134.7.4.4 Delay Constraints ... 159

135. Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P ... 160

135.1 Overview ... 160
135.1.1 Scope ... 160
135.1.2 Position of the PMA in the 50GBASE-R and 100GBASE-P sublayers ... 160
135.1.3 Summary of functions ... 160
135.1.4 PMA sublayer positioning ... 161
135.2 PMA interfaces ... 163
135.3 PMA service interface ... 164
135.4 Service interface below PMA ... 165
135.5 Functions within the PMA ... 166
135.5.1 Per input-lane clock and data recovery ... 167
135.5.2 Bit-level multiplexing ... 168
135.5.3 Skew and Skew Variation ... 168
135.5.3.1 Skew generation toward SP0 ... 169
135.5.3.2 Skew tolerance at SP0 ... 169
135.5.3.3 Skew generation toward SP1 ... 169
135.5.3.4 Skew tolerance at SP1 ... 170
135.5.3.5 Skew generation toward SP2 ... 170
135.5.3.6 Skew tolerance at SP5 ... 170
135.5.3.7 Skew generation at SP6 ... 170
135.5.3.8 Skew tolerance at SP6 ... 170
135.5.3.9 Skew generation at SP7 ... 170
135.5.3.10 Skew tolerance at SP7 ... 170
135.5.4 Delay constraints ... 171
135.5.5 Clocking architecture ... 171
135.5.6 Signal drivers ... 171
135.5.7 PAM4 encoding ... 172
135.5.7.1 Gray coding for PAM4 encoded lanes ... 172
135.5.7.2 Precoding for PAM4 encoded lanes ... 172
135.5.8 PMA local loopback mode (optional) ... 172
135.5.9 PMA remote loopback mode (optional) ... 173
135.5.10 PMA test patterns (optional) ... 173
135.5.10.1 Test patterns for NRZ encoded signals ... 173
135.5.10.1.1 PRBS31 test pattern ... 173
135.5.10.1.2 PRBS9 test pattern ... 173
135.5.10.1.3 Square-wave test pattern ... 174
135.5.10.2 Test patterns for PAM4 encoded signals ... 174
135.5.10.2.1 PRBS13Q test pattern ... 174
135.5.10.2.2 PRBS31Q test pattern ... 174
135.5.10.2.3 SSPRQ test pattern ... 174
135.5.10.2.4 Square wave (quaternary) test pattern ... 174
135.6 PMA MDIO function mapping ... 174
135.7 Protocol implementation conformance statement (PICS) proforma for Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P ... 178

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000135

135.7.1 Introduction ... 178
135.7.2 Identification ... 178
135.7.2.1 Implementation identification ... 178
135.7.2.2 Protocol summary ... 178
135.7.3 Major capabilities/options ... 179
135.7.4 PICS proforma tables for Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P ... 179
135.7.4.1 Functions ... 179
135.7.4.2 Timing ... 180
135.7.4.3 Electrical ... 181
135.7.4.4 Diagnostics ... 181
135.7.7 Encoding ... 183

136. Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 ... 184

136.1 Overview ... 184
136.2 Conventions ... 186
136.3 PMD service interfaces ... 186
136.4 PCS requirements for Auto-Negotiation (AN) service interface ... 188
136.5 Delay constraints ... 188
136.6 Skew constraints ... 189
136.6.1 Skew Constraints for 50GBASE-CR ... 189
136.6.2 Skew Constraints for 100GBASE-CR2 and 200GBASE-CR4 ... 189
136.7 PMD MDIO function mapping ... 189
136.8 PMD functional specifications ... 192
136.8.1 Link block diagram ... 192
136.8.2 PMD transmit function ... 194
136.8.3 PMD receive function ... 194
136.8.4 PMD global signal detect function ... 194
136.8.5 PMD lane-by-lane signal detect function ... 194
136.8.6 PMD global transmit disable function (optional) ... 194
136.8.7 PMD lane-by-lane transmit disable function ... 195
136.8.8 PMD fault function ... 195
136.8.9 PMD transmit fault function (optional) ... 195
136.8.10 PMD receive fault function (optional) ... 195
136.8.11 PMD control function ... 195
136.8.11.1 Training frame structure ... 196
136.8.11.1.1 Frame marker ... 196
136.8.11.1.2 Control and status fields ... 196
136.8.11.1.3 Training pattern ... 197
136.8.11.1.4 Zero pad ... 198
136.8.11.2 Control field structure ... 199
136.8.11.2.1 Initial condition request ... 199
136.8.11.2.2 Modulation and precoding request ... 199
136.8.11.2.3 Coefficient select ... 199
136.8.11.2.4 Coefficient request ... 200
136.8.11.3 Status field structure ... 200
136.8.11.3.1 Receiver ready ... 200
136.8.11.3.2 Modulation and precoding status ... 201
136.8.11.3.3 Receiver frame lock ... 201
136.8.11.3.4 Initial condition status ... 201
136.8.11.3.5 Parity bit ... 201
136.8.11.3.6 Coefficient select echo ... 201

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000136

136.8.11.3.7 Coefficient status 201
136.8.11.4 Initial condition setting 201
136.8.11.5 Coefficient update 202
136.8.11.6 Handshake timing 203
136.8.11.7 Variables, functions, timers, counters, and state diagrams 204
136.8.11.7.1 Variables 204
136.8.11.7.2 Functions 205
136.8.11.7.3 Timers 206
136.8.11.7.4 Counters 206
136.8.11.7.5 State diagrams 206
136.9 Electrical characteristics 211
136.9.1 AC-coupling 211
136.9.2 Signal paths 211
136.9.3 Transmitter characteristics 211
136.9.3.1 Transmitter output waveform 212
136.9.3.1.1 Linear fit to the measured waveform 213
136.9.3.1.2 Steady-state voltage and linear fit pulse peak 214
136.9.3.1.3 Coefficient initialization 214
136.9.3.1.4 Coefficient step size 214
136.9.3.1.5 Coefficient range 215
136.9.4 Receiver characteristics 215
136.9.4.1 Receiver input amplitude tolerance 215
136.9.4.2 Receiver interference tolerance 216
136.9.4.2.1 Test setup 216
136.9.4.2.2 Test channel 216
136.9.4.2.3 Test channel calibration 216
136.9.4.2.4 Pattern generator and noise injection 217
136.9.4.2.5 Test procedure 218
136.9.4.3 Receiver jitter tolerance 218
136.9.4.3.1 Test setup 218
136.9.4.3.2 Test procedure 218
136.9.4.4 Signaling rate range 218
136.10 Channel characteristics 219
136.11 Cable assembly characteristics 219
136.11.1 Characteristic impedance and reference impedance 219
136.11.2 Cable assembly insertion loss 219
136.11.3 Cable assembly differential return loss 220
136.11.4 Differential to common-mode return loss 220
136.11.5 Differential to common-mode conversion loss 220
136.11.6 Common-mode to common-mode return loss 220
136.11.7 Cable assembly Channel Operating Margin 220
136.11.7.1 Channel signal and crosstalk path calculations 222
136.11.7.1.1 Channel signal path 222
136.11.7.1.2 Channel crosstalk paths 222
136.11.7.2 Signal and crosstalk paths used in calculation of COM 223
136.11.7.2.1 SFP28 to SFP28 223
136.11.7.2.2 QSFP28 to SFP28 224
136.11.7.2.3 SFP28 to QSFP28 224
136.11.7.2.4 QSFP28 to QSFP28 224
136.12 MDI specifications 224
136.13 Environmental specifications 225
136.14 Protocol implementation conformance statement (PICS) proforma for Clause 136, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 226

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000137

136.14.1 Introduction ... 226
136.14.2 Identification ... 226
136.14.2.1 Implementation identification ... 226
136.14.2.2 Protocol summary ... 226
136.14.3 Major capabilities/options ... 227
136.14.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 ... 228
136.14.4.1 PMD functional specifications ... 228
136.14.4.2 PMD control function ... 229
136.14.4.3 Transmitter specifications ... 229
136.14.4.4 Receiver specifications ... 230
136.14.4.5 Cable assembly specifications ... 230
136.14.4.6 MDI connector specifications ... 231
136.14.4.7 Environmental specifications ... 231

137. Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 ... 232

137.1 Overview ... 232
137.2 Conventions ... 234
137.3 PMD service interfaces ... 235
137.4 PCS requirements for Auto-Negotiation (AN) service interface ... 235
137.5 Delay constraints ... 235
137.6 Skew constraints ... 235
137.6.1 Skew Constraints for 50GBASE-KR ... 235
137.6.2 Skew Constraints for 100GBASE-KR2 and 200GBASE-KR4 ... 236
137.7 PMD MDIO function mapping ... 236
137.8 PMD functional specifications ... 236
137.8.1 Link block diagram ... 236
137.8.2 PMD transmit function ... 236
137.8.3 PMD receive function ... 236
137.8.4 PMD global signal detect function ... 237
137.8.5 PMD lane-by-lane signal detect function ... 237
137.8.6 PMD global transmit disable function (optional) ... 237
137.8.7 PMD lane-by-lane transmit disable function ... 237
137.8.8 PMD fault function ... 237
137.8.9 PMD transmit fault function (optional) ... 237
137.8.10 PMD receive fault function (optional) ... 237
137.8.11 PMD control function ... 237
137.9 Electrical characteristics ... 238
137.9.1 MDI ... 238
137.9.2 Transmitter characteristics ... 238
137.9.3 Receiver characteristics ... 238
137.9.3.1 Receiver input return loss ... 238
137.10 Channel characteristics ... 239
137.10.1 Channel Insertion loss ... 241
137.10.2 Channel return loss ... 241
137.11 Environmental specifications ... 242
137.12 Protocol implementation conformance statement (PICS) proforma for Clause 137, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 ... 243
137.12.1 Introduction ... 243
137.12.2 Identification ... 243
137.12.2.1 Implementation identification ... 243

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000138

137.12.2.2 Protocol summary ... 243
137.12.3 Major capabilities/options ... 243
137.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 ... 245
137.12.4.1 Functional specifications ... 245
137.12.4.2 PMD control function ... 246
137.12.4.3 Transmitter characteristics ... 246
137.12.4.4 Receiver characteristics ... 247
137.12.4.5 Channel characteristics ... 247
137.12.4.6 Environmental specifications ... 248

138. Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4 ... 249

138.1 Overview ... 249
138.1.1 Bit error ratio ... 251
138.2 Physical Medium Dependent (PMD) service interface ... 252
138.3 Delay and Skew ... 253
138.3.1 Delay constraints ... 253
138.3.2 Skew constraints ... 253
138.3.2.1 Skew Constraints for 50GBASE-SR ... 253
138.3.2.2 Skew Constraints for 100GBASE-SR2 and 200GBASE-SR4 ... 253
138.4 PMD MDIO function mapping ... 254
138.5 PMD functional specifications ... 254
138.5.1 PMD block diagram4 ... 254
138.5.2 PMD transmit function ... 256
138.5.3 PMD receive function ... 256
138.5.4 PMD global signal detect function ... 256
138.5.5 PMD lane-by-lane signal detect function ... 257
138.5.6 PMD reset function ... 257
138.5.7 PMD global transmit disable function (optional) ... 257
138.5.8 PMD lane-by-lane transmit disable function (optional) ... 257
138.5.9 PMD fault function (optional) ... 257
138.5.10 PMD transmit fault function (optional) ... 257
138.5.11 PMD receive fault function (optional) ... 258
138.6 Lane assignments ... 258
138.7 PMD to MDI optical specifications for 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 ... 258
138.7.1 Transmitter optical specifications ... 258
138.7.2 Receiver optical specifications ... 258
138.7.3 Illustrative link power budget ... 258
138.8 Definition of optical parameters and measurement methods ... 261
138.8.1 Test patterns for optical parameters ... 261
138.8.1.1 Multi-lane testing considerations ... 261
138.8.2 Center wavelength and spectral width ... 262
138.8.3 Average optical power ... 262
138.8.4 Outer Optical Modulation Amplitude (OMAouter) ... 262
138.8.5 Transmitter and dispersion eye closure - quaternary (TDECQ) ... 262
138.8.5.1 TDECQ reference equalizer ... 262
138.8.6 Extinction ratio ... 262
138.8.7 Receiver sensitivity ... 262
138.8.8 Stressed receiver sensitivity ... 263
138.8.8.1 Sinusoidal jitter for receiver conformance test ... 263
138.9 Safety, installation, environment, and labeling ... 263

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This is an unapproved IEEE Standards draft, subject to change.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000139

138.9.1 General safety 263
138.9.2 Laser safety 264
138.9.3 Installation 264
138.9.4 Environment 264
138.9.5 Electromagnetic emission 264
138.9.6 Temperature, humidity, and handling 264
138.9.7 PMD labeling requirements 264
138.10 Fiber optic cabling model 265
138.10.1 Fiber optic cabling model 265
138.10.2 Characteristics of the fiber optic cabling (channel) 266
138.10.2.1 Optical fiber cable 266
138.10.2.2 Optical fiber connection 266
138.10.2.2.1 Connection insertion loss 266
138.10.2.2.2 Maximum discrete reflectance 266
138.10.3 Medium Dependent Interface (MDI) 267
138.10.3.1 Optical lane assignments for 100GBASE-SR2 and 200GBASE-SR4 267
138.10.3.2 MDI requirements for 50GBASE-SR 267
138.10.3.3 MDI requirements for 100GBASE-SR2 and 200GBASE-SR4 268
138.11 Protocol implementation conformance statement (PICS) proforma for Clause 138, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4 269
138.11.1 Introduction 269
138.11.2 Identification 269
138.11.2.1 Implementation identification 269
138.11.2.2 Protocol summary 269
138.11.3 Major capabilities/options 270
138.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4 270
138.11.4.1 PMD functional specifications 270
138.11.4.2 Management functions 271
138.11.4.3 PMD to MDI optical specifications 272
138.11.4.4 Optical measurement methods 272
138.11.4.5 Environmental specifications 272
138.11.4.6 Characteristics of the fiber optic cabling and MDI 273

139. Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR 274

139.1 Overview 274
139.1.1 Bit error ratio 275
139.2 Physical Medium Dependent (PMD) service interface 275
139.3 Delay and Skew 276
139.3.1 Delay constraints 276
139.3.2 Skew constraints 276
139.4 PMD MDIO function mapping 277
139.5 PMD functional specifications 277
139.5.1 PMD block diagram 277
139.5.2 PMD transmit function 278
139.5.3 PMD receive function 278
139.5.4 PMD global signal detect function 278
139.5.5 PMD reset function 279
139.5.6 PMD global transmit disable function (optional) 279
139.5.7 PMD fault function (optional) 279
139.5.8 PMD transmit fault function (optional) 279

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This is an unapproved IEEE Standards draft, subject to change.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000140

139.5.9 PMD receive fault function (optional) ... 279
139.6 PMD to MDI optical specifications for 50GBASE-FR and 50GBASE-LR ... 280
139.6.1 50GBASE-FR and 50GBASE-LR transmitter optical specifications ... 280
139.6.2 50GBASE-FR and 50GBASE-LR receive optical specifications ... 281
139.6.3 50GBASE-FR and 50GBASE-LR illustrative link power budgets ... 282
139.7 Definition of optical parameters and measurement methods ... 282
139.7.1 Test patterns for optical parameters ... 282
139.7.2 Wavelength ... 283
139.7.3 Average optical power ... 283
139.7.4 Outer Optical Modulation Amplitude (OMAouter) ... 283
139.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ) ... 284
139.7.5.1 TDECQ conformance test setup ... 284
139.7.5.2 Channel requirements ... 284
139.7.5.3 TDECQ measurement method ... 285
139.7.5.4 TDECQ reference equalizer ... 285
139.7.6 Extinction ratio ... 286
139.7.7 Relative intensity noise ($RIN_{16.5}OMA$ and $RIN_{15.1}OMA$) ... 286
139.7.8 Receiver sensitivity ... 286
139.7.9 Stressed receiver sensitivity ... 286
139.7.9.1 Stressed receiver conformance test block diagram ... 286
139.7.9.2 Stressed receiver conformance test signal characteristics and calibration ... 287
139.7.9.3 Stressed receiver conformance test signal verification ... 288
139.8 Safety, installation, environment, and labeling ... 288
139.8.1 General safety ... 288
139.8.2 Laser safety ... 288
139.8.3 Installation ... 288
139.8.4 Environment ... 288
139.8.5 Electromagnetic emission ... 289
139.8.6 Temperature, humidity, and handling ... 289
139.8.7 PMD labeling requirements ... 289
139.9 Fiber optic cabling model ... 289
139.10 Characteristics of the fiber optic cabling (channel) ... 289
139.10.1 Optical fiber cable ... 290
139.10.2 Optical fiber connection ... 290
139.10.2.1 Connection insertion loss ... 290
139.10.2.2 Maximum discrete reflectance ... 291
139.10.3 Medium Dependent Interface (MDI) requirements ... 291
139.11 Protocol implementation conformance statement (PICS) proforma for Clause 139, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR ... 292
139.11.1 Introduction ... 292
139.11.2 Identification ... 292
139.11.2.1 Implementation identification ... 292
139.11.2.2 Protocol summary ... 292
139.11.3 Major capabilities/options ... 293
139.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR ... 293
139.11.4.1 PMD functional specifications ... 293
139.11.4.2 Management functions ... 294
139.11.4.3 PMD to MDI optical specifications for 50GBASE-FR ... 294
139.11.4.4 PMD to MDI optical specifications for 50GBASE-LR ... 295
139.11.4.5 Optical measurement methods ... 295
139.11.4.6 Environmental specifications ... 295
139.11.4.7 Characteristics of the fiber optic cabling and MD ... 296

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This is an unapproved IEEE Standards draft, subject to change.

Marvell Semiconductor, Inc. - Ex. 1002, Page 000141

140. Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR 297

140.1 Overview 297
140.1.1 Bit error ratio 298
140.2 Physical Medium Dependent (PMD) service interface 298
140.3 Delay and Skew 299
140.3.1 Delay constraints 299
140.3.2 Skew constraints 299
140.4 PMD MDIO function mapping 300
140.5 PMD functional specifications 300
140.5.1 PMD block diagram 300
140.5.2 PMD transmit function 301
140.5.3 PMD receive function 301
140.5.4 PMD global signal detect function 301
140.5.5 PMD reset function 302
140.5.6 PMD global transmit disable function (optional) 302
140.5.7 PMD fault function (optional) 302
140.5.8 PMD transmit fault function (optional) 302
140.5.9 PMD receive fault function (optional) 302
140.6 PMD to MDI optical specifications for 100GBASE-DR 303
140.6.1 100GBASE-DR transmitter optical specifications 303
140.6.2 100GBASE-DR receive optical specifications 304
140.6.3 100GBASE-DR illustrative link power budget 304
140.7 Definition of optical parameters and measurement methods 305
140.7.1 Test patterns for optical parameters 305
140.7.2 Wavelength 306
140.7.3 Average optical power 306
140.7.4 Outer Optical Modulation Amplitude (OMAouter) 306
140.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ) 306
140.7.6 Extinction ratio 306
140.7.7 Relative intensity noise (RIN21.4OMA) 307
140.7.8 Receiver sensitivity 307
140.7.9 Stressed receiver sensitivity 307
140.8 Safety, installation, environment, and labeling 307
140.8.1 General safety 307
140.8.2 Laser safety 307
140.8.3 Installation 307
140.8.4 Environment 308
140.8.5 Electromagnetic emission 308
140.8.6 Temperature, humidity, and handling 308
140.8.7 PMD labeling requirements 308
140.9 Fiber optic cabling model 308
140.10 Characteristics of the fiber optic cabling (channel) 309
140.10.1 Optical fiber cable 309
140.10.2 Optical fiber connection 309
140.10.2.1 Connection insertion loss 310
140.10.2.2 Maximum discrete reflectance 310
140.10.3 Medium Dependent Interface (MDI) 310
140.11 Protocol implementation conformance statement (PICS) proforma for Clause 140, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR 311
140.11.1 Introduction 311
140.11.2 Identification 311
140.11.2.1 Implementation identification 311
140.11.2.2 Protocol summary 311

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000142

140.11.3 Major capabilities/options ... 312
140.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR ... 312
140.11.4.1 PMD functional specifications ... 312
140.11.4.2 Management functions ... 313
140.11.4.3 PMD to MDI optical specifications for 100GBASE-DR ... 313
140.11.4.4 Optical measurement methods ... 314
140.11.4.5 Environmental specifications ... 314
140.11.4.6 Characteristics of the fiber optic cabling and MD ... 314

Annex 4A (normative) Simplified full duplex media access control ... 315

4A.4 Specific implementations ... 315
4A.4.2 MAC parameters ... 315

Annex 31B (normative) MAC Control PAUSE operation ... 316

31B.3 Detailed specification of PAUSE operation ... 316
31B.3.7 Timing considerations for PAUSE operation ... 316

Annex 93A (normative) Specification methods for electrical channels ... 317

93A.1 Channel Operating Margin ... 317
93A.1.4 Filters ... 318
93A.1.4.2 Transmitter equalizer ... 318
93A.1.6 Determination of variable equalizer parameters ... 319

Annex 135A (informative) 50 Gb/s and 100 Gb/s PMA sublayer partitioning examples ... 320

135A.1 Partitioning examples of 50GBASE-R PHYs ... 320
135A.2 Partitioning examples of 100GBASE-P PHYs ... 325

Annex 135B (normative) Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C) ... 326

135B.1 Overview ... 326
135B.2 LAUI-2 C2C compliance point definition ... 327
135B.3 LAUI-2 C2C electrical characteristics ... 327
135B.3.1 LAUI-2 C2C transmitter characteristics ... 327
135B.3.2 LAUI-2 C2C receiver characteristics ... 327
135B.4 LAUI-2 C2C channel characteristics ... 328
135B.5 Protocol implementation conformance statement (PICS) proforma for Annex 135B, Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C) ... 329
135B.5.1 Introduction ... 329
135B.5.2 Identification ... 329
135B.5.2.1 Implementation identification ... 329
135B.5.2.2 Protocol summary ... 329
135B.5.3 Major capabilities/options ... 330
135B.5.4 PICS proforma tables for Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C) ... 330
135B.5.4.1 Transmitter ... 330
135B.5.4.2 Receiver ... 331
135B.5.4.3 Channel ... 331

Annex 135C (normative) Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2M) ... 332

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000143

135C.1 Overview ... 332
135C.1.1 Bit error ratio ... 333
135C.2 LAUI-2 C2M compliance point definitions ... 333
135C.3 LAUI-2 C2M electrical characteristics ... 333
135C.3.1 LAUI-2 C2M host output characteristics ... 333
135C.3.2 LAUI-2 C2M module output characteristics ... 333
135C.3.3 LAUI-2 C2M host input characteristics ... 333
135C.3.4 LAUI-2 C2M module input characteristics ... 333
135C.4 LAUI-2 C2M measurement methodology ... 334
135C.5 Protocol implementation conformance statement (PICS) proforma for Annex 135C, Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2M) ... 335
135C.5.1 Introduction ... 335
135C.5.2 Identification ... 335
135C.5.2.1 Implementation identification ... 335
135C.5.2.2 Protocol summary ... 335
135C.5.3 Major capabilities/options ... 336
135C.5.4 PICS proforma tables for Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2M) ... 336
135C.5.4.1 Host output ... 336
135C.5.4.2 Module output ... 337
135C.5.4.3 Host input ... 337
135C.5.4.4 Module input ... 337

Annex 135D (normative) Chip-to-chip 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2C) ... 338

135D.1 Overview ... 338
135D.2 50GAUI-2 C2C and 100GAUI-4 C2C compliance point definition ... 340
135D.3 50GAUI-2 C2C and 100GAUI-4 C2C electrical characteristics ... 340
135D.3.1 50GAUI-2 C2C and 100GAUI-4 C2C transmitter characteristics ... 340
135D.3.2 50GAUI-2 C2C and 100GAUI-4 C2C receiver characteristics ... 340
135D.4 50GAUI-2 C2C and 100GAUI-4 C2C channel characteristics ... 340
135D.5 Protocol implementation conformance statement (PICS) proforma for Annex 135D, Chip-to-chip 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2C) ... 341
135D.5.1 Introduction ... 341
135D.5.2 Identification ... 341
135D.5.2.1 Implementation identification ... 341
135D.5.2.2 Protocol summary ... 341
135D.5.3 Major capabilities/options ... 342
135D.5.4 PICS proforma tables for Chip-to-chip 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2C) ... 342
135D.5.4.1 Transmitter ... 342
135D.5.4.2 Receiver ... 343
135D.5.4.3 Channel ... 343

Annex 135E (normative) Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2M) ... 344

135E.1 Overview ... 344
135E.1.1 Bit error ratio ... 345
135E.2 50GAUI-2 C2M and 100GAUI-4 C2M compliance point definitions ... 346
135E.3 50GAUI-2 C2M and 100GAUI-4 C2M electrical characteristics ... 346
135E.3.1 50GAUI-2 C2M and 100GAUI-4 C2M host output characteristics ... 346

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000144

135E.3.2 50GAUI-2 C2M and 100GAUI-4 C2M module output characteristics 346
135E.3.3 50GAUI-2 C2M and 100GAUI-4 C2M host input characteristics 346
135E.3.4 50GAUI-2 C2M and 100GAUI-4 C2M module input characteristics 346
135E.4 50GAUI-2 C2M and 100GAUI-4 C2M measurement methodology 346
135E.5 Protocol implementation conformance statement (PICS) proforma for Annex 135E, Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2M) 347
135E.5.1 Introduction 347
135E.5.2 Identification 347
135E.5.2.1 Implementation identification 347
135E.5.2.2 Protocol summary 347
135E.5.3 Major capabilities/options 348
135E.5.4 PICS proforma tables for Annex 135E, Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2M) 348
135E.5.4.1 Host output 348
135E.5.4.2 Module output 349
135E.5.4.3 Host input 350
135E.5.4.4 Module input 350

Annex 135F (normative) Chip-to-chip 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2C) 351

135F.1 Overview 351
135F.2 50GAUI-1 C2C and 100GAUI-2 C2C compliance point definition 353
135F.3 50GAUI-1 C2C and 100GAUI-2 C2C electrical characteristics 353
135F.3.1 50GAUI-1 C2C and 100GAUI-2 C2C transmitter characteristics 353
135F.3.2 50GAUI-1 C2C and 100GAUI-2 C2C receiver characteristics 353
135F.3.2.1 Transmitter precoder request (optional) 353
135F.4 50GAUI-1 C2C and 100GAUI-2 C2C channel characteristics 353
135F.5 Protocol implementation conformance statement (PICS) proforma for Annex 135F, Chip-to-chip 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2C) 354
135F.5.1 Introduction 354
135F.5.2 Identification 354
135F.5.2.1 Implementation identification 354
135F.5.2.2 Protocol summary 354
135F.5.3 Major capabilities/options 355
135F.5.4 PICS proforma tables for Chip-to-chip 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2C) 355
135F.5.4.1 Transmitter 355
135F.5.4.2 Receiver 356
135F.5.4.3 Channel 356

Annex 135G (normative) Chip-to-module 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2M) 357

135G.1 Overview 357
135G.1.1 Bit error ratio 358
135G.2 50GAUI-1 C2M and 100GAUI-2 C2M compliance point definitions 359
135G.3 50GAUI-1 C2M and 100GAUI-2 C2M electrical characteristics 359
135G.3.1 50GAUI-1 C2M and 100GAUI-2 C2M host output characteristics 359
135G.3.2 50GAUI-1 C2M and 100GAUI-2 C2M module output characteristics 359
135G.3.3 50GAUI-1 C2M and 100GAUI-2 C2M host input characteristics 359

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000145

135G.3.4 50GAUI-1 C2M and 100GAUI-2 C2M module input characteristics 359
135G.4 50GAUI-1 C2M and 100GAUI-2 C2M measurement methodology 359
135G.5 Protocol implementation conformance statement (PICS) proforma for Annex 135G, Chip-to-module 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2M) 360
135G.5.1 Introduction 360
135G.5.2 Identification 360
135G.5.2.1 Implementation identification 360
135G.5.2.2 Protocol summary 360
135G.5.3 Major capabilities/options 361
135G.5.4 PICS proforma tables for Chip-to-module 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2M) 361
135G.5.4.1 Host output 361
135G.5.4.2 Module output 362
135G.5.4.3 Host input 362
135G.5.4.4 Module input 362

Annex 136A (normative) TP0 and TP5 test point parameters and channel characteristics for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 363

136A.1 Overview 363
136A.2 Transmitter characteristics at TP0 363
136A.3 Receiver characteristics at TP5 363
136A.4 Transmitter and receiver differential printed circuit board trace loss 363
136A.5 Channel insertion loss 363
136A.6 Channel return loss 366
136A.7 Channel Operating Margin (COM) 366

Annex 136B (normative) Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M 367

136B.1 Test fixtures 367
136B.1.1 Mated test fixtures 367
136B.1.1.1 Mated test fixtures differential insertion loss 367
136B.1.1.2 Mated test fixtures differential return loss 367
136B.1.1.3 Mated test fixtures common-mode conversion insertion loss 367
136B.1.1.4 Mated test fixtures common-mode return loss 368
136B.1.1.5 Mated test fixtures common-mode to differential mode return loss 368
136B.1.1.6 Mated test fixtures integrated crosstalk noise 368
136B.2 Protocol implementation conformance statement (PICS) proforma for Annex 136B, Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M 369
136B.2.1 Introduction 369
136B.2.2 Identification 369
136B.2.2.1 Implementation identification 369
136B.2.2.2 Protocol summary 369
136B.2.3 Major capabilities/options 370
136B.2.4 PICS proforma tables for test fixtures for Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M 370

Annex 136C (normative) Host and cable assembly form factors for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 371

136C.1 Overview 371

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000146

136C.2 Host form factors 371
136C.2.1 SFP28 host form factor 371
136C.2.2 QSFP28 host form factor 372
136C.3 Cable assembly form factors 372
136C.3.1 SFP28 to SFP28 cable assembly form factor 372
136C.3.2 QSFP28 to QSFP28 cable assembly form factor 373
136C.3.3 QSFP28 to 4×SFP28 cable assembly form factor 373

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Draft Standard for Ethernet Amendment: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation

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NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

TO BE REMOVED PRIOR TO FINAL PUBLICATION: Reviewers and the publication editor should note that editing instructions have been written to minimize the probability of changes being lost at publication from other IEEE 802.3 amendment projects running in parallel (e.g., IEEE P802.3bj and IEEE P802.3bk) that modified the same text and tables.

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1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Insert the following new compatibility interfaces after "k) 40 Gb/s Parallel Physical Interface (XLPPI)":

k1) *50 Gb/s Media Independent Interface (50GMII).* The 50GMII is designed to connect a 50 Gb/s capable MAC to a 50 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The 50GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 50GMII. The 50GMII is optional.

k2) *50 Gb/s Attachment Unit Interface (LAUI-2/50GAUI-n).* The LAUI-2/50GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The LAUI-2/50GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of 50GAUI-n are defined: a two-lane version (50GAUI-2) in Annex 135D and Annex 135E, and a one-lane version (50GAUI-1) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the LAUI-2/50GAUI-n. The LAUI-2/50GAUI-n is optional.

Change the compatibility interface "m) 100 Gb/s Attachment Unit Interface (CAUI-n)" as follows:

m) *100 Gb/s Attachment Unit Interface (CAUI-n/100GAUI-n).* The CAUI-n/100GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 100 Gb/s speeds. The CAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Three~~Two~~ widths of CAUI-n are defined: a ten-lane version (CAUI-10) in Annex 83A and Annex 83B, ~~and~~ a four-lane version (CAUI-4/100GAUI-4) in Annex 83D ~~and~~, Annex 83E, Annex 135D, and Annex 135E, and a two-lane version (100GAUI-2) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the CAUI-n/100GAUI-n. The CAUI-n/100GAUI-n is optional.

1.3 Normative references

Change the reference for IEC 61753-022-2 as follows:

IEC 61753-022-2:2012, Fibre optic interconnecting devices and passive components - Performance standard - Part 022-2: Fibre optic connectors terminated on multimode fibre for category C - Controlled environment~~, performance Class M~~.

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1.4 Definitions

Insert the following new definition after 1.4.52 "100GBASE-R encoding":

1.4.52a 100GBASE-CR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

Insert the following new definition after 1.4.54 "100GBASE-CR10":

1.4.54a 100GBASE-DR: IEEE 802.3 Physical Layer specification for 100 Gb/s serial transmission using 100GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 140.)

Insert the following new definition after 1.4.55 "100GBASE-KP4":

1.4.55a 100GBASE-KR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

Insert the following new definition after 1.4.58 "100GBASE-LR4":

1.4.58a 100GBASE-SR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of multimode fiber. (See IEEE Std 802.3, Clause 138.)

Insert the following new definitions after 1.4.72a "40GBASE-T" (as inserted by IEEE Std 802.3bq-2016):

1.4.72a1 50GBASE-CR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

1.4.72a2 50GBASE-FR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 139.)

1.4.72a3 50GBASE-KR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

1.4.72a4 50GBASE-LR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 139.)

1.4.72a5 50GBASE-R: An IEEE 802.3 physical coding sublayer for one-lane 50 Gb/s operation. (See IEEE Std 802.3, Clause 131.)

1.4.72a6 50GBASE-SR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over multimode fiber. (See IEEE Std 802.3, Clause 138.)

1.4.72a7 50 Gb/s Attachment Unit Interface (50GAUI-n, LAUI-2): A physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs over one lane (50GAUI-1) or two lanes (50GAUI-2, LAUI-2), used for chip-to-chip or chip-to-module interconnections. (See IEEE Std 802.3, Clause 135 and Annex 135B through Annex 135G.)

1.4.72a8 50 Gb/s Media Independent Interface (50GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 50 Gb/s operation. (See IEEE Std 802.3, Clause 132)

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1.4.72a9 200GBASE-CR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136)

Insert the following new definition after 1.4.72c "200GBASE-FR4" (as inserted by IEEE Std 802.3bs-201x):

1.4.72c1 200GBASE-KR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

Insert the following new definition after 1.4.72e "200GBASE-R" (as inserted by IEEE Std 802.3bs-201x):

1.4.72e1 200GBASE-SR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of multimode fiber. (See IEEE Std 802.3, Clause 138.)

Modify 1.4.81 as follows:

1.4.81 100 Gb/s Attachment Unit Interface (CAUI-n, 100GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. Three~~Two~~ widths of CAUI-n are defined: a ten-lane version (CAUI-10), ~~and~~ two four-lane versions (CAUI-4, 100GAUI-4), and a two-lane version (100GAUI-2). (See IEEE Std 802.3, Annex 83A and Annex 83B for CAUI-10, ~~or~~ Annex 83D and Annex 83E for CAUI-4, Clause 135, Annex 135D, and Annex 135E for 100GAUI-4, or Clause 135, Annex 135F, and Annex 135G for 100GAUI-2.)

Insert the following new definition after 1.4.203 "fast wake":

1.4.203a FEC lane (FECL): In 50GBASE-R and 100GBASE-R the FEC distributes encoded data to multiple logical lanes, these logical lanes are called FEC lanes. One or more FEC lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 135.)

Modify 1.4.325 (as modified by IEEE Std 802.3bs-201x) as follows:

1.4.325 PCS lane (PCSL): In 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R, the PCS distributes encoded data to multiple logical lanes, these logical lanes are called PCS lanes. One or more PCS lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 83~~ and~~, Clause 120, and Clause 135.)

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

100GAUI	100 Gb/s Attachment Unit Interface
50GAUI	50 Gb/s Attachment Unit Interface
50GMII	50 Gb/s Media Independent Interface
FECL	FEC Lane
LAUI	50 Gb/s Attachment Unit Interface

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4. Media Access Control

4.4 Specific implementations

4.4.2 MAC parameters

Change Table 4–2 (as modified by IEEE Std 802.3by-2016, IEEE Std 802.3bz-2016 and IEEE Std 802.3bs-201x) as follows:

Table 4–2—MAC parameters

Parameters	MAC data rate			
	Up to and including 100 Mb/s	**1 Gb/s**	**2.5 Gb/s, 5 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s**	**10 Gb/s**
slotTime	512 bit times	4096 bit times	not applicable	not applicable
interPacketGap[a]	96 bits	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable	not applicable
backoffLimit	10	10	not applicable	not applicable
jamSize	32 bits	32 bits	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	1518 octets	1518 octets
maxEnvelopeFrameSize	2000 octets	2000 octets	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	not applicable	104 bits

[a]References to interFrameGap or interFrameSpacing in other clauses (e.g., 13, 35, and 42) shall be interpreted as interPacketGap.

Change Note 7 below Table 4–2 (as modified by IEEE Std 802.3bs-201x) as follows:

NOTE 7—For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, 50GMII, CGMII, 200GMII, or 400GMII receive signals at the DTE due to clock tolerance and lane alignment requirements.

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30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry in "APPROPRIATE SYNTAX" after the entry for 40GBASE-R:

APPROPRIATE SYNTAX:

...

50GBASE-R	Clause 133 50 Gb/s multi-PCS lane 64B/66B

30.3.2.1.3 aPhyTypeList

Insert the following new entry in "APPROPRIATE SYNTAX" after the entry for 40GBASE-R:

APPROPRIATE SYNTAX:

...

50GBASE-R	Clause 133 50 Gb/s multi-PCS lane 64B/66B

30.3.2.1.5 aSymbolErrorDuringCarrier

Change the fourth paragraph in the "BEHAVIOUR DEFINED AS" section of 30.3.2.1.5 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

> For operation at 10 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, it is a count of the number of times the receiving media is non-idle (the time between the Start of Packet Delimiter and the End of Packet Delimiter as defined by 46.2.5 and 81.2.5) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate "Receive Error" on the (see Table 46–4 and Table 81–3).

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entries in "APPROPRIATE SYNTAX" section of 30.5.1.1.2 (as modified by IEEE Std 802.3bs-201x) with the 50G entries going after 40GBASE-FR, the 100G entries going after 100GBASE-ER4 and the 200G entries going after 200GBASE-LR4:

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APPROPRIATE SYNTAX:

...

50GBASE-R	Multi-lane PCS as specified in Clause 133 with PMA as specified in Clause 135 over undefined PMD
50GBASE-CR	50GBASE-R PCS/PMA over shielded copper balanced cable PMD as specified in Clause 136
50GBASE-KR	50GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
50GBASE-SR	50GBASE-R PCS/PMA over multimode fiber PMD as specified in Clause 138
50GBASE-FR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139
50GBASE-LR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139
...	
100GBASE-CR2	100GBASE-R PCS/PMA over 2-lane shielded copper balanced cable PMD as specified in Clause 136
100GBASE-KR2	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
100GBASE-SR2	100GBASE-R PCS/PMA over 2-lane multimode fiber PMD as specified in Clause 138
100GBASE-DR	100GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 140
...	
200GBASE-CR4	100GBASE-R PCS/PMA over 4-lane shielded copper balanced cable PMD as specified in Clause 136
200GBASE-KR4	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
200GBASE-SR4	100GBASE-R PCS/PMA over 4-lane multimode fiber PMD as specified in Clause 138
...	

Change the last paragraph of the "BEHAVIOUR DEFINED AS" section of 30.5.1.1.2 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

The enumerations 1000BASE-X, 1000BASE-XHD, 1000BASE-XFD, 10GBASE-X, 10GBASE-R, 10GBASE-W, 25GBASE-R, 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R shall only be returned if the underlying PMD type is unknown.;

30.5.1.1.4 aMediaAvailable

Change the sixth paragraph of the "BEHAVIOUR DEFINED AS" section of 30.5.1.1.4 (as modified by IEEE Std 802.3bq-2016 and IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, the enumerations map to value of the link_fault variable within the Link Fault Signaling state diagram (see 81.3.4.1 and Figure 46–11) as follows: the values OK and Link Interruption map to the enumeration "available", the value

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Local Fault maps to the enumeration "not available" and the value Remote Fault maps to the enumeration "remote fault".

30.5.1.1.11 aBIPErrorCount

Change "APPROPRIATE SYNTAX" and first sentence of "BEHAVIOUR DEFINED AS" of 30.5.1.1.11 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 10 000 counts per second for 40 Gb/s and 50 Gb/s implementations and 5 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 40/50/100GBASE-R PHYs and 100GBASE-P PHYS, an array of BIP error counters.

30.5.1.1.12 aLaneMapping

Change the first sentence of "BEHAVIOUR DEFINED AS" of 30.5.1.1.12 (as modified by IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

For 40/50/100/200/400GBASE-R PHYs and 100GBASE-P PHYs, an array of PCS lane identifiers.

30.5.1.1.15 aFECAbility

Change the first sentence of "BEHAVIOUR DEFINED AS" of 30.5.1.1.15 (as modified by IEEE Std 802.3by-2016) as follows:

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an FEC sublayer for forward error correction (see 65.2, Clause 74, Clause 91, ~~and~~ Clause 108, and Clause 134).

30.5.1.1.17 aFECCorrectedBlocks

Change "APPROPRIATE SYNTAX" of 30.5.1.1.17 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

Change the first sentence of the "BEHAVIOUR DEFINED AS" of 30.5.1.1.17 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

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For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of corrected FEC block counters.

30.5.1.1.18 aFECUncorrectableBlocks

Change "APPROPRIATE SYNTAX" of 30.5.1.1.18 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

Change the first sentence of the "BEHAVIOUR DEFINED AS" of 30.5.1.1.18 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of uncorrectable FEC block counters.

30.5.1.1.26 aRSFECBIPErrorCount

Change "APPROPRIATE SYNTAX" and first sentence of "BEHAVIOUR DEFINED AS" of 30.5.1.1.26 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 5 000 counts per second for 50 Gb/s and 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R, and 100GBASE-P PHYs, an array of BIP error counters.

30.5.1.1.27 aRSFECLaneMapping

Change the first sentence of "BEHAVIOUR DEFINED AS" of 30.5.1.1.27 as follows:

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R, and 100GBASE-P PHYs, an array of PCS lane identifiers.

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30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entries in "APPROPRIATE SYNTAX" section of 30.6.1.1.5 with the 50GR entry going after 40GBASE-CR4, and the 100GR2 and 200GR4 entries going after 100GBASE-KP4 as follows:

APPROPRIATE SYNTAX:

50GR	50GBASE-CR as specified in Clause 136 or 50GBASE-KR as specified in Clause 137
100GR2	100GBASE-CR2 as specified in Clause 136 or 100GBASE-KR2 as specified in Clause 137
200GR4	200GBASE-CR4 as specified in Clause 136 or 200GBASE-KR4 as specified in Clause 137

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45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change Table 45–3 (as modified by IEEE Std 802.3bz-2016 and IEEE Std 802.3bs-201x) as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.20	~~Reserved~~ 50G PMA/PMD extended ability	45.2.1.14b1
…		
1.25, ~~1.26~~	~~Reserved~~ PMA/PMD extended ability 2	45.2.1.14f1
1.26	Reserved	
…		
1.500 through 1.515	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 through lane 15	45.2.1.116d, 45.2.1.116e
1.516 through 1.531	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 through lane 15	45.2.1.116f, 45.2.1.116g
…		
~~1.532 through 1.699~~ 1.532 through 1.599	Reserved	
1.600	PMA precoder control down Tx	45.2.1.116h
1.601	PMA precoder control down Rx	45.2.1.116i
1.602	PMA precoder control up Tx	45.2.1.116j
1.603	PMA precoder control up Rx	45.2.1.116k
1.604	PMA precoder request status	45.2.1.116l
1.605	PMA precoder request down	45.2.1.116m
1.606	PMA precoder request up	45.2.1.116n
1.607 through 1.699	Reserved	
…		
1.1110 through 1.1119	Reserved	
1.1120 through 1.1123	BASE-R PAM4 PMD training LP control registers, lanes 0 through 3	45.2.1.118a
~~1.1110 through 1.1199~~ 1.1124 through 1.1199	Reserved	

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Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
…		
1.1210 through 1.1219	Reserved	
1.1220 through 1.1223	BASE-R PAM4 PMD training LP status registers, lanes 0 through 3	45.2.1.119a
~~1.1210 through 1.1299~~ 1.1224 through 1.1299	Reserved	
…		
1.1310 through 1.1319	Reserved	
1.1320 through 1.1323	BASE-R PAM4 PMD training LD control registers, lanes 0 through 3	45.2.1.120a
~~1.1310 through 1.1399~~ 1.1324 through 1.1399	Reserved	
…		
1.1410 through 1.1419	Reserved	
1.1420 through 1.1423	BASE-R PAM4 PMD training LD status registers, lanes 0 through 3	45.2.1.121a
~~1.1410 through 1.1449~~ 1.1424 through 1.1449	Reserved	
…		

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change the row for bits 1.0.5:2 in Table 45–4 (as modified by IEEE Std 802.3by-2016, IEEE Std 802.3bz-2016, and IEEE Std 802.3bs-201x) as follows (unchanged rows not shown):

45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Change the last paragraph of 45.2.1.1.3 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

When bits 5 through 2 are set to 0010 the use of a 40G PMA/PMD is selected; when set to 0011 the use of a 100G PMA/PMD is selected; when set to 0100 the use of a 25G PMA/PMD is selected; when set to 0101 the use of a 50G PMA/PMD is selected; when set to 1000 the use of a 200G PMA/PMD is selected; when set to 1001 the use of a 400G PMA/PMD is selected. More specific selection is performed using the PMA/PMD control 2 register (Register 1.7) (see 45.2.1.6.3).

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Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 400 Gb/s 1 0 0 0 = 200 Gb/s 0 1 1 1 = 5 Gb/s 0 1 1 0 = 2.5 Gb/s 0 1 0 1 = ~~Reserved~~ 50 Gb/s 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
…			

[a]R/W = Read/Write, SC = Self-clearing, RO = Read only

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

45.2.1.2.3 Fault (1.1.7)

Change the fourth sentence of 45.2.1.2.3 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

For 10/25/40/50/100/200/400 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one.

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45.2.1.4 PMA/PMD speed ability (Register 1.4)

Change the row for 1.4.3 in Table 45–6 (as modified by IEEE Std 802.3bn-2016, IEEE Std 802.3bz-2016 and IEEE Std 802.3bs-201x) as follows (unchanged rows not shown):

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.4.3	~~Reserved~~ 50G capable	~~Value always 0~~ 1 = PMA/PMD is capable of operating at 50 Gb/s 0 = PMA/PMD is not capable of operating at 50 Gb/s	RO
…			

[a]RO = Read only

Insert 45.2.1.4.6a after 45.2.1.4.6 as follows:

45.2.1.4.6a 50G capable (1.4.3)

When read as a one, bit 1.4.3 indicates that the PMA/PMD is able to operate at a data rate of 50 Gb/s. When read as a zero, bit 1.4.3 indicates that the PMA/PMD is not able to operate at a data rate of 50 Gb/s.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45–7 (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, IEEE Std 802.3bp-2016, IEEE Std 802.3bn-201x, IEEE Std 802.3bv-2016, IEEE Std 802.3bz-2016, IEEE Std 802.3bs-201x, IEEE Std 802.3cb-201x, and IEEE Std 802.3cc-201x) as follows:

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:10	Reserved	Value always 0	RO
1.7.9	PIASE	PMA ingress AUI stop enable	R/W
1.7.8	PEASE	PMA egress AUI stop enable	R/W
1.7.7	Reserved	Value always 0	RO

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Table 45–7—PMA/PMD control 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.7.6:0	PMA/PMD type selection	6 5 4 3 2 1 0 1 1 x x x x x = reserved 1 0 1 1 1 1 x = reserved 1 0 1 1 1 0 1 = reserved 1 0 1 1 1 0 0 = 400GBASE-LR8 PMA/PMD 1 0 1 1 0 1 1 = 400GBASE-FR8 PMA/PMD 1 0 1 1 0 1 0 = 400GBASE-DR4 PMA/PMD 1 0 1 1 0 0 1 = 400GBASE-SR16 PMA/PMD 1 0 1 1 0 0 0 = reserved 1 0 1 0 1 1 x = reserved 1 0 1 0 1 0 1 = 200GBASE-LR4 PMA/PMD 1 0 1 0 1 0 0 = 200GBASE-FR4 PMA/PMD 1 0 1 0 0 1 1 = 200GBASE-DR4 PMA/PMD 1 0 1 0 0 1 0 = 200GBASE-SR4 PMA/PMD ~~reserved~~ 1 0 1 0 0 0 1 = 200GBASE-CR4 PMA/PMD 1 0 1 0 0 0 0 = 200GBASE-KR4 PMA/PMD ~~1 0 1 0 0 0 x = reserved~~ ~~1 0 0 x x x x = reserved~~ 1 0 0 1 1 x x = reserved 1 0 0 1 0 1 1 = 100GBASE-DR PMA/PMD 1 0 0 1 0 1 0 = 100GBASE-SR2 PMA/PMD 1 0 0 1 0 0 1 = 100GBASE-CR2 PMA/PMD 1 0 0 1 0 0 0 = 100GBASE-KR2 PMA/PMD 1 0 0 0 1 1 x = reserved 1 0 0 0 1 0 1 = reserved 1 0 0 0 1 0 0 = 50GBASE-LR PMA/PMD 1 0 0 0 0 1 1 = 50GBASE-FR PMA/PMD 1 0 0 0 0 1 0 = 50GBASE-SR PMA/PMD 1 0 0 0 0 0 1 = 50GBASE-CR PMA/PMD 1 0 0 0 0 0 0 = 50GBASE-KR PMA/PMD 0 1 1 1 1 1 x = reserved 0 1 1 1 1 0 1 = BASE-T1 PMA/PMD[b] 0 1 1 1 1 0 0 = 5GBASE-KR PMA/PMD 0 1 1 1 0 1 1 = 2.5GBASE-KX PMA/PMD 0 1 1 1 0 1 0 = 25GBASE-SR PMA/PMD 0 1 1 1 0 0 1 = 25GBASE-KR or 25GBASE-KR-S PMA/PMD 0 1 1 1 0 0 0 = 25GBASE-CR or 25GBASE-CR-S PMA/PMD 0 1 1 0 1 1 1 = 25GBASE-T PMA 0 1 1 0 1 1 0 = 25GBASE-ER PMA/PMD 0 1 1 0 1 0 1 = 25GBASE-LR PMA/PMD 0 1 1 0 1 0 0 = BASE-H PMA/PMD[c] 0 1 1 0 0 1 1 = 10GPASS-XR-U PMA/PMD 0 1 1 0 0 1 0 = 10GPASS-XR-D PMA/PMD 0 1 1 0 0 0 1 = 5GBASE-T PMA 0 1 1 0 0 0 0 = 2.5GBASE-T PMA 0 1 0 1 1 1 1 = 100GBASE-SR4 PMA/PMD 0 1 0 1 1 1 0 = 100GBASE-CR4 PMA/PMD 0 1 0 1 1 0 1 = 100GBASE-KR4 PMA/PMD 0 1 0 1 1 0 0 = 100GBASE-KP4 PMA/PMD 0 1 0 1 0 1 1 = 100GBASE-ER4 PMA/PMD 0 1 0 1 0 1 0 = 100GBASE-LR4 PMA/PMD 0 1 0 1 0 0 1 = 100GBASE-SR10 PMA/PMD 0 1 0 1 0 0 0 = 100GBASE-CR10 PMA/PMD 0 1 0 0 1 1 1 = reserved	R/W

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Table 45–7—PMA/PMD control 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.7.6:0 *(continued)*	PMA/PMD type selection *(continued)*	0 1 0 0 1 1 0 = 40GBASE-T PMA 0 1 0 0 1 0 1 = 40GBASE-ER4 PMA/PMD 0 1 0 0 1 0 0 = 40GBASE-FR PMA/PMD 0 1 0 0 0 1 1 = 40GBASE-LR4 PMA/PMD 0 1 0 0 0 1 0 = 40GBASE-SR4 PMA/PMD 0 1 0 0 0 0 1 = 40GBASE-CR4 PMA/PMD 0 1 0 0 0 0 0 = 40GBASE-KR4 PMA/PMD 0 0 1 1 1 1 1 = 10/1GBASE-PRX-U4 0 0 1 1 1 1 0 = 10GBASE-PR-U4 0 0 1 1 1 0 1 = 10/1GBASE-PRX-D4 0 0 1 1 1 0 0 = 10GBASE-PR-D4 0 0 1 1 0 1 1 = reserved 0 0 1 1 0 1 0 = 10GBASE-PR-U3 0 0 1 1 0 0 1 = 10GBASE-PR-U1 0 0 1 1 0 0 0 = 10/1GBASE-PRX-U3 0 0 1 0 1 1 1 = 10/1GBASE-PRX-U2 0 0 1 0 1 1 0 = 10/1GBASE-PRX-U1 0 0 1 0 1 0 1 = 10GBASE-PR-D3 0 0 1 0 1 0 0 = 10GBASE-PR-D2 0 0 1 0 0 1 1 = 10GBASE-PR-D1 0 0 1 0 0 1 0 = 10/1GBASE-PRX-D3 0 0 1 0 0 0 1 = 10/1GBASE-PRX-D2 0 0 1 0 0 0 0 = 10/1GBASE-PRX-D1 0 0 0 1 1 1 1 = 10BASE-T PMA/PMD 0 0 0 1 1 1 0 = 100BASE-TX PMA/PMD 0 0 0 1 1 0 1 = 1000BASE-KX PMA/PMD 0 0 0 1 1 0 0 = 1000BASE-T PMA/PMD 0 0 0 1 0 1 1 = 10GBASE-KR PMA/PMD 0 0 0 1 0 1 0 = 10GBASE-KX4 PMA/PMD 0 0 0 1 0 0 1 = 10GBASE-T PMA 0 0 0 1 0 0 0 = 10GBASE-LRM PMA/PMD 0 0 0 0 1 1 1 = 10GBASE-SR PMA/PMD 0 0 0 0 1 1 0 = 10GBASE-LR PMA/PMD 0 0 0 0 1 0 1 = 10GBASE-ER PMA/PMD 0 0 0 0 1 0 0 = 10GBASE-LX4 PMA/PMD 0 0 0 0 0 1 1 = 10GBASE-SW PMA/PMD 0 0 0 0 0 1 0 = 10GBASE-LW PMA/PMD 0 0 0 0 0 0 1 = 10GBASE-EW PMA/PMD 0 0 0 0 0 0 0 = 10GBASE-CX4 PMA/PMD	

[a]R/W = Read/Write, RO = Read only
[b]If BASE-T1 is selected, bits 1.2100.3:0 are used to differentiate which BASE-T1 PMA/PMD is selected.
[c]If BASE-H PMA/PMD is selected, register 1.900 is used to differentiate which BASE-H PMA/PMD is selected

Change 45.2.1.6.3 (as modified by IEEE Std 802.3bs-201x) as follows:

45.2.1.6.3 PMA/PMD type selection (1.7.6:0)

The PMA/PMD type of the PMA/PMD shall be selected using bits 6 to 0. The PMA/PMD type abilities of the PMA/PMD are advertised in bits 9 and 7 through 0 of the PMA/PMD status 2 register; the PMA/PMD extended ability register; the 40G/100G PMA/PMD extended ability register; the 50G PMA/PMD extended ability register; the 200G PMA/PMD extended ability register, and the 400G PMA/PMD extended ability register. A PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types

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it has not advertised. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert the following rows after the row for 40GBASE-T (which was inserted by IEEE Std 802.3bq-2016) with the exception of the 100GBASE-DR row which goes after the 100GBASE-SR4 PMD in Table 45–9 as follows (unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
…	
50GBASE-KR, 100GBASE-KR2, 200GBASE-KR4	137.8.9
50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4	136.8.9
50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4	138.5.10
50GBASE-FR, 50GBASE-LR	139.5.8
…	
100GBASE-DR	140.5.8

45.2.1.7.5 Receive fault (1.8.10)

Insert the following rows after the row for 40GBASE-T (which was inserted by IEEE Std 802.3bq-2016) with the exception of the 100GBASE-DR row which goes after the 100GBASE-SR4 PMD in Table 45–10 as follows (unchanged rows not shown):

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Table 45–10—Receive fault description location

PMA/PMD	Description location
…	
50GBASE-KR, 100GBASE-KR2, 200GBASE-KR4	137.8.10
50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4	136.8.10
50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4	138.5.11
50GBASE-FR, 50GBASE-LR	139.5.9
…	
100GBASE-DR	140.5.9

45.2.1.8 PMD transmit disable register (Register 1.9)

Insert the following rows after the row for 40GBASE-T (which was inserted by IEEE Std 802.3bq-2016) with the exception of the 100GBASE-DR row which goes after the 100GBASE-SR4 PMD in Table 45–12 as follows (unchanged rows not shown):

Table 45–12—Transmit disable description location

PMA/PMD	Description location
…	
50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4	137.8.6
50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4	136.8.6
50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4	138.5.7
50GBASE-FR and 50GBASE-LR	139.5.6
…	
100GBASE-DR	140.5.6

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Insert 45.2.1.14b1 before 45.2.1.14c (as inserted by IEEE Std 802.3bz-2016) as follows:

45.2.1.14b1 50G PMA/PMD extended ability (Register 1.20)

The assignment of bits in the 50G PMA/PMD extended ability register is shown in Table 45–17b1.

Table 45–17b1—50G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.20.15	50G PMA remote loopback ability	1 = 50G PMA has the ability to perform a remote loopback function 0 = 50G PMA does not have the ability to perform a remote loopback function	RO
1.20.14:5	Reserved	Value always 0	RO
1.20.4	50GBASE-LR ability	1 = PMA/PMD is able to perform 50GBASE-LR 0 = PMA/PMD is not able to perform 50GBASE-LR	RO
1.20.3	50GBASE-FR ability	1 = PMA/PMD is able to perform 50GBASE-FR 0 = PMA/PMD is not able to perform 50GBASE-FR	RO
1.20.2	50GBASE-SR ability	1 = PMA/PMD is able to perform 50GBASE-SR 0 = PMA/PMD is not able to perform 50GBASE-SR	RO
1.20.1	50GBASE-CR ability	1 = PMA/PMD is able to perform 50GBASE-CR 0 = PMA/PMD is not able to perform 50GBASE-CR	RO
1.20.0	50GBASE-KR ability	1 = PMA/PMD is able to perform 50GBASE-KR 0 = PMA/PMD is not able to perform 50GBASE-KR	RO

[a]RO = Read only

45.2.1.14b1.1 50G PMA remote loopback ability (1.20.15)

When read as a one, bit 1.20.15 indicates that the 50G PMA is able to perform the remote loopback function. When read as a zero, bit 1.20.15 indicates that the 50G PMA is not able to perform the remote loopback function. If a PMA is able to perform the remote loopback function, then it is controlled using the PMA remote loopback bit 1.0.1 (see 45.2.1.1.4).

45.2.1.14b1.2 50GBASE-LR ability (1.20.4)

When read as a one, bit 1.20.4 indicates that the PMA/PMD is able to operate as a 50GBASE-LR PMA/PMD type. When read as a zero, bit 1.20.4 indicates that the PMA/PMD is not able to operate as a 50GBASE-LR PMA/PMD type.

45.2.1.14b1.3 50GBASE-FR ability (1.20.3)

When read as a one, bit 1.20.3 indicates that the PMA/PMD is able to operate as a 50GBASE-FR PMA/PMD type. When read as a zero, bit 1.20.3 indicates that the PMA/PMD is not able to operate as a 50GBASE-FR PMA/PMD type.

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45.2.1.14b1.4 50GBASE-SR ability (1.20.2)

When read as a one, bit 1.20.2 indicates that the PMA/PMD is able to operate as a 50GBASE-SR PMA/PMD type. When read as a zero, bit 1.20.2 indicates that the PMA/PMD is not able to operate as a 50GBASE-SR PMA/PMD type.

45.2.1.14b1.5 50GBASE-CR ability (1.20.1)

When read as a one, bit 1.20.1 indicates that the PMA/PMD is able to operate as a 50GBASE-CR PMA/PMD type. When read as a zero, bit 1.20.1 indicates that the PMA/PMD is not able to operate as a 50GBASE-CR PMA/PMD type.

45.2.1.14b1.6 50GBASE-KR ability (1.20.0)

When read as a one, bit 1.20.0 indicates that the PMA/PMD is able to operate as a 50GBASE-KR PMA/PMD type. When read as a zero, bit 1.20.0 indicates that the PMA/PMD is not able to operate as a 50GBASE-KR PMA/PMD type.

Insert 45.2.1.14f1 after 45.2.1.14f (as inserted by IEEE Std 802.3bs-201x) as follows:

45.2.1.14f1 PMA/PMD extended ability 2 (Register 1.25)

The assignment of bits in the PMA/PMD extended ability 2 register is shown in Table 45–17f1.

Table 45–17f1—PMA/PMD extended ability 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.25.15:1	Reserved	Value always 0	RO
1.25.0	50G extended abilities	1 = PMA/PMD has 50G extended abilities listed in register 1.20 0 = PMA/PMD does not have 50G extended abilities	RO

[a]RO = Read only

45.2.1.14f1.1 50G extended abilities (1.25.0)

When read as a one, bit 1.25.0 indicates that the PMA/PMD has 50G extended abilities listed in register 1.20. When read as a zero, bit 1.25.0 indicates that the PMA/PMD does not have 50G extended abilities.

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45.2.1.101 RS-FEC control register (Register 1.200)

Change Table 45–79 (as modified by IEEE Std 802.3by-2016) as follows:

Table 45–79—RS-FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.200.15:4 ~~1.200.15:3~~	Reserved	Value always 0	RO
1.200.3	Four lane PMD indication	1 = FEC is not being used with a four-lane PMD (the four_lane_pmd variable defined 91.6.2a is set to zero) 0 = FEC is being used with a four-lane PMD (the four_lane_pmd variable defined 91.6.2a is set to one)	R/W
1.200.2	25G RS-FEC enable	1 = The 25GBASE-R Reed-Solomon FEC is enabled 0 = The 25GBASE-R Reed-Solomon FEC is disabled	R/W
1.200.1	FEC bypass indication enable	1 = FEC decoder does not indicate errors to the PCS 0 = FEC decoder indicates errors to the PCS layer	R/W
1.200.0	FEC bypass correction enable	1 = FEC decoder performs error detection without error correction 0 = FEC decoder performs error detection and error correction	R/W

[a]R/W = Read/Write, RO = Read only

Insert 45.2.1.101.aa before 45.2.1.101.a (as inserted by IEEE Std 802.3by-2016) as follows:

45.2.1.101.aa Four-lane PMD (1.200.3)

This bit enables the alignment marker mapping function in the RS-FEC to substitute the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16 (see 91.5.2.6). When this bit is set to zero, the alignment markers corresponding to PCS lanes 17, 18, and 19 are passed through unmodified. The default value of this bit is zero.

45.2.1.102 RS-FEC status register (Register 1.201)

Change the reserved rows for 1.201.7:3 in Table 45–80 as follows (unchanged rows not shown):

Table 45–80—RS-FEC status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.201.7	FEC optional states supported	1 = RS-FEC supports optional states in Figure 91–8 0 = RS-FEC does not support optional states in Figure 91–8	RO
~~1.201.7:3~~ 1.201.6:3	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000168

Change 45.2.1.102.1, 45.2.1.102.2 (as modified by IEEE Std 802.3by-2016), and 45.2.1.102.5, and 45.2.1.102.6 as follows

45.2.1.102.1 PCS align status (1.201.15)

Bit 1.201.15 indicates the PCS alignment status of the RS-FEC. For the RS-FEC described in Clause 91 or Clause 134, PCS alignment is defined as block lock, alignment marker lock and deskew of all 20 transmit PCS lanes. For the RS-FEC described in Clause 108, PCS alignment is defined as block lock of the transmit PCS signal. When read as a zero, bit 1.201.15 indicates that the RS-FEC has not obtained PCS alignment. When read as a one, bit 1.201.15 indicates that the RS-FEC has obtained PCS alignment.

45.2.1.102.2 RS-FEC align status (1.201.14)

Bit 1.201.14 indicates the PMA alignment status of the RS-FEC. For the RS-FEC described in Clause 91 or Clause 134, PMA alignment is defined as alignment marker lock and deskew of all four lanes on the PMA service interface. For the RS-FEC described in Clause 108, PMA alignment is defined as codeword marker lock on the PMA service interface. When read as a zero, bit 1.201.14 indicates that the RS-FEC has not obtained PMA alignment. When read as a one, bit 1.201.14 indicates that the RS-FEC has obtained PMA alignment.

45.2.1.102.5 FEC AM lock 1 (1.201.9)

When read as a one, bit 1.201.9 indicates that the RS-FEC described in Clause 91 or Clause 134 has locked and aligned lane 1 of the PMA service interface. When read as a zero, bit 1.201.9 indicates that the RS-FEC has not locked and aligned lane 1 of the PMA service interface. This bit reflects the state of amps_lock[1] (see 91.5.3.1).

45.2.1.102.6 FEC AM lock 0 (1.201.8)

When read as a one, bit 1.201.8 indicates that the RS-FEC described in Clause 91 or Clause 134 has locked and aligned lane 0 of the PMA service interface. When read as a zero, bit 1.201.8 indicates that the RS-FEC has not locked and aligned lane 0 of the PMA service interface. This bit reflects the state of amps_lock[0] (see 91.5.3.1).

Insert 45.2.1.102.6a after 45.2.1.102.6 as follows:

45.2.1.102.6a FEC optional states supported (1.201.7)

When read as a one, bit 1.201.7 indicates that the RS-FEC described in Clause 91 implements the optional states in Figure 91–8. When read as a zero, bit 1.201.7 indicates that the optional states are not implemented.

Change the second sentence of 45.2.1.108 as follows

45.2.1.108 RS-FEC BIP error counter lane 0 (Register 1.230)

The RS-FEC described in Clause 91 or Clause 134 calculates a BIP value for each PCS lane (see 91.5.2.4, 91.6.3).

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Change 45.2.1.116d to 45.2.1.116f (as inserted by IEEE Std 802.3bs-201x) as follows:

45.2.1.116d 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register (Register 1.500)

The assignment of bits in the 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register is shown in Table 45–90ab. The transmitter, receive direction, is the transmitter that sends data towards the MAC.

Table 45–90ab—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.500.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.500.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Requested_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Requested_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Requested_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Requested_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Requested_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Requested_eq_c1* = 0 (c(1) ratio 0)	RO
1.500.11:10	Pre-cursor request	11 10 1 1 *Requested_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Requested_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Requested_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Requested_eq_cm1* = 0 (c(–1) ratio 0)	RO
1.500.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Remote_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Remote_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Remote_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Remote_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Remote_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Remote_eq_c1* = 0 (c(1) ratio 0)	R/W
1.500.6:5	Pre-cursor remote setting	6 5 1 1 *Remote_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Remote_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Remote_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Remote_eq_cm1* = 0 (c(–1) ratio 0)	R/W

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000170

Table 45–90ab—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.500.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Local_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Local_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Local_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Local_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Local_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Local_eq_c1* = 0 (c(1) ratio 0)	R/W
1.500.1:0	Pre-cursor local setting	1 0 1 1 *Local_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Local_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Local_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Local_eq_cm1* = 0 (c(–1) ratio 0)	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.116d.1 Request flag (1.500.15)

The value of this bit indicates the value of the variable *Request_flag* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This indicates whether the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip device is issuing a request to change the remote transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.116d.2 Post-cursor request (1.500.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to 1, this value indicates the ratio of the post-cursor coefficient c(1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction.

45.2.1.116d.3 Pre-cursor request (1.500.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to 1, this value indicates the ratio of the pre-cursor coefficient c(–1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction.

45.2.1.116d.4 Post-cursor remote setting (1.500.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient c(1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and

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120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.116d.5 Pre-cursor remote setting (1.500.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient c(−1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and 120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.116d.6 Post-cursor local setting (1.500.4:2)

The value of these bits sets the variable *Local_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.2 and 120D.3.2.3), which controls the weight of the transmitter equalization post-cursor coefficient c(1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.116d.7 Pre-cursor local setting (1.500.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and 120D.3.1.2), which controls the weight of the transmitter equalization pre-cursor coefficient c(−1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.116e 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 1 through lane 15 registers (Registers 1.501 through 1.515)

The 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 1 through lane 15 registers are defined similarly to register 1.500 (which is used for lane 0, see 45.2.1.116d) but for lanes 1 through 15, respectively. The transmitter, receive direction, is the transmitter that sends data towards the MAC.

45.2.1.116f 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register (Register 1.516)

The assignment of bits in the 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register is shown in Table 45–90ac. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

45.2.1.116f.1 Request flag (1.516.15)

The value of this bit indicates the value of the variable *Request_flag* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This indicates whether the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip device is issuing a request to change the remote transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000172

Table 45–90ac—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.516.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.516.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Requested_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Requested_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Requested_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Requested_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Requested_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Requested_eq_c1* = 0 (c(1) ratio 0)	RO
1.516.11:10	Pre-cursor request	11 10 1 1 *Requested_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Requested_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Requested_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Requested_eq_cm1* = 0 (c(–1) ratio 0)	RO
1.516.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Remote_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Remote_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Remote_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Remote_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Remote_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Remote_eq_c1* = 0 (c(1) ratio 0)	R/W
1.516.6:5	Pre-cursor remote setting	6 5 1 1 *Remote_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Remote_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Remote_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Remote_eq_cm1* = 0 (c(–1) ratio 0)	R/W
1.516.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Local_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Local_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Local_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Local_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Local_eq_c1* = 1 (c(1) ratio–0.05) 0 0 0 *Local_eq_c1* = 0 (c(1) ratio 0)	R/W
1.516.1:0	Pre-cursor local setting	1 0 1 1 *Local_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Local_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Local_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Local_eq_cm1* = 0 (c(–1) ratio 0)	R/W

[a]R/W = Read/Write, RO = Read only

400GAUI-n receiver in the transmit direction is not present in the package, then the value returned for this bit should be zero.

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45.2.1.116f.2 Post-cursor request (1.516.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to 1, this value indicates the ratio of the post-cursor coefficient c(1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction.

45.2.1.116f.3 Pre-cursor request (1.516.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to 1, this value indicates the ratio of the pre-cursor coefficient c(−1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction.

45.2.1.116f.4 Post-cursor remote setting (1.516.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient c(1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.116f.5 Pre-cursor remote setting (1.516.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient c(−1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.116f.6 Post-cursor local setting (1.516.4:2)

The value of these bits sets the variable *Local_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2), which controls the weight of the transmitter equalization post-cursor coefficient c(1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.116f.7 Pre-cursor local setting (1.516.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2), which controls the weight of the transmitter equalization pre-cursor coefficient c(−1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction is not present in the package, then these bits have no effect.

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45.2.1.116g 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 15 registers (Registers 1.517 through 1.531)

The 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 15 registers are defined similarly to register 1.516 (which is used for lane 0, see 45.2.1.116f) but for lanes 1 through 15, respectively. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

Insert 45.2.1.116h to 45.2.1.116n after 45.2.1.116g (as inserted by IEEE Std 802.3bs-201x) as follows:

45.2.1.116h PMA precoder control down Tx (Register 1.600)

The assignment of bits in the PMA precoder control down Tx register is shown in Table 45–90ad.

Table 45–90ad—PMA precoder control down Tx register bit definitions

Bit(s)	Name	Description	R/W[a]
1.600.15:4	Reserved	Value always 0	RO
1.600.3	Lane 3 down transmitter precoder enable	1 = Lane 3 down Tx precoder enabled 0 = Lane 3 down Tx precoder disabled	RW
1.600.2	Lane 2 down transmitter precoder enable	1 = Lane 2 down Tx precoder enabled 0 = Lane 2 down Tx precoder disabled	RW
1.600.1	Lane 1 down transmitter precoder enable	1 = Lane 1 down Tx precoder enabled 0 = Lane 1 down Tx precoder disabled	RW
1.600.0	Lane 0 down transmitter precoder enable	1 = Lane 0 down Tx precoder enabled 0 = Lane 0 down Tx precoder disabled	RW

[a]R/W = Read/Write, RO = Read only

45.2.1.116h.1 PMA precoder down Tx enable lane 3 (1.600.3)

This bit enables the lane 3 down Tx precoder.

45.2.1.116h.2 PMA precoder down Tx enable lane 2 (1.600.2)

This bit enables the lane 2 down Tx precoder.

45.2.1.116h.3 PMA precoder down Tx enable lane 1 (1.600.1)

This bit enables the lane 1 down Tx precoder.

45.2.1.116h.4 PMA precoder down Tx enable lane 0 (1.600.0)

This bit enables the lane 0 down Tx precoder.

45.2.1.116i PMA precoder control down Rx (Register 1.601)

The assignment of bits in the precoder control down Rx register is shown in Table 45–90ae.

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Table 45–90ae—PMA precoder control down Rx register bit definitions

Bit(s)	Name	Description	R/W[a]
1.601.15:4	Reserved	Value always 0	RO
1.601.3	Lane 3 down receiver precoder enable	1 = Lane 3 down Rx precoder enabled 0 = Lane 3 down Rx precoder disabled	RW
1.601.2	Lane 2 down receiver precoder enable	1 = Lane 2 down Rx precoder enabled 0 = Lane 2 down Rx precoder disabled	RW
1.601.1	Lane 1 down receiver precoder enable	1 = Lane 1 down Rx precoder enabled 0 = Lane 1 down Rx precoder disabled	RW
1.601.0	Lane 0 down receiver precoder enable	1 = Lane 0 down Rx precoder enabled 0 = Lane 0 down Rx precoder disabled	RW

[a]R/W = Read/Write, RO = Read only

45.2.1.116i.1 PMA precoder down Rx enable lane 3 (1.601.3)

This bit enables the lane 3 down Rx precoder.

45.2.1.116i.2 PMA precoder down Rx enable lane 2 (1.601.2)

This bit enables the lane 2 down Rx precoder.

45.2.1.116i.3 PMA precoder down Rx enable lane 1 (1.601.1)

This bit enables the lane 1 down Rx precoder.

45.2.1.116i.4 PMA precoder down Rx enable lane 0 (1.601.0)

This bit enables the lane 0 down Rx precoder.

45.2.1.116j PMA precoder control up Tx (Register 1.602)

The assignment of bits in the precoder control up Tx register is shown in Table 45–90af.

Table 45–90af—PMA precoder control up Tx register bit definitions

Bit(s)	Name	Description	R/W[a]
1.602.15:2	Reserved	Value always 0	RO
1.602.1	Lane 1 up transmitter precoder enable	1 = Lane 1 up Tx precoder enabled 0 = Lane 1 up Tx precoder disabled	RW
1.602.0	Lane 0 up transmitter precoder enable	1 = Lane 0 up Tx precoder enabled 0 = Lane 0 up Tx precoder disabled	RW

[a]R/W = Read/Write, RO = Read only

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000176

45.2.1.116j.1 PMA precoder up Tx enable lane 1 (1.602.1)

This bit enables the lane 1 up Tx precoder.

45.2.1.116j.2 PMA precoder up Tx enable lane 0 (1.602.0)

This bit enables the lane 0 up Tx precoder.

45.2.1.116k PMA precoder control up Rx (Register 1.603)

The assignment of bits in the precoder control up Rx register is shown in Table 45–90ag.

Table 45–90ag—PMA precoder control up Rx register bit definitions

Bit(s)	Name	Description	R/W[a]
1.603.15:2	Reserved	Value always 0	RO
1.603.1	Lane 1 up receiver precoder enable	1 = Lane 1 up Rx precoder enabled 0 = Lane 1 up Rx precoder disabled	RW
1.603.0	Lane 0 up receiver precoder enable	1 = Lane 0 up Rx precoder enabled 0 = Lane 0 up Rx precoder disabled	RW

[a]R/W = Read/Write, RO = Read only

45.2.1.116k.1 PMA precoder up Rx enable lane 1 (1.603.1)

This bit enables the lane 1 up Rx precoder.

45.2.1.116k.2 PMA precoder up Rx enable lane 0 (1.603.0)

This bit enables the lane 0 up Rx precoder.

45.2.1.116l PMA precoder request status (Register 1.604)

The assignment of bits in the precoder request status register is shown in Table 45–90ah.

Table 45–90ah—PMA precoder request status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.604.15:2	Reserved	Value always 0	RO
1.604.1	precoder_request_status_1	1 = Lane 1 precoding requested 0 = Lane 1 precoding not requested	RO
1.604.0	precoder_request_status_0	1 = Lane 0 precoding requested 0 = Lane 0 precoding not requested	RO

[a]R/W = Read/Write, RO = Read only

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45.2.1.116l.1 PMA precoder request status lane 1 (1.604.1)

This bit indicates the lane 1 precoder request status.

45.2.1.116l.2 PMA precoder request status lane 0 (1.604.0)

This bit indicates the lane 0 precoder request status.

45.2.1.116m PMA precoder request down (Register 1.605)

The assignment of bits in the precoder request down register is shown in Table 45–90ai.

Table 45–90ai—PMA precoder request down register bit definitions

Bit(s)	Name	Description	R/W[a]
1.605.15:2	Reserved	Value always 0	RO
1.605.1	precoder_request_down_1	1 = Lane 1 precoder down requested 0 = Lane 1 precoder down not requested	RW
1.605.0	precoder_request_down_0	1 = Lane 0 precoder down requested 0 = Lane 0 precoder down not requested	RW

[a]R/W = Read/Write, RO = Read only

45.2.1.116m.1 PMA precoder request down lane 1 (1.605.1)

This bit enables the request of precoding in the down direction for lane 1.

45.2.1.116m.2 PMA precoder request down lane 0 (1.605.0)

This bit enables the request of precoding in the down direction for lane 0.

45.2.1.116n PMA precoder request up (Register 1.606)

The assignment of bits in the precoder request up register is shown in Table 45–90aj.

Table 45–90aj—PMA precoder request up register bit definitions

Bit(s)	Name	Description	R/W[a]
1.606.15:2	Reserved	Value always 0	RO
1.606.1	precoder_request_up_1	1 = Lane 1 precoder up requested 0 = Lane 1 precoder up not requested	RW
1.606.0	precoder_request_up_0	1 = Lane 0 precoder up requested 0 = Lane 0 precoder up not requested	RW

[a]R/W = Read/Write, RO = Read only

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45.2.1.116n.1 PMA precoder request up lane 1 (1.606.1)

This bit enables the request of precoding in the up direction for lane 1.

45.2.1.116n.2 PMA precoder request up lane 0 (1.606.0)

This bit enables the request of precoding in the up direction for lane 0.

Insert 45.2.1.118a after 45.2.1.118 as follows:

45.2.1.118a BASE-R PAM4 PMD training LP control registers, lanes 0 through 3 (Register 1.1120 through 1.1123)

The BASE-R PAM4 PMD training LP control registers, lanes 0 through 3, reflect the contents of the first 16-bit word of the training frame most recently received from the control channel for each lane. Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123.

The assignment of bits in the BASE-R PAM4 PMD training LP control registers is shown in Table 45–90ak.

Table 45–90ak—BASE-R PAM4 PMD training LP control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1120.15:41	Reserved	Value always 0	RO
1.1120.13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control	RW
1.1120.11:10	Reserved	Value always 0	RO
1.1120.9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RW
1.1120.7:5	Reserved	Value always 0	RO
1.1120.4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RW
1.1120.1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold	RW

[a]R/W = Read/Write, RO = Read only

Normally the bits in this register are read only; however, when training is disabled the registers become writeable.

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Insert 45.2.1.119a after 45.2.1.119 as follows:

45.2.1.119a BASE-R PAM4 PMD training LP status registers, lanes 0 through 3 (Register 1.1220 through 1.1223)

The BASE-R PAM4 PMD training LP status registers, lanes 0 through 3, reflect the contents of the second 16-bit word of the training frame most recently received from the control channel for each lane. Lane 0 maps to register 1.1220, lane 1 maps to register 1.1221, lane 2 maps to register 1.1222, and lane 3 maps to register 1.1223.

The assignment of bits in the BASE-R PAM4 PMD training LP status registers is shown in Table 45–90al.

Table 45–90al—BASE-R PAM4 PMD training LP status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1220.15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue	RO
1.1220.14:12	Reserved	Value always 0	RO
1.1220.11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RO
1.1220.9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified	RO
1.1220.8	Initial condition status	1 = Updated 0 = Not updated	RO
1.1220.7	Parity	Even parity bit	RO
1.1220.6	Reserved	Value always 0	RO
1.1220.5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RO
1.1220.2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated	RO

[a]R/W = Read/Write, RO = Read only

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Insert 45.2.1.120a after 45.2.1.120 as follows:

45.2.1.120a BASE-R PAM4 PMD training LD control registers, lanes 0 through 3 (Register 1.1320 through 1.1323)

The BASE-R PAM4 PMD training LD control registers, lanes 0 through 3, reflect the contents of the first 16-bit word of the outgoing training frame for each lane. Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, and lane 3 maps to register 1.1323.

The assignment of bits in the BASE-R PAM4 PMD training LP control registers is shown in Table 45–90am.

Table 45–90am—BASE-R PAM4 PMD training LD control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1320.15:41	Reserved	Value always 0	RO
1.1320.13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control	RW
1.1320.11:10	Reserved	Value always 0	RO
1.1320.9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RW
1.1320.7:5	Reserved	Value always 0	RO
1.1320.4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RW
1.1320.1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold	RW

[a]R/W = Read/Write, RO = Read only

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Insert 45.2.1.121a after 45.2.1.121 as follows:

45.2.1.121a BASE-R PAM4 PMD training LD status registers, lanes 0 through 3 (Register 1.1420 through 1.1423)

The BASE-R PAM4 PMD training LD status registers, lanes 0 through 3, reflect the contents of the second 16-bit word of the outgoing training frame for each lane. Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, and lane 3 maps to register 1.1423.

The assignment of bits in the BASE-R PAM4 PMD training LD status registers is shown in Table 45–90an.

Table 45–90an—BASE-R PAM4 PMD training LD status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1420.15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue	RO
1.1420.14:12	Reserved	Value always 0	RO
1.1420.11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RO
1.1420.9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified	RO
1.1420.8	Initial condition status	1 = Updated 0 = Not updated	RO
1.1420.7	Parity	Even parity bit	RO
1.1420.6	Reserved	Value always 0	RO
1.1420.5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RO
1.1420.2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated	RO

[a]R/W = Read/Write, RO = Read only

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45.2.1.124 PRBS pattern testing control (Register 1.1501)

Change the last four sentences of 45.2.1.124 (as inserted by IEEE Std 802.3bs-201x) as follows:

For the 50GBASE-R, 100GBASE-R PAM4, 200GBASE-R, and 400GBASE-R PMAs, the assertion of register 1.1501 bit 13 operates in conjunction with register 1.1501 bits 3 and 1. If neither bit is asserted, then register 1.1501 bit 13 has no effect. Also for the 50GBASE-R, 100GBASE-R PAM4, 200GBASE-R, and 400GBASE-R PMAs, the assertion of register 1.1501 bit 14 operates in conjunction with register 1.1501 bit 3. If bit 1.1501.3 is not asserted, then register 1.1501 bit 14 has no effect. For other PMA/PMD types register 1.1501 bits 13 and 14 have no effect.

45.2.3 PCS registers

45.2.3.1 PCS control 1 register (Register 3.0)

Change the row for bits 3.0.5:2 in Table 45–120 (as modified by IEEE Std 802.3bz-2016) as follows (unchanged rows not shown):

Table 45–120—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
3.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 1 = Reserved 1 0 1 0 = 400 Gb/s 1 0 0 1 = 200 Gb/s 1 0 0 0 = 5 Gb/s 0 1 1 1 = 2.5 Gb/s 0 1 1 0 = 50 Gb/s ~~Reserved~~ 0 1 0 1 = 25 Gb/s 0 1 0 0 = 100 Gb/s 0 0 1 1 = 40 Gb/s 0 0 1 0 = 10/1 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
…			

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

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45.2.3.2 PCS status 1 register (Register 3.1)

45.2.3.2.7 PCS receive link status (3.1.2)

Change the third sentence of 45.2.3.2.7 (as modified by IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016 and IEEE Std 802.3bs-201x) as follows:

When a 10/25/40/50/100/200/400GBASE-R, 10GBASE-W, or any MultiGBASE-T mode of operation is selected for the PCS using the PCS type selection field (3.7.2:0), this bit is a latching low version of bit 3.32.12.

45.2.3.4 PCS speed ability (Register 3.4)

Change the row for 3.4.5 in Table 45–122 (as inserted by IEEE Std 802.3bz-2016) as follows (unchanged rows not shown):

Table 45–122—PCS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
3.4.5	~~Reserved~~ 50G capable	~~Value always 0~~ 1 = PCS is capable of operating at 50 Gb/s 0 = PCS is not capable of operating at 50 Gb/s	RO
…			

[a]RO = Read only

Insert 45.2.3.4.5a after 45.2.3.4.5 (as inserted by IEEE Std 802.3by-2016) as follows:

45.2.3.4.5a 50G capable (3.4.5)

When read as a one, bit 3.4.5 indicates that the PCS is able to operate at a data rate of 50 Gb/s. When read as a zero, bit 3.4.5 indicates that the PCS is not able to operate at a data rate of 50 Gb/s.

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45.2.3.6 PCS control 2 register (Register 3.7)

Change Table 45–123 (as modified by IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, IEEE Std 802.3bz-2016, and IEEE Std 802.3bs-201x) as follows:

Table 45–123—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.7.15:4	Reserved	Value always 0	RO
3.7.3:0	PCS type selection	3 2 1 0 1 1 1 x = reserved 1 1 0 1 = Select 400GBASE-R PCS type 1 1 0 0 = Select 200GBASE-R PCS type 1 0 1 1 = Select 5GBASE-T PCS type 1 0 1 0 = Select 2.5GBASE-T PCS type 1 0 0 1 = Select 25GBASE-T PCS type 1 0 0 0 = Select 50GBASE-R PCS type ~~reserved~~ 0 1 1 1 = Select 25GBASE-R PCS type 0 1 1 0 = Select 40GBASE-T PCS type 0 1 0 1 = Select 100GBASE-R PCS type 0 1 0 0 = Select 40GBASE-R PCS type 0 0 1 1 = Select 10GBASE-T PCS type 0 0 1 0 = Select 10GBASE-W PCS type 0 0 0 1 = Select 10GBASE-X PCS type 0 0 0 0 = Select 10GBASE-R PCS type	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.7 PCS status 2 register (Register 3.8)

Change row for 3.8.8 in Table 45–124a (as modified by IEEE Std 802.3bq-2016) as follows (unchanged rows not shown):.

Table 45–124 —PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.8.8	~~Reserved~~ 50GBASE-R capable	~~Value always 0~~ 1 = PCS is able to support 50GBASE-R PCS type 0 = PCS is not able to support 50GBASE-R PCS type	RO

[a]RO = Read only

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Insert 45.2.3.7.3ab after 45.2.3.7.3aa (as inserted by IEEE Std 802.3bq-2016) as follows:

45.2.3.7.3ab 50GBASE-R capable (3.8.8)

When read as a one, bit 3.8.8 indicates that the PCS is able to support the 50GBASE-R PCS type. When read as a zero, bit 3.8.8 indicates that the PCS is not able to support the 50GBASE-R PCS type.

45.2.3.9 EEE control and capability 1 (Register 3.20)

Change the reserved row for 3.20.15:14 in Table 45–125 as follows (unchanged rows not shown):

Table 45–125—EEE control and capability 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.20.15~~:14~~	Reserved	Value always 0	RO
3.20.14	50GBASE-R fast wake	1 = EEE fast wake is supported for 50GBASE-R 0 = EEE fast wake is not supported for 50GBASE-R	RO
…			

[a]R/W = Read/Write, RO = Read only

Insert 45.2.3.9.a before 45.2.3.9.1 as follows:

45.2.3.9.a 50GBASE-R EEE fast wake supported (3.20.14)

If the PCS supports EEE fast wake operation for 50GBASE-R, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.13 BASE-R and MultiGBASE-T PCS status 1 register (Register 3.32)

45.2.3.13.1 BASE-R and MultiGBASE-T receive link status (3.32.12)

Change the last sentence of 45.2.3.13.1 (as modified by IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, IEEE Std 802.3bz-2016, and IEEE Std 802.3bs-201x) as follows:

This bit is a reflection of the PCS_status variable defined in 49.2.14.1 for 10/25GBASE-R, in 126.3.7.1 for 2.5GBASE-T and 5GBASE-T, in 55.3.7.1 for 10GBASE-T, in 113.3.7.1 for 25GBASE-T and 40GBASE-T, in 82.3.1 for 40/50/100GBASE-R, and in 119.3 for 200/400GBASE-R.

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45.2.3.13.4 BASE-R and MultiGBASE-T PCS high BER (3.32.1)

Change third sentence of 45.2.3.13.4 (as modified by IEEE Std 802.3by-2016) as follows:

This bit is a direct reflection of the state of the hi_ber variable in the 64B/66B state diagram and is defined in 49.2.13.2.2 for 10/25GBASE-R and in 82.2.19.2.2 for 40/50/100GBASE-R.

45.2.3.13.5 BASE-R and MultiGBASE-T PCS block lock (3.32.0)

Change third sentence of 45.2.3.13.5 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

This bit is a direct reflection of the state of the block_lock variable in the 64B/66B state diagram and is defined in 49.2.13.2.2 for 5/10/25GBASE-R and in 82.2.19.2.2 for 40/50/100GBASE-R.

45.2.3.14 BASE-R and MultiGBASE-T PCS status 2 register (Register 3.33)

45.2.3.14.1 Latched block lock (3.33.15)

Change 45.2.3.14.1 (as modified by IEEE Std 802.3bq-2016 and IEEE Std 802.3cb-201x) as follows:

When read as a one, bit 3.33.15 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has achieved block lock. When read as a zero, bit 3.33.15 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has lost block lock.

The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 5/10/25/40/50/100GBASE-R and MultiGBASE-T PCS block lock status bit (3.32.0).

45.2.3.14.2 Latched high BER (3.33.14)

Change 45.2.3.14.2 (as modified by IEEE Std 802.3bq-2016, IEEE Std 802.3by-2016, and IEEE Std 802.3cb-201x) as follows:

When read as a one, bit 3.33.14 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has detected a high BER. When read as a zero, bit 3.33.14 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has not detected a high BER.

The latched high BER bit shall be implemented with latching high behavior.

This bit is a latching high version of the 5/10/25/40/50/100GBASE-R and MultiGBASE-T PCS high BER status bit (3.32.1).

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45.2.3.14.3 BER(3.33.13:8)

Change first sentence of 45.2.3.14.3 (as modified by IEEE Std 802.3bq-2016, IEEE Std 802.3by-2016, and IEEE Std 802.3cb-201x) as follows:

The BER counter is a six bit count as defined by the ber_count variable in 49.2.14.2 and 82.2.19.2.4 for 5/10/25/40/50/100GBASE-R and defined by counter lfer_count in 55.3.6.2 for 10GBASE-T and in 113.3.6.2.2 for 25GBASE-T and 40GBASE-T.

45.2.3.14.4 Errored blocks (3.33.7:0)

Change first sentence of 45.2.3.14.4 (as modified by IEEE Std 802.3bq-2016, IEEE Std 802.3by-2016, and IEEE Std 802.3cb-201x) as follows:

The errored blocks counter is an eight bit count defined by the errored_block_count counter specified in 49.2.14.2 for 5/10/25GBASE-R, in 82.3.1 for 40/50/100GBASE-R and defined by counter errored_block_count in 55.3.6.2 for 10GBASE-T and in 113.3.6.2.2 for 25GBASE-T and 40GBASE-T.

45.2.3.17 BASE-R PCS test-pattern control register (Register 3.42)

Change the fifth sentence of 45.2.3.17 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

Scrambled idle test patterns are defined for 25/40/50/100/200/400GBASE-R PCS only.

45.2.7 Auto-Negotiation registers

Change the reserved row 7.49 through 7.59 in Table 45–200 as follows (unchanged rows not shown):

Table 45–200—Auto-Negotiation MMD registers

Register address	Register name	Subclause
7.49	Backplane Ethernet, BASE-R copper status 2	45.2.7.12a
7.4950 through 7.59	Reserved	

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45.2.7.12 Backplane Ethernet, BASE-R copper status (Register 7.48)

Change the title and text of 45.2.7.12.2 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

45.2.7.12.2 Negotiated Port Type (7.48.1, 7.48.2, 7.48.3, 7.48.5, 7.48.6, 7.48.8, 7.48.9, 7.48.10, 7.48.11, 7.48.12, 7.48.13, 7.48.14, 7.48.15, 7.49.0, 7.49.1, 7.49.2)

When the AN process has been completed as indicated by the AN complete bit, these bits in register 7.48 and register 7.49 indicate the negotiated port type.

Insert 45.2.7.12a after 45.2.7.12 as follows

45.2.7.12a Backplane Ethernet, BASE-R copper status 2 (Register 7.49)

The assignment of bits in the Backplane Ethernet, BASE-R copper status 2 register is shown in Table 45–209a.

Table 45–209a—Backplane Ethernet, BASE-R copper status 2 register (Register 7.49) bit definitions

Bit(s)	Name	Description	RO[a]
7.49.15:3	Reserved	Value always 0	RO
7.49.2	200GBASE-KR4 or 200GBASE-CR4	1 = PMA/PMD is negotiated to perform 200GBASE-KR4 or 200GBASE-CR4 0 = PMA/PMD is not negotiated to perform 200GBASE-KR4 or 200GBASE-CR4	RO
7.49.1	100GBASE-KR2 or 100GBASE-CR2	1 = PMA/PMD is negotiated to perform 100GBASE-KR2 or 100GBASE-CR2 0 = PMA/PMD is not negotiated to perform 100GBASE-KR2 or 100GBASE-CR2	RO
7.49.0	50GBASE-KR or 50GBASE-CR	1 = PMA/PMD is negotiated to perform 50GBASE-KR or 50GBASE-CR 0 = PMA/PMD is not negotiated to perform 50GBASE-KR or 50GBASE-CR	RO

[a]RO = Read only

45.2.7.12a.1 Negotiated Port Type

See 45.2.7.12.2.

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45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) interface[1]

45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface

45.5.3.3 PMA/PMD management functions

Insert the following row at the end of the table in (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] N/A [ ]

[1]*Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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69. Introduction to Ethernet operation over electrical backplanes

69.1 Overview

69.1.1 Scope

Change the second paragraph of 69.1.1 (as modified by IEEE Std 802.3by-201x and IEEE Std 802.3cb-201x) as follows:

Backplane Ethernet supports the IEEE 802.3 full duplex MAC operating at 1000 Mb/s, 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, or 100 Gb/s providing a bit error ratio (BER) better than or equal to 10^{-12} at the MAC/PLS service interface or 200 Gb/s providing a BER better than or equal to 10^{-13} at the MAC/PLS service interface. The following Physical Layers are supported:

Change the list after the second paragraph of 69.1.1 as follows (some unmodified list items are not shown):

- ...
- 40GBASE-KR4 for 40 Gb/s operation over four lanes
- 50GBASE-KR for 50 Gb/s operation over one lane
- 100GBASE-KR4 and 100GBASE-KP4 for 100 Gb/s operation over four lanes
- 100GBASE-KR2 for 100 Gb/s operation over two lanes
- 200GBASE-KR4 for 200 Gb/s operation over four lanes

69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model

Change the first paragraph of 69.1.2 (as modified by IEEE Std 802.3by-201x and IEEE Std 802.3cb-201x) as follows:

Backplane Ethernet couples the IEEE 802.3 MAC to a family of Physical Layers defined for operation over electrical backplanes. The relationships among Backplane Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 69–1, Figure 69–1a, Figure 69–2, ~~and~~ Figure 69–2a, and Figure 69–4.

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Insert Figure 69–4 after Figure 69–2a (as inserted by IEEE Std 802.3cb-201x) as follows:

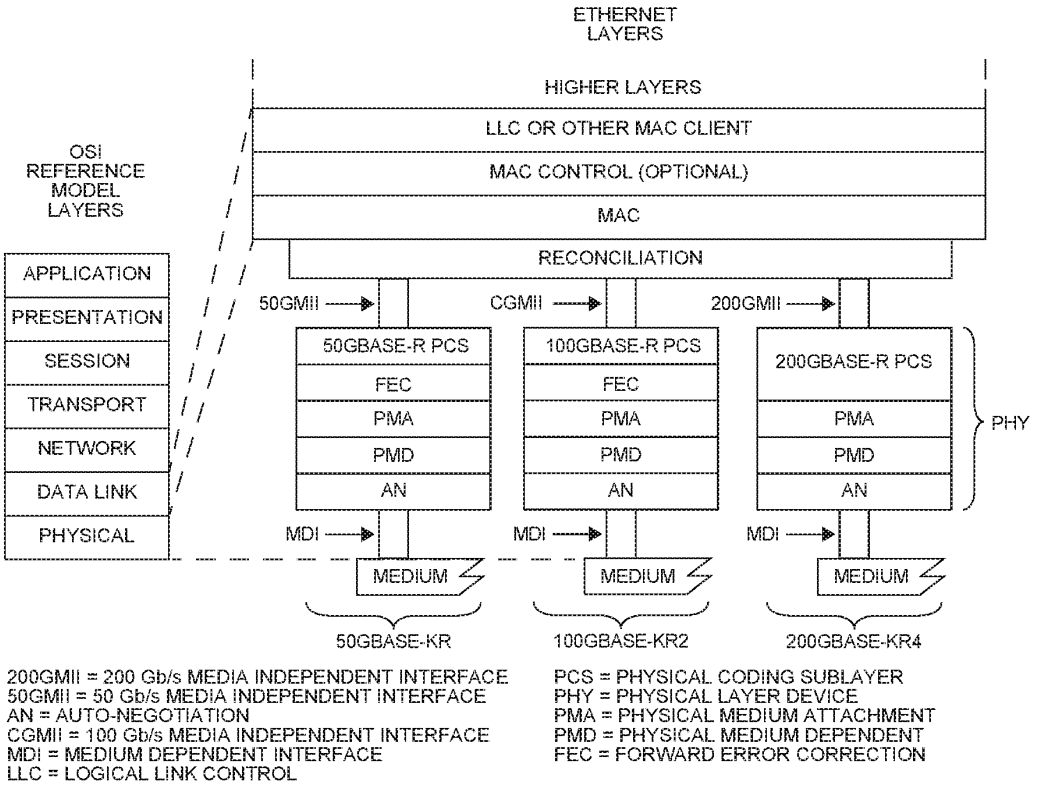


Figure 69–4—Architectural positioning of 50 Gb/s, 100 Gb/s, and 200 Gb/s PAM4 Backplane Ethernet

Change the lettered list after Figure 69–2 (as modified by IEEE Std 802.3by-201x and IEEE Std 802.3cb-201x) as follows (some unchanged rows not shown):

f) The PMA service interface, which, when physically implemented as 25GAUI (25 Gigabit Attachment Unit Interface) or as 50GAUI-1 (50 Gb/s one-lane Attachment Unit Interface) at an observable interconnection port, uses a serial data path as specified in Annex 109A or Annex 135F, respectively.

g) The PMA service interface, which, when physically implemented as LAUI-2/50GAUI-2 (50 Gb/s two-lane Attachment Unit Interface) or as 100GAUI-2 (100 Gb/s two-lane Attachment Unit Interface) at an observable interconnection port, uses a serial two-lane path as specified in Annex 135B, Annex 135D, or Annex 135F, respectively.

h) The PMA service interface, which, when physically implemented as XLAUI (40 Gb/s Attachment Unit Interface), ~~or~~ as CAUI-4 (100 Gb/s four-lane Attachment Unit Interface), or as 200GAUI-4 (200 Gb/s four-lane Attachment Unit Interface) at an observable interconnection port, uses a four-lane data path as specified in Annex 83A, ~~or~~ Annex 83D, or Annex 120D respectively.

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i) The PMA service interface, which, when physically implemented as 200GAUI-8 (200 Gb/s eight-lane Attachment Unit Interface) at an observable interconnection port, uses an eight-lane data path as specified in Annex 120B.

j) The PMA service interface, which, when physically implemented as CAUI-10 (100 Gb/s ten-lane Attachment Unit Interface) at an observable interconnection port, uses a ten-lane data path as specified in Annex 83A.

k) The MDIs for 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KR, 25GBASE-KR, ~~and~~ 25GBASE-KR-S, and 50GBASE-KR use a serial data path ~~while the MDIs for 10GBASE-KX4, 40GBASE-KR4, 100GBASE-KR4, and 100GBASE-KP4 use a four-lane data path~~.

l) The MDI for 100GBASE-KR2 uses a two-lane data path.

m) The MDIs for 10GBASE-KX4, 40GBASE-KR4, 100GBASE-KR4, 100GBASE-KP4, and 200GBASE-KR4 use a four-lane data path.

69.2 Summary of Backplane Ethernet Sublayers

69.2.1 Reconciliation sublayer and media independent interfaces

Change 69.2.1 (as modified by IEEE Std 802.3by-201x) as follows:

The Clause 35 RS and GMII, the Clause 46 RS and XGMII, the Clause 106 RS and 25GMII, ~~and~~ the Clause 81 RS, XLGMII, and CGMII, the Clause 132 RS and 50GMII, and the Clause 117 RS and 200GMII are employed for the same purpose in Backplane Ethernet, that being the interconnection between the MAC sublayer and the PHY.

69.2.3 Physical Layer signaling systems

Insert the following new paragraph after the fourth paragraph in 69.2.3 (as inserted by IEEE Std 802.3cb-201x):

Backplane Ethernet also specifies 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4. The 50GBASE-KR embodiment employs the PCS defined in Clause 133, the RS-FEC defined in Clause 134, the PMA defined in Clause 135, and the PMD defined in Clause 137, and specifies 50 Gb/s operation using 4-level PAM over one differential path in each direction. The 100GBASE-KR2 embodiment employs the PCS defined in Clause 82, the RS-FEC defined in Clause 91, the PMA defined in Clause 135, and the PMD defined in Clause 137, and specifies 100 Gb/s operation using 4-level PAM over two differential paths in each direction. The 200GBASE-KR4 embodiment employs the PCS defined in Clause 119, the PMA defined in Clause 120, and the PMD defined in Clause 137, and specifies 200 Gb/s operation using 4-level PAM over four differential paths in each direction.

Change the last paragraph in 69.2.3 (as modified by IEEE Std 802.3by-201x and IEEE Std 802.3cb-201x) as follows:

Table 69–1, Table 69–1a, Table 69–2, ~~and~~ Table 69–2a, Table 69–2b, Table 69–2c, and Table 69–2d specify the correlation between nomenclature and clauses. A complete implementation conforming to one or more nomenclatures meets the requirements of the corresponding clauses.

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Insert Table 69–2b, Table 69–2c, and Table 69–2d after Table 69–2a (as inserted by IEEE Std 802.3cb-201x):

Table 69–2b—Nomenclature and clause correlation for 50 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause[a]									
	78	132		133	134	135	135A	135B	135C	137
	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	LAUI-2 C2C	50GAUI-2 C2C	50GAUI-1 C2C	50GBASE-KR PMD
50GBASE-KR	O	M	O	M	M	M	O	O	O	M

[a]O = Optional, M = Mandatory.

Table 69–2c—Nomenclature and clause correlation for 100 Gb/s two-lane Backplane Ethernet Physical Layers

Nomenclature	Clause[a]											
	78	81		82	83	83A	83B	91	135	135B	135D	137
	EEE	RS	100GMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10 C2C	CAUI-4 C2C	100GBASE-R RS-FEC	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-2 C2C	100GBASE-KR2 PMD
100GBASE-KR2	O	M	O	M	O	O	O	M	M	O	O	M

[a]O = Optional, M = Mandatory.

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Table 69–2d—Nomenclature and clause correlation for 200 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause[a]							
	78	117		119	120	120B	120D	137
	EEE	RS	200GMII	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-4 C2C	100GBASE-KR4 PMD
200GBASE-KR4	O	M	O	M	M	O	O	M

[a]O = Optional, M = Mandatory.

69.3 Delay constraints

Insert the following paragraph after the fourth paragraph of 69.3:

For 50GBASE-KR, normative delay specifications may be found in 132.1.4, 133.3, 135.5.4, and 137.5, and also referenced in 131.4.

Insert the following paragraphs after the sixth paragraph of 69.3:

For 100GBASE-KR2, normative delay specifications may be found in 81.1.4, 82.5, 135.5.4, and 137.5, and also referenced in 80.4.

For 200GBASE-KR4, normative delay specifications may be found in 117.1.4, 119.5, 120.5.4, and 137.5, and also referenced in 116.4.

69.5 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph of 69.5 (as modified by IEEE Std 802.3by-201x and IEEE Std 802.3cb-201x) as follows:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 70 through Clause 74, Clause 84, Clause 91, Clause 93, Clause 94, Clause 108, Clause 111, Clause 119, Clause 128, Clause 130, Clause 134, Clause 137, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

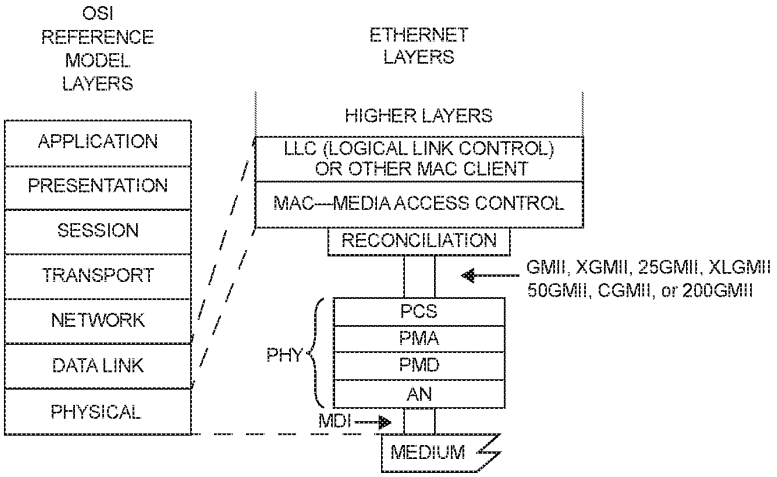
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73. Auto-Negotiation for backplane and copper cable assembly

73.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

Replace Figure 73–1 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) with the following:



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
25GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 73–1—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

73.3 Functional specifications

Change the third paragraph of 73.3 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

These functions shall comply with the state diagrams from Figure 73–9 through Figure 73–11. The Auto-Negotiation functions shall interact with the technology-dependent PHYs through the Technology-Dependent interface (see 73.9). Technology-Dependent PHYs are those supported by the Auto-Negotiation process (see Table 73–4)~~include 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KX4, 10GBASE-KR, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, 25GBASE-CR-S, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-KP4, 100GBASE-KR4, and 100GBASE-CR4~~.

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73.5 DME transmission

73.5.1 DME electrical specifications

Change the second paragraph of 73.5.1 as follows:

For any multi-lane PHY, DME pages shall be transmitted only on lane 0. The transmitters on other lanes should be disabled as specified in 71.6.7, 84.7.7, 85.7.7, 92.7.7, 93.7.7, ~~or~~ 94.3.6.7, 136.8.7, or 137.8.7.

73.6 Link codeword encoding

73.6.4 Technology Ability Field

Change Table 73–4 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

.

Table 73–4—Technology Ability Field encoding

Bit	Technology
A0	1000BASE-KX
A1	10GBASE-KX4
A2	10GBASE-KR
A3	40GBASE-KR4
A4	40GBASE-CR4
A5	100GBASE-CR10
A6	100GBASE-KP4
A7	100GBASE-KR4
A8	100GBASE-CR4
A9	25GBASE-KR-S or 25GBASE-CR-S
A10	25GBASE-KR or 25GBASE-CR
A11	2.5GBASE-KX
A12	5GBASE-KR
A13	50GBASE-KR or 50GBASE-CR
A14	100GBASE-KR2 or 100GBASE-CR2
A15	200GBASE-KR4 or 200GBASE-CR4
~~A13~~A16 through A22	Reserved for future technology

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Replace the third paragraph of 73.6.4 with a note and change the fourth and fifth paragraphs (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

~~For 25 Gb/s operation the same bits are used to advertise backplane and copper cable assembly operation. For other speeds, a PHY for operation over an electrical backplane (e.g., 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 100GBASE-KP4, 100GBASE-KR4) shall not be advertised simultaneously with a PHY for operation over a copper cable assembly (e.g., 40GBASE-CR4, 100GBASE-CR10, 100GBASE-CR4).~~

NOTE– Previous editions of this standard prohibited advertisement of PHYs that support operation over electrical backplanes with PHYs that support operation over copper cable assemblies.

25GBASE-KR-S abilities are a subset of 25GBASE-KR abilities, and likewise 25GBASE-CR-S abilities are a subset of 25GBASE-CR abilities. To allow interoperation between 25GBASE-KR-S and 25GBASE-KR PHY types, and between 25GBASE-CR-S and 25GBASE-CR PHY types, a device that supports 25GBASE-KR or 25GBASE-CR should advertise both A9 and A10 ability bits during auto-negotiation.

The fields A[22:16~~13~~] are reserved for future use. Reserved fields shall be sent as zero and ignored on receive.

73.7 Receive function requirements

73.7.1 DME page reception

Change 73.7.1 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

To be able to detect the DME bits, the receiver should have the capability to receive DME signals sent with the electrical specifications of the PHY~~ (1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KX4, 10GBASE-KR, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, 25GBASE-CR-S, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-KP4, 100GBASE-KR4, or 100GBASE-CR4)~~. The DME transmit signal level and receive sensitivity are specified in 73.5.1.

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73.7.6 Priority Resolution function

Change Table 73–5 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:.

Table 73–5—Priority Resolution

Priority	Technology	Capability
1	200GBASE-KR4 or 200GBASE-CR4	200 Gb/s 4 lane, highest priority
2	100GBASE-KR2 or 100GBASE-CR2	100 Gb/s 2 lane
3 ~~1~~	100GBASE-CR4	100 Gb/s 4 lane~~, highest priority~~
4 ~~2~~	100GBASE-KR4	100 Gb/s 4 lane
5 ~~3~~	100GBASE-KP4	100 Gb/s 4 lane
6 ~~4~~	100GBASE-CR10	100 Gb/s 10 lane
7	50GBASE-KR or 50GBASE-CR	50 Gb/s 1 lane
8 ~~5~~	40GBASE-CR4	40 Gb/s 4 lane
9 ~~6~~	40GBASE-KR4	40 Gb/s 4 lane
10 ~~7~~	25GBASE-KR or 25GBASE-CR	25 Gb/s 1 lane
11 ~~8~~	25GBASE-KR-S or 25GBASE-CR-S	25 Gb/s 1 lane, short reach
12 ~~9~~	10GBASE-KR	10 Gb/s 1 lane
13 ~~10~~	10GBASE-KX4	10 Gb/s 4 lane
14 ~~11~~	5GBASE-KR	5 Gb/s 1 lane
15 ~~12~~	2.5GBASE-KX	2.55 Gb/s 1 lane
16 ~~13~~	1000BASE-KX	1 Gb/s 1 lane, lowest priority

73.10 State diagrams and variable definitions

73.10.1 State diagram variables

Insert the following variables in the variable list by adding 50GR, 100GR, and 200GR at the appropriate place.

50GR; represents the 50GBASE-KR or 50GBASE-CR PMD.

100GR2; represents the 100GBASE-KR2 or 100GBASE-CR2 PMD.

200GR4; represents the 200GBASE-KR4 or 200GBASE-CR4 PMD.

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Insert the following entries in the single_link_ready status at the appropriate place and renumber the existing entries:

9) link_status_[50GR] = OK
14) link_status_[100GR2] = OK
15) link_status_[200GR4] = OK

73.10.2 State diagram timers

Change the link_fault_inhibit timer definition as follows:

link_fail_inhibit_timer

Timer for qualifying a link_status=FAIL indication or a link_status=OK indication when a specific technology link is first being established. A link will only be considered "failed" if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire within the timer values given in Table 73–7 ~~40 ms to 50 ms~~ after entering the AN LINK GOOD CHECK state ~~when the link is 1000BASE-KX or 10GBASE-KX4. Otherwise the The link_fail_inhibit_timer shall expire 500 ms to 510 ms after entering the AN LINK GOOD CHECK state~~.

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Change Table 73–7 (as modified by IEEE Std 802.3cb-201x) as follows:

Table 73–7—Timer min/max value summary

Parameter	Min	Value and tolerance	Max	Units
autoneg_wait_timer	25		50	ms
break_link_timer	60		75	ms
clock_detect_min_timer	4.8		6.2	us
clock_detect_max_timer	6.6		8.0	ns
data_detect_min_timer	1.6		3.0	ns
data_detect_max_timer	3.4		4.8	ns
interval_timer		3.2 ± 0.01%		ns
link_fail_inhibit_timer (when the link is 50GBASE-KR, 50GBASE-CR, 100GBASE-KR2, 100GBASE-CR2, 200GBASE-KR4 or 200GBASE-CR4)	1.6		1.7	s
link_fail_inhibit_timer (when the link is 10GBASE-KR, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, 25GBASE-CR-S, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-KR4, 100GBASE-KP4, 100GBASE-CR4, or 100GBASE-CR10 ~~neither 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, nor 10GBASE-KX4~~)	500		510	ms
link_fail_inhibit_timer (when the link is 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, or 10GBASE-KX4)	40		50	ms
page_test_min_timer	305		330	ns
page_test_max_timer	350		375	ns

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73.11 Protocol implementation conformance statement (PICS) proforma for Clause 73, Auto-Negotiation for backplane and copper cable assembly[2]

73.11.4 PICS proforma tables for Auto-Negotiation for backplane and copper cable assembly

73.11.4.3 Link codeword encoding

Change table to delete PICS item LE18 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
~~LE18~~	~~Incompatible abilities~~	~~73.6.4~~	~~PHYs for operation over electrical backplane are not simultaneously advertised with PHYs for operation over copper cable~~	~~M~~	~~Yes [ ]~~

73.11.4.7 State diagrams and variable definitions

Change Table (as modified by IEEE Std 802.3cb-201x) as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
SD15	link_fail_inhibit_timer	73.10.2	The values in Table 73–7~~500 to 510 ms when the link is not 1000BASE-KX, 2.5GBASE-X, 5GBASE-R or 10GBASE-KX4 and 40 ms to 50 ms otherwise~~	M	Yes [ ]

[2]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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78. Energy-Efficient Ethernet (EEE)

78.1 Overview

78.1.4 PHY types optionally supporting EEE

Change Table 78–1 (as modified by IEEE Std 802.3bs-201x) as follows (some unmodified rows not shown):

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
…	…
40GBASE-ER4[b]	82, 83, 87
50GBASE-KR[b]	133, 134, 137
50GBASE-CR[b]	133, 134, 136
50GBASE-SR[b]	133, 134, 138
50GBASE-FR[b]	133, 134, 139
50GBASE-LR[b]	133, 134, 139
CAUI-4[a]	83D
100GBASE-KP4	82, 91, 94
100GBASE-KR4	82, 83, 91, 93
100GBASE-KR2[b]	82, 135, 137
100GBASE-CR10	82, 83, 85, 74
100GBASE-CR4	82, 83, 91, 92
100GBASE-CR2[b]	82, 135, 136
100GBASE-SR10[b]	82, 83, 86
100GBASE-SR4[b]	82, 83, 91, 95
100GBASE-SR2[b]	82, 135, 138
100GBASE-DR[b]	82, 135, 140
100GBASE-LR4[b]	82, 83, 88
100GBASE-ER4[b]	82, 83, 88
200GBASE-KR4[b]	119, 120, 137
200GBASE-CR4[b]	119, 120, 136
200GBASE-SR4[b]	119, 120, 138
200GBASE-DR4[b]	119, 120, 121
…	…

[a]25GAUI/XLAUI/CAUI-n shutdown is supported only when deep sleep is enabled for the associated PHY.
[b]The deep sleep mode of EEE is not supported for this PHY.

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78.5 Communication link access latency

Insert new row into Table 78–4 below the row for 40GBASE-KR4 (unmodified rows not shown):

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy\_shrink\_tx}$ (max) (μs)	$T_{phy\_shrink\_rx}$ (max) (μs)	$T_{w\_sys\_rx}$ (min) (μs)
…	…	…	…	…	…	…
50GBASE-R fast wake		0.34	0.3	0	0	0.25
…	…	…	…	…	…	…

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80. Introduction to 40 Gb/s and 100 Gb/s networks

80.1 Overview

80.1.3 Relationship of 40 Gigabit and 100 Gigabit Ethernet to the ISO OSI reference model

Change the second paragraph in 80.1.3 as follows:

While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The XLGMII and CGMII, which, when implemented as a logical interconnection port between the MAC sublayer and the Physical Layer (PHY), uses a 64-bit wide data path as specified in Clause 81.

b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.

c) The PMA service interface, which, when physically implemented as XL (40 Gb/s Attachment Unit Interface) or CAUI-4 and 100GAUI-4 (100 Gb/s four-lane Attachment Unit Interface) at an observable interconnection port, uses a 4 lane data path as specified in Annex 83A, Annex 83B, Annex 83D, or Annex 83E.

d) The PMA service interface, which, when physically implemented as CAUI-10 (100 Gb/s ten-lane Attachment Unit Interface) at an observable interconnection port, uses a 10 lane data path as specified in Annex 83A or Annex 83B.

e) The PMA service interface, which, when physically implemented as 100GAUI-2 (100 Gb/s two-lane Attachment Unit Interface) at an observable interconnection port, uses a 2-lane data path as specified in Annex 135F or Annex 135G.

f) The PMD service interface, which, when physically implemented as XLPPI (40 Gb/s Parallel Physical Interface) at an observable interconnection port, uses a 4 lane data path as specified in Annex 86A.

g) The PMD service interface, which, when physically implemented as CPPI (100 Gb/s Parallel Physical Interface) at an observable interconnection port, uses a 10 lane data path as specified in Annex 86A.

h) The MDIs as specified in Clause 89 for 40GBASE-FR and Clause 140 for 100GBASE-DR uses a single lane data path.

i) The MDIs as specified in Clause 85 for 40GBASE-CR4, in Clause 86 for 40GBASE-SR4, in Clause 87 for 40GBASE-LR4 and 40GBASE-ER4, in Clause 88 for 100GBASE-LR4 and 100GBASE-ER4, in Clause 92 for 100GBASE-CR4, and in Clause 95 for 100GBASE-SR4 all use a 4 lane data path.

j) The MDIs as specified in Clause 85 for 100GBASE-CR10, and in Clause 86 for 100GBASE-SR10 use a 10 lane data path.

k) Although there is no electrical or mechanical specification of the MDI for backplane Physical Layers, the PMDs as specified in Clause 84 for 40GBASE-KR4, in Clause 93 for 100GBASE-KR4, and in Clause 94 for 100GBASE-KP4 all use a 4 lane data path.

l) The MDIs as specified in Clause 136 for 100GBASE-CR2, in Clause 137 for 100GBASE-KR2, and in Clause 138 for 100GBASE-SR2 all use a 2-lane data path.

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80.1.4 Nomenclature

Change Table 80–1 as follows (some unchanged rows not shown):

Table 80–1—40 Gb/s and 100 Gb/s PHYs

Name	Description
…	…
40GBASE-ER4	40 Gb/s PHY using 40GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km (see Clause 87)
100GBASE-KR2	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 4-level pulse amplitude modulation over two lanes of an electrical backplane, with a total insertion loss up to 30 dB at 13.28 GHz (see Clause 137)
100GBASE-KR4	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 2-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 35 dB at 12.9 GHz (see Clause 93)
100GBASE-KP4	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 4-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 33 dB at 7 GHz (see Clause 94)
100GBASE-CR2	100 Gb/s PHY using 100GBASE-R encoding and Clause 91 RS-FEC and 4-level pulse amplitude modulation over two lanes of shielded balanced copper cabling, with reach up to at least 3 m (see Clause 136)
100GBASE-CR4	100 Gb/s PHY using 100GBASE-R encoding and Clause 91 RS-FEC over four lanes of shielded balanced copper cabling, with reach up to at least 5 m (see Clause 92)
100GBASE-CR10	100 Gb/s PHY using 100GBASE-R encoding over ten lanes of shielded balanced copper cabling, with reach up to at least 7 m (see Clause 85)
100GBASE-SR10	100 Gb/s PHY using 100GBASE-R encoding over ten lanes of multimode fiber, with reach up to at least 100 m (see Clause 86)
100GBASE-SR2	100 Gb/s PHY using 100GBASE-R encoding over two lanes of multimode fiber, with reach up to at least 100 m (see Clause 138)
100GBASE-SR4	100 Gb/s PHY using 100GBASE-R encoding over four lanes of multimode fiber, with reach up to at least 100 m (see Clause 95)
100GBASE-DR	100 Gb/s PHY using 100GBASE-R encoding over single-mode fiber, with reach up to at least 500 m (see Clause 140)
100GBASE-LR4	100 Gb/s PHY using 100GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 10 km (see Clause 88)
…	…

80.1.5 Physical Layer signaling systems

Change the first paragraph of 80.1.5 as follows:

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This standard specifies a family of Physical Layer implementations. Table 80–2, Table 80–3, ~~and~~ Table 80–4, and Table 80–4a specify the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures must meet the requirements of the corresponding clauses.

Change Table 80–3 as follows:

Table 80–3—Nomenclature and clause correlation (100GBASE copper)

Nomenclature	Clause[a]																			
	73	74	78	81		82	83	83A	83B	86	91	92	93	94	135	135D	135F	136	137
	Auto-Negotiation	BASE-R FEC	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10	CAUI-4	100GBASE-CR10 PMD	RS-FEC	100GBASE-CR4 PMD	100GBASE-KR4 PMD	100GBASE-KP4 PMD	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-2 C2C	100GBASE-CR2	100GBASE-KR2
100GBASE-KR2	M		O	M	O	M		O	O		M				M	O	O		M
100GBASE-KR4	M		O	M	O	M	M	O	O		M		M						
100GBASE-KP4	M		O	M	O	M	O	O	O		M			M					
100GBASE-CR2	M		O	M	O	M		O	O		M				M	O	O	M	
100GBASE-CR4	M		O	M	O	M	M	O	O		M	M							
100GBASE-CR10	M	O	O	M	O	M	M	O	O	M									

[a]O = Optional, M = Mandatory.

Change the title of Table 80–4 as follows:

Table 80–4—Nomenclature and clause correlation (100GBASE-R optical)

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Insert Table 80–4a after Table 80–4 as follows:

Table 80–4a—Nomenclature and clause correlation (100GBASE-P optical)

Nomenclature	Clause[a]															
	78	81		83	83A	83B	83D	83E	91	135	135D	135E	135F	135G	138	140
	EEE	RS	CGMII	100GBASE-R PMA	CAUI-10	CAUI-10	CAUI-4	CAUI-4	RS-FEC	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-4 C2M	100GAUI-2 C2C	100GAUI-2 C2M	100GBASE-SR2	100GBASE-DR
100GBASE-SR2	O	M	O	O	O	O	O	O	M	M	O	O	O	O	M	
100GBASE-DR	O	M	O	O	O	O	O	O	M	M	O	O	O	O		M

[a]O = Optional, M = Mandatory.

80.2 Summary of 40 Gigabit and 100 Gigabit Ethernet sublayers

80.2.1 Physical Coding Sublayer (PCS)

Change the text in 80.2.1 as follows:

The terms 40GBASE-R, 100GBASE-R, and 100GBASE-P refer to a specific family of Physical Layer implementations based upon the 64B/66B data coding method specified in Clause 82 and the PMA specifications defined in Clause 83, ~~or~~ Clause 94, or Clause 135. Clause 82 PCSs perform encoding (decoding) of data from (to) the XLGMII/CGMII to 64B/66B code blocks, distribute the data to multiple lanes, and transfer the encoded data to the PMA.

80.2.3 Forward Error Correction (FEC) sublayers

Change the first paragraph in 80.2.3 as follows:

A Forward Error Correction sublayer ~~is available for all 40GBASE-R and 100GBASE-R copper and backplane PHYs as well as 100GBASE-SR4. It~~ is optional for 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 PHYs and mandatory for 100GBASE-CR2, 100GBASE-CR4, 100GBASE-KR2, 100GBASE-KR4, 100GBASE-KP4, 100GBASE-SR2, ~~and~~ 100GBASE-SR4, and 100GBASE-DR PHYs. The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers.

80.2.4 Physical Medium Attachment (PMA) sublayer

Change the second paragraph of 80.2.4 as follows:

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The 40GBASE-R and 100GBASE-R PMA are specified in Clause 83. The PMA specific to the 100GBASE-KP4 PHY is specified in Clause 94. The PMA for other 100GBASE-P PHYs is specified in Clause 135.

80.2.5 Physical Medium Dependent (PMD) sublayer

Change the second paragraph of 80.2.5 as follows:

The 40GBASE-R, 100GBASE-R, and 100GBASE-P PMDs and their corresponding media are specified in Clause 84 through Clause 89, ~~and~~ Clause 92 through Clause 95, Clause 136 through Clause 138, and Clause 140.

80.2.6 Auto-Negotiation

Change the second paragraph of 80.2.6 as follows:

Clause 73 Auto-Negotiation is used by the 40 Gb/s and 100 Gb/s backplane PHYs (40GBASE-KR4, 100GBASE-KR2, 100GBASE-KP4, and 100GBASE-KR4) and the 40 Gb/s and 100 Gb/s copper PHYs (40GBASE-CR4, 100GBASE-CR2, 100GBASE-CR10, and 100GBASE-CR4).

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80.4 Delay constraints

Change Table 80–5 as follows (some unchanged rows not shown):

Table 80–5—Sublayer delay constraints

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
…	…	…	…	…
100GBASE-R PMA	9216	18	92.16	See 83.5.4.
100GBASE-P PMA	9216	18	92.16	See 135.5.4.
100GBASE-KR2 PMD	4096	8	40.96	Includes allocation of 20 ns for one direction through backplane medium. See 137.5.
100GBASE-KR4 PMD	2048	4	20.48	Includes delay of one direction through backplane medium. See 93.4.
100GBASE-KP4 PMA/PMD	8192	16	81.92	Includes delay of one direction through backplane medium. See 94.2.5.
100GBASE-CR2 PMD	4096	8	40.96	Includes allocation for 20 ns for one direction through cable medium. See 136.5.
100GBASE-CR4 PMD	2048	4	20.48	Does not include delay of cable medium. See 92.4.
100GBASE-CR10 PMD	9728	19	97.28	Does not include delay of cable medium. See 85.4.
100GBASE-SR2 PMD	2048	4	20.48	Includes 2 m of fiber. See 138.3.
100GBASE-SR4 PMD	2048	4	20.48	Includes 2 m of fiber. See 95.3.3.
100GBASE-SR10 PMD	2048	4	20.48	Includes 2 m of fiber. See 86.3.1.
100GBASE-DR PMD	2048	4	20.48	Includes 2 m of fiber. See 140.3.
100GBASE-LR4 PMD	2048	4	20.48	Includes 2 m of fiber. See 88.3.1.
100GBASE-ER4 PMD	2048	4	20.48	Includes 2 m of fiber. See 88.3.1.

[a] For 40GBASE-R, 1 bit time (BT) is equal to 25 ps and for 100GBASE-R, 1 bit time (BT) is equal to 10 ps. (See 1.4.117 for the definition of bit time.)

[b] For 40GBASE-R, 1 pause_quantum is equal to 12.8 ns and for 100GBASE-R, 1 pause_quantum is equal to 5.12 ns. (See 31B.2 for the definition of pause_quanta.)

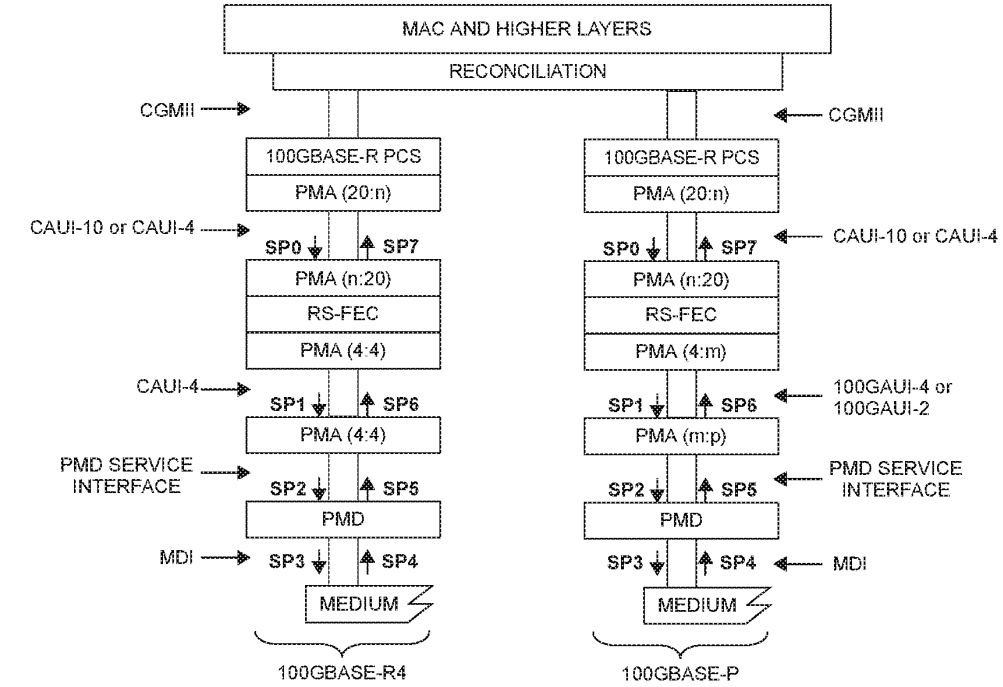
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

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80.5 Skew constraints

Replace Figure 80–8 with the following figure:



100GAUI-2 = 100 Gb/s TWO-LANE ATTACHMENT UNIT INTERFACE
100GAUI-4 = 100 Gb/s FOUR-LANE FEC-RATE ATTACHMENT UNIT INTERFACE
CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
m = 2 or 4
n = 4 or 10
p = 1 or 2

Figure 80–8—100GBASE-R Skew points with RS-FEC, CAUI-n, and 100GAUI-n

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Change Table 80–6 as follows (table footnotes not shown):

Table 80–6—Summary of Skew constraints

Skew points	Maximum Skew (ns)	Maximum Skew for 40GBASE-R PCS lane (UI)	Maximum Skew for 100GBASE-R PCS lane (UI)	Notes
SP0	29	N/A	≈ 150	See 83.5.3.1 or 135.5.3
SP1	29	≈ 299	≈ 150	See 83.5.3.2 or 135.5.3
SP2	43	≈ 443	≈ 222	See 83.5.3.4, 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP3	54	≈ 557	≈ 278	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP4	134	≈ 1382	≈ 691	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP5	145	≈ 1495	≈ 748	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP6	160	≈ 1649	≈ 824	See 83.5.3.6 or 135.5.3
SP7	29	N/A	≈ 150	See 83.5.3.8 or 135.5.3
At PCS receive	180	≈ 1856	≈ 928	See 82.2.13
At RS-FEC transmit	49	N/A	≈ 253	See 91.5.2.2
At RS-FEC receive	180	N/A	≈ 4641	See 91.5.3.3
At PCS receive (with RS-FEC)	49	N/A	≈ 253	See 82.2.13

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Change Table 80–7 as follows (table footnotes not shown):

Table 80–7—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation (ns)	Maximum Skew Variation for 10.3125 GBd PMD lane (UI)	Maximum Skew Variation for 25.78125 GBd PMD lane (UI)	Notes
SP0	0.2	≈ 2	N/A	See 83.5.3.1 or 135.5.3
SP1	0.2	≈ 2	N/A	See 83.5.3.2 or 135.5.3
SP2	0.4	≈ 4	≈ 10	See 83.5.3.4, 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP3	0.6	≈ 6	≈ 15	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 136.6, 137.6, 138.3, or 140.4
SP4	3.4	≈ 35	≈ 88	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 136.6, 137.6, 138.3, or 140.4
SP5	3.6	≈ 37	≈ 93	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP6	3.8	≈ 39	≈ 98	See 83.5.3.6 or 135.5.3
SP7	0.2	≈ 2	N/A	See 83.5.3.8 or 135.5.3
At PCS receive	4	≈ 41	N/A	See 82.2.13
At RS-FEC transmit	0.4	N/A	≈ 10	See 91.5.2.2
At RS-FEC receive	4	N/A	≈ 103	See 91.5.3.1
At PCS receive (with RS-FEC)	0.4	N/A	≈ 10	See 82.2.13

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82. Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R

82.6 Auto-Negotiation

Change the paragraph in 82.6 as follows:

The following requirements apply to a PCS used with a 40GBASE-KR4 PMD, 40GBASE-CR4 PMD, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-KR4, ~~or~~ 100GBASE-KP4, or 100GBASE-KR2 PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

82.7 Protocol implementation conformance statement (PICS) proforma for Clause 82, Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R

82.7.4 PICS Proforma Tables for PCS, type 40GBASE-R and 100GBASE-R

Change the heading number of 82.7.5 "Test-pattern modes" to 82.7.4.5 as follows:

82.7.4.5 Test-pattern modes

Change the heading number of 82.7.6 "Management" to 82.7.4.7 as follows:

82.7.4.7 Management

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82.7.4.11 Auto-Negotiation for Backplane Ethernet functions

Change the table in 82.7.6.4 (renumbered as 82.7.4.11) as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
*AN1	Support for use with a 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-KR4, ~~or~~ 100GBASE-KP4, or 100GBASE-KR2 PMD	82.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN2	AN_LINK.indication primitive	82.6	Support of the primitive AN_LINK.indication(link_status); ~~when the PCS is used with 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-KR4, or 100GBASE-KP4 PMD~~	AN1:M	Yes [ ] N/A [ ]
AN3	link_status parameter	82.6	Takes the value OK or FAIL, as described in 82.6	AN1:M	Yes [ ] N/A [ ]
AN4	Generation of AN_LINK.indication primitive	82.6	Generated when the value of link_status changes	AN1:M	Yes [ ] N/A [ ]

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90. Ethernet support for time synchronization protocols

90.1 Introduction

Change the first paragraph of 90.1 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

The TSSI is defined for the full-duplex mode of operation only. It supports MAC operation at various data rates. The MII (Clause 22), GMII (Clause 35), XGMII (Clause 46), 25GMII (Clause 106), XLGMII (Clause 81), 50GMII (Clause 132), CGMII (Clause 81), 200GMII (Clause 117), and 400GMII (Clause 117) specifications are all compatible with the gRS sublayer defined in 90.5.

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91. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs

91.5 Functions within the RS-FEC sublayer

91.5.2 Transmit function

91.5.2.6 Alignment marker mapping and insertion

Change the third and fourth paragraphs of 91.5.2.6 as follows:

For x=0 to 19, amp_tx_x<63:0> is constructed as follows:

a) Set y = 0 when $x \leq 3$, set y = 16 when $x \geq 16$ and four_lane_pmd, otherwise set $y = x$.
b) amp_tx_x<23:0> is set to M_0, M_1, and M_2 as shown in Figure 82–9 (bits 25 to 2) using the values in Table 82–2 for PCS lane number y. If am_tx_x corresponds to a Rapid Alignment marker, then the M_4, M_5, and M_6 values are used instead (see Figure 82–11).
c) amp_tx_x<31:24> = am_tx_x<33:26>
d) amp_tx_x<55:32> is set to M_4, M_5, and M_6 as shown in Figure 82–9 (bits 57 to 34) using the values in Table 82–2 for PCS lane number y. If am_tx_x corresponds to a Rapid Alignment marker, then the M_0, M_1, and M_2 values are used instead (see Figure 82–11).
e) amp_tx_x<63:56> = am_tx_x<65:58>

This process replaces the fixed bytes of the alignment markers received, possibly with errors, with the values from Table 82–2. In addition it substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 1, 2, and 3 with the fixed bytes for the alignment marker corresponding to PCS lane 0. Similarly when used with a four-lane PMD, it substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16. The variable bytes BIP or CD are unchanged. This process simplifies receiver synchronization since the receiver only needs to search for the fixed bytes corresponding to PCS lane 0 on each FEC lane. When the optional EEE deep sleep capability is supported, the receiver only needs to search for the fixed bytes corresponding to PCS lanes 0 and 16.

91.5.2.7 Reed-Solomon encoder

Change the second sentence of the second paragraph of 91.5.2.7 as follows:

When used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR PHY, the RS-FEC sublayer shall implement RS(544,514).

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91.5.3 Receive function

91.5.3.1 Alignment lock and deskew

Replace Figure 91–8 with the following:

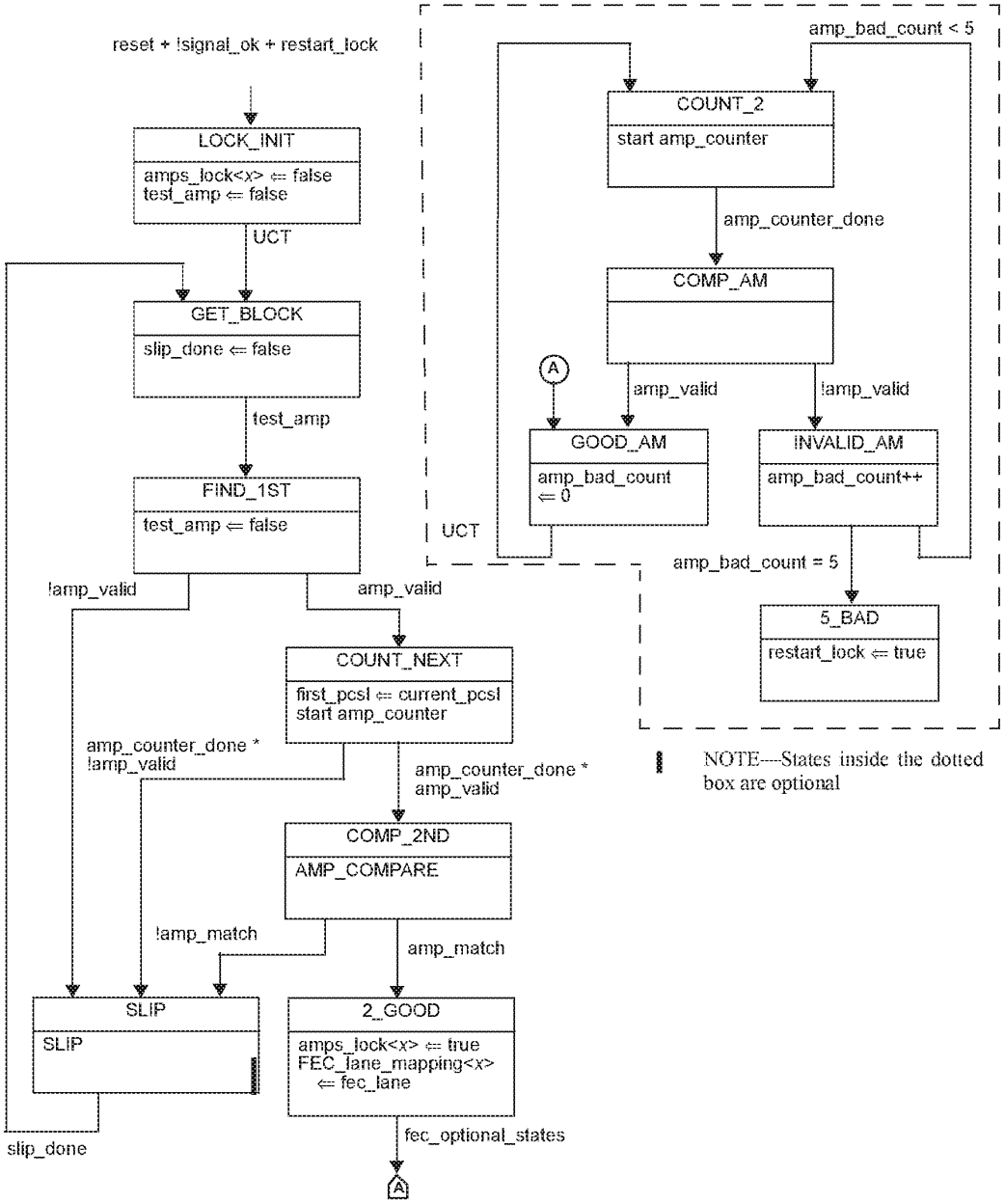


Figure 91–8—FEC synchronization state diagram

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91.5.3.3 Reed-Solomon decoder

Change the second sentence of the second paragraph of 91.5.3.3 as follows:

When used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword.

Change the last sentence of 91.5.3.3 as follows:

When the RS-FEC sublayer used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR PHY, the symbol error threshold shall be K=6380.

91.5.4 Detailed functions and state diagrams

91.5.4.2 State variables

91.5.4.2.1 Variables

Change restart_lock definition as follows:

restart_lock
: Boolean variable that is set by the FEC alignment process to reset the synchronization process on all FEC lanes. It is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) and set to false upon entry into the LOSS_OF_ALIGNMENT state. It is also set to true when 5 Alignment Markers in a row fail to match (5_BAD state) if the optional states are supported in the FEC synchronization process.

Insert fec_optional_states definition after fec_lane as follows:

fec_optional_states
: Boolean variable that is true if the optional states are implemented and false otherwise.

91.5.4.2.3 Counters

Insert new counter amp_bad_count before amp_counter as follows:

amp_bad_count
: Counts the number of consecutive alignment markers that don't match the expected values for a given FEC lane if the optional states are supported in the FEC synchronization process.

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91.6 RS-FEC MDIO function mapping

Change Table 91–2 as follows:.

Table 91–2—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass correction enable	RS-FEC control register	1.200.0	FEC_bypass_correction_enable
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable
Four lane PMD	RS-FEC control register	1.200.3	four_lane_pmd

Insert new row in Table 91–3 after "RS-FEC high SER" row as follows:.

Table 91–3—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
…	…	…	…
FEC optional states supported	RS-FEC status register	1.201.7	fec_optional_states

Insert 91.6.2a after 91.6.2 as follows:

91.6.2a four_lane_pmd

When this variable is set to one, the alignment marker mapping function substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16 (see 91.5.2.6). When this variable is set to zero, the alignment markers corresponding to PCS lanes 17, 18, and 19 are passed through unmodified. The default value of the variable is one which is the value required by the 100GBASE-CR4, 100GBASE-KR4, 100GBASE-KP4, and 100GBASE-SR4 PMDs. This variable is set to zero for the 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, and 100GBASE-DR PMDs. This variable is mapped to the bit defined in 45.2.1.101 (1.200.3).

Insert 91.6.5a after 91.6.5 as follows:

91.6.5a FEC_optional_states

This variable is set to true when the optional states in the FEC synchronization state diagram are implemented.

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91.7 Protocol implementation conformance statement (PICS) proforma for Clause 91, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs[3]

91.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs

91.7.4.1 Transmit function

Change PICS item TF11 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
...	...	...	...	...	...
TF11	Reed-Solomon encoder for 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR	91.5.2.7	RS(544,514)	KP4:M	Yes [ ] N/A [ ]

91.7.4.3 State diagrams

Insert new PICS item SD6 after SD5 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
...	...	...	...	...	...
SD6	FEC synchronization enhancement	91.5.4.3	Check AMs after synchronization is achieved per Figure 91–8	O	Yes [ ] No [ ]

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116. Introduction to 200 Gb/s and 400 Gb/s networks

116.1 Overview

116.1.2 Relationship of 200 Gigabit and 400 Gigabit Ethernet to the ISO OSI reference model

Change item h as follows:

h) The MDIs as specified in Clause 121 for 200GBASE-DR4, in Clause 122 for 200GBASE-FR4 and 200GBASE-LR4, and in Clause 124 for 400GBASE-DR4, Clause 136 for 200GBASE-CR4, Clause 137 for 200GBASE-KR4, and Clause 138 for 200GBASE-SR4, all use a 4-lane data path.

116.1.3 Nomenclature

Change Table 116-1 as shown (some unchanged rows not shown):

Table 116–1—200 Gb/s PHYs

Name	Description
200GBASE-KR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of an electrical backplane (see Clause 137)
200GBASE-CR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of twinaxial copper cable (see 1.4.407 and Clause 136)
200GBASE-SR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of multimode fiber (see Clause 138)
200GBASE-DR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of single-mode fiber, with reach up to at least 500 m (see Clause 121)
...	...

116.1.4 Physical Layer signaling systems

Change the first paragraph in 116.1.4 as follows:

This standard specifies a family of Physical Layer implementations. Table 116–2a, Table 116–3, and Table 116–4 specify the correlation between PHY types and clauses. Implementations conforming to one or more PHY types must meet the requirements of the corresponding clauses.

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Insert Table 116-2a as shown:

Table 116–2a—PHY type and clause correlation (200GBASE copper)

PHY type	Clause[a]								
	78	117		119	120	120B	120D	136	137
	EEE	RS	200GMII	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-4 C2C	200GBASE-CR4 PMD	200GBASE-KR4 PMD
200GBASE-KR4	O	M	O	M	M	O	O		M
200GBASE-CR4	O	M	O	M	M	O	O	M	

[a]O = Optional, M = Mandatory.

Change Table 116-3 as shown:

Table 116–3—PHY type and clause correlation (200GBASE optical)

PHY type	Clause[a]											
	78	117		119	120	120B	120C	120D	120E	121	122	122	138
	EEE	RS	200GMII	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-8 C2M	200GAUI-4 C2C	200GAUI-4 C2M	200GBASE-DR4 PMD	200GBASE-FR4 PMD	200GBASE-LR4 PMD	200GBASE-SR4 PMD
200GBASE-SR4	O	M	O	M	M	O	O	O	O				M
200GBASE-DR4	O	M	O	M	M	O	O	O	O	M			
200GBASE-FR4	O	M	O	M	M	O	O	O	O		M		
200GBASE-LR4	O	M	O	M	M	O	O	O	O			M	

[a]O = Optional, M = Mandatory.

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116.2 Summary of 200 Gigabit and 400 Gigabit Ethernet sublayers

116.2.5 Physical Medium Dependent (PMD) sublayer

Change the second paragraph in 116.2.5 as shown:

The 200GBASE-R PMDs and their corresponding media are specified in Clause 121, ~~and~~ Clause 122, and Clause 136 through Clause 138. The 400GBASE-R PMDs and their corresponding media are specified in Clause 122 through Clause 124.

116.4 Delay constraints

Change Table 116-5 as shown (some unchanged rows not shown):

Table 116–5—Sublayer delay constraints (200GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
…	…	…	…	…
200GBASE-R PMA	18 432	36	92.16	See 120.5.4.
200GBASE-KR4 PMD	8 192	16	40.96	Includes allocation of 20 ns for one direction through backplane medium. See 137.5.
200GBASE-CR4 PMD	8 192	16	40.96	Includes allocation of 20 ns for one direction through cable medium. See 137.5.
200GBASE-SR4 PMD	4 096	8	20.48	See 138.3.
200GBASE-DR4 PMD	4 096	8	20.48	Includes 2 m of fiber. See 121.3.1.
…	…	…	…	…

[a]For 200GBASE-R, 1 bit time (BT) is equal to 5 ps. (See 1.4.117 for the definition of bit time.)
[b]For 200GBASE-R, 1 pause_quantum is equal to 2.56 ns. (See 31B.3 for the definition of pause_quanta.)
[c]Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

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119. Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R

Insert new subclause 119.6 after subclause 119.5 as follows:

119.6 Auto-Negotiation

The following requirements apply to a PCS used with a 200GBASE-CR4 or 200GBASE-KR4 PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the AN_LINK.indication(link_status) primitive (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

119.7 Protocol implementation conformance statement (PICS) proforma for Clause 119, Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R

119.7.4 PICS proforma tables for Physical Coding Sublayer (PCS) 64B/66B, type 200GBASE-R and 400GBASE-R

Insert new subclause 119.7.4.12 after subclause 119.6.4.11 as follows:

119.7.4.12 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Support for use with a 200GBASE-CR4 or 200GBASE-KR4 PMD	119.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN1	AN_LINK.indication primitive	119.6	Support of the AN_LINK.indication(link_status) primitive	AN:M	Yes [ ] N/A [ ]
AN2	link_status parameter	119.6	Takes the value OK or FAIL, as described in 119.6	AN:M	Yes [ ] N/A [ ]
AN3	Generation of AN_LINK.indication primitive	119.6	Generated when the value of link_status changes	AN:M	Yes [ ] N/A [ ]

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120. Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R

120.5 Functions within the PMA

Insert new heading 120.5.7 and change heading number 120.5.7 to 120.5.7.1 as follows:

120.5.7 PAM4 Encoding

120.5.7.1 Gray coding for PAM4 encoded lanes

Insert new subclause 120.5.7.2 as follows:

120.5.7.2 Precoding for PAM4 encoded lanes

A PMA adjacent to a 200GBASE-CR4 or 200GBASE-KR4 PMD, shall provide 1/(1+D) mod 4 precoding capability on all transmit lanes and may optionally provide 1/(1+D) mod 4 decoding capability on all receive lanes on the PMD service interface. Precoding is implemented as specified in 135.5.7.2.

The precoder is enabled independently for the transmitter and receiver on each lane (0, 1, 2, and 3). Precoding is enabled and disabled using variables precoder_down_tx_enable_*i* and precoder_down_rx_enable_*i* (where *i* is 0, 1, 2, or 3).

If a Clause 45 MDIO is implemented, the variables precoder_down_tx_enable_*i* and precoder_down_rx_enable_*i* are accessible through register 1.600 and 1.601 (see 45.2.1.116h and 45.2.1.116i).

The variables precoder_down_tx_enable_*i* and precoder_down_rx_enable_*i* are always set to 0 in a PMA that is not adjacent to a 200GBASE-CR4 or 200GBASE-KR4 PMD.

The variables precoder_down_tx_enable_*i* and precoder_down_rx_enable_*i* shall be set as determined by the PMD control function on lane *i* (see 136.8.11.7.5). The method by which the PMD control function affects these variables is implementation dependent.

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120.6 PMA MDIO function mapping

Change Table 120–1 as shown (some unchanged rows not shown):

Table 120–1—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PMA remote loopback	PMA/PMD control 1	1.0.1	Remote_loopback_enable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
Lane 0 down transmitter precoder enable	PMA precoder control down Tx	1.600.0	precoder_down_tx_enable_0
Lane 1 down transmitter precoder enable	PMA precoder control down Tx	1.600.1	precoder_down_tx_enable_1
Lane 2 down transmitter precoder enable	PMA precoder control down Tx	1.600.2	precoder_down_tx_enable_2
Lane 3 down transmitter precoder enable	PMA precoder control down Tx	1.600.3	precoder_down_tx_enable_3
Lane 0 down receiver precoder enable	PMA precoder control down Rx	1.601.0	precoder_down_rx_enable_0
Lane 1 down receiver precoder enable	PMA precoder control down Rx	1.601.1	precoder_down_rx_enable_1
Lane 2 down receiver precoder enable	PMA precoder control down Rx	1.601.2	precoder_down_rx_enable_2
Lane 3 down receiver precoder enable	PMA precoder control down Rx	1.601.3	precoder_down_rx_enable_3
PRBS31 pattern enable	PRBS pattern testing control	1.1501.7	PRBS31_enable
…	…	…	…

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120.7 Protocol implementation conformance statement (PICS) proforma for Clause 120, Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R[4]

Insert new subclause 120.7.7 as follows:

120.7.7 Encoding

Item	Feature	Subclause	Value/Comment	Status	Support
*CKR4	PMA is adjacent to a 200GBASE-CR4 or 200GBASE-KR4 PMD.	120.5.7.2		O	Yes [ ] No [ ]
E1	PMA supports Tx precoding	120.5.7.2		CKR4:M	Yes [ ] N/A [ ]
E2	PMA supports Rx precoding	120.5.7.2		CKR4:O	Yes [ ] No [ ] N/A [ ]

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Insert Clause 131 to Clause 140 as follows:

131. Introduction to 50 Gb/s networks

131.1 Overview

131.1.1 Scope

This clause describes the general requirements for 50 Gigabit Ethernet.

50 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 50 Gb/s, coupled with any IEEE 802.3 50GBASE Physical Layer implementation and is defined for full duplex operation only.

50 Gb/s Physical Layer entities, such as those specified in Table 131–1, provide a frame loss ratio (see 1.4.223) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

131.1.2 Relationship of 50 Gigabit Ethernet to the ISO OSI reference model

50 Gigabit Ethernet couples the IEEE 802.3 MAC to a family of 50 Gb/s Physical Layers. The relationships among 50 Gigabit Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 131–1.

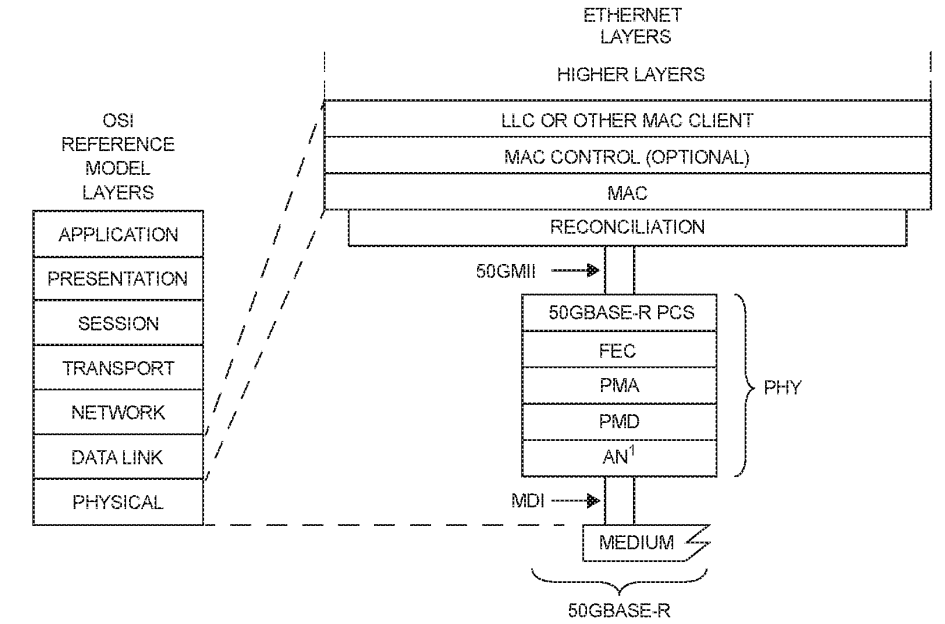


Figure 131–1—Architectural positioning of 50 Gigabit Ethernet

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While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The 50GMII, which, when implemented as logical interconnection point between the MAC sublayer and the Physical Layer (PHY), uses a 64-bit wide data path as specified in Clause 132. Physical instantiations of this interface may use other data-path widths.

b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.

c) The PMA service interface, which, when physically implemented as LAUI-2, as specified in Annex 135B and Annex 135C, or as 50GAUI-2 (50 Gb/s two-lane Attachment Unit Interface), as specified in Annex 135D and Annex 135E, at an observable interconnection port, uses a 2-lane data path.

d) The PMA service interface, which, when physically implemented as 50GAUI-1 (50 Gb/s one-lane Attachment Unit Interface) at an observable interconnection port, uses a 1-lane data path as specified in Annex 135F or Annex 135G.

e) The MDI as specified in Clause 136 for 50GBASE-CR, Clause 137 for 50GBASE-KR, Clause 138 for 50GBASE-SR, and Clause 139 for 50GBASE-FR and 50GBASE-LR use a 1-lane data path.

131.1.3 Nomenclature

The nomenclature employed by the 50 Gb/s Physical Layer is explained as follows.

The alpha-numeric prefix 50GBASE in the port type (e.g., 50GBASE-R) represents a family of Physical Layer devices operating at a speed of 50 Gb/s.

50GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) for 50 Gb/s operation over multiple PCS lanes (see Clause 133). Physical Layer devices listed in Table 131–1 are defined for operation at 50 Gb/s.

Table 131–1—50 Gb/s PHYs

Name	Description
50GBASE-KR	50 Gb/s PHY using 50GBASE-R encoding over an electrical backplane (see Clause 137).
50GBASE-CR	50 Gb/s PHY using 50GBASE-R encoding over twinaxial copper cable (see 1.4.407 and Clause 136).
50GBASE-SR	50 Gb/s PHY using 50GBASE-R encoding over multimode fiber (see Clause 138).
50GBASE-FR	50 Gb/s PHY using 50GBASE-R encoding over single-mode fiber, with reach up to at least 2 km (see Clause 139).
50GBASE-LR	50 Gb/s PHY using 50GBASE-R encoding over single-mode fiber, with reach up to at least 10 km (see Clause 139).

131.1.4 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. Table 131–2 and Table 131–3 specify the correlation between PHY types and clauses. Implementations conforming to one or more PHY types must meet the requirements of the corresponding clauses.

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Table 131–2—PHY types and clause correlation (50GBASE copper)

PHY type	Clause[a]											
	78	132		133	134	135	135B	135D	135F	136	137
	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	LAUI-2 C2C	50GAUI-2 C2C	50GAUI-1 C2C	50GBASE-CR PMD	50GBASE-KR PMD
50GBASE-KR	O	M	O	M	M	M	O	O	O		M
50GBASE-CR	O	M	O	M	M	M	O	O	O	M	

[a]O = Optional, M = Mandatory.

Table 131–3—PHY types and clause correlation (50GBASE optical)

PHY type	Clause[a]														
	78	132		133	134	135	135B	135C	135D	135E	135F	135G	138	139	
	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	LAUI-2 C2C	LAUI-2 C2M	50GAUI-2 C2C	50GAUI-2 C2M	50GAUI-1 C2C	50GAUI-1 C2M	50GBASE-SR PMD	50GBASE-FR PMD	50GBASE-LR PMD
50GBASE-SR	O	M	O	M	M	M	O	O	O	O	O	O	M		
50GBASE-FR	O	M	O	M	M	M	O	O	O	O	O	O		M	
50GBASE-LR	O	M	O	M	M	M	O	O	O	O	O	O			M

[a]O = Optional, M = Mandatory.

131.2 Summary of 50 Gigabit Ethernet sublayers

131.2.1 Reconciliation Sublayer (RS) and Media Independent Interface (50GMII)

The Media Independent Interface specified in Clause 132 provides a logical interconnection between the MAC sublayer and Physical Layer entities (PHY). The Media Independent Interface is not intended to be physically instantiated, rather it can logically connect layers within a device.

The 50GMII supports 50 Gb/s operation through its 64-bit-wide transmit and receive data paths. The Reconciliation Sublayer (RS) provides a mapping between the signals provided at the 50GMII and the MAC/PLS service definition.

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While the 50GMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for the physical coding sublayer defined in Clause 133.

131.2.2 Physical Coding Sublayer (PCS)

50GBASE-R PHYs use the PCS specified in Clause 133. The 50GBASE-R PCS performs encoding of data from the 50GMII to 64B/66B code blocks and transfers the encoded data to the PMA (or FEC) and performs decoding of 64B/66B blocks from the PMA (or FEC) and transfers the decoded data to the 50GMII.

131.2.3 Forward Error Correction (FEC) sublayer

50GBASE-R PHYs use the FEC sublayer specified in Clause 134. The FEC sublayer can be placed between the PCS and PMA sublayers or between two PMA sublayers.

131.2.4 Physical Medium Attachment (PMA) sublayer

The 50GBASE-R PMA specified in Clause 135 provides a medium-independent means for the PCS to support the use of a range of physical media.

The 50GBASE-R PMA performs the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface, the mapping of transmit and receive data streams between the FEC and the PMA via the PMA service interface, and the mapping and multiplexing of transmit and receive data streams between the PMA and PMD via the PMD service interface. In addition, the PMA performs retiming of the received data stream when appropriate, optionally provides data loopback at the PMA or PMD service interface, and optionally provides test-pattern generation and checking.

131.2.5 Physical Medium Dependent (PMD) sublayer

The Physical Medium Dependent sublayer is responsible for interfacing to the transmission medium. The PMD is located just above the Medium Dependent Interface (MDI). The MDI, logically subsumed within each PMD subclause, is the actual medium attachment for the various supported media.

The 50GBASE-R PMDs and their corresponding media are specified in Clause 136 through Clause 139.

131.2.6 Management interface (MDIO/MDC)

The optional MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMDs) and Station Management (STA) entities.

131.2.7 Management

Managed objects, attributes, and actions are defined for all 50 Gigabit Ethernet components. These items are defined in Clause 30.

131.3 Service interface specification method and notation

The service interface specification for the 50GBASE-R Physical Layers is as per the definition in 1.2.2. Note that the 50GBASE-R inter-sublayer service interfaces use multiple scalar REQUEST and INDICATION primitives, to indicate the transfer of multiple independent streams of data units, as defined in 131.3.1 through 131.3.3.

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131.3.1 Inter-sublayer service interface

The inter-sublayer service interface is defined in 116.3.1.

131.3.2 Instances of the inter-sublayer service interface

The inter-sublayer interface can be instantiated between different sublayers, hence a prefix notation is defined to identify a specific instance of an inter-sublayer service interface. The following prefixes are defined:

a) PMD:—for primitives issued on the interface between the PMD sublayer and the PMA sublayer called the PMD service interface.

b) PMA:—for primitives issued on the interface between the PMA sublayer and the PCS or the FEC sublayer called the PMA service interface.

c) FEC:—for primitives issued on the interface between the FEC sublayer and the PCS or the PMA sublayer called the FEC service interface.

Examples of inter-sublayer service interfaces for 50GBASE-R with their corresponding instance names are illustrated in Figure 131–2. For example, the primitives for one instance of the inter-sublayer service interface, named the PMD service interface, are identified as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication.

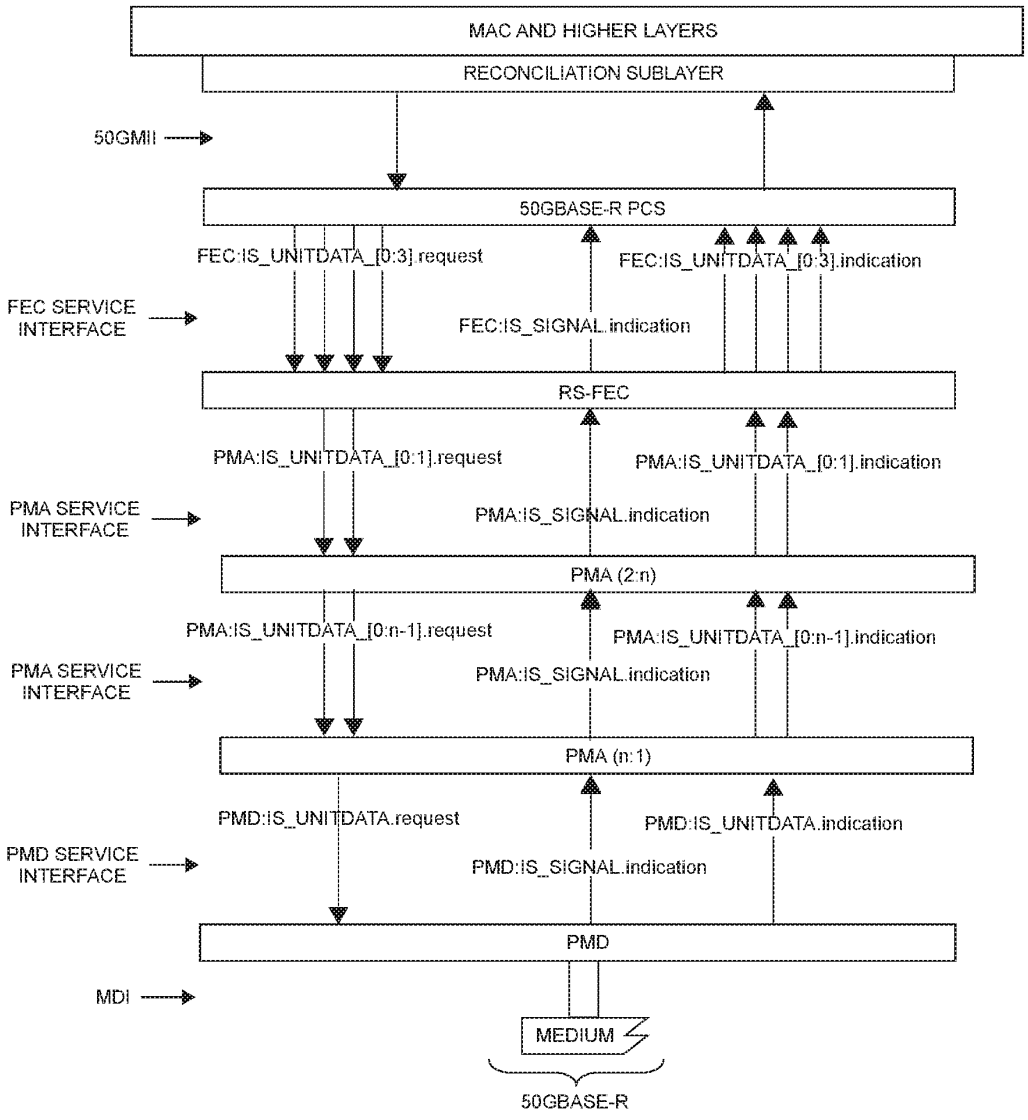
Primitives for other instances, of inter-sublayer interfaces, are represented in a similar manner as described above.

131.3.3 Semantics of inter-sublayer service interface primitives

The semantics of the inter-sublayer service interface primitives for the 50GBASE-R sublayers are described in 116.3.3.1 through 116.3.3.3.

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50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = NUMBER OF PARALLEL STREAMS
n = 1 or 2

Figure 131–2—50GBASE-R inter-sublayer service interfaces

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131.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 131–4 contains the values of maximum sublayer delay (sum of transmit and receive delays at one end of the link) in bit times as specified in 1.4 and pause_quanta as specified in 31B.2 for 50 Gigabit Ethernet. If a PHY contains an Auto-Negotiation sublayer, the delay of the Auto-Negotiation sublayer is included within the delay of the PMD and medium.

Table 131–4—Sublayer delay constraints (50GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
50G MAC, RS, and MAC Control	16 384	32	327.68	See 132.1.4.
50GBASE-R PCS	11 264	22	225.28	See 133.3.
50GBASE-R RS-FEC	25 600	50	512	See 134.4.
50GBASE-R PMA	4 608	9	92.16	See 135.5.4.
50GBASE-KR PMD	2 048	4	40.96	See 137.5. Includes allocation of 20 ns for the medium.
50GBASE-CR PMD	2 048	4	40.96	See 136.5. Includes allocation of 20 ns for the medium.
50GBASE-SR PMD	1 024	2	20.48	Includes 2 m of fiber. See 138.3.1.
50GBASE-FR PMD	1 024	2	20.48	Includes 2 m of fiber. See 139.3.
50GBASE-LR PMD	1 024	2	20.48	Includes 2 m of fiber. See 139.3.

[a]For 50GBASE-R, 1 bit time (BT) is equal to 20 ps. (See 1.4.117 for the definition of bit time.)
[b]For 50GBASE-R, 1 pause_quantum is equal to 10.24 ns. (See 31B.2 for the definition of pause_quanta.)
[c]Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

See 80.4 for the calculation of bit time per meter of fiber or electrical cable.

See 31B.3.7 for PAUSE reaction timing constraints for stations at operating speeds of 50 Gb/s.

131.5 Skew constraints

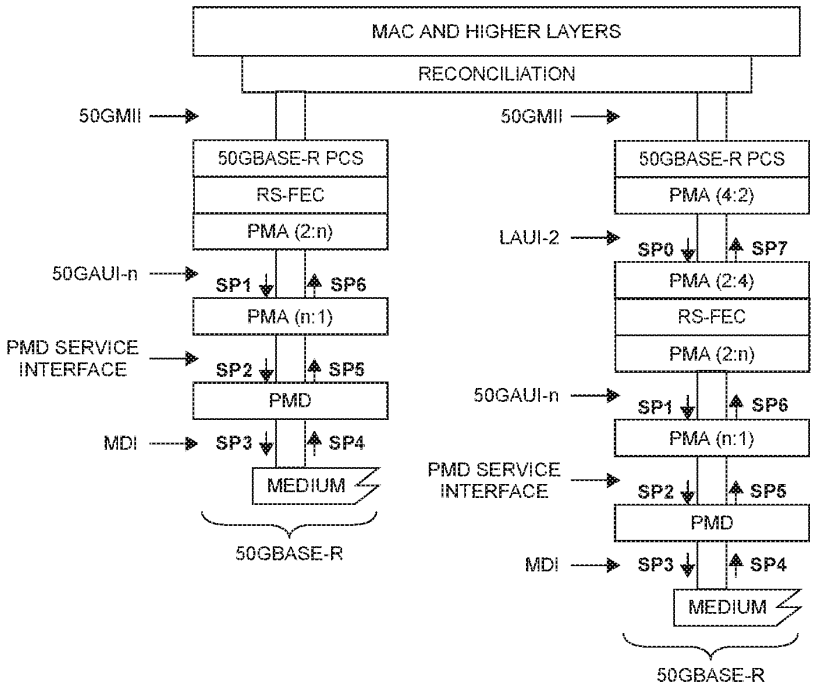
Skew (or relative delay) can be introduced between lanes by both active and passive elements of a 50GBASE-R link. Skew is defined as the difference between the times of the earliest PCS lane and latest PCS lane for the one to zero transition of the alignment marker sync bits. The PCS deskew function (see 133.2.3) compensates for all lane-to-lane Skew observed at the receiver. The Skew between the lanes must be kept within limits as shown in Table 131–5 so that the transmitted information on the lanes can be reassembled by the receive PCS.

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Skew Variation may be introduced due to variations in electrical, thermal or environmental characteristics. Skew Variation is defined as the change in Skew between any PCS lane and any other PCS lane over the entire time that the link is in operation. From the time the link is brought up, Skew Variation must be limited to ensure that each PCS lane always traverses the same lane between any pair of adjacent sublayers while the link remains in operation.

The maximum Skew and Skew Variation at physically instantiated interfaces is specified at Skew points SP0, SP1, SP2, and SP3 for the transmit direction and SP4, SP5, SP6, and SP7 for the receive direction as illustrated in Figure 131–3.



50GAUI-n = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
LAUI-2 = 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = 1 or 2

Figure 131–3—50GBASE-R Skew points

In the transmit direction, the Skew points are defined in the following locations:

- SP0 on the LAUI-2 interface, at the input of the PMA above the RS-FEC;
- SP1 on the 50GAUI-n interface, at the input of the PMA closest to the PMD;
- SP2 on the PMD service interface, at the input of the PMD;
- SP3 at the output of the PMD, at the MDI.

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In the receive direction, the Skew points are defined in the following locations:

— SP4 at the MDI, at the input of the PMD;
— SP5 on the PMD service interface, at the output of the PMD;
— SP6 on the 50GAUI-n interface, at the output of the PMA below to the RS-FEC;
— SP7 on the LAUI-2 interface, at the output of the PMA above the RS-FEC.

The allowable limits for Skew are shown in Table 131–5 and the allowable limits for Skew Variation are shown in Table 131–6.

The Skew requirements for the PCS, PMA and PMD sublayers are specified in the respective clauses as noted in Table 131–5 and Table 131–6.

Table 131–5—Summary of Skew constraints

Skew points	Maximum Skew (ns)[a]	Maximum Skew for 50GBASE-R PCS lane (UI)[b]	Maximum Skew for 50GBASE-R FEC lane (UI)[c]	Notes[d]
SP0	29	≈ 374	—	See 135.5.3.1
SP1	29	—	≈ 771	See 135.5.3.3
SP2	43	—	≈ 1143	See 135.5.3.3, 136.6, 137.6, 138.3.2, 139.3
SP3	54	—	≈ 1435	See 136.6, 137.6, 138.3.2, 139.3
SP4	134	—	≈ 3560	See 136.6, 137.6, 138.3.2, 139.3
SP5	145	—	≈ 3852	See 135.5.3.3, 136.6, 137.6, 138.3.2, 139.3
SP6	160	—	≈ 4250	See 135.5.3.7
SP7	29	≈ 374	—	See 135.5.3.8
At FEC transmit	49	—	≈ 1302	See 134.5.2.2
At FEC receive	180	—	≈ 4782	See 134.5.2.2
At PCS receive	49	≈ 632	—	See 133.2.3

[a]The Skew limit includes 1 ns allowance for PCB traces that are associated with the Skew points.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew in UI based on 1 UI equals 77.5758 ps at PCS lane signaling rate of 12.890625 Gb/s.
[c]The symbol ≈ indicates approximate equivalent of maximum Skew in UI based on 1 UI equals 37.6471 ps at FEC lane signaling rate of 26.5625 Gb/s.
[d]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

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Table 131–6—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation (ns)	Maximum Skew Variation for 25.78125 Gbd lane (UI)[a]	Maximum Skew Variation for 26.5625 Gbd lane (UI)[b]	Notes[c]
SP0	0.2	≈ 6	—	See 135.5.3.1
SP1	0.2	—	≈ 6	See 135.5.3.3
SP2	0.4	—	≈ 11	See 135.5.3.5, 136.6, 137.6, 138.3.2, 139.3
SP3	0.6	—	≈ 16	See 136.6, 137.6, 138.3.2, 139.3
SP4	3.4	—	≈ 91	See 136.6, 137.6, 138.3.2, 139.3
SP5	3.6	—	≈ 96	See 135.5.3.6, 136.6, 137.6, 138.3.2, 139.3
SP6	3.8	—	≈ 101	See 135.5.3.7
SP7	0.2	≈ 6	—	See 135.5.3.8
At FEC transmit	0.4	—	≈ 11	See 134.5.2.2
At FEC receive	4	—	≈ 107	See 134.5.2.2
At PCS receive	0.4	11	—	See 133.2.3

[a]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI based on 1 UI equals 38.7879 ps at LAUI-2 lane signaling rate of 25.78125 GBd.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI based on 1 UI equals 37.6471 ps at 50GAUI-n or PMD lane signaling rate of 26.5625 GBd.
[c]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

131.6 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

Multiple states of a function that have a transition to a common state utilizing different qualifiers (for example, multiple exit conditions to an IDLE or WAIT state) may be indicated by a shared arrow. An exit transition arrow must connect to the shared arrow, and the qualifier must be met prior to termination of the transition arrow on the shared arrow. The shared arrow has no qualifier.

131.7 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 132 through Clause 140, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each

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clause as appropriate. Each of the 50 Gigabit Ethernet PICS conforms to the same notation and conventions used in 21.6.

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132. Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation

132.1 Overview

This clause defines the characteristics of the Reconciliation Sublayer (RS) and the Media Independent Interface between Ethernet media access controllers and various PHYs. Figure 132–1 shows the relationship of the RS and Media Independent Interface to the ISO/IEC OSI reference model. The 50 Gb/s RS has identical logical functionality to the 40 Gb/s RS defined in Clause 81.

The 50GMII is an optional logical interface between the MAC sublayer and the Physical Layer (PHY).

The RS adapts the bit serial protocols of the MAC to the parallel format of the PCS service interface. Though the 50GMII is an optional interface, it is used in this standard as a basis for specification. The Physical Coding Sublayer (PCS) is specified to the 50GMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and 50GMII were implemented.

The 50GMII has the following characteristics:

a) The 50GMII supports a speed of 50 Gb/s.
b) Data and delimiters are synchronous to a clock reference.
c) It provides independent 64-bit wide transmit and receive data paths.
d) It supports full duplex operation only.

132.1.1 Summary of major concepts

The following are the major concepts of the 50GMII:

a) The 50GMII is functionally similar to other media independent interfaces that have been defined for other speeds, as they all define an interface allowing independent development of MAC and PHY logic.
b) The RS converts between the MAC serial data stream and the parallel data paths of the 50GMII.
c) The RS maps the signal set provided at the 50GMII to the PLS service primitives provided at the MAC.
d) Each direction of data transfer is independent and serviced by data, control, and clock signals.
e) The RS generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.
f) The RS participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link, and generating status reports on the transmit path to report detected link faults to the DTE on the remote end of the connecting link.
g) The 50GMII may also support Low Power Idle (LPI) signaling for PHY types supporting Energy Efficient Ethernet (EEE) (see Clause 78).

132.1.2 Application

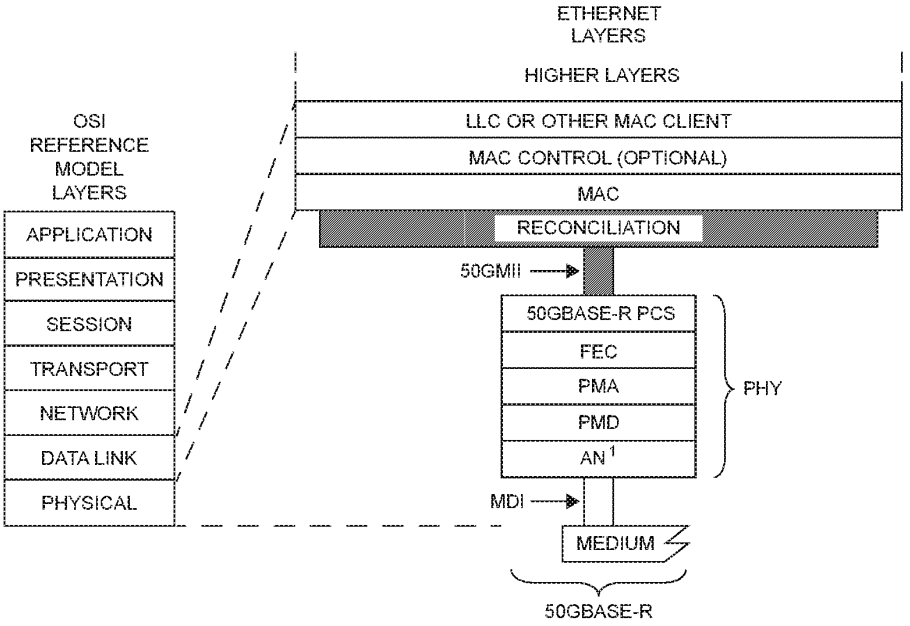
This clause applies to the interface between the MAC and PHY. This logical interface is used to provide media independence so that an identical media access controller may be used with all 50GBASE PHY types.

132.1.3 Rate of operation

The 50GMII is specified to support 50 Gb/s operation.

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50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 132–1—RS and MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

132.1.4 Delay constraints

The maximum cumulative MAC Control, MAC, and RS delay (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 132–1. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

Table 132–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
50 Gb/s MAC, RS, and MAC Control	16 384	32	327.68

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132.1.5 Allocation of functions

The allocation of functions at the 50GMII balances the need for media independence with interface simplicity. The 50GMII maximizes media independence by separating the Data Link and Physical Layers of the OSI seven-layer reference model.

132.1.6 50GMII structure

The 50GMII structure is identical to the CGMII structure specified in 81.1.7.

132.1.7 Mapping of 50GMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the 50GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 50 Gb/s; therefore, PLS service primitives supporting CSMA/CD operation are not mapped through the RS to the 50GMII. This behavior and restrictions are the same as described in 22.7, with the details of the signaling described in 132.3. LPI_REQUEST shall not be set to ASSERT unless the attached link has been operational for at least one second (i.e., link_status = OK, according to the underlying PCS/PMA).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

Mappings for the following primitives are defined for 50 Gb/s:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

The RS maps all primitives in an identical manner as the CGMII does and as specified in 81.1.7.

132.2 50GMII data stream

The 50GMII data stream has the same characteristics as the CGMII data stream described in 81.2.

132.3 50GMII functional specifications

The 50GMII functions identically to the CGMII specified in 81.3.

132.4 LPI assertion and detection

LPI assertion and detection function identically to the CGMII specified in 81.4, with the single exception that the PMA stop signaling is not applicable.

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been deasserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake-up time is enforced by the transmit LPI state diagram using CARRIER_SENSE.indication in an identical manner to that defined in 81.4, with the single exception that the PMA stop signaling described in 81.4.4 is not applicable.

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132.5 Protocol implementation conformance statement (PICS) proforma for Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation[5]

132.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

132.5.2 Identification

132.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

132.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-20xx, Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

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132.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PHY	PHY support of 50GMII	132.2		O	Yes [ ] No [ ]
*RS	Reconciliation Sublayer support of 50GMII	132.2		O	Yes [ ] No [ ]
*LPI	Implementation of LPI	132.4		O	Yes [ ] No [ ]

132.5.3 PICS proforma Tables for Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation

132.5.3.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	PHY support of MAC data rate	132.1	Support MAC data rate of 50 Gb/s	PHY:M	Yes [ ] N/A [ ]
G2	Cumulative MAC Control, MAC, and RS round-trip delay	132.1.4	Per Table 132–1	RS:M	Yes [ ] N/A [ ]

132.5.3.2 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Mapping to Clause 6	132.1.7	RS implements mapping to Clause 6 PLS service primitives	RS:M	Yes [ ] N/A [ ]

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133. Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R

133.1 Overview

133.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) that is common to a family of 50 Gb/s Physical Layer implementations known as 50GBASE-R. The 50GBASE-R PCS is a sublayer of the 50 Gb/s PHYs listed in Table 131–1.

133.1.2 Relationship of 50GBASE-R to other standards

Figure 133–1 depicts the relationships among the 50GBASE-R sublayers, the Ethernet MAC and Reconciliation Sublayers, and the higher layers.

The 50GBASE-R PCS is identical to the 40GBASE-R PCS specified in Clause 82 with the following exceptions:

1) The nominal rate at the FEC or PMA service interface is 12.890625 Gb/s per PCS lane, rather than 10.3125 Gb/s per PCS lane.
2) The alignment marker spacing is modified such that alignment markers are inserted after every 20 479 66-bit blocks on each PCS lane, rather than after every 16 383 66-bit blocks on each PCS lane as described in 82.2.7.
3) The definitions of "current_am", "am_counter", "ber_cnt" and "xus_timer" in the state diagrams defined in 82.2.19 are modified to support the different alignment marker spacing and the different data rate.
4) The optional EEE deep sleep capability is not supported.

133.1.3 Summary of 50GBASE-R sublayers

Figure 133–1 shows the relationship of the 50GBASE-R PCS sublayer (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model.

133.1.3.1 Physical Coding Sublayer (PCS)

The PCS service interface is the 50GMII, which is defined in Clause 132. The 50GMII provides a uniform interface to the Reconciliation Sublayer for all 50 Gb/s PHY implementations

The 50GBASE-R PCS provides all services required by the 50GMII.

133.1.4 Inter-sublayer interfaces

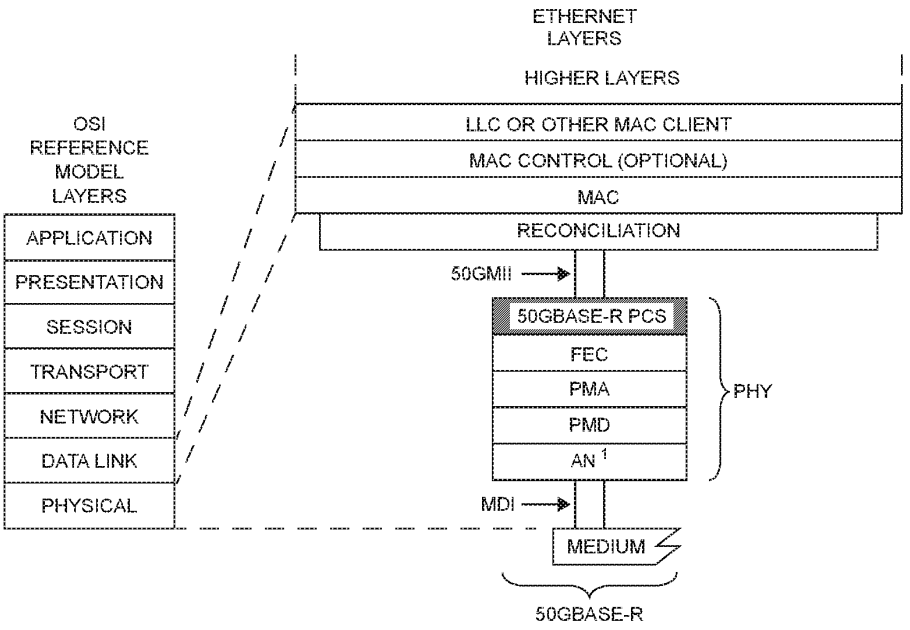
The upper interface of the PCS may connect to the Reconciliation Sublayer through the 50GMII.

The lower interface of the PCS connects to the FEC sublayer. If the optional LAUI-2 interface (see 135B.1 and 135C.1) is physically instantiated directly below the PCS sublayer, then the lower interface of the PCS instead connects to the PMA. The 50GBASE-R PCS is based on 4 PCS lanes and has a nominal rate at the FEC or PMA service interface of 12.890625 Gb/s per PCS lane, which provides capacity for the MAC data rate of 50Gb/s.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

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50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTATION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
FEC = FORWARD ERROR CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 133–1—50GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

133.1.4.1 PCS service interface (50GMII)

The PCS service interface allows the 50GBASE-R PCS to transfer information to and from a PCS client. The PCS client is the Reconciliation Sublayer. The PCS Service Interface is defined as the 50GMII in Clause 132.

133.1.4.2 Forward Error Correction (FEC) or Physical Medium Attachment (PMA) service interface

The FEC or PMA service interface for the PCS is described in an abstract manner and does not imply any particular implementation. The FEC or PMA Service Interface supports the exchange of encoded data between the PCS and the FEC or PMA sublayer. The FEC service interface is defined in 134.2. The PMA service interface is defined in 135.3.

133.1.5 Functional block diagram

Figure 133–2 provides a functional block diagram of the 50GBASE-R PCS.

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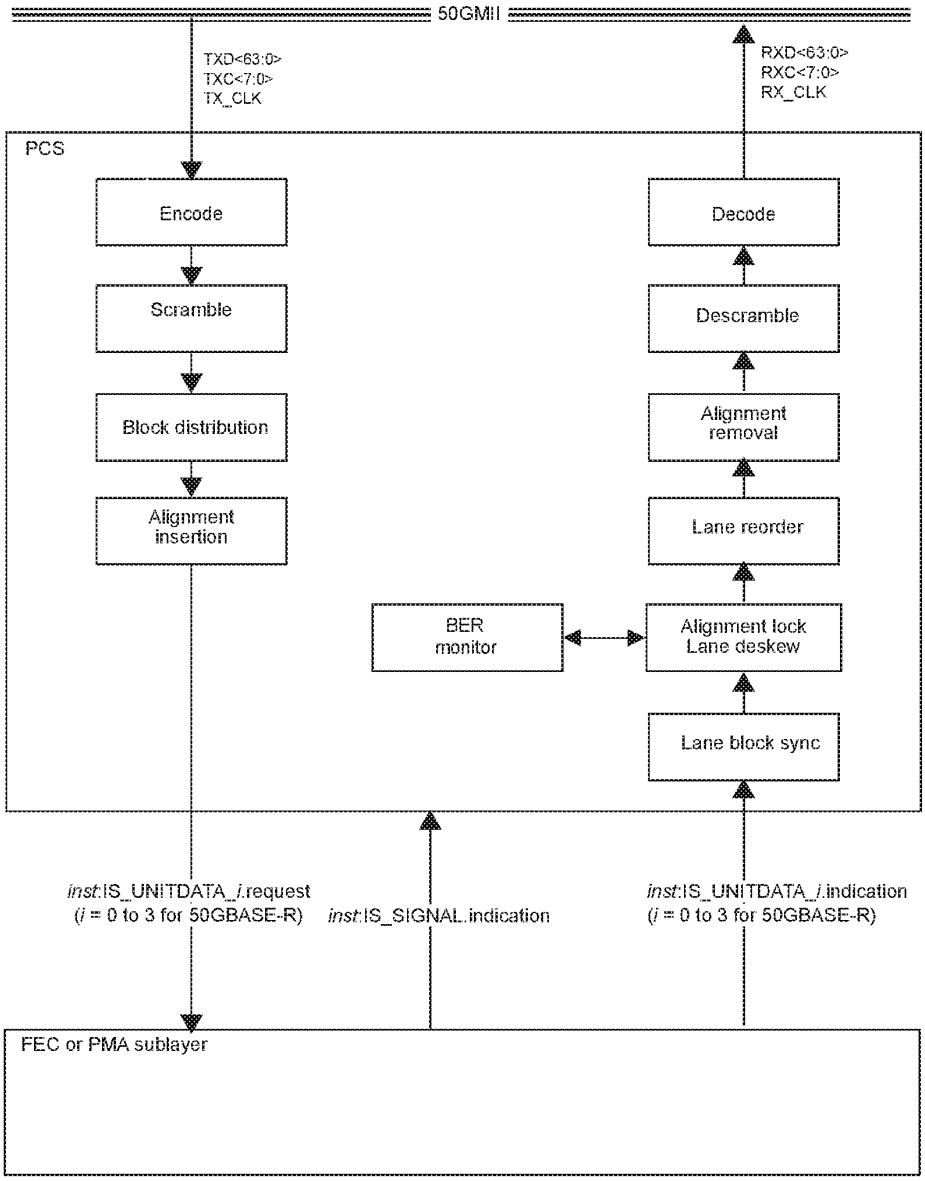


Figure 133–2—50GBASE-R PCS functional block diagram

133.2 Physical Coding Sublayer (PCS)

133.2.1 Functions within the PCS

The 50GBASE-R PCS shall have all of the functionality of the 40GBASE-R PCS specified in Clause 82 with the following exceptions:

1) The nominal rate at the FEC or PMA service interface is 12.890625 Gb/s per PCS lane, rather than 10.3125 Gb/s per PCS lane.

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2) The alignment marker spacing is modified such that alignment markers are inserted after every 20 479 66-bit blocks on each PCS lane, rather than after every 16 383 66-bit blocks on each PCS lane as described in 82.2.7. (See 133.2.2.)

3) The definition of "current_am", "am_counter" "ber_cnt" and "xus_timer" in the state diagrams defined in 82.2.19 are modified to account for the different alignment marker spacing and the different data rate. (See 133.2.4.)

4) The optional deep sleep mode of EEE is not supported.

133.2.2 Alignment marker insertion

The alignment marker insertion for the 50GBASE-R PCS is identical to the alignment marker insertion for the 40GBASE-R PCS described in 82.2.7, with the exception that the alignment markers shall be inserted after every 20 479 66-bit blocks on each PCS lane, rather than after every 16 383 66-bit blocks on each PCS lane as described in 82.2.7. Alignment marker insertion is illustrated in Figure 133–3 and Figure 133–4.

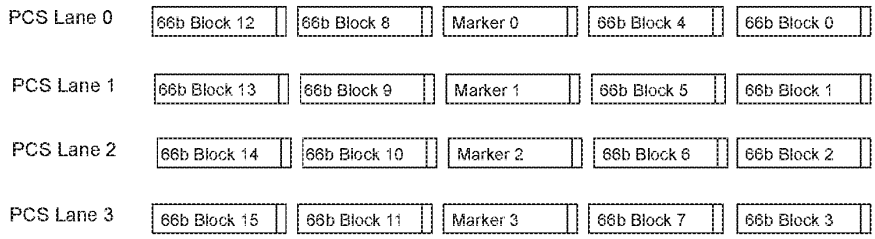


Figure 133–3—Alignment marker insertion

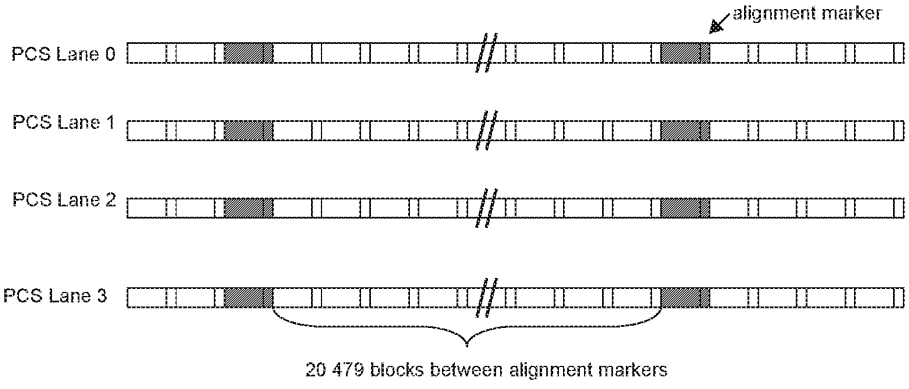


Figure 133–4—Alignment marker insertion period

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The format of the 50GBASE-R PCS alignment markers is identical to the format of the 40GBASE-R PCS alignment markers described in 82.2.7 and shown in Figure 82–9.

The content of the 50GBASE-R PCS alignment markers is identical to the content of the 40GBASE-R PCS alignment markers described in 82.2.7 and shown in Table 82–3.

133.2.3 PCS lane deskew

The 50GBASE-R PCS receiver shall support a maximum Skew of 49 ns and a maximum Skew Variation of 0.4 ns.

Skew and Skew Variation are defined in 131.5.

133.2.4 Detailed functions and state diagrams

The state diagrams are identical to those for the 40GBASE-R PCS defined in 82.2.19 with the exception that some variables, counters and timers are redefined as follows:

current_am
: This variable holds the lane number of the current alignment marker. This is compared to the variable first_am to determine if we have alignment marker lock and is always n × 20 480 66-bit blocks away from the first_am.

am_counter
: This counter counts 66-bit blocks that separate two consecutive alignment markers. The terminal count is 20 479.

ber_cnt
: This counter counts up to a maximum of 97 of the number of invalid sync headers within the current 1 ms period.

xus_timer
: Timer that is triggered every 1 ms +1%, –25%.

133.3 Delay constraints

The maximum delay contributed by the 50GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 11 264 BT (22 pause_quanta or 225.28 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

133.4 Auto-Negotiation

The following requirements apply to a PCS used with a 50GBASE-CR or 50GBASE-KR PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

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133.5 Protocol implementation conformance statement (PICS) proforma for Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R[6]

133.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

133.5.2 Identification

133.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

133.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

[6]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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133.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
PCS	Supports 50GBASE-R PCS functionality	133.1.1		M	Yes [ ]
XGE50	50GMII logical interface	132, 133.1.4	Logical interface is supported	O	Yes [ ] No [ ]
*MD	MDIO	45, 82.3	Registers and interface supported	O	Yes [ ] No [ ]
PMA	Supports operation directly connected to a PMA	133.1.4.2		O.1	Yes [ ] No [ ]
FEC	Supports operation directly connected to a FEC sublayer	133.1.4.2		O.1	Yes [ ] No [ ]
*JTM	Supports test-pattern mode	82.2.3		PMA:M	Yes [ ] N/A[ ]

133.5.4 PICS Proforma Tables for Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R

133.5.4.1 Coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder (and ENCODE function) implements the code as specified	82.2.3 and 82.2.19.2.3		M	Yes [ ]
C2	Decoder (and DECODE function) implements the code as specified	82.2.3 and 82.2.19.2.3		M	Yes [ ]
C3	Only valid block types are transmitted	82.2.3.3		M	Yes [ ]
C4	Invalid block types are treated as an error	82.2.3.3		M	Yes [ ]
C5	Only valid control characters are transmitted	82.2.3.4		M	Yes [ ]
C6	Invalid control characters are treated as an error	82.2.3.4		M	Yes [ ]
C7	Idles do not interrupt data	82.2.3.6		M	Yes [ ]
C8	IDLE control code insertion and deletion	82.2.3.6	Insertion or Deletion in groups of 8 /I/s	M	Yes [ ]
C9	Sequence ordered set deletion	82.2.3.9	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ]

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133.5.4.2 Scrambler and Descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	82.2.5	Performs as shown in Figure 49–8	M	Yes [ ]
S2	Descrambler	82.2.16	Performs as shown in Figure 49–10	M	Yes [ ]

133.5.4.3 Deskew and Reordering

Item	Feature	Subclause	Value/Comment	Status	Support
DR1	Deskew	82.2.13, 133.2.3	Able to deskew up to the value in 133.2.3.	M	Yes [ ]
DR2	Reordering	82.2.14	Performs reordering.	M	Yes [ ]

133.5.4.4 Alignment Markers

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Alignment marker insertion	133.2.2	Alignment markers are inserted periodically as described in section 133.2.2	M	Yes [ ]
AM2	Alignment marker format	133.2.2	Alignment markers are formed as described in Figure 82–9 and Table 82–3	M	Yes [ ]
AM3	Lane mapping	82.2.19.3	PCS lane number is captured	MD:M	Yes [ ] N/A [ ]

133.5.4.5 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Scrambled idle transmit test-pattern generator is implemented	82.2.11	Performs as in 82.2.11	JTM:M	Yes [ ] N/A[ ]
JT2	Scrambled idle receive test-pattern checker is implemented	82.2.18	Performs as in 82.2.18	JTM:M	Yes [ ] N/A[ ]
JT3	Transmit and receive test-pattern modes can operate simultaneously	82.2.3		JTM:M	Yes [ ] N/A[ ]

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133.5.4.6 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	133.2.1, 82.2.3.2	Placement of bits into the PCS lanes as shown in Figure 82–3.	M	Yes [ ]
B2	Receive bit order	133.2.1, 82.2.3.2	Placement of bits into the 50GMII as shown in Figure 82–4	M	Yes [ ]

133.5.4.7 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Alternate access to PCS Management objects is provided	82.3		O	Yes [ ] No [ ]

133.5.4.8 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	50GBASE-R Block Lock	133.2.4	Implements 4 block lock processes as depicted in Figure 82–12	M	Yes [ ]
SM2	The SLIP function evaluates all possible bit positions	133.2.4		M	Yes [ ]
SM3	50GBASE-R Alignment Marker Lock	133.2.4	Implements 4 alignment marker lock processes as depicted in Figure 82–13	M	Yes [ ]
SM4	The AM_SLIP functions evaluates all possible blocks	133.2.4		M	Yes [ ]
SM5	50GBASE-R PCS deskew state diagram	133.2.4	Meets the requirements of Figure 82–14	M	Yes [ ]
SM6	50GBASE-R BER Monitor	133.2.4	Meets the requirements of Figure 82–15 with xus_timer_done set to 1 ms	M	Yes [ ]
SM7	50GBASE-R Transmit process	133.2.4	Meets the requirements of Figure 82–16	M	Yes [ ]
SM8	50GBASE-R Receive process	133.2.4	Meets the requirements of Figure 82–17	M	Yes [ ]

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133.5.4.9 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports loopback	82.4	Performs as in 82.4	M	Yes [ ]
L2	When in loopback, transmits what it receives from the 50GMII	82.4	Performs as in 82.4	M	Yes [ ]

133.5.4.10 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS Delay Constraint	133.3	No more than 11 264 BT for sum of transmit and receive path delays for 50GBASE-R	M	Yes [ ]

133.5.4.11 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Support for use with a 50GBASE-CR or 50GBASE-KR PMD	82.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN1	AN_LINK.indication primitive	82.6	Support of the primitive AN_LINK.indication(link_status)	AN:M	Yes [ ] N/A[ ]
AN2	link_status parameter	82.6	Takes the value OK or FAIL, as described in 82.6	AN:M	Yes [ ] N/A[ ]
AN2	Generation of AN_LINK.indication primitive	82.6	Generated when the value of link_status changes	AN:M	Yes [ ] N/A[ ]

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134. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs

134.1 Overview

134.1.1 Scope

This clause specifies a Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs.

The RS-FEC sublayer for 50GBASE-R PHYs is identical to the RS-FEC sublayer for 100GBASE-R PHYs specified in Clause 91 with the following exceptions:

1) The service interface has four PCS lanes instead of 20 PCS lanes
2) It only implements the RS(544,514) Reed-Solomon encoder option defined in 91.5.2.7.
3) The output of the Reed-Solomon encoder is distributed to two FEC lanes, rather than the four FEC lanes described in 91.5.2.8.
4) The alignment marker processing is modified to account for the difference in the alignment marker format between the 50GBASE-R PCS (Clause 133) and the 100GBASE-R PCS (Clause 82), for the fact that the alignment markers are mapped to two FEC lanes rather than four FEC lanes, and for the fact that the alignment marker mapping to the two FEC lanes needs to maintain a 10-bit alignment.
5) The definition of some of the variables and counters for the state diagrams in 91.5.4 are modified to support the different alignment marker spacing and the different number of FEC lanes
6) The states identified as optional in the FEC synchronization state diagram in 91.5.4.3 (Figure 91–8) are mandatory for the 50GBASE-R RS-FEC.
7) The optional EEE deep sleep capability is not supported.
8) The optional FEC bypass correction feature is not supported.

134.1.2 Position of RS-FEC in the 50GBASE-R sublayers

Figure 134–1 shows the relationship of the RS-FEC sublayer to the ISO/IEC Open System Interconnection (OSI) reference model.

134.2 FEC service interface

This subclause specifies the services provided by the RS-FEC sublayer. The service interface is described in an abstract manner and does not imply any particular implementation.

The FEC service interface is provided to allow the PCS to transfer information to and from the RS-FEC. The PCS may be connected to the RS-FEC using an optional instantiation of the PMA service interface (see Annex 135B) in which case a PMA is the client of the FEC service interface.

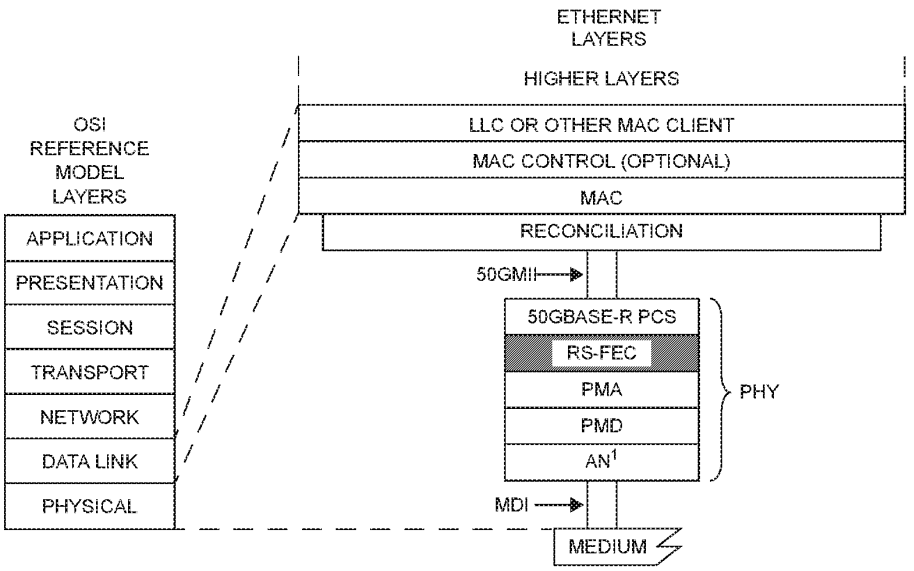
The FEC service interface is an instance of the inter-sublayer service interface defined in 131.3. The FEC service interface primitives are summarized as follows:

FEC:IS_UNITDATA_*i*.request
FEC:IS_UNITDATA_*i*.indication
FEC:IS_SIGNAL.indication

The RS-FEC operates on four parallel bit streams, hence $i = 0$ to 3.

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50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTATION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 134–1—RS-FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The PCS or PMA continuously sends four parallel bit streams to the RS-FEC, one per PCS lane, each at a nominal signaling rate of 12.890625 Gb/s. The RS-FEC continuously sends four parallel bit streams to the PCS or PMA, one per PCS lane, each at a nominal signaling rate of 12.890625 Gb/s.

The SIGNAL_OK parameter of the FEC:IS_SIGNAL.indication primitive can take one of two values: OK or FAIL. The value is set to OK when the FEC receive function has identified codeword boundaries as indicated by fec_align_status equal to true. That value is set to FAIL when the FEC receive function is unable to reliably establish codeword boundaries as indicated by fec_align_status equal to false. When SIGNAL_OK is FAIL, the rx_bit parameters of the FEC:IS_UNITDATA_*i*.indication primitives are undefined.

134.3 PMA compatibility

The RS-FEC sublayer requires that the PMA service interface consist of exactly two upstream FEC lanes and exactly two downstream FEC lanes, with each lane running at a nominal signaling rate of 26.5625 Gb/s. Therefore, the RS-FEC sublayer may be a client of the 50GBASE-R PMA sublayer defined in Clause 135, when the PMA service interface width, *p*, is set to 2.

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134.4 Delay constraints

The maximum delay contributed by the RS-FEC sublayer (sum of transmit and receive delays at one end of the link) shall be no more than 25 600 bit times (50 pause_quanta or 512 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

134.5 Functions within the RS-FEC sublayer

134.5.1 Functional block diagram

A functional block diagram of the RS-FEC sublayer is shown in Figure 134–2.

134.5.2 Transmit function

134.5.2.1 PCS Lane block synchronization

The RS-FEC transmit function forms four bit streams by concatenating the bits from each of the four FEC:IS_UNITDATA_*i*.request primitives in the order they are received. It obtains lock to the 66-bit blocks in each bit stream using the sync headers and outputs 66-bit blocks. Block lock is obtained as specified in the block lock state diagram shown in Figure 82–12, but using the variable definitions from 133.2.4.

134.5.2.2 PCS Alignment lock and deskew

Once the RS-FEC transmit function achieves block lock on a PCS lane, it then begins obtaining alignment marker lock as specified by the alignment marker lock state diagram shown in Figure 82–13, but using the variable definitions from 133.2.4. This process identifies the PCS lane number received on a particular lane of the service interface. After alignment marker lock is achieved on all four PCS lanes, all inter-lane Skew is removed as specified by the PCS deskew state diagram shown in Figure 82–14, but using the variable definitions from 133.2.4. The RS-FEC transmit function shall support a maximum Skew of 49 ns and a maximum Skew Variation of 0.4 ns. Skew and Skew Variation are defined in 131.5.

134.5.2.3 PCS Lane reorder

PCS lanes can be received on different lanes of the service interface from which they were originally transmitted due to Skew between lanes and multiplexing by the PMA. The RS-FEC transmit function shall order the PCS lanes according to the PCS lane number.

134.5.2.4 Alignment marker removal

After all PCS lanes are aligned and deskewed, the PCS lanes are multiplexed together in the proper order to reconstruct the original stream of blocks and the alignment markers are removed from the data stream. Note that an alignment marker is always removed when am_lock is true for a given PCS lane even if it does not match the expected alignment marker value (due to a bit error for example). Repeated alignment marker errors result in am_lock being set to false for a given PCS lane, but until that happens it is sufficient to remove the block in the alignment marker position.

As part of the alignment marker removal process, the BIP_3 field is compared to the calculated Bit Interleaved Parity (BIP) value (see 82.2.8) for each PCS lane. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 1.230 to 1.233) is incremented by one each time the calculated BIP value does not equal the value received in the BIP_3 field. The incoming bit error ratio can be estimated by dividing the BIP block error ratio by a factor of 1 351 680.

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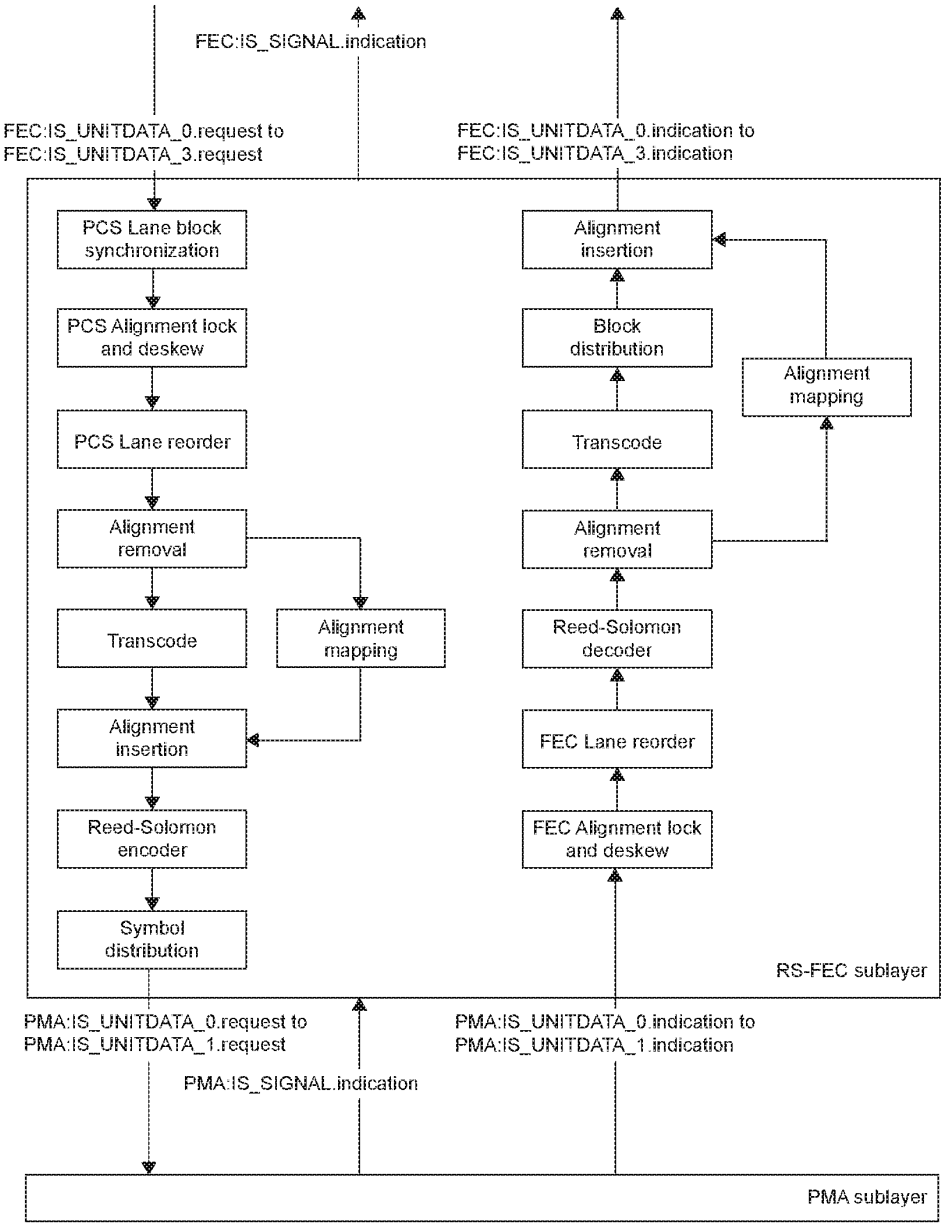


Figure 134–2—Functional block diagram

134.5.2.5 64B/66B to 256B/257B transcoder

The 64B/66B to 256B/257B transcoder is identical to the transcoder for the 100GBASE-R RS-FEC sublayer defined in 91.5.2.5.

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134.5.2.6 Alignment marker mapping and insertion

The alignment markers that were removed per 134.5.2.4 are re-inserted after being processed by the alignment marker mapping function. The alignment marker mapping function compensates for the operation of the symbol distribution function defined in 134.5.2.8 and rearranges the alignment marker bits so that they appear on the FEC lanes intact and in the desired sequence. This preserves the properties of the alignment markers (e.g., DC balance, transition density) and provides a deterministic pattern for the purpose of synchronization at the receiver. The RS-FEC receive function uses knowledge of this mapping to determine the FEC lane that is received on a given lane of the PMA service interface, to compensate for skew between FEC lanes, and to identify RS-FEC codeword boundaries.

The alignment marker mapping function operates on a group of four aligned and reordered alignment markers received from the PCS. Let am_tx_*x*<65:0> be the alignment marker for PCS lane *x*, *x*=0 to 3, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_txmapped<256:0> in a manner that yields the same result as the following process.

For *x*=0 to 3, amp_tx_*x*<63:0> is constructed as follows:

- Set *y* = 0 when *x* ≤ 1, otherwise set *y* = *x*.
- amp_tx_*x*<23:0> is set to M_0, M_1, and M_2 as shown in Figure 82–9 (bits 25 to 2) using the values in Table 82–3 for PCS lane number *y*.
- amp_tx_*x*<31:24> = am_tx_*x*<33:26>
- amp_tx_*x*<55:32> is set to M_4, M_5, and M_6 as shown in Figure 82–9 (bits 57 to 34) using the values in Table 82–3 for PCS lane number *y*.
- amp_tx_*x*<63:56> = am_tx_*x*<65:58>

This process replaces the fixed bytes of the alignment markers received from the PCS, possibly with errors, with the values from Table 82–3. In addition it substitutes the fixed bytes of the alignment markers corresponding to PCS lane 1 with the fixed bytes for the alignment marker corresponding to PCS lane 0. The variable bytes of the alignment markers received from the PCS (BIP_3 and BIP_7) are unchanged. This simplifies the synchronization process at the RS-FEC receiver, as the receiver only needs to search for the fixed alignment marker bytes corresponding to PCS lane 0 on each FEC lane.

am_txpayloads<0,129:0> and am_txpayloads<1,125:0> are then constructed from amp_tx as follows:

- am_txpayloads<0, 63:0> = amp_tx_0<63:0>
- am_txpayloads<0, 127:64> = amp_tx_2<63:0>
- am_txpayloads<0, 129:128> = amp_tx_3<57:56>
- am_txpayloads<1, 63:0> = amp_tx_1<63:0>
- am_txpayloads<1, 119:64> = amp_tx_3<55:0>
- am_txpayloads<1, 125:120> = amp_tx_3<63:58>

This process is an intermediate step in the generation of am_txmapped<256:0>, and is illustrated in Figure 134–3.

Given *i*=0 to 1, *k*=0 to 12, and *y*=*i*+2*k*, am_txmapped<255:0> is constructed from am_txpayloads as follows:

- If (*y* < 25) then am_txmapped<(10*y*+9):10*y*> = am_txpayloads<*i*, (10*k*+9):10*k*>
- am_txmapped<255:250> = am_txpayloads<1, 125:120>

A 1-bit pad is appended to the mapped alignment markers to yield the equivalent of one 257-bit block. The pad bit, am_txmapped<256>, shall be set to 0 or 1 in an alternating pattern.

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am_txmapped<256:0> is inserted into the data path prior to the Reed-Solomon encoder (see Figure 134–4) every 4 × 20 480 66-bit blocks, corresponding to every 1 024 Reed-Solomon codewords. The mapped alignment markers, am_txmapped<256:0> shall be inserted as the first 257 message bits to be transmitted every 1024th codeword. The first 257-bit block inserted after am_txmapped shall correspond to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective PCS lane.

The result of this alignment mapping process is that after Reed-Solomon encoding and symbol distribution (134.5.2.7 and 134.5.2.8 respectively), the alignment marker bit patterns shown in Figure 134–3 appear on the two FEC output lanes and aligned with the start of every 1024th FEC codeword. The FEC receiver uses this information to lock onto the two FEC lanes and to identify the FEC codeword boundaries.

An additional result of this alignment mapping process, is that the BIP_3 and BIP_7 fields from normal PCS alignment markers are carried across the link protected by FEC. These fields cannot be used to monitor errors on the link protected by FEC as 64B/66B to 256B/257B transcoding and Reed-Solomon encoding alters the bit sequence. However, these fields may again be used to monitor errors after the original bit sequence is restored, i.e., following Reed-Solomon decoding and 256B/257B to 64B/66B transcoding.

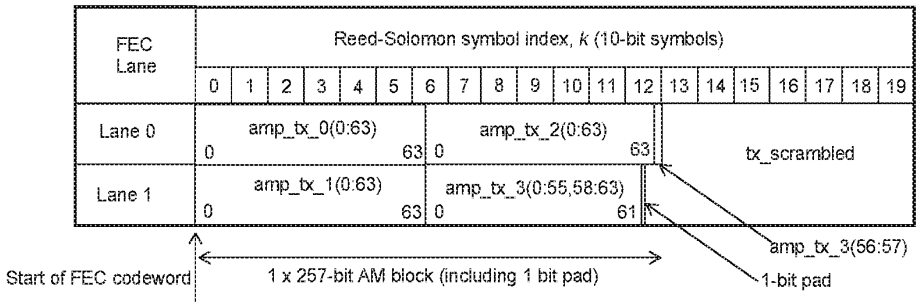


Figure 134–3—Alignment marker mapping to FEC lanes

134.5.2.7 Reed-Solomon encoder

The Reed-Solomon encoder is identical to the RS(544,514) Reed-Solomon encoder defined in 91.5.2.7.

134.5.2.8 Symbol distribution

Once the data has been Reed-Solomon encoded, it is distributed to two FEC lanes, one 10-bit symbol at a time in a round robin distribution from the lowest to the highest numbered FEC lane. The distribution process is shown in Figure 134–4.

134.5.2.9 Transmit bit ordering

The transmit bit ordering is illustrated in Figure 134–4.

134.5.3 Receive function

134.5.3.1 Alignment lock and deskew

The RS-FEC receive function forms two bit streams by concatenating the bits from each of the two PMA:IS_UNITDATA_*i*.indication primitives in the order they are received. It obtains lock to the alignment markers as specified by the FEC synchronization state diagram shown in Figure 91–8, but using the variable definitions from 134.5.4.

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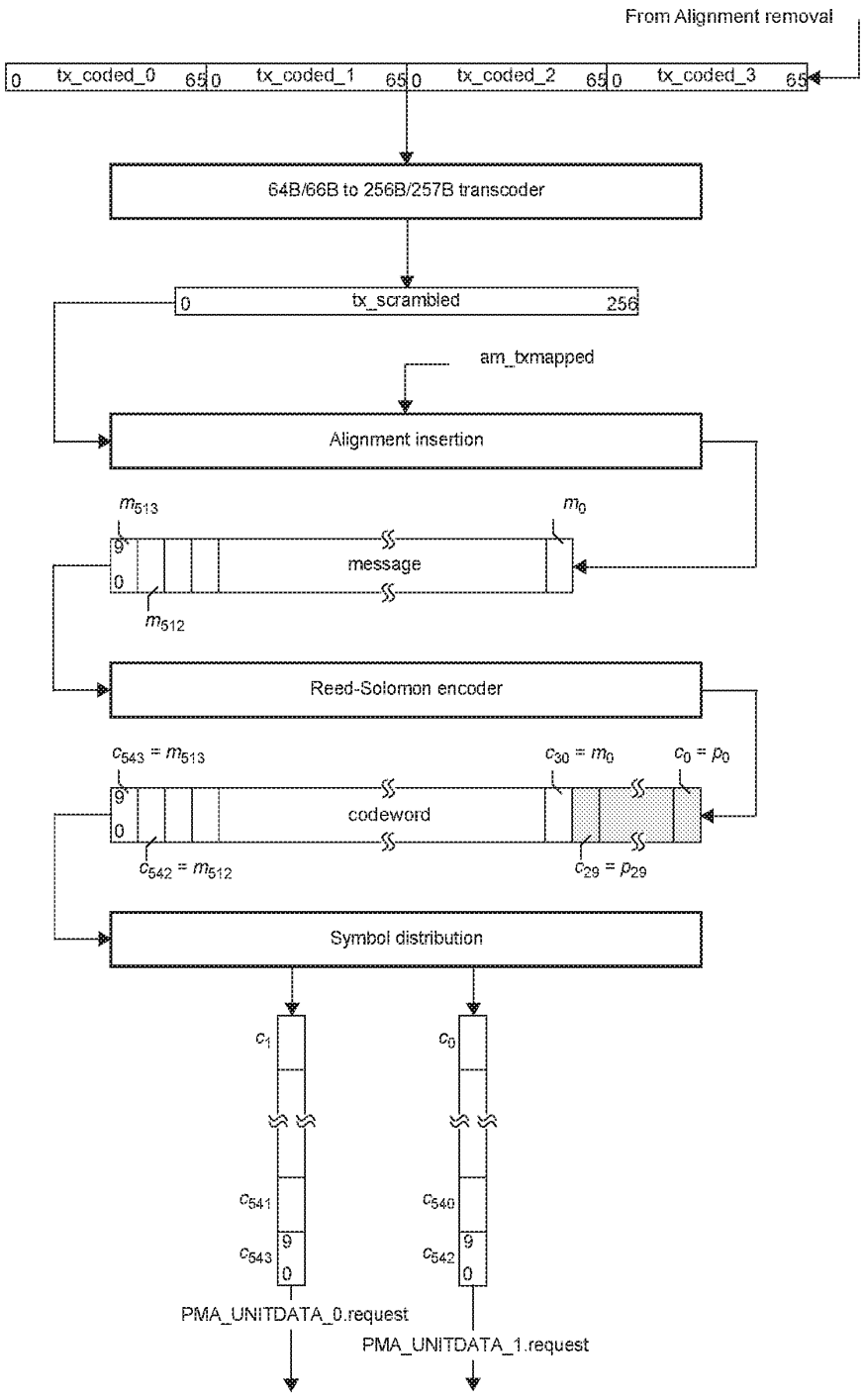


Figure 134–4—Transmit bit ordering

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After alignment marker lock is achieved the two FEC lanes, all inter-lane Skew is removed as specified by the FEC alignment state diagram shown in Figure 91–9. The FEC receive function shall support a maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns.

134.5.3.2 FEC Lane reorder

FEC lanes can be received on different lanes of the service interface from which they were originally transmitted. The FEC receive function shall order the FEC lanes according to the FEC lane number (see 134.5.2.6). The FEC lane number is defined by the sequence of alignment markers that are mapped to each FEC lane.

After all FEC lanes are aligned, deskewed, and reordered, the FEC lanes are multiplexed together in the proper order to reconstruct the original stream of FEC codewords.

134.5.3.3 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols.

The RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when an errored codeword was not corrected. The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10^{-6}. This limit is also expected to apply for t+2 errors, t+3 errors, and so on.

The Reed-Solomon decoder shall indicate errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors that were not corrected, it ensures that for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11. In addition, it shall ensure that rx_coded_0<1:0> corresponding to the second 257-bit block and rx_coded_3<1:0> corresponding to the last (20th) 257-bit block in the codeword are set to 11. Setting rx_coded_0<1:0> to 11 as described causes the PCS to assign R_BLOCK_TYPE=E to the 66-bit block and decode its content as EBLOCK_R (see 49.2.13.2.1 and 49.2.13.2.3). This causes the PCS to discard all frames 64 bytes and larger that are fully or partially contained within the codeword.

The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see 134.6.2). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see 134.6.1).

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the RS-FEC sublayer to reduce the likelihood that errors in a packet are not detected. The Reed-Solomon decoder counts the number of symbol errors detected in consecutive non-overlapping blocks of 8192 codewords. When the number of symbol errors in a block of 8192 codewords exceeds 6380, the Reed- Solomon decoder shall cause synchronization header rx_coded<1:0> of each subsequent 66-bit block that is delivered to the PCS to be assigned a value of 00 or 11 for a period of 60 ms to 75 ms. As a result, the PCS sets hi_ber = true, which inhibits the processing of received packets. When Auto-Negotiation is supported and enabled, assertion of hi_ber causes Auto-Negotiation to restart.

134.5.3.4 Alignment marker removal

The first 257 message bits in every 1024th codeword is the vector am_rxmapped<256:0> where bit 0 is the first bit received. The specific codewords that include this vector are indicated by the alignment lock and deskew function (see 134.5.3.1).

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The vector am_rxmapped shall be removed prior to transcoding.

134.5.3.5 256B/257B to 64B/66B transcoder

The 256B/257B to 64B/66B transcoder is identical to the transcoder for the 100GBASE-R RS-FEC sublayer defined in 91.5.3.5.

134.5.3.6 Block distribution

After the data has been transcoded, it shall be distributed to four PCS lanes, one 66-bit block at a time in a round robin distribution from the lowest to the highest numbered PCS lanes. The distribution process is shown in Figure 82–6.

134.5.3.7 Alignment marker mapping and insertion

The alignment marker mapping function compensates for operation of the lane reorder function (see 134.5.2.3) to derive the PCS lane alignment markers, am_rx_*x*<65:0> for *x*=0 to 3, from am_rx-mapped<256:0> (see134.5.3.4).

The alignment markers shall be derived from am_rxmapped<256:0> in a manner that yields the same result as the following process.

Given *i*=0 to 1, *k*=0 to 12, and *y*=*i*+2*k*, am_rxpayloads is constructed from am_rxmapped as follows:.

- If (*y* < 25) then am_rxpayloads<*i*, (10*k*+9):10*k*> = am_rxmapped<(10*y*+9):10*y*>
- am_rxpayloads<1, 125:120> = am_rxmapped<255:250>

The one bit pad am_rxmapped<256> is ignored by the receiver.

For *x*=0 to 3, amp_rx_*x*<63:0> is constructed from am_rxpayloads as follows:

- amp_rx_0<63:0> = am_rxpayloads<0, 63:0>
- amp_rx_1<63:0> = am_rxpayloads<1, 63:0>
- amp_rx_2<63:0> = am_rxpayloads<0, 127:64>
- amp_rx_3<55:0> = am_rxpayloads<1, 119:64>
- amp_rx_3<57:56> = am_rxpayloads<0, 129:128>
- amp_rx_3<63:58> = am_rxpayloads<1, 125:120

For *x*=0 to 3, am_rx_*x*<65:0> is constructed as follows:

- am_rx_*x*<0>=1 and am_rx_*x*<1>=0.
- am_rx_*x*<25:2> is set to M_0, M_1, and M_2 as shown in Figure 82–9 using the values in Table 82–3 for PCS lane number *x*.
- am_rx_*x*<33:26> = amp_rx_*x*<31:24>.
- am_rx_*x*<57:34> is set to M_4, M_5, and M_6 as shown in Figure 82–9 using the values in Table 82–3 for PCS lane number *x*.
- am_rx_*x*<65:58> = amp_rx_*x*<63:56>

One vector is mapped to four alignment markers every 1 024 Reed-Solomon codewords (see 134.5.3.4). The alignment markers are simultaneously transmitted on the four PCS lanes after every 20 479th column of four 66-bit blocks.

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The alignment markers am_rx_0 to am_rx_3 shall be inserted so that they are immediately followed by rx_coded_0 to rx_coded_3, respectively, as derived from the first 257-bit block following am_rxmapped

134.5.3.8 Receive bit ordering

The receive bit ordering is illustrated in Figure 134–5. This illustration shows the case where the FEC lanes appear across the PMA:IS_UNITDATA_*i*.indication primitives in the correct order.

134.5.4 Detailed functions and state diagrams.

The state diagrams, including the associated definitions of variables, functions and counters, are identical to those for the 100GBASE-R RS-FEC sublayer defined in 91.5.4, with the exception that some of the variables and counters are redefined to account for the differences in alignment marker spacing and number of FEC lanes.

In addition, EEE optional deep sleep capability is not supported for 50GBASE-R PHYs and therefore any reference to the optional EEE deep sleep capability in 91.5.4 can be ignored.

134.5.4.1 State diagram conventions

The state diagram conventions are identical to those defined in 91.5.4.1.

134.5.4.2 State variables

134.5.4.2.1 Variables

This following variables are redefined from what is described in 91.5.4.2.1:

amp_valid
: Boolean variable that is set to true if the received 64-bit block is a valid alignment marker payload. The alignment marker payload, mapped to an FEC lane according to the process described in 134.5.2.6, consists of 48 known bits and 16 variable bits (the BIP3 field and its complement BIP7 see 82.2.7). The bits of the candidate block that are in the positions of the known bits in the alignment marker payload are compared on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles in the alignment marker payload, the candidate block is considered a valid alignment marker payload. Each FEC lane compares the candidate block to the alignment marker payload for PCS lane 0.

amps_lock<*x*>
: Boolean variable that is set to true when the receiver has detected the location of the alignment marker payload sequence for a given lane on the PMA service interface, where *x* = 0:1.

fec_lane
: A variable that holds the FEC lane number (0 to 1) received on lane *x* of the PMA service interface when amps_lock<*x*> = true. The FEC lane number is determined by the alignment marker payloads in the 2nd position of the sequence based on the mapping defined in 134.5.2.6. The 48 bits that are in the positions of the known bits in the received alignment marker payload are compared to the expected values for a given payload position and FEC lane on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles on a given FEC lane, then the FEC lane number is assigned accordingly.

fec_lpi_fw
: Boolean variable that controls the behavior of the Transmit LPI and Receive LPI state dia-

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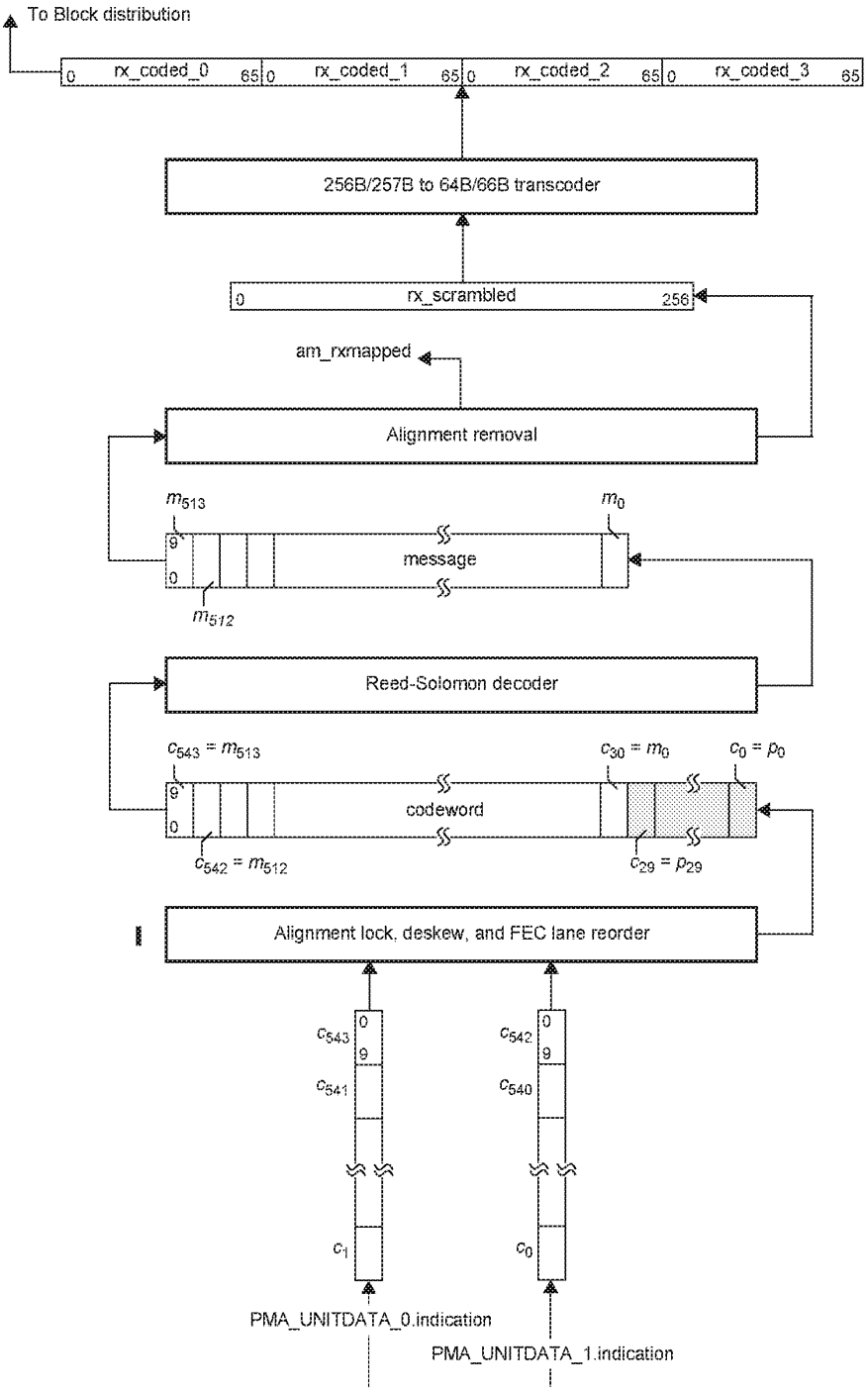


Figure 134–5—Receive bit ordering

grams. This variable is set to true when the local PCS is configured to use the fast wake mechanism and set to false otherwise. This variable shall always be set to true.

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fec_optional_states

Boolean variable that is always set to true to indicate that the optional states in the FEC synchronization state diagram in Figure 91–8 are implemented.

134.5.4.2.2 Functions

The functions are identical to those defined in 91.5.4.2.2.

134.5.4.2.3 Counters

This following counters are redefined from what is described in 91.5.4.2.3:

amp_counter

This counter counts the 1 024 FEC codewords that separate the ends of two consecutive normal alignment marker payload sequences. A FEC codeword is 2 720 bits per FEC lane

134.5.4.3 State diagrams

The state diagrams are identical to those defined in 91.5.4.3.

134.6 RS-FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the RS-FEC. If MDIO is implemented, it shall map MDIO control bits to RS-FEC control variables as shown in Table 134–1, and MDIO status bits to RS-FEC status variables as shown in Table 134–2, and if a separated PMA (see 45.2.1) is connected to the FEC service interface (e.g., if the RS-FEC and PCS are separated via a LAUI-2 interface) it shall map additional MDIO status bits to additional RS-FEC status variables as shown in Table 134–3.

Table 134–1—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable

The following subclauses define variables that are not otherwise defined, e.g., for use by state diagrams.

134.6.1 FEC_bypass_indication_enable

This variable is set to one to bypass the error indication function (see 91.5.3.3) when this ability is supported. When this variable is set to zero, the decoder indicates errors to the PCS sublayer. The default value of this variable is zero. This variable is mapped to the bit defined in 45.2.1.101 (1.200.1).

134.6.2 FEC_bypass_indication_ability

The Reed-Solomon decoder may have the option to bypass the error indication function (see 91.5.3.3) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error indication. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.102 (1.201.1).

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Table 134–2—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication ability	RS-FEC status register	1.201.1	FEC_bypass_indication_ability
RS-FEC high SER	RS-FEC status register	1.201.2	hi_ser
FEC AM lock *x*, *x*=0 to 1	RS-FEC status register	1.201.8:9	amps_lock<*x*>
RS-FEC align status	RS-FEC status register	1.201.14	fec_align_status
FEC corrected codewords	RS-FEC corrected code-words counter register	1.202, 1.203	FEC_corrected_cw_counter
FEC uncorrected codewords	RS-FEC uncorrected code-words counter register	1.204, 1.205	FEC_uncorrected_cw_counter
FEC lane *x* mapping	RS-FEC lane mapping register	1.206	FEC_lane_mapping<*x*>
FEC symbol errors, FEC lanes 0 to 1	RS-FEC symbol error counter register, FEC lanes 0 to 1	1.210 to 1.213	FEC_symbol_error_counter_*i*

Table 134–3—MDIO/RS-FEC status variable mapping for separated PMA

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
PCS align status	RS-FEC status register	1.201.15	align_status
BIP errors, PCS lanes 0 to 3	RS-FEC BIP error counter register, PCS lanes 0 to 3	1.230 to 1.233	BIP_error_counter_*i*
PCS lane *x* mapping	PCS lane *x* mapping register	1.250 to 1.253	lane_mapping<*x*>
Block *x* lock	RS-FEC PCS alignment status 1 register	1.280	block_lock<*x*>
Lane *x* aligned	RS-FEC PCS alignment status 3 register	1.282	am_lock<*x*>

134.6.3 hi_ser

This variable is defined when the FEC_bypass_indication_ability variable is set to one. When FEC_bypass_indication_enable is set to one, this bit is set to one if the number of RS-FEC symbol errors in a window of 8 192 codewords exceeds the threshold (see 91.5.3.3) and is set to zero otherwise. This variable is mapped to the bit defined in 45.2.1.102 (1.201.2).

134.6.4 amps_lock<*x*>

These variables are assigned by the FEC alignment state diagram shown in Figure 91–9 (see 91.5.4.3.and 134.5.4). They are mapped to the bits defined in 45.2.1.102 (1.201.8 to 1.201.9 for FEC lanes 0 to 1, respectively).

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134.6.5 fec_align_status

This variable assigned by the FEC alignment state diagram shown in Figure 91–9 (see 91.5.4.3). It is mapped to the bit defined in 45.2.1.102 (1.201.14).

134.6.6 FEC_corrected_cw_counter

A corrected FEC codeword is a codeword that contains errors and was corrected.

FEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.103 (1.202, 1.203).

134.6.7 FEC_uncorrected_cw_counter

An uncorrected FEC codeword is a codeword that contains errors (when the bypass correction feature is supported and enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled).

FEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.104 (1.204, 1.205).

134.6.8 FEC_lane_mapping<*x*>

When the RS-FEC receive function detects and locks to an alignment marker payload on PMA service interface lane *x*, the FEC lane number corresponding to the detected alignment marker payload is assigned to the variable FEC_lane_mapping<*x*>. These variables are mapped to the register defined in 45.2.1.105 (1.206).

134.6.9 FEC_symbol_error_counter_*i*

FEC_symbol_error_counter_*i*, where *i*=0 to 1, is a 32-bit counter that counts once for each 10-bit symbol corrected on FEC lane *i* when fec_align_status is true. These variables are mapped to the registers defined in 45.2.1.106 and 45.2.1.107 (1.210 to 1.213).

134.6.10 align_status

This variable is assigned the value of rx_align_status as defined by the PCS deskew state diagram shown in Figure 82–14 (see 134.5.2.2) It is mapped to the bit defined in 45.2.1.102 (1.201.15).

134.6.11 BIP_error_counter_*i*

BIP_error_counter_*i*, where *i*=0 to 3, is a 16-bit counter that holds the BIP error count for PCS lane *i* as calculated by the RS-FEC transmit function (see 134.5.2.4). These variables are mapped to the registers defined in 45.2.1.108 and 45.2.1.109 (1.230 to 1.233).

134.6.12 lane_mapping<*x*>

When the RS-FEC transmit function detects and locks to an alignment marker on FEC service interface lane *x*, the PCS lane number corresponding to the detected alignment marker is assigned to the variable lane_mapping<*x*>. These variables are mapped to the registers defined in 45.2.1.110 and 45.2.1.111 (1.250 to 1.253).

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134.6.13 block_lock<*x*>

These variables are assigned by the block lock state diagram shown in Figure 82–12 (see 134.5.2.1). They are mapped to the registers defined in 45.2.1.112 (1.280).

134.6.14 am_lock<*x*>

These variables are assigned by the alignment marker lock state diagram shown in Figure 82–13 (see 134.5.2.2). They are mapped to the registers defined in 45.2.1.114 (1.282).

134.7 Protocol implementation conformance statement (PICS) proforma for Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs[7]

134.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

134.7.2 Identification

134.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

[7]*Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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134.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-201x.)	

Date of Statement	

134.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
RS-FEC	Supports 50GBASE-R RS-FEC functionality	134.1.1		M	Yes [ ]
*MD	MDIO capability	45, 134.6	Registers and interface supported	O	Yes [ ] No [ ]
*BEI	Bypass error indication	134.5.3.3	Capability is supported	O	Yes [ ] No [ ]

134.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs

134.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Skew tolerance	134.5.2.2	Maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps.	M	Yes [ ]
TF2	Lane reorder	134.5.2.3	Order the PCS lanes according to the PCS lane number	M	Yes [ ]
TF3	64B/66B to 256B/257B transcoder	134.5.2.5	tx_xcoded<256:0> constructed per 134.5.2.5	M	Yes [ ]
TF4	257-bit block transmission order	134.5.2.5	First bit transmitted is bit 0	M	Yes [ ]
TF5	Alignment maker mapping	134.5.2.6	Map to am_tx-mapped<256:0> per 134.5.2.6	M	Yes [ ]
TF6	Pad value	134.5.2.6	Set to 0 or 1 in an alternating pattern	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TF7	Alignment marker insertion	134.5.2.6	First 256 message bits to be transmitted from every 1024th codeword	M	Yes [ ]
TF8	Alignment marker insertion point	134.5.2.6	First 257-bit block inserted after am_txmapped corresponds to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective lane	M	Yes [ ]
TF9	Reed-Solomon encoder	134.5.2.7		M	Yes [ ]
TF10	Symbol distribution	134.5.2.8	Distributed to 2 FEC lanes, one 10-bit symbol at a time in a round robin distribution from the lowest to the highest numbered FEC lane	M	Yes [ ]

134.7.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	134.5.3.1	Maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder	134.5.2.3	Order the FEC lanes according to the FEC lane number	M	Yes [ ]
RF3	Reed-Solomon decoder for RS(544,514)	134.5.3.3	Corrects any combination of up to t=15 symbol errors in a codeword.	M	Yes [ ]
RF4	Reed-Solomon decoder	134.5.3.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF5	Error indication function	134.5.3.3	Corrupts 66-bit block synchronization headers for uncorrected errored codewords.	M	Yes [ ]
RF7	Error monitoring while error indication is bypassed	134.5.3.3	When the number of symbols errors in a block of 8 192 codewords exceeds K, corrupt 66-bit block synchronization headers	BEI:M	Yes [ ] N/A [ ]
RF8	Symbol error threshold for RS(544,514)	134.5.3.3	K=6380	BEI:M	Yes [ ] N/A [ ]
RF9	Alignment marker removal	134.5.3.4	am_rxmapped removed prior to transcoding	M	Yes [ ]
RF10	256B/257B to 64B/66B transcoder	134.5.3.5	rx_coded_j<65:0>, j=0 to 3 constructed per 134.5.3.5	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RF11	Block distribution	134.5.3.7	One 66-bit block at a time in a round robin fashion from the lowest to the highest numbered PCS lane	M	Yes [ ]
RF12	Alignment marker mapping	134.5.3.7	Map to am_rx_*x*, *x*=0 to 3 per 134.5.3.7	M	Yes [ ]
RF13	Alignment marker insertion point	134.5.3.7	Alignment markers immediately followed by the 66-bit blocks derived from the 257-bit blocks immediately following am_rxmapped	M	Yes [ ]

134.7.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	SLIP function	134.5.4.2.2	Ensure that all possible block positions are evaluated	M	Yes [ ]
SD2	Synchronization process	134.5.4.3	One instance per FEC lane per Figure 91–8	M	Yes [ ]
SD3	Alignment process	134.5.4.3	Per Figure 91–9	M	Yes [ ]

134.7.4.4 Delay Constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	RS-FEC Delay Constraint	134.4	No more than 25 600 BT for sum of transmit and receive path delays.	M	Yes [ ]

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135. Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P

135.1 Overview

135.1.1 Scope

This clause specifies the Physical Medium Attachment sublayer (PMA) for the families of 50 Gb/s and 100 Gb/s PAM4 Physical Layer implementations known as 50GBASE-R (see 131.1.3) and 100GBASE-P (see 80.1.4). The PMA allows the PCS (see Clause 133 and Clause 82) and FEC (see Clause 134 and Clause 91) to connect in a media-independent way with a range of physical media. The 50GBASE-R PMA can support any of the 50 Gb/s PMDs in Table 131–1 and the 100GBASE-P PMA can support any of the 100 Gb/s PAM4 PMDs according to Table 80–3 and Table 80–4a.

50GBASE-R and 100GBASE-P PHYs can be extended to support any full duplex medium requiring only that the PMD be compliant with the appropriate PMA interface.

The interfaces for the inputs of the 50GBASE-R and 100GBASE-P PMAs are defined in an abstract manner and do not imply any particular implementation. For 50GBASE-R PMAs, electrical interfaces connecting PMA sublayers, known as LAUI-2 and 50GAUI-n, are defined in Clause 135B through Clause 135G. For 100GBASE-P PMAs, electrical interfaces connecting PMA sublayers, known as 100GAUI-n, are defined in Clause 135D through Clause 135G.

135.1.2 Position of the PMA in the 50GBASE-R and 100GBASE-P sublayers

Figure 135–1 shows the relationship of the PMA sublayer (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model

135.1.3 Summary of functions

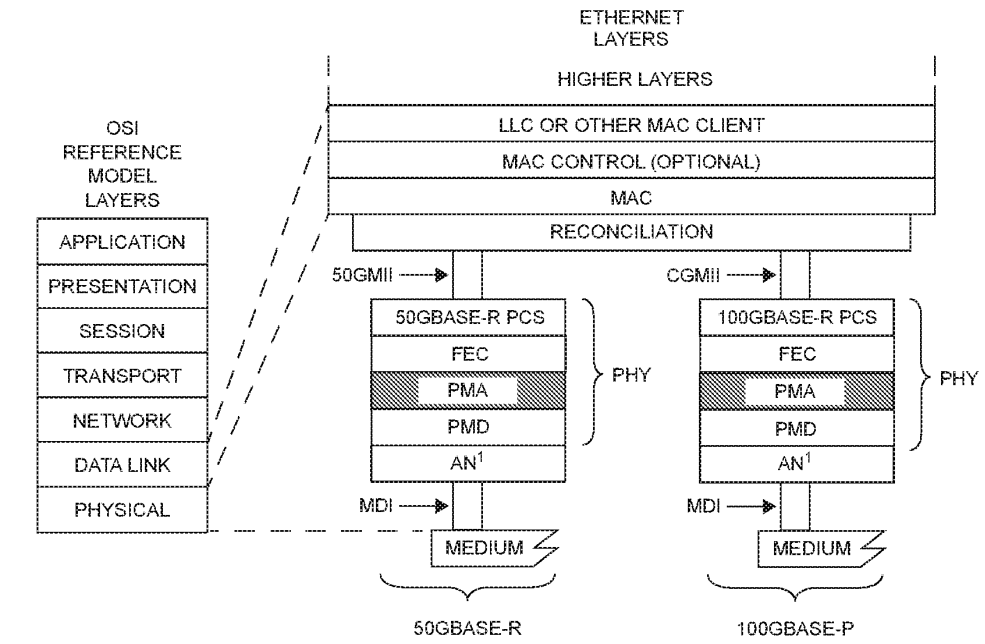
The following is a summary of the principal functions implemented (when required) by the PMA in both the transmit and receive directions:

a) Adapt the PCSL/FECL-formatted signal to the appropriate number of abstract or physical lanes.
b) Provide per-input-lane clock and data recovery.
c) Provide bit-level multiplexing.
d) Provide clock generation.
e) Provide signal drivers.
f) Optionally provide local loopback to/from the PMA service interface.
g) Optionally provide remote loopback to/from the PMD service interface.
h) Optionally provide test-pattern generation and checking.
i) Tolerate Skew Variation.
j) Perform PAM4 encoding and decoding when required

PAM4 encoding and decoding is required for 50GBASE-R PMAs where the number of physical lanes is 1 and for 100GBASE-P PMAs where the number of physical lanes is 1 or 2.

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50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 135–1—50GBASE-R and 100GBASE-P PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

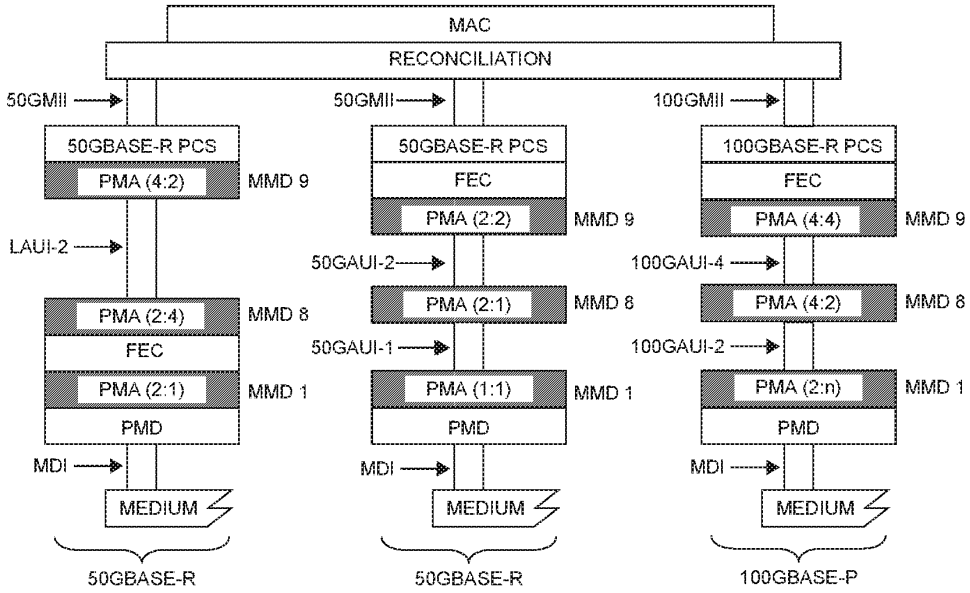
135.1.4 PMA sublayer positioning

An implementation may use one or more PMA sublayers to adapt the number and rate of the PCS lanes to the number and rate of the PMD lanes. The number of PMA sublayers required depends on the partitioning of functionality for a particular implementation. An example is illustrated in Figure 135–2. Additional examples are illustrated in Annex 135A. Each PMA maps the PCSLs/FECLs from p PMA input lanes to q PMA output lanes in the Tx direction, and from q PMA input lanes to p PMA output lanes in the Rx direction.

Management Data Input/Output (MDIO) Manageable Device (MMD) addresses 1, 8, 9, and 10 are available for addressing multiple instances of PMA sublayers (see Table 45–1 for MMD device addresses). If the PMA sublayer that is closest to the PMD is packaged with the PMD, it shares MMD 1 with the PMD. More addressable instances of PMA sublayers, each one separated from lower addressable instances by chip-to-chip interfaces, may be implemented and addressed allocating MMD addresses to PMAs in increasing numerical order going from the PMD toward the MAC. The examples shown in Figure 135–2 could be implemented with three addressable instances: MMD 1 addressing the lowest PMA sublayer (co-packaged with the PMD), MMD 8 addressing the middle PMA sublayer, and MMD 9 addressing the highest PMA sublayer (immediately below the FEC).

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100GAUI = 100 Gb/s ATTACHMENT UNIT INTERFACE
100GMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
50GAUI = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LAUI = 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

n = 1 or 2

Figure 135–2—Example 50GBASE-R and 100GBASE-P PMA layering

The number of input lanes and the number of output lanes for a PMA are always divisors of the number of PCSLs/FECLs. For PMA sublayers supporting 50GBASE-R PMDs, the number of PCSLs (above the FEC) is 4 and the number of FECLs (below the FEC) is 2. For PMA sublayers supporting 100GBASE-P PMDs, the number of FECLs is 4.

The following guidelines apply to the partitioning of PMAs:

a) The inter-sublayer service interface, defined in 131.3.1, is used for the PMA service interfaces supporting a flexible architecture with multiple PMA sublayers.
   1) An instance of this interface can only connect service interfaces with the same number of lanes, where the lanes operate at the same rate.

b) The abstract PMA service interface can be physically instantiated as a LAUI-2, 50GAUI-n, or 100GAUI-n, using associated PMAs to map to the appropriate number of lanes.

c) For physical instantiations of the PMA service interface, the PMA:IS_SIGNAL.indication is conveyed outside of this physically instantiated interface.

d) Physical instantiations of the PMA service interface define electrical and timing specification as well as requiring a receive re-timing function.

e) LAUI-2 is a physical instantiation of the PMA service interface between two adjacent 50GBASE-R PMA sublayers above the FEC.
   1) LAUI-2 provides bit-multiplexing of 4 PCSLs.
   2) LAUI-2 is a 25.78125 GBd by 2 lane NRZ physical instantiation of the 50 Gb/s connection.

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f) 50GAUI-n is a physical instantiation of the PMA service interface between two adjacent 50GBASE-R PMA sublayers below the FEC and contains 2 FECLs.

1) 50GAUI-n provides bit-multiplexing of 2 FECLs.

2) 50GAUI-2 is a 26.5625 GBd by 2 lane NRZ physical instantiation of the 50 Gb/s connection.

3) 50GAUI-1 is a 26.5625 GBd by 1 lane PAM4 physical instantiation of the 50 Gb/s connection.

g) CAUI-n is a physical instantiation of the PMA service interface between two adjacent 100GBASE-R PMA (see Clause 83) sublayers above the FEC for a 100GBASE-P PHY or between adjacent sublayers below the PCS for a 100GBASE-R PHY. CAUI-n is not specified in this clause, but is listed here for completeness.

1) CAUI-n provides bit-multiplexing of 20 PCSLs.

2) CAUI-4 is a 25.78125 GBd by 4 lane NRZ physical instantiation of the 100 Gb/s connection. CAUI-4 is specified in Clause 83 and associated annexes.

3) CAUI-10 is a 10.3125 GBd by 10 lane NRZ physical instantiation of the 100 Gb/s connection. CAUI-10 is specified Clause 83 and associated annexes.

h) 100GAUI-n is a physical instantiation of the PMA service interface between two adjacent 100GBASE-P PMA sublayers below the FEC for a 100GBASE-P PHY.

1) 100GAUI-n provides bit-multiplexing of 4 FECLs.

2) 100GAUI-4 is a 26.5625 GBd by 4 lane NRZ physical instantiation of the 100 Gb/s connection.

3) 100GAUI-2 is a 26.5625 GBd by 2 lane PAM4 physical instantiation of the 100 Gb/s connection.

i) Opportunities for optional test-pattern generation, optional test-pattern detection, optional local loopback and optional remote loopback are dependent upon the location of the PMA sublayer in the implementation. See Figure 135–5.

j) A minimum of one PMA sublayer is required in a PHY.

k) A maximum of four PMA sublayers are addressable as MDIO MMDs.

135.2 PMA interfaces

All PMA variants for 50GBASE-R and 100GBASE-P are based on a generic specification of a bit mux function that applies to all input/output lane counts and each direction of transmission. Each direction of transmission may employ one or more such bit muxes to adapt from the appropriate number of input lanes to the appropriate number of output lanes as illustrated in Figure 135–3.

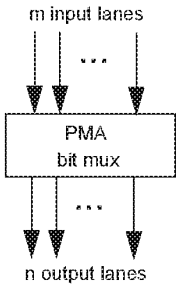


Figure 135–3—PMA bit mux used in both Tx and Rx directions

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Conceptually, the PMA bit mux operates in one direction of transmission by demultiplexing PCSLs/FECLs from m PMA input lanes and remultiplexing them into n PMA output lanes. The mapping of PCSLs/FECLs from input to output lanes is not specified. See 135.5.2 and Figure 135–4 for details.

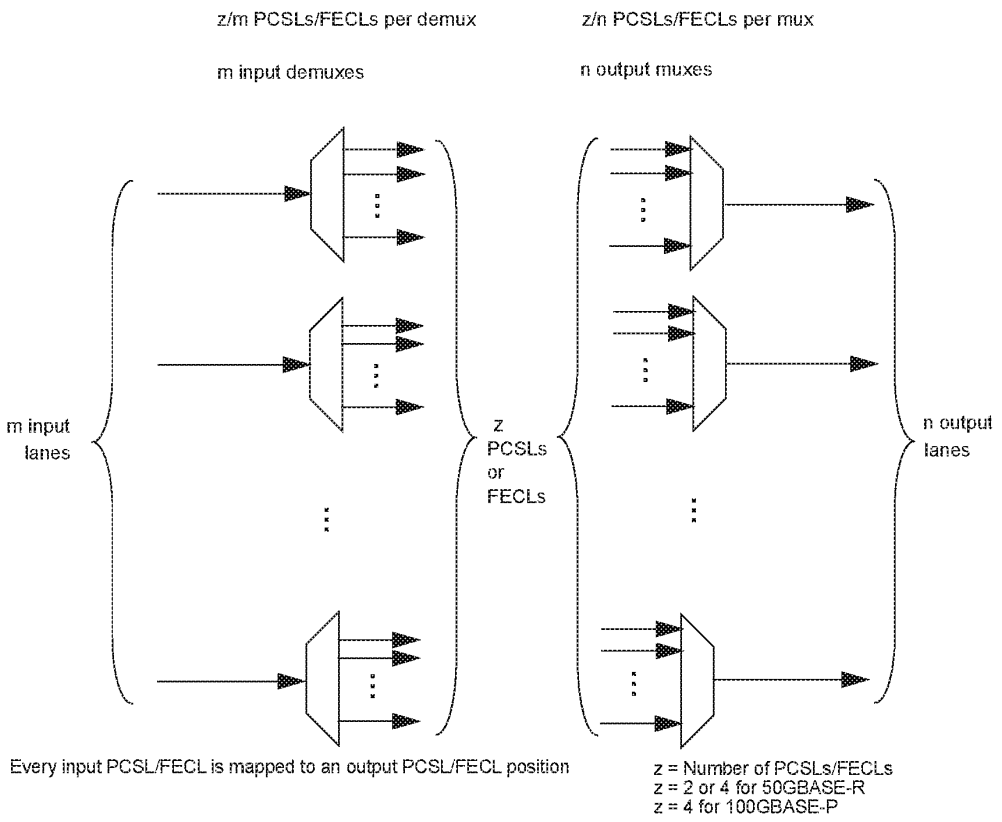


Figure 135–4—PMA bit mux operation used in both Tx and Rx directions

135.3 PMA service interface

The PMA service interface for 50GBASE-R and 100GBASE-P is an instance of the inter-sublayer service interface defined in 131.3.1. The PMA service interface primitives are summarized as follows:

PMA:IS_UNITDATA_*i*.request
PMA:IS_UNITDATA_*i*.indication)
PMA:IS_SIGNAL.indication

For a PMA service interface with p lanes, the primitives are defined for $i = 0$ to $p - 1$.

If the PMA client is the 50GBASE-R PCS, the PMA continuously sends four parallel bit streams to the PCS, each at the nominal signaling rate of the PCSL.

If a PMA client is another PMA, a 50GBASE-R PMA with p=2 physical input lanes receives NRZ symbols on each of its input lanes at 2 times the PCSL/FECL rate. A 50GBASE-R PMA with p=1 physical input lane

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receives PAM4 symbols on each of its input lanes at 2 times the PCSL/FECL rate, with each symbol formed from two bits. The bit stream represented by the input symbols carries z/p bit-multiplexed PCSLs/FECLs on each physical input lane, where z=2 (below the FEC) or z=4 (above the FEC) for 50GBASE-R.

If a PMA client is another PMA, 100GBASE-P PMA with p=4 physical input lanes receives NRZ symbols on each of its input lanes at the FECL rate. A 100GBASE-P PMA with p=1 or p=2 physical input lanes receives PAM4 symbols on each of its input lanes at 4 or 2 times, respectively, the FECL rate, with each symbol formed from two bits. The bit stream represented by the input symbols carries z/p bit-multiplexed FECLs on each physical input lane, where z=4 for 100GBASE-P.

Skew may exist between different PCSLs/FECLs received on the same physical input lane even though all PCSLs/FECLs originate from the same synchronous source, so there is independence of arrival of bits from each PCSL/FECL on each physical input lane.

In the Tx direction, if the symbol from a PMA:IS_UNITDATA_*i*.request primitive is received over a physically instantiated interface (LAUI-2, 50GAUI-n, or 100GAUI-n), clock and data are recovered on the lane receiving the symbol. If necessary, PAM4 symbols are converted to pairs of bits. Bits are routed through the PMA to an output lane through a process that may demultiplex PCSLs/FECLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs/FECLs to output lanes. If necessary, pairs of bits on output lanes are converted to PAM4 symbols. The symbols are sent on an output lane to the sublayer below using the *inst*:IS_UNITDATA_*k*.request (*k* not necessarily equal to *i*) primitive (see 135.4).

In the Rx direction, the PMA passes symbols from the input lanes to the output lanes when data is being received from every input lane from the sublayer below the PMA that has a PCSL/FECL that is routed to a particular output lane at the PMA service interface, and (if necessary) buffers are filled to allow tolerating the Skew Variation that may appear between the input lanes, PCSLs/FECLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and symbols are transferred over each output lane to the PMA client via the PMA:IS_UNITDATA_i.indication primitive. If necessary, PAM4 symbols are converted to pairs of bits on the input lanes and/or pairs of bits are converted to PAM4 symbols on the output lanes.

The PMA:IS_SIGNAL.indication primitive is generated by a Signal Indication Logic (SIL) function that reports signal health based on receipt of the *inst*:IS_SIGNAL.indication from the sublayer below, data being received on all of the input lanes from the sublayer below, buffers filled (if necessary) to accommodate Skew Variation, and symbols being sent to the PMA client on all of the output lanes. When these conditions are met, the SIGNAL_OK parameter sent to the PMA client via the PMA:IS_SIGNAL.indication primitive has the value OK. Otherwise, the SIGNAL_OK primitive has the value FAIL.

135.4 Service interface below PMA

Since the architecture supports multiple PMA sublayers for various PMD lane counts and device partitioning, there are several different sublayers that may appear below a PMA, including the FEC, PMD, or another PMA. The variable *inst* represents whichever sublayer appears below the PMA (e.g., another PMA, FEC, or PMD).

The sublayer below the PMA utilizes the inter-sublayer service interface defined in 131.3. The service interface primitives provided to the PMA are summarized as follows:

inst:IS_UNITDATA_*i*.request
inst:IS_UNITDATA_*i*.indication
inst:IS_SIGNAL.indication

The number of lanes q for the service interface matches the number of lanes expected by the PMA. The *inst*:IS_UNITDATA_*i* primitives are defined for each lane $i = 0$ to $q - 1$ of the service interface below the

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PMA. Note that electrical and timing specifications of the service interface are defined if the interface is physically instantiated (e.g., LAUI-2, 50GAUI-n, or 100GAUI-n), otherwise the service interface is specified only abstractly. The interface between the PMA and the sublayer below consists of q lanes for data transfer and a status indicating a good signal from the sublayer below the PMA (see Figure 135–5).

In the Tx direction, the PMA transfers symbols from the input lanes to the output lanes when data is being received via the PMA:IS_UNITDATA_i.request primitive from every input lane from the PMA client at the PMA service interface (see 135.3) that has a PCSL/FECL that is routed to this output lane, and (if necessary), buffers are filled to provide the ability to tolerate the Skew Variation that may appear between the input lanes from the PMA client, PCSLs/FECLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and symbols are transferred over each output lane to the sublayer below the PMA.

In the Rx direction, if the symbol is received over a physically instantiated interface (50GAUI-n, 100GAUI-n, or physically instantiated PMD service interface), clock and data are recovered on the lane receiving the symbol. If necessary, PAM4 symbols received on the input lanes are converted to pairs of bits. The bits are routed through the PMA to an output lane toward the PMA client through a process that may demultiplex PCSLs/FECLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs/FECLs to output lanes. If necessary, pairs of bits are converted to PAM4 symbols on the output lanes. Each symbol is sent on an output lane to the PMA client using the PMA:IS_UNITDATA_k.indication (k not necessarily equal to i) primitive at the PMA service interface.

135.5 Functions within the PMA

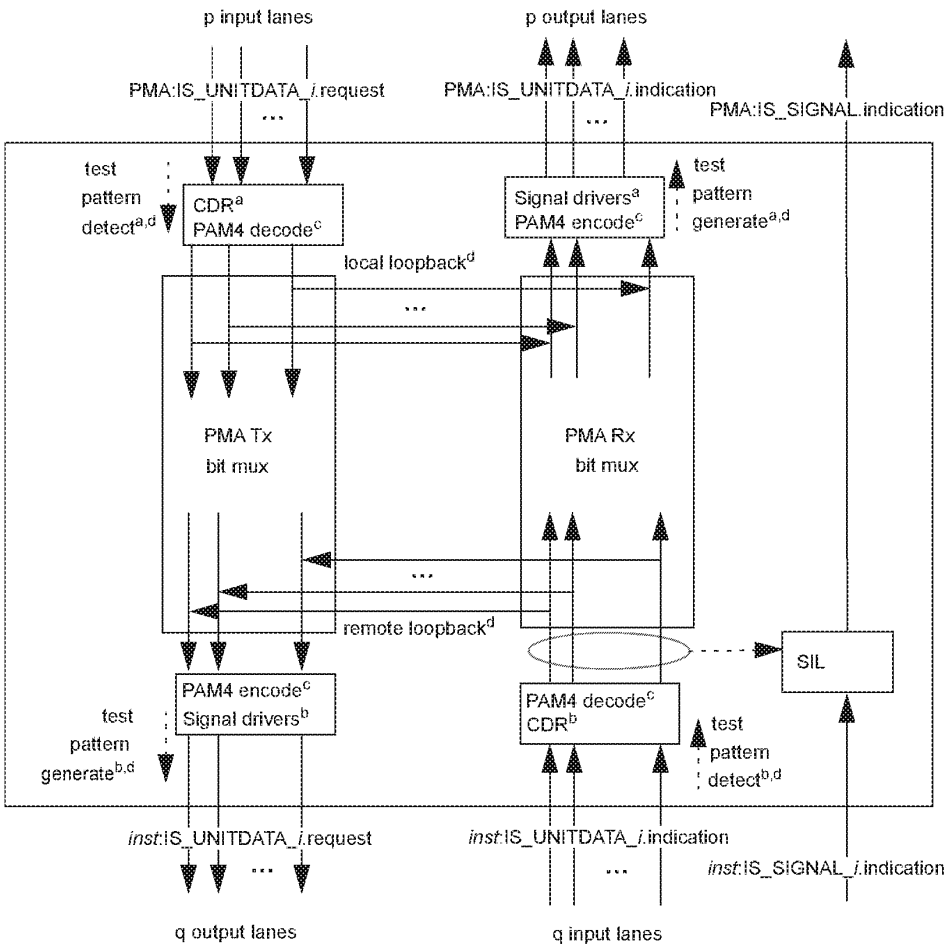
The purpose of the PMA is to adapt the PCSL/FECL-formatted signal to an appropriate number of abstract or physical lanes, to recover clock from the received signal (if appropriate), and optionally to provide test signals and loopback. Each input (Tx direction) or output (Rx direction) lane between the PMA and the PMA client carries one or more PCSLs/FECLs that are bit-multiplexed. All input and output lanes between the PMA and the PMA client carry the same number of PCSLs/FECLs and operate at the same nominal signaling rate. Likewise, each input (Rx direction) or output (Tx direction) lane between the PMA and the sublayer below the PMA carries one or more PCSLs/FECLs that are bit-multiplexed. All input and output lanes between the PMA and the sublayer below the PMA carry the same number of PCSLs/FECLs and operate at the same nominal signaling rate. As described in 135.1.4, the number of input lanes and the number of output lanes for a given PMA are divisors of 2 (below the FEC) or 4 (above the FEC) for 50GBASE-R, or 4 for 100GBASE-P, which are the number of PCSLs/FECLs for the respective PHYs.

Figure 135–5 provides the functional block diagram of a PMA. The parameters of a PMA include the following:

- The numbers of input and output lanes in each direction.
- Whether the PMA is adjacent to a physically instantiated interface (LAUI-2, 50GAUI-n, or 100GAUI-n above or below).
- Whether the PMA is adjacent to the PCS.
- Whether the PMA is adjacent to the PMD.
- Whether the PMA is adjacent to the FEC.

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inst = PMD, PMA, depending on which sublayer is below this PMA
SIL = Signal Indication Logic

[a] If LAUI-2, 50GAUI-n, or 100GAUI-n immediately above this PMA.
[b] If LAUI-2, 50GAUI-n, or 100GAUI-n immediately below this PMA or if this is the closest PMA to the PMD.
[c] If number of input or output lanes is 1 for a 50GBASE-R PMA, or 1 or 2 for a 100GBASE-P PMA.
[d] Optional.

Figure 135–5—PMA Functional Block Diagram

135.5.1 Per input-lane clock and data recovery

If the interface between the PMA client and the PMA is physically instantiated as LAUI-2, 50GAUI-n, or 100GAUI-n, the PMA shall meet the electrical and timing specifications above the PMA in Annex 135B through Annex 135G, as appropriate.

If the interface between the sublayer below the PMA and the PMA is physically instantiated as LAUI-2, 50GAUI-n, or 100GAUI-n, the PMA shall meet the electrical and timing specifications below the PMA at the service interface as specified in Annex 135B through Annex 135G, as appropriate.

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135.5.2 Bit-level multiplexing

The PMA provides bit-level multiplexing in both the Tx and Rx directions. In the Tx direction, the function is performed among the bits received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitives (for PMA client lanes $i = 0$ to $p - 1$) with the result sent to the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes $i = 0$ to $q - 1$), referencing the functional block diagram shown in Figure 135–5. The bit multiplexing behavior is illustrated in Figure 135–4.

The aggregate signal carried by the group of input lanes or the group of output lanes is arranged as a set of PCSLs/FECLs. The number of PCSLs/FECLs z is 2 FECLs (below the FEC) and 4 PCSLs (above the FEC) for 50GBASE-R interfaces and 4 FECLs for 100GBASE-P interfaces. For 50GBASE-R, the nominal bit rate R_{lane} is 12.890625 Gb/s for each PCSL and 26.5625 Gb/s for each FECL. For 100GBASE-P, the nominal bit rate R_{lane} is 26.5625 Gb/s for each FECL.

For a PMA with m input lanes (Tx or Rx direction), each input lane carries, bit multiplexed, z/m PCSLs/FECLs. Each input lane has a nominal bit rate of $z/m \times R_{lane}$. Note that the signaling rate is equal to the bit rate when the signal modulation is NRZ. The signaling rate is equal to half of the bit rate when the signal modulation is PAM4. If necessary, PAM4 symbols are converted to pairs of bits on the input lanes and/or pairs of bits are converted to PAM4 symbols on the output lanes. If bit x received on an input lane belongs to a particular PCSL/FECL, the next bit of that same PCSL/FECL is received on the same input lane at bit position $x+(z/m)$. The z/m PCSLs/FECLs may arrive in any sequence on a given input lane.

For a PMA with n output lanes (Tx or Rx direction), each output lane carries, bit multiplexed, z/n PCSLs/FECLs. Each output lane has a nominal signaling rate of $z/n \times R_{lane}$. Each PCSL/FECL is mapped from a position in the sequence on one of the m input lanes to a position in the sequence on one of the n output lanes. If bit x sent on an output lane belongs to a particular PCSL/FECL, the next bit of that same PCSL/FECL is sent on the same output lane at bit position $x + (z/n)$. The PMA shall maintain the chosen sequence of PCSLs/FECLs on all output lanes while it is receiving a valid stream of bits on all input lanes.

Each PCSL/FECL received in any temporal position on an input lane is transferred into a temporal position on an output lane. As the PCS (see Clause 133 and Clause 82) and FEC (See Clause 91 and Clause 134) have fully flexible receive logic, an implementation is free to perform the mapping of PCSLs/FECLs from input lanes to output lanes without constraint. Figure 135–6 illustrates one possible bit ordering for a 100GBASE-P 4:2 PMA bit mux. Other bit orderings are also valid.

Note that since the number of input lanes and output lanes for a 50GBASE-R or 100GBASE-P PMA is always a power of two, many PMAs converting between different numbers of lanes normally simply multiplex two or four input lanes to one output lane, or demultiplex two or four output lanes from one input lane. However, any PMA implementation which produces an allowable order of bits from all PCSLs/FECLs on the output lanes is valid.

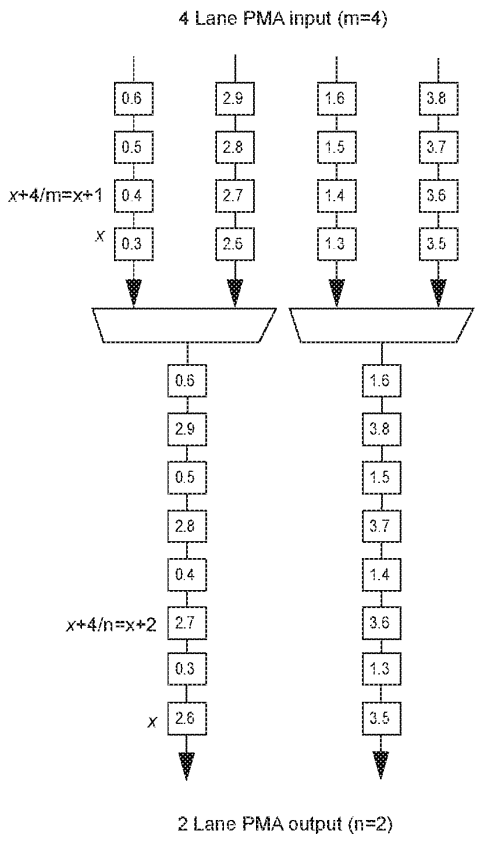
135.5.3 Skew and Skew Variation

The Skew (relative delay) between the PCSLs/FECLs must be kept within limits so that the information on the lanes can be reassembled by the PCS and FEC.

Any PMA that combines PCSLs/FECLs from different input lanes onto the same output lane must tolerate Skew Variation between the input lanes without changing the PCSL/FECL positions on the output. Skew and Skew Variation are defined in 131.5. The limits for Skew and Skew Variation at physically instantiated interfaces are specified at Skew points SP0, SP1, and SP2 in the transmit direction and SP5, SP6, and SP7 in the receive direction as defined in 131.5 and illustrated in Figure 131–3 for 50GBASE-R and as defined in 80.5 and illustrated in Figure 80–8 for 100GBASE-P.

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NOTE—i.k indicates bit k on FECL i. Skew may exist between FECLs.

Figure 135–6—Example 4:2 100GBASE-P PMA bit mux

135.5.3.1 Skew generation toward SP0

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA that sends data in the transmit direction toward the LAUI-2 (SP0 in Figure 131–3) shall produce no more than 29 ns of Skew between PCSLs and no more than 0.2 ns of Skew Variation.

135.5.3.2 Skew tolerance at SP0

In an implementation with an instantiated LAUI-2 interface, the PMA service interface that receives data in the transmit direction from the LAUI-2 (SP0 in Figure 131–3) shall tolerate the maximum amount of Skew Variation allowed at SP0 (0.2 ns) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

135.5.3.3 Skew generation toward SP1

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA that sends data in the transmit direction toward the 50GAUI-n or 100GAUI-n that is closest to the PMD (SP1 in Figure 131–3 and Figure 80–8) shall produce no more than 29 ns of Skew between FECLs toward the 50GAUI-n or 100GAUI-n and no more than 0.2 ns of Skew Variation.

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135.5.3.4 Skew tolerance at SP1

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA service interface that receives data in the transmit direction from the 50GAUI-n or 100GAUI-n (SP1 in Figure 131–3 and Figure 80–8) shall tolerate the maximum amount of Skew Variation allowed at SP1 (0.2 ns) between input lanes while maintaining the bit ordering and position of each FECL on each PMA lane in the transmit direction (toward the PMD).

135.5.3.5 Skew generation toward SP2

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, the PMA adjacent to the PMD service interface shall generate no more than 43 ns of Skew, and no more than 0.4 ns of Skew Variation between output lanes toward the PMD service interface (SP2 in Figure 80–8 and Figure 131–3). If there is a physically instantiated 50GAUI-n or 100GAUI-n as well, then the Skew measured at SP1 is limited to no more than 29 ns of Skew and no more than 0.2 ns of Skew Variation.

135.5.3.6 Skew tolerance at SP5

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, the PMA adjacent to the PMD service interface (SP5 in Figure 131–3 and Figure 80–8) shall tolerate the maximum amount of Skew Variation allowed at SP5 (0.4 ns) between output lanes from the PMD service interface while maintaining the bit ordering and position of each FECL on each PMA lane in the receive direction (toward the MAC).

135.5.3.7 Skew generation at SP6

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, at SP6 (the receive direction of the 50GAUI-n or 100GAUI-n closest to the FEC), the PMA or group of PMAs between the PMD and the 50GAUI-n or 100GAUI-n closest to the FEC shall deliver no more than 160 ns of Skew, and no more than 3.8 ns of Skew Variation between output lanes toward the 50GAUI-n or 100GAUI-n in the Rx direction. If there is a physically instantiated PMD service interface that allows the Skew to be measured, the Skew measured at SP5 is limited to no more than 145 ns of Skew and no more than 3.6 ns of Skew Variation. If there is no physically instantiated PMD service interface, the Skew measured at SP4 is limited to no more than 134 ns of Skew, and no more than 3.4 ns of Skew Variation.

135.5.3.8 Skew tolerance at SP6

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA between the 50GAUI-n or 100GAUI-n closest to the FEC and the FEC shall tolerate the maximum amount of Skew Variation allowed at SP6 (3.8 ns) between input lanes while maintaining the bit order and position of FECLs on lanes sent in the receive direction towards the MAC.

135.5.3.9 Skew generation at SP7

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA that sends data in the receive direction toward the LAUI-2 (SP7 in Figure 131–3) shall produce no more than 29 ns of Skew between PCSLs and no more than 0.2 ns of Skew Variation.

135.5.3.10 Skew tolerance at SP7

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA service interface that receives data in the receive direction from the LAUI-2 (SP7 in Figure 131–3) shall tolerate the maximum amount of Skew Variation allowed at SP7 (0.2 ns) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

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135.5.4 Delay constraints

The maximum cumulative delay contributed by up to three PMA stages in a PHY (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 135–1. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 131.4 and its references.

Table 135–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
50GBASE-R PMA	4608	9	92.16
100GBASE-P PMA	9216	18	92.16

135.5.5 Clocking architecture

A PMA with m input lanes and n output lanes shall clock the output lanes such that the bit rate of the output lanes is m/n times the bit rate of the input lanes. For input or output lanes encoded as PAM4, the symbol rate is half of the bit rate. This applies in both the Tx and Rx directions of transmission. In the case where the interfaces between the PMA client and the PMA and/or the PMA and the sublayer below the PMA are physically instantiated, the PMA may derive its input clock(s) from the electrical interface on one or more of the input lanes, and generate the output clock(s) with an appropriate PLL multiplier/divider circuit.

There is no requirement that the PMA clock all output lanes in unison. Examples of independent clocking of output lanes include the following:

— The case where the number of input and output lanes are equal (the PMA is provided for retiming and regeneration of the signal). This may be implemented without any rearrangement of PCSLs/FECLs between input lanes and output lanes (although rearrangements are allowed). Such a PMA may be implemented by driving each output lane using the clock recovered from the corresponding input lane.
— Since the number of PCSLs/FECLs is a power of 2, whenever the number of input and output lanes are unequal, each input lane could be mapped to multiple output lanes (in the case where the number of output lanes is greater), or multiple input lanes could be mapped to a single output lane.

135.5.6 Signal drivers

For cases where the interface between the PMA client and the PMA or between the PMA and the sublayer below the PMA represent a physically instantiated interface, the PMA provides electrical signal drivers for that interface. The electrical and jitter/timing specifications for these interfaces appear in

— Annex 135B for LAUI-2 C2C applications
— Annex 135C for LAUI-2 C2M applications
— Annex 135D for 50GAUI-2 and 100GAUI-4 C2C applications
— Annex 135E for 50GAUI-2 and 100GAUI-4 C2M applications
— Annex 135F for 50GAUI-1 and 100GAUI-2 C2C applications
— Annex 135G for 50GAUI-1 and 100GAUI-2 C2M applications

The modulation format is NRZ for LAUI-2, 50GAUI-2, and 100GAUI-4 and the modulation format is PAM4 for 50GAUI-1 and 100GAUI-2.

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135.5.7 PAM4 encoding

135.5.7.1 Gray coding for PAM4 encoded lanes

For lanes encoded as PAM4, the PMA transmit process shall map consecutive pairs of bits to one of four Gray-coded symbols as specified in 120.5.7.

135.5.7.2 Precoding for PAM4 encoded lanes

For lanes encoded as PAM4, the PMA shall provide 1/(1+D) mod 4 precoding capability on each transmit lane and may optionally provide 1/(1+D) mod 4 decoding capability on each receive lane.

On each transmit lane, for each Gray-coded symbol G(j), a precoded symbol P(j) shall be determined by the following algorithm, where j is an index indicating the symbol number:

$$P(j) = (G(j) - P(j\text{-}1)) \bmod 4 \qquad (135\text{–}1)$$

On each receive lane, for each precoded symbol P(j), a Gray-code symbol G(j) shall be determined by the following algorithm:

$$G(j) = (P(j) + P(j\text{-}1)) \bmod 4 \qquad (135\text{–}2)$$

The precoder is enabled independently for the transmitter and receiver on each lane (0 and 1) and interface (up towards the MAC and down towards the PMD). Precoding is enabled and disabled using variables precoder_up_tx_enable_i, precoder_up_rx_enable_i, precoder_down_tx_enable_i, precoder_down_rx_enable_i (where i is 0 or 1). If a Clause 45 MDIO is implemented, the variables precoder_up_tx_enable_i, precoder_up_rx_enable_i, precoder_down_tx_enable_i, precoder_down_rx_enable_i are accessible through register 1.600, 1.601, 1.602, and 1.603 (see 45.2.1.116h through 45.2.1.116k).

The variables precoder_up_tx_enable_i and precoder_up_rx_enable_i are always set to 0 in a PMA that does not have a physical instantiation of its service interface towards the MAC. The variables precoder_down_tx_enable_i and precoder_down_rx_enable_i are always set to 0 in a PMA that does not have a physical instantiation of its service interface towards the PMD and is not adjacent to a PMD.

In a PMA that is adjacent to a 50GBASE-CR, 50GBASE-KR, 100GBASE-CR2, 100GBASE-KR2, 200GBASE-CR4, or 200GBASE-KR4 PMD, precoder_down_tx_enable_i and precoder_down_rx_enable_i shall be set as determined by the PMD control function on lane i (see 136.8.11.7.5). The method by which the PMD control function affects these variables is implementation dependent.

135.5.8 PMA local loopback mode (optional)

PMA local loopback mode is optional. If it is implemented, it shall be as specified in this subclause.

The PMA sublayer may provide a local loopback function. The function involves looping back each input lane to the corresponding output lane. Each bit received from the PMA:IS_UNITDATA_i.request(tx_symbol) primitive is looped back toward the MAC using the PMA:IS_UNITDATA_i.indication(rx_symbol) primitive.

During local loopback, the PMA performs normal bit muxing of PCSLs/FECLs per 135.5.2 onto the lanes in the Tx direction toward the service interface below the PMA.

Ability to perform this function is indicated by the Local_loopback_ability status variable. If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.8.0 (45.2.1.7.15).

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A device is placed in local loopback mode when the Local_loopback_enable control variable is set to one, and removed from local loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD control 1 register (bit 1.0.0, see 45.2.1.1.1).

NOTE—Placing a network port into loopback mode can be disruptive to a network.

135.5.9 PMA remote loopback mode (optional)

PMA remote loopback mode is optional. If implemented, it shall be as described in this subclause.

Remote loopback, if provided, should be implemented in a PMA sublayer close enough to the PMD to maintain the bit sequence on each individual PMD lane. When remote loopback is enabled, each symbol received over a lane of the service interface below the PMA via *inst*:IS_UNITDATA_*i*.indication is looped back to the corresponding output lane toward the PMD via *inst*:IS_UNITDATA_*i*.request. Note that the service interface below the PMA can be provided by the PMD, FEC (LAUI-2 only), or another PMA sublayer.

During remote loopback, the PMA performs normal bit muxing of PCSLs/FECLs per 135.5.2 onto the lanes in the Rx direction towards the PMA client.

The ability to perform this function is indicated by the 50G_Remote_loopback_ability status variable for 50GBASE-R 100G_Remote_loopback_ability status variable for 100GBASE-P.

A device is placed in remote loopback mode when the Remote_loopback_enable control variable is set to one and removed from remote loopback mode when this variable is set to zero.

If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.13.15 (45.2.1.12.1).

If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD Control register 1 (bit 1.0.1, see 45.2.1.1.4).

135.5.10 PMA test patterns (optional)

Where the output lanes of the PMA appear on a physically instantiated interface LAUI-2, 50GAUI-n, 100GAUI-n or the PMD service interface (whether or not is physically instantiated), the PMA may optionally generate and detect test patterns. These test patterns are used to test adjacent-layer interfaces for an individual PMA sublayer or to perform testing between a physically instantiated interface of a PMA sublayer and external test equipment.

135.5.10.1 Test patterns for NRZ encoded signals

For a 50GBASE-R PMA with NRZ encoding, the test patterns in this clause may be supported.

135.5.10.1.1 PRBS31 test pattern

A PMA may optionally include a PRBS31 test-pattern generator on output lanes in either direction as specified in 120.5.11.1.1.

A PMA may optionally include a PRBS31 test-pattern checker on input lanes in either direction as specified in 120.5.11.1.1.

135.5.10.1.2 PRBS9 test pattern

A PMA may optionally include a PRBS9 test-pattern generator on output lanes in either direction as specified in 120.5.11.1.2.

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135.5.10.1.3 Square-wave test pattern

A PMA may optionally include a square-wave test-pattern generator on output lanes in either direction as specified in 120.5.11.1.3.

135.5.10.2 Test patterns for PAM4 encoded signals

For a 50GBASE-R PMA with PAM4 encoding, the test patterns described in this clause may be supported.

The PRBS13Q and quaternary square wave test patterns are enabled on a lane-by-lane basis. The patterns PRBS31Q and SSPRQ are enabled on all lanes of an interface at once. If a per-lane pattern is enabled on one or more of the lanes and a per-interface pattern is also enabled, the per-lane patterns are generated only on the indicated lanes and the per-interface pattern is generated on the remaining lanes. The behavior if more than one per-lane pattern is enabled for the same lane or more than one per-interface pattern is enabled is not defined.

Editor's note: JP03A and JP03B test patterns were deleted from P802.3bs. Since these patterns are required only by specifications reference from P802.3bs the related test pattern subclauses, MDIO variables, and other text were removed. This editor's note will be removed in D1.3.

135.5.10.2.1 PRBS13Q test pattern

A PMA may optionally include a PRBS13Q test-pattern generator as specified in 120.5.11.2.1.

135.5.10.2.2 PRBS31Q test pattern

A PMA may optionally include a PRBS31Q test-pattern generator as specified in 120.5.11.2.2.

135.5.10.2.3 SSPRQ test pattern

A PMA may optionally include a short stress pattern random quaternary (SSPRQ) test-pattern generator as specified in 120.5.11.2.3.

135.5.10.2.4 Square wave (quaternary) test pattern

Transmit square wave (quaternary) test-pattern generator optionally applies to each lane of the Tx direction PMA towards a physically instantiated 50GAUI-1 or 100GAUI-1, or towards a PAM4 PMD service interface whether or not it is physically instantiated as specified in 120.11.5.2.4.

135.6 PMA MDIO function mapping

The optional MDIO capability described in Clause 45 describes several variables that provide control and status information for and about the PMA. Since a given implementation may employ more than one PMA sublayer, the PMA control and status information is organized into multiple addressable instances, one for each possible PMA sublayer. See 45.2.1 and 135.1.4 for the allocation of MMD addresses to PMA sublayers. Control and status registers for MMD 8, 9, and 10 use the Extended PMA control and status registers at identical locations to those for MMD 1.

Mapping of MDIO control variables to PMA control variables is shown in Table 135–2. Mapping of MDIO status variables to PMA status variables is shown in Table 135–3. Mapping of MDIO counter to PMA

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counters is shown in Table 135–4. These tables provide the register and bit numbers for the PMA addressed as MMD 1. For implementations with multiple PMA sublayers, additional PMA sublayers use the corresponding register and bit numbers in MMDs 8, 9, and 10 as necessary.

Table 135–2—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PMA remote loopback	PMA/PMD control 1	1.0.1	Remote_loopback_enable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
Lane 1 up transmitter pre-coder enable	PMA precoder control up Tx	1.602.1	precoder_up_tx_enable_1
Lane 0 up transmitter pre-coder enable	PMA precoder control up Tx	1.602.0	precoder_up_tx_enable_0
Lane 1 up receiver pre-coder enable	PMA precoder control up Rx	1.603.1	precoder_up_rx_enable_1
Lane 0 up receiver pre-coder enable	PMA precoder control up Rx	1.603.0	precoder_up_rx_enable_0
Lane 1 down transmitter precoder enable	PMA precoder control down Tx	1.600.1	precoder_down_tx_enable_1
Lane 0 down transmitter precoder enable	PMA precoder control down Tx	1.600.0	precoder_down_tx_enable_0
Lane 1 down receiver pre-coder enable	PMA precoder control down Rx	1.601.1	precoder_down_rx_enable_1
Lane 0 down receiver pre-coder enable	PMA precoder control down Rx	1.601.0	precoder_down_rx_enable_0
PRBS31 pattern enable	PRBS pattern testing control	1.1501.7	PRBS31_enable
PRBS9 pattern enable	PRBS pattern testing control	1.1501.6	PRBS9_enable
PRBS31Q pattern enable	PRBS pattern testing control	1.1501.13	PRBS31Q_pattern_enable
SSPRQ pattern enable	PRBS pattern testing control	1.1501.14	SSPRQ_pattern_enable
Tx generator enable	PRBS pattern testing control	1.1501.3	PRBS_Tx_gen_enable
Tx checker enable	PRBS pattern testing control	1.1501.2	PRBS_Tx_check_enable
Rx generator enable	PRBS pattern testing control	1.1501.1	PRBS_Rx_gen_enable
Rx checker enable	PRBS pattern testing control	1.1501.0	PRBS_Rx_check_enable
Lane 0 SW enable	Square wave testing control	1.1510.0	Square_wave_enable_0
Lane 1 SW enable	Square wave testing control	1.1510.1	Square_wave_enable_1
Lane 2 SW enable	Square wave testing control	1.1510.2	Square_wave_enable_2
Lane 3 SW enable	Square wave testing control	1.1510.3	Square_wave_enable_3

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Table 135–2—MDIO/PMA control variable mapping *(continued)*

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
Lane 0 PRBS13Q enable	PRBS13Q testing control	1.1512.0	PRBS13Q_enable_0
Lane 1 PRBS13Q enable	PRBS13Q testing control	1.1512.1	PRBS13Q_enable_1
Lane 2 PRBS13Q enable	PRBS13Q testing control	1.1512.2	PRBS13Q_enable_2
Lane 3 PRBS13Q enable	PRBS13Q testing control	1.1512.3	PRBS13Q_enable_3

Table 135–3—MDIO/PMA status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMA status variable
PMA local loopback ability	PMA/PMD status 2	1.8.0	Local_loopback_ability
PMA remote loopback ability	40G/100G PMA extended ability	1.13.15	100G_Remote_loopback_ability
50G PMA remote loopback ability	50G PMA extended ability	1.22.15	50G_Remote_loopback_ ability
PRBS9 Tx generator ability	Test-pattern ability	1.1500.5	PRBS9_Tx_generator_ability
PRBS9 Rx generator ability	Test-pattern ability	1.1500.4	PRBS9_Rx_generator_ability
PRBS31Tx generator ability	Test-pattern ability	1.1500.3	PRBS31_Tx_generator_ability
PRBS31Tx checker ability	Test-pattern ability	1.1500.2	PRBS31_Tx_checker_ability
PRBS31 Rx generator ability	Test-pattern ability	1.1500.1	PRBS31_Rx_generator_ability
PRBS31 Rx checker ability	Test-pattern ability	1.1500.0	PRBS31_Rx_checker_ability
Square wave test ability	Test-pattern ability	1.1500.12	Square_wave_ability
PRBS13Q Tx generator ability	Test-pattern ability	1.1500.11	PRBS13Q_gen_Tx_ability
PRBS13Q Rx generator ability	Test-pattern ability	1.1500.10	PRBS13Q_gen_Rx_ability
PRBS31Q Tx generator ability	Test-pattern ability	1.1500.9	PRBS31Q_gen_Tx_ability
PRBS31Q Rx generator ability	Test-pattern ability	1.1500.7	PRBS31Q_gen_rx_ability
PRBS31Q Tx checker ability	Test-pattern ability	1.1500.8	PRBS31Q_Tx_checker_ability
PRBS31Q Rx checker ability	Test-pattern ability	1.1500.6	PRBS31Q_Rx_checker_ability
SSPRQ Tx generator ability	Test-pattern ability	1.1500.13	SSPRQ_gen_Tx_ability

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Table 135–4—MDIO/PMA counters mapping

MDIO variable	PMA/PMD register name	Register/bit number	PMA status variable
Error counter Tx, lane 0	PRBS Tx pattern testing error counter, lane 0	1.1600	Ln0_PRBS_Tx_test_err_counter
Error counter Tx, lane 1	PRBS Tx pattern testing error counter, lane 1	1.1601	Ln1_PRBS_Tx_test_err_counter
Error counter Tx, lane 2	PRBS Tx pattern testing error counter, lane 2	1.1602	Ln2_PRBS_Tx_test_err_counter
Error counter Tx, lane 3	PRBS Tx pattern testing error counter, lane 3	1.1603	Ln3_PRBS_Tx_test_err_counter
Error counter Rx, lane 0	PRBS Rx pattern testing error counter, lane 0	1.1700	Ln0_PRBS_Rx_test_err_counter
Error counter Rx, lane 1	PRBS Rx pattern testing error counter, lane 1	1.1701	Ln1_PRBS_Rx_test_err_counter
Error counter Rx, lane 2	PRBS Rx pattern testing error counter, lane 2	1.1702	Ln2_PRBS_Rx_test_err_counter
Error counter Rx, lane 3	PRBS Rx pattern testing error counter, lane 3	1.1703	Ln3_PRBS_Rx_test_err_counter

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135.7 Protocol implementation conformance statement (PICS) proforma for Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P[8]

135.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135.7.2 Identification

135.7.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

[8]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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135.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*P50	PMA for 50GBASE-R	135.1.1		O.1	Yes [ ] No [ ]
*P100	PMA for 100GBASE-P	135.1.1		O.1	Yes [ ] No [ ]
*LNU	Number of lanes in direction of MAC	135.1.4	Divisor of number of PCS lanes	P50: M	2 [ ] 1 [ ]
				P100:M	4 [ ] 2 [ ]
*PUN	NRZ modulation used for physically instantiated PMA service interface	135.5.6		(P50*LNU=2)+ (P100*LNU=4):M	Yes [ ] N/A [ ]
*PUP	PAM4 modulation used for physically instantiated PMA service interface	135.5.6		(P50*LNU=1)+ (P100*LNU=2):M	Yes [ ] N/A [ ]
*LND	Number of lanes in the direction of PMD	135.1.4	Divisor of number of PCS lanes	P50: M	2 [ ] 1 [ ]
				P100:M	4 [ ] 2 [ ] 1 [ ]
*PDN	NRZ modulation used for physically instantiated service interface below the PMA	135.5.6		(P50*LND=2)+ (P100*LND=4):M	Yes [ ] N/A [ ]
*PDP	PAM4 modulation used for physically instantiated service interface or PMD service interface below the PMA	135.5.6		(P50*LND=1)+ (P100*LND=2)+: M	Yes [ ] N/A [ ]
MD	MDIO	135.6	Registers and interface supported	O	Yes [ ] No [ ]

135.7.4 PICS proforma tables for Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P

135.7.4.1 Functions

Item	Feature	Subclause	Value/Comment	Status	Support
FI	Maintain lane mapping while link is in operation	135.5.2	Maintain sequence of PCSLs/FECLs on all output lanes	M	Yes [ ]

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135.7.4.2 Timing

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Skew generation toward SP0 in Tx direction	135.5.3.1	≤ 29 ns	PID:M	Yes [ ] N/A [ ]
S2	Skew Variation generation toward SP0 in Tx direction	135.5.3.1	≤ 200 ps	PID:M	Yes [ ] N/A [ ]
S3	Skew Variation tolerance at SP0	135.5.3.2	Minimum 200 ps	PIU:M	Yes [ ] N/A [ ]
S4	Skew generation toward SP1 in Tx direction	135.5.3.3	≤ 29 ns	PID:M	Yes [ ] N/A [ ]
S5	Skew Variation generation toward SP1 in Tx direction	135.5.3.3	≤ 200 ps	PID:M	Yes [ ] N/A [ ]
S6	Skew Variation tolerance at SP1	135.5.3.4	Minimum 200 ps	PIU:M	Yes [ ] N/A [ ]
S7	Skew generation toward SP2 in Tx direction	135.5.3.5	≤ 43 ns	PIP:M	Yes [ ] N/A [ ]
S8	Skew Variation generation toward SP2 in Tx direction	135.5.3.5	≤ 400 ps	PIP:M	Yes [ ] N/A [ ]
S9	Skew Variation tolerance at SP5	135.5.3.6	Minimum 3.6 ns	PIP:M	Yes [ ] N/A [ ]
S10	Skew generation toward SP6 in Rx direction	135.5.3.7	≤ 160 ns	PIU:M	Yes [ ] N/A [ ]
S11	Skew Variation generation toward SP6 in Rx direction	135.5.3.7	≤ 3.8 ns	PIU:M	Yes [ ] N/A [ ]
S12	Skew Variation tolerance at SP6	135.5.3.8	Minimum 3.8 ns	PID:M	Yes [ ] N/A [ ]
S13	Skew generation toward SP7 in Rx direction	135.5.3.9	≤ 160 ns	PIU:M	Yes [ ] N/A [ ]
S14	Skew Variation generation toward SP7 in Rx direction	135.5.3.9	≤ 3.8 ns	PIU:M	Yes [ ] N/A [ ]
S15	Skew Variation tolerance at SP7	135.5.3.10	Minimum 3.8 ns	PID:M	Yes [ ] N/A [ ]
S16	Round-trip delay limit for 50GBASE-R	135.5.4	No more than 18 432 BT or 36 pause_quanta	P50:M	Yes [ ] N/A [ ]
S17	Round-trip delay limit for 100GBASE-P	135.5.4	No more than 36 864 BT or 72 pause_quanta	P100:M	Yes [ ] N/A [ ]

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135.7.4.3 Electrical

Item	Feature	Subclause	Value/Comment	Status	Support
E1	Lane signaling rate for LAUI-2		25.78125 GBd	M	Yes [ ]
E2	Lane signaling rate for 50GAUI-2		26.5625 GBd	M	Yes [ ]
E3	Lane signaling rate for 50GAUI-1		26.5625 GBd	M	Yes [ ]
E4	Lane signaling rate for one-lane 50 Gb/s PMD service interface.		26.5625 GBd	M	Yes [ ]
E5	Lane signaling rate for 100GAUI-4		26.5625 GBd	M	Yes [ ]
E6	Lane signaling rate for 100GAUI-2		26.5625 GBd	M	Yes [ ]
E7	Lane signaling rate for two-lane PMD service interface.		26.5625 GBd	M	Yes [ ]
E8	Lane signaling rate for one-lane PMD service interface.		53.125 GBd	M	Yes [ ]
E9	Electrical and timing requirements of Annex 135B through Annex 135G as appropriate met by upstream LAUI-2, 50GAUI-n or 100GAUI-n	135.5.1, 135.5.5		PIU:M	Yes [ ] N/A [ ]
E10	Electrical and timing requirements of Annex 135B through Annex 135G as appropriate met by downstream LAUI-2, 50GAUI-n or 100GAUI-n	135.5.1, 135.5.5		PID:M	Yes [ ] N/A [ ]

135.7.4.4 Diagnostics

Item	Feature	Subclause	Value/Comment	Status	Support
*LBL	PMA local loopback	135.5.8	Supports local loopback	O	Yes [ ] No [ ]
*LBR	PMA remote loopback	135.5.9	Supports remote loopback	O	Yes [ ] No [ ]
D1	PMA local loopback implemented	135.5.8	Meets the requirements of 135.5.8	LBL:M	Yes [ ] N/A [ ]
D2	PMA remote loopback implemented	135.5.9	Meets the requirements of 135.5.9	LBR:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
D3	Send PRBS31 Tx	135.5.10.1.1		PDN:O	Yes [ ] No [ ] N/A[ ]
D4	Send PRBS31 Rx	135.5.10.1.1		PUN:O	Yes [ ] No [ ] N/A[ ]
D5	Check PRBS31 Tx	135.5.10.1.1		PUN:O	Yes [ ] No [ ] N/A[ ]
D6	Check PRBS31 Rx	135.5.10.1.1		PDN:O	Yes [ ] No [ ] N/A[ ]
D7	Send PRBS9 Tx	135.5.10.1.2		PDN:O	Yes [ ] No [ ] N/A[ ]
D8	Send PRBS9 Rx	135.5.10.1.2		PUN:O	Yes [ ] No [ ] N/A[ ]
D9	Send NRZ square wave Tx	135.5.10.1.3		PDN:O	Yes [ ] No [ ] N/A[ ]
D10	Send PRBS13Q Tx	135.5.10.2.1		PDP:O	Yes [ ] No [ ] N/A[ ]
D11	Send PRBS13Q Rx	135.5.10.2.1		PUP:O	Yes [ ] No [ ] N/A[ ]
D12	Send PRBS31Q Tx	135.5.10.2.2		PDP:O	Yes [ ] No [ ] N/A[ ]
D13	Send PRBS31Q Rx	135.5.10.2.2		PUP:O	Yes [ ] No [ ] N/A[ ]
D14	Check PRBS31Q Tx	135.5.10.2.2		PUP:O	Yes [ ] No [ ] N/A[ ]
D15	Check PRBS31Q Rx	135.5.10.2.2		PDP:O	Yes [ ] No [ ] N/A[ ]
D16	Send SSPRQ Tx	135.5.10.2.3		PDP:O	Yes [ ] No [ ] N/A[ ]
D17	Send quaternary square wave Tx	135.5.10.2.4		PDP:O	Yes [ ] No [ ] N/A[ ]

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135.7.7 Encoding

Item	Feature	Subclause	Value/Comment	Status	Support
E1	PMA supports Gray coding	135.5.7.2		PUP+PDP:M	Yes [ ] N/A [ ]
E2	PMA supports Tx precoding	135.5.7.2		PUP+PDP:M	Yes [ ] N/A [ ]
E3	PMA supports Rx precoding	135.5.7.2		PUP+PDP:O	Yes [ ] No [ ] N/A [ ]

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136. Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136.1 Overview

This clause specifies the 50GBASE-CR PMD, the 100GBASE-CR2 PMD, the 200GBASE-CR4 PMD, and the baseband medium. The specifications for the three PMDs are similar, except for the number of lanes and associated parameters and the MDI.

There are three associated annexes. Annex 136A provides information on parameters with test points that may not be testable in an implemented system. Annex 136B specifies test fixtures. Annex 136C describes 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 host and cable assembly form factors.

When forming a complete Physical Layer, a PMD shall be connected as illustrated in Figure 136–1, to the appropriate sublayers (as specified in Table 136–1, Table 136–2, and Table 136–3), to the medium through the appropriate MDI, and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 136–1—Physical Layer clauses associated with the 50GBASE-CR PMD

Associated clause	50GBASE-CR
132—RS	Required
132—50GMII[a]	Optional
133—PCS for 50GBASE-R	Required
134—RS-FEC	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135D—50GAUI-2 C2C	Optional
135F—50GAUI-1 C2C	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The 50GMII is an optional interface. However, if the 50GMII is not implemented, a conforming implementation must behave functionally as though the RS and 50GMII were present.

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Table 136–2—Physical Layer clauses associated with the 100GBASE-CR2 PMD

Associated clause	100GBASE-CR2
80—RS	Required
80—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R	Optional[b]
83A—CAUI-10	Optional
83D—CAUI-4 C2C	Optional
135—PMA for 100GBASE-P	Required
135D—100GAUI-4 C2C	Optional
135F—100GAUI-2 C2C	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.
[b]PMA for 100GBASE-R is required when either CAUI-10 or CAUI-4 is used.

Table 136–3—Physical Layer clauses associated with the 200GBASE-CR4 PMD

Associated clause	200GBASE-CR4
117—RS	Required
117—200GMII[a]	Optional
119—PCS for 200GBASE-R	Required
120—PMA for 200GBASE-R	Required
120B—200GAUI-8 C2C	Optional
120D—200GAUI-4 C2C	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The 200GMII is an optional interface. However, if the 200GMII is not implemented, a conforming implementation must behave functionally as though the RS and 200GMII were present.

For the 50GBASE-CR and 100GBASE-CR2 PHYs, in order to support the required frame loss ratio (see 1.4.223) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are required to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 10^{-10} after processing by the RS-FEC (Clause 134 or Clause 91) and the PCS (Clause 133 or Clause 82) if there are negligible errors due to other electrical interfaces (50GAUI-n or 100GAUI-n). If the PMD and

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PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 10^{-10}.

For the 200GBASE-CR4 PHY, in order to support the required frame loss ratio (see 1.4.223) of less than 6.2×10^{-11} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are required to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 9.2×10^{-13} after processing by the PCS (Clause 119) if there are negligible errors due to other electrical interfaces (200GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 9.2×10^{-13}.

A compliant input signal is a transmitter output of a compliant PHY that has passed through a compliant cable assembly.

50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Figure 136–1 shows the relationship of the 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMD sublayers and MDIs to the ISO/IEC Open System Interconnection (OSI) reference model.

136.2 Conventions

Clause 136 describes three PMDs, 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMD, which have one, two, and four lanes, respectively. For efficient description, the parameter n is used to describe the number of lanes in a specific PMD. Accordingly, n = 1 for 50GBASE-CR, n = 2 for 100GBASE-CR2, and n = 4 for 200GBASE-CR4.

The parameter *i* is used as an index or a suffix to identify a specific lane, and takes the values 0 to n – 1.

Within this clause, the unqualified term "PMD" refers to any of 50GBASE-CR PMD, 100GBASE-CR2 PMD, or 200GBASE-CR4 PMD.

136.3 PMD service interfaces

This subclause specifies the services provided by the 50GBASE-CR, 100GBASE-CR2 and 200GBASE-CR4 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

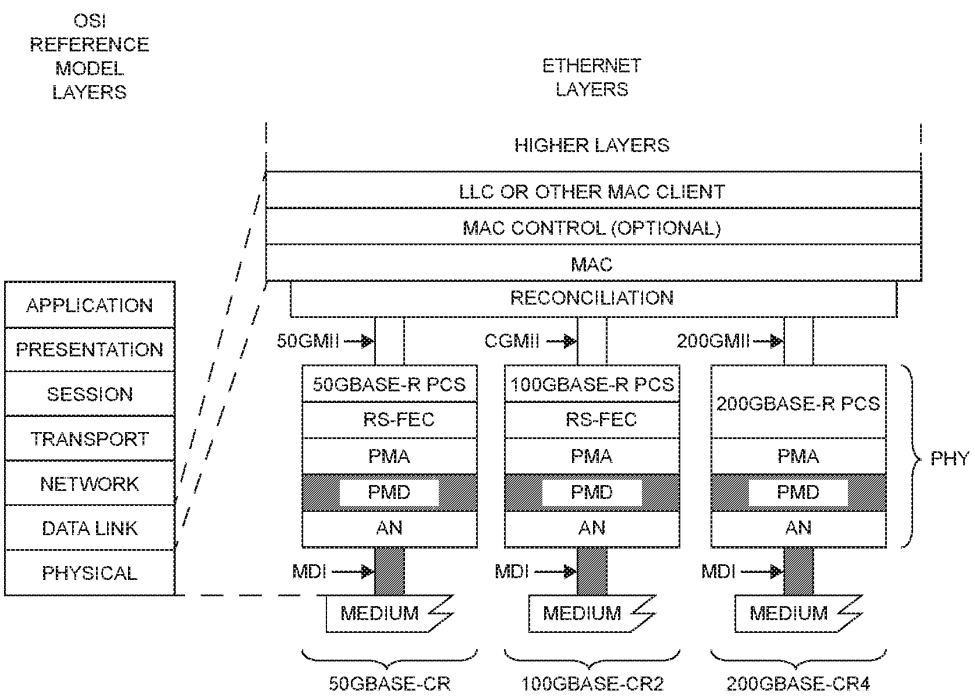
The 50GBASE-CR PMD service interface is an instance of the inter-sublayer service interface defined in 131.3, with a single symbol stream (n = 1).

The 100GBASE-CR2 PMD service interface is an instance of the inter-sublayer service interface defined in 136.3, with the exception that there are two parallel symbol streams (n = 2).

The 200GBASE-CR4 PMD service interface is an instance of the inter-sublayer service interface defined in 136.3, with four parallel symbol streams (n = 4).

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200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 136–1—50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 50GBASE-SR PMD has a single symbol stream, hence $i = 0$.

The 100GBASE-SR2 PMD has two parallel symbol streams, hence $i = 0$ to 1.

The 200GBASE-SR4 PMD has four parallel symbol streams, hence $i = 0$ to 3.

In the transmit direction, the PMA continuously sends n streams of PAM4 symbols to the PMD, one per lane, using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.6525 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

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In the receive direction, the PMD continuously sends *n* streams of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, one per lane, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.6525 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable Global_PMD_signal_detect as defined in 136.8.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_OK is FAIL, the PMD:IS_UNITDATA_*i*.indication parameter is undefined.

136.4 PCS requirements for Auto-Negotiation (AN) service interface

The PCSs associated with the 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMDs are required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 133.4, 82.6, and 119.6.)

50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR-4 PHYs may be extended using chip-to-chip (C2C) 50GAUI-n/LAUI-2, 100GAUI-n/CAUI-n, and 200GAUI-n, respectively, as physical instantiations of the inter-sublayer service interface between devices. If such extension is used, then the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

136.5 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the PMD and AN including the medium in one direction shall be no more than the maximum delays listed in Table 136–4. It is assumed that the one-way delay through the medium is no more than 20 ns.

Table 136–4—Delay constraints

PMD	Maximum (bit times)[a]	Maximum (pause_quanta)[b]	Maximum (ns)
50GBASE-CR	2048	4	40.96
100GBASE-CR2	4096	8	40.96
200GBASE-CR4	8192	16	40.96

[a]One bit time is equal to 20 ps for 50GBASE-CR, 10 ps for 100GBASE-CR2, and 5 ps for 200GBASE-CR4. (See 1.4.117 for the definition of bit time.)
[b]One pause_quantum is equal to 10.24 ns for 50GBASE-CR, 5.12 ns for 100GBASE-CR2, and 2.56 ns for 200GBASE-CR4. (See 31B.2 for the definition of pause_quanta.)

Descriptions of overall system delay constraints can be found in 131.4 for 50GBASE-CR, in 80.4 for 100GBASE-CR2, and in 116.4 for 200GBASE-CR4.

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136.6 Skew constraints

The Skew (relative delay) between the PCS or FEC lanes must be kept within limits so that the information on the PCS or FEC lanes can be reassembled by the PCS or FEC. The Skew Variation must also be limited to ensure that a given PCS or FEC lane always traverses the same physical lane.

136.6.1 Skew Constraints for 50GBASE-CR

Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2.

136.6.2 Skew Constraints for 100GBASE-CR2 and 200GBASE-CR4

Skew and Skew Variation are defined in 80.5 and 116.5 and specified at the points SP1 to SP6 shown in Figure 80–8 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5 and 116.5.

136.7 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD

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control variables as shown in Table 136–5, and MDIO status bits to PMD status variables as shown in Table 136–6.

Table 136–5—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 3 to PMD transmit disable 2[a]	PMD transmit disable	1.9.4:3	PMD_transmit_disable_3, PMD_transmit_disable_2
PMD transmit disable 1[b]	PMD transmit disable	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable	1.9.1	PMD_transmit_disable_0
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable
Polynomial identifier 3[a]	PMD training pattern lane 3	1.1453.12:11	identifier_3
Seed 3[a]	PMD training pattern lane 3	1.1453.10:0	seed_3
Polynomial identifier 2[a]	PMD training pattern lane 2	1.1452.12:11	identifier_2
Seed 2[a]	PMD training pattern lane 2	1.1452.10:0	seed_2
Polynomial identifier 1[b]	PMD training pattern lane 1	1.1451.12:11	identifier_1
Seed 1[b]	PMD training pattern lane 1	1.1451.10:0	seed_1
Polynomial identifier 0	PMD training pattern lane 3	1.1450.12:11	identifier_0
Seed 0	PMD training pattern lane 3	1.1450.10:0	seed_0
Initial condition request 3[a]	PMD training LP control lane 3	1.1123.13:12	ic_req (lane 3)
Coefficient select 3[a]	PMD training LP control lane 3	1.1123.4:2	coef_sel (lane 3)
Coefficient request 3[a]	PMD training LP control lane 3	1.1123.1:0	coef_req (lane 3)
Initial condition request 2[a]	PMD training LP control lane 2	1.1122.13:12	ic_req (lane 2)
Coefficient select 2[a]	PMD training LP control lane 2	1.1122.4:2	coef_sel (lane 2)
Coefficient request 2[a]	PMD training LP control lane 2	1.1122.1:0	coef_req (lane 2)
Initial condition request 1[b]	PMD training LP control lane 1	1.1121.13:12	ic_req (lane 1)
Coefficient select 1[b]	PMD training LP control lane 1	1.1121.4:2	coef_sel (lane 1)
Coefficient request 1[b]	PMD training LP control lane 1	1.1121.1:0	coef_req (lane 1)
Initial condition request 0	PMD training LP control lane 0	1.1120.13:12	ic_req (lane 0)
Coefficient select 0	PMD training LP control lane 0	1.1120.4:2	coef_sel (lane 0)
Coefficient request 0	PMD training LP control lane 0	1.1120.1:0	coef_req (lane 0)

[a]Available only in 200GBASE-CR4.
[b]Available only in 100GBASE-CR2 and 200GBASE-CR4.

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Table 136–6—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 2[a]	PMD receive signal detect	1.10.4:3	PMD_signal_detect_3 to PMD_signal_detect_2
PMD receive signal detect 1[b]	PMD receive signal detect	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect	1.10.1	PMD_signal_detect_0
Receiver status 3[a]	BASE-R PMD status	1.151.12	rx_trained_3
Frame lock 3[a]	BASE-R PMD status	1.151.13	local_frame_lock_3
Start-up protocol status 3[a]	BASE-R PMD status	1.151.14	training_3
Training failure 3[a]	BASE-R PMD status	1.151.15	training_failure_3
Receiver status 2[a]	BASE-R PMD status	1.151.8	rx_trained_2
Frame lock 2[a]	BASE-R PMD status	1.151.9	local_frame_lock_2
Start-up protocol status 2[a]	BASE-R PMD status	1.151.10	training_2
Training failure 2[a]	BASE-R PMD status	1.151.11	training_failure_2
Receiver status 1[b]	BASE-R PMD status	1.151.4	rx_trained_1
Frame lock 1[b]	BASE-R PMD status	1.151.5	local_frame_lock_1
Start-up protocol status 1[b]	BASE-R PMD status	1.151.6	training_1
Training failure 1[b]	BASE-R PMD status	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status	1.151.0	rx_trained_0
Frame lock 0	BASE-R PMD status	1.151.1	local_frame_lock_0
Start-up protocol status 0	BASE-R PMD status	1.151.2	training_0
Training failure 0	BASE-R PMD status	1.151.3	training_failure_0
Receiver ready 3[a]	PMD training LP status lane 3	1.1223.15	remote_rx_ready (lane 3)
Modulation and precoding status 3[a]	PMD training LP status lane 3	1.1223.11:10	tp_mode (lane 3)
Receiver frame lock 3[a]	PMD training LP status lane 3	1.1223.9	remote_tf_lock (lane 3)
Initial condition status 3[a]	PMD training LP status lane 3	1.1223.8	ic_sts (lane 3)
Coefficient status 3[a]	PMD training LP status lane 3	1.1223.2:0	coef_sts (lane 3)
Receiver ready 2[a]	PMD training LP status lane 2	1.1222.15	remote_rx_ready (lane 2)
Modulation and precoding status 2[a]	PMD training LP status lane 2	1.1222.11:10	tp_mode (lane 2)
Receiver frame lock 2[a]	PMD training LP status lane 2	1.1222.9	remote_tf_lock (lane 2)
Initial condition status 2[a]	PMD training LP status lane 2	1.1222.8	ic_sts (lane 2)

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Table 136–6—MDIO/PMD status variable mapping *(continued)*

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Coefficient status 2[a]	PMD training LP status lane 2	1.1222.2:0	coef_sts (lane 2)
Receiver ready 1[b]	PMD training LP status lane 1	1.1221.15	remote_rx_ready (lane 1)
Modulation and precoding status 1[b]	PMD training LP status lane 1	1.1221.11:10	tp_mode (lane 1)
Receiver frame lock 1[b]	PMD training LP status lane 1	1.1221.9	remote_tf_lock (lane 1)
Initial condition status 1[b]	PMD training LP status lane 1	1.1221.8	ic_sts (lane 1)
Coefficient status 1[b]	PMD training LP status lane 1	1.1221.2:0	coef_sts (lane 1)
Receiver ready 0	PMD training LP status lane 0	1.1220.15	remote_rx_ready (lane 0)
Modulation and precoding status 0	PMD training LP status lane 0	1.1220.11:10	tp_mode (lane 0)
Receiver frame lock 0	PMD training LP status lane 0	1.1220.9	remote_tf_lock (lane 0)
Initial condition status 0	PMD training LP status lane 0	1.1220.8	ic_sts (lane 0)
Coefficient status 0	PMD training LP status lane 0	1.1220.2:0	coef_sts (lane 0)

[a]Available only in 200GBASE-CR4.
[b]Available only in 100GBASE-CR2 and 200GBASE-CR4.

136.8 PMD functional specifications

136.8.1 Link block diagram

One direction of a 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4 link is shown in Figure 136–2.

Note that the source lane (SL) signals SL_i<p> and SL_i<n> are the positive and negative sides of the transmitter's differential signal pair on lane *i* and the destination lane (DL) signals DL_i<p> and DL_i<n> are the positive and negative sides of the receiver's differential signal pair on lane *i*.

For purposes of system conformance, the PMD sublayer is standardized at the test points described in this subclause.

The electrical transmit signal is defined at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 136.9.3 are made at TP2 utilizing the test fixture specified in 136B.1.1.

The electrical receive signal is defined at TP3. Unless specified otherwise, all receiver measurements and tests defined in 136.9.4 are performed at TP3 utilizing the test fixture specified in 136B.1.1.

A mated connector pair has been included in both the transmitter and receiver specifications defined in 136.9.3 and 136.9.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is provided in 92.8.3.6. Annex 136A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system.

The channel (see 136.9) is defined between the transmitter (TP0) and receiver (TP5) blocks to include the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss, as illustrated in Figure 136–2. All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 136–2. The cable assembly test fixture of 136B.1.1, or its

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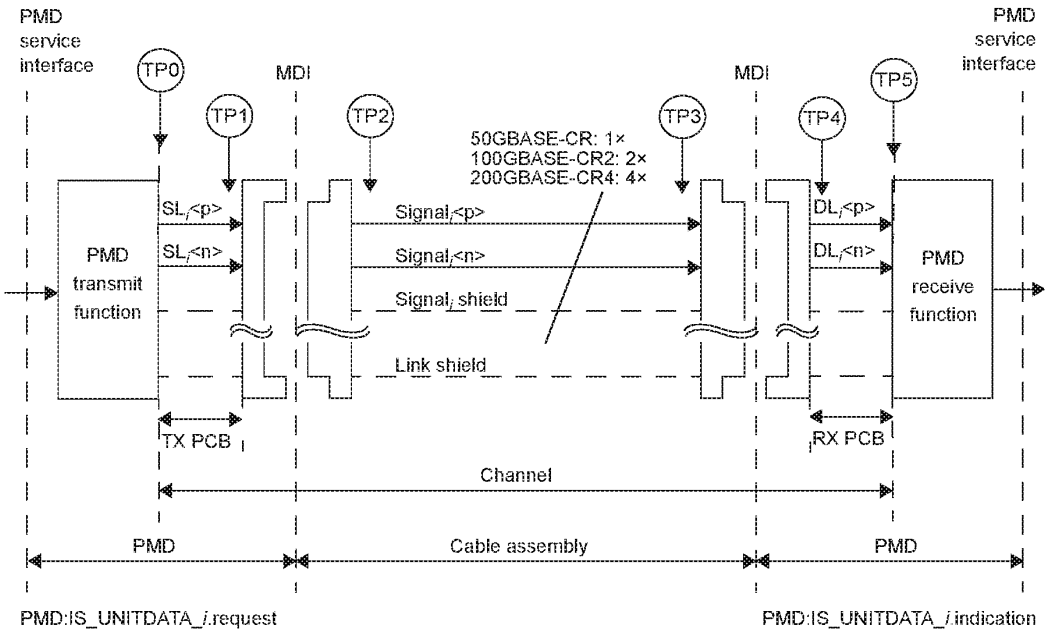


Figure 136–2—50GBASE-CR, 100GBASE-CR2 or 200GBASE-CR4 link (one direction is illustrated)

equivalent, is required for measuring the cable assembly specifications in 136.10 at TP1 and TP4. Two mated connector pairs and the cable assembly test fixture have been included in the cable assembly specifications defined in 136.10. Transmitter and receiver differential controlled impedance printed circuit board insertion losses defined between TP0 and the MDI and between the MDI and TP5, respectively, are provided informatively in 136A.4.

Table 136–7 describes the defined test points illustrated in Figure 136–2.

Table 136–7—Test points

Test points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 136–2. The cable assembly test fixture of 136B.1.1, or its equivalent, is required for measuring the cable assembly specifications in 136.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 136.9.3 and 136.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 92.8.3.6.
TP2	Unless specified otherwise, all transmitter measurements defined in 136.9.3 are made at TP2 utilizing the test fixture specified in 136B.1.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 136.9.4 are made at TP3 utilizing the test fixture specified in 136B.1.1.

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136.8.2 PMD transmit function

The PMD transmit function has two operating modes, DATA and TRAINING. The operating mode is controlled by the PMD control state diagram (Figure 136–7).

When operating in DATA mode, the PMD transmit function shall convert the symbol stream requested by the PMD service interface message PMD:IS_UNITDATA_*i*.request(tx_symbol) of each lane into an electrical signal, and deliver the electrical signals to the MDI, according to the transmit electrical specifications in 136.9.3. The highest differential output voltage (SL_i<p> minus SL_i<n>) shall correspond to tx_symbol = three and the lowest differential output voltage shall correspond to tx_symbol = zero.

When operating in TRAINING mode, the PMD transmit function shall convert the symbol stream generated by the PMD control function of each lane into an electrical signal, and deliver the electrical signals to the MDI, according to the transmit electrical specifications in 136.9.3. The highest differential output voltage (SL_i<p> minus SL_i<n>) shall correspond to the symbol 3 and the lowest differential output voltage shall correspond to the symbol 0.

136.8.3 PMD receive function

The PMD receive function shall convert the electrical signal from each of the lanes on the MDI into a symbol stream for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_*i*.indication(rx_symbol). The highest differential input voltage (DL_i<p> minus DL_i<n>) shall correspond to rx_symbol = three and the lowest differential input voltage shall correspond to rx_symbol = zero.

136.8.4 PMD global signal detect function

For the 50GBASE-CR PMD, the variable Global_PMD_signal_detect is set to PMD_signal_detect_0 (see 136.8.5). For the 100GBASE-CR2 and 200GBASE-CR4 PMDs, the variable Global_PMD_signal_detect is set to the logical AND of the values of PMD_signal_detect_*i* from each of the PMD lanes.

136.8.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function is used by the PMD to indicate the successful completion of the start-up protocol by the PMD control function (see 136.8.11). PMD_signal_detect_*i* shall be set to zero when signal_detect on lane *i* is set to false, and to one when signal_detect on lane *i* is set to true. The signal_detect variables are set independently on each lane by the PMD control state diagram (Figure 136–7).

If training is disabled by the management variable mr_training_enable (see 136.7), PMD_signal_detect_*i* shall be set to one for all lanes.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 136.7.

136.8.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional. When implemented, it allows the transmitters on all lanes to be disabled with a single variable.

When Global_PMD_transmit_disable variable is set to one, this function shall turn off all the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max.) with Tx disabled in Table 136–11.

If a PMD fault (136.8.8) is detected, then the PMD may set Global_PMD_transmit_disable to one.

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136.8.7 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function allows the transmitter in each lane to be selectively disabled.

When a PMD_transmit_disable_*i* variable is set to one, this function shall turn off the transmitter in lane *i* so that it drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max.) with Tx disabled in Table 136–11.

If a PMD fault (136.8.8) is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the transmitter in each lane.

If MDIO is not implemented, an alternative method shall be provided to access the PMD_transmit_disable_*i* variables in order to enable independently disabling each transmit lane for testing purposes.

136.8.8 PMD fault function

PMD_fault is the logical-OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault. If the MDIO interface is implemented, then PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

136.8.9 PMD transmit fault function (optional)

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault.

If PMD_transmit_fault is set to one, then Global_PMD_transmit_disable should also be set to one.

If the MDIO interface is implemented, then PMD_transmit_fault shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

136.8.10 PMD receive fault function (optional)

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall be mapped to the Receive fault bit as specified in 45.2.1.7.5.

136.8.11 PMD control function

The PMD control function performs the PMD start-up protocol. This protocol facilitates timing recovery and equalization while providing a mechanism through which the receiver can configure the transmitter to optimize performance. The protocol supports these functions through the continuous exchange of fixed-length training frames.

The PMD shall implement one instance of the PMD control function described in this subclause for each lane. The PMD control functions operate independently on each lane.

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136.8.11.1 Training frame structure

The training frame is a sequence of PAM4 symbols whose values correspond to the possible values of the tx_symbol and rx_symbol variables (the symbol values 0, 1, 2, and 3 correspond to tx_symbol or rx_symbol values zero, one, two, and three, respectively). The structure of a training frame is shown in Figure 136–3.

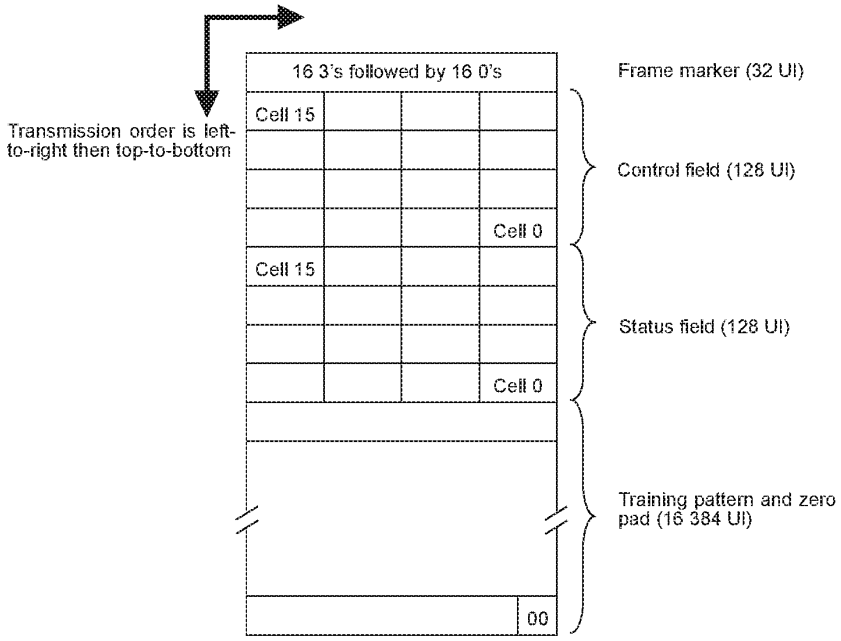


Figure 136–3—Training frame structure

136.8.11.1.1 Frame marker

Training frames are delimited by a specific sequence of PAM4 symbols. The training frame marker is a run of 16 consecutive "3" symbols followed by a run of 16 consecutive "0" symbols. This sequence is not found in the control field, status field, or training pattern and it uniquely identifies the beginning of a training frame.

136.8.11.1.2 Control and status fields

The control field comprises 16 bits with the structure defined in 136.8.11.2. The status field comprises 16 bits with the structure defined in 136.8.11.3.

Each bit of the control and status fields is sent as a differential Manchester encoded cell where each cell is eight unit intervals in length. The specific rules for this encoding follow.

a) A transition from 0 to 3 or from 3 to 0 occurs at the start of the cell.

b) A transition from 0 to 3 or from 3 to 0 at the midpoint of the cell, i.e., four unit intervals from the transition at the beginning of the cell, corresponds to a logical one.

c) The absence of a transition at the midpoint of the cell corresponds to a logical zero.

The control field is transmitted immediately after the frame marker where the first cell transmitted corresponds to the highest bit index in the field. The status field is transmitted immediately after the control field where the first cell transmitted corresponds to the highest bit index in the field.

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136.8.11.1.3 Training pattern

The training pattern is the result of a training pattern generator equivalent to the structure shown in Figure 136–4.

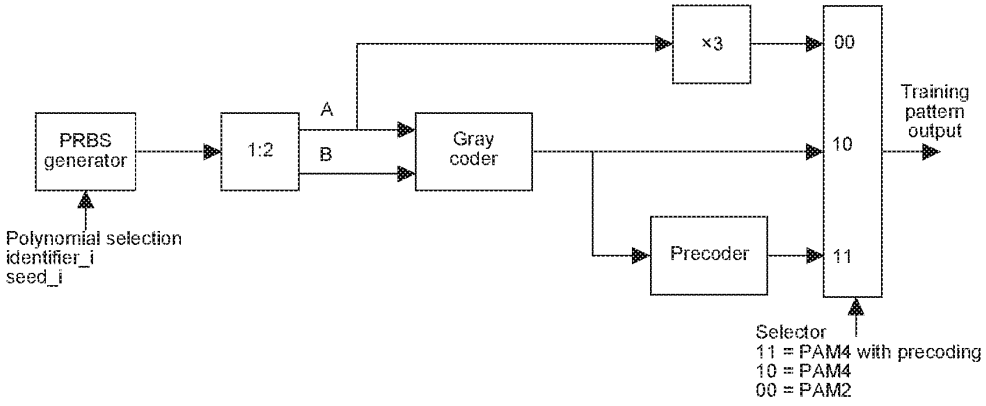


Figure 136–4—Training pattern generator

A set of four PRBS generator polynomials are defined to minimize correlated interference between PMDs, or physical lanes within a PMD, during the start-up protocol. The PRBS generator for each lane shall implement each of four generator polynomials defined in Table 136–8. The polynomial used in each lane *i* is selectable by identifier_*i*. The default identifier for each lane is its lane number (e.g., the default value for identifier_0 is 0 which selects polynomial_0). A sample implementation of the PRBS generator for identifier_*i* = 0 is shown in Figure 136–5.

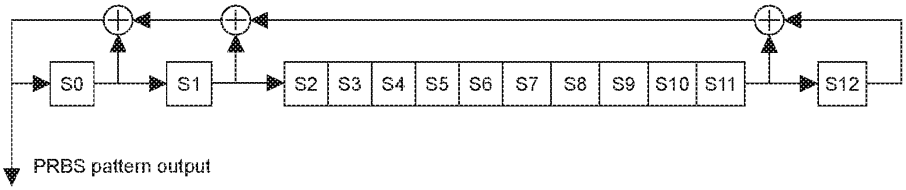


Figure 136–5—Training pattern PRBS generator (identifier_*i* = 0)

At the start of the training pattern, the state of the PRBS generator shall be set to the value seed_*i*. The default value of seed_*i* shall be the value given in Table 136–8 for $n = i$. A seed of all zeros is not valid.

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The polynomials for each identifier value *n* and the default seeds, as well as the first 13 symbols of the training pattern for each modulation and precoding mode, using the default seed, are provided in Table 136–8.

Table 136–8—Training patterns

n	Polynomial_*n*, *G*(*x*)	Default seed bits[a]	Initial output, PAM2	Initial output, PAM4	Initial output, PAM4 with precoding
0	$1 + x + x^2 + x^{12} + x^{13}$	0000010101011	0030330330000	1031320220111[b]	1301200200101
1	$1 + x^2 + x^3 + x^7 + x^{13}$	0011101000001	3030303030333	3030213021333	3122012201212
2	$1 + x^2 + x^4 + x^8 + x^{13}$	1001000101100	0303333033030	1212332133031	1102120121301
3	$1 + x^2 + x^5 + x^9 + x^{13}$	0100010000010	3330300030330	2231210121221	2032013201110

[a]The leftmost bit in the sequence corresponds to the initial value of S0 and the rightmost bit corresponds to the initial value of S12.
[b]This is equivalent to the PRBS13Q test pattern defined in 120.5.11.2.3.

For a given configuration of the PRBS generator, there are three possible training patterns. The construction of each training pattern begins by demultiplexing the PRBS generator output into pairs of bits {A, B} where A corresponds to the 1st, 3rd, 5th, etc. bits output by the PRBS generator and B corresponds to the 2nd, 4th, 6th, etc. bits output by the PRBS generator. There is a new pair of bits each unit interval which implies that the PRBS generator is required to generate bits at twice the signaling rate. Given these pairs of bits, the three different training patterns correspond to three modulation and precoding modes: PAM2, PAM4, PAM4 with precoding.

When the modulation and precoding mode is set to PAM2, the training pattern is the sequence of 16 382 PAM4 symbols derived by mapping only the A bits such that logical 0 is transmitted as 0 and logical 1 is transmitted as 3.

When the modulation and precoding mode is set to PAM4, the training pattern is the sequence of 16 382 PAM4 symbols derived by Gray coding the {A, B} pairs as specified in 135.5.7.1.

When the modulation and precoding mode is set to PAM4 with precoding, the training pattern is the sequence of 16 382 PAM4 symbols derived by Gray coding the {A, B} pairs as specified in 135.5.7.1 and precoding the result as specified in 135.5.7.2. The precoder state is initialized to 0 at the beginning of each training pattern, so that P(j=0) in Equation (135–1) is set to 0.

The modulation and precoding mode is set to PAM2 upon entry to the INITIALIZE state of the PMD control state diagram (see Figure 136–7).

NOTE—Exiting TRAINING mode requires both sides to use PAM4 modulation, thus the request and the status of the modulation and precoding are both required to have values other than PAM2 (either "PAM4" or "PAM4 with precoding").

136.8.11.1.4 Zero pad

Two "0" symbols are transmitted immediately after the training pattern. This zero pad ensures the training frame is DC balanced and helps to delineate the start of the frame marker for the next training frame.

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136.8.11.2 Control field structure

The structure of the control field shall be as shown in Table 136–9.

Table 136–9—Control field structure

Bit(s)	Name	Description
15:14	Reserved	Transmit as 0, ignore on receipt
13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control
11:10	Reserved	Transmit as 0, ignore on receipt
9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2
7:5	Reserved	Transmit as 0, ignore on receipt
4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$
1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold

136.8.11.2.1 Initial condition request

The initial condition request bits are used to select one of the three pre-defined transmitter equalizer configurations (presets) specified in 136.8.11.3.4. When the initial condition request bits are 00, the coefficient select and coefficient request bits are used to update the transmitter equalizer configuration.

136.8.11.2.2 Modulation and precoding request

The modulation and precoding request bits are used to request that the link partner transmitter transmit one of the three training pattern formats defined in 136.8.11.1.3.

136.8.11.2.3 Coefficient select

The coefficient select bits are used to identify the coefficient that is the target of a coefficient request. The value of the field is the two's complement encoding of the coefficient index. For example, binary value 111 corresponds to a coefficient index of –1.

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136.8.11.2.4 Coefficient request

The coefficient request bits are used to change the value of the coefficient specified by the coefficient select bits. A coefficient may be changed by incrementing or decrementing its value or by setting it to "No equalization". The "No equalization" value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.

136.8.11.3 Status field structure

The structure of the status field is shown in Table 136–10.

Table 136–10—Status field structure

Bit(s)	Name	Description
15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue
14:12	Reserved	Transmit as 0, ignore on receipt
11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2
9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified
8	Initial condition status	1 = Updated 0 = Not updated
7	Parity	Even parity bit
6	Reserved	Transmit as 0, ignore on receipt
5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$
2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated

136.8.11.3.1 Receiver ready

The receiver ready bit is used to signal the local receiver state to the link partner. When this bit is 1, it indicates that the local receiver has completed training and is prepared to receive data. When this bit is 0, it indicates that the local receiver is requesting that training continue.

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136.8.11.3.2 Modulation and precoding status

The modulation and precoding status bits acknowledge the modulation and precoding request bits received from the link partner. When a change in the received modulation and precoding request bits are detected, the format of the training pattern is changed accordingly (see 136.8.11.1.3). The modulation and precoding status bits are then updated to confirm that the change to the format of the training pattern was completed.

136.8.11.3.3 Receiver frame lock

When the receiver frame lock bit is set to 1, the receiver is indicating that it has identified training frame marker positions and is in a state where the response time requirements specified in 136.8.11.6 are met.

Receiver frame lock shall be set to 0 upon entering TRAINING mode and shall not be set to 1 until local_tf_lock is true.

136.8.11.3.4 Initial condition status

The initial condition status bit acknowledges the initial condition request bits received from the link partner. The acknowledgment reflects the value of ic_sts resulting from the procedure described in 136.8.11.4.

136.8.11.3.5 Parity bit

The parity bit is calculated based on the other bits in the control field and status field to create even parity for these fields. Even parity ensures that the resulting pattern is DC balanced. This field may be ignored on receipt.

136.8.11.3.6 Coefficient select echo

The coefficient select echo bits acknowledge the coefficient select bits received from the link partner. When a change to the coefficient select bits is detected, the coefficient select echo bits are updated to represent the same coefficient index. This serves as a confirmation to the link partner that subsequent coefficient requests will act on the targeted coefficient.

136.8.11.3.7 Coefficient status

The coefficient status bits acknowledge the coefficient request bits received from the link partner. The acknowledge reflects the value of coef_sts resulting from the procedure described in 136.8.11.5.

136.8.11.4 Initial condition setting

When a change to the initial condition request bits is detected, the coefficients are configured in a manner consistent with the following algorithm.

```
if ic_req = ind_ctl
   ic_sts = not_upd
else
   if ic_req = preset 1
      Set coefficients to preset 1
   else if ic_req = preset 2
      Set coefficients to preset 2
   else if ic_req = preset 3
      Set coefficients to preset 3
   end if
   ic_sts = updated
end if
```

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The variables ic_req and ic_sts are defined in 136.8.11.7.1. The transmitter equalizer coefficients corresponding to each of the three presets shall be within the ranges specified in Table 136–12.

The transmitter equalizer is set to preset 1 upon entry to the INITIALIZE state of the PMD control state diagram.

136.8.11.5 Coefficient update

When a change to the coefficient select or coefficient request bits is detected, the corresponding coefficient update is performed in a manner consistent with the following algorithm.

```
if k in k_list

   if coef_req = INCREMENT
      ck_ask = c(k) + ck_stp
   else if coef_req = DECREMENT
      ck_ask = c(k) - ck_stp
   else if coef_req = NO EQUALIZATION
      if k = 0
         ck_ask = 1
      else
         ck_ask = 0
      end if
   else
      ck_ask = c(k)
   end if

   if ck_ask > ck_max
      c(k) = ck_max
      if CHECK_EQ(ck_ask,k)
         coef_sts = COEFFICIENT AT LIMIT AND EQUALIZATION LIMIT
      else
         coef_sts = COEFFICIENT AT LIMIT
      end if
   else if ck_ask < ck_min
      c(k) = ck_min
      if CHECK_EQ(ck_ask,k)
         coef_sts = COEFFICIENT AT LIMIT AND EQUALIZATION LIMIT
      else
         coef_sts = COEFFICENT AT LIMIT
      end if
   else if CHECK_EQ(ck_ask,k)
      coef_sts = EQUALIZATION LIMIT
   else
      c(k) = ck_ask
      coef_sts = UPDATED
   end if
else
   coef_sts = COEFFICIENT NOT SUPPORTED
end if
```

The variables coef_req, coef_sts, and k are defined in 136.8.11.7.1. The following additional variables and functions are used.

c(k)

Variable that contains the current value of the coefficient *c*(k).

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ck_ask

Variable that contains the value of $c(k)$ that would result from the requested update.

ck_min

Variable that contains the minimum supported value of $c(k)$.

ck_max

Variable that contains the maximum supported value of $c(k)$.

ck_stp

Variable that contains the magnitude of the change in $c(k)$ for one step up or one step down from its current value.

k_list

The set of valid transmitter equalizer coefficient indices {–2, –1, 0, 1}.

CHECK_EQ(ck_ask,k)

Compares the transmitter's steady-state voltage that would result from setting transmit equalization coefficient $c(k)$ value to ck_ask, while keeping all other coefficients unchanged, against the transmitter's steady-state voltage (see 136.9.3.1.2) and equalization capability. Returns true if the resulting combination of coefficients would exceed the maximum steady-state voltage or the transmitter's equalization capability. Otherwise returns false.

136.8.11.6 Handshake timing

Changes to the configuration of the transmitter equalizer or the transmitted training pattern may occur at any point between the time the request for the new configuration is received and the time that the request is acknowledged.

The time from the receipt of a new request to the time that request is acknowledged shall be less than 2 ms when the receiver frame lock bit in the status field of transmitted training frames is set to 1. A new request is defined to be a received training frame whose control field differs from the control field of the preceding training frame. An acknowledgment is defined as the first transmitted training frame that contains a status field encoding that is an appropriate response for the requested action. For example, a change in the coefficient select bits in the control field would be acknowledged by a change in the coefficient select echo bits of the status field. Similarly, a change in the modulation and precoding request bits in the control field would be acknowledged by a change in the modulation and precoding status bits in the status field. All timing measurements are referred to a common reference point within the training frame (e.g., the 3 to 0 transition in the training frame marker).

The timing of requests and acknowledgment is illustrated in Figure 136–6.

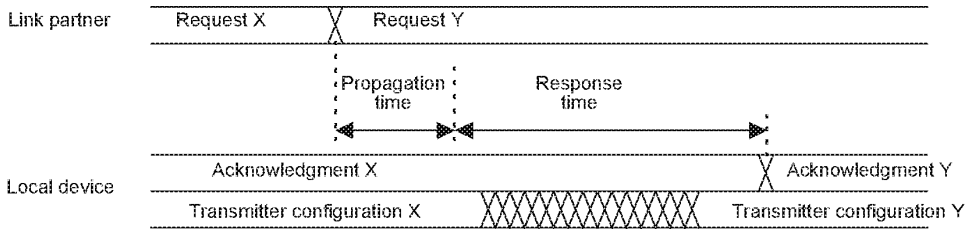


Figure 136–6—Transmitter update timing

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136.8.11.7 Variables, functions, timers, counters, and state diagrams

The PMD implements one instance of each of the PMD control state diagrams, and the set of associated variables, functions, counters and timers defined in this subclause, independently for each of the n physical lanes.

136.8.11.7.1 Variables

coef_req
: Enumerated variable derived from the "coefficient request" bits from the control field of the received training frames (see 136.8.11.2). This variable may be one of the following values: hold, decrement, increment, no equalization.

coef_sel
: Variable derived from the "coefficient select" bits from the control field of the received training frames (see 136.8.11.2). It is assigned a signed integer value that is the two's complement interpretation of the bits.

coef_sts
: Enumerated variable that may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): not updated (not_upd), updated, coefficient at limit, coefficient not supported. This value is assigned by the UPDATE_Cn function and encoded in the status field of transmitted training frames via the ENCODE_STS function.

ic_req
: Enumerated variable derived from the "initial condition request" bits from the control field of the received training frames (see 136.8.11.2). This variable may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): individual control (ind_ctl), preset 1, preset 2, preset 3.

ic_sts
: Enumerated variable that may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): not updated (not_upd), updated.

k
: Variable that stores the most recent value of coef_sel.

local_rx_ready
: Boolean variable that is set to true by the training state diagram when local_trained is asserted and is set to false otherwise. This value is encoded as the "receiver ready" bit in the status field of transmitted training frames.

local_tf_lock
: Boolean variable that is true if the value of training is true and training frame marker positions have been identified and is false otherwise.

local_trained
: Boolean variable that is set to true when the local receiver has determined that the remote transmit and local receive equalizers have been optimized and normal data transmission may commence. It is set to false otherwise. The exact criteria for setting this variable to true are implementation specific.

marker_valid
: Boolean variable that is set to true when the candidate frame marker matches the frame marker pattern defined in 136.8.11.1.1 and is set to false otherwise.

mr_restart_training
: Boolean variable used by system management to restart the start-up protocol. When set to true, it forces the PMD control state diagram to the INITIALIZE state.

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mr_training_enable
: Boolean variable used by system management to enable or disable the start-up protocol. When set to true it enables the start-up protocol, and when set to false it disables the start-up protocol.

new_marker
: Boolean variable that is set to true when a new candidate frame marker is available for testing and is set to false when the TEST_MARKER state is entered. A new frame marker is available for testing when the training frame lock process has accumulated 32 consecutive symbols starting at the candidate frame start position.

remote_rx_ready
: Boolean variable derived from the "receiver ready" bit of the status field of received training frames. If the bit is 1, the value of remote_rx_ready is true, otherwise it is false.

remote_tf_lock
: Boolean variable derived from the "receiver frame lock" bit of the status field of received training frames. If the bit is 1, the value of remote_tf_lock is true, otherwise it is false.

reset
: Boolean variable that resets the PMD. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PMD into low-power mode. It is false otherwise.

signal_detect
: Boolean variable that is set to true when the training process is complete and is set to false otherwise. The value of signal_detect is used by the PMD lane-by-lane signal detect function (136.8.5).

slip_done
: Boolean variable that is set to TRUE when the SLIP requested by the Training frame lock state diagram (Figure 136–8) is completed indicating that the next candidate frame sync position can be tested.

tf_offset
: Boolean variable that is set to true when receiving one full training frame (16 672 symbols, see 136.8.11.1) following the recent frame start position, such that a new frame marker is expected. Otherwise it is set to false

tp_mode
: Enumerated variable that corresponds to the "modulation and precoding status" bits in the status field of received training frames. It may be assigned one of the following values: pam2, pam4, pam4 with precoding.

training
: Boolean variable that is set to true when the start-up protocol is in progress and is set to false otherwise.

training_failure
: Boolean variable that is set to true when training failed to complete successfully within the allotted time limit. Otherwise it is set to false.

136.8.11.7.2 Functions

ENCODE_STS
: Encodes portions of the status field of transmitted training frames. local_tf_lock is mapped to the receiver frame lock bit, k is mapped to the coefficient select echo bits, coef_sts is mapped to the coefficient status bits, ic_sts is mapped to the initial condition status bit, local_rx_ready is mapped to the receiver ready bit, and tp_mode is mapped to modulation and precoding bits (see 136.8.11.3.2).

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SLIP

Causes the next candidate frame marker position to be tested. Repeated invocations of SLIP cause all possible positions to be evaluated. The precise method for determining the next candidate frame marker position is implementation dependent and beyond the scope of this standard.

TRANSMIT(tx_mode)

Controls the output of the PMD transmit function on the current lane. When tx_mode = DATA, the PMD transmit function output is the parameter of the PMD:IS_UNITDATA_*i*.request primitive (see 136.3). When tx_mode = TRAINING, the PMD transmit function output is the stream of symbols generated by the PMD control function.

UPDATE_Cn

Updates the value of $c(k)$ based on the current values of the variables k and coef_req. The result of the update is stored in the variable coef_sts. This function implements the algorithm specified in 136.8.11.5.

UPDATE_IC

Updates all transmit equalizer coefficients based on the current value of the variable ic_req. The result is stored in the variable ic_sts. This function implements the algorithm specified in 136.8.11.3.4.

136.8.11.7.3 Timers

holdoff_timer

This timer is started when the PMD control state diagram enters the TIMEOUT state. The terminal count of holdoff_timer is 80 ms ± 2%.

max_wait_timer

This timer sets the limit for how long the PMD start-up protocol is allowed to operate. It is started upon entry to the INITIALIZE state of the PMD control state diagram. If the timer expires before the LINK_READY state is reached, then a failure to train is indicated. The terminal count of max_wait_timer is 1.5 s ± 2%.

wait_timer

This timer is started when the local receiver has completed training and detects that the remote receiver is ready to receive data. The local transmitter sends additional training frames until the timer expires to ensure that the link partner correctly detects the local receiver state. The terminal count of wait_timer is between 25 µs and 125 µs, equivalent to approximately 40 to 200 training frames.

136.8.11.7.4 Counters

bad_markers

Count of the number of consecutive frame marker mismatches.

good_markers

Count of the number of consecutive frame marker matches.

136.8.11.7.5 State diagrams

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter indicates that its value is to be incremented.

The PMD control state diagram (Figure 136–7) defines the operation of the start-up protocol.

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If the LINK_READY state is entered while the modulation and precoding status bits indicate "PAM4 with precoding", then the PMD shall cause the adjacent PMA to transmit all subsequent data on the corresponding lane with precoding (see 135.5.7.2 and 120.5.7.2).

If the LINK_READY state is entered while the modulation and precoding request bits are set to "PAM4 with precoding", then the PMD shall inform the adjacent PMA that all subsequently received data on the corresponding lane includes precoding (see 135.5.7.2 and 120.5.7.2).

The PMD control state diagram is supported by the training frame lock and coefficient update state diagrams. The training frame lock state diagram (Figure 136–8) determines when the PMD control function has detected training frame boundaries. The coefficient update state diagram (Figure 136–9) defines the process for updating the local transmitter equalizer coefficients in response to requests from the link partner.

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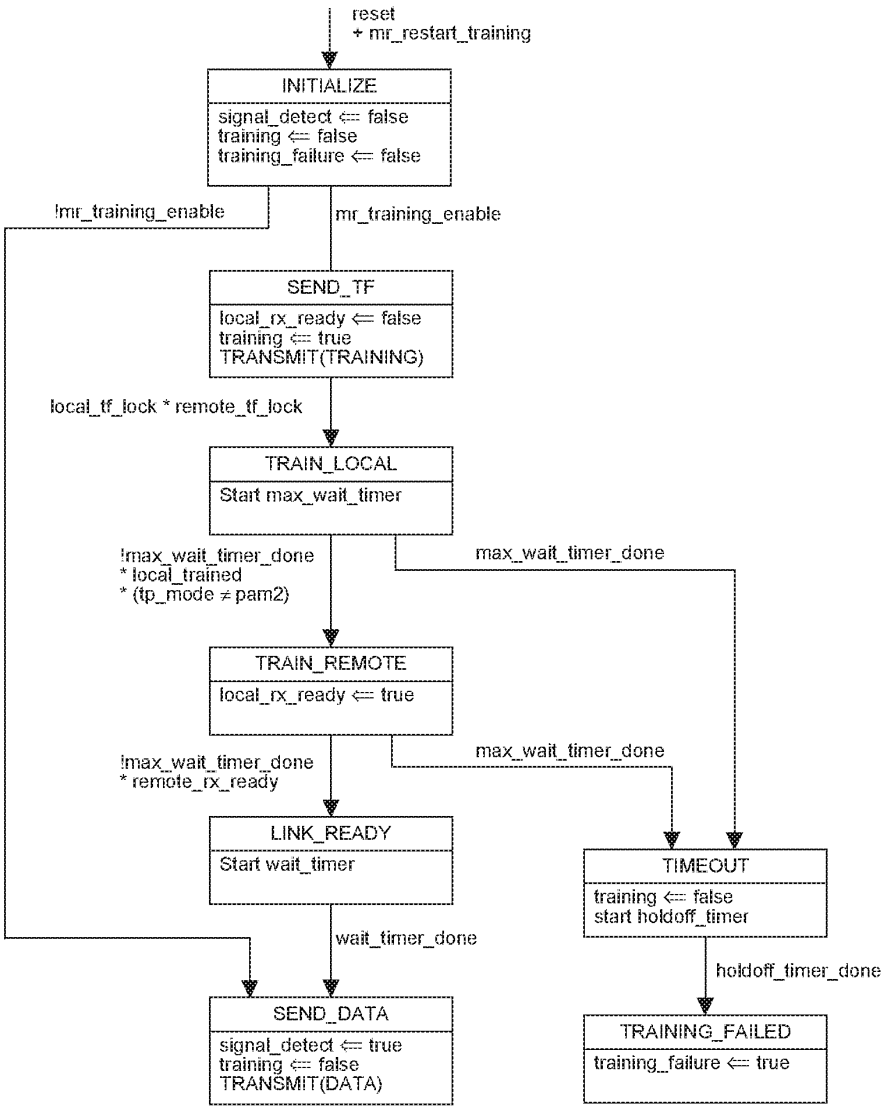


Figure 136–7—PMD control state diagram

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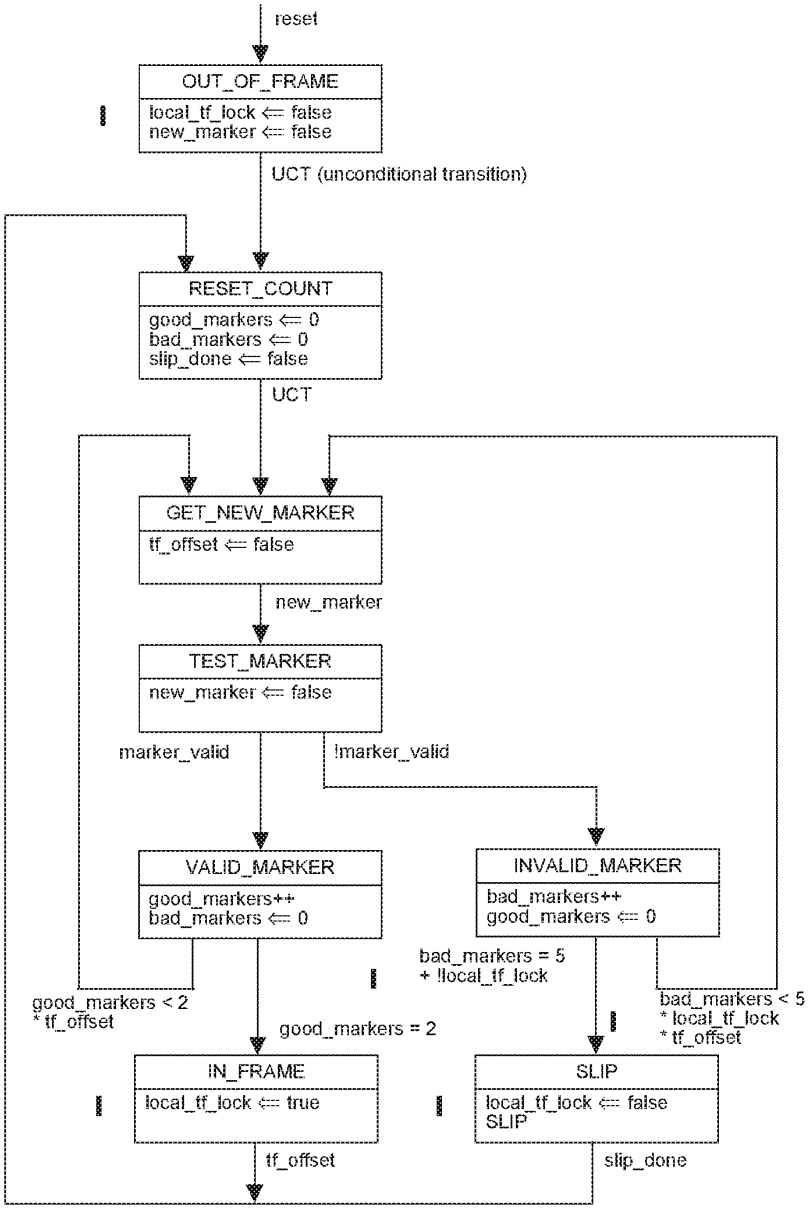


Figure 136–8—Training frame lock state diagram

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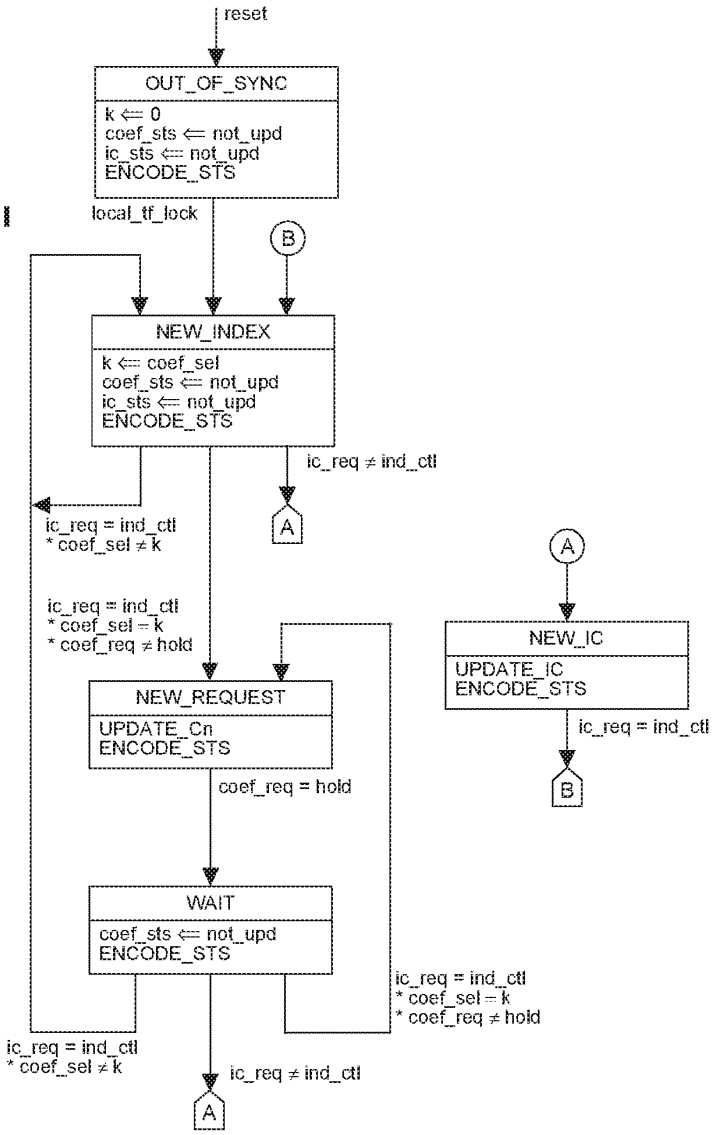


Figure 136–9—Coefficient update state diagram

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000323

136.9 Electrical characteristics

136.9.1 AC-coupling

The MDI (see 136.12) is a low-swing AC-coupled differential interface. AC-coupling within the plug connectors, as defined in 136.12, allows for interoperability between components operating from different supply voltages.

136.9.2 Signal paths

The MDI transmit and receive paths are point-to-point connections. Each path corresponds to one MDI lane and comprises two complementary signals, which form a balanced differential pair.

For 50GBASE-CR, there is one differential path in each direction for a total of two pairs, or four connections. For 100GBASE-CR2, there are two differential paths in each direction for a total of four pairs, or eight connections. For 200GBASE-CR4, there are four differential paths in each direction for a total of eight pairs, or sixteen connections.

136.9.3 Transmitter characteristics

The transmitter on each lane shall meet the specifications given in Table 136–11 and detailed in the referenced subclauses. Unless specified otherwise, all transmitter measurements are made for each lane separately, at TP2, utilizing the test fixtures specified in 136B.1.1, using a test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth.

The transmitter characteristics at TP0 are provided informatively in 136A.2.

Table 136–11—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Differential pk-pk output voltage (max.) with Tx disabled[a]	94.3.12.3	30	mV
DC common-mode voltage (max.)[a]	94.3.12.3	1.9	V
AC common-mode RMS output voltage, v_{cmi} (max.)[a]	94.3.12.3	30	mV
Differential pk-pk voltage, v_{di} (max.)[a]	94.3.12.3	1.200	mV
Differential output return loss (min.)	92.8.3.2	See Equation (92–1)	dB
Common-mode to differential mode output return loss (min.)	92.8.3.3	See Equation (92–2)	dB
Common-mode to common-mode output return loss (min.)	92.8.3.4	See Equation (92–3)	dB
Transmitter steady-state voltage, v_f (min.) Transmitter steady-state voltage, v_f (max.)	136.9.3.1.2	0.34 0.6	V
Linear fit pulse peak (min.)	136.9.3.1.2	$0.49 \times v_f$	V
Level separation mismatch ratio R_{LM} (min.)	120D.3.1.2.1	TBD	----

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000324

Table 136–11—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Transmitter output waveform			
abs step size for $c(-1)$, $c(0)$, and $c(1)$ (min.)	136.9.3.1.4	0.005	—
abs step size for $c(-1)$, $c(0)$, and $c(1)$ (max.)	136.9.3.1.4	0.05	—
abs step size for $c(-2)$ (min.)	136.9.3.1.4	0.005	—
abs step size for $c(-2)$ (max.)	136.9.3.1.4	0.025	—
value at minimum state for $c(-1)$ and $c(1)$ (max.)	136.9.3.1.5	−0.25	—
value at maximum state for $c(-2)$ (min.)	136.9.3.1.5	0.1	—
Signal-to-noise-and-distortion ratio (min.)	TBD	TBD	dB
SNR_{ISI} (min.)	120D.3.1.7	30	dB
Output jitter (max.)	120D.3.1.1		
Even-odd jitter, pk-pk		0.019	UI
J_{RMS}		TBD	UI
J4		TBD	UI
Signaling rate		26.5625 ± 100 ppm	GBd
Unit interval nominal		37.64706	ps

[a]Measurement uses the method described in 94.3.12.3 with the exception that the PRBS13Q test pattern is used.

136.9.3.1 Transmitter output waveform

The transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer on each lane is the four-tap transversal filter shown in Figure 136–10.

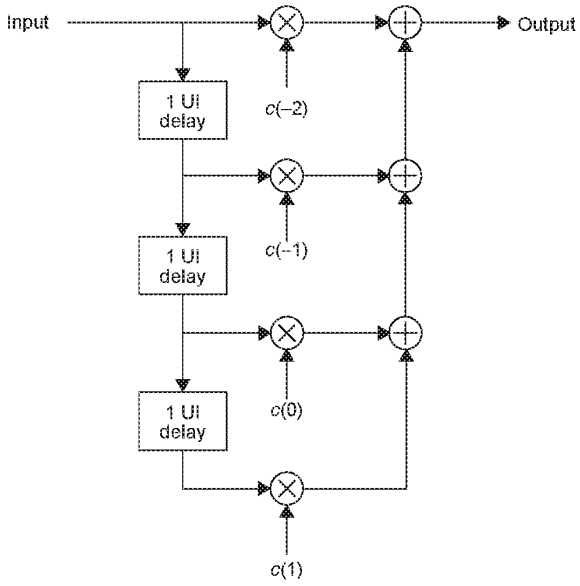


Figure 136–10—Transmit equalizer functional model

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000325