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(54) **DATA TRANSMISSION SYSTEM**

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(57) **ABSTRACT**

A data transmission method includes, detecting an incoming link training sequence that is transmitted from an upstream transmitter, generating a marker indicating a timing location of a word included in the incoming link training sequence, generating a self link training sequence based on a local reference clock, adjusting a time difference in the incoming link training sequence and the self link training sequence, and retransmitting an incoming bit stream based on the self link training sequence being matched to the incoming link training sequence.

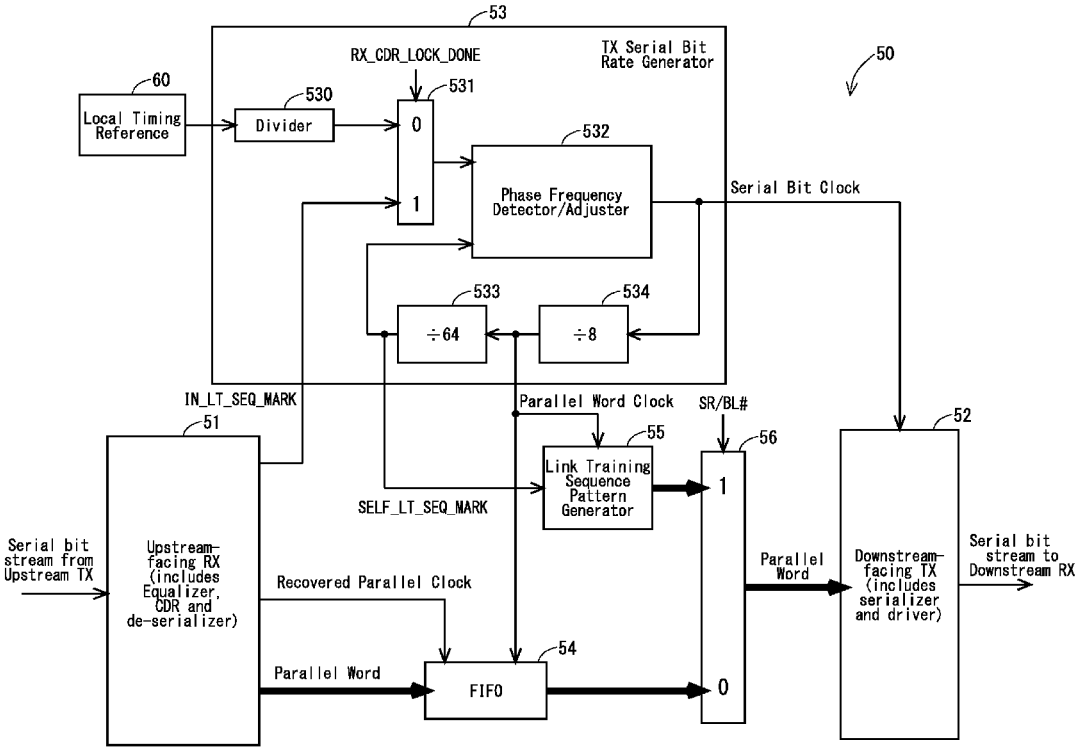


FIG. 1

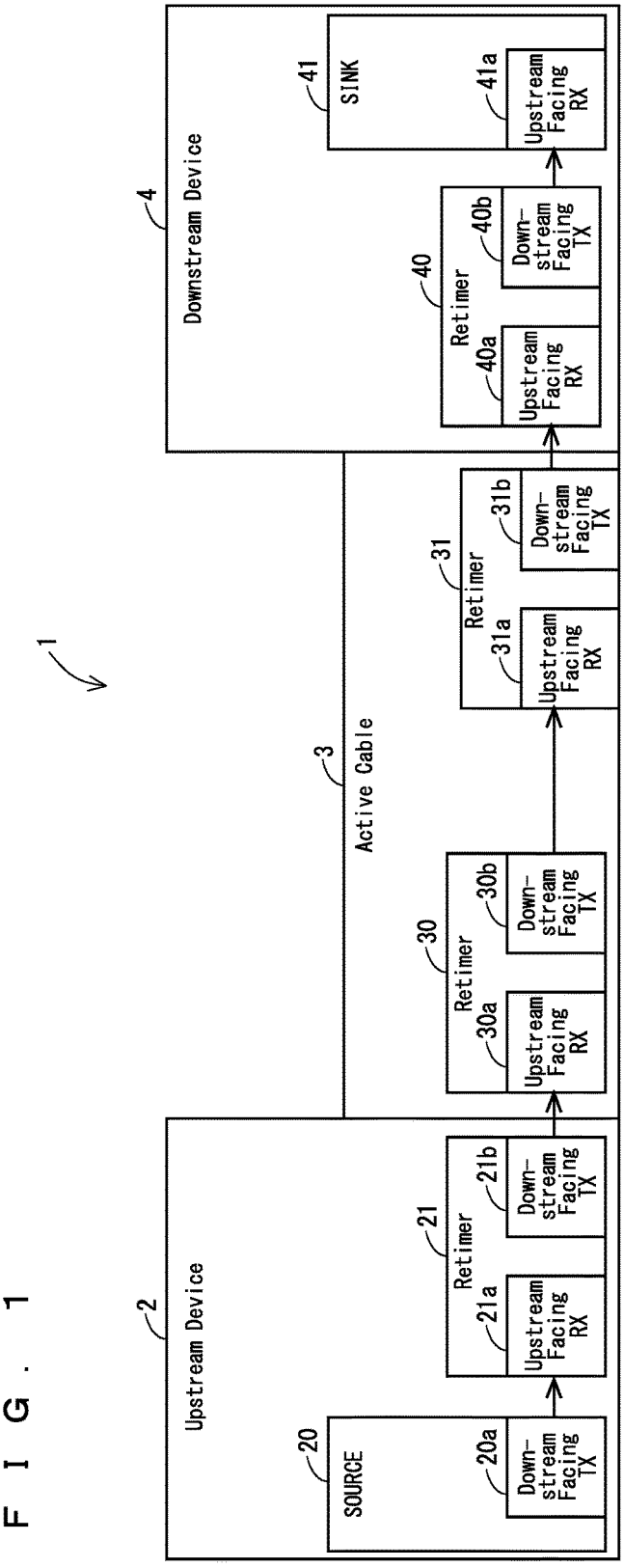
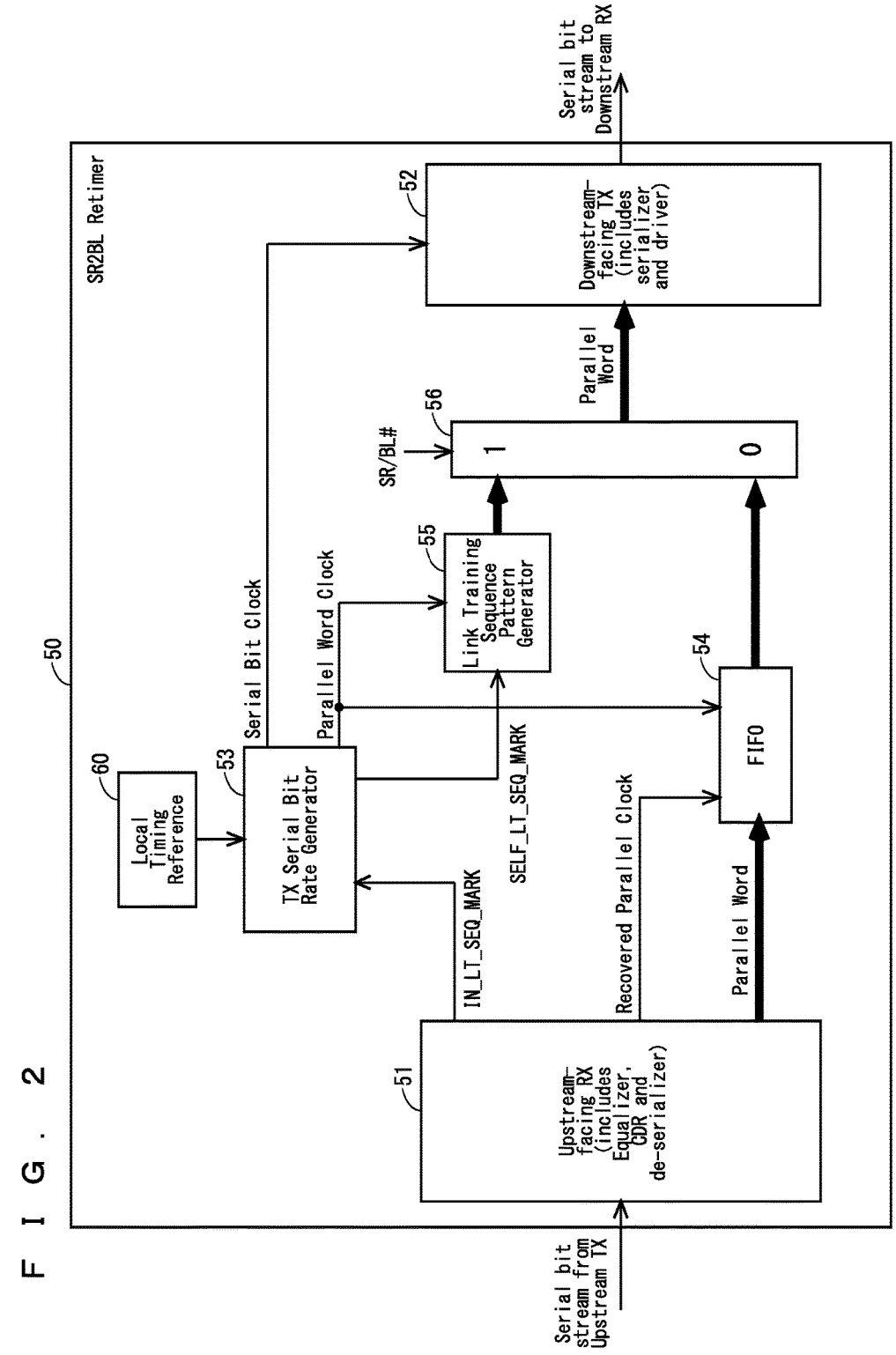

1
2
Upstream Device
20
SOURCE
20a
Down-stream Facing TX
21
Retimer
21a
Upstream Facing RX
21b
Down-stream Facing TX
3
Active Cable
30
Retimer
30a
Upstream Facing RX
30b
Down-stream Facing TX
31
Retimer
31a
Upstream Facing RX
31b
Down-stream Facing TX
4
Downstream Device
40
Retimer
40a
Upstream Facing RX
40b
Down-stream Facing TX
41
SINK
41a
Upstream Facing RX

FIG. 2


SR2BL Retimer
50
Serial bit stream from Upstream TX
Serial bit stream to Downstream RX
51
Upstream-facing RX (includes Equalizer, CDR and de-serializer)
52
Downstream-facing TX (includes serializer and driver)
53
TX Serial Bit Rate Generator
54
FIFO
55
Link Training Sequence Pattern Generator
56
SR/BL#
1
0
60
Local Timing Reference
Serial Bit Clock
Parallel Word Clock
Recovered Parallel Clock
IN_LT_SEQ_MARK
SELF_LT_SEQ_MARK
Parallel Word
Parallel Word

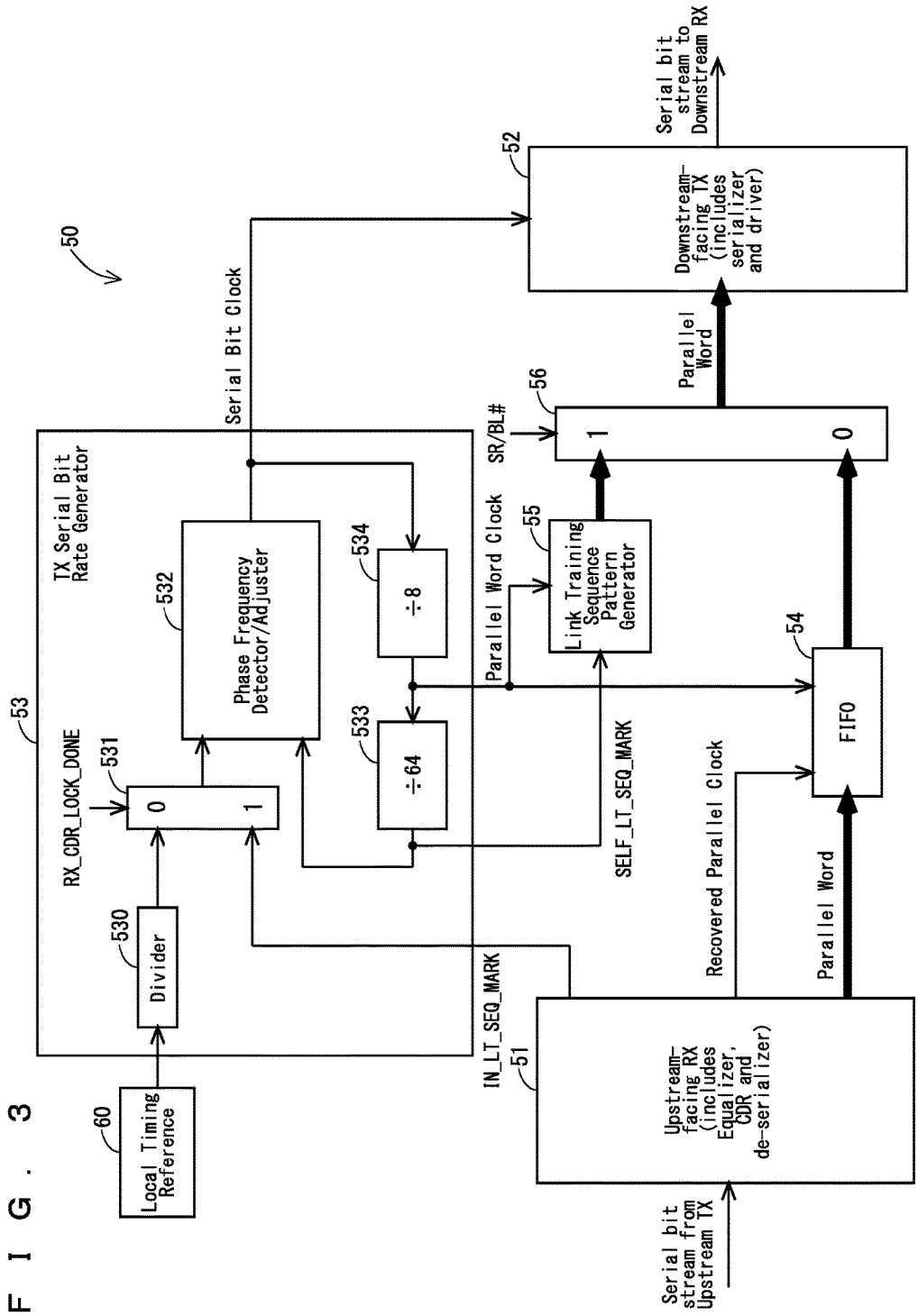

50
Serial Bit Clock
TX Serial Bit Rate Generator
53
RX_CDR_LOCK_DONE
531
0
1
Phase Frequency Detector/Adjuster
532
÷8
534
÷64
533
Divider
530
Local Timing Reference
60
Parallel Word Clock
SR/BL#
56
1
0
Link Training Sequence Pattern Generator
55
SELF_LT_SEQ_MARK
IN_LT_SEQ_MARK
Recovered Parallel Clock
54
FIFO
Parallel Word
Parallel Word
Downstream-facing TX (includes serializer and driver)
52
Serial bit stream to Downstream RX
Upstream-facing RX (includes Equalizer, CDR and de-serializer)
51
Serial bit stream from Upstream TX

FIG. 3

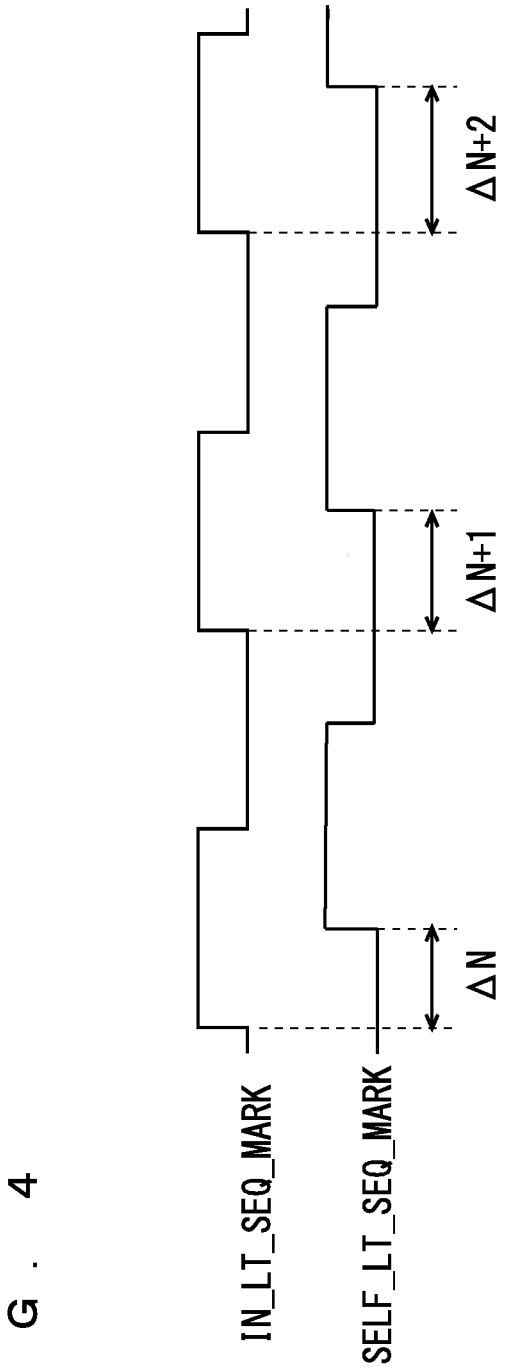


FIG. 4

DATA TRANSMISSION SYSTEM

TECHNICAL FIELD

[0001] The present invention relates generally to a data transmission method and a data transmission system which have Display Port (DP) and/or Universal Serial Bus (USB).

BACKGROUND ART

[0002] As high-speed data transmission interfaces, Display Port and USB are known. In these interfaces, a link training sequence is performed so that a synchronization between a source and a sink (Display Port) or between a host and a device (USB) is established. This sequence is usually performed after powered on and before starting a normal operation. In order to avoid high-speed serial bit stream signal quality degradation, a component type called "retimer" is defined in high-speed transport specifications such as USB3.1 and DPI.4. A retimer is used to extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the retimer. The retimer contains a clock-data recovery (CDR) circuit that retimes the signal and latches the signal into a synchronous memory element before retransmitting it.

PRIOR ART DOCUMENTS

Non-Patent Documents

[0003] Non-patent Document 1: Universal Serial Bus 3.1 specification, revision 1.0, Jul. 26, 2013

SUMMARY OF INVENTION

Problems to be Solved by the Invention

[0004] The delay in data transmission is preferably as small as possible.

Means for Solving the Problem

[0005] It is an object of fee present invention to provide a data transmission method and system for eliminating a transmission initiation delay and minimizing a retransmission delay by using a separate-reference-to-bit-level retimer (or "SR2BL retimer", for short). Note that "Sink training sequence" of the present invention includes both of a link training sequence of DP and a training sequence (TSEQ) of USB.

[0006] According to one aspect of the invention, a data transmission method includes, detecting an incoming link training sequence that is transmitted from an upstream transmitter, generating a marker indicating a timing location of a word included in the incoming link training sequence, generating a self link training sequence based on a local reference clock, adjusting a time difference in the incoming link training sequence and the self link training sequence, and retransmitting an incoming bit stream based on the self link training sequence being matched to the incoming link training sequence.

[0007] Also, according to another aspect of the invention, a data transmission system includes, a retimer having a local timing reference unit and a clock data recovery unit, in which a link training sequence of a data transmission is initially performed based on a local reference clock, generated from the local timing reference unit, and a normal operation sequence of the data transmission is transitioned from a local clock generated to a clock generated by the clock data recovery unit.

Effect of the Invention

[0008] The data transmission method and system of the present invention has following advantages:
1) Eliminates the transmission initiation delay inherent in a bit-level retimer by starting the transmission of a link training sequence using own local timing reference (=a separate reference operation)
2) Minimizes the retransmission delay inherent in a separate-reference retimer by seamlessly transitioning from separate-reference retimer operation to bit-level retimer operation before the end of the link training sequence.

BRIEF DESCRIPTION OF DRAWINGS

[0009] FIG. **1** is a block diagram of a data transmission topology with four retimers.

[0010] FIG. **2** is a block diagram of a separate-reference-to-bit-level retimer.

[0011] FIG. **3** is a block diagram of a PLL unit of a transmitter of the separate-reference-to-bit-level retimer.

[0012] FIG. **4** is a timing diagram depicting timing signals of IN_LT_SEQ_MARK and SELF_LT_SEQ_MARK.

DESCRIPTION OF EMBODIMENTS

[0013] FIG. **1** illustrates an example of the data transmission system **1** having retimers. An upstream device (known as "Host" in USB or "Source" in DP) may have a retimer, an active cable may have two retimers on both ends of the cable, and a downstream device (known as "Device" in USB and "Sink" in DP) may have a retimer, resulting in four retimers cascaded between a downstream-feeing transmitter (TX) within an upstream device and an upstream facing receiver (RX) within a downstream device.

[0014] As shown in FIG. **1**, the data transmission system **1** is in accordance with DP1.4, for example, and includes an upstream device **2**, a downstream device **4**, and an active cable **3** connecting the upstream device **2** and downstream device **4**.

[0015] The upstream device **2** includes a source **20** having a downstream facing TX **20***a* and a retimer **21** having an upstream feeing RX **21***a* and a downstream facing TX **21***b*. The active cable **3** includes a retimer **30** having an upstream facing RX **30***a* and a downstream facing TX **30***b* and a retimer **31** having an upstream facing RX **31***a* and a downstream feeing TX **31***b*. The retimer **30** is located in one end of a side of the upstream device **2** in the active cable **3**. The retimer **31** is located in one end of a side of the downstream device **4** in the active cable **3**. The downstream device **4** includes a retimer **40** having an upstream facing RX **40***a* and a downstream facing TX **40***b*. In the data transmission system **1**, the retimes **21**, **30**, **31**, and **40** are cascade-connected.

[0016] In the data transmission system **1** having the above configuration, the source **20** in the upstream device **2** generates a serial bit stream which is a video signal, for example. The source **20** transmits the generated serial bit stream from the downstream facing TX **20***a* to the retimer **21**. The retimer **21** receives the serial bit stream transmitted from the downstream facing TX **20***a* in the upstream facing

TX **21***a*. The retimer **21** performs a waveform shaping on the received serial bit stream and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX **21***b* to the active cable **3**.

[0017] The active cable **3** receives the serial bit stream transmitted from the upstream device **2** in the upstream facing RX **30***a* in one retimer **30**. The retimer **30** performs a waveform shaping on the serial bit stream received by the upstream facing RX **30***a* and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX **30***b* to the other retime **31**. The retimer **31** receives the serial bit stream transmitted from the retimer **30** in the upstream facing RX **31***a*. The retimer **31** performs a waveform shaping on the serial bit stream received by the upstream facing RX **31***a* and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream feeing TX **31***b* to the downstream device **4**.

[0018] The downstream device **4** receives the serial bit stream transmitted from the active cable **3** in the upstream facing RX **40***a* in the retimer **40**. The retimer **40** performs a waveform shaping on the serial bit stream received by the upstream facing RX **40***a* and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX **40***b* to a sink **41**. The sink **41** displays a video, for example, based on the received serial bit data.

[0019] A transport latency introduced by a retimer gets multiplied as multiple retimers get cascaded. The resulting accumulation of latency can negatively affect the transport protocol between the upstream device and the downstream device to the extent the link fails to get established.

[0020] There are two retimer approaches. A bit-level retimer retimes an incoming serial bit stream and retransmits it using a serial bit clock recovered by a CDR of the upstream-facing RX. The bit-level retimer has an advantage in that it does not require transport-protocol processing (insertion and/or removal of dummy symbols (known as Skip Ordered Sets in USB3.1 spec) by the retimer. However, the bit-level retimer increases the latency in the serial bit stream retransmission initiation. It is because the bit-level retimer needs to have its CDR realize frequency and phase lock to the incoming serial bit stream, which takes multiple microseconds, before being able to start the retransmission. For some serial transport specifications, this retransmission initiation delay, especially when multiple bit-level retimers are cascaded, results in the transport timing specification violation.

[0021] Also, a separate-reference retimer retransmits the incoming serial bit stream with a serial bit clock generated from its own local timing reference which is independent from the clock generated by the CDR. However, to compensate the inherent rate difference between the incoming serial bit rate and the outgoing serial bit rate, insertion and/or removal of dummy symbols (known as Skip Ordered Sets in USB3.1 spec) in conjunction with an elastic buffer by the separate-reference retimer is required.

[0022] Described hereinafter is a data transmission system winch enables an elimination of a transmission initiation delay inherent in a bit-level retimer and also enables a reduction in a retransmission delay inherent in a separate-reference retimer.

[0023] FIG. **2** is an exemplary block diagram of a separate-reference-to-bit-level retimer (or the SR2BL retimer, for short) **50** of the present invention. The SR2BL retimer can be used as the retimers **21**, **30**, **31**, and **40** shown in the above FIG. **1**. Hereinafter, the SR2BL retimer **50** is also referred to simply as the retimer **50** in some cases. The retimer **50** is made up of a hardware circuit, for example. The retimer is deemed to have a circuitry.

[0024] As shown in FIG. **2**, the retimer **50** includes an upstream facing RX **51**, a downstream facing TX **52**, a TX serial bit rate generator **53**, a FIFO **54**, a link training sequence pattern generator **55**, and a selection circuit **56**. The upstream facing RX **51** includes an equalizer, a CDR, and a de-serializer. The downstream facing TX **52** includes a serializer and a driver.

[0025] The upstream facing RX **51** generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them.

[0026] The TX serial bit rate generator **53** generates a serial bit clock and a parallel word clock based on a local timing reference **60** (a type of reference clock) generated in the retimer **50** and outputs them. The TX serial bit rate generator **53** also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer **50** itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK

[0027] FIG. **3** is a block diagram mainly illustrating one example of a configuration of the TX serial bit rate generator **53**. As shown in FIG. **3**, the TX serial bit rate generator **53** includes a divider **530**, a selection circuit **531**, a phase frequency detector/adjuster **532**, a ⅛ divider **534**, and a 1/64 divider **533**.

[0028] The divider **530** divides the local timing reference **60** and outputs it. The selection circuit **531** selects an output signal of the divider **530** or the IN_LT_SEQ_MARK based on a switching signal RX_CDR_LOCK_DONE and outputs a selected signal.

[0029] The ⅛ divider **534** performs ⅛ division of the serial bit clock being output from the phase frequency detector/adjuster **532** and outputs it. When the selection circuit **531** outputs the output signal of the divider **530**, the output signal from the ⅛ divider **534** is output from the TX serial bit rate generator **53** as the parallel word clock.

[0030] The 1/64 divider **533** performs 1/64 division of the signal being output from the ⅛ divider **534** and outputs it. When the selection circuit **531** outputs the IN_LT_SEQ_MARK, the output signal from the ⅛ divider **534** is output from the TX serial bit rate generator **53** as the SELF_LT_SEQ_MARK.

[0031] The phase frequency detector/adjuster **532** synchronizes the output signal of the 1/64 divider **533** with the output signal of the selection circuit **531**. Specifically, the phase frequency detector/adjuster **532** detects a phase difference and a frequency difference between the output signal of the 1/64 divider **533** and the output signal of the selection circuit **531** and adjusts a phase and frequency of the serial bit clock to be output so that the detected phase difference and the frequency difference are minimized. Thereby, the serial bit clock is synchronized with the local timing reference.

[0032] The FIFO **54** takes in, in synchronization with the recovered parallel clock, the parallel word being output from the upstream facing RX and stores it. The FIFO **54** outputs

the stored parallel word in synchronization with the parallel word clock being output from the TX serial bit rate generator **53**.

[0033] The link training sequence pattern generator **55** generates 8 parallel bits per parallel word clock. When the 8 parallel bits are concatenated over multiple parallel word clock cycles, they constitute an outgoing link training pattern. The link training pattern is repeated, marked with the SELF_LT_SEQ_MARK (which is a 10-bit character) at the beginning of the pattern.

[0034] Link training pattern is defined in a standard (for example, USB3.1). So the incoming link training pattern from the upstream device and the outgoing link training pattern the link training sequence pattern generator **55** generates are the same.

[0035] Once the TX serial bit rate generator **53** achieves the frequency and phase alignment of the outgoing link training sequence pattern to the incoming link training sequence pattern (synchronizes the SELF_LT_SEQ_MARK output from the 1/64 divider **533** with the IN_LT_SEQ_MARK output from selection circuit **531**), the switch signal SR/BR# is cleared to 0, resulting in the retransmission of the incoming link training sequence pattern. As the frequency and phase alignment had already been achieved, the clearing of the switch signal SR/BR# to 0 does not cause the disruption of in the outgoing link training sequence pattern.

[0036] The selection circuit **56** selects data being output from the link training sequence pattern generator **55** or data being output from the FIFO based on the switch signal SR/BL# and outputs selected data.

[0037] The downstream facing TX **52** converts the data being output from the selection circuit **56** into the serial bit stream. The downstream facing TX **52** transmits the serial bit stream to the downstream RX in synchronization with the serial bit clock being output from the TX serial bit rate generator **53**.

[0038] The operation of the retimer **50** having the above configuration makes a transition from the separate-reference retiming operation to the bit-level retiming operation. This transition is described in detail hereinafter.

[0039] To avoid the serial link transmission initiation delay, the SR2BL retimer **50** starts the transmission of the Sink initiation bit stream sequence (also known as link training sequence) using its own local timing reference **50**.

[0040] Before starting the transmission of link training sequence, the SR28L retimer **50** monitors the reception of incoming link training sequence from the upstream TX. The purpose of the monitoring is the detection of the initiation of the link training sequence transmission by the upstream TX. This detection is achieved by detecting the incoming differential pair toggling at a rate much higher than LPFS (low frequency periodic signaling) rate. The detection can be realized in a matter of few tens of serial bit period (also known as UI, or unit interval), which is multiple orders of magnitude shorter than multiple microseconds needed for the realization of frequency and phase lock of the CDR.

[0041] The downstream-facing TX **32** of the SR2BL retimer **50** initiates the transmission of the link training sequence as soon as it has detected the initiation of the sequence by the upstream TX, and awaits the CDR of the upstream-feeing RX **51** to realize the frequency and phase lock to the incoming link training sequence.

[0042] Once the CDR has realized the frequency and phase lock to the incoming link training sequence (RX_CDR_LOCK_DONE=1), the upstream-facing RX **51** starts generating the incoming link training sequence marker (IN_LT_SEQ_MARK) which indicates the timing location of the parallel word representing the first link symbol of the repetitive link training sequence.

[0043] For USB3.1 Super Speed mode at 5 Gbits per second, for example, the link training sequence called TSEQ sequence consists of 64 link symbols (each symbol having 10 serial bits, 0.2 ns each) starting with K28.5− of ANS18b/10b channel code and repeats 32,768 times, thus lasting over 4 ms. Therefore, K28.5− is to be used as IN_LT_SEQ_MARK.

[0044] The SR28L retimer **50**, while in a separate reference operation, generates its own link training sequence marker (SELF_LT_SEQ_MARK, which is K28.5−).

[0045] FIG. **4** indicates a timing diagram depicting timing signals of IN_LT_SEQ_MARK and SELF_LT_SEQ_MARK. TX Serial Bit Rate Generator **53** measures the time delta between IN_LT_SEQ_MARK and SELF_LT_SEQ_MARK and adjust the TX Serial Bit Rate Generator **53** to minimize the differences in measured delta's (i.e., frequency locking) and then to minimize the delta values (phase locking).

[0046] When the frequency and phase locking of SELF_LT_SEQ_MARK to IN_LT_SEQ_MARK is done, the phase frequency detector/adjuster **532** switches from the transmission of the internal link training sequence pattern to retransmission of the incoming serial bit rate by changing the switching signal RX_CDR_LOCK_DONE and the switching signal SR/BL# from 1 to 0. The switching from the transmission of the internal link training sequence pattern to retransmission of the incoming serial bit rate is done at the 10-bit code boundary of Link Training Sequence Marker. So, receiver will not see any discontinuity in the received Link Training symbol sequence. As a result, the switching is achieved in a manner not disturbing the symbol sequence.

[0047] The present invention has been described in connection with the preferred embodiment, it is not intended to limit the scope of the invention to the particular form set forth, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents as may be included within the spirit and scope of the inventions as defined by the appended claims.

1. A data transmission system, comprising:

a transmitter and a receiver;

a retimer provided between the transmitter and the receiver, the retimer having local liming reference circuitry and clock data recovery circuitry, wherein:

a link training sequence of a data transmission is initially performed based on a local reference clock generated from the local timing reference circuitry, and

a normal operation sequence of the data transmission is performed based on a clock generated by the clock data recovery circuitry and by transitioning from the local reference clock.

2. The data transmission system according to claim **1**, wherein the normal operation sequence starts before the end of the link training sequence.

3. The data transmission system according to claim **1**, wherein the retimer comprises an upstream-facing receiver having the clock data recovery circuitry, and

wherein the upstream-facing receiver generates an incoming link training sequence marker.

4. The data transmission system according to claim **1**, wherein the retimer comprises a serial bit rate generator which generates a self link training sequence marker during the link training sequence.

5. The data transmission system according to claim **1**, wherein the data transmission is performed between a host and a device in a Universal Serial Bus.

6. The data transmission system according to claim **1**, wherein the data transmission is performed between a source and a sink in a Display Port.

7. A data transmission system comprising:

a transmitter and a receiver;

a retimer provided between the transmitter and the receiver,

wherein the retimer comprises:

an upstream-facing receiver which receives a serial bit stream from the transmitter and generates an incoming link training sequence marker,

a serial bit rate generator which generates a self link training sequence marker based on a local timing reference, and

a downstream-feeing transmitter which retransmits the serial bit stream to the receiver in synchronization with a serial bit clock recovered from the serial bit stream.

8. The data transmission system according to claim **7**, wherein the downstream-facing transmitter retransmits the serial bit stream after adjusting a time difference in the incoming link training sequence marker and the self link training sequence marker.

9. The data transmission system according to claim **7**, wherein the retimer further comprises a link training sequence pattern generator which receives the self link training sequence marker and a parallel word clock from the serial bit rate generator.

10. The data transmission system according to claim **7**, wherein the transmitter and the receiver are a host and a device respectively in a Universal Serial Bus.

11. The data transmission system according to claim **7**, wherein the transmitter and the receiver are a source and a sink respectively in a Display Port.

* * * * *