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CMOS Continuous-Time Adaptive Equalizers for High-Speed Serial Links

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Preface

This book studies CMOS continuous-time adaptive equalizers for high-speed serial links. Continuous-time equalizers have been widely used in different data transmission applications such as short- and long-distance copper communications, in printed circuit board transmissions and short-haul optical communications through plastic optical fibers (POF). The equalizer compensates the bandwidth limitation of the communication channel to reach the required transmission speed.

CMOS Continuous-Time Adaptive Equalizers for High-Speed Serial Links first explores the theoretical fundamentals of continuous-time adaptive equalizers. After this, different structures are proposed for the different blocks that constitute it and a complete continuous-time adaptive equalizer is designed. The main objectives are low-voltage supply, low-power consumption, and high-speed operation. Experimental measurements certify the correct operation of the proposed equalization approach. Finally, a cost-effective CMOS receiver which includes the proposed continuous-time adaptive equalizer is designed for 1.25 Gb/s optical communications through 50-m length, 1-mm diameter POF.

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Symbols

A	Gain
A_C	Common mode gain
A_D	Differential gain
A_{Opt}	Optimum gain for equalization
C	Capacitance
clk	Clock signal
C_{gs}, C_{gd}	Gate-source and gate-drain capacitance
C_{int}	Integrating capacitor
C_{oi}	Output node capacitance of the transistor i
C_{OX}	Oxide capacitance per unit of area
C_{PD}	Photodiode capacitance
D_{clk}	Clock output data
D_{in}	Input data
$D_{(x)}$	X-bit digital control word
f	Frequency
f_{co}	Cut-off frequency
g_m	MOS transistor transconductance defined as $\delta I_D/\delta V_{GS}$
g_{mb}	MOS transistor bulk-transconductance defined as $\delta I_D/\delta V_{BS}$
GND	Ground
$H(s)$	Transfer function
I_B	Bias current
I_D	MOS drain current
I_{DS}	Drain-source current
$I^2_{N,IN}$	Input referred noise
I_O	Output current
I_{out}	Output current
I_S	Input current
j	Complex
k	Scaling factor between transistors
K	Boltzmann's constant (1.38×10^{-23} J/K)

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L	Transistor length
M_i	Transistor i
p	Pole
P_{acc}	Accumulated power
q	Electron charge (1.602×10^{-19} C)
Q	Quality factor
R_B	Bit Rate
R_F	Shunt-feedback or floating load resistance
R_L	Load resistance
r_0	MOS transistor output resistance
R_O	Output resistance
R_{var}	Variable resistance
S_{in}	Power spectral density at the input
S_{out}	Power spectral density at the output
s_P	Pole frequency
S_{xy}	S-parameters
s_Z	Zero frequency
T	Temperature
T_B	Bit period
T_F	Fall time
T_i	Transconductor i
T_{INT}	Constant time of the integrator
T_R	Rise time
t_{trans}	Transition time
UI	Unit interval
V_b	Bias voltage
V_C	Control voltage
V_{CG}	Gain control voltage
V_{CM}	Common-mode voltage
V_{CT}	TIA control voltage
V_{DD}	Supply voltage
V_{Dsat}	Drain saturation voltage of a MOS transistor
V_{fc}	Frequency control voltage
V_{GS}, V_{DS}, V_{BS}	Gate-source, drain-source and bulk-source MOS transistor
V_{in}	Input voltage
V_O	Output voltage
V_{REF}	Reference voltage
V_S	Equalizer input voltage
V_{TH}	Threshold voltage of a MOS transistor
W	Transistor width
z	Zero
ε	Dielectric constant
ε_0	Vacuum dielectric constant ($8.8542\ 10^{-12}$ F/m)
φ	Phase of a clock

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ω	Angular frequency
ω_0	Characteristic frequency
μ_N	Electron mobility
λ	Channel-length modulation factor of a MOS transistor

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Acronyms

ADC	Analog-to-Digital Converter
ADSL	Asymmetric Digital Subscriber Line
AGC	Automatic Gain Control
APF	All-Pass Filter
BPD	Binary Phase Detector
BBPD	Bang-Bang Phase Detector
BER	Bit Error Rate
BFD	Binary Phase Detector
BJT	Bipolar Junction Transistor
BPF	Band-Pass Filter
BW	Bandwidth
CDR	Clock and Data Recovery Circuit
CML	Current-Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common Mode Rejection Ratio
CP	Charge-Pump
CT	Continuous-Time
DAC	Digital to Analog Converter
DCA	Digital Communications Analyzer
DEMUX	Demultiplexer
DFE	Decision Feedback Equalizer
DFF	D-Flip-Flops
DUT	Device Under Test
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge
FFE	Feed-Forward Equalizer
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
FSG	Fluorosilicate glass
GI-POF	Graded-Index Plastic Optical Fiber
GOF	Glass Optical Fiber
HAN	Home Area Networks

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HPF	High-Pass Filter
IC	Integrated Circuit
I-V	Current-to-Voltage
IIR	Infinite Impulse Response
ISDN	Integrated Services Digital Network
ISI	Intersymbol Interference
LA	Limiting Amplifier
LED	Light-Emitting Diode
LMS	Least Mean Squares
LPF	Low-Pass Filter
MIM	Metal-Insulator-Metal
MDAC	Multi Digital to Analog Converter
MOST	Media Oriented Systems Transport
MSE	Mean-Square Error
MUX	Multiplexer
NRZ	Non Return-to-Zero
PAM	Pulse Amplitude Modulation
PAN	Personal Area Networks
PCB	Printed Circuit Board
PD	Photo Diode
PLL	Phased-Locked Loop
POF	Plastic Optical Fiber
PRBS	Pseudo Random Bit Sequence
PSD	Power Spectral Density
PVT	Process Voltage Temperature
RCLED	Resonant-Cavity Light Emitting Diodes
RMS	Root Mean Square
RX	Receiver
RZ	Return-to-Zero
S&H	Sample and Hold Amplifier
SI-POF	Step-Index Plastic Optical Fiber
SNR	Signal-to-Noise Ratio
SOLT	Short, Open, Load and Through
STP	Shielded Twisted Pair
TIA	TransImpedance Amplifier
TX	Transmitter
UTP	Unshielded Twisted Pair
VCO	Voltage-Controlled Oscillator
VCSEL	Vertical-Cavity Surface-Emitting Laser
VGA	Variable Gain Amplifier
WDM	Wavelength Division Multiplex
ZF	Zero Forcing Algorithm

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Chapter 1
Introduction

In today's world, there is an increasing demand to transmit information from one place to another. Whether it is for long-haul links such as cable or digital television networks, or for short-distance connections such as backplane routing or chip-to-chip interconnects, fast and robust systems are required to correctly drive all the transmitted data.

Because of their low cost and high bandwidth, high-speed CMOS serial link transceivers are widely used for backplane and optical communication networks.

In most systems, the communication channel has become the major bottleneck for the overall bandwidth, and hence the overall performance. Therefore, there is a great research interest in reducing the gap between the on-chip and off-chip bandwidths. Equalization is a well-known technique used to overcome non-idealities introduced by the bandwidth-limiting channel.

In this introductory chapter, we will do a review of the state of the art of equalizers for wireline applications, describing why they are necessary, their types, and their main applications. We avoid the study of equalization for wireless communications, as they present specific equalization problems caused in the multipath fading wireless channel that comes from the mobility of communicators to accomplish the goal of providing all the information asked for any possible location [CHI06, JAL12]. After that, we focus our attention on equalization for short-reach optical communications because that is the application our equalizers are designed for.

1.1 Equalization for High-Speed Serial Links

Recent advances in integrated circuit (IC) fabrication technology coupled with innovative circuit and architectural techniques led to the design of high-performance digital systems. These systems require efficient communication between multiple chips for proper functioning of the whole system. However, the off-chip

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Fig. 1.1 Basic communication system block diagram

bandwidth (BW) scales at a much lower rate when comparing with the on-chip bandwidth, making the off-chip communication link the major bottleneck for the overall performance [LIU04]. Therefore, it is no longer sufficient to solely increase the speed of the ICs to achieve higher data rates.

A representative description of a communication link between two chips is shown in Fig. 1.1. It always involves three basic parts: the transmitter, the channel, and the receiver. Dedicated circuits designed for high-speed operation are used as transmitters and receivers of the data. The medium of transmission is called the channel, which, in the ideal wireline case, is a wire representing a short circuit.

However, the nonideal channel characteristics, e.g., channel bandwidth and crosstalk noise, make them behave as lossy transmission lines severely degrading the quality of the received signal and causing error in data recovery. This is produced since in the practical communication system, the channel behaves like a low-pass filter; therefore, different frequency components of the transmitted signal suffer different attenuation and phase distortion when propagating through the channel. The channel BW limitation decisively contributes to the corruption of the original signal, producing intersymbol interference (ISI): one single bit, which ideally should only occupy one unit interval, spreads over several unit intervals, and the adjacent bits will be interfered such that an error may occur.

According to the Shannon-Hartley theorem, the maximum data rate at which error-free signal can be transmitted through a bandwidth-limited channel in the presence of noise can be improved by widening the bandwidth of the transmission channel or improving the signal-to-noise ratio (SNR) of the signal. The general formula for the Shannon-Hartley theorem is expressed as

$$R_B = BW \cdot \log_2 (1 + SNR) \tag{1.1}$$

where R_B is the data rate measured in bits per second (b/s), BW is the bandwidth of the signal measured in Hz, and SNR is the signal-to-noise ratio [LEE12].

Utilizing multilevel signaling scheme such as duo binary and 4-PAM (pulse amplitude modulation) instead of binary signaling provides spectral efficiencies higher than simple non return-to-zero (NRZ) modulation and can help in reducing the BW requirements of the system [MIN12]. On the other hand, the BW of the system can be improved with relatively low-cost electronics. Equalization is a circuit technique targeting at increasing the data BW of the transmission channel to meet the high data rate requirement. The working principle of an equalizer circuit is aimed to flatten the frequency response of the impaired channel up to at least the Nyquist frequency.[1] Conventional methods such as replacing the channel with

[1] The Nyquist frequency is the bandwidth of a sampled signal, and is equal to half the sampling frequency of that signal.

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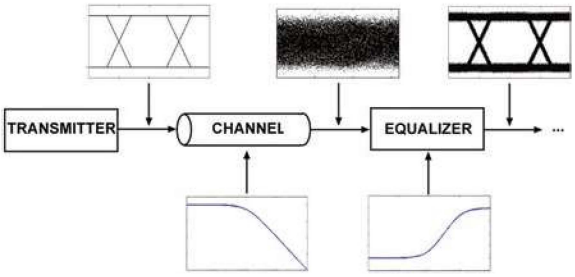


Fig. 1.2 Concept of equalization

low-loss material, incorporating repeater in the channel, and reducing the channel length are no longer effective in solving high-speed communication issues.

Equalizers reduce ISI and can increase the achievable data rates tremendously. The conceptual diagram illustrating the way of performing equalization is shown in Fig. 1.2. In summary, equalization is used to improve the received signal quality for a correct clock and data recovery, so that the system achieves lower bit error rate for the goal of error-free data communications.

A classical equalization application was, and still is, sending fax through the telephone line; the connection tones we hear at the beginning of sending fax are for the purpose of equalization. The path connecting two phone terminals is different depending on the phone number; even with the same phone number, the switch network might connect them differently each time depending on the traffic. Thus, in this case, training sequences known to both the transmitter and the receiver are transmitted; the channel characteristics can be computed by comparing the known training sequence with the actual received signal [LIU04].

Other typical examples are Ethernet communications with transmission rate of several hundred Mb/s [BAB98], where over 100 m of transmission distance causes extreme channel loss, and the magnetic read/write channels for hard disk drives [ABB94, BUR00] with speed around 500 Mb/s, where adjacent track causes severe ISI at high storage densities. Equalization has also been widely used in communication applications such as voice-band modems, wireless [LIN03], digital subscriber lines, and integrated services digital network (ISDN) [INA88]. Recently, equalization has also been used in USB 3.0 redrivers that are used to equalize and reshape the distorted signals so that the following host or device can recover the data without failing the bit error rate specifications [LIU13].

With the increasing demand for higher-speed processing, the data rate in chip-to-chip communications for back-plane, front-plane, personal, and mainframe computer has been pushed to several Gb/s range and even beyond 10 Gb/s range. At this frequency range, the low-cost printed circuit board (PCB) trace introduces significant attenuation to the signal; equalization has become mandatory to ensure reasonable transmission distance [HAR06].

Equalization has been widely used to compensate the attenuation of coaxial cable both in long- and short-distance communication links. For all metallic media, including PCB traces and metallic cables like unshielded twisted pair

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(UTP) cables, shielded twisted pair (STP) cables, and coaxial cables, the channel losses at higher frequencies are mainly caused by skin effect, length of the cable, and dielectric loss [JOH03, LIU05]. This produces a limitation in the BW, which causes ISI, making equalization necessary to increase the rates of transmission over band-limited channels.

However, copper cable systems experience many problems. Therefore, optical communication is outperforming the copper-based communication links as they are cheaper, safer and immune to electromagnetic interference (EMI).

Equalization has also been used in long-distance communications through optical-fiber channels, *e.g.*, in modems and ADSL (asymmetric digital subscriber line), to compensate the dispersion produced by the fiber, principally modal and chromatic dispersion in multimode fibers [ZIE08], as well as other impairments [SHT03].

In medium-distance applications with silica fiber, equalization is not usually necessary: the BW of the channel is several times higher than the transmission frequency. However, in short-distance communications, such as local area networks (LAN) between computers, the economic viability requires the use of low-cost technologies for both microelectronic and optical components. Standard CMOS technologies should be used to implement the electronic part, and polymethylmethacrylate or "plastic" optical fibers (POF) are a cost-effective choice for the optical channel. Therefore, equalization is absolutely essential in this kind of applications to achieve high BW at competitive prices when comparing with transmission using copper wire [BAN08, DON10].

Equalization is not exclusively used for POF applications. For silica fibers, it is usually not necessary because the BW of the fiber and the photodiode (PD) is much higher than the frequency limitation of the electronics circuits. However, for transmission rates higher than 40 Gb/s, the necessity of using equalization arises [LIA08].

Recently, in short-distance and high-volume communication systems, such as: home area networks (HAN), personal area networks (PAN), backplane interconnect, and optical storage systems; optical receivers with monolithically integrated photodetectors have drawn tremendous research interest. In contrast to the conventional multi-die solutions, which are composed of photo-detector implemented in more expensive GaAs or InP-InGaAs technology, the fully integrated optical receiver is much more cost-effective (a really appreciative characteristics as the communication channels are not shared between many users). Besides, the issues of parasitic capacitance introduced by ESD (electrostatic discharge) pads and leading inductance for multi-die integration can be avoided. The main disadvantage of CMOS integrated PD is that the transmission rate is very low. In fact, in the design of integrated front-ends, this response limits the BW of the whole optical receiver. In the literature, there are some alternatives to improve the BW of the PDs; however, most of them use nonstandard CMOS technologies, which contradict the cost aspect previously mentioned. Therefore, equalization is a good alternative to compensate the limited intrinsic frequency response of the integrated PDs [HER06, RAD05, TAV06].

There are several techniques to implement the equalizer circuit. As the characteristics of the communication channels are very different depending on the type of channel (air, vacuum, seawater, twisted pair telephone lines, coaxial cables,

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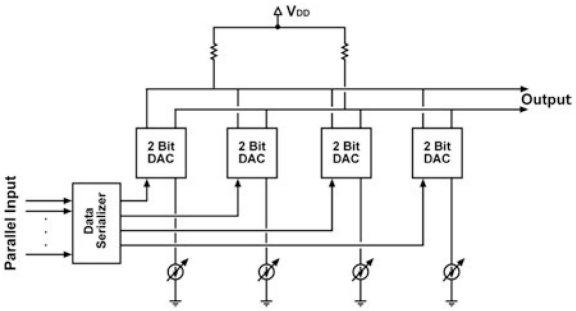


Fig. 1.3 4 tap FIR filter for transmitter pre-emphasis[2]

waveguides, printed circuit board (PCB) traces, fiber-optic cables, and magnetic read/write channels), choosing the right equalization strategy will depend on the particular application and channel characteristics. We now describe different equalization strategies and their trade-offs.

1.1.1 Transmitter Equalization

Depending on the localization of the equalizer, we can differentiate between transmitter equalization and receiver equalization.

Transmitter equalization can be divided into pre-emphasis [DAL97, FAR99, MAR03], if it pre-shapes the transmitted data increasing the high-frequency components, or de-emphasis, if it reduces the power of low-frequency components [FIE97, FOL02, LEE03]. Pre-emphasis can cause electromagnetic interference (EMI) and more severe crosstalk [LIU04], but de-emphasis reduces the emitted power.

Finite impulse response (FIR) filters are generally used for transmitter pre-emphasis. A simplified approach is to use two differential amplifiers, the first one controlled by the original code and the second by emphasis code (produced by inverting the original code and delaying one symbol period).

Figure 1.3 shows the block diagram of 4-tap sparse FIR filter for pre-emphasis equalizer with 4-PAM scheme [STO03]. Four 2-bit digital to analog converters (DAC) serve as the multiplier for FIR filter. Output currents of four multi digital to analog converters (MDACs) are summed up at their output node and converted to voltage.

When parallel data are not present, the tap delay line[3] can be simply realized with digital delay unit without the need for high-speed analog to digital converter (ADC) or analog tap delay line [FAR99]. Figure 1.4 shows a block diagram of transmitter equalizer realized as 4-tap transversal FIR filter.

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[2] In this and the following pictures dc variable current sources are included to symbolize a control signal that depends on the different weight coefficients.

[3] A tap delay line is a discrete element which allows a signal to be delayed by a number of samples. It extracts a signal output from somewhere within the delay line, optionally scales it, and usually sums with other taps for forming an output signal.

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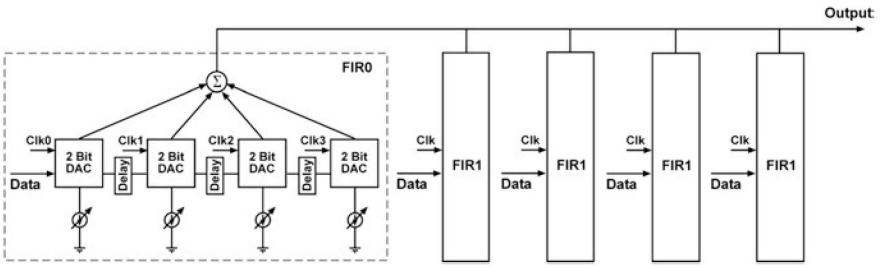
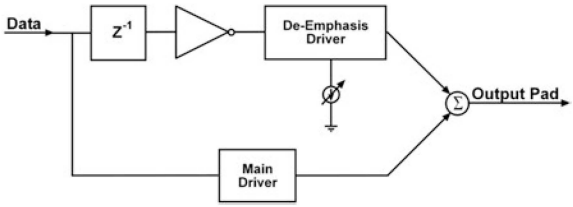


Fig. 1.4 Block diagram of a 4 tap transmitter equalizer

Fig. 1.5 Block diagram of de-emphasis equalizer



As mentioned earlier, transmitter equalizer can also be a de-emphasis filter, which reduces the power of low-frequency component. The simplest way is increasing the signal amplitude at each transition edge and reducing the signal amplitude when there is no transition. In [FIE97], the de-emphasis equalizer uses the inverted signal of previous bit as emphasis signal. During "0" to "1" transition edge, signal amplitude is increased; in "1" to "0" transition edge, signal amplitude is further increased in the negative direction. In other periods when there is no transition, the emphasis signal is opposite to the current bit and the signal amplitude is reduced. Block diagram of de-emphasis equalizer is shown in Fig. 1.5. This de-emphasis is actually a 2-tap FIR filter with a high-pass frequency response. Figure 1.6 illustrates the effect of de-emphasis.

The implementation of transmitter equalization using FIR filter is relatively easier than that at the receiver side, because the parallel data bus naturally supplies the data input for FIR filter. However, there are several limitations in transmitter equalization. First, due to the signal attenuation, transmitter pre-emphasis cannot improve SNR. Second, it is essential to maximize the transmitted signal swings to incorporate large amount of equalization, thus resulting in excessive crosstalk [ZER01]. Third, high-resolution DACs are required to implement pre-emphasis filters to equalizer channels containing large number of ISI terms [ZER03]. Finally, despite transmit pre-emphasis, there is a considerable residual ISI, which results in reduction of both timing and voltage margins, particularly at higher data rates.

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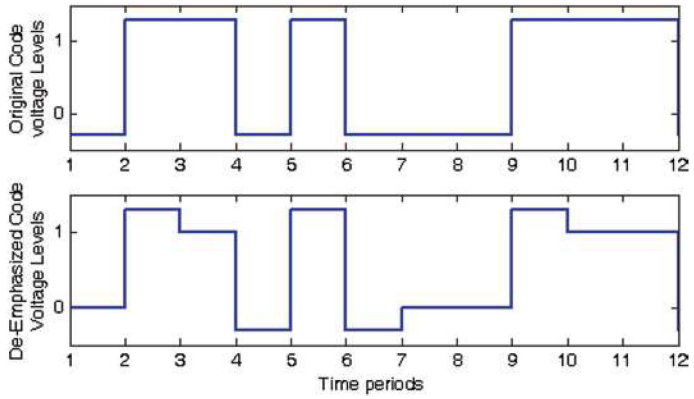


Fig. 1.6 Illustration of de-emphasis

In addition, since pre-emphasis is at the transmitter side, no channel characteristics information is present; so, it is simpler to implement an adaptive equalizer in the receiver because the error signal needed for adaptation is readily available. Although there are some authors who propose adaptive transmitter equalization [GOO11, KIM07], information needs to be sent from the receiver for dynamic or fine-tuned equalization, with special encoding packet or sideband signaling.

Alternatively, in some applications, although the definitive equalization is made on the receiver side, a fixed amount of pre-emphasis without consideration of the channel characteristics is chosen to improve the received signal quality to a certain degree [DON12, HAR06, MAS09]. Both transmitter and receiver equalizations present some problems: peak power constraint in the transmitter equalization, and several nonidealities such as limited bandwidth), noise enhancement, amplifier nonlinearity, in the receiver equalization, as it will be shown later. By using both transmitter and receiver equalizations together, some of the problems can be circumvented.

1.1.2 Receiver Equalization

Receiver equalization offers a method to mitigate ISI without any peak power constraint. The loss in the channel is suppressed by boosting the high-frequency signal spectrum rather than attenuating the low-frequency content. Because of the inherent gain in the system, this method often results in larger noise margins.

We will present now different receiver equalizer architectures.

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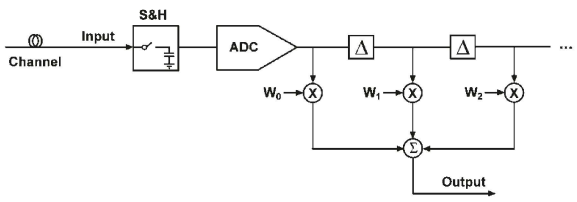


Fig. 1.7 Digital FIR equalizer

Discrete Time Digital FIR Equalizer

A finite impulse response filter (FIR)[4] can be used on the receiver side to perform equalization [RYL01, STA00]. Here, the input to the receiver filter is the output of the channel, which is analog in nature. An analog-to-digital conversion is required to interface the channel output to the filter. Figure 1.7 shows the block diagram of a digital FIR equalizer.

Although digital circuits are more robust than analog circuits, there are two major bottlenecks in the practical implementation of this kind of equalizers. First, the critical path shown in Fig. 1.7 limits the maximum operation frequency to only few hundred megahertz. Well-known techniques such as transposition [AZA98] and parallelism [THO95] can be used to shorten the critical path. Nevertheless, these transposed filters are still speed-limited to less than a gigabit data rate. Second, the practical usefulness of this equalizer is severely limited by the high-speed ADC requirement at the front-end. Even though it is possible to design digital FIR equalizers with high-speed ADCs [CHU09, YAN01], they are hard to realize with CMOS technology at Gb/s data rate and they add large power and area overhead. Also, the front-end ADC can add unwanted latency in adaptive loops such as the timing recovery loop [KIM05]. Owing to these constraints, digital FIR equalizers are employed only in medium-rate interfaces. The price paid for high-speed operation using digital FIR is excessive power consumption.

Discrete Time Analog FIR Equalizer

An analog FIR equalizer [LEE01, RAO12, VAH06] obviates the need for a high-speed ADC and is therefore attractive for high-speed operation with potentially lower power consumption. Figure 1.8 shows a conceptual block diagram of this kind of equalizer. The high-speed ADC is replaced by a simpler sample and hold amplifier (S&H). As opposed to a digital delay in the case of digital FIR, an analog delay chain is required to implement the analog FIR.

Even though digital equalizers have more robustness and are less sensitive to environment parameters, analog equalizers commonly have higher SNR for a given number of taps because they offer the advantage of processing the

[4] A finite impulse response (FIR) filter are distinguished by having an impulse response which become exactly zero past a certain time, thus being of finite duration. This is in contrast to a infinite impulse response (IIR) filter in which the impulse response does not become exactly zero past a certain point, but continues indefinitely.

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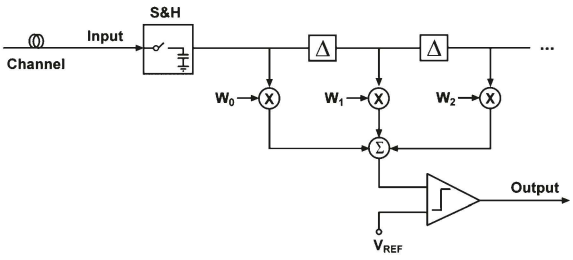


Fig. 1.8 Analog FIR equalizer

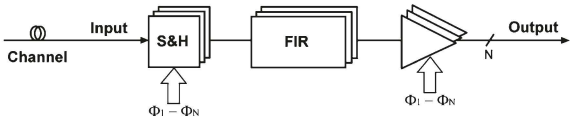


Fig. 1.9 Block diagram of a parallelized analog FIR equalizer

unquantized signal. However, the FIR analog equalizer suffers from many implementation difficulties. First, the settling time of the S&H block limits the overall operating speed. Moreover, each S&H cell introduces distortion and attenuation to the delayed signal. All distortion and attenuation due to nonlinearity, clock feed through, and limited bandwidth of S&H cell will be accumulated along the line [KIR97]. Second, the sampled signal experiences considerable attenuation due to the limited BW of the delay elements in the delay chain. Each unit must settle down in one symbol period, which requires high-frequency clock and wide-bandwidth S&H. Moreover, this limited bandwidth-induced error accumulates along the delay chain, thus limiting this technique to FIR filters with few taps. Finally, the precise generation of analog delay consumes excessive power at high data rates, thus invalidating the main benefit of an analog FIR equalizer.

To avoid error accumulation, parallel sampling units can be used permitting very high data rates [JAU04, MEK10, RAO12]. The conceptual block diagram of a parallelized analog FIR equalizer is shown in Fig. 1.9. Extra redundant S&H units have been added to relieve timing constraint on settling time of S&H. Phases Φ_i represent the different phases of a clock. This method lowers speed requirement of S&H at the cost of additional delay and area.

Employing parallelism and time-interleaving, this architecture is suitable for equalizing multi-gigabit serial links, at the expense of increased power and area incurred due to massive parallelism.

Continuous-Time Equalizer

The discrete-time receiver equalizers discussed thus far need sampling front-end to perform equalization. This requirement results in two main drawbacks. First, the sampling clock-jitter reduces the effectiveness of the equalization. Second, in a truly serial communication system, the clock is recovered from the incoming data. However, due to the sampling front-end, the clock-recovery loop needs to operate on raw channel output resulting in an excessive jitter in the recovered clock [BUC04].

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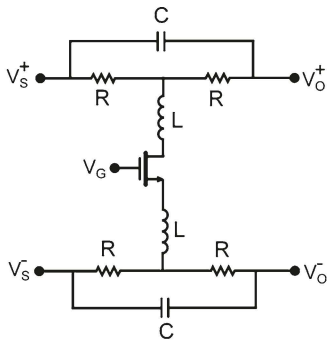


Fig. 1.10 Circuit diagram of a differential passive equalization filter [SUN05]

Therefore, practical serial links employing discrete-time FIR equalizers are limited to source synchronous interfaces [JAU04] containing a separate clock channel, such as high-speed interfaces between microchips, including DDR, SDRAM, etc.

Continuous-time circuits that can provide high-frequency boost are a very attractive alternative. A continuous-time equalizer is a simple one-tap continuous-time circuit with high-frequency gain boosting transfer function that effectively flattens the channel response. A continuous-time equalizer can exhibit a good trade-off for low-power high-speed applications, requiring less complexity and smaller area than discrete-time or purely digital approaches.

The simplest continuous-time solution is to use a passive receiver equalizer. Some authors [SUN05, SUN11] use this alternative because fixed passive equalization is easy to implement, it can work in a wide bit rate range, and has low power consumption. Figure 1.10 shows an example of a passive equalizer.

However, the implementation highly depends on the coding scheme, it is sensitive to the process variation, and has a low SNR level (equalization is performed by attenuating low-frequency signal spectrum) and narrow compensation range. Moreover, in most cases, inductors have to be used to avoid large impedance discontinuity at the channel and equalizer interface, making it less suitable for on-chip integration, as they require a big chip area to be implemented and are not available in every technology. Therefore, passive equalizers have limited use in high-speed serial links; they are preferred when the received signal has large amplitude and the receiver sensitivity is high.

It is desirable to have a greater gain to maximize the benefit from receiver-side equalization. Therefore, equalizers using active circuit elements rather than passive components are required.

Active filters with a desired frequency response can be designed using standard filter design techniques [SCH01]. Such standard filters are typically implemented either with operational amplifiers in negative feedback or with Gm-C split-path amplifiers. Traditional filters using operational amplifiers in negative feedback provide precise gain and low nonlinearity [BAB98]. However, the negative feedback greatly degrades the maximum operating frequency preventing the amplifier to work in the gigahertz range. Phase mismatch between feedback loop and input

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