APPENDIX INTEL05

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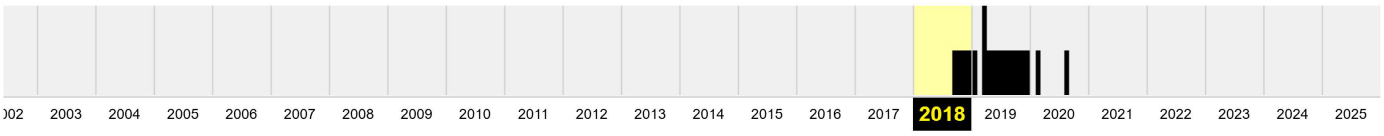
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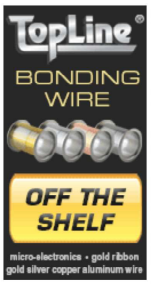
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IMAPS 2018 - Pasadena

51st Symposium on Microelectronics

www.imaps2018.org

PASADENA
51st International Symposium on Microelectronics
October 8-11, 2018
Pasadena Convention Center

Conference: October 9-11, 2018

Exhibition: October 9-10, 2018

Professional Development Courses: October 8, 2018

General Chair:
Mark Gerber
ASE US Inc.

General Chair-elect (2019):
Curtis Zwenger
Amkor Technology

Past General Chair (2017):
Dan Krueger
Honeywell FM&T

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TECHNICAL PROGRAM

(Keynote Presentations, Sessions, Posters, and more!)

REGISTER ONLINE

Technical Program	PDCs (Short Courses)	Registration & Hotel	Speakers	Students
For Exhibitors	Visiting the Exhibits			

Monday, October 8, 2018

Professional Development Courses (PDCs) - 8:00 AM - 5:30 PM

Monday, October 8: 2-hour formats, by theme/track

8:00 AM-10:00 AM | 10:30 AM - 12:30 PM | 1:00 PM - 3:00 PM | 3:30 PM - 5:30 PM

Attendees can take ONE PDC during each timeslot

	Track A: Intro to Microelectronics Packaging	*Track B: Process and Materials*	*Track C: Emerging Technologies*	*Track D: Reliability*
8:00 AM-10:00 AM	A1: Fundamentals of Microelectronics Packaging - PART 1 - John Pan, Cal Poly University	B1: Polymers Used in Wafer Level Packaging - Jeff Gotro, InnoCentrix	C1: Flexible Ceramics - John Olenick, ENrG Inc.	D1: Achieving High Reliability Solder Joints for Lead-Free Alloys - Dr. Ning-Cheng Lee, Indium Corporation
10:00 AM-10:30 AM	**Coffee / Networking** *Open to all PDC participants*			
10:30 AM - 12:30 PM	A2: Introduction to System in Package (SiP) - The Heterogeneous Integration Driver - Mark Gerber, ASE	B2: Electroplating Processes for Flip Chips - Fred Mueller Consultant, Metal Finishing	C2: Electronic Packaging for 5G Microwave and Millimeter Wave Systems - Rick Sturdivant, Ph.D.,	D2: Package/Board Level Integrity & Solder Joint Reliability - Dr. Jennie S. Hwang,

	US, Inc.	Instructor	Azusa Pacific University	Ph.D., D.Sc. H-Technologies Group
12:30 PM-1:00 PM	**Lunch** *Open ONLY to PDC participants taking morning AND afternoon courses*			
1:00 PM-3:00 PM	A3: Fan-Out Wafer/Panel-Level Packaging - John Lau, ASM	B3: Introduction to Solder Flip Chip with an Emphasis on Cu Pillar - Mark Gerber, ASE US, Inc.	C3: MEMS and nanoMEMS Packaging - Slobodan Petrovic, Oregon Institute of Technology	D3: A Methodology for Understanding the Reliability of Electronic Packaging - Greg Caswell, DfR Solutions
3:00 PM-3:30 PM	**Coffee / Networking** *Open to all PDC participants*			
3:30 PM-5:30 PM	A4: Fundamentals of Microelectronics Packaging - PART 2 - John Pan, Cal Poly University	B4: Temporary Bonding of Electronics (Wafers, Packages, Displays) - John Moore, Daetec LLC	C4: Fundamentals of 3D and 2.5D Packaging Integration - Urmi Ray, JCET Group	D4: Thermal Stress Failures in Electronic Packaging: Prediction and Prevention - Ephraim Suhir, Portland State University
5:30 PM-7:30 PM	**Welcome Reception** *Open to all IMAPS 2018 participants*			

Cost for Each PDC: $300 (on/before 9/12/2018); $400 (after 9/12/2018)
REGISTER ONLINE

Microelectronics/Packaging Industry Tour - 1:00 PM - 3:30 PM - (Departure approx. 12pm & Return approx. 4pm)
JET PROPULSION LABORATORY

*****TOUR REGISTRATION HAS CLOSED*****

â€¢ All US citizens 18 years of age or older visiting JPL MUST present official, government-issued photo identification, such as a driver's license or passport, before being allowed entry.
â€¢ All non-US citizens (Foreign Nationals) 18 years of age or older MUST present either a passport or resident visa (green card) before being allowed entry. Individuals without the appropriate identification will NOT be admitted to the facility.
â€¢ The tour includes considerable walking and stair climbing. Dress comfortably and appropriately for the weather. Wheelchairs can be accommodated with prior notice. Cameras are allowed on the tour. *Note: All tours are conducted in English*

Welcome Reception | 5:30 PM - 7:30 PM
Pasadena Convention Center

Welcome Reception Sponsored by:

Premier Program Sponsor:

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DIVERSITY Discussion and Networking | 7:00 PM - 8:00 PM
Join IMAPS leaders for a networking discussion on diversity in IMAPS and the microelectronics industry on Monday, October 8th from 7pm-8pm just following the welcome reception. Moderators will lead a question and answer questions about overcoming diversity barriers, using your strengths in a diverse workforce, and promoting cooperation and communication in the work environment, plus additional topics. Come explore options to bridge generational, cultural, and gender communication gaps. All IMAPS attendees are invited to participate!

TUESDAY, OCTOBER 9, 2018

7:00 AM - 6:00 PM: Registration Open
11:00 AM - 5:00 PM: Exhibit Hall Open

IMAPS 2018 Opening & Plenary Session:
PASADENA CONVENTION CENTER

8:00 AM - 8:20 AM: Welcome, IMAPS Business Meeting, and more
Ron Huemoeller, Amkor Technology - IMAPS President

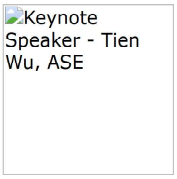
8:20 AM - 8:45 AM: Welcome to IMAPS 2018 & Intro of Keynotes
Mark Gerber, ASE Group - IMAPS 2018 General Chair

Keynote Session sponsored by:

8:45 AM - 9:30 AM: Keynote Presentation 1

Bridging the Gaps

The packaging industry is facing higher expectations in business enablement due to the increasing complexity of inhomogeneous integration alongside multiple dimensions of business requirements. During his keynote, Dr. Tien Wu will focus on key aspects of future packaging technologies and explore how these might open up new design concepts and business freedoms to ultimately enable better performance and efficiency at the system level.



Tien Wu, Ph.D. ASE
President & CEO

Dr Tien Wu is the President and Chief Executive Officer of Advanced Semiconductor Engineering, Inc (ASE) and concurrently the Chief Executive Officer of Universal Scientific Industrial Co (USI). Tien serves as a Board Member of the Global Semiconductor Association (GSA) and SEMI, both of which are global industry associations serving the manufacturing supply chain for the micro- and nano-electronics industries.

Prior to joining ASE, Tien held several management positions within IBM including R&D, manufacturing and sales in the United States, Europe and Asia-Pacific. He holds twelve U.S. patents and has authored over twenty-five articles. Tien holds a BSCE degree from Taiwan University, and also earned MS and Ph.D. degrees in mechanical engineering and applied mechanics respectively from the University of Pennsylvania. In 2015, Tien received an Honorary Degree of Doctor of Science from Binghamton University.

9:30 AM - 10:15 AM: Coffee Break in Foyer

Coffee Break Sponsor:

Break Sponsor: Geib Refining

10:15 AM - 11:00 AM: Keynote Presentation 2

Challenges and Potential Solutions in Heterogeneous Integration from a Foundry Viewpoint

A common need across computing and communication products is integration of different functions that do not integrate well on a single chip for various reasons. The cost of leading-edge integration is also become unaffordable to all but the largest volume devices. One node is not the best solution for all functions. The demand for fast access memory is causing die size to exceed reticle size. Integration of RF devices with antennas will drive 5G products. All this integration must be done at a lower cost than is available today. Multi-chip devices are needed but how will first pass design success be enabled? How will IC interfaces be enabled when they come from different suppliers? These challenges and some solutions will be discussed.



David McCann, GLOBALFOUNDRIES
Vice President, World Wide Post Fab

David McCann has been at GLOBALFOUNDRIES for seven years, where he is Vice President of Packaging R+D and Operations. He is responsible for GFâ€™s internal bump and probe factories, for packaging and test development for GFâ€™s Foundry, ASIC, and RF businesses, for OSAT partnerships, supply chain qualification and external bump-probe-assembly-test production. He is based at the Fab 8 site, in Malta, New York. He led the GLOBALFOUNDRIES/IBM post-fab process and business integration.

Davidâ€™s background prior to GLOBALFOUNDRIES was in flip chip technology development and business management in the OSAT industry, and prior to that, flip chip assembly and product development in implantable medical electronics.

11:00 AM - 11:15 AM:
This Weekâ€™s Program & Future IMAPS Activities
Urmi Ray, JCET Group & IMAPS VP of Technology

***** IMAPS 2018 EXHIBITS OPEN: 11:00 AM - 5:00 PM *****

11:15 AM - 2:00 PM: Lunch Break in Exhibit Hall

Exhibit Lunch Sponsor:

TUESDAY AFTERNOON PROGRAM

	SiP/SiM (Systems Solutions) *Track Chairs:* ***Urmi Ray, JCET Group; Rich Rice, ASE Group***	Wafer Level/Panel Level (Advanced RDL) *Track Chairs:* ***John Hunt, ASE Group; Rajiv Dunne, Qualcomm***	High Performance-High Reliability *Track Chairs:* ***Erica Folk, Northrop Grumman; Ivan Ndip, Fraunhofer IZM***	Flip Chip/ 2.5D/3D/Optical (Advanced Package) *Track Chairs:* ***Karl Friedrich Becker, Fraunhofer-IZM; Sandeep Sane, Intel***	Advanced Process & Materials (Enabling Technologies) *Track Chairs:* ***Habib Hichri, SUSS Microtec; Benson Chan, Binghamton Univ.***
	Session TP1 **SYSTEM DESIGN & INTEGRATION** Session Chairs: Venky Sundaram; Dickson Yeung, Huawei	**Session TP2** **ADVANCED FAN OUT** Session Chairs: Suresh Jayaraman, Amkor Technology; Kim Yess, Brewer Science	**Session TP3** **HIGH RELIABILITY IN EXTREME ENVIRONMENTS** Session Chairs: Zhenzhen Shen, Baker Hughes GE; Carl Edwards, Adv Materials Innovations	**Session TP4** **LARGE BODY / SMALL BODY FLIP CHIP** Session Chairs: Rockwell Hsu, Cisco; Jaimal Williamson, Texas Instruments	**Session TP5** **SUBSTRATE TECHNOLOGY** Session Chairs: Ton Schless, Sibco; Aric Shorey, Mosaic Microsystems
2:00 pm - 2:25 pm	037 **A 3D System-in-Package (SiP) for RF Application** Shihwen "Wayne" Liu, ASE Group (Chanlin Yeh, Gavin Kao, YE Yeh, Harrison Chang)	057 **Upscaling panel size for Cu plating on FOPLP (Fan Out Panel Level Packaging) applications to reduce manufacturing cost** Henning HÃ¼bner, Atotech Deutschland GmbH (Christian Ohde, Dirk Ruess)	182 **Converter-Level Integration for Wide Band-Gap Automotive Power Electronics** Bassem Mouawad, C Mark Johnson, University of Nottingham (Jordi Espina, The Thinking Pod Innovations Ltd; Behzad Ahmadi, Jingru Dai, Lee Empringham, Liliana De Lillo, University of Nottingham; Christina Dimarino, Virginia Tech)	030 **Thin Core Substrate Large Size FCBGA Stress and Thermal Challenges and Characterization** PoHsien Sung, Advanced Semiconductor Engineering, Inc. (Ian Hu, Penny Yang, Avis Feng, Shouyi Chin, MengKai Shih, David Tarng, Marwan Wang, CP Hung)	063 **A Comparison of the Cu Electromigration Behavior Between Cu Lines with 5 Âµm L/S Realized by Conventional Semi Additive Process (SAP) and an Innovative Excimer Laser Damascene Process** Robert Gernhardt, Fraunhofer IZM (Friedrich MÃ¼ller, Karin Hauck, Fraunhofer IZM; Markus Woehrmann, Klaus-Dieter Lang, Technische University of Berlin; Habib Hichri; Markus Arendt, Suss MicroTec Photonic Systems Inc.)
2:30 pm - 2:55 pm	072 **A Cross-Domain, System Planning Methodology** Bill Acito, Cadence Design Systems	052 **Unlocking the full Potential of Lithography for Advanced Packaging** Jelle van der Voort, Kulicke & Soffa Liteq B.V.	163 **Novel Solder Alloy with Wide Service Temperature Capability for Automotive Applications** Ning-Cheng Lee, Indium Corporation (Jie Geng, Hongwen Zhang, Francis Mutuku)	136 **fcLGA Package Assembly Qualification for Mobile Applications** Mumtaz Bora, PSEMI	076 **Physical and Application Characteristics of Core-Shell Conductive Materials for LTCC in 5G Technology** Richard Stephenson, SVMT LLC
3:00 pm - 3:25 pm	093 **Recess in the Motherboard Architectures for Small Form Factor Systems** Tim Swettlen, Intel Corp. (Juan Landeros, Scott Mokler, Antonio Caputo)	120 **Advances in Temporary Bonding and Debonding Technologies for use with Wafer-Level System-in-Package (WLSiP) and Fan-Out Wafer-Level Packaging (FOWLP) Processes** Michelle Fowler, Brewer Science, Inc (John Massey, Matthew Koch, Kevin Edwards, Brewer Science, Inc; Tanja Braun, Steve Voges, Robert Germhardt, Markus Wohrmann, Fraunhofer Institute IZM)	036 **Power Cycle Tests of High Temperature Ag Sinter Die-attach on Metalized Ceramic Substrate by Using Micro-heater SiC Chip** Dongjin Kim, The Institute of Scientific and Industrial Research, Osaka University (Shijo Nagao, Aiji Suetake, Katsuaki Suganuma, Osaka University; Naoki Wakasugi, Yamato Scientific Co., Ltd.; Yusuyuki Yamamoto, Tokuyama Co., Ltd.; Tetsu Takemasa, Senju Metal Industry Co., Ltd.)	025 **Molding Recipe Study for MUF Solder Crack Improvement** Michael Shy, Advanced Semiconductor Engineering, Inc. (Scott Chen, Leander Liang, Pallas Hsu, Tim Tsai, Mason Liang)	035 **The Effect of Nickel Oxide Formed in the Interface of ENEPIG Structure for Flip Chip Technology** Chuan Lung Chuang, ASE Global (Min-Fong Shu, Yi-Hsiu Tseng)
	Dessert & Coffee Break in Exhibit Hall: 3:25 PM - 4:30 PM **Dessert Break Sponsor:** EMD Performance Materials				
4:30 pm - 4:55 pm	086 **Universal Connection Matrix: A Breadboard in a Package** Erik Welsh, Octavo Systems	152 **Design, Materials, Process, and Fabrication of Fan-Out Panel-Level Heterogeneous Integration** John Lau, ASM Pacific Technology (Cheng-Ta Ko, Henry Yang, Curry Lin, JW Lin, YH Chen, Unimicron Technology Corp.; Ming Li, Margie Li, Penny Lo, Nelson Fan, Eric Kuah, ASM Pacific Technology; Chieh-Lin Chang, Jhih-Yuan Pan, Hsing-Hui Wu, Chia-Hung Lin, Rozalia Beica, Dow Chemical Company; Tony Chen, Iris Xu, Zhang Li, Kim Hwee Tan, Jiangyin	096 **Perspectives of High-Temperature Pb-Free Bonding Materials** Hongwen Zhang, Indium Corporation (Ning-Cheng Lee)	077 **Understanding Mold Compound Behavior on Flip Chip QFN Packages** Ruby Ann M. Camenforte, Texas Instruments (Jason Colle, Richard Sumalinog, Sylvester Sanchez, Jaimal Williamson)	123 **Result of High Accelerated Stress Test of Organic Substrates made by Integrated Dry Process** Tomoyuki Habu, Ushio Inc. (Shinichi Endo, Shintaro Yabu)

		Changdian Advanced Packaging Co., Ltd.; Cao Xi, Huawei Technologies Co. Ltd.; Sze Pei Lim, NC Lee, Indium Corp.; Mian Tao, Jeffery Lo, Ricky Lee, Hong Kong University of Science and Technology)			
5:00 pm - 5:25 pm	139 **System-level Trade-offs and Optimization for Data-Driven Applications** Pushkar Apte, SEMI (Tom Salmon, SEMI; Richard Rice, Mark Gerber, Patricia Macleod, ASE Inc.; Rozalia Beica, Jeff Calvert, Dow Chemical; Dave Hemker, Yezdi Dordi, Manish Ranjan, Lam Research; Suresh Kamalingam, Jaspreet Gandhi, Alireza Kaviani, Xilinx; Subhasish Mitra, Philip Wong, Vincent Lee, Mohamed M. Sabry Aly; Stanford University)	114 **Ultra Fine RDL Formation using an Alternative Pattering Solution for Advanced Packaging** Habib Hichri, SUSS MicroTec Photonic Systems Inc	121 **3D Printed and Additively Manufactured RoboSiC for Space, Cryogenic, Laser and Nuclear Environments** Bill Goodman, Goodman Technologies LLC	022 **FCCSP IMC Growth under Reliability Stress follow Automotive Criteria** Wei-Wei "Xenia" Liu, Advanced Semiconductor Engineering (Berdy Weng, Jerry Li, CK Yeh)	020 **Copper Oxidation Effect in the EMC/Cu Interfacial Adhesion Improvement for a Novel Copper Interconnection Substrate Application** Min-Fong Shu, ASE Group (Yi-Hsiu Tseng)
5:30 pm - 5:55 pm	095 **Flip Chip Reliability and Intermetallic Compounds for SIP Module** Adrien Morard, SAFRAN Tech (Jean-Christophe Riou, Safran Electronics & Defense; Gabriel Pares, CEA Leti)	186 **Fine Pitch(40µm) Integration Platform for Flexible Hybrid Electronics using Fan-Out Wafer-level Packaging** Amir Hanna, University of California, Los Angeles (Arsalan Alam, Goutham Ezhilarasu, Subramanian Iyer)	138 **Solder-Joint Reliability of a Radar Processor for Semi-Autonomous Driving Applications** Mollie Benson, NXP Semiconductors (Burton Carpenter, Andrew Mawer)	006 **Fluxes Effective in Suppressing Non-Wet-Open at BGA Assembly** Ning-Cheng Lee, Indium Corporation (Fengying Zhou, Fen Chen)	009 **Shear Strength and Thermo-mechanical Reliability of Sintered Ag Joints Containing low CTE Non-metal Additives for Die Attach** Guangyu Fan, Indium Corporation (Christine Labarbera, Ning-Cheng Lee, Indium Corporation; Colin Clark, Rochester Institute of Technology)

WEDNESDAY, OCTOBER 10, 2018

7:00 AM - 7:00 PM: Registration Open
11:00 AM - 5:30 PM: Exhibit Hall Open

IMAPS 2018 Plenary Session:
PASADENA CONVENTION CENTER

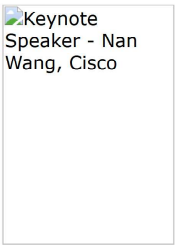
8:00 AM - 8:15 AM: Day 2 Opening Comments & Intro of Keynote
Mark Gerber, ASE Group - IMAPS 2018 General Chair

Keynote Session sponsored by:

8:15 AM - 9:00 AM: KEYNOTE PRESENTATION 3

Accelerating the Digital Transformation - An Ecosystem View

This keynote will provide an overview of the industry trend that drives the networking bandwidth and performance growth, market transition to more intelligent and intent based networking solutions, and underlying technology and business drivers for highly integrated systems in silicon and package. It will also attempt to share a view on how the emergence of AI and machine learning is shaping the new wave of customer applications, its implication to compute and networking solutions, as well as why it is imperative that we leverage this new technology capability to collaborate and partner much more closely as an ecosystem to jointly tackle some of the common challenges.



Mr. Nan Wang, Cisco Systems, Inc.
Sr. Director, Technology and Quality, Supply Chain Operations

Nan Wang has been with Cisco Systems for 17 years, where he serves as Sr. Director in the Technology and Quality organization within Ciscoâ€™s global Supply Chain Operations. He leads the Component Quality and Technology Group, with focus on strategic component technology development for next generation products across Cisco.

In recent years, his team has been focusing on the component technology innovations, such as Silicon Photonics, 2.5D/3D IC, to enable the next generation of the networking applications and accelerate the digital transformation.

WEDNESDAY MORNING PROGRAM

	SiP/SiM (Systems Solutions)	Wafer Level/Panel Level (Advanced	High Performance-High Reliability	Flip Chip/ 2.5D/3D/Optical (Advanced	Advanced Process & Materials

		RDL)		Package)	(Enabling Technologies)
	Track Chairs: ***Urmi Ray, JCET Group; Rich Rice, ASE Group***	*Track Chairs:* ***John Hunt, ASE Group; Rajiv Dunne, Qualcomm***	*Track Chairs:* ***Erica Folk, Northrop Grumman; Ivan Ndip, Fraunhofer IZM***	*Track Chairs:* ***Karl Friedrich Becker, Fraunhofer-IZM; Sandeep Sane, Intel***	*Track Chairs:* ***Habib Hichri, SUSS Microtec; Benson Chan, Binghamton Univ.***
	Session WA1 CPI and MODELING Session Chairs: Karthik Dhandapani, Qualcomm; Lei Fu, AMD	**Session WA2 WAFER-LEVEL FAN OUT** Session Chairs: Eric Gongora, Enthone; Elvino Da Silveira, Rudolph Technologies	**Session WA3 mm WAVE/ HIGH-SPEED PACKAGING** Session Chairs: Ken Kuang, Torrey Hills Technologies; Rick Sturdivant, MPT, Inc.	**Session WA4 ADVANCED INTERPOSER TECHNOLOGIES** Session Chairs: Akash Agrawal, AMD; Manish Dubey, Intel	**Session WA5 POLYMER MATERIALS / PROCESSES** Session Chairs: Frank Eberle, Northrop Grumman; Jeff Gotro, InnoCentrix, LLC
9:10 am - 9:35 am	055 **Chip Package Interaction: Understanding of Contributing Factors in Back End of Line (BEOL) Silicon / Cu Pillar Design and Applied Process Improvements** Frank Kuechenmeister, GLOBALFOUNDRIES (Dirk Breuer, Holm Geisler, Bjoern Boehme, Kashi Vishwanath Machani, Michael Hecker, Sven Kosgalwies, Jae Kyu Cho, GLOBALFOUNDRIES; Dongming He, Xuefeng Zhang, Lily Zhao, Qualcomm Technologies)	099 **Enabling Robust Copper Seed Etching for Fine Line RDL by Electroplating on a Thin PVD Seed Layer** Marvin Bernt, Applied Materials (Paul Van Valkenburg, David Surdock, Prayudi Lianto)	071 **5G Systems and Packaging Opportunities** Rick Sturdivant, MPT, Inc.	061 **Cu Diffusion into the Glass Under Bias Temperature Stress Condition for Through Glass Vias (TGV) Applications** Hoon Kim, Corning Research and Development Corp. (Ling Cai, Albert Fahey, Rajesh Vaddi, Bin Zhu, Prantik Mazumder)	040 **Smart Passivation Materials with a Microencapsulated Liquid Metal for Self-Healing Conductors in Sustainable Electronic Devices** Kinman Chu, Samsung Advanced Institute of Technology (Byong Gwon Song, Yongsung Kim, Chang Seung Lee)
9:40 am - 10:05 am	085 **System Co-Design Modeling Methodology of a High Speed (25Gbps) Multi-Rate 4-Channel Retimer: Simulation to Measurement Correlation** Tony Tang, Texas Instruments, Inc. (Bridger Wray, Rajen Murugan)	101 **Enhancements to Picosecond Acoustic Metrology for application in FO-WLP Process** Johnny Dai, Rudolph Technologies (M. Mehendale, R. Mair, J. Chen, J. Tan, P. Mukundhan, C. Kim, T. Kryman)	151 **Systematic Design of Ka-band Transmitter Modules using the M3-Approach** Ivan Ndip, Fraunhofer IZM (Christian Tschoban, Jacob Reyes, Brian Curran, Klaus-Dieter Lang)	080 **Processing Through Glass Via (TGV) Interposers for Advanced Packaging** Charles G. Woychik, i3 Electronics, Inc. (John Lauffer, David Bajkowski, Michael Gaige, Robert Edwards, Gordon Benninger, William Wilson)	097 **Fabrication of an Advanced Epoxy based Molding Compound with High Thermal Conductivity and Exceptional Mechanical Properties** Nazila Dadvand, Texas Instruments Inc. (Mina Dadvand, Polytechnique de Montreal; Georges Kipouros, Dalhousie University)
	Coffee Break in Foyer: 10:05 am - 10:30 am **Coffee Break Sponsor:** PacTech				
10:30 am - 10:55 am	094 **A Systematic Approach to the Reliability Characterization of System in Package (SiP)** Karthikeyan Dhandapani, Qualcomm, Inc. (Brian Roggeman, David Rae)	028 **Optical Run-Out Correction for Improved Lithography Overlay Accuracy for FOWLP Applications** Habib Hichri, SUSS MicroTec Photonic Systems Inc. (William Vis, Markus Arendt)	158 **Enabling High-Performance Heterogeneous Integration via Interface Standards, IP Reuse, and Modular Design** Jeffrey Demmin, Booz Allen Hamilton (Andreas Olofsson, Defense Advanced Research Projects Agency; Daniel S. Green, Office of Naval Research)	029 **Bumping Process Impact on the Chip Package Interaction (CPI) Reliability** Lei Fu, Advanced Micro Devices (Milind Bhagavat, Ivor Barber)	125 **Advanced Build-up Materials for High Speed Transsmission Application** Shiro Tatsumi, AJINOMOTO CO., INC.
11:00 am 11:25 am	017 **System ElectroThermal Co-Design of a Zero-Drift Current-Shunt Monitor with Precision Integrated Shunt Resistor** Jie Chen, Texas Instruments, Inc. (Rajen Murugan, Steven Kummerl, Usman Chaudhry, Edwin Lim, Tatsuhiro Shimizu, Thatcher Klumpp, Jack Grantham)	118 **Customization of Chemistry Continues** Eric Gongora, Elie Najjar, MacDermid Enthone Advanced Electronic Solutions	054 **Packaging and Integration Strategy for mm-Wave Products** Urmi Ray, JCET Group (NJ Cho, YC Kim, SW Yoon, WK Choi, Pandi Marimuthu, JCET Group)	172 **High Frequency Base Materials: Laser-Material Interaction for HDI/ICP Applications** Christopher Ryder, ESI	120 **Solderable Polymer Thick-film Conductors for Low Temperature Substrates** Gregory Berube, Heraeus Precious Metals North America (Seigi Suh, Ryan Persons, Doug Hargrove)
11:30 am - 11:55 am	007 **Sn3.2Ag0.7Cu5.5Sb Solder Alloy with High Reliability Performance up to 175C** Ning-Cheng Lee, Indium Corporation (Jie Geng, Hongwen Zhang, Francis Mutuku)	153 **Reliability of Fan-Out Wafer-Level Heterogeneous Integration** John H Lau, ASM Pacific Technology (Ming Li, Yang Lei, Margie Li, Wu Kai, Penny Lo, Y. M. Cheung, Nelson Fan, Eric Kuah,ASM Pacific Technology; Iris Xu, Tony Chen, Zhang Li, Kim Hwee Tan, Jiangyin Changdian Advanced Packaging Co., Ltd.; Qing Xiang Yong, Zhong Cheng, Cao Xi, Jiang Ran, Huawei Technologies Co. Ltd.; Rozalia Beica, Dow Chemical Company; Sze		193 **Status on 3D Stacking Using Direct Hybrid Bonding** Bruno Paing, CEA LETI (Severine Cheramy, Amandine Jouve, Lucile Arnaud)	178 **Evaluation of Low Cost, High Temperature Die and Substrate Attach Materials for Silicon Carbide (SiC) Power Modules** Sayan Seal, WolfSpeed, a CREE Company (Brice McPherson, Brandon Passmore)

		Pei Lim, N. C. Lee, Indium Corporation; C. T. Ko, Henry Yang, Y. H. Chen, Unimicron Technology Corporation; Mian Tao, Jeffery Lu, Ricky Lee, Hong Kong University of Science and Technology)			

12:00 pm - 1:15 pm: Lunch in Exhibit Hall

Lunch Sponsor:



WEDNESDAY AFTERNOON PROGRAM

	SiP/SiM (Systems Solutions) *Track Chairs:* ***Urmi Ray, JCET Group; Rich Rice, ASE Group***	**Wafer Level/Panel Level (Advanced RDL)** *Track Chairs:* ***John Hunt, ASE Group; Rajiv Dunne, Qualcomm***	**High Performance-High Reliability** *Track Chairs:* ***Erica Folk, Northrop Grumman; Ivan Ndip, Fraunhofer IZM***	**Flip Chip/ 2.5D/3D/Optical (Advanced Package)** *Track Chairs:* ***Karl Friedrich Becker, Fraunhofer-IZM; Sandeep Sane, Intel***	**Advanced Process & Materials (Enabling Technologies)** *Track Chairs:* ***Habib Hichri, SUSS Microtec; Benson Chan, Binghamton Univ.***
	Session WP1 **EMBEDDED & HIGH DENSITY** Session Chairs: Trevor Yancey, TechSearch International; Mak Kulkarni, Texas Instruments	**Session WP2** **PANEL-LEVEL FAN OUT** Session Chairs: Markus WÃ¶hrmann, Fraunhofer IZM; Linda Bal, TechSearch International	**Session WP3** **RF/WIRELESS COMPONENTS** Session Chairs: Ivan Ndip, Fraunhofer IZM; Ege Engin, San Diego State University	**Session WP4** **OPTICAL and ENABLING TECHNOLOGIES** Session Chairs: Kevin Demartini, DuPont; Jim Will, Honeywell FM&T	**Session WP5** **NOVEL MATERIALS / PROCESSES** Session Chairs: Benson Chan, Binghamton Univ.; W. Hong Yeo, Georgia Tech
1:15 pm - 1:40 pm	083 **Increase Power Density and Simplify Designs Using 3-D SiP Modules** Steven Kummerl, Texas Instruments (Charles Devries, Usman Chaudhry, Chong Han Lim)	089 **Fine Line Panel Level Fan Out changes the SiP Landscape** David Fang, Powertech Technology Inc. (Michael Hsu, CC Chang, KW Chung, Alex Liu, Irving Lin, Daniel Fann)	141 **Low-fire Processing and Dielectric Properties of a Binary Crystallizable Glasses+alumina System** Jau-Ho Jean, National Tsing Hua University (Shih-An Tung)	019 **Design of Solder Connections for Self-Assembly of Optoelectronic Devices** Thomas Marinis, Charles Stark Draper Laboratory (Joseph Soucy)	111 **Reliability of Novel Ceramic Encapsulation Materials for Electronic Packaging** Stefan Kaessner, Robert Bosch GmbH (M. Scheibel, Heraeus Deutschland GmbH & Co. KG; S. Behrendt, Forschungs- und Entwicklungszentrum FH Kiel GmbH; B. Boettge, Fraunhofer IMWS; K. G. Nickel, University of Tuebingen)
1:45 pm - 2:10 pm	117 **Design and Demonstration of Glass Panel Embedding for 3D System Packages for Heterogeneous Integration Applications** Siddharth Ravichandran, 3D Systems Packaging Research Center, Georgia Institute of Technology (Fuhan Liu, Vanessa Smet, Venky Sundaram, Rao Tummala, Georgia Tech.; Shuhei Yamada, Murata Manufacturing Co., Ltd.; Tomonori Ogawa, Asahi Glass Company)	164 **Integrating a Low Cure Dielectric Material into Panel and Wafer Level Manufacturing Process** Markus Woehrmann, Fraunhofer IZM - Department WLSI	116 **Mixed-Mode Hybrid Parameters for High-Speed Differential Lines** A. Ege Engin, San Diego State University (Ivan Ndip, Klaus-Dieter Lang, Fraunhofer Institut IZM; Jerry Aguirre, Kyocera North America)	098 **Reversed Pulse Plating of Silver-Cobalt for Connector Applications** Nazila Dadvand, Texas Instruments Inc. (Mina Dadvand, Polytechnique de Montreal; Georges Kipouros, Dalhousie University)	082 **Synthesis, Characterization, and Processing of Novel Metallic Core-Shell Materials for Thick-Film Applications** Kyle Bandaccari, SVMT LLC
2:15 pm - 2:40 pm	003 **Reliability of an Electronic Product Fabricated of Mass-Produced Components** Ephraim Suhir, Portland State University	148 **A Numerical Study on Mitigation of Flying Dies in Compression Molding of Microelectronic Packages** Marc Dreissigacker, TU Berlin	142 **Integration of a K-Band Receiver Front-End Using a Copper Core Printed Circuit Board** Brian Curran, Fraunhofer IZM (Jacob Reyes, Christian Tschoban, Ivan Ndip, Klaus-Dieter Lang)	087 **X-Ray Advances in Support of Advanced Packaging - Today and Tomorrow** David Bernard, David Bernard Consultancy	185 **High Reliable and High Bonding Strength of Silver Sintered Joints on Copper Surfaces by Pressure Sintering Under Air Atmosphere** Ly May Chew, Heraeus Deutschland GmbH & Co. KG (Wolfgang Schmitt)
2:45 pm - 3:10 pm	133 **Warpage Behaviors of System-in-Packages on a Substrate Strip** Eric Ouyang, STATS ChipPAC Inc (Billy Ahn, SeonMo Gu, Yonghyuk Jeong, JaeMyong Kim; STATS ChipPAC Korea; Jim Hsu, Susan Lin, Goran Liu, Anthony Yang, CoreTech System (Moldex3D))	068 **Lithographic Evaluation of Thin Photoimageable Dielectric Dry Film for Advanced Panel Level Packaging Applications** Roger McCleary, Rudolph Technologies (Keith Best, Sudmun Habib, Rudolph Technologies; Ognian Dimov, Sanjay Malik, Fujifilm Electronic Materials, U.S.A.)	145 **A Reusable 3D Printed Cavity Resonator for Liquid Sample Characterization** Saranraj Karuppuswami, Michigan State University (Saikat Mondal, Mohd Ifwat Mohd Ghazali, Premjeet Chahal)	034 **The Low Dk and Df Photosensitive Insulation Material for Low Transmission Loss Packages** Shinichiro Abe, Hitachi Chemical Co. Ltd. (Kazuyuki Mitsukura, Yuki Imazu, Masaya Toba, Takashi Masuko, Kazuhiko Kurafuchi)	109 **Study on High Temperature Resistant Die Bonding Formed by Al/Ni Nano-particles Composite Paste** Yasunori Tanaka, Waseda University
3:15 pm - 3:40 pm			194 **Dielectric Constant**	169 **Ribbon Ceramic**	066 **Zinc Oxide Nanowire**

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			and Loss Tangent Characterization of Alumina Substrate Using Cavity Resonators Robert B. Paul, San Diego State University (A. Ege Engin, SDSU; Jerry Aguirre, Kyocera North America)	John Olenick ENrG Incorporated	Sensor Packaging Bruce Kim, City University of New York (Sang-Bock Cho, Ulsan University)

3:45 pm - 5:30 pm: Happy Hour in Exhibits

Exhibit Lunch Sponsor:

Heraeus

Panel Session Sponsor:

JCET

PASADENA CONVENTION CENTER
5:30 pm - 7:30 pm:

Panel Session & Reception on:
ELIMINATING THE AI CONFUSION -
IMPACT ON COMPUTING, COMMUNICATIONS, AND AUTOMOTIVE

Artificial Intelligence (AI) makes it possible for machines to learn from experience, adjust to new inputs and perform human-like tasks. The term â€œdeep learningâ€□ or a type of â€œmachine learningâ€□ refers to training a computer to perform human-like tasks, such as recognizing speech, identifying images or making predictions. Instead of organizing data to run through predefined equations, deep learning establishes basic parameters about the data and trains the computer to learn on its own by recognizing patterns using many layers of processing. AI or deep learning is expected to be applied to a wide range of applications, including connectivity or Internet of Things (IoT), big data processing and servers, cloud services, autonomous driving, 5G communications, smart factory or Industry 4.0, robotics, AR/VR, cryptocurrency mining, and blockchain.

This panel discussion focuses on the impact of AI on computing, communications, and automotive. The experts on the panel will comment on their understanding of the application of AI and the impact on packaging and assembly. Package choice, design, and materials impact and the importance of co-design will be discussed. A set of experts will address these issues and others in a dynamic discussion setting.

***MODERATOR**:*
Jan Vardaman, President and Founder of TechSearch International, Inc.

***PANELISTS**:*
Ivor Barber - AMD
Rama Divakaruni - IBM
Ron Huemoeller - Amkor Technology
David McCann - GLOBALFOUNDRIES
Raj Pendse - Facebook
Urmi Ray - JCET Group
Rich Rice - ASE

Includes Beer, Wine and Appetizers

THURSDAY, OCTOBER 11, 2018

7:00 AM - 3:00 PM: Registration Open
NO EXHIBITS - Exhibitor Move-Out

IMAPS 2018 Plenary Session:
PASADENA CONVENTION CENTER

8:00 AM - 8:15 AM: Day 3 Opening Comments & Intro of Keynote
Mark Gerber, 2018 General Chair; Curtis Zwenger, General Chair-Elect (2019)

Keynote Session sponsored by:

8:15 AM - 9:00 AM: Keynote Presentation 4

AI Hardware: Packaging to the Core!

AI workloads are strongly driving systems to become much more architecturally diverse. Today's accelerators are composed of a mix of heterogeneous components including CPUs, GPUs, specialized accelerators, and memories. Advanced packaging techniques to enable high inter-connectivity among these components will be crucial for continued progress in AI as this is the key bottleneck for AI Applications. As scaling continues to slow, value at the system level for today's workloads is achieved more by a diversity of parts, connectivity and bandwidth rather than sheer compute power in a monolithically integrated SoC.

Continued increases in compute performance for modern unstructured data will drive technologies for higher bandwidth including but not limited to 3D stacking. While research has explored advanced cooling techniques -- which are viable in a modern data center -- a plethora of form factors which will evolve for different AI workloads and is expected to color the landscape. With the advent of analog-based accelerators --also currently in a research phase - it becomes clear to envision a future where a variety of heterogeneously enabled form factors driving different workloads for inference and training are pervasive in the edge and in the Cloud.

Thus, AI hardware will be truly packaging to the core!



Rama Divakaruni, IBM
IBM Distinguished Engineer

Rama Divakaruni received his B.Tech in Electrical Engineering from the Indian Institute of Technology, Madras, India in 1988. He received his Ph.D in Electrical Engineering from the University of California, Los Angeles in 1994. Since 1994, he has been working on advanced semiconductor technologies at IBM. From 1994 through 2003, he worked on DRAM Technology Development and his team introduced the world's first sub-8F2 vertical transistor DRAM trench technology. From 2004 through 2008 he worked on various strained silicon technologies in both SOI and bulk Si semiconductors. These technologies were the basis of the Nintento Wii, XBOX360 and the PlayStation3 game platforms and at 45nm were introduced into the modern mobile semiconductor fabric. From 2008 through 2013, Dr. Divakaruni worked on IBM's unique Hi-K technologies and FINFET technologies. Much of this work culminated with the introduction of mobile technologies by IBM's partners and IBM's SUMMIT Supercomputer earlier this year using 14nm SOI FINFET technology.

Dr. Divakaruni is currently an IBM Distinguished Engineer and is reponsible for IBM Advanced Process Technology Research. His current focus is on AI Hardware technologies for Deep Learning. He is one of IBMs top inventors with over 225+ issued US patents.

THURSDAY MORNING PROGRAM

	SiP/SiM (Systems Solutions) *Track Chairs:* ***Urmi Ray, JCET Group; Rich Rice, ASE Group***	**Wafer Level/Panel Level (Advanced RDL)** *Track Chairs:* ***John Hunt, ASE Group; Rajiv Dunne, Qualcomm***	**High Performance-High Reliability** *Track Chairs:* ***Erica Folk, Northrop Grumman; Ivan Ndip, Fraunhofer IZM***	**Flip Chip/ 2.5D/3D/Optical (Advanced Package)** *Track Chairs:* ***Karl Friedrich Becker, Fraunhofer-IZM; Sandeep Sane, Intel***	**Advanced Process & Materials (Enabling Technologies)** *Track Chairs:* ***Habib Hichri, SUSS Microtec; Benson Chan, Binghamton Univ.***
	Session THA1 AUTOMOTIVE Session Chairs: Mark Hoffmeyer, IBM; Rich Rice, ASE Group	**Session THA2 WLCSP / WAFER-LEVEL FAN OUT** Session Chairs: Farhad Kiaei, HD MicroSystems; Mak Kulkarni, Texas Instruments	**Session THA3 HIGH RELIABILITY IN BIOMEDICAL** Session Chairs: Tim LeClair; Cerapax; Julia Brueckner, Quantum Analytics	**Session THA4 BUMP/ INTERCONNECT** Session Chairs: Adeel Bajwa, UCLA; Karl Friedrich Becker, Fraunhofer-IZM	**Session THA5 ADVANCED WIREBOND** Session Chairs: Martin Schneider-Ramelow, Fraunhofer IZM; Michael McKeown, Hesse Mechatronics
9:10 am 9:35 am	060 **Advanced Packaging for Automotive Dashboard Application** Nokibul Islam, JCET Group (HC Choi)	039 **Photosensitive Polyimide having Low Loss Tangent for RF Application** Masao Tomikawa, Toray Industries (Hitoshi Araki, Yohei Kiuchi, Akira Shimada)	112 **When Failure is Not an Option - Packaging Materials and Technologies for the Reliable Protection of Medical Electronics** Thomas Zetterer, SCHOTT AG (J. Herzberg, J. Baehr, K. Waxman, Jochen Herzberg)	107 **Fine Pitch Paste for System-in-Package Applications** Zhang Ruifen, Heraeus Materials Singapore Pte Ltd (Sarangapani Murali, Vinobaji Sureshkumar, Teo Lingling, Loke Chee Keong, Chan Li-San)	105 **Ultra-Fine Pitch Wedge bonding for Device Reliability Characterization** Lacey Badger, Intel Corporation
9:40 am 10:05 am	023 **Batch Microwave Plasma Cleaning for Robustification of Automotive Devices: an Alternative to**	137 **Novel Low Temperature Curable Photo-patternable Polyamide with High Planarity for Wafer**	162 **Sequence-Specific Nucleic Acid Detection at 1 aM; Microfluidics Device** Harold G. Monbouquette,	012 **Elevated Stand-Off Heights in Solder Joint Interconnections of Surface Mounted IC Packages Result in**	108 **Process Development of Al-alloy Wire Bonding for High-Temperature Power Electronics**

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	Strip-type Radiofrequency Plasma Ghizelle Jane E. Abarro, ON Semiconductor Philippines Inc. (Rod Delos Santos Jr., Alvin Denoyo, Manny Ramos)	**Level Fan-Out Packaging (WLFO)** Daniel Nawrocki, MicroChem Corp / Nippon Kayaku (Andrew Cooper, Takanori Koizumi, Shinya Inagaki, Naoki Kawamoto, Nao Honda, Kristina Markt, Milton Bernal)	University of California, Los Angeles	**Appreciable Stress and Warpage Relief** Ephraim Suhir, Portland State University (Sung Yi, Portland State University; Jennie Hwang, H-Technologies Group; R. Ghaffarian, Jet Propulsion Laboratory, California Institute of Technology)	Omid Niayesh, Kulicke & Soffa Industries, Inc. (Tao Xu, Xuan Che, Jason Fu, Omid Niayesh)
Coffee Break in Foyer: 10:05 am - 10:20 am Coffee Break Sponsor: Oneida Research Services & Silicon Cert Labs					
10:20 am - 10:45 am	033 **A New Photosensitive Dielectric Material for High-Density RDL with Ultra-Small Photo-Vias and High Reliability** Daichi Okamoto, TAIYO INK MFG. CO. (Yoko Shibasaki, Daisuke Shibata, Tadahiko Hanada)	103 **Study of Sub-micron Fan-out Wafer Level Packaging Solutions** Yoshio Goto, Canon (Kosuke Urushihara, Bunsuke Takeshita, Ken-Ichiro Mori)	170 **Glass Encapsulation for Wireless Highly Miniaturized Implantable Devices** Jim Ohneck, GlencaTec AG	070 **Fatigue Cycling of Electrical Interconnects Dispensed on Flexible Substrate** Mohammed Alhendi, Binghamton University (J.P. Lombardi III, G. S. Khinda, M.Z. Kokash, D. L. Weerawarne, P. Borgesen, M. D. Poliks)	113 **Intelligent Production of Wire Bonds using Multi-Objective Optimization â€“ Insights, Opportunities and Challenges** Michael McKeown, Hesse Mechatronics (Andreas Unger, Matthias Hunstig, Michael BrÃ¶kelmann, Hesse GmbH; Tobias Meyer, Fraunhofer IWES; Walter Sextro, Paderborn University)
10:50 am - 11:15 am	079 **Inspection and Metrology of Wet Print** Sebastian Stenger, EPP Germany	092 **Implementation of a Temperature Ramp Rate Requirement and Impact on the Packaging Processes** Randy Hamm, Honeywell KCP (Daren Withlock, Elizabeth Brown, Ryan Eatinger, Honeywell KCP; Jeremy Stearns, Samuel Ringwood, Sandia National Laboratories)	100 **Flexible PET Substrate for Higher Definition Printing of Polymer Thick Film Conductive Pastes** Art Dubie, Ikonics/Chromaline	165 **Analysis of Ultrasonic Welding of Mechanically Coupled Small Area Contacts for a Silicon Carbide Power Module** Kuldeep Saxena, CREE (Aryn Hays, Ivan Kao, Zach Cole)	106 **Growth of Intermetallics at Coated Silver Wire Bond Interfaces** Sarangapani Murali, Heraeus Materials Singapore Pte Ltd (Wong Chin Yeung)
11:20 am - 11:45 am	154 **Highly Reliable Solderless Contact with Press-fit Technology for Power Modules** Minoru Egusa, Mitsubishi Electric Corporation (Hidetoshi Ishibashi, Yoshitaka Otsubo, Masao Kikuchi, Mitsubishi Electric Corporation; Yoshihiro Kashiba, Osaka University)	192 **Novel Low Temperature Curable Photosensitive Negative-tone PI with Higher Resolution and Reliability** Daisaku Matsukawa, Hitachi Chemical DuPont MicroSystems, Ltd. (Hiroko Yotsuyanagi, Shiori Sakakibara, Noriyuki Yamazaki, Tetsuya Enomoto, Takeharu Motobe)	NEW PRESENTATION: Hermiticity for High-reliability Applications Antti Peltonen, SCHOTT Primoceler OY	187 **Characterization of Fine Pitch Interconnections (<=10µm) on Silicon Interconnect Fabric for Heterogeneous Integration** SivaChandra Jangam, University of California, Los Angeles (Adeel Bajwa, Kannan K. Thankappan, Premsagar Kittur, Subramanian Iyer)	168 **Wire Bonding Advances for Multi-Chip and System in Package Devices** Hui Xu, Kulicke and Soffa Industries, Inc. (Aashish Shah, Basil Milton, Ivy Qin)

11:45 am - 1:15 pm:
POSTERS & PIZZA (in Foyer)
Session Chairs: Erica Folk, Northrop Grumman; Andre Rouzaud, CEA Leti; Gabriel Pares, CEA Leti

(POSTER SETUP FROM 10:30 AM UNTIL 11:40 AM)

Posters & Pizza Sponsored by:

021
Comparisons of Soldering Alloys in Large Ceramic Substrate to Metal Heatsink Attachment Application
Frank Fan Wang, Crane Aerospace & Electronics

011
A New Method for Non-Destructive Characterization of Through Holes in Printed Circuit Boards
Sarah Czaplewski, IBM (Joe Doman, Joe Kuczynski)

056
Microstrucuture and Mechanical Properties of Pressureless Sintered Silver Die-attach Materials
Masafumi Takesue, Bando Chemical Industries (Tomofumi Watanabe, Keisuke Tanaka)

069
Investigation Towards the Optimum of Power Capability, Ageing Stability and Costs Effectiveness on Thick Film Resistor Pastes for AlN Ceramics
Richard Schmidt, Fraunhofer Institute for Ceramic Technologies and Systems (Manja Marcinkowski, Claudia Feller, Uwe Partsch)

081
Thermal Shrinkage Management of Silver Core-shell Conductive Layers with AG and LS LTCC Architectures

176
Development of High Temperature Tantalum Polymer Capacitors
Antony P. Chacko, KEMET Electronics Corporation (James Chen, Chris Stolarski, Cristina MotaCaetano, Philip Lessner)

181
Development of skills and tools for micro opto-electrical integration on wafer level
Saskia SchrÃ¶der, Fraunhofer Institute for Silicon Technology (Vanessa Stenchly, Hans-Joachim Quenzer, Wolfgang Reinert)

188
A Network for Silicon Interconnect Fabric
Boris Vaisband, University of California, Los Angeles (Adeel Bajwa, Subramanian Iyer)

189
Dynamically Controlled Flow Loop to Benchmark Rapid Transient Cooling Utilizing Flash Boiling for High Heat Flux Electronic Systems
Ujash Shah, University of California, Los Angeles (Chen Ling, Timothy Fisher)

190
Integrated Sensor Nodes for Industry 4.0 Applications
P. Fruehauf, Fraunhofer IZM (M. Heimann, S. Nerreter, R. Blank, S.

Richard Stephenson, SVMT LLC

128
Aqueous Washable Thermal Resistant Coatings and Adhesives
John Moore, Daetec LLC

130
High Performance Etchable RoHS Compliant Thick Film Gold Conductor
Samson Shahbazi, Heraeus Precious Metals (Stephanie Edwards, Ryan Persons, Caitlin Shahbazi)

140
Novel Formaldehyde-free Electroless Copper for Plating on Next Generation Substrates
Christian Wendeln, Atotech Deutschland GmbH (Edith SteinhÃ¤user, Lutz Stamp, Bexy Dosse-Gomez, Elisa Langhammer, Sebastian Reiber, SebastiÃ¡n DÃ¼rrnebeil, Sandra RÃ¶seler)

161
Low-temperature Sintering IMC-nano-solder for High Temperature Interconnect
Ying Zhong, University of California at San Diego

146
Investigation of a Proactive Glass Filler Removal in IC Substrate Build up Films and its Effect on Topography and Copper Adhesion Reliability
Stefan Kempa, Atotech Deutschland GmbH (Wolfgang Friz, Florian Gaul, Ellen Habig, Laurence J. Gregoriades)

078
Development of a Mechanical Cycling Reliability Test Program for Evaluating Thermal Interface Materials for Semiconductor Test and Burn-in Requirements
David Saums, DS&A LLC (Tim Jensen, Carol Gowans, Seth Homer, Ron Hunadi, Indium Corporation)

173
Optimization of Cupric Chloride Subtractive Etching for Cu High Density Interconnects
Oliver Chyan, University of North Texas (Alexander Lambert, Goutham Issac, Ashish Salunke, Luwen Lu, University of North Texas; Oscar Ojeda, Jeremy Ecton, Arnab Roy, Hsin-Wei Wang, Leonel Arana, Intel)

183
Explore High Bonding Reliability of Cu Wire Bonded Devices under Extreme Halide Contaminated Environments
Oliver Chyan, University of North Texas (M. Asokan, J. Caperton, A. Salunke, University of North Texas, Interfacial Electrochemistry and Materials Research Lab; Fei Xu, Changzhou Ruize Microelectronics Co., Ltd.)

Gottwald, A. Hofmeister, M. Schmied, D. SchÃ¼tze, B. SchrÃ¶der, S. Voges, K.-F. Becker, M. Kreitmeier, W. Neifer)

191
Application of Portable Nanogenerator Using Friction Charging
Dongseob Kim, KITECH (Banseok Kim, Jihoon Chung, Haksung Moon, Sangmin Lee, Chung-Ang University)

ALSO IN SESSION WA1
172
High Frequency Base Materials: Laser-Material Interaction for HDI/ICP Applications
Christopher Ryder, ESI

ALSO IN SESSION TP5
009
Shear Strength and Thermo-mechanical Reliability of Sintered Ag Joints Containing low CTE Non-metal Additives for Die Attach
Guangyu Fan, Indium Corporation (Christine Labarbera, Ning-Cheng Lee, Indium Corporation; Colin Clark, Rochester Institute of Technology)

THURSDAY AFTERNOON PROGRAM

	SiP/SiM (Systems Solutions) *Track Chairs:* ***Urmi Ray, JCET Group; Rich Rice, ASE Group***	**Wafer Level/Panel Level (Advanced RDL)** *Track Chairs:* ***John Hunt, ASE Group; Rajiv Dunne, Qualcomm***	**High Performance-High Reliability** *Track Chairs:* ***Erica Folk, Northrop Grumman; Ivan Ndip, Fraunhofer IZM***	**Flip Chip/ 2.5D/3D/Optical (Advanced Package)** *Track Chairs:* ***Karl Friedrich Becker, Fraunhofer-IZM; Sandeep Sane, Intel***	**Advanced Process & Materials (Enabling Technologies)** *Track Chairs:* ***Habib Hichri, SUSS Microtec; Benson Chan, Binghamton Univ.***
	Session THP1 WEARABLE / TEST Session Chairs: Urmi Ray, JCET Group; Curtis Zwenger, Amkor Technology	**Session THP2 MEMS & SENSORS** Session Chairs: Gabriel Pares, CEA-LETI; Marco Del Sarto, ST Microelectronics	**Session THP3 HIGH RELIABILITY IN DEFENSE and AEROSPACE** Session Chairs: Erica Folk, Northrop Grumman; Daniel Fisher	**Session THP4 3D & ENABLING TECHNOLOGIES** Session Chairs: Nokibul Islam, JCET Group;	**Session THP5 ADVANCED EQUIPMENT /ADDITIVE MANUFACTURING** Session Chairs: Doug Shelton, Canon USA; Douglas Hopkins, NC State University
1:15 pm - 1:40 pm	**Latest Packaging Developments in Wearable Electronics** Jan Vardaman, TechSearch International, Inc.	160 **Scalable Hybrid Microelectronic-Microfluidic Integration of Highly Sensitive Biosensors for Point of Care Applications** Karl-Friedrich Becker, Fraunhofer IZM (Patrick Reinecke, Tanja Braun, Martin Schneider-Ramelow, Klaus-Dieter Lang, Technical University of Berlin; Marie-Theres Putze, Leopold Georgi, Ruben Kahle, Fraunhofer IZM; David Kaiser, Daniel HÃ¼ger, Andrey Turchanin, Friedrich Schiller University; Pavel Livshits, Jens WeidenmÃ¼ller, Fraunhofer IMS; Thomas Weimann, Physikalisch-Technische Bundesanstalt)	018 **The Impact of PWB Glass Style and Orientation on the Reliability of SMT Components** Maxim Serebreni, DfR Solutions (Greg Caswell)	053 **3D Integration: 300mm MOCVD Copper Seed Layer Deposition for High Aspect Ratios TSV** Sabrina Fadloun, SPTS Technologies	047 **Productivity Comparison of Wafer Transport Architectures in PVD Tools Used for Fan-Out Packaging RDL Barrier/Seed Formation** Paul Werbaneth, Intevac, Inc. (Terry Bluck, Chris Smith)
1:45 pm - 2:10 pm	008 **Smart and Connected Bioelectronics for Persistent Human-Machine Interfaces** Woon-Hong Yeo, Georgia Institute of Technology (Yun-Soung Kim)	132 **Glass Packaging for RF MEMS** Raj Parmar, Corning Inc. (Aric Shorey, Jay Zhang, Corning Inc.; Chris Keimel, Menlo Microsystems)	065 **Reliability & Characterization of Wide Band Gap Power Modules using POL-kW Packaging Technology** Christopher Kapusta, General Electric	149 **Electrical Characterization of Low Temperature PECVD Oxides for TSV Applications** Piotr Mackowiak, Fraunhofer IZM (Rachid Abdallah, Martin Wilke,	075 **Ultra-Wideband High Gain Vivaldi Antennas Using Additive Manufacturing** Mohd Ifwat Mohd Ghazali, Michigan State University (Premjeet Chahal)

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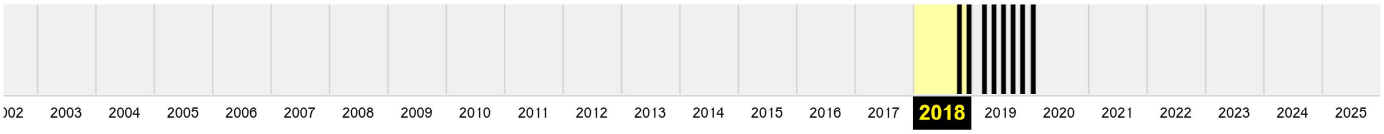
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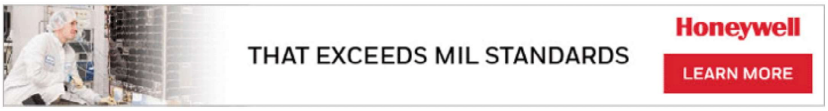
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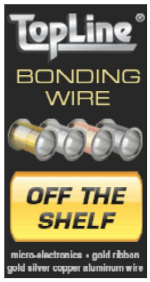
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System Co-Design Modeling Methodology of a High Speed (25Gbps) Multi-Rate 4-Channel Retimer: Simulation to Measurement Correlation

Keywords: FC Packaging, Modeling, Simulation, Co-Design, Measurement and Simulation Correlation

Goal/Objective. In this paper we detail the system (viz. silicon-package-pcb) electrical co-design of a 130nm BiCMOS high-speed (25Gbps) 4-channel multi-rate retimer, packaged in a small 6-mm x 6-mm FC BGA package, with integrated advanced signal conditioning circuitries. Electrical optimization of the silicon-package-pcb over the high speed channels, to achieve desired performance, was achieved through a coupled circuit-to-electromagnetic co- design modeling and simulation methodology. Key figure of merits for system performance (viz. insertion loss, return loss, crosstalk/isolation, jitter, power supply inductance and resistance parasitics, among others) are modeled and characterized via simulation and measurements. Laboratory measurements, on a real SoC, are presented that validate the integrity of the modeling and simulation approach. Good correlation between modeling methodology and laboratory measurements is achieved. The Modeling Methodology. Operating parameters, cost, and package design considerations will impact high-speed channel performance. Consequently, ensuring that the packaged SoC meets specification is essential in high speed data communications. Across various implementations of high speed retimer, there are standard electrical performance metrics/figure of merits (FOMs) that are employed to characterize system design performance. Of particular importance to the package performance, are time- domain and frequency domain parameters. For time-domain, these include the inductance/resistance (RL) parasitics of the supply/ground network and jitter (both deterministic and random) which impact the power integrity of the device. The frequency domain parameters (viz. insertion loss, return loss, crosstalk, and isolation) impact the signal integrity performance of the device. To assess the signal and power integrity electrical performance of the package for both high-speed, an iterative coupled circuit-to- electromagnetic methodology was developed. The methodology/flow has primarily 4 steps – namely [1] initial package physical design, [2] 3D time- domain quasi-static electromagnetic parasitics extraction model (RLGC) and 3D full-wave frequency-domain model extraction (s-parameters), [3] coupled silicon spice-level netlist circuit-to-electromagnetic system- level analysis, and [4] a check step where the FOMs requirements are compared to modeling results. If the requirements are met, the flow exits. If not, the flow iteratively proceeds back to the physical design until requirements are met. The accuracy of the electromagnetic solvers employed for the extraction of the package and PCB models have been validated on previous designs [1-3]. The flow described here was also employed to assess PCB performance. Additionally, a more accurate approach for the high speed links - is to merge the physical design of the package onto the physical design of the PCB and perform the extraction in one step. This is more accurate than extracting the model of the package and PCB separately and then concatenate them in the system-level circuit for transient analysis. This improved technique was demonstrated in [4] for a 12.5Gbps high speed link and has been employed for the analysis and correlation study here. Device/System Description, Measurement Set-up, and Results: The system-level co-design modeling methodology discussed above was implemented on TI DS250DF410, a 25Gbps multi-rate 4-channel retimer. The DS250DF410 is a four-channel multi- rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive. Each channel includes an independent voltage- controlled oscillator (VCO) and phase- locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter. Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410. To characterize/verify the high- frequency channel integrity and transmit jitter performance of the DS250DF410, an electronic verification module, i.e. a PCB system was designed and built. This EVM allows for easy evaluation of the 25 Gbps retimer DS250DF410. The high-frequency measurements (viz. insertion and return loss) set-up includes driving the high speed channels on the EVM with a PNA Series Network Analyzer & S-Parameter Test Set. The signal generator module is used to transmit (TX) the signals through the channel on the EVM and loop back out of the EVM to the RX signal analyzer module. This set-up provides for a complete channel characterization. The TX jitter was characterized using pattern generator, waveform analyzer, and high-end sampling scope. All measurements were done over wide frequency range and temperature. Good correlations are observed between modeling and measurements for high- frequency channel integrity and jitter.

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Texas Instruments, Inc
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United States

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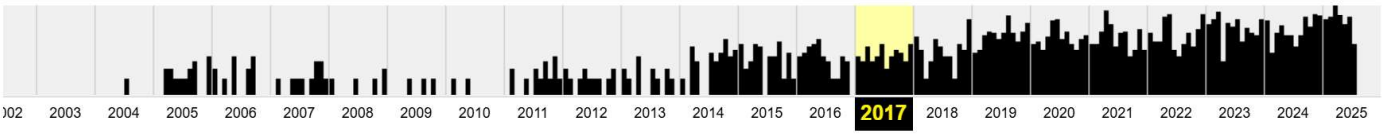
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PCI Express

From Wikipedia, the free encyclopedia

Not to be confused with PCI-X.
For Engineering, Procurement, Construction and Installation (EPCI), see EPCI.

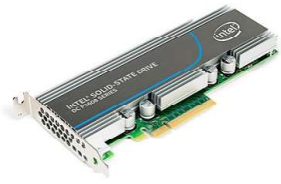
PCI Express (**Peripheral Component Interconnect Express**), officially abbreviated as **PCIe** or **PCI-e**,[1] is a high-speed serial computer expansion bus standard, designed to replace the older PCI, PCI-X, and AGP bus standards. PCIe has numerous improvements over the older standards, including higher maximum system bus throughput, lower I/O pin count and smaller physical footprint, better performance scaling for bus devices, a more detailed error detection and reporting mechanism (Advanced Error Reporting, AER[2]), and native hot-plug functionality. More recent revisions of the PCIe standard provide hardware support for I/O virtualization.

The PCI Express electrical interface is also used in a variety of other standards, most notably in ExpressCard as a laptop expansion card interface, and in SATA Express as a computer storage interface.

Format specifications are maintained and developed by the PCI-SIG (PCI Special Interest Group), a group of more than 900 companies that also maintain the conventional PCI specifications. PCIe 3.0 is the latest standard for expansion cards that are in production and available on mainstream personal computers.[3][4]

PCI Express

Year created	2004; 13 years ago
Created by	Intel · Dell · HP · IBM
Supersedes	AGP · PCI · PCI-X
Width in bits	1–32
No. of devices	One device each on each endpoint of each connection. PCI Express switches can create multiple endpoints out of one endpoint to allow sharing one endpoint with multiple devices.
Speed	For single-lane (×1) and 16-lane (×16) links, in each direction: **v. 1.x** (2.5 GT/s): 250 MB/s (×1) 4 GB/s (×16) **v. 2.x** (5 GT/s): 500 MB/s (×1) 8 GB/s (×16) **v. 3.x** (8 GT/s): 985 MB/s (×1) 15.75 GB/s (×16) **v. 4.0** (16 GT/s): 1.969 GB/s (×1) 31.51 GB/s (×16)
Style	Serial
Hotplugging interface	Yes, if ExpressCard, Mobile PCI Express Module, XQD card or Thunderbolt
External interface	Yes, with PCI Express External Cabling, such as Thunderbolt



Intel P3608 NVMe flash SSD, PCI-E add-in card

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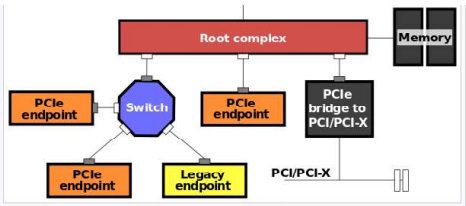
Architecture [edit]

Conceptually, the PCI Express bus is a high-speed serial replacement of the older PCI/PCI-X bus.[6] One of the key differences between the PCI Express bus and the older PCI is the bus topology; PCI uses a shared parallel bus architecture, in which the PCI host and all devices share a common set of



Marvell Semiconductor, Inc. - Ex. 1018, Page 000144

address, data and control lines. In contrast, PCI Express is based on point-to-point topology, with separate serial links connecting every device to the root complex (host). Due to its shared bus topology, access to the older PCI bus is arbitrated (in the case of multiple masters), and limited to one master at a time, in a single direction. Furthermore, the older PCI clocking scheme limits the bus clock to the slowest peripheral on the bus (regardless of the devices involved in the bus transaction). In contrast, a PCI Express bus link supports full-duplex communication between any two endpoints, with no inherent limitation on concurrent access across multiple endpoints.



An example of the PCI Express topology; white "junction boxes" represent PCI Express device downstream ports, while the gray ones represent upstream ports.[5]:7

In terms of bus protocol, PCI Express communication is encapsulated in packets. The work of packetizing and de-packetizing data and status-message traffic is handled by the transaction layer of the PCI Express port (described later). Radical differences in electrical signaling and bus protocol require the use of a different mechanical form factor and expansion connectors (and thus, new motherboards and new adapter boards); PCI slots and PCI Express slots are not interchangeable. At the software level, PCI Express preserves backward compatibility with PCI; legacy PCI system software can detect and configure newer PCI Express devices without explicit support for the PCI Express standard, though new PCI Express features are inaccessible.

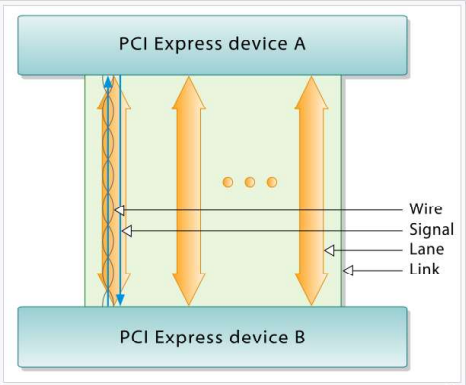

A PCI Express ×1 card containing a PCI Express switch (covered by a small heat sink), which creates multiple endpoints out of one endpoint and allows it to be shared by multiple devices

The PCI Express link between two devices can consist of anywhere from one to 32 lanes. In a multi-lane link, the packet data is striped across lanes, and peak data throughput scales with the overall link width. The lane count is automatically negotiated during device initialization, and can be restricted by either endpoint. For example, a single-lane PCI Express (×1) card can be inserted into a multi-lane slot (×4, ×8, etc.), and the initialization cycle auto-negotiates the highest mutually supported lane count. The link can dynamically down-configure itself to use fewer lanes, providing a failure tolerance in case bad or unreliable lanes are present. The PCI Express standard defines slots and connectors for multiple widths: ×1, ×4, ×8, ×12, ×16 and ×32.[5]:4,5 This allows the PCI Express bus to serve both cost-sensitive applications where high throughput is not needed, as well as performance-critical applications such as 3D graphics, networking (10 Gigabit Ethernet or multiport Gigabit Ethernet), and enterprise storage (SAS or Fibre Channel).

As a point of reference, a PCI-X (133 MHz 64-bit) device and a PCI Express 1.0 device using four lanes (×4) have roughly the same peak single-direction transfer rate of 1064 MB/s. The PCI Express bus has the potential to perform better than the PCI-X bus in cases where multiple devices are transferring data simultaneously, or if communication with the PCI Express peripheral is bidirectional.

Interconnect [edit]

PCI Express devices communicate via a logical connection called an *interconnect*[7] or *link*. A link is a point-to-point communication channel between two PCI Express ports allowing both of them to send and receive ordinary PCI requests (configuration, I/O or memory read/write) and interrupts (INTx, MSI or MSI-X). At the physical level, a link is composed of one or more *lanes*.[7] Low-speed peripherals (such as an 802.11 Wi-Fi card) use a single-lane (×1) link, while a graphics adapter typically uses a much wider and faster 16-lane link.



A PCI Express link between two devices consists of one or more lanes, which are dual simplex channels using two differential signaling pairs.[5]:3

Lane [edit]

A lane is composed of two differential signaling pairs, with one pair for receiving data and the other for transmitting. Thus, each lane is composed of four wires or signal traces. Conceptually, each lane is used as a full-duplex byte stream, transporting data packets in eight-bit "byte" format simultaneously in both directions between endpoints of a link.[8] Physical PCI Express links may contain from one to 32 lanes, more precisely 1, 2, 4, 8, 12, 16 or 32 lanes.[5]:4,5[7] Lane counts are written with an "×" prefix (for example, "×8" represents an eight-lane card or slot), with ×16 being the largest size in common use.[9]

Serial bus [edit]

The bonded serial bus architecture was chosen over the traditional parallel bus due to inherent limitations of the latter, including half-duplex operation, excess signal count, and inherently lower bandwidth due to timing skew. Timing skew results from separate electrical signals within a parallel interface traveling through conductors of different lengths, on potentially different printed circuit board (PCB) layers, and at possibly different signal velocities. Despite being transmitted simultaneously as a single word, signals on a parallel interface have different travel duration and arrive at their destinations at different times. When the interface clock period is shorter than the largest time difference between signal arrivals, recovery of the transmitted word is no longer possible. Since timing skew over a parallel bus can amount to a few nanoseconds, the resulting bandwidth limitation is in the range of hundreds of megahertz.

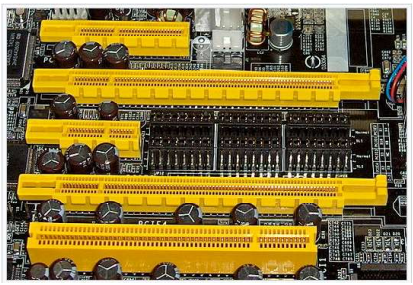
A serial interface does not exhibit timing skew because there is only one differential signal in each direction within each lane, and there is no external clock signal since clocking information is embedded within the serial signal itself. As such, typical bandwidth limitations on serial signals are in the multi-gigahertz range. PCI Express is one example of the general trend toward replacing parallel buses with serial interconnects; other examples include Serial ATA (SATA), USB, Serial Attached SCSI (SAS), FireWire (IEEE 1394), and RapidIO. In digital video, examples in common use are DVI, HDMI and DisplayPort.

Multichannel serial design increases flexibility with its ability to allocate fewer lanes for slower devices.

Form factors [edit]

PCI Express (standard) [edit]

A PCI Express card fits into a slot of its physical size or larger (with ×16 as the largest used), but may not fit into a smaller PCI Express slot; for example, a ×16 card may not fit into a ×4 or ×8 slot. Some slots use open-ended sockets to permit physically longer cards and negotiate the best available electrical and logical connection.

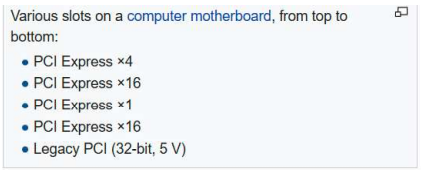


The number of lanes actually connected to a slot may also be fewer than the number supported by the physical slot size. An example is a ×16 slot that runs at ×4, which will accept any ×1, ×2, ×4, ×8 or ×16 card, but provides only four lanes. Its specification may read as "×16 (×4 mode)", while "×size @ ×speed" notation ("×16 @ ×4") is also common. The advantage is that such slots can accommodate a larger range of PCI Express cards without requiring motherboard hardware to support the full transfer rate.

The cards themselves are designed and manufactured in various sizes. For example, solid-state drives

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(SSDs) that come in the form of PCI Express cards often use HHHL (half height, half length) and FHHL (full height, half length) to describe the physical dimensions of the card.[10][11]



Various slots on a computer motherboard, from top to bottom:

- PCI Express ×4
- PCI Express ×16
- PCI Express ×1
- PCI Express ×16
- Legacy PCI (32-bit, 5 V)

Pinout [edit]

The following table identifies the conductors on each side of the edge connector on a PCI Express card. The solder side of the printed circuit board (PCB) is the A side, and the component side is the B side.[12] PRSNT1# and PRSNT2# pins must be slightly shorter than the rest, to ensure that a hot-plugged card is fully inserted. The WAKE# pin uses full voltage to wake the computer, but must be pulled high from the standby power to indicate that the card is wake capable.[13]

PCI Express connector pinout (×1, ×4, ×8 and ×16 variants)

Pin	Side B	Side A	Description
1	+12 V	PRSNT1#	Must connect to farthest PRSNT2# pin
2	+12 V	+12 V	Main power pins
3	+12 V	+12 V	
4	Ground	Ground	
5	SMCLK	TCK	SMBus and JTAG port pins
6	SMDAT	TDI	
7	Ground	TDO	
8	+3.3 V	TMS	
9	TRST#	+3.3 V	
10	+3.3 V aux	+3.3 V	Standby power
11	WAKE#	PERST#	Link reactivation; fundamental reset
Key notch			
12	CLKREQ#	Ground	Request running clock
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK−	Lane 0 transmit data, + and −
15	HSOn(0)	Ground	
16	Ground	HSIp(0)	Lane 0 receive data, + and −
17	PRSNT2#	HSIn(0)	
18	Ground	Ground	
PCI Express ×1 cards end at pin 18			
19	HSOp(1)	Reserved	Lane 1 transmit data, + and −
20	HSOn(1)	Ground	
21	Ground	HSIp(1)	Lane 1 receive data, + and −
22	Ground	HSIn(1)	
23	HSOp(2)	Ground	Lane 2 transmit data, + and −
24	HSOn(2)	Ground	
25	Ground	HSIp(2)	Lane 2 receive data, + and −
26	Ground	HSIn(2)	
27	HSOp(3)	Ground	Lane 3 transmit data, + and −
28	HSOn(3)	Ground	
29	Ground	HSIp(3)	Lane 3 receive data, + and −
30	Reserved	HSIn(3)	
31	PRSNT2#	Ground	
32	Ground	Reserved	
PCI Express ×4 cards end at pin 32			
33	HSOp(4)	Reserved	Lane 4 transmit data, + and −
34	HSOn(4)	Ground	
35	Ground	HSIp(4)	Lane 4 receive data, + and −
36	Ground	HSIn(4)	
37	HSOp(5)	Ground	Lane 5 transmit data, + and −
38	HSOn(5)	Ground	
39	Ground	HSIp(5)	Lane 5 receive data, + and −
40	Ground	HSIn(5)	
41	HSOp(6)	Ground	Lane 6 transmit data, + and −
42	HSOn(6)	Ground	
43	Ground	HSIp(6)	Lane 6 receive data, + and −
44	Ground	HSIn(6)	
45	HSOp(7)	Ground	Lane 7 transmit data, + and −
46	HSOn(7)	Ground	

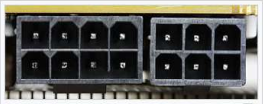
Pin	Side B	Side A	Description
50	HSOp(8)	Reserved	Lane 8 transmit data, + and −
51	HSOn(8)	Ground	
52	Ground	HSIp(8)	Lane 8 receive data, + and −
53	Ground	HSIn(8)	
54	HSOp(9)	Ground	Lane 9 transmit data, + and −
55	HSOn(9)	Ground	
56	Ground	HSIp(9)	Lane 9 receive data, + and −
57	Ground	HSIn(9)	
58	HSOp(10)	Ground	Lane 10 transmit data, + and −
59	HSOn(10)	Ground	
60	Ground	HSIp(10)	Lane 10 receive data, + and −
61	Ground	HSIn(10)	
62	HSOp(11)	Ground	Lane 11 transmit data, + and −
63	HSOn(11)	Ground	
64	Ground	HSIp(11)	Lane 11 receive data, + and −
65	Ground	HSIn(11)	
66	HSOp(12)	Ground	Lane 12 transmit data, + and −
67	HSOn(12)	Ground	
68	Ground	HSIp(12)	Lane 12 receive data, + and −
69	Ground	HSIn(12)	
70	HSOp(13)	Ground	Lane 13 transmit data, + and −
71	HSOn(13)	Ground	
72	Ground	HSIp(13)	Lane 13 receive data, + and −
73	Ground	HSIn(13)	
74	HSOp(14)	Ground	Lane 14 transmit data, + and −
75	HSOn(14)	Ground	
76	Ground	HSIp(14)	Lane 14 receive data, + and −
77	Ground	HSIn(14)	
78	HSOp(15)	Ground	Lane 15 transmit data, + and −
79	HSOn(15)	Ground	
80	Ground	HSIp(15)	Lane 15 receive data, + and −
81	PRSNT2#	HSIn(15)	
82	Reserved	Ground	

Legend	
Ground pin	Zero volt reference
Power pin	Supplies power to the PCIe card
Card-to-host pin	Signal from the card to the motherboard

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47	Ground	HSIp(7)	Lane 7 receive data, + and −	**Host-to-card pin**	Signal from the motherboard to the card
48	PRSNT2#	HSIn(7)		**Open drain**	May be pulled low or sensed by multiple cards
49	Ground	Ground		**Sense pin**	Tied together on card
PCI Express ×8 cards end at pin 49				**Reserved**	Not presently used, do not connect

Power [edit]



8-pin (left) and 6-pin (right) power connectors used on PCI Express cards

All PCI express cards may consume up to 3 A at +3.3 V (9.9 W). The amount of +12 V and total power they may consume depends on the type of card:[14]:35–36[15]

- ×1 cards are limited to 0.5 A at +12V (6 W) and 10 W combined.
- ×4 and wider cards are limited to 2.1 A at +12V (25 W) and 25 W combined.
- A full-sized ×1 card may draw up to the 25 W limits after initialization and software configuration as a "high power device".
- A full-sized ×16 graphics card[13] may draw up to 5.5 A at +12V (66 W) and 75 W combined after initialization and software configuration as a "high power device".

Optional connectors add 75 W (6-pin) or 150 W (8-pin) of +12 V power for up to 300 W total (2×75 W + 1×150 W). Some cards are using two 8-pin connectors, but this has not been standardized yet, therefore such cards must not carry the official PCI Express logo. This configuration allows 375 W total (1×75 W + 2×150 W) and will likely be standardized by PCI-SIG with the PCI Express 4.0 standard. The 8-pin PCI Express connector could be confused with the EPS12V connector, which is mainly used for powering SMP and multi-core systems.

6-pin power connector (75 W)[16]	
Pin	**Description**
1	+12 V
2	Not connected (usually +12 V as well)
3	+12 V
4	Ground
5	Sense
6	Ground

8-pin power connector (150 W)[17][18][19]	
Pin	**Description**
1	+12 V
2	+12 V
3	+12 V
4	Sense1 (8-pin connected[a])
5	Ground
6	Sense0 (6-pin or 8-pin connected)
7	Ground
8	Ground



6 pin power connector pin map



8 pin power connector pin map

a. ^ When a 6-pin connector is plugged into an 8-pin receptacle the card is notified by a missing *Sense1* that it may only use up to 75 W.

PCI Express Mini Card [edit]

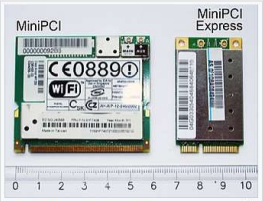


A WLAN PCI Express Mini Card and its connector

PCI Express Mini Card (also known as **Mini PCI Express**, **Mini PCIe**, **Mini PCI-E**, **mPCIe**, and **PEM**), based on PCI Express, is a replacement for the Mini PCI form factor. It is developed by the PCI-SIG. The host device supports both PCI Express and USB 2.0 connectivity, and each card may use either standard. Most laptop computers built after 2005 use PCI Express for expansion cards; however, as of 2015, many vendors are moving toward using the newer M.2 form factor for this purpose.

Due to different dimensions, PCI Express Mini Cards are not physically compatible with standard full-size PCI Express slots; however, passive adapters exist that allow them to be used in full-size slots.[20]

Physical dimensions [edit]



MiniPCI and MiniPCI Express cards in comparison

Dimensions of PCI Express Mini Cards are 30 × 50.95 mm (width × length) for a Full Mini Card. There is a 52-pin edge connector, consisting of two staggered rows on a 0.8 mm pitch. Each row has eight contacts, a gap equivalent to four contacts, then a further 18 contacts. Boards have a thickness of 1.0 mm, excluding the components. A "Half Mini Card" (sometimes abbreviated as HMC) is also specified, having approximately half the physical length of 26.8 mm.

Electrical interface [edit]

PCI Express Mini Card edge connectors provide multiple connections and buses:

- PCI Express ×1 (with SMBus)
- USB 2.0
- Wires to diagnostics LEDs for wireless network (i.e., Wi-Fi) status on computer's chassis
- SIM card for GSM and WCDMA applications (UIM signals on spec.).
- Future extension for another PCIe lane
- 1.5 V and 3.3 V power

Mini-SATA (mSATA) variant [edit]

Despite sharing the Mini PCI Express form factor, an mSATA slot is not necessarily electrically compatible with Mini PCI Express. For this reason, only certain notebooks are compatible with mSATA drives. Most compatible systems are based on Intel's Sandy Bridge processor architecture, using the Huron River platform. Notebooks like Lenovo's ThinkPad T, W and X series, released in March–April 2011, have support for an mSATA SSD card in their WWAN card slot. The ThinkPad Edge E220s/E420s, and the Lenovo IdeaPad Y460/Y560 also support mSATA.[21]

Some notebooks (notably the Asus Eee PC, the Apple MacBook Air, and the Dell mini9 and mini10) use a variant of the PCI Express Mini Card as an SSD. This variant uses the reserved and several non-reserved pins to implement SATA and IDE interface passthrough, keeping only USB, ground lines, and sometimes the core PCIe ×1 bus intact.[22] This makes the "miniPCIe" flash and solid-state drives sold for netbooks largely incompatible with true PCI Express Mini implementations.

Also, the typical Asus miniPCIe SSD is 71 mm long, causing the Dell 51 mm model to often be (incorrectly) referred to as half length. A true 51 mm Mini PCIe SSD was announced in 2009, with two stacked PCB layers that allow for higher storage capacity. The announced design preserves the PCIe interface, making it compatible with the standard mini PCIe slot. No working product has yet been developed.

Intel has numerous desktop boards with the PCIe ×1 Mini-Card slot which typically do not support mSATA SSD. A list of desktop boards that natively support mSATA in the PCIe ×1 Mini-Card slot (typically multiplexed with a SATA port) is provided on the Intel Support site.[23]

Mini PCIe v2 [edit]

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Main article: M.2

The new version of Mini PCI express, M.2 replaces the mSATA standard. Computer bus interfaces provided through the M.2 connector are PCI Express 3.0 (up to four lanes), Serial ATA 3.0, and USB 3.0 (a single logical port for each of the latter two). It is up to the manufacturer of the M.2 host or device to select which interfaces are to be supported, depending on the desired level of host support and device type.

PCI Express External Cabling [edit]

PCI Express External Cabling (also known as *External PCI Express*, *Cabled PCI Express*, or *ePCIe*) specifications were released by the PCI-SIG in February 2007.[24][25]

Standard cables and connectors have been defined for ×1, ×4, ×8, and ×16 link widths, with a transfer rate of 250 MB/s per lane. The PCI-SIG also expects the norm will evolve to reach 500 MB/s, as in PCI Express 2.0. The maximum cable length remains undetermined. An example of the uses of Cabled PCI Express is a metal enclosure, containing a number of PCI slots and PCI-to-ePCIe adapter circuitry. This device would not be possible had it not been for the ePCIe spec.

Derivative forms [edit]

Several other types of expansion card are derived from PCIe; these include:

- Low-height card
- ExpressCard: Successor to the PC Card form factor (with ×1 PCIe and USB 2.0; hot-pluggable)
- PCI Express ExpressModule: A hot-pluggable modular form factor defined for servers and workstations
- XQD card: A PCI Express-based flash card standard by the CompactFlash Association
- XMC: Similar to the CMC/PMC form factor (VITA 42.3)
- AdvancedTCA: A complement to CompactPCI for larger applications; supports serial based backplane topologies
- AMC: A complement to the AdvancedTCA specification; supports processor and I/O modules on ATCA boards (×1, ×2, ×4 or ×8 PCIe).
- FeaturePak: A tiny expansion card format (43 × 65 mm) for embedded and small-form-factor applications which implements two ×1 PCIe links on a high-density connector along with USB, I2C, and up to 100 points of I/O
- Universal IO: A variant from Super Micro Computer Inc designed for use in low-profile rack-mounted chassis.[26] It has the connector bracket reversed so it cannot fit in a normal PCI Express socket, but it is pin-compatible and may be inserted if the bracket is removed.
- Thunderbolt: A variant from Intel that combines DisplayPort and PCIe protocols in a form factor compatible with Mini DisplayPort. Thunderbolt 3.0 also combines USB 3.1 and uses the USB Type-C form factor as opposed to Mini DisplayPort.
- Serial Digital Video Out: Some 9xx series Intel chipsets allow for adding another output for the integrated video into a PCIe slot (mostly dedicated and 16 lanes).
- M.2 (formerly known as NGFF)
- M-PCIe brings PCIe 3.0 to mobile devices (such as tablets and smartphones), over the M-PHY physical layer.[27][28]
- U.2 (formerly known as SFF-8639)

History and revisions [edit]

While in early development, PCIe was initially referred to as *HSI* (for *High Speed Interconnect*), and underwent a name change to *3GIO* (for *3rd Generation I/O*) before finally settling on its PCI-SIG name *PCI Express*. A technical working group named the *Arapaho Work Group* (AWG) drew up the standard. For initial drafts, the AWG consisted only of Intel engineers; subsequently the AWG expanded to include industry partners.

PCI Express is a technology under constant development and improvement.

As of 2013, PCI Express version 4 has been drafted with final specifications expected in 2017.[29] At the 2016 PCI SIG's annual developer's conference and at the Intel Developer Forum, Synopsys showed a system running on PCIe 4.0, while Mellanox provided an appropriate network card.[30][31]

PCI Express link performance[29][32]

PCI Express version	Line code	Transfer rate[i]	Throughput[i]			
			×1	×4	×8	×16
1.0	8b/10b	2.5 GT/s	250 MB/s	1 GB/s	2 GB/s	4 GB/s
2.0	8b/10b	5 GT/s	500 MB/s	2 GB/s	4 GB/s	8 GB/s
3.0	128b/130b	8 GT/s	984.6 MB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s
4.0 (*expected in 2017*)	128b/130b	16 GT/s	1.969 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s
5.0 (*far future*)[30][31]	128b/130b	32 or 25 GT/s[ii]	3.9 or 3.08 GB/s	15.8 or 12.3 GB/s	31.5 or 24.6 GB/s	63.0 or 49.2 GB/s

i. ^ [a] [b] In each direction (each lane is a dual simplex channel).
ii. ^ Both rates are being considered for technical feasibility.

PCI Express 1.0a [edit]

In 2003, PCI-SIG introduced PCIe 1.0a, with a per-lane data rate of 250 MB/s and a transfer rate of 2.5 gigatransfers per second (GT/s). Transfer rate is expressed in transfers per second instead of bits per second because the number of transfers includes the overhead bits, which do not provide additional throughput;[33] PCIe 1.x uses an 8b/10b encoding scheme, resulting in a 20% (= 2/10) overhead on the raw channel bandwidth.[34]

PCI Express 1.1 [edit]

In 2005, PCI-SIG[35] introduced PCIe 1.1. This updated specification includes clarifications and several improvements, but is fully compatible with PCI Express 1.0a. No changes were made to the data rate.

PCI Express 2.0 [edit]

PCI-SIG announced the availability of the PCI Express Base 2.0 specification on 15 January 2007.[36] The PCIe 2.0 standard doubles the transfer rate compared with PCIe 1.0 to 5 GT/s and the per-lane throughput rises from 250 MB/s to 500 MB/s. Consequently, a 32-lane PCIe connector (×32) can support an aggregate throughput of up to 16 GB/s.

PCIe 2.0 motherboard slots are fully backward compatible with PCIe v1.x cards. PCIe 2.0 cards are also generally backward compatible with PCIe 1.x motherboards, using the available bandwidth of PCI Express 1.1. Overall, graphic cards or motherboards designed for v2.0 will work with the other being v1.1 or v1.0a.

The PCI-SIG also said that PCIe 2.0 features improvements to the point-to-point data transfer protocol and its software architecture.[37]



A PCI Express 2.0 expansion card that provides USB 3.0 connectivity.[a]

Intel's first PCIe 2.0 capable chipset was the X38 and boards began to ship from various vendors (Abit, Asus, Gigabyte) as of October 21, 2007.[38] AMD started supporting PCIe 2.0 with its AMD 700 chipset series and nVidia started with the MCP72.[39] All of Intel's prior chipsets, including the Intel P35 chipset, supported PCIe 1.1 or 1.0a.[40]

Like 1.x, PCIe 2.0 uses an 8b/10b encoding scheme, therefore delivering, per-lane, an effective 4 Gbit/s max transfer rate from its 5 GT/s raw data rate.

PCI Express 2.1 [edit]

PCI Express 2.1 (with its specification dated March 4, 2009) supports a large proportion of the management, support, and troubleshooting systems planned for full implementation in PCI Express 3.0. However, the speed is the same as PCI Express 2.0. Unfortunately, the increase in power from the slot breaks backward compatibility between PCI Express 2.1 cards and some older motherboards with 1.0/1.0a, but most motherboards with PCI Express 1.1 connectors are provided with a BIOS update by their manufacturers through utilities to support backward compatibility of cards with PCIe 2.1.

PCI Express 3.0 [edit]

PCI Express 3.0 Base specification revision 3.0 was made available in November 2010, after multiple delays. In August 2007, PCI-SIG announced that PCI Express 3.0 would carry a bit rate of 8 gigatransfers per second (GT/s), and that it would be backward compatible with existing PCI Express implementations. At that time, it was also announced that the final specification for PCI Express 3.0 would be delayed until Q2 2010.[41] New features for the PCI Express 3.0 specification include a number of optimizations for enhanced signaling and data integrity, including transmitter and receiver equalization, PLL improvements, clock data recovery, and channel enhancements for currently supported topologies.[42]

Following a six-month technical analysis of the feasibility of scaling the PCI Express interconnect bandwidth, PCI-SIG's analysis found that 8 gigatransfers per second can be manufactured in mainstream silicon process technology, and can be deployed with existing low-cost materials and infrastructure, while maintaining full compatibility (with negligible impact) to the PCI Express protocol stack.

PCI Express 3.0 upgrades the encoding scheme to 128b/130b from the previous 8b/10b encoding, reducing the bandwidth overhead from 20% of PCI Express 2.0 to approximately 1.54% (= 2/130). This is achieved by a technique called "scrambling" that applies a known binary polynomial to a data stream in a feedback topology. Because the scrambling polynomial is known, the data can be recovered by running it through a feedback topology using the inverse polynomial. PCI Express 3.0's 8 GT/s bit rate effectively delivers 985 MB/s per lane, practically doubling the lane bandwidth relative to PCI Express 2.0.[32]

On November 18, 2010, the PCI Special Interest Group officially published the finalized PCI Express 3.0 specification to its members to build devices based on this new version of PCI Express.[43]

PCI Express 3.1 [edit]

In September 2013, PCI Express 3.1 specification was announced to be released in late 2013 or early 2014, consolidating various improvements to the published PCI Express 3.0 specification in three areas: power management, performance and functionality.[28][44] It was released in November 2014.[45]

PCI Express 4.0 [edit]

On November 29, 2011, PCI-SIG announced PCI Express 4.0,[46] providing a 16 GT/s bit rate that doubles the bandwidth provided by PCI Express 3.0, while maintaining backward and forward compatibility in both software support and used mechanical interface.[47] PCI Express 4.0 specs will also bring OCuLink-2, an alternative to Thunderbolt connector. OCuLink version 2 will have up to 16 GT/s (8GB/s total for ×4 lanes),[48] while the maximum bandwidth of a thunderbolt 3 connector is 5GB/s. Additionally, active and idle power optimizations are to be investigated. Final specifications are expected to be released in 2017.[49][50]

In August 2016, Synopsys presented a test machine running PCIe 4.0 at the Intel Developer Forum. Their IP has been licensed to several firms planning to present their chips and products at the end of 2016.[31]

Extensions and future directions [edit]

Some vendors offer PCIe over fiber products,[51][52][53] but these generally find use only in specific cases where transparent PCIe bridging is preferable to using a more mainstream standard (such as InfiniBand or Ethernet) that may require additional software to support it; current implementations focus on distance rather than raw bandwidth and typically do not implement a full ×16 link.

Thunderbolt was co-developed by Intel and Apple as a general-purpose high speed interface combining a ×4 PCIe link with DisplayPort and was originally intended to be an all-fiber interface, but due to early difficulties in creating a consumer-friendly fiber interconnect, most early implementations are hybrid copper-fiber systems. A notable exception, the Sony VAIO Z VPC-Z2, uses a nonstandard USB port with an optical component to connect to an outboard PCIe display adapter. Apple has been the primary driver of Thunderbolt adoption through 2011, though several other vendors[54] have announced new products and systems featuring Thunderbolt.

Mobile PCIe specification (abbreviated to *M-PCIe*) allows PCI Express architecture to operate over the MIPI Alliance's M-PHY physical layer technology. Building on top of already existing widespread adoption of M-PHY and its low-power design, Mobile PCIe allows PCI Express to be used in tablets and smartphones.[55]

OCuLink (standing for "optical-copper link") is an extension for the "cable version of PCI Express", acting as a competitor to version 3 of the Thunderbolt interface. Version 1.0 of OCuLink, to be released in fall 2015, supports up to PCIe 3.0 x4 lanes (8 GT/s, 3.9 GB/s) over copper cabling; a fiber optic version may appear in the future.[28][56]

Hardware protocol summary [edit]

The PCIe link is built around dedicated unidirectional couples of serial (1-bit), point-to-point connections known as *lanes*. This is in sharp contrast to the earlier PCI connection, which is a bus-based system where all the devices share the same bidirectional, 32-bit or 64-bit parallel bus.

PCI Express is a layered protocol, consisting of a *transaction layer*, a *data link layer*, and a *physical layer*. The Data Link Layer is subdivided to include a media access control (MAC) sublayer. The Physical Layer is subdivided into logical and electrical sublayers. The Physical logical-sublayer contains a physical coding sublayer (PCS). The terms are borrowed from the IEEE 802 networking protocol model.

Physical layer [edit]

The PCIe Physical Layer (*PHY*, *PCIEPHY*, *PCI Express PHY*, or *PCIe PHY*) specification is divided into two sub-layers, corresponding to electrical and logical specifications. The logical sublayer is sometimes further divided into a MAC sublayer and a PCS, although this division is not formally part of the PCIe specification. A specification published by Intel, the PHY Interface for PCI Express (PIPE),[58] defines the MAC/PCS functional partitioning and the interface between these two sub-layers. The PIPE specification also identifies the *physical media attachment* (PMA) layer, which includes the serializer/deserializer (SerDes) and other analog circuitry; however, since SerDes implementations vary greatly among ASIC vendors, PIPE does not specify an interface between the PCS and PMA.

At the electrical level, each lane consists of two unidirectional LVDS pairs operating at 2.5, 5, 8 or 16 Gbit/s,

Card pins and lengths

Lanes	Pins		Length	
	Total	Variable	Total	Variable
×1	2×18 = 36[57]	2×7 = 14	25 mm	7.65 mm
×4	2×32 = 64	2×21 = 42	39 mm	21.65 mm
×8	2×49 = 98	2×38 = 76	56 mm	38.65 mm
×16	2×82 = 164	2×71 = 142	89 mm	71.65 mm

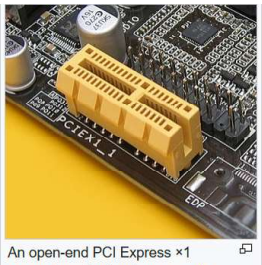
Marvell Semiconductor, Inc. - Ex. 1018, Page 000149

depending on the negotiated capabilities. Transmit and receive are separate differential pairs, for a total of four data wires per lane.

A connection between any two PCIe devices is known as a *link*, and is built up from a collection of one or more *lanes*. All devices must minimally support single-lane (×1) link. Devices may optionally support wider links composed of 2, 4, 8, 12, 16, or 32 lanes. This allows for very good compatibility in two ways:

- A PCIe card physically fits (and works correctly) in any slot that is at least as large as it is (e.g., an ×1 sized card will work in any sized slot);
- A slot of a large physical size (e.g., ×16) can be wired electrically with fewer lanes (e.g., ×1, ×4, ×8, or ×12) as long as it provides the ground connections required by the larger physical slot size.

In both cases, PCIe negotiates the highest mutually supported number of lanes. Many graphics cards, motherboards and BIOS versions are verified to support ×1, ×4, ×8 and ×16 connectivity on the same connection.



An open-end PCI Express ×1 connector, allowing longer cards capable of using more lanes to be plugged while operating at ×1 speeds

Even though the two would be signal-compatible, it is not usually possible to place a physically larger PCIe card (e.g., a ×16 sized card) into a smaller slot – though if the PCIe slots are altered or a riser is used most motherboards will allow this. The width of a PCIe connector is 8.8 mm, while the height is 11.25 mm, and the length is variable. The fixed section of the connector is 11.65 mm in length and contains two rows of 11 (22 pins total), while the length of the other section is variable depending on the number of lanes. The pins are spaced at 1 mm intervals, and the thickness of the card going into the connector is 1.8 mm.[59][60]

Data transmission [edit]

PCIe sends all control messages, including interrupts, over the same links used for data. The serial protocol can never be blocked, so latency is still comparable to conventional PCI, which has dedicated interrupt lines.

Data transmitted on multiple-lane links is interleaved, meaning that each successive byte is sent down successive lanes. The PCIe specification refers to this interleaving as *data striping*. While requiring significant hardware complexity to synchronize (or deskew) the incoming striped data, striping can significantly reduce the latency of the n^{th} byte on a link. While the lanes are not tightly synchronized, there is a limit to the *lane to lane skew* of 20/8/6 ns for 2.5/5/8 GT/s so the hardware buffers can re-align the striped data.[61] Due to padding requirements, striping may not necessarily reduce the latency of small data packets on a link.

As with other high data rate serial transmission protocols, the clock is embedded in the signal. At the physical level, PCI Express 2.0 utilizes the 8b/10b encoding scheme[32] to ensure that strings of consecutive identical digits (zeros or ones) are limited in length. This coding was used to prevent the receiver from losing track of where the bit edges are. In this coding scheme every eight (uncoded) payload bits of data are replaced with 10 (encoded) bits of transmit data, causing a 20% overhead in the electrical bandwidth. To improve the available bandwidth, PCI Express version 3.0 instead uses 128b/130b encoding with scrambling. 128b/130b encoding relies on the scrambling to limit the run length of identical-digit strings in data streams and ensure the receiver stays synchronised to the transmitter. It also reduces electromagnetic interference (EMI) by preventing repeating data patterns in the transmitted data stream.

Data link layer [edit]

The data link layer performs three vital services for the PCIe express link:

1. sequence the transaction layer packets (TLPs) that are generated by the transaction layer,
2. ensure reliable delivery of TLPs between two endpoints via an acknowledgement protocol (ACK and NAK signaling) that explicitly requires replay of unacknowledged/bad TLPs,
3. initialize and manage flow control credits

On the transmit side, the data link layer generates an incrementing sequence number for each outgoing TLP. It serves as a unique identification tag for each transmitted TLP, and is inserted into the header of the outgoing TLP. A 32-bit cyclic redundancy check code (known in this context as Link CRC or LCRC) is also appended to the end of each outgoing TLP.

On the receive side, the received TLP's LCRC and sequence number are both validated in the link layer. If either the LCRC check fails (indicating a data error), or the sequence-number is out of range (non-consecutive from the last valid received TLP), then the bad TLP, as well as any TLPs received after the bad TLP, are considered invalid and discarded. The receiver sends a negative acknowledgement message (NAK) with the sequence-number of the invalid TLP, requesting re-transmission of all TLPs forward of that sequence-number. If the received TLP passes the LCRC check and has the correct sequence number, it is treated as valid. The link receiver increments the sequence-number (which tracks the last received good TLP), and forwards the valid TLP to the receiver's transaction layer. An ACK message is sent to remote transmitter, indicating the TLP was successfully received (and by extension, all TLPs with past sequence-numbers.)

If the transmitter receives a NAK message, or no acknowledgement (NAK or ACK) is received until a timeout period expires, the transmitter must retransmit all TLPs that lack a positive acknowledgement (ACK). Barring a persistent malfunction of the device or transmission medium, the link-layer presents a reliable connection to the transaction layer, since the transmission protocol ensures delivery of TLPs over an unreliable medium.

In addition to sending and receiving TLPs generated by the transaction layer, the data-link layer also generates and consumes DLLPs, data link layer packets. ACK and NAK signals are communicated via DLLPs, as are flow control credit information, some power management messages and flow control credit information (on behalf of the transaction layer).

In practice, the number of in-flight, unacknowledged TLPs on the link is limited by two factors: the size of the transmitter's replay buffer (which must store a copy of all transmitted TLPs until the remote receiver ACKs them), and the flow control credits issued by the receiver to a transmitter. PCI Express requires all receivers to issue a minimum number of credits, to guarantee a link allows sending PCIConfig TLPs and message TLPs.

Transaction layer [edit]

PCI Express implements split transactions (transactions with request and response separated by time), allowing the link to carry other traffic while the target device gathers data for the response.

PCI Express uses credit-based flow control. In this scheme, a device advertises an initial amount of credit for each received buffer in its transaction layer. The device at the opposite end of the link, when sending transactions to this device, counts the number of credits each TLP consumes from its account. The sending device may only transmit a TLP when doing so does not make its consumed credit count exceed its credit limit. When the receiving device finishes processing the TLP from its buffer, it signals a return of credits to the sending device, which increases the credit limit by the restored amount. The credit counters are modular counters, and the comparison of consumed credits to credit limit requires modular arithmetic. The advantage of this scheme (compared to other methods such as wait states or handshake-based transfer protocols) is that the latency of credit return does not affect performance, provided that the credit limit is not encountered. This assumption is generally met if each device is designed with adequate buffer sizes.

PCIe 1.x is often quoted to support a data rate of 250 MB/s in each direction, per lane. This figure is a calculation from the physical signaling rate (2.5 gigabaud) divided by the encoding overhead (10 bits per byte.) This means a sixteen lane (×16) PCIe card would then be theoretically capable of 16×250 MB/s = 4 GB/s in each direction. While this is correct in terms of data bytes, more meaningful calculations are based on the usable data payload rate, which depends on the profile of the traffic, which is a function of the high-level (software) application and intermediate protocol levels.

Like other high data rate serial interconnect systems, PCIe has a protocol and processing overhead due to the additional transfer robustness (CRC and acknowledgements). Long continuous unidirectional transfers (such as those typical in high-performance storage controllers) can approach >95% of PCIe's raw (lane) data rate. These transfers also benefit the most from increased number of lanes (×2, ×4, etc.) But in more typical applications (such as a USB or Ethernet controller), the traffic profile is characterized as short data packets with frequent enforced acknowledgements.[62] This type of traffic reduces the efficiency of the link, due to overhead from packet parsing and forced interrupts (either in the device's host interface or the PC's CPU). Being a protocol for devices connected to the same printed circuit board, it does not require the same tolerance for transmission errors as a protocol for communication over longer distances, and thus, this loss of efficiency is not particular to PCIe.

Applications [edit]

PCI Express operates in consumer, server, and industrial applications, as a motherboard-level interconnect (to link motherboard-mounted peripherals), a passive backplane interconnect and as an expansion card interface for add-in boards.



Asus Nvidia GeForce GTX 650 Ti, a PCI Express 3.0 ×16 graphics card

In virtually all modern (as of 2012) PCs, from consumer laptops and desktops to enterprise data servers, the PCIe bus serves as the primary motherboard-level interconnect, connecting the host system-processor with both integrated-peripherals (surface-mounted ICs) and add-on peripherals (expansion cards). In most of these systems, the PCIe bus co-exists with one or more legacy PCI buses, for backward compatibility with the large body of legacy PCI peripherals.

As of 2013 PCI Express has replaced AGP as the default interface for graphics cards on new systems. Almost all models of graphics cards released since 2010 by AMD (ATI) and Nvidia use PCI Express. Nvidia uses the high-bandwidth data transfer of PCIe for its Scalable Link Interface (SLI) technology, which allows multiple graphics cards of the same chipset and model number to run in tandem, allowing increased performance. AMD has also developed a multi-GPU system based on PCIe called CrossFire. AMD and Nvidia have released motherboard chipsets that support as many as four PCIe ×16 slots, allowing tri-GPU and quad-GPU card configurations.



Intel 82574L Gigabit Ethernet NIC, a PCI Express ×1 card

External GPUs [edit]

Theoretically, external PCIe could give a notebook the graphics power of a desktop, by connecting a notebook with any PCIe desktop video card (enclosed in its own external housing, with strong power supply and cooling); possible with an ExpressCard interface or a Thunderbolt interface. The ExpressCard interface provides bit rates of 5 Gbit/s (0.5 GB/s throughput), whereas the Thunderbolt interface provides bit rates of up to 40 Gbit/s (5 GB/s throughput).

In 2010 external card hubs were introduced that can connect to a laptop or desktop through a PCI ExpressCard slot. These hubs can accept full-sized graphics cards. Examples include MSI GUS,[63] Village Instrument's ViDock,[64] the Asus XG Station, Bplus PE4H V3.2 adapter,[65] as well as more improvised DIY devices.[66] However such solutions are limited by the size (often only x1) and version of the available PCIe slot on a laptop.



A Marvell-based SATA 3.0 controller, as a PCI Express ×1 card

In 2008, AMD announced the ATI XGP technology, based on a proprietary cabling system that is compatible with PCIe ×8 signal transmissions.[67] This connector is available on the Fujitsu Amilo and the Acer Ferrari One notebooks. Fujitsu launched their AMILO GraphicBooster enclosure for XGP soon thereafter.[68] Around 2010 Acer launched the Dynavivid graphics dock for XGP.[69]

Intel Thunderbolt interface has given opportunity to new and faster products to connect with a PCIe card externally. Magma has released the ExpressBox 3T, which can hold up to three PCIe cards (two at ×8 and one at ×4).[70] MSI also released the Thunderbolt GUS II, a PCIe chassis dedicated for video cards.[71] Other products such as the Sonnet's Echo Express[72] and mLogic's mLink are Thunderbolt PCIe chassis in a smaller form factor.[73] However, all these products require a computer with a Thunderbolt port (i.e., Thunderbolt devices), such as, for example, Apple's Macbook Pro released in fall 2013.

For the professional market, Nvidia has developed the Quadro Plex external PCIe family of GPUs that can be used for advanced graphic applications. These video cards require a PCI Express ×8 or ×16 slot for the host-side card which connects to the Plex via a VHDCI carrying 8 PCIe lanes.[74]

Storage devices [edit]

See also: SATA Express and NVM Express



An OCZ RevoDrive SSD, a full-height ×4 PCI Express card

PCI Express protocol can be used as data interface to flash memory devices, such as memory cards and solid-state drives (SSDs).

XQD card is a memory card format utilizing PCI Express, developed by the CompactFlash Association, with transfer rates of up to 500 MB/s.[75]

Many high-performance, enterprise-class SSDs are designed as PCI Express RAID controller cards with flash memory chips placed directly on the circuit board, utilizing proprietary interfaces and custom drivers to communicate with the operating system; this allows much higher transfer rates (over 1 GB/s) and IOPS (over one million I/O operations per second) when compared to Serial ATA or SAS drives.[76][77] For example, in 2011 OCZ and Marvell co-developed a native PCI Express solid-state drive controller for a PCI Express 3.0 ×16 slot with maximum capacity of 12 TB and a performance of to 7.2 GB/s sequential transfers and up to 2.52 million IOPS in random transfers.[78]

SATA Express is an interface for connecting SSDs, by providing multiple PCI Express lanes as a pure PCI Express connection to the attached storage device.[79] M.2 is a specification for internally mounted computer expansion cards and associated connectors, which also uses multiple PCI Express lanes.[00]

PCI Express storage devices can implement both AHCI logical interface for backward compatibility, and NVM Express logical interface for much faster I/O operations provided by utilizing internal parallelism offered by such devices. Enterprise-class SSDs can also implement SCSI over PCI Express.[81]

Cluster interconnect [edit]

Certain data-center applications (such as large computer clusters) require the use of fiber-optic interconnects due to the distance limitations inherent in copper cabling. Typically, a network-oriented standard such as Ethernet or Fibre Channel suffices for these applications, but in some cases the overhead introduced by routable protocols is undesirable and a lower-level interconnect, such as InfiniBand, RapidIO, or NUMAlink is needed. Local-bus standards such as PCIe and HyperTransport can in principle be used for this purpose,[82] but as of 2015 solutions are only available from niche vendors such as Dolphin ICS.

Competing protocols [edit]

Other communications standards based on high bandwidth serial architectures include InfiniBand, RapidIO, HyperTransport, Intel QuickPath Interconnect, and the Mobile Industry Processor Interface (MIPI). The differences are based on the trade-offs between flexibility and extensibility vs latency and overhead. For example, adding complex header information to a transmitted packet allows for complex routing (PCI Express is capable of this through an optional End-to-End TLP Prefix feature[83]). The

additional overhead reduces the effective bandwidth of the interface and complicates bus discovery and initialization software. Also making the system hot-pluggable requires that software track network topology changes. InfiniBand is such a technology.

Another example is making the packets shorter to decrease latency (as is required if a bus must operate as a memory interface). Smaller packets mean packet headers consume a higher percentage of the packet, thus decreasing the effective bandwidth. Examples of bus protocols designed for this purpose are RapidIO and HyperTransport.

PCI Express falls somewhere in the middle, targeted by design as a system interconnect (local bus) rather than a device interconnect or routed network protocol. Additionally, its design goal of software transparency constrains the protocol and raises its latency somewhat.

Delays in PCIe 4.0 implementations led to the Gen-Z consortium, the CCIX[84] effort and an open Coherent Accelerator Processor Interface (CAPI) all being announced by the end of 2016.[85]

See also [edit]

- Active State Power Management (ASPM)
- Conventional PCI
- PCI configuration space
- PCI-X
- PCI/104-Express
- PCIe/104
- Root complex
- Serial Digital Video Out (SDVO)
- List of device bit rates § Main buses

Electronics portal

Notes [edit]

a. ^ The card's Serial ATA power connector is present because the USB 3.0 ports require more power than the PCI Express bus can supply. More often, a 4-pin Molex power connector is used.

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v·t·e **Technical and *de facto* standards for wired computer buses** [show]

v·t·e **Basic computer components** [show]

Categories: 2004 introductions | Peripheral Component Interconnect | Serial buses | Standards organizations | Motherboard expansion slot

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