

EXHIBIT 65

Exhibit 65 – Domestic Industry Claim Chart for U.S. Patent No. 10,877,233 (“’233 Patent”)

The following chart is based on information known to date. Credo reserves the right to amend and update this chart as additional information is obtained and analyzed. The exemplary claim mappings below rely on images and data from Credo’s 800G OSFP PAM4 to 800G OSFP PAM4 Plug & Play Active Electrical Cable. The following chart is representative of all the Domestic Industry Products.

As outlined in the below claim chart, the Domestic Industry Products practice, either literally or under the doctrine of equivalents, at least Claim 1 of the ’233 patent.

<u>’233 Patent</u>	<u>Domestic Industry Products</u>
<u>Claim 1</u>	
[1pre] A cable that comprises:	<p>The Domestic Industry Products comprise a cable.</p> <p>See, e.g.:</p>  <p>Ex. 62, <i>Credo 800G OSFP AEC Product Specification</i> at 1.</p>

'233 Patent	Domestic Industry Products																						
Claim 1																							
[1a] a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;	<p>The Domestic Industry Products comprise a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug.</p> <p>For example, the first DRR device is a first digital signal processor (“DSP”) at one end of the cable.</p> <p>The first DSP in the Domestic Industry Products is a retimer that exchanges inbound and outbound multi-lane data streams (i.e., 8 TX and 8 RX) with a first host interface port (i.e., an OSFP port) via a connector plug (i.e., an OSFP connector) at one end of the cable.</p> <p>See, e.g.:</p> <table border="1"> <thead> <tr> <th>Parameter</th><th>Value</th></tr> </thead> <tbody> <tr> <td>Module Form Factor</td><td>OSFP</td></tr> <tr> <td>Number of Data Lanes</td><td>8 TX and 8 RX per module (PAM4)</td></tr> <tr> <td>Maximum Aggregate Data Rate</td><td>800Gbps</td></tr> <tr> <td>Nominal Data Rate per Lane</td><td>106.25Gbps (PAM4)</td></tr> <tr> <td>Electrical Interface and Pin-out</td><td>60-pin edge connector</td></tr> <tr> <td>Pin Description</td><td>Per OSFP Hardware Specification</td></tr> <tr> <td>Management Interface</td><td>I²C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers v 4.0</td></tr> <tr> <td>Length of Copper AEC</td><td>0.5m - 2.5m in 0.5m increments</td></tr> <tr> <td>BER (Pre-FEC)*</td><td>Typ. <10⁻⁸</td></tr> <tr> <td>BER (Post-FEC)*</td><td><10⁻¹⁵</td></tr> </tbody> </table> <p>* Tested with QPRBS31 pattern</p> <p>Ex. 62, <i>Credo 800G OSFP AEC Product Specification</i> at 2 (annotated).</p>	Parameter	Value	Module Form Factor	OSFP	Number of Data Lanes	8 TX and 8 RX per module (PAM4)	Maximum Aggregate Data Rate	800Gbps	Nominal Data Rate per Lane	106.25Gbps (PAM4)	Electrical Interface and Pin-out	60-pin edge connector	Pin Description	Per OSFP Hardware Specification	Management Interface	I ² C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers v 4.0	Length of Copper AEC	0.5m - 2.5m in 0.5m increments	BER (Pre-FEC)*	Typ. <10 ⁻⁸	BER (Post-FEC)*	<10 ⁻¹⁵
Parameter	Value																						
Module Form Factor	OSFP																						
Number of Data Lanes	8 TX and 8 RX per module (PAM4)																						
Maximum Aggregate Data Rate	800Gbps																						
Nominal Data Rate per Lane	106.25Gbps (PAM4)																						
Electrical Interface and Pin-out	60-pin edge connector																						
Pin Description	Per OSFP Hardware Specification																						
Management Interface	I ² C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers v 4.0																						
Length of Copper AEC	0.5m - 2.5m in 0.5m increments																						
BER (Pre-FEC)*	Typ. <10 ⁻⁸																						
BER (Post-FEC)*	<10 ⁻¹⁵																						

'233 Patent	Domestic Industry Products
Claim 1	
<p>[1b] a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and</p>	<p>The Domestic Industry Products comprise a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug.</p> <p>For example, the second DRR device is a second DSP retimer at the other end of the cable.</p>  <p>Ex. 62, <i>Credo 800G OSFP AEC Product Specification</i> at 1.</p> <p>The second DSP exchanges inbound and outbound multi-lane data streams (i.e., 8 TX and 8 RX) with a second host interface port (i.e., an OSFP port) via a connector plug (i.e., an OSFP connector) at the other end of the cable.</p>

'233 Patent	Domestic Industry Products																						
Claim 1																							
	<table> <tr> <th>Parameter</th><th>Value</th></tr> <tr> <td>Module Form Factor</td><td>QSFP</td></tr> <tr> <td>Number of Data Lanes</td><td>8 TX and 8 RX per module (PAM4)</td></tr> <tr> <td>Maximum Aggregate Data Rate</td><td>800Gbps</td></tr> <tr> <td>Nominal Data Rate per Lane</td><td>106.25Gbps (PAM4)</td></tr> <tr> <td>Electrical Interface and Pin-out</td><td>60-pin edge connector</td></tr> <tr> <td>Pin Description</td><td>Per QSFP Hardware Specification</td></tr> <tr> <td>Management Interface</td><td>I²C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers v 4.0</td></tr> <tr> <td>Length of Copper AEC</td><td>0.5m - 2.5m in 0.5m increments</td></tr> <tr> <td>BER (Pre-FEC)*</td><td>Typ. <10⁻⁸</td></tr> <tr> <td>BER (Post-FEC)*</td><td><10⁻¹⁵</td></tr> </table> <p>* Tested with QPRBS31 pattern</p> <p>Ex. 62, <i>Credo 800G QSFP AEC Product Specification</i> at 2 (annotated).</p>	Parameter	Value	Module Form Factor	QSFP	Number of Data Lanes	8 TX and 8 RX per module (PAM4)	Maximum Aggregate Data Rate	800Gbps	Nominal Data Rate per Lane	106.25Gbps (PAM4)	Electrical Interface and Pin-out	60-pin edge connector	Pin Description	Per QSFP Hardware Specification	Management Interface	I ² C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers v 4.0	Length of Copper AEC	0.5m - 2.5m in 0.5m increments	BER (Pre-FEC)*	Typ. <10 ⁻⁸	BER (Post-FEC)*	<10 ⁻¹⁵
Parameter	Value																						
Module Form Factor	QSFP																						
Number of Data Lanes	8 TX and 8 RX per module (PAM4)																						
Maximum Aggregate Data Rate	800Gbps																						
Nominal Data Rate per Lane	106.25Gbps (PAM4)																						
Electrical Interface and Pin-out	60-pin edge connector																						
Pin Description	Per QSFP Hardware Specification																						
Management Interface	I ² C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers v 4.0																						
Length of Copper AEC	0.5m - 2.5m in 0.5m increments																						
BER (Pre-FEC)*	Typ. <10 ⁻⁸																						
BER (Post-FEC)*	<10 ⁻¹⁵																						
[1c] electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,	<p>The Domestic Industry Products comprise electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween.</p> <p>For example, the electrical conductors are a plurality of twin-axial copper conductors that connect the first and second DSPs to convey electrical transit signals therebetween.</p> <p>See, e.g.:</p>																						

'233 Patent	Domestic Industry Products								
Claim 1									
	<div>Mechanicals</div> <table><tr><th>Parameter</th><th>Cable Type</th><th>Typical</th><th>Length</th></tr><tr><td>Diameter</td><td>16P 32AWG</td><td>6.8mm</td><td>0.5-2.5m</td></tr></table> <p>Ex. 62, <i>Credo 800G OSFP AEC Product Specification</i> at 2.</p>	Parameter	Cable Type	Typical	Length	Diameter	16P 32AWG	6.8mm	0.5-2.5m
Parameter	Cable Type	Typical	Length						
Diameter	16P 32AWG	6.8mm	0.5-2.5m						
[1d] the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and	<p>The first DRR device in the Domestic Industry Products converts between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port.</p> <p>For example, the first DSP receives electrical transit signals from the cable and converts them (via the retimer) into multi-lane data streams that are sent to the host. The first DSP also receives multi-lane data streams from the host and converts them (via the retimer) into electrical transit signals that are sent to the cable.</p> <p>See, e.g.:</p>								

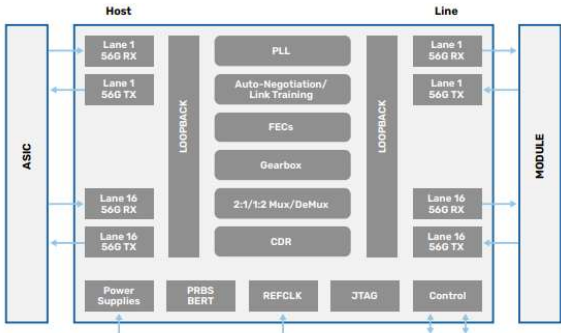
'233 Patent	Domestic Industry Products
Claim 1	<ul style="list-style-type: none"> Multi-channel bidirectional retimers for 10 - 56Gbps Superior random jitter performance Up to 35dB insertion loss CEI-56G-VSR/MR/LR-PAM4 compliant CEI-28G-LR and CEI-28G-VSR/SR/MR compliant TX equalization with programmable main, pre, and post-cursor Fully adaptive and programmable RX equalization with CTLE,FFE, and DFE Auto negotiation between the link partners on both sides of the retimer (IEEE 802.3 clause 73) KR back-channel training (IEEE 802.3 clause 72,92,93,136) Input/output polarity switch control Register control via I²C or standard MDIO interface Built in diagnostic features including PRBS generator and checker, PRBS FEC Analyzer, internal eye monitor and analog test point <p>Ex. 53, CRT55321 Product Brief at 2 (annotated).</p>

'233 Patent	Domestic Industry Products
Claim 1	
<p>[1e] the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,</p>	<p>The second DRR device in the Domestic Industry Products converts between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port.</p> <p>For example, the second DSP at the other end of the cable also converts between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port via the retimer.</p> <p>See, e.g.:</p>

'233 Patent	Domestic Industry Products
Claim 1	<ul style="list-style-type: none"> Multi-channel bidirectional retimers for 10 - 56Gbps Superior random jitter performance Up to 35dB insertion loss CEI-56G-VSR/MR/LR-PAM4 compliant CEI-28G-LR and CEI-28G-VSR/SR/MR compliant TX equalization with programmable main, pre, and post-cursor Fully adaptive and programmable RX equalization with CTLE,FFE, and DFE Auto negotiation between the link partners on both sides of the retimer (IEEE 802.3 clause 73) KR back-channel training (IEEE 802.3 clause 72,92,93,136) Input/output polarity switch control Register control via I²C or standard MDIO interface Built in diagnostic features including PRBS generator and checker, PRBS FEC Analyzer, internal eye monitor and analog test point <p>Ex. 53, CRT55321 Product Brief at 2 (annotated).</p>

'233 Patent	Domestic Industry Products
Claim 1 [1f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.	
	<p>The first and second DRR devices in the Domestic Industry Products provide pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.</p> <p>For example, the exemplary Domestic Industry Products use OSFP connectors.</p> <p>Supported Standards and Interfaces</p>  <ul style="list-style-type: none"> • Common Management Interface Specification (CMIS) v4.0 • OSFP MSA v3.0 <p>Ex. 62, <i>Credo 800G OSFP AEC Product Specification</i> at 1.</p> <p>The OSFP standard requires compliance with the IEEE 802.3ck standard.</p> <p>The high-speed signals follow the electrical specifications of IEEE802.3bs, IEEE802.3cd, IEEE 802.3ck and CEI-56G-VSR-PAM4 as defined in OIF-CEI-05.2 for 400GAUI-8 mode and IEEE802.3bj, IEEE802.3bm for CAUI-4 mode.</p> <p>Ex. 54, <i>OSFP Specification</i> at 147 (annotated).</p>

'233 Patent	Domestic Industry Products
Claim 1	
	<p>The first and second DSPs provide different levels of pre-equalization corresponding to “short” and “long” modes used for 112G-per-lane chip-to-module (C2M) transmission, per the IEEE 802.3ck standard. The transmit filter coefficient values used for short-channel and long-channel pre-equalization are stored in nonvolatile memories so they are available for C2M communications when the cable is connected to the host.</p> <p>See, e.g.:</p> <p>120G.3.2.1 Module output modes</p> <p>The module output shall support two modes: short and long. The means of controlling the module output mode is implementation dependent. For each output mode, the module shall meet the requirements for eye height (min) and VEC (max) in Table 120G-3 for both near-end and far-end measurements (see 120G.3.2.2.1).</p> <p>Ex. 52, <i>IEEE 802.3ck Specification</i> at 7275 (annotated).</p> <p>Transmit filter coefficients are stored in non-volatile flash memories in a microcontroller unit (MCU) connected to the retimer chip. The MCU retrieves these coefficients and provides them to the retimer chip at boot-up (power-on).</p> <p>See, e.g.:</p>

'233 Patent	Domestic Industry Products
Claim 1	
	<ul style="list-style-type: none"> • Multi-channel bidirectional retimers for 10 - 56Gbps • Superior random jitter performance • Up to 35dB insertion loss • CEI-56G-VSR/MR/LR-PAM4 compliant • CEI-28G-LR and CEI-28G-VSR/SR/MR compliant • TX equalization with programmable main, pre, and post-cursor • Fully adaptive and programmable RX equalization with CTLE,FFE, and DFE • Auto negotiation between the link partners on both sides of the retimer (IEEE 802.3 clause 73) • KR back-channel training (IEEE 802.3 clause 72,92,93,136) • Input/output polarity switch control • Register control via I²C or standard MDIO interface • Built in diagnostic features including PRBS generator and checker, PRBS FEC Analyzer, internal eye monitor and analog test point  <p>Ex. 53, CRT55321 Product Brief at 2 (annotated).</p>