

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Marvell Semiconductor, Inc.,

Petitioner,

v.

Credo Technology Group Ltd.,

Patent Owner.

Case No. IPR2025-01218

U.S. Patent 10,877,233

Declaration of Michael S. Chen

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I, Michael Shuo-Wei Chen, declare as follows:

1. My name is Michael Shuo-Wei Chen. I am a Professor in the Department of Electrical Engineering at the University of Southern California. A summary of my background and qualifications can be found in §VI below. My full Curriculum Vitae is attached to this declaration as Appendix 1.

2. I have prepared this report as an expert witness retained by Marvell Semiconductor, Inc. In this report I give my opinions as to whether certain claims of U.S. Patent No. 10,877,233 (“the ’233 patent”) are invalid. I provide technical bases for these opinions as appropriate.

3. This report contains statements of my opinions formed to date and the bases and reasons for those opinions. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses. I make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained herein.

I. OVERVIEW OF THE TECHNOLOGY

4. High-speed serial communications became popular and widespread in the 1990s. In contrast to parallel architectures where multiple lines send different data signals, serial communications send a single signal down a single channel. As transmission speeds increased, parallel data lines reached their limits due to

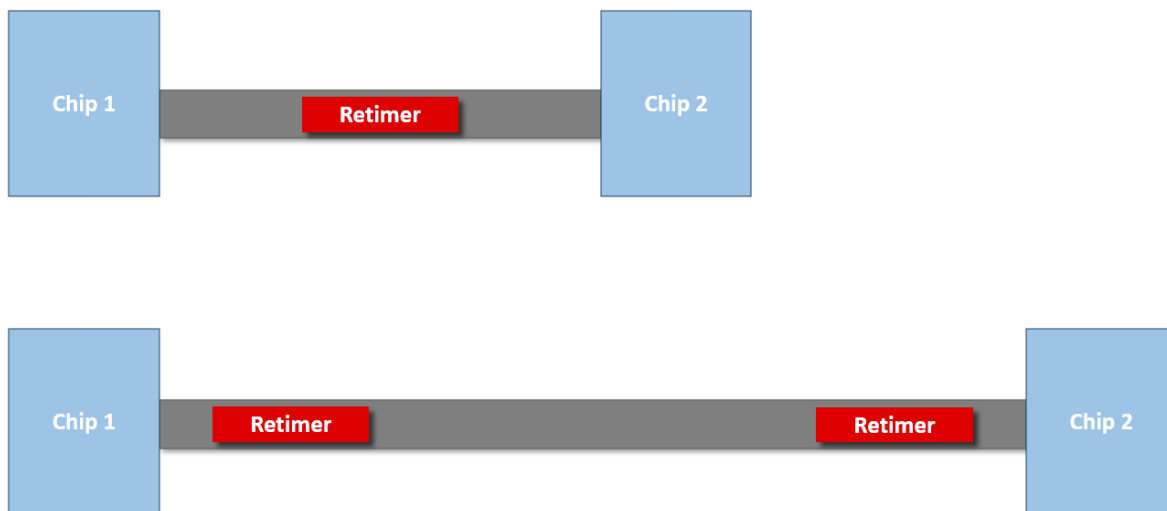
limitations from having to route numerous data lines next to each other (in parallel) along with clock signals. Ex-1020, 000011-000012. Parallel signals needed to be synchronized so that all signals and their shared clock arrived at the receiver within a certain window, which became increasingly difficult as bus widths and clock speeds increased. *See* Ex-1020, 000011-000014. Serial communications techniques avoid these issues while saving pin count on the integrated circuit (“IC”).

5. By the 2000-2005 timeframe, computer bus and networking protocols had largely transitioned to serial connections, where parallel data within a chip was converted into a serial format, sent over a serial link, and then converted back into a parallel format. This process of serialization and then de-serialization, called “SerDes,” was used in various standardized bus and networking protocols. For example, the parallel ATA standard was replaced by Serial ATA, or “SATA” for short. The parallel PCI standard was replaced by a serial version called PCIe. The Universal Serial Bus (“USB”) replaced various parallel interfaces. And the ubiquitous Ethernet standard had long been implemented using serial cables and CAT-5 plugs. Ex-1020, 000058-000061.

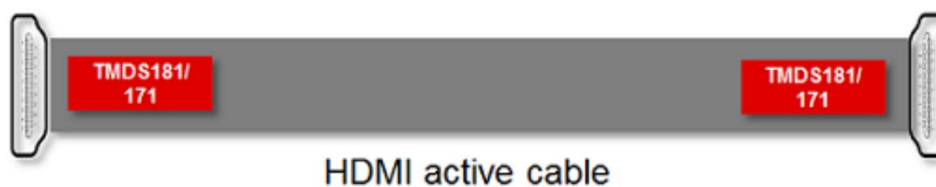
A. Active Cables

6. In serial communications, retimers were often used to extend the length and bandwidth of serial communications links (Ex-1021, 000001 (“Retimers and redrivers have enabled longer physical channels in servers and storage systems

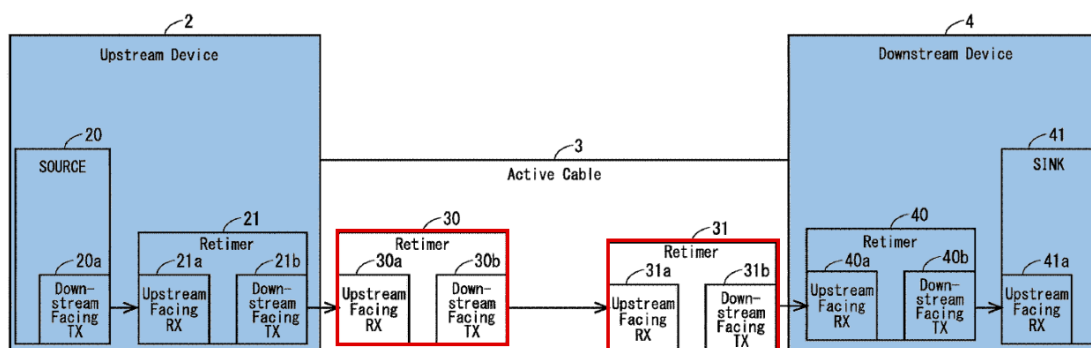
since Peripheral Component Interface Express (PCIe®) 3.0 specification was first introduced almost 10 years ago.”)) by recovering digital data from the channel and re-modulated them, eliminating noise from the earlier segment of a link and renewing the signal for the next. Ex-1007, ¶¶15-16, ¶202. I prepared the following diagrams to illustrate how retimers were used to extend the length of channels between chips.



7. Active electric cables extended the length of cables by incorporating retimers in the plugs at each end of a cable. Ex-1010, ¶2 (“A retimer is used to extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the retimer.”), ¶13 (“an active cable may have two retimers on both ends of the cable”). For example, Texas Instruments (“TI”) offered a retimer chip (TMDS181) that was included in active HDMI cables. Ex-1026, Fig.1:



Active electric cables commonly included a retimer at each end of the cable. Ex-1010, Fig.1:¹



By the early-to-mid 2010s, active electric cables were used for a variety of common data transmission standards, including DisplayPort, PCIe, USB, and Ethernet.

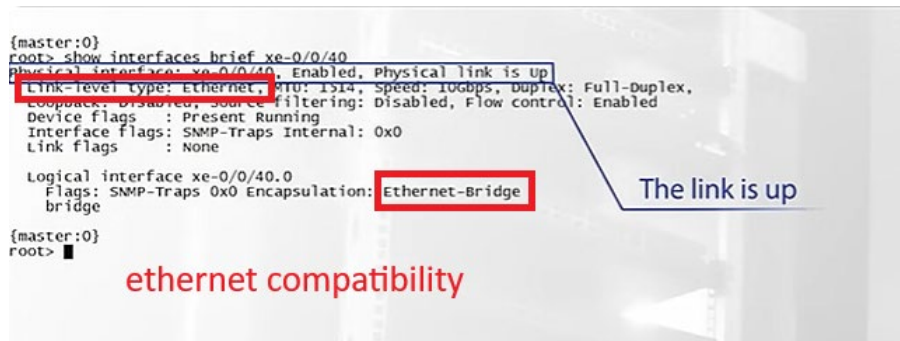
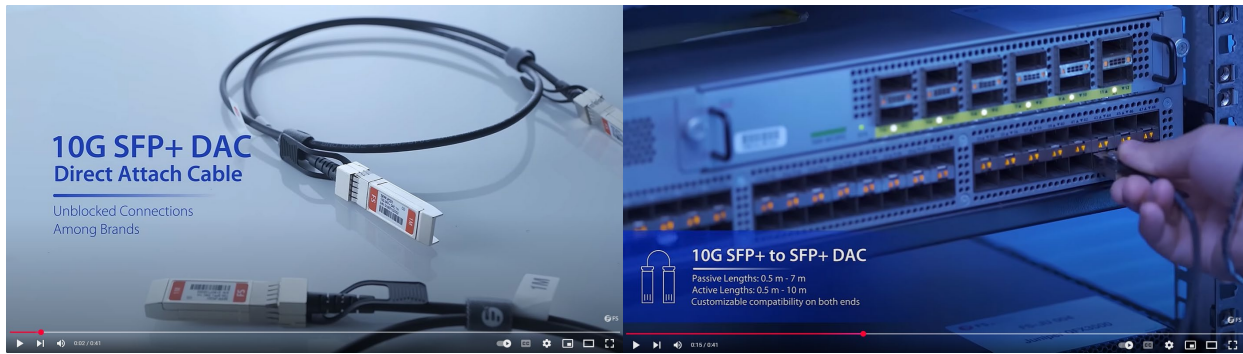
8. Ethernet was a popular networking standard going back to the 1990s. By the 2010s, Ethernet was widely used for high-speed serial communications in enterprise and data-center networks, scaling from 1 Gigabit Ethernet (GbE) in the early 2000s to the widespread adoption of 10 GbE by 2010. To meet industry demand for higher speeds and longer reach, manufacturers introduced active Ethernet cables, which integrated electronics such as retimers within the cable

¹ All emphasis and annotations added unless stated otherwise.

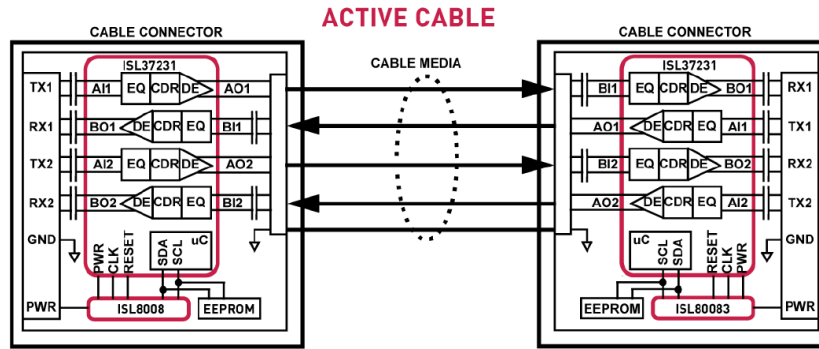
assembly. Active Ethernet cables have been on the market from a variety of vendors by at least 2014. *See* Ex-1011 (datasheet for TE SFP+ cables, supporting 1 and 10 Gigabit Ethernet); Ex-1012, 000001, 000003, 000004-000005, 000008-000009 (various Cisco transceiver and cable modules supporting 40 Gigabit Ethernet). Petitioner Marvell is a leading supplier of retimer/transceiver chips for active Ethernet cables.

9. Some active Ethernet cables, shown below, use the SFP+ form factor, with a transceiver in a module at both ends. Ex-1019,² Video Description (“10G SFP+ direct attach copper cable ... or 10G SFP+ DAC cable assembly, is a twinaxial cable assembly that has a length of copper cable and terminates with SFP+ connector modules on either end.”), 000001, 000002, 000004:

² I created exhibit 1019 by visiting <https://youtu.be/IeI2DIE4QhQ?si=MERK3x9eFo6FLkUG> and taking screen captures at times 0:02, 0:15, and 0:29. I added annotations in red to the screen capture at time 0:29.



10. One high-profile active cable, called Thunderbolt, came from a collaboration between Apple and Intel. Apple developed and marketed the cable (Ex-1014, 000002; Ex-1013, 000001-000002), while Intel provided the port and retimer architectures used in the connector assemblies at each end of the cable. Ex-1016, 000001-000002; Ex-1015, 000003 (“Thunderbolt port and controller specification are entirely Intel’s”). Mac computers included Thunderbolt ports starting in 2011 (Ex-1013, 000001), and other vendors began providing Thunderbolt solutions by 2013. Ex-1009, 000001 (describing Intersil retimer chip for Thunderbolt), Ex-1008, 000003-000005 (discussing ISL37231 retimers in Thunderbolt connectors).



B. Pre-Equalization

11. As connection protocols shifted to serial links, the protocols adopted established serial communications techniques. One widely used technique was pre-equalization, commonly found in active cables and retimers.

12. Pre-equalization was a well-established serial communication technique. By 2018, and for many years prior, it was one of several common components taught in undergraduate courses on high-speed serial communications. Ex-1020, 000020-000024. Textbooks on serial communications typically included a chapter or section explaining pre-equalization. Ex-1020, 000020-000024; Ex-1017, §1.1.1 at 000025-000027.

13. Pre-equalization was performed at the transmitter to adjust the signal prior to the signal being sent over the channel, to compensate for anticipated signal loss. Equalization was also performed at the receiver to adjust for channel losses after the signal crossed the channel. The use of pre-equalization at the transmitter and equalization at the receiver allowed robust and reliable transmission over noisy channels and at high data rates. Ex-1020, 000020-000024.

14. Because a channel affects different frequencies unevenly, pre-equalization boosts the signal at frequencies where greater losses were expected. This compensation counteracted channel losses, so that after traversing the channel, the received signal more closely matched the original. The resulting signal at the receiver had a signal spectrum more constant over frequency, resulting in less waveform distortion and reduced inter-symbol interference (“ISI”). Pre-equalization was most commonly performed using “pre-emphasis” to boost certain frequencies; it is illustrated below, where the red boxes show the original waveform with and without pre-emphasis, and the waveforms on the right show the result after passing through the channel. Ex-1020, Figs. 1.9-1.10 at 000021:

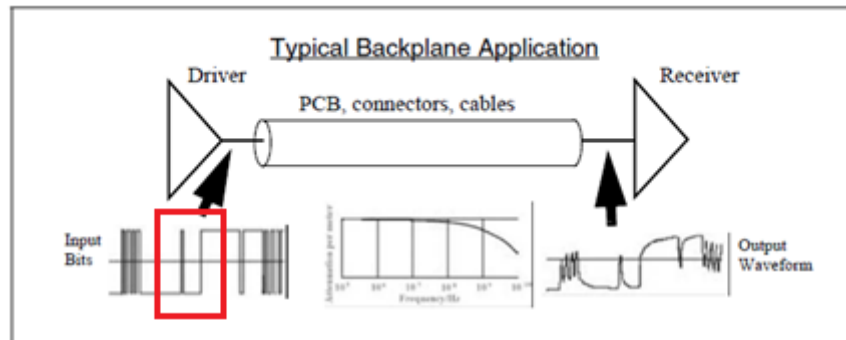


Fig. 1.9 Signal distortion for a typical channel application

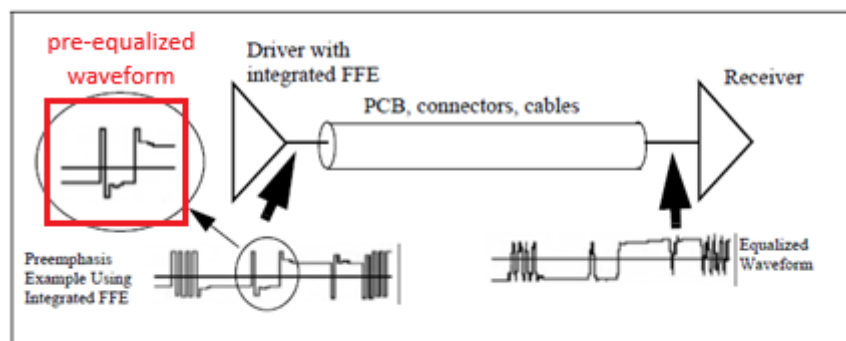


Fig. 1.10 Typical channel application with equalization at the transmitter

15. Pre-equalization at transmitter is often implemented using a finite impulse response (“FIR”) filter. An FIR filter essentially performs a weighted sum between adjacent data symbols by multiplying coefficients with adjacent data (also called “taps”) and summing the results. For pre-equalization, the FIR filter coefficients are chosen to boost frequencies that the channel diminishes. This way, when the signal goes through both the filter and the channel, their effects cancel out, helping the signal reach the receiver closer to its original form. Typically, the FIR filter provides more signal gain at higher frequencies (so-called pre-emphasis) or attenuates the signal more at lower frequencies (so-called de-emphasis) to compensate for the frequency-dependent channel loss. Ex-1020, 000020-000021; Ex-1017, 000025-000027.

16. In the area of wireline communication, data (typically in the form of digital binary bits: “0” or “1”) is conveyed from one end (transmitting end) to the other end (receiving end) via a physical channel, such as a cable or a trace on a printed circuit board (“PCB”). For example, “0” can be conveyed using low voltage, while “1” can be conveyed using high voltage. If the physical channel is perfect without any loss, the receiver simply needs to detect whether the received voltage level is above or below a certain threshold to recover the transmitted bits. However, in practice, physical channels are not perfect and include various loss mechanisms, such as parasitic resistance, capacitance, skin effects, dielectric loss,

connectors, vias, etc., which attenuate and distort signals transmitted through the physical channel.

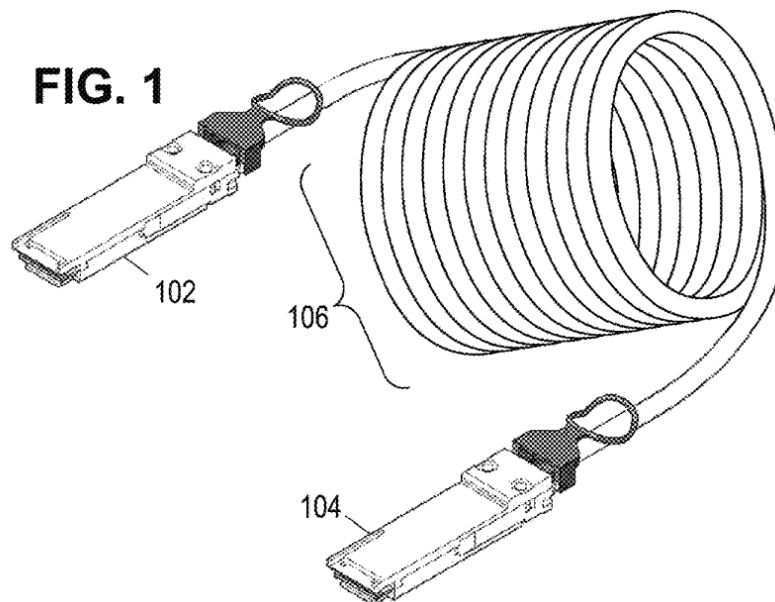
17. If such a channel loss were strictly constant over frequency, the lost signal energy will result in smaller signal swing at the receiving end but the transmitted signal waveform can be retained. However, in reality, the channel loss is frequency dependent and can cause distorted signal waveform at the receiving end and interference between data symbols, resulting in inter-symbol interference (“ISI”). Ex-1020, 000072 (“This type of jitter [DDJ], also known as pattern dependent jitter or intersymbol interference (ISI), is observed on nonclocklike waveforms since the frequency spectrum of such signals is continually changing.” “[H]igh baud rates still expose these signals to a significant amount of signal attenuation resulting in DDJ contribution.”), 000071, 000073-000075. The ISI effect can cause the received waveform smeared to anywhere between the high and low voltage. Sometimes, the supposedly high voltage may be attenuated to a much lower voltage. As a consequence, the receiver is unable to detect the intended data reliably and can cause bit error (i.e. detected as “0” while the transmitted data is “1” and vice versa), often characterized as bit error rate (BER).

18. It was common for the coefficients of equalization and pre-equalization filters to start with initial values based on a pre-determined, estimated channel response and subsequently updated during operation based on the actual

channel response. Ex-1020, 000020-000021 (discussing an FFE implementation of an FIR filter: “FFE tap weights are determined for many applications by design and coded as fixed values within system software, however, there are some applications where FFE tap weights are adjusted dynamically by the protocol based on signal characteristics at the receiver.”). “[P]re-programmed or pre-set” equalizer coefficients were saved in various forms of nonvolatile memory during manufacturing. Ex-1005, 7:18-33.

II. THE '233 PATENT

19. The '233 patent is directed to an active electric cable:



20. According to the patent, ever-higher data rates caused “increased channel attenuation and dispersion even as the equalizers are forced to operate at faster symbol rates.” Ex-1001, 1:15-19. “For distance spans of no more than 2 meters, attenuation is reasonably limited such that passive copper cable... can be

employed.” Ex-1001, 1:25-28. For larger distance spans, data centers relied on active cable designs, including “[a]ctive ethernet cable (AEC)” products that extended range with “hard-wired data recovery and remodulation (DRR) chips in the cable connectors.” Ex-1001, 1:25-36. Therefore, the ’233 patent does not purport to invent active cables; it admits they were used in the background art.

21. According to the patent, there was a need for increased levels of equalization as cable lengths extended. Ex-1001, 1:37-40. The ’233 patent purports to address this need by using pre-equalization, “employing preset transmit-side equalization to provide enhanced performance and/or to reduce receive-side equalization requirements.” Ex-1001, 1:44-48, 1:61-63 (“The first and second DRR devices provide pre-equalization...”).

22. However, as explained above, pre-equalization was a textbook component of serial communication systems. Years before the ’233 patent, the Petitioner’s own prior art included pre-equalization in active cables (Lugthart). Prior art from Apple and Intel likewise taught pre-equalization in active cables (Ground 4), and the use of preset equalizer coefficients was both known and trivial. *See, e.g.*, Ex-1005, 7:18-33; Ex-1004, 29:21-28, 23:59-64, 9:39-49.

A. Prosecution History

23. The ’233 patent was granted without any Office Rejections. Ex-1002, 000563. In the Notice of Allowance, the Examiner stated that the prior art does not

teach or suggest limitations [1f], [8f] and [15c]: first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories. Ex-1002, 000568-000571.

24. After the initial allowance, the Applicant filed a Request for Continued Examination (RCE) to submit an Information Disclosure Statement citing four Office communications from two separate patent applications (Application Nos. 16/539, 910 and 16/541094). Ex-1002, 000591-000596. In less than a month, the Examiner issued a second Notice of Allowance without addressing the new information disclosed in the IDS, indicating that “[n]o new art is cited.” Ex-1002, 000668-000673. The Examiner again concluded that the prior art did not teach limitations [1f], [8f], and [15c]. Ex-1002, 000671.

25. None of the references used in the invalidity grounds discussed below were considered during examination. These references are not listed on the face of the patent, nor have I seen them addressed in the prosecution history.

B. Priority Date

26. The '233 Patent issued from an application filed November 27, 2019. The file history references Chinese Application No. CN201910542576.3 and states that the effective filing date is July 1, 2019. Ex-1002, 000529-000530. However, the issued patent does not contain any reference to CN201910542576.3.

27. For purposes of this Declaration, I have analyzed obviousness as of June 21, 2019. I do not offer an opinion as to whether the '233 patent is entitled to this priority date. My invalidity opinions would not change if a later date was determined to be the appropriate because the prior art relied upon in this declaration would still be prior art.

C. Challenged Claims

28. I understand that Petitioner is challenging the validity of claims 1-20 of the '233 patent in the Petition for Inter Partes Review to which this declaration will be attached. Those claims are reproduced in Appendix 3. While this Petition and declaration are directed to the challenged claims, I have considered all claims 1-20 of the '233 patent, as well as portions of the '233 patent prosecution history in forming my opinions.

III. FIELD AND LEVEL OF ORDINARY SKILL IN THE ART

29. I have analyzed the '233 patent and determined that the field of the '233 patent is high-speed communications. The '233 patent seeks to addresses challenges that arise in this domain. It begins by describing its background in terms of high data rate communications over a variety of physical mediums including twinaxial cable, fiber optics, and electrical backplanes, and then recognizes the demand for “ever-higher data rates.” Ex-1001, 1:16. The patent acknowledges that active Ethernet cables are used to provide “high-bandwidth data transport over

distance” (Ex-1001, 1:25–36) and proposes improving the performance of high-bandwidth serial communications by implementing pre-equalization at the transmitter, thereby mitigating the receiver power burden. Ex-1001, 1:38–48. The ’233 patent embodiments describe numerous examples of high-speed communications. For example, the specification explains that in Figure 1, the “...outbound data streams may be expected to be compliant with the relevant standard (e.g., the Ethernet standard for 400 Gbps)...” Ex-1001, 3:63-4:1, Fig. 1. Similarly, in Figure 2, the end connector 100 “may be designed for sending and receiving a 200 Gbps Ethernet data stream” and each of the split-end connectors 101-104 “may be designed for sending and receiving a 50 Gbps Ethernet data stream.” Ex-1001, 4:23-45, Fig. 2. In short, the ’233 patent is directed to the field of high-speed communications.

30. In determining the characteristics of a hypothetical person of ordinary skill in the art (“POSITA”) of the ’233 patent at the time of the claimed invention, I considered several things, including various prior art techniques relating to the field, the type of problems that such techniques gave rise to, and the rapidity with which innovations were made. I also considered the sophistication of the technologies involved, and the educational background and experience of those actively working in the field at the time. I also considered the level of education that would be necessary to understand the ’233 patent. Finally, I placed myself

back in the relevant period of time and considered the engineers and programmers that I have worked with and managed in the field.

31. I came to the conclusion that a person of ordinary skill in the field of art of the '233 patent would have been a person with a bachelor's degree in electrical or computer engineering with at least three years of experience in the field (explained above). A person with less practical experience but more relevant education may also meet this standard.

32. In the relevant timeframe (*see* above §II.C), a POSITA with the above-described level of skill would have been able to:

- Understand common components in high-speed serial communications systems, including but not limited to transceivers, equalization, clock and data recovery, PCS, pre-equalization, FIR filters, mixed-signal circuits, and digital-analog conversion (or vice versa);
- Design high-speed serial communication systems;
- Design active electric cables;
- Design various equalization and pre-equalization filters, including by using an FIR filter and customizing the tap coefficients of the filter;
- Program a DSP to perform common functions in transceivers; and

- Implement protocols for calibrating and setting equalization parameters.

IV. CLAIM CONSTRUCTION

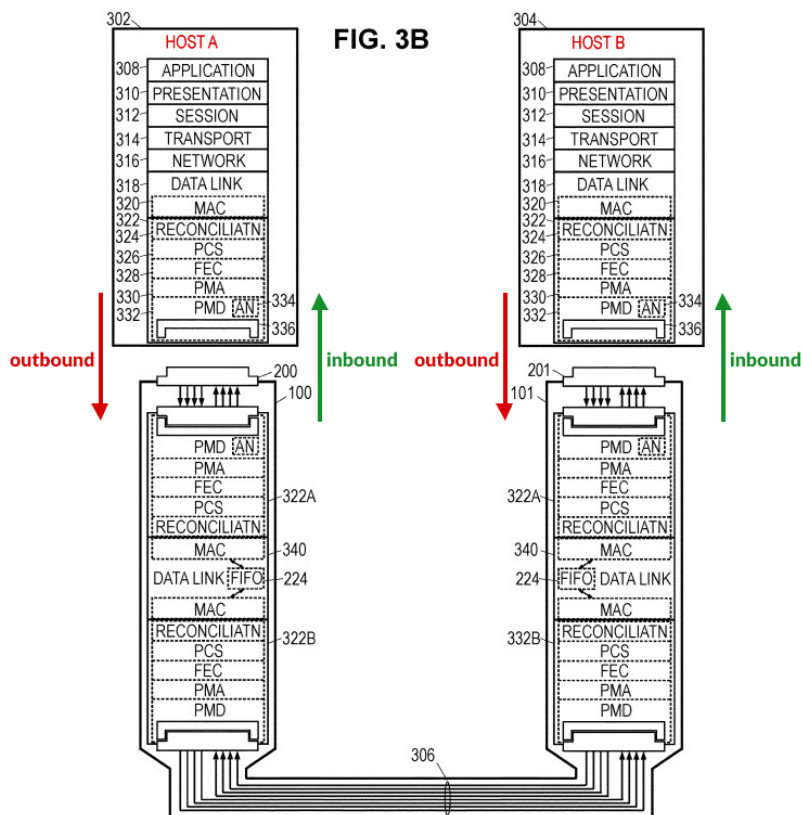
33. For purposes of this inter partes review, I have considered the claim language, specification, and portions of the prosecution history, to determine the meaning of the claim language as it would have been understood by a person of ordinary skill in the art at the time of the invention. The “plain and ordinary meaning” or *Phillips* standard has traditionally been applied in district court litigation, where a claim term is given its plain and ordinary meaning in view of the specification from the view point of a person of ordinary skill in the art.

34. I have applied the *Phillips* standard in my analysis. Unless otherwise stated, I have applied the plain and ordinary meaning to claim terms.

A. “inbound”/“outbound” (claim 1)

35. The '233 patent defines the “inbound” and “outbound” direction from the perspective of the host. For example, the '233 patent explains that the transceivers perform CDR and re-modulation “not only of the inbound data streams to the host interface as they exit the cable, but also of the outbound data streams from the host interface entering the cable.” Ex-1001, 3:57-60, 4:46-52, Figs. 3A-3B. That is, data streams exiting the cable and transmitted to the host interface are considered “inbound,” while data streams transmitted to the cable

from the host interface are considered “outbound.” Ex-1001, 3:57-60, 4:46-52, Figs. 3A-3B.



V. INVALIDITY GROUNDS

36. Based on my review and analysis of the materials cited herein, my opinions regarding the understanding of a POSITA in the relevant timeframe (*see* above §II.B), and my training and experience, it is my opinion that the Challenged Claims are obvious in view of the Grounds below. The reasons for my conclusions are explained more fully below.

Grounds	Claims	Statutory Basis	Prior Art
1	1, 6, 8, 13, 15	§103	Lugthart

2	1-20	§103	Lugthart and Gorecki
3	7, 14, 20	§103	Lugthart, Gorecki, and Samaan
4	1-20	§103	Cornelius, Samaan, and Gorecki

A. Grounds 1-3: Lugthart-based grounds

37. For Ground 1, Lugthart teaches an active cable with all limitations of the independent claims. For Ground 2, Gorecki teaches several limitations of dependent claims and, to the extent the Patent Owner argues that Lugthart does not explicitly disclose storing values in nonvolatile memories (limitations [1f], [8f] and [15c]), Gorecki teaches this. The motivation to combine and reasonable expectation of success are explained in more detail below. *See* below §V.A.3.[1f] (Motivation to Combine subsection).

38. For Ground 3, Samaan provides an additional teaching for a set of dependent claims. Samaan is introduced in §V.B.2.

1. U.S. Patent 9,882,706 (“Lugthart”) (Ex-1004)

39. I have reviewed the Lugthart reference. Lugthart was filed on December 28, 2016 and issued on January 30, 2018, claiming priority to December 27, 2013. Therefore, Lugthart is prior art under post-AIA §102(a) before June 21, 2019. *See* below, Appendix 4 (Understanding of the Law).

40. Lughart is directed to an active cable with transceivers at each end that transmit and receive signals to each over a cable. Ex-1004, Fig. 2A; 6:65–7:3; 14:7–31.

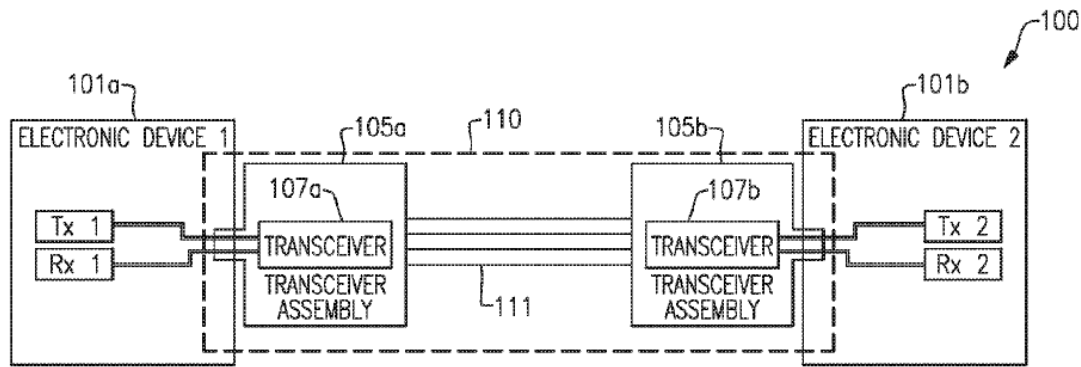


FIG. 2A

41. The transceivers use an FIR filter to perform “output pre-emphasis” on signals before transmission “to compensate for channel losses.” Ex-1004, 29:21-28, 23:59-24:2, Figs. 1A, 4A-4B.

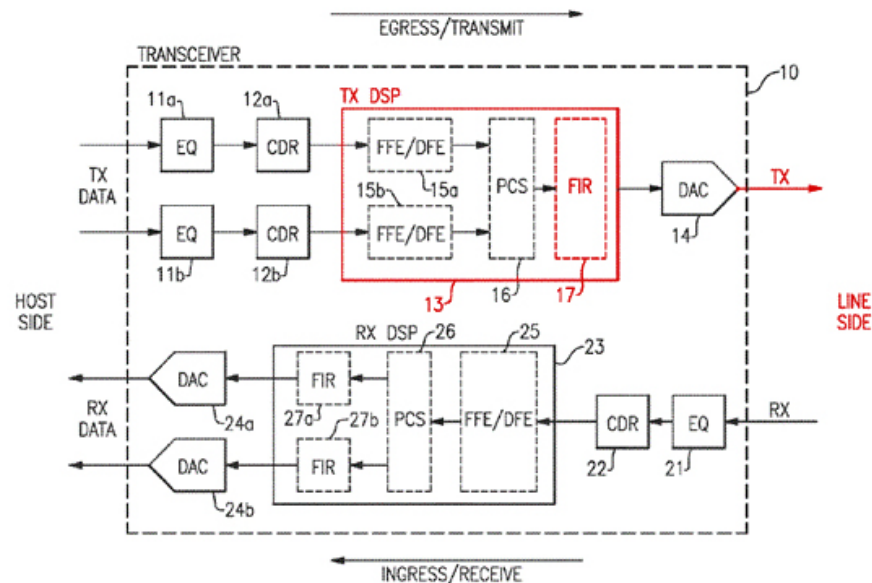


FIG. 1A

42. Lugthart is analogous art to the '233 patent because it is in the same field of endeavor (high-speed communications). *See* above §III. Lugthart is directed to “[s]ystems and methods for high speed communications” to “achieve reliable high-speed point-to-point communication between different electronic devices, computing devices, storage devices and peripheral devices.” Ex-1004, Abstract, 1: 36-37 (Field of Lugthart), 3:12-16, 4:10-12, 6:55-7:5, 14:29-31. The objective of Lugthart is to “establish high-speed point-to-point links” between different electronic devices, computing devices, storage devices and peripheral devices. Ex-1004, 47:24-27. Lugthart is also reasonably pertinent to the problem addressed by the '233 patent because it teaches equalization techniques in the transmitter and receiver for high-speed serial communications to account for signal degradation caused by channel loss.

2. U.S. Patent 7,233,617 (“Gorecki”)(Ex-1005)

43. I have reviewed the Gorecki reference. Gorecki was filed on April 10, 2003 and issued on June 19, 2007, claiming priority to October 11, 2002. Therefore, Gorecki is prior art under post-AIA §102(a) before June 21, 2019. *See* below, Appendix 4 (Understanding of the Law).

44. Gorecki aims to enhance high-speed digital communications over backplanes and cables. Ex-1005, 1:12-17, Abstract. Gorecki employs “equalization circuitry” at the transmitter side “to compensate for bandwidth limitations and

reflections in high-speed digital communication systems.” Ex-1005, 3:11-15. In particular, the “equalization circuitry” includes multiple tap coefficients stored in memory, including “ROM, PROM, EPROM, [or] EEPROM.” Ex-1005, 7:18-26.

45. Gorecki is analogous art to the ’233 patent because it is in the same field of endeavor (high-speed communications). *See* above §III. Gorecki is directed to enhancing the performance of “high-speed communication” over a cable and discloses a “high-speed digital communication system” including a transmitter and a receiver. Ex-1005, Abstract, 3:11-15, 6:3-22, 8:1-4. Fig. 3. Gorecki is reasonably pertinent to the problem addressed by the ’233 patent, which recognized a problem where “equalizers are forced to operate at faster symbol rates” and the need for “increasing levels of equalization” posed problems at the receiver. Ex-1001, 1:15-20, 1:36-40. The ’233 patent addresses this problem with “preset transmit-side equalization to provide enhanced performance and/or to reduce receive-side equalization requirements.” Ex-1001, Abstract, 1:44-50. Gorecki recognizes similar challenges where “increase[s] in data rate[s]” make it more difficult to recover the transmitted signal. Ex-1005, 1:17-24. And Gorecki provides pertinent solutions for equalizers “in wired type environments” (Ex-1005, 1:12-17), where “a transmitter includes equalization circuitry to compensate for bandwidth limitations and reflections in high-speed digital communication systems.” Ex-

1005, Abstract. This includes the use of “pre-set” coefficients in nonvolatile memories. Ex-1005, 7:18-33. Therefore, Gorecki was reasonably pertinent.

3. Independent Claim 1

46. As an initial matter, for each of the below limitations, the “first” and “second” designations can be swapped between elements at one end of the active cable versus the other. As will be explained below, Lugthart’s cable design is symmetric to support bi-directional communication; each side has identical components and operation.

[1pre] A cable that comprises:

47. I understand that a preamble generally does not state a claim limitation. Nonetheless, it is my opinion that Grounds 1 and 2 teach it.

48. For example, Lugthart describes “[a] high-speed communication link” that “include[s] a cable,” where “a first electronic device” and “a second electronic device” are “electrically connected to one another via a cable.” Ex-1004, 6:65-7:3, 3:12-16, 14:7-15, 4:10-13, 10:4-22, Figs. 2A, 3A-3B, 4A. Lugthart further specifies that “[t]he cable can be implemented in a wide variety of ways,” and explains that one such implementation would be “an electrical cable including one or more pairs of differential micro coaxial cables or conductors.” Ex.1004, 6:65-7:5.

49. The cable further includes the elements discussed below for limitations [1a]-[1f].

[1a] a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;

50. Lugthart teaches a **first DRR device**. For example, Lugthart discloses “a pair of transceivers provided at respective ends of the cable.” Ex-1004, 6:65-7:3, Figs. 2A, 4A.

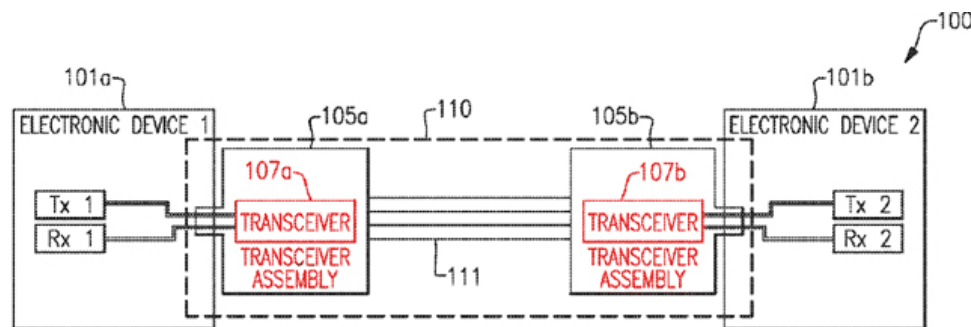


FIG. 2A

51. Lugthart details transceiver internals in Figure 1A, and then illustrates those details in context in Figure 4A, which combines the transceiver details of Figure 1A with the active cable shown in Figure 2A. I have annotated the figures to illustrate this relationship. Ex-1004, Figs. 1A, 2A, 4A-4B, 7:67-10:22, 19:34-64. As will be explained below, either transceiver would be a first DRR device.

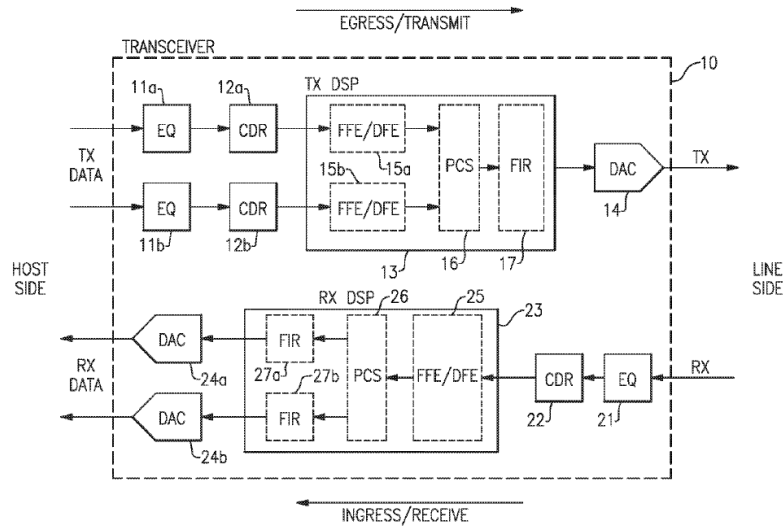


FIG. 1A

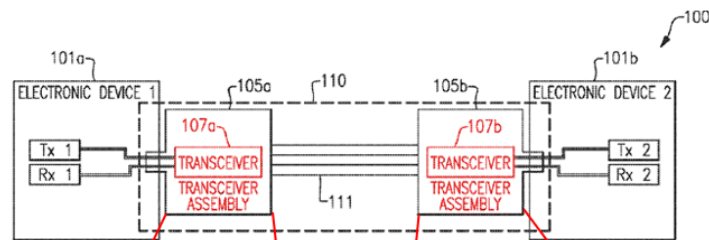


FIG. 2A

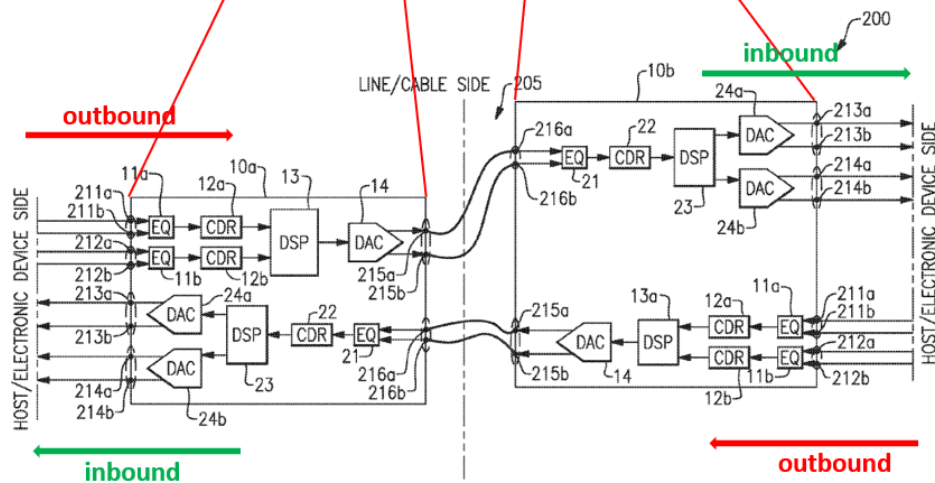


FIG. 4A

52. Each transceiver includes “a first transmit path clock and data recovery (CDR) circuit” and “a second transmit path CDR circuit[.]” Ex-1004,

7:66-8:7, 1:63-2:3, 9:26-37, 21:35-46, 33:23-28, Figs. 1A, 4A-4B, 8. These CDR circuits “perform clock and data recovery operations.” Ex-1004, 9:26-28. For example, the two CDR circuits “recover data in data streams generated by...transmit path equalizers.” Ex-1004, 9:34-37.

53. After data recovery, the transceiver further performs remodulation, including for example using PAM-4 modulation over the cable. Lugthart describes a “multi-level modulation encoding” process in which “each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable,” or “vice versa.” Ex-1004, 7:13-33, 8:48-60, 15:64-16:10, 23:44-58, 24:17-23, Figs. 1A, 4B. In other words, Lugthart’s transceiver recovers data from an NRZ signal from the host and then remodulates the recovered data signal into PAM-4 over the cable (for the outbound direction), or vice versa for the inbound direction to the host. Ex-1004, 7:13-33, 8:48-60, 15:64-16:10, 23:44-58, 24:17-23, Figs. 1A, 4B.³ Therefore, Lugthart’s transceiver performs remodulation by converting a data signal for transmission over a communications channel (e.g., the cable in the outbound direction or path to the host in the inbound direction).

³ Likewise, in the ’233 patent embodiments, the DRR devices “convert[] 1 lane of PAM4 symbols into 2 lanes of NRZ symbols, and vice versa.” Ex-1001, 4:43-45.

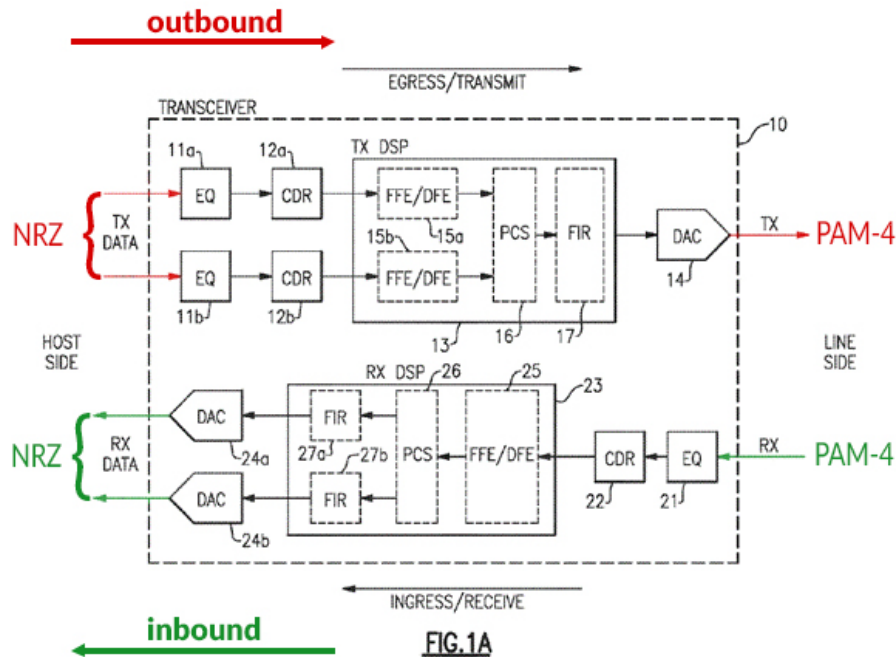


FIG.1A

54. Lugthart further explains the process of data recovery and remodulation in Figures 6A-6B. In Figure 6A, the transceivers first “recover[] digital clock and digital data signals from the converted digital signal” as shown in block 303, and then “convert[] the multiplexed digital signal to an analog differential signal having a suitable modulation format[.]” Ex-1004, Figs. 6A-6B, 30:20-31:22.

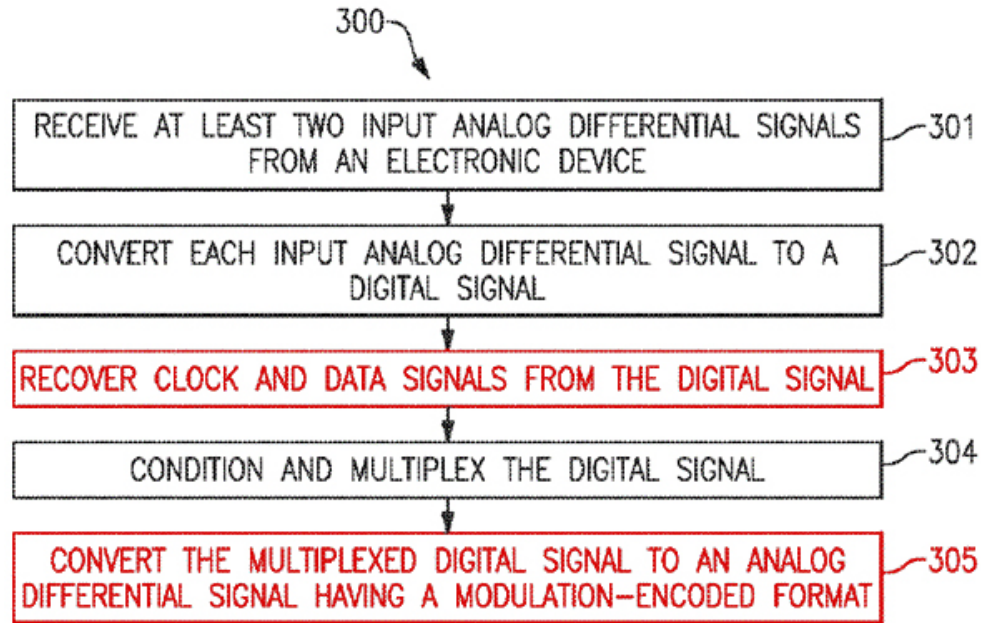
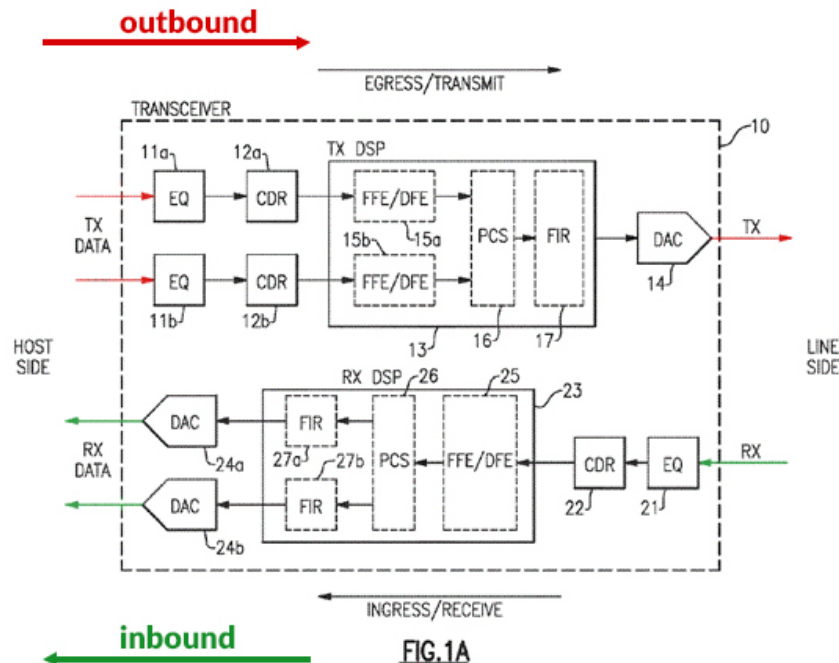


FIG.6A

55. The DRR device (e.g., the transceiver) **exchanges inbound and outbound multi-lane data streams**. Each transceiver includes an “egress/transmit path” “capable of receiving...signals on the host side and multiplexing these signals...for transmission to the line side over the cable.” Ex-1004, 8:48-60, 15:64-16:3, 19:56-64, Figs. 1A, 2A, 4A. This means that outbound data streams from the host are received by the transceiver and transmitted over the cable using its egress/transmit path. From the host’s perspective,⁴ this constitutes an exchange of an outbound data stream with the transceiver. Lugthart also includes a path going the other way through the cable: each transceiver includes an “ingress/receive

⁴ The ’233 patent defines inbound/outbound from the host’s perspective. *See* claim construction §IV.A.

path” that is “capable of receiving ...on the line side and de-multiplexing this signal...for communication to the host side.” Ex-1004, 8:48-60, 16:11-15, 19:56-64, Figs. 1A, 2A, 4A. In other words, inbound data streams heading from the cable to the host are received by the transceiver and transmitted to the host via the ingress path. From the host’s perspective, this constitutes an exchange of inbound data with the transceiver.



56. The inbound/outbound streams are multi-lane data streams. Lugthart describes its transceiver having more than one lane for host-side data streams, including “two” or “four host-side 10 Gbps NRZ data streams” in each direction. Ex-1004, 7:21-30, 13:13-48, 23:50-58, Figs. 1A, 4B. Therefore, the transceiver exchanges multi-lane data streams in each direction at the host interface.

57. The DRR device exchanges the inbound/outbound data streams **with a first host interface port via a first end connector plug** (e.g., at one end of the cable). For example, Lugthart also describes the transceiver assembly as a pluggable module, where “[t]he first pluggable module can include a first transceiver[.]” Ex-1004, 4:10-14, Fig. 2A, 15:30-31 (each transceiver “enclosed in a packaging”). The pluggable module exchanges “host-side signals[.]” Ex-1004, 4:13-19. Each transceiver assembly “has an input port that is configured to mechanically and electrically connect...to a corresponding port or other interface on the respective electronic device[.]” referring to the host device. Ex-1004, 14:14-15 (referring to electronic devices 101a and 101b as “host devices”), Fig. 2A, 15:42-47.

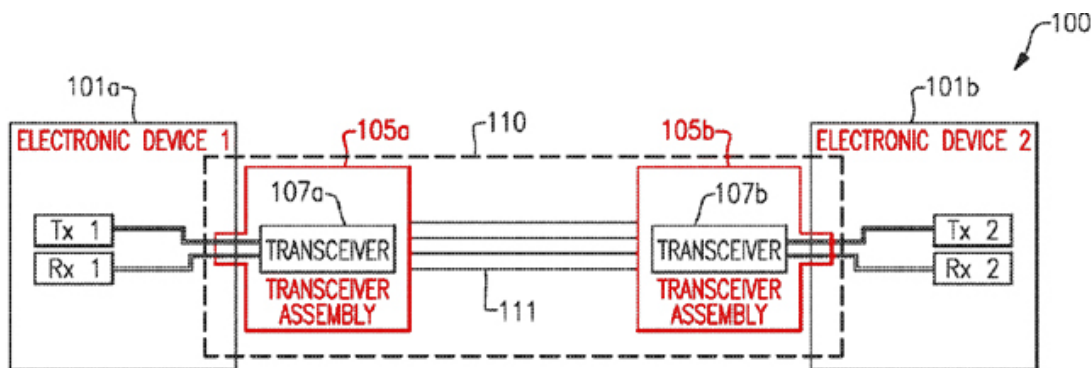


FIG.2A

58. Lugthart teaches exemplary form-factors for the connector plugs at the ends of the cable: the transceiver assembly’s “input port can include a connector,” such as “small form-factor pluggable (SFP), enhanced small form-

factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP).” Ex-1004, 15:47-52. These pluggable connectors allow the transceiver assembly’s input port to be connected to the host interface port “in a releasable fashion.” Ex-1004, 15:42-52.

59. Accordingly, Lugthart teaches that each transceiver assembly (at each end of the cable) has an end connector plug that connects to an interface port on the host mechanically and electrically. One (first) transceiver exchanges inbound and outbound data streams with its host using the (first) host interface port via the (first) end connector plug at that end of the cable; the other (second) transceiver does the same with its host using the (second) host interface port via the (second) end connector plug at the other end of the cable. Ex-1004, 4:10-14, 15:42-52, 8:48-60, 15:64-16:3, 19:56-64.

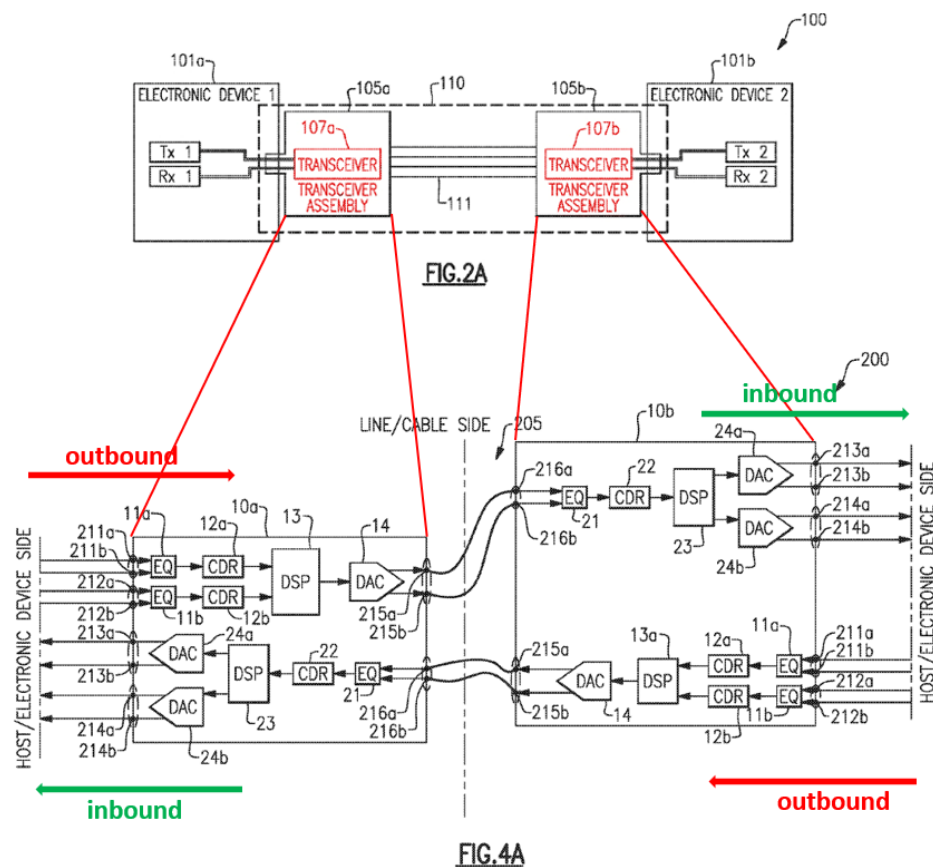
60. For at least these reasons, Lugthart teaches limitation [1a].

[1b] second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug

61. Limitation [1b] mirrors [1a] and differs only by changing “first” to “second.”

62. Lugthart teaches a cable with two symmetric DRR devices (e.g., two transceivers, one at each end of the cable). As explained above, Lugthart describes that each cable has “a pair of transceivers provided at respective ends,” and the

functionalities described apply to both transceivers. Ex-1004, 6:65-7:3, 7:13-20 (“each transceiver is capable of” performing relevant signal transmission and conversion functions), Figs. 1A, 2A, 4A. This is further illustrated in Figures 2A and 4A, which depicts a cable structure with two identical transceivers located at opposite ends. Ex-1004, Fig. 1A, 2A, 4A, 14:7-31, 19:34-40 (explaining that the first and second transceivers 10a and 10b are both implemented “in a manner similar to that of the transceiver 10 of 1A.” Ex-1004, 19:34-40.



63. Because Lugthart teaches a symmetric cable with two DRR devices, either DRR device would be the first DRR device recited in [1a]; the other DRR device would be the second DRR device recited in [1b], for the same reasons

explained previously. Ex-1004, 6:65-7:3, 7:13-20, 14:7-31, 19:34-40, Figs. 1A, 2A, 4A. The analysis from [1a] also applies to [1b] and is incorporated here. *See* above §V.A.3[1a]. The interface port and plug for the second transceiver, at its end of the cable, would be the second host interface port and second end connector plug.

64. For at least these reasons, Lugthart teaches limitation [1b].

[1c] electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,

65. Lugthart teaches **electrical conductors connecting the first and second DRR devices** (e.g., transceivers). For example, Lugthart discloses an active cable that includes “electrical conducting lines 111,” which connect the two DRR devices located at opposite ends of the cable. Ex-1004, 16:11-15, 14:29-42, 19:34-48, Figs. 2A, 4A.

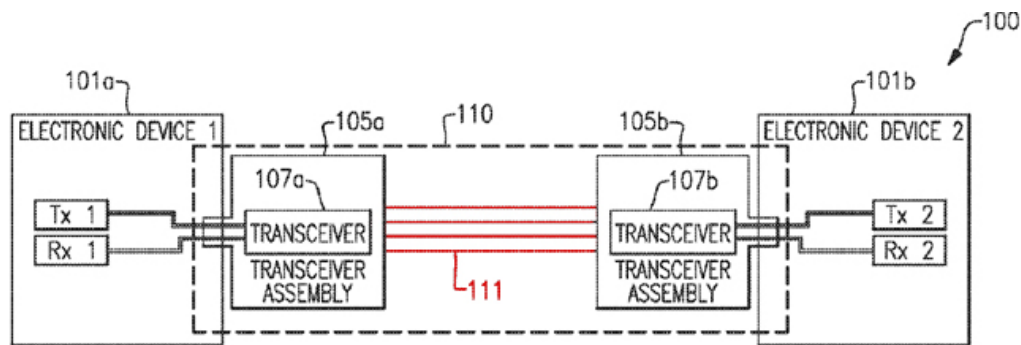


FIG. 2A

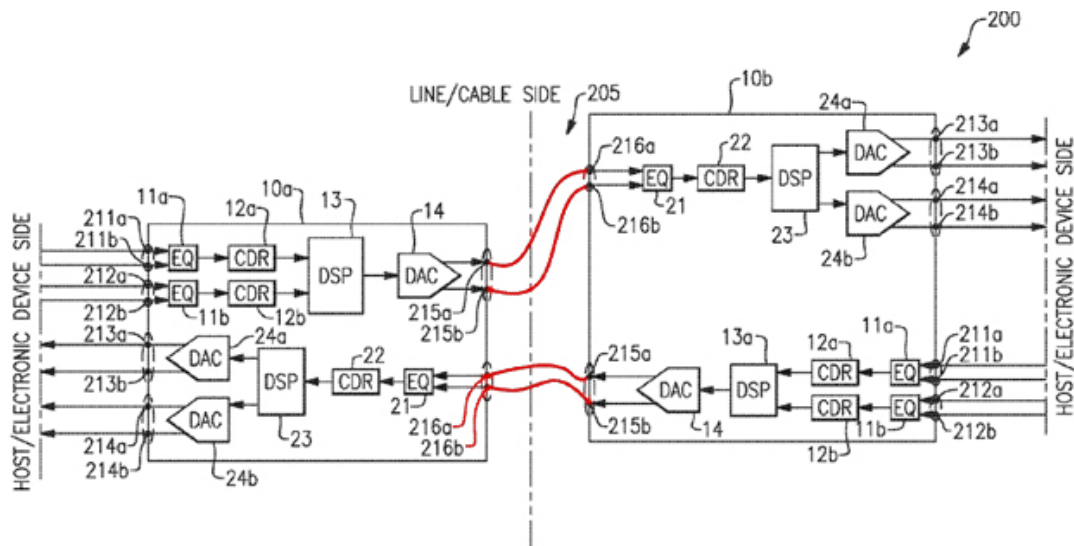


FIG. 4A

66. The cable connecting the two transceivers includes two pairs of “conducting lines,” each including a first and second “micro coaxial cable” with “an inner conductor” and “an outer conductor.” Ex-1004, 17:43-56, 18:40-63, Figs. 3A-3B.

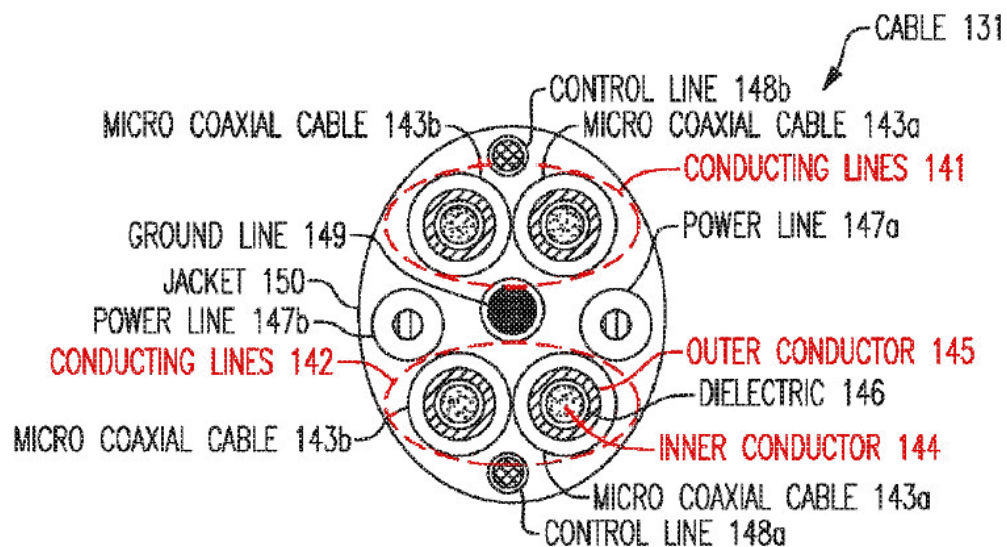


FIG. 3A

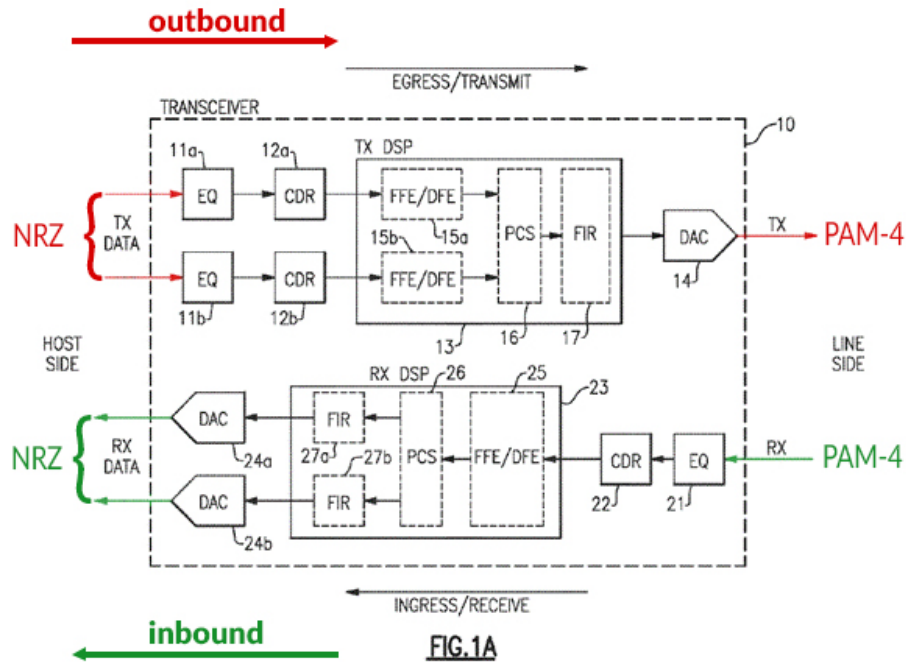
67. The conductors **convey electrical transit signals** between the DRR devices. Lugthart teaches the “electrical conducting lines” “transport electrical signals between” the two transceivers. Ex-1004, 16:11-15, 4:11-13.

68. For at least these reasons, Lugthart teaches limitation [1c].

[1d] the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and

69. Lugthart teaches the **first DRR device** (e.g., transceiver) **converting between said electrical transit signals** (which are sent over the cable) **and said inbound and outbound multi-lane data streams for the first host interface port**. Lugthart teaches that each transceiver converts between the NRZ signals of the inbound and outbound data streams on the host side (for the host interface) and PAM-4 electrical signals on the cable side. Ex-1004, 7:13-33 (“receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable,” or “vice versa.”), 8:48-60, 15:64-16:10, 23:44-58, 24:17-23, Figs. 1A, 4B.⁵

⁵ The '233 patent confirms that this falls within its scope. In the specification, the DRR devices perform “format conversion” by “converting 1 lane of PAM4 symbols into 2 lanes of NRZ symbols, and vice versa.” Ex-1001, 4:43-45.



70. As explained above, the host-side of the transceiver includes inbound and outbound multi-lane data streams that are exchanged with the first host interface port. See above §V.A.3[1a]; see, e.g., Ex-1004, 8:48-60, 15:42-47 (each transceiver “has an input port that is configured to mechanically and electrically connect...to a corresponding port or other interface on the respective electronic device”).

71. For at least these reasons, Lugthart teaches limitation [1d].

[1e] the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,

72. Limitation [1e] mirrors [1d] and differs only by changing “first” to “second.” Lugthart teaches a cable with two symmetric DRR devices (e.g., transceivers), one at each end of the cable. *See* above §V.A.3[1b] (explaining Lugthart’s symmetric cable design; that analysis applies and is incorporated here). Either DRR device would be the first DRR device recited in [1d]; the other DRR device would be the second DRR device recited in [1e], with corresponding second host interface port, for the same reasons explained previously. That analysis applies to [1e] and is incorporated here. *See* above §V.A.3[1d].

73. For at least these reasons, Lugthart teaches limitation [1e].

[1f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

74. Lugthart teaches **the first and second DRR devices** (e.g., transceivers at respective ends of the cable) **providing pre-equalization of the electrical transit signals**. The DRR devices were explained above (*see* above §V.A.3[1a]-[1b]); for example, Lugthart teaches “a pair of transceivers provided at respective ends of the cable.” Ex-1004, 6:65-7:3, Figs. 2A, 4A. The transceivers are symmetric; one is the first DRR device, while the other is the second. Ex-1004, 19:34-40.

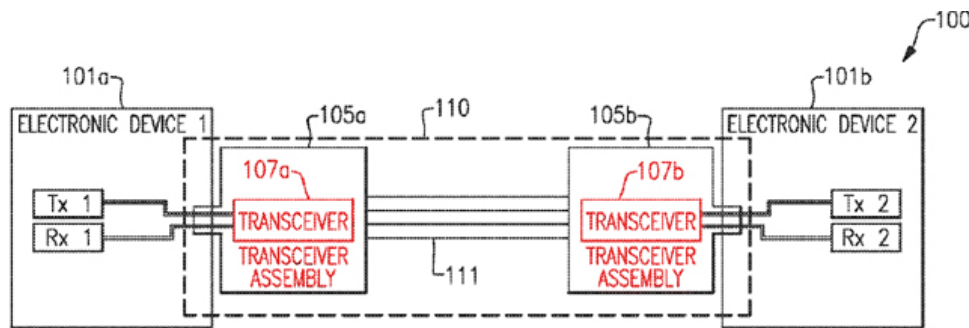


FIG.2A

75. Each transceiver performs pre-equalization using “output pre-emphasis” on the electric signals that are to be transmitted over the cable. Ex-1004, 29:21-28. Before transmission, FIR filter 17 within DSP 13 performs “emphasis on the signal to compensate for channel losses.” Ex-1004, 23:59-64, 9:39-49, Figs. 1A, 4B. “DSP 13 can include additional processing...to further process signals” including “de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies”; this is also pre-equalization. Ex-1004, 23:66-24:2, Fig. 4B.

76. “Pre-emphasis” is the most common way to perform pre-equalization. I have routinely heard these terms used interchangeably in my decades of experience in the field, as further confirmed in textbooks and dictionaries.⁶ “De-emphasis” is another way to perform pre-equalization, which attenuates certain

⁶ This was a basic concept confirmed by numerous textbooks and other references. See Ex-1020, 000020-000021, Fig.1.10 (describing “[p]re-emphasis” as “equalization at the transmitter”); Ex-1031, 2:39-42 (describing that a commonly used technology for combating inter-symbol interference is known as “‘pre-emphasis’ or ‘pre-equalization’”).

frequency components instead of boosting them. Lugthart uses pre-emphasis, with an option of also using de-emphasis, to perform pre-equalization by shaping the signal before transmission to account for anticipated channel losses.

77. Figures 1A and 4B focus on an individual transceiver and show a DSP with an FIR filter for performing pre-equalization before a signal is transmitted across the line. Figure 4A shows the transceivers at both ends of the cable; the DSP in each transceiver 10a and 10b incorporates the FIR filter described for Figures 1A and 4B. Ex-1004, 23:59-24:2, 9:39-49, 19:34-40, Figs. 1A, 4B. Lugthart makes it clear that “the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable[.]” Ex-1004, 19:52-56. Therefore, in the egress path, both transceivers (e.g., DRR devices) use the FIR filter to provide pre-emphasis/ pre-equalization before transporting the signals to the cable.

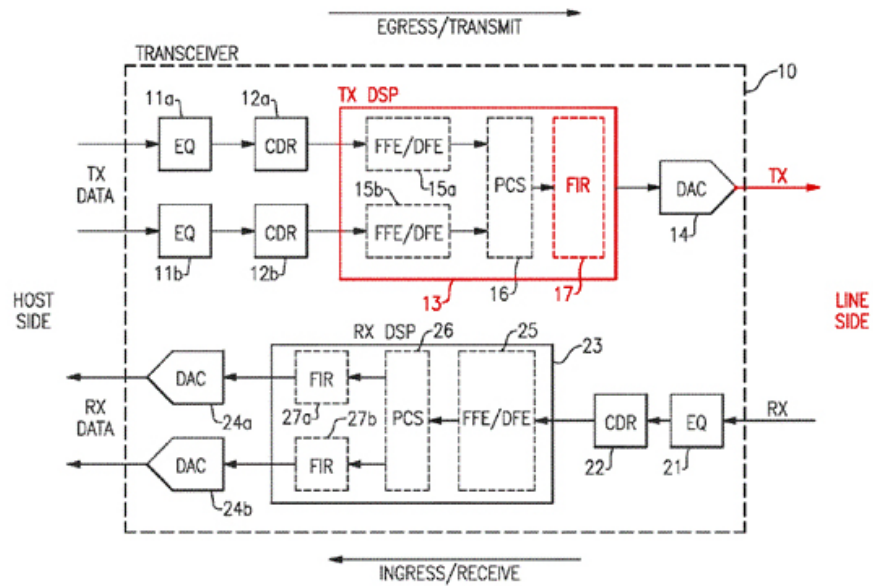


FIG. 1A

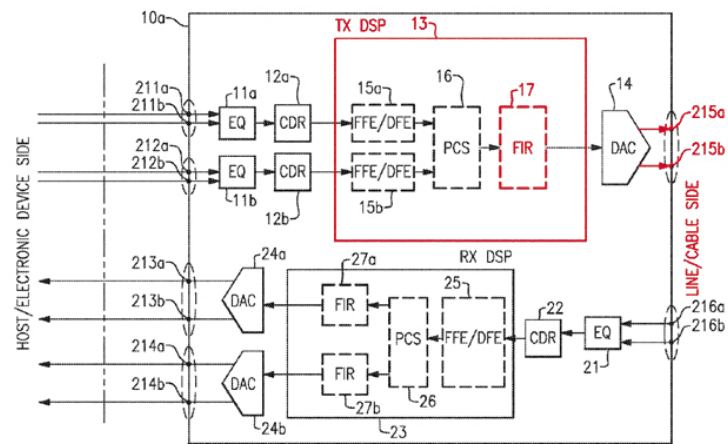
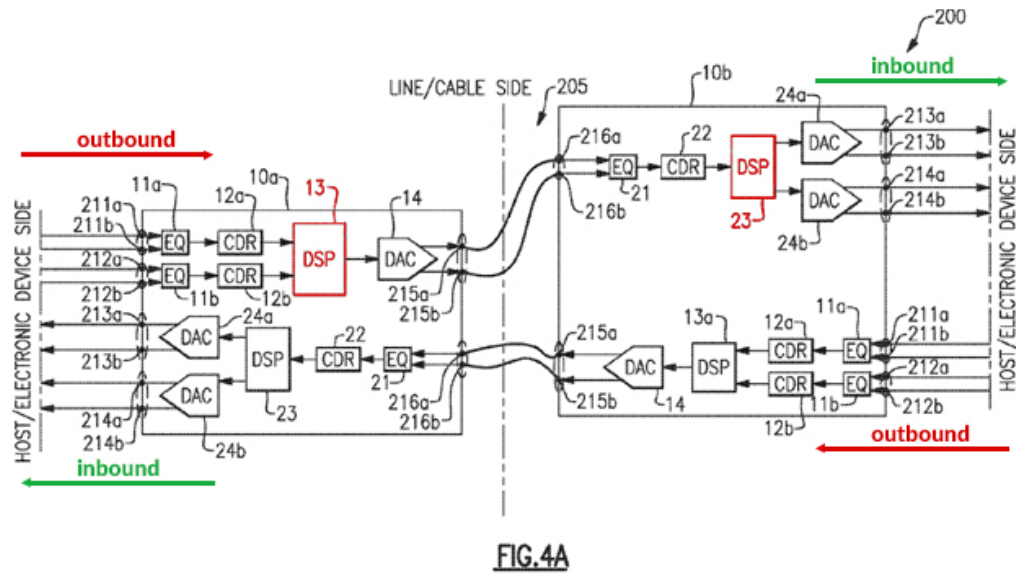


FIG. 4B



78. The transceivers provide pre-equalization **using transmit filter coefficient values stored in nonvolatile memories.** The transceivers use “finite impulse response (FIR) filters” to “perform emphasis on the signal to compensate for channel losses.” Ex-1004, 23:59-64, 9:46-51, Figs. 1A, 4B. This is a transmit filter because Lugthart uses the FIR filter for transmission. Ex-1004, 23:59-64 (using FIR filter to “condition” and “forward” the signal to a DAC for transmission), 8:19-22, 9:38-51, Figs. 1A, 4B.

79. The FIR filter contains “tap coefficients.” Ex-1004, 22:13-17, Fig. 4B. Lugthart teaches storing these coefficient values in nonvolatile memories such as ROM and EEPROM. Lugthart implements its teachings as hardware, software, or combinations of both, including with combinations involving “a digital signal processor (DSP)” designed to perform the functions described herein. Ex-1004, 56:62-57:30. The FIR filter is implemented on a DSP. Ex-1004, Figs. 1A, 4A-4B

(“TX DSP”), 7:67-8:7, 9:38-10:3. As Lugthart explains, “the subject matter described in this specification also can be implemented as one or more computer programs ... encoded on a computer storage media[.]” Ex-1004, 57:30-39. “The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium” including “ROM, EEPROM, ... or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer.” Ex-1004, 57:40-67. Because Lugthart’s FIR filter is implemented on its DSP, Lugthart teaches storing its FIR software program in nonvolatile memory, including FIR “instructions” and “data structures,” which would include the FIR coefficients that are used to perform the FIR filter operations taught by Lugthart. Ex-1004, 57:40-67, 22:13-17, Fig. 4B.

80. A POSITA would have found it obvious and been motivated to apply Lugthart’s teachings and store Lugthart’s coefficients in nonvolatile memory. Ex-1004, 56:62-57:67. FIR filters (including their coefficients) were often implemented using software for DSPs. Lugthart’s FIR filter was already implemented on a DSP, meaning Lugthart’s active cable would already have nonvolatile storage to store the DSP software for the FIR filter. The software program would obviously have included associated data, such as FIR coefficients, because they are needed for FIR filter operation. Ex-1004, 22:13-17. It would not

make sense to store some portions of the FIR code while excluding the coefficients. The simplest, fastest, and most straightforward implementation of Lugthart's teachings would have been to save the FIR instructions and data (including coefficients) in a nonvolatile memory (Ex-1004, 57:40-67), so they can be loaded and used whenever Lugthart's cable is connected and powered on. The storage of software instructions and data in memory was a trivial implementation detail that a POSITA would have found routine and obvious because that is how software has been used for decades, and those are basic skills taught in undergraduate engineering courses. Additionally, a POSITA would have been motivated to apply Lugthart's teachings in this manner to provide default, baseline parameters, for reasons explained below for Ground 2 (Motivation to Combine subsection).

81. Additionally, POSITA would have recognized the need for these coefficient values to be stored so the cable operates as described by Lugthart. Because volatile memory loses data when unpowered, while nonvolatile memory retains data, a POSITA would have found it obvious, based on Lugthart's teachings, to use nonvolatile memory for storing these coefficients. Otherwise, the coefficient value would be lost whenever the cable is disconnected, and the FIR filter would not function as taught. Ex-1004, 22:13-17, 23:59-64. Moreover, even if the coefficients were loaded into volatile memory during operation, they would

still need to be restored from nonvolatile memory each time the cable is reconnected and powered on, to ensure the FIR filter operates as intended. Manual re-entry of the coefficients with each reconnection would be impractical, and given the straightforward nature of storing coefficients in nonvolatile memory—especially since such memory would already be used for storing the rest of the FIR DSP program—doing so would have been obvious to a POSITA. That way, the coefficients only need to be stored once per cable. Even if that initial storage of coefficients is performed manually, subsequent uses of the cable would simply load the pre-set parameters.

82. For at least these reasons, Lugthart teaches limitation [1f].

Ground 2: Gorecki further teaches storing transmit filter coefficient values in nonvolatile memories.

83. Like Lugthart, Gorecki teaches pre-equalization of electrical signals over a cable. Ex-1005, Abstract, 3:8-16, 8:1-8. For example, Gorecki teaches a communication system that includes “a first transmitter and a first receiver,” and specifies that “the first transmitter includes equalization circuitry to compensate for bandwidth limitations and reflections[.]” Ex-1005, Abstract, 3:8-16, 3:35-38, 6:3-9, Fig. 3. This equalization circuitry performs pre-equalization because it is located on the transmitter side and conditions the signal before transmission to compensate for limitations and reflections of the channel. Ex-1005, Abstract, 3:8-16, 3:35-38, 6:3-9, Fig. 3.

84. Gorecki teaches pre-equalization circuitry comprising a finite impulse response (“FIR”) filter with multiple tap coefficient values. Ex-1005, 6:38-41, 9:3-15. Gorecki further teaches storing “pre-programmed”/“pre-set” tap coefficient values in various types of nonvolatile memories, including “ROM, PROM, EPROM, [and] EEPROM[.]” Ex-1005, 7:18-26.

85. Therefore, the combination of Lugthart and Gorecki teaches [1f].

86. **Motivation to Combine.** Lugthart teaches an active cable with filter coefficient values in its transceivers. Ex-1004, 4:10-12, 22:6-17, 23:59-64, 9:46-51, Figs. 2A, 4B. Gorecki teaches storing these types of coefficient values in nonvolatile memory and retrieving the coefficient values using a controller. Ex-1005, 6:39-55, 7:4-33, 9:3-15. A POSITA would have been motivated to apply Gorecki’s teachings to Lugthart by storing Lugthart’s coefficient values in nonvolatile memory, with a reasonable expectation of success, for numerous reasons explained below.

87. First, Lugthart teaches coefficient values, and as with all data in computers, those values would naturally to be stored in memory. There are two types of memory: (i) volatile (where data is lost when unpowered) and (ii) nonvolatile memory (where data is retained without power). Using nonvolatile memory would have been one of two possible solutions, which a POSITA would have chosen with predictable results and a reasonable expectation of success

because the types of nonvolatile memory taught by Gorecki (e.g., ROM, PROM, EPROM, and EEPROM) have been used to store data in computers for many decades. Lugthart provides express motivation to combine by teaching software implementations where program instructions and data are stored in nonvolatile memory, as explained above. Ex-1004, 57:40-67, Figs. 1A, 4A-4B, 7:67-8:7, 9:38-10:3.

88. Moreover, a POSITA would have been motivated to use *nonvolatile* memory to store Lugthart's coefficients, so that the coefficients are preserved when the cable is disconnected—a common scenario for Ethernet cables—and available for subsequent use in the manner taught by Lugthart. Ex-1004, 22:13-17, 23:59-24:2, 24:23-29. Otherwise, if stored in volatile memory, the coefficient values would be lost whenever the cable is disconnected and the transceivers lose power, including for example when the cable is shipped from the manufacturer to customers or when a customer plugs the cable into different computers or switches. For example, in situations where coefficient values are manually determined and entered for the specific cable deployment, storing these values in nonvolatile memory allows them to be saved for future uses. Otherwise, the coefficients would be lost when the cable is disconnected, requiring recalculation and re-entering each time the cable is reconnected. Having the filter coefficient values available in nonvolatile memory would have been advantageous because the cable can simply

read and use the values immediately after the cable is connected, without having to determine the values on the fly each time from scratch, which takes additional time. Moreover, even if link training was used to fine-tune coefficient values during operation (Ex-1005, 7:50-61), a POSITA would nonetheless have been motivated to start with a baseline set of coefficient values to use as a default when the cable is first connected because it provides a level of equalization from the start and helps adjust coefficients to their final values in a shorter time during operation. Therefore, a POSITA would have been motivated to use nonvolatile memory to have coefficient values readily available whenever the cable is connected.

89. Gorecki provides additional implementation details that a POSITA would also have been motivated to combine with Lugthart. For example, given Gorecki's teaching of storing coefficient values in memory, a POSITA would also have been motivated to apply Gorecki's teachings of a controller to read those tap values from memory and distribute them to a "transmitter or set of transmitters." Ex-1005, 7:14-17. Each transceiver in Lugthart includes two DSPs with two transmitters. Ex-1004, Fig. 1A. Having a controller configure both, as Gorecki teaches, would have simplified the configuration process and required only a single controller to access the memory, rather than multiple DSPs; controllers were routinely used for these types of configuration purposes. Therefore, a POSITA would have been motivated to apply Gorecki's teachings and use a controller to

read the requisite coefficient values from memory when the cable is plugged in (and thus powered on) and then to use configure the FIR filters with the FIR coefficient values.

90. Additionally, a POSITA would have been motivated to combine Lugthart and Gorecki due to the similarity of their teachings. For example, both are directed to high-speed communications over a cable. Ex-1004, Abstract, 3:12-16, 4:10-12, 6:55-7:5, 14:29-31; Ex-1005, Abstract, 1:12-17. Both connect a transmitter and receiver located at opposite ends of the cable. Ex-1004, Figs. 2A, 4A, 14:29-34; Ex-1005, 4:16-21, 8:1-6, Fig. 3. Both recognize signal loss over the cable, and both address it with pre-emphasis, using an FIR filter, in the transmitter. Ex-1004, 22:3-17, 23:13-23, 23:59-64, 29:21-28; Ex-1005, Abstract, 3:8-16, 6:38-41, 9:3-7. Gorecki further teaches a trivial detail of storing the FIR filter tap coefficients in nonvolatile memory. Ex-1005, 7:18-26. Therefore, the combination uses a known technique (storing data in nonvolatile memory) to improve similar devices in the same way.

91. The combination of Lugthart and Gorecki would not have changed the principle of operation of either reference. As explained above, both references are directed to high speed communication over a cable, with pre-equalization implemented on the transmitting side. Gorecki's teachings would simply have been used to store values in nonvolatile memory, which is already implied or suggested

by Lugthart because otherwise those values would not have been available to be used in the manner Lugthart teaches, as explained above.

92. In addition to the reasons explained earlier in this section, a POSITA would have had a reasonable expectation of success in combining teachings from Lugthart and Gorecki because computers have, for decades, stored values they require in nonvolatile memory such as ROM, PROM, EPROM, and EEPROM. This was a trivial implementation detail that would have been well within the level of ordinary skill (*see* above §III). Undergraduate students would have been expected to be able to write data to nonvolatile memory, including ROM, PROM, EPROM, and EEPROM.

93. This would have been a combination of prior art elements (e.g., using nonvolatile memory with Lugthart's teachings) according to known methods (e.g., saving data in ROM, PROM, EPROM, or EEPROM) to yield predictable results (e.g., data stored in memory). Therefore, a POSITA would have found it obvious to combine Lugthart and Gorecki, with a reasonable expectation of success.

4. Dependent Claim 2

2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.

94. Ground 2 teaches claim 2. As explained above, Ground 2 teaches a DRR device providing pre-equalization using transmit filter coefficient values

stored in the nonvolatile memories. *See* above §V.A.3[1f] (explaining combination and motivation).

95. Gorecki teaches **a first controller that configures the first DRR device in response to a power-on event**. For example, Gorecki teaches a “controller” that distributes the coefficients of the tap(s) to “the transmitter or a set of transmitters.” Ex-1005, 7:1-17. Gorecki also teaches storing coefficients in memory; when there is a “start-up/power-up” event, necessary information is retrieved from memory. Ex-1005, 7:14-33. This obviously would have included “coefficients of the tap(s),” which are needed for filter operation (Ex-1005, 7:14-33, 9:3-15), and when a controller is used, the controller would obviously have read the coefficients from memory to distribute them to the transmitters, as Gorecki teaches. Ex-1005, 7:1-17. Controllers were commonly used to configure devices; this was a simple and easy configuration technique. Based on Gorecki’s teachings, a POSITA would have been motivated and found it obvious to add a controller to Lugthart’s active cable and to use that controller to configure the transmitter coefficients by reading them from memory. *See* above §V.A.3[1f] (Motivation subsection explaining the combination of Gorecki’s controller teachings to Lugthart).

96. Gorecki also teaches **the first controller retrieves the transmit filter coefficient values from the nonvolatile memories as part of said configuring**.

Gorecki teaches coefficients being programmed by the user (Ex-1005, 7:1-4), and that the coefficients may be pre-programmed/pre-set in nonvolatile memories such as “ROM, PROM, EPROM, [and] EEPROM.” Ex-1005, 7:18-31; *see* above §V.A.3[1f] (explaining memory teachings). Therefore, it was obvious for the user to provide the coefficients by programming them into nonvolatile memory; when the controller configures the tap coefficients in the transmitter, the controller obviously retrieved those coefficient values from the nonvolatile memories where they are stored. Ex-1005, 7:13-31. Gorecki teaches this, and it would have been obvious to retrieve the filter coefficient values from memory because, as a matter of basic programming, values must be retrieved before they can be used.

5. Dependent Claim 3

3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

97. Ground 2 teaches claim 3. This claim recites “the transmit coefficient values” without antecedent basis. To the extent this claim is not indefinite, a POSITA would have understood “the transmit coefficient values” to refer to “the transmit filter coefficient values.”

98. As explained above, Ground 2 teaches that the first and second DRR devices (e.g., transceivers at respective ends of the cable) use transmit filter

coefficient values to transmit signals. *See* above §V.A.3[1f] (explaining combination and motivation).

99. Lugthart teaches that the DRR devices are **programmed** to use the transmit coefficient values. Ex-1004, 11:58-60. For example, Lugthart teaches programmable equalization circuitry such as DSPs in the first and second DRR devices (e.g., transceivers). Ex-1004, Figs. 1A, 4A-4B (“TX DSP”), 7:67-8:7 (describing “transmit path digital signal processor (DSP)” in transceiver), 9:38-10:3 (discussing “transmit path DSP”), 30:39-47 (teaching “digital signal processing” using, e.g., “[p]rogrammable chip sets,” including for “conditioning” data signals, “equalizing the data signals to reduce the effects of ISI, framing, error correction, scrambling”). Because the transceivers include programmable equalizers/DSPs, the transceivers are programmable to perform the functions described by Lugthart.

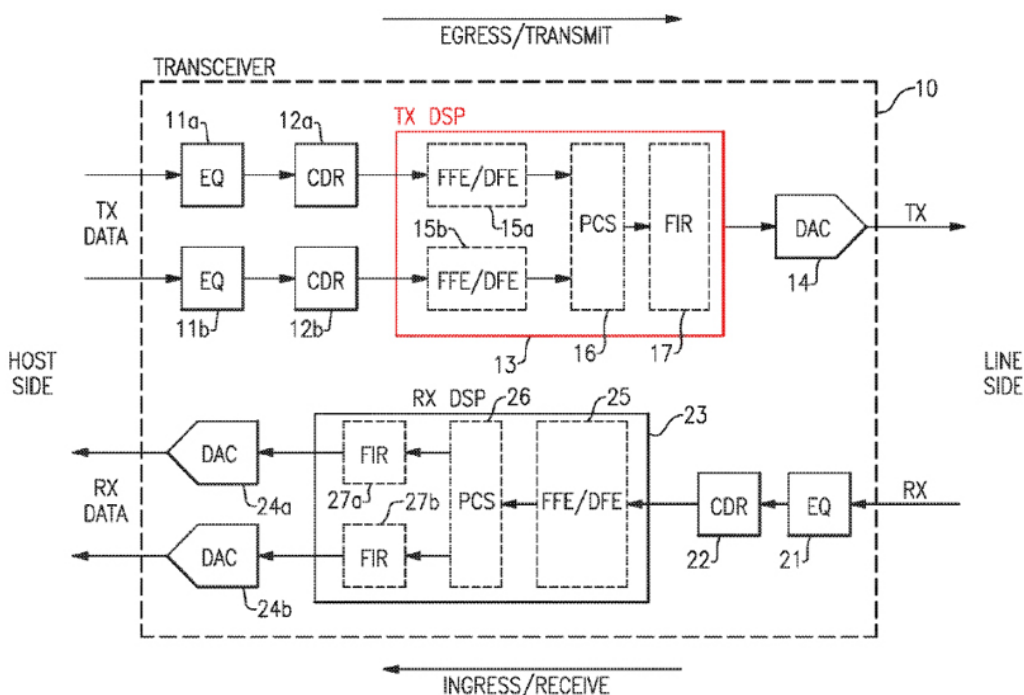


FIG.1A

100. DSP refers to digital signal processors, which as known in the art were programmable processors that ran software programs. Moreover, Lugthart teaches using programming to implement its teachings, such as with DSPs or more general processors. Ex-1004, 57:10-21 (“[T]he various illustrative logics, logical blocks, modules and circuits described in connection with the aspects disclosed herein may be implemented or performed with a general purpose single- or multi-chip processor, a digital signal processor (DSP)...”).

101. Furthermore, Gorecki teaches programming the transmit coefficient values, which are used by the transmitter for performing equalization. Ex-1005, 7:1-4 (“[T]he adjustment or control of the taps of the equalization circuitry may be by the user via programming either before or during operation of the transmitter.”).

Gorecki also discloses that the transmitter “may...program...the operation or response of the equalization circuitry.” Ex-1005, 3:59-62, 7:1-4.

102. The DRR devices are programmed to **use the transmit coefficient values each time power is supplied to the first and second end connector plugs**. For example, Gorecki teaches that “the transmitter may access the memory to retrieve” coefficient values “during startup/power-up,” which are used to program the taps in the equalization circuitry. Ex-1005, 7:18-33. Lugthart teaches that each end of the active cable has a transceiver and an end connector plug. *See* above, §V.A.3[1a]-[1b]. Power is supplied to the first/second DRR devices via power lines connected to their perspective end connector plugs. Ex-1004, 14:29-31 (“FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110.”), 17:26-29 (“...various implementations of cables can include power lines configured to supply power from one of the electronic devices 101a and 101b to the another electronic device.”), 17:57-59. Therefore, because the coefficients are used to transmit data when the active cable is in operation, Ground 2 teaches the transceivers being programmed to use the transmit coefficient values each time power is supplied to the plugs.

6. Dependent Claim 4

- 4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.**

103. Ground 2 teaches claim 4. Lugthart uses the transmit filter coefficient values to “compensate for channel losses” of its active cable. Ex-1004, 23:59-24:2. Those values would obviously have been determined after assembly of the active cable; otherwise, the properties of the cable could not be measured because there would not be a cable attached to the transceivers. By measuring and storing the coefficients after cable assembly, the equalization process can be tailored to the specific characteristics of each individual cable, thereby improving the effectiveness of equalization and enhancing overall signal quality performance. This customization would have naturally fit into test and quality assurance (QA) procedures, and it would have been appropriate for applications that demand maximum performance, high data throughput, or extended cable lengths. For example, this would benefit data centers with long cable lengths or high bitrates by more accurately compensating for cable-specific losses and thereby improving signal quality. Thus, it would have been obvious to determine the transmit filter coefficients after assembly, based on actual cable measurements, and to store them in nonvolatile memories so that they can be reliably accessed during operation in accordance with Lugthart’s teachings. *See* above §V.A.3[1f] (explaining how and

why Lugthart would have been combined with Gorecki, including for storing coefficients in memory).

104. Additionally, Gorecki teaches that coefficient values may be “determined or controlled in response to $a[n]$... adaptive algorithm ... to provide enhanced or optimal reception ... at a receiver.” Ex-1005, 6:56-61. “[T]he adjustment or control of the taps” may be made by the user “via programming either before or during operation of the transmitter.” Ex-1005, 7:1-4. Adjustments can include, fine adjustments or reprogramming during operation. Ex-1005, 7:50-53 (coefficient values “may be fine-tuned to enhance the system performance”), 7:18-26 (describing “...the coefficients of the tap(s)” may be “re-programmed”). Such fine adjustment happens “after (or during) the performance of an initialization or re-initialization process”. Ex-1005, 7:53-59. Both options occur after assembly. Because the updated coefficient values reflect the current characteristics of the cable, it would have been obvious to periodically update the values stored in nonvolatile memory (for example, the first time when the cable is connected after assembly, or from time to time when the difference between the new and previously stored values become too large) to reflect the updated coefficient values. In fact, Gorecki explains that the coefficient values can be stored “semi-permanently” or “temporarily” until “re-programmed.” Ex-1005, 7:18-33. Therefore Gorecki teaches re-programming coefficient values into the

memories where they are stored, including EEPROM. *Id.* Because the active cable would not have been operable before it was assembled, the adjustment and storage of coefficient values would obviously have occurred after assembly of the cable.

7. Dependent Claim 5

5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

105. Ground 2 teaches claim 5. First, Lugthart teaches that **the first and second DRR devices** (e.g., transceivers at respective ends of the cable) **employ receiver-based equalization of the electrical transit signals**. For example, Lugthart teaches that each transceiver includes a receiver path that performs equalization (e.g., “EQ” and “FFE/DFE”) on the electrical transit signal that is received from the cable (“RX”). Ex-1004, Figs. 1A, 4A-4B, 8:5-7, 8:22-25, 9:42-44, 22:40-49, 23:18-21. Lugthart teaches that the receiving path equalizer such as “receive path equalizer 21” is “used to provide signal equalization to compensate for transmission line losses on the line side[.]” Ex-1004, 9:10-15, 22:40-49, Figs. 1A, 4B.

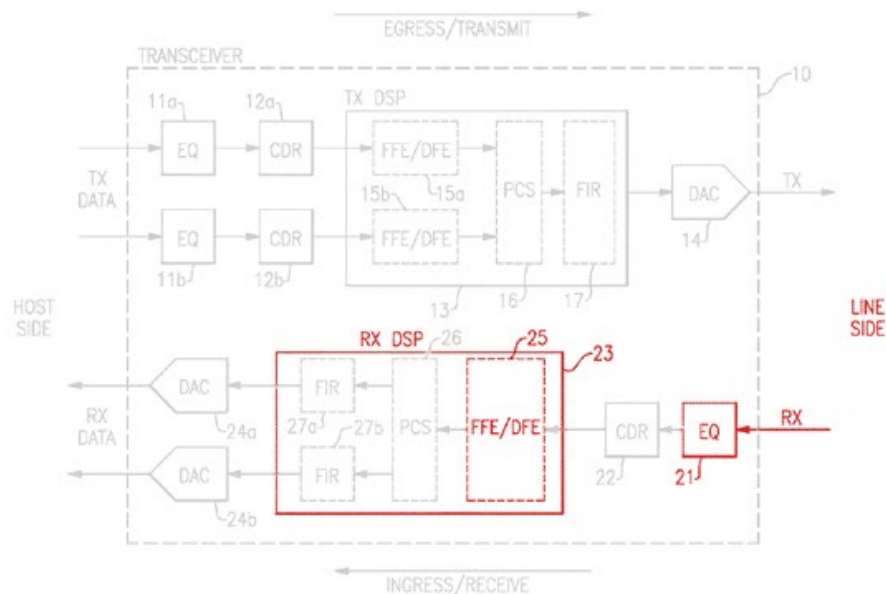


FIG. 1A

106. Because Lugthart teaches a transceiver at both ends of the cable (*see* above §V.A.3[1a]-[1b]), the first transceiver employs receiver-based equalization in one direction, while the second transceiver employs receiver-based equalization in the other direction. Ex-1004, 7:55-8:5, Figs. 2A, 4A.

107. The combination with Gorecki teaches receiver-based equalization **using coefficient values stored in the nonvolatile memories**. First, Lugthart teaches software implementations, where its teachings are implemented using program instructions and data (including coefficients) stored in nonvolatile memories. *See* above §V.A.3[1f] (explaining obviousness) ; Ex-1004, 56:65-57:67. Additionally, Gorecki teaches how “conventional” systems often employ “a finite impulse response filter (‘FIR filter’), in the receiver to equalize the transmitted

signals in an effort to address, or compensate for the effects of dispersion and reflection of the transmitted signal and/or the sensitivity of the system to that distortion or reflection.” Ex-1005, 1:59-65. Gorecki further explains that the equalization circuitry comprising the FIR filter “typically includes a one or more taps having fixed or pre-programmed...coefficients.” Ex-1005, 1:65-67. Because Gorecki teaches storing equalization coefficient values in nonvolatile memories (Ex-1005, 7:18-26), it would have been obvious to store the equalization coefficients values for the receiver in nonvolatile memories as well. *See above* §V.A.3[1f] (explaining the obviousness and motivation to store coefficient values in nonvolatile memory; that analysis applies here to receiver coefficients).

108. **Motivation to Combine.** The motivation to combine Lugthart and Gorecki was explained above. *See above* §V.A.3[1f] (explaining combination and motivation). A POSITA would have further been motivated to apply Gorecki’s teachings to receiver-side equalization, by storing filter coefficient values in nonvolatile memory, for the same reasons that were explained for transmit-side pre-equalization. Lugthart provides motivation to combine by teaching receiver-side equalization, along with implementations where software instruction and data (which would include coefficients) are stored in nonvolatile memory. *See above* §V.A.3[1f]. Storing the coefficients in memory would have been the simplest and most straightforward way for Lugthart’s receiver-based equalization to operate as

taught. Ex-1004, 9:10-15, 22:40-49. This trivial implementation detail allows the coefficients to be stored when the cable is disconnected and retrieved when the cable is powered on, just as explained for the transmit side. Therefore, the same analysis and motivations apply here.

8. Dependent Claim 6

6. The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

109. Grounds 1 and 2 teach claim 4. For example, Lugthart teaches that the cable includes “twinaxial cables (‘Twinax’), where each Twinax cable includes two inner conductors instead of a single inner conductor.” Ex-1004, 19:2-6. “In such cases, the two inner conductors can be configured to implement differential signaling[,]” to carry electrical transit signals in differential form across the cable (in both directions). Ex-1004, 19:2-6, 2:45-47, 3:12-16, 12:13-15, 16:27-30, Figs. 6A-6B. As Lugthart explains, “[d]ifferential signaling is advantageously used...to provide enhanced noise immunity via common-mode noise rejection.” Ex-1004, 16:37-49. These benefits would have motivated a POSITA to apply Lugthart’s teachings of an active cable with twin-axial conductors that carry each of the electrical transit signals in differential form, using two inner conductors.

9. Dependent Claim 7

7. The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

110. Ground 2 teaches claim 7. Lugthart teaches that the first/second DRR devices (e.g., transceivers at respective ends of the cable) perform pre-equalization using FIR filters. *See* above §V.A.3[1f]. Similarly, Gorecki teaches implementing “equalization circuitry” using an “FIR filter” with leading, main cursor (data), and trailing taps. Ex-1005, 9:3-7. The main cursor tap is the data from the current sample. The leading tap “determines the amplitude of the signal introduced in the leading tap[,]” and the trailing tap “determines the amplitude of the signal introduced in the trailing tap.” Ex-1005, 9:18-21.

111. Gorecki teaches that the leading and trailing taps can be “changed” (Ex-1005, 9:24-25), including circumstances where the “leading and/or trailing taps may be ‘turned off’ or disabled[.]” Ex-1005, 18:15-18. Turning off the leading and trailing taps leaves only the main cursor tap and therefore is mathematically equivalent to performing no equalization. Because an FIR filter calculates a weighted average, when only the tap for the current sample is enabled, the filter performs an average of only a single sample with itself, leaving only the current sample. This is basic math that a POSITA would have understood because FIR filters are taught in undergraduate Digital Signal Processing courses such as linear

systems. Therefore, Lugthart and Gorecki teach a scenario where the first and second transceivers do not perform pre-equalization.

112. It would have been obvious to apply Gorecki's teaching to Lugthart by disabling equalization of the multi-lane data streams provided to the host interface ports. A POSITA would have been motivated to do this because the path from the transceiver (in the cable) through the host interface port to the host IC was known to be far shorter than the cable, on the order of inches rather than feet. Some designs had smaller loss budgets allocated to that path, for example with requirements of shorter lengths and low-loss connectors. In those designs, where the channel is known to have reduced loss, a POSITA would have been motivated to turn off pre-emphasis because it is not needed, and to reduce power.

113. A POSITA would have had a reasonable expectation of success in doing so because it merely involves turning off the FIR filter. Gorecki provides a simple mechanism to do so—disabling leading and trailing taps—which merely requires changing tap values or filter settings. A POSITA would have found it trivial to disable an FIR filter because it merely requires passing the signal through as-is, instead of modifying it with a filter.

Ground 3: Samaan further teaches claim 7.

114. Like Lugthart and Gorecki, Samaan teaches transmit-side pre-equalization using an FIR filter. Ex-1007, ¶¶78-82, ¶¶139-142, Figs. 21-22, 34-35.

Samaan explains how FIR filters have tap coefficient values, including coefficients C_{-1} (analogous to Gorecki's leading taps) and C_{+1} (analogous to Gorecki's trailing taps). Ex-1007, ¶¶78-82.

115. Samaan teaches that both coefficients C_{-1} and C_{+1} can “range from 0 to 0.25.” Ex-1007, ¶¶78-82, Figs. 21-22⁷. When both are 0, the only remaining tap is the main cursor (data) sample, which as explained above is mathematically equivalent to turning pre-emphasis off (passing the signal through unmodified). Ex-1007, ¶¶78-82, Figs. 21-22. The combination therefore teaches that the first and second DRR devices do not perform pre-equalization.

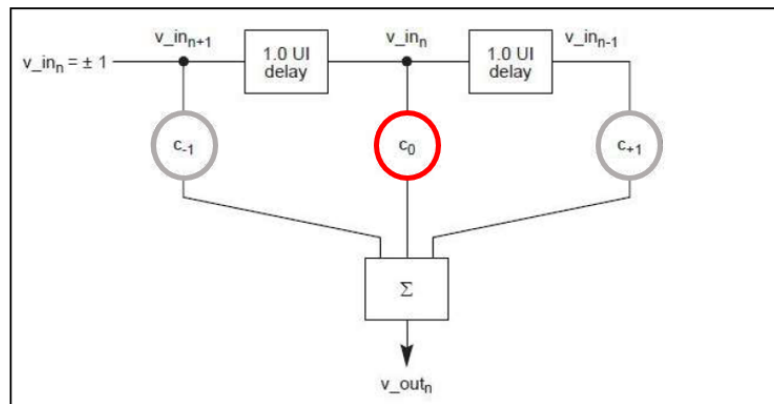


Figure 22 The PCIe 3.0 Tx Equalization FIR filter representation. (Note: The 10G-KR Filter is similar in definition).

116. **Motivation to combine.** Ground 2 (the combination of Lugthart and Gorecki) teaches an active cable performing pre-equalization using coefficient

⁷ Even though the figure 22 illustrates a PCIe 3.0 Tx Equalization FIR filter, Samaan makes it clear that the Ethernet 10GBASE KR Equalization Standard uses “an FIR filter which is identical to the one used for PCIe 3.0 as shown previously in Figure 22.” Ex-1007, ¶¶139-142, Fig. 22.

values in nonvolatile memory. *See* above §V.A.3[1f] (explaining combination and motivation). Samaan further teaches details about filter coefficient values, including that the coefficient values are adjustable to achieve certain output signal amplitude, with zeros in leading and trailing values disabling the filter. Ex-1007, 78-82, Figs. 21-22. A POSITA would have been motivated to apply Samaan's teachings to Ground 2 by adjusting the coefficient values that are already used by the active cable in Ground 2, because doing so enables the active cable to achieve desired "amount of equalization" (Ex-1005, 9:37-40). A POSITA would have further been motivated to set the value of the leading and trailing tap to 0 to disable pre-equalization for the reasons explained above. *See* above §V.A.9 (Claim 7, explaining the motivation to apply Gorecki's teaching to Lugthart by disabling equalization.)

117. A POSITA would have had a reasonable expectation of success in combining teachings from Samaan's teachings and Ground 2. Gorecki already explains that the coefficient values "may be fine-tuned to enhance the system performance", and that the "amount of equalization may be adjusted or controlled" by "altering" the coefficient values. Ex-1005, 7:50-53, 9:37-40. Gorecki further explains that the leading tap and the trailing tap can be "controlled, set and/or changed." Ex-1005, 9:16-26. Samaan merely explains how the leading tap and the trailing tap can be changed (can be adjusted from 0 to 0.25) to achieve the desired

“amount of equalization.” Ex-1007, ¶¶78-82, ¶¶139-142, Figs. 21-22, 34-35; Ex-1005, 9:37-40. Therefore, applying Samaan to Ground 3 simply adds on additional details on techniques already used in Ground 2.

118. This would have been a combination of prior art elements (e.g., adjusting coefficient values, which were already used in Ground 2) according to known methods (e.g., altering the leading and trailing taps within the range to zero), to achieve a predictable result (e.g., disabling the FIR filter). Therefore, a POSITA would have found it obvious to combine Samaan and Ground 2, with a reasonable expectation of success.

10. Independent Claim 8

[8pre] A cable manufacturing method that comprises:
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119. I understand that a preamble generally does not state a claim limitation. Nonetheless, it is my opinion that Grounds 1 and 2 teach it.

120. Grounds 1 and 2 teach the cable of claim 1. *See* above §V.A.3 (Claim 1). Lugthart further teaches a method of manufacturing a cable by connecting the components of Lugthart’s active cable together, including the steps explained for limitations below. Ex-1004, Figs. 2A, 4A, 6:65-67, 7:66-8:7.

[8a] connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;

121. Grounds 1 and 2 teach [8a]. Most of limitation [8a] mirrors [1a]; Grounds 1 and 2 teach the overlapping limitations as explained above. *See above* §V.A.3[1a].

122. Lugthart further teaches **connecting a first connector plug** to the first DRR device (e.g., first transceiver). Lugthart teaches that these components are connected. The cable assembly has “a first pair of conductors including a first pluggable module”; “the first pluggable module can include a first transceiver[.]” Ex-1004, 4:10-14, 15:30-31 (each transceiver “enclosed in a packaging”). Each transceiver assembly “has an input port” which includes a connector, and that the input port “is configured to mechanically and electrically connect...to a corresponding port or other interface on the respective electronic device[.]” referring to the host device. Ex-1004, 15:42-47, 14:14-15. And Lugthart illustrates a first connector plug connected to the first transceiver. Ex-1004, Figs. 1A, 2A, 4A-4B.

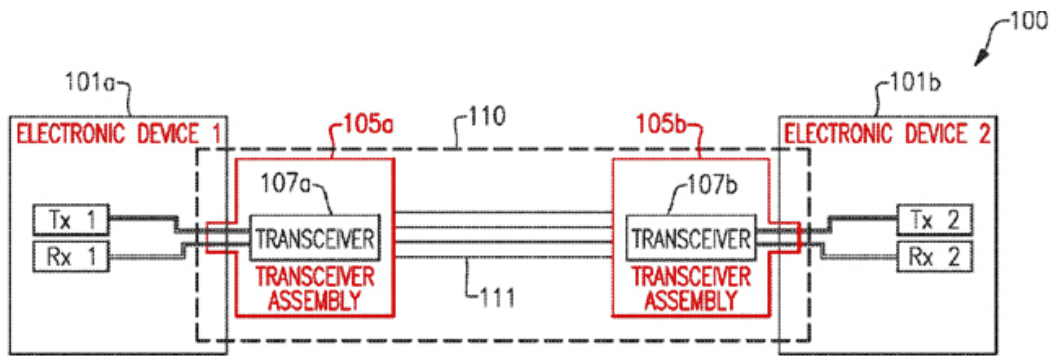


FIG. 2A

123. Therefore, because Lugthart teaches a first connector plug connected to a first transceiver, Lugthart teaches or suggests the step of connecting these components together. Ex-1004, Figs. 1A, 2A, 4A-4B, 4:11-17, 15:47-52. At a minimum, it would have been obvious because, in order for the plug and connector to be connected in an assembled cable (as Lugthart teaches), they would have obviously been connected during manufacturing, when the cable components were assembled into Lugthart's active cable. Ex-1004, Figs. 2A, 4A.

[8b] connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;

124. Grounds 1 and 2 teach [8b]. Limitation [8b] mirrors [8a], differing only by changing "first" to "second." Lugthart teaches a cable with two symmetric DRR devices, one at each end of the cable. *See* above §V.A.3[1b] (explaining Lugthart's symmetric cable design; that analysis applies and is incorporated here). Either transceiver would be the first DRR device recited in [8a]; the other transceiver would be the second DRR device recited in [8b], for the same reasons

explained previously. *See* above §V.A.10[8a]. That analysis also applies to [8b] and is incorporated here. The interface port and plug for the second transceiver, at its end of the cable, would be the second host interface port and second connector plug.

125. Therefore, limitation [8b] is satisfied for the same reasons explained for [8a]. *See* above §V.B.10[8a].

[8c] connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,

126. Grounds 1 and 2 teach [8c]. Most of limitation [8c] mirrors [1c]; Grounds 1 and 2 teach the overlapping limitations as explained above. *See* above §V.A.3[1c].

127. Lugthart also teaches **connecting** electrical conductors to the first and second DRR devices (e.g., transceivers at respective ends of the cable). As explained above, Lugthart teaches electrical conductors that are connected to first and second DRR devices. *See* above §V.A.3[1c]. Therefore, Lugthart teaches or suggests the step of connecting these components together. Ex-1004, Figs. 1A, 2A, 3A-3B, 4A-4B, 4:11-17, 15:47-52, 17:35-39. At a minimum, it would have been obvious because, in order for these components to be connected in an assembled cable (as Lugthart teaches), they would have obviously been connected during

manufacturing, when the cable components were assembled into Lugthart's active cable. Ex-1004, Figs. 2A, 4A.

- | | |
|-------------|---|
| [8d] | the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and |
| [8e] | the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port, |
| [8f] | the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories. |

128. Grounds 1 and 2 teach [8d]-[8f]. The limitations in [8d]-[8f] also appear in limitations [1d]-[1f], respectively, and are satisfied for the same reasons explained previously. *See* above §V.A.3[1d]-[1f].

- 1 [1d] the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and
- 2 [1e] the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,
- 3 [1f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

- 1 [8d] the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and
- 2 [8e] the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,
- 3 [8f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

11. Dependent Claim 9

9. **The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.**

129. Ground 2 teaches claim 9. Beyond the preamble, claim 9 mostly overlaps with claim 2; Ground 2 teaches the overlapping limitations as explained above. *See* above §V.A.4 (Claim 2).

1 2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.

1 9. The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.

130. Ground 2 also teaches **providing** a first controller **device** because it teaches a first controller, which is a device, as part of the active cable. *See* above §V.A.4 (Claim 2). Additionally, it would have been obvious to provide a controller so that it is part of the cable to perform the functions that Ground 2 teaches.

131. Ground 2 further teaches **internal** nonvolatile memory. Ground 2 teaches using nonvolatile memory as part of the active cable, to store coefficient values. *See* above §V.A.3[1f] (explaining combination and motivation). Because that nonvolatile memory is part of the cable, it obviously would have been internal to the cable. Ex-1005, 7:43-48 (“...the memory used to store...the coefficients of the tap(s)...may reside on the integrated circuit containing the transmitter, receiver or transceiver.”).

12. Dependent Claim 10

10. The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.
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132. The limitation of claim 10 is identical to claim 3, other than a change to verb tense and passive voice (“programmed” to “programming”). Therefore, claim 10 is satisfied for the same reasons explained previously. *See* above §V.A.5 (Claim 3).

13. Dependent Claim 11

11. The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.

133. Ground 2 teaches claim 11. As explained above, Ground 2 teaches that the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable. *See* above §V.A.6 (Claim 4). Because the assembly of Lugthart’s active cable includes connecting the electrical conductors (*see* above §V.A.10[8c], §V.A.3[1c]), Ground 2 teaches determining the coefficient values and storing them in nonvolatile memories after connecting the electrical conductors.

134. Lugthart and Gorecki use pre-equalization to compensate for the loss characteristics of the channel. As Lugthart explains, the FIR filters within the DSP

are used to “perform emphasis on the signal to compensate for channel losses.” Ex-1004, 23:59-24:2. Likewise, Gorecki teaches using transmitter-side equalization circuitry to “compensate for bandwidth limitations and reflections in high-speed digital communication systems.” Ex-1005, 3:8-16. To achieve the desired compensation result, Gorecki explains that the coefficients used by FIR filters are “pre-programmed or pre-set” so that the introduced “compensation...is ideally the inverse of the effects caused by the communication channel.” Ex-1005, 7:18-33, 9:3-15. Therefore, Ground 2 teaches the obvious step of determining transmit filter coefficient values by characterizing channel characteristics of the electrical conductors, so that Lugthart’s pre-equalization filter can compensate for those channel characteristics as taught. Ex-1004, 22:3-17, 23:59-24:2; Ex-1005, 3:8-16, 7:18-33, 9:3-15.

14. Dependent Claims 12-14

- | | |
|-----|--|
| 12. | The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories. |
| 13. | The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form. |
| 14. | The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports. |

135. The limitations of claims 12-14 are identical to claims 5-7 and are satisfied for the same reasons. *See* above §V.A.7-9 (Claims 5-7).

1 5. The cable of claim 4, wherein the first and second DRR devices employ
receiver-based equalization of the electrical transit signals using
coefficient values stored in the nonvolatile memories.
2 6. The cable of claim 4, wherein the electrical conductors comprise twin-
axial conductors that carry each of the electrical transit signals in
differential form.
3 7. The cable of claim 4, wherein the first and second DRR devices do not
perform pre-equalization of the multi-lane data streams provided to the first
and second host interface ports.

1 12. The method of claim 11, wherein the first and second DRR devices
employ receiver-based equalization of the electrical transit signals using
coefficient values stored in the nonvolatile memories.
2 13. The method of claim 11, wherein the electrical conductors comprise
twin-axial conductors that carry each of the electrical transit signals in
differential form.
3 14. The method of claim 8, wherein the first and second DRR devices do
not perform pre-equalization of the multi-lane data streams provided to the
first and second host interface ports.

15. Independent Claim 15

[15pre] A communications method that comprises:
--

136. I understand that a preamble generally does not state a claim limitation. Nonetheless, it is my opinion that Grounds 1 and 2 teach it.

137. Lugthart teaches **a communications method**. For example, Lugthart is directed to “methods for high speed communications,” which can be used to “achieve reliable high-speed point-to-point communication between different electronic devices, computing devices, storage devices and peripheral devices.”

Ex-1004, Abstract, 6:65-7:1. Lugthart teaches a communications method for active cables with the various components and techniques discussed above for claim 1.

See above §V.A.3 (Claim 1).

138. Gorecki also teaches “a technique of...enhancing the performance of high-speed digital communications through a communications channel.” Ex-1005, Abstract, 1:12-17.

139. The communications method taught by Grounds 1 and 2 further includes the limitations of claim 15 discussed below.

[15a] inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and
--

140. Grounds 1 and 2 teach [15a]. Lugthart teaches **inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first DRR device** (e.g., first transceiver).

This is shown in Figure 2A, for example with Electronic Device 1 as the first host and an end connector plug inserted into its interface port; wiring connects the transceiver to the end connector plug. Ex-1004, 14:14-15 (referring to the electric devices as “host devices”), Figs. 1A-2A, 4A-4B (teaching connections from transceivers to end connector plugs).

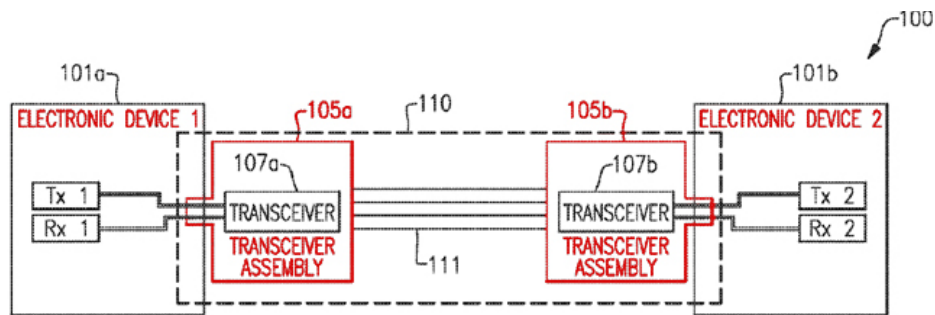


FIG. 2A

141. Additionally, it would have been obvious to insert the plug into the host interface port because that is how cables work: the plug is inserted into the port. Lugthart explains that “[e]ach of the transceiver assemblies...has an input port[,]” which includes a pluggable connector, and that the input port “is configured to mechanically and electrically connect...to a corresponding port or other interface on the respective electronic device...” Ex-1004, 15:42-52. Lugthart further teaches connecting the transceiver to the host “in a releasable fashion”, meaning the plug can be inserted and removed from the host port. Ex-1004, 15:42-52.

142. The rest of [15a] combines elements recited in [1a], [1c], and [1d]; Grounds 1 and 2 teach the rest of [15a] for the same reasons explained previously. *See above* §V.A.3[1a], [1c]-[1d].

[15b] inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,

143. Grounds 1 and 2 teach [15b]. Limitation [15b] mirrors [15a] and differs only by changing “first” to “second.” As explained above, Lugthart teaches a cable with two identical transceivers, one at each end. *See above* §V.A.3[1a] (explaining how the transceivers are DRR devices), [1b] (explaining Lugthart’s symmetric cable design). Either transceiver would be the first DRR device recited in [15a]; the other transceiver would be the second DRR device recited in [15b]. The interface port and plug for the second transceiver, at its end of the cable, would be the second host interface port and second end connector plug. Therefore, limitation [15b] is satisfied for the same reasons explained for [15a]. *See above* §V.A.15[15a].

[15c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

144. Grounds 1 and 2 teach [15c]. Limitation [15c] is identical to [1f] and is satisfied for the same reasons. *See above* §V.A.3[1f].

1 [1f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

1 [15c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

16. Dependent Claim 16

- 16. The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.**

145. Ground 2 teaches claim 16. For example, Lugthart teaches **supplying power to the first and second end connector plugs**. For example, Lugthart teaches its “active cable including actively powered componentry,” e.g., “first and second transceiver assemblies” at each end of the active cable. Ex-1004, 14:29-42. Lugthart teaches the power consumption of several form factors for active cables. Ex-1004, 54:45-55:45. Additionally, it would have been obvious to supply power to both end connector plugs because Lugthart explains that they include “actively powered componentry” that requires power. Ex-1004, 14:29-42, 54:45-55:45. Without power, Lugthart’s cable would not operate as taught; the DSP and other components in the transceiver assembly would not function without power. Therefore, the simple and obvious way to implement Lugthart’s teachings would have been to provide power to both end connector plugs, so that the transceivers on both sides of the cable can operate as Lugthart describes.

146. Ground 2 teaches **the first and second end connector plugs being connected to first and second controller devices, respectively**. Gorecki teaches

that the “controller” distributes the coefficient values to the transmitter. For a controller to perform this function, it would have been connected to the DRR device and connector plug at its end of the cable, so that it is able to configure the DRR device and also receive power. Ex-1005, 7:14-17; *see* above §V.A.4 (Claim 2, explaining Gorecki’s controller), §V.A.3[1a]-[1b] (explaining the DRR devices’ end connector plug configuration).

147. Ground 2 teaches **each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory**. Ground 2 teaches that a first controller operates to configure the first DRR device in response to a power-on event, and the configuration includes retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring, for the reasons explained above. *See* above §V.A.4 (Claim 2). Because Lugthart teaches a cable with two symmetric DRR devices (one at each end of the cable), Ground 2 likewise teaches that the second controller devices operates in the same manner as the first controller device. *See* above §V.A.3[1b] (explaining symmetry)

17. Dependent Claims 17-20

- | | |
|-----|--|
| 17. | The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs. |
| 18. | The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable. |
| 19. | The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories. |
| 20. | The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports. |

148. Claims 17-20 recite identical limitations to claims 3-5 and 7, respectively, and are satisfied for the same reasons explained previously. *See above* §V.A.5-7, 9 (Claims 3-5, 7).

- | | |
|---|---|
| 1 | 3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs. |
| 2 | 4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable. |
| 3 | 5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories. |
| 4 | 7. The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports. |

- | | |
|---|--|
| 1 | 17. The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs. |
| 2 | 18. The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable. |
| 3 | 19. The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories. |
| 4 | 20. The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports. |
| 5 | |

B. Ground 4: Cornelius, Samaan, and Gorecki

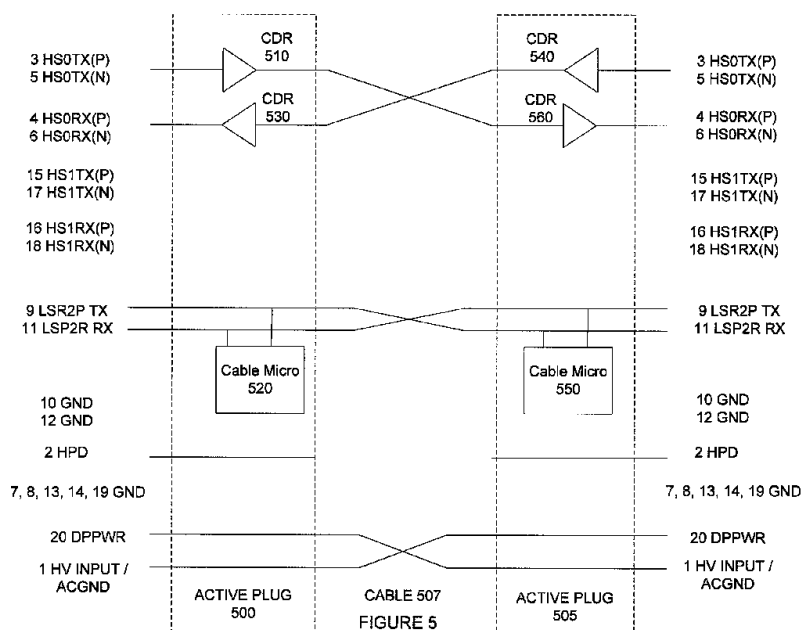
149. It is my opinion that a POSITA would have found the Challenged Claims obvious based on the teachings of Cornelius, Samaan and Gorecki.

Cornelius is Apple prior art that teaches an active cable, where CDR circuitry at both ends of the cable “retime[s] data” and perform other functions including equalization. Ex-1006, 6:6-32. Samaan is an Intel paper that teaches retimer architectures that perform CDR and equalization. The motivation to combine and reasonable expectation of success are explained in more detail below. See below §V.B.3.[1a] (Motivation to Combine subsection).

1. U.S. Patent No. 8,516,238 (“Cornelius”) (Ex-1006)

150. I have reviewed the Cornelius reference. Cornelius was filed on June 30, 2011 and issued on August 20, 2013, claiming priority to February 23, 2011. Therefore, Cornelius is prior art under post-AIA §102(a) before June 21, 2019. *See* below, Appendix 4 (Understanding of the Law).

151. Cornelius teaches “an active cable” that has “the ability to retime data at each of its ends” (Ex-1006, 6:6-10), using “clock and data recovery circuits” (CDR circuits) within each active plug located at the cable’s ends. Ex-1006, 6:11-29, Fig. 5:



152. Cornelius CDR circuits provide more than typical clock/data recovery; they also “employ equalizer circuits, buffers, emphasis, and de-emphasis circuits” that can be calibrated to improve “the reliability and accuracy of data connections.” Ex-1006, 6:30-32, 11:45-48.

153. Cornelius is analogous art to the '233 patent because it is in the same field of endeavor as the '233 patent (high-speed communications). Cornelius discloses an active cable that provides a “high-speed connection.” Ex-1006, 3:27-42, 3:54-64, 4:22-31, 4:45-54, 6:11-24, 8:57-9:6. Each of the two active plugs “provides” and “receives high-speed signals.” Ex-1006, 6:11-20, Fig. 5. Cornelius is reasonably pertinent to the problem addressed by the '233 patent because Cornelius teaches pre-equalization/equalization for high-speed serial

communications. Ex-1006, 6:30-42, 6:6-20, 11:45-62; *see* above §V.A.2

(explaining the problem addressed by the '233 patent).

2. High-Speed Serial Bus Repeater Primer: Re-driver and Retimer Micro-architecture, Properties, and Usage, Intel Corp., Revision 1.2” (“Samaan”) (Ex-1007)

154. I have reviewed the Samaan reference. Samaan is a white paper that was published in 2015. Ex-1007, ¶1. Therefore, Samaan is prior art to the '233 patent under post-AIA §102(a) before June 21, 2019.

155. **Prior Publication.** A declaration by librarian June Munford confirms Samaan was published and publicly accessible before the priority date of the '233 patent. Ex-1018. Samaan was uploaded to and freely available for download through Intel's website at least by February 2, 2016. Ex-1018, ¶7. Intel was a large corporation that developed many components for computer and networking devices, and had a well-funded research department. Intel published whitepapers on technical topics, including for data transmission. Researchers and academia would seek out such whitepapers to learn about Intel's research and development efforts and trends in industry.

156. In my own research, I have occasionally sought out white papers, datasheets, application notes, or the like that Intel and other large, well-known vendors publish on their websites to disseminate to the public. I recall that Intel's website included search functionality (which it still retains) that allowed a web-

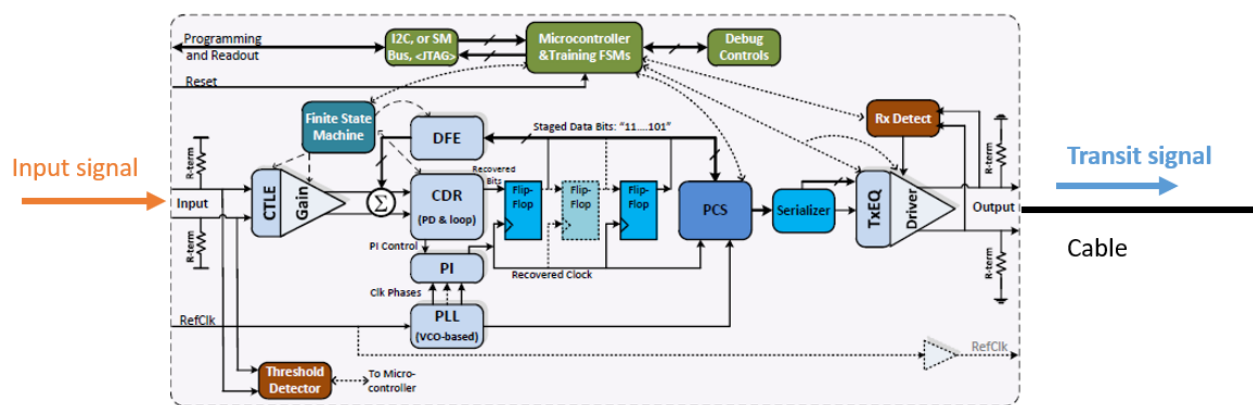
surfer to locate information of interest by searching with keywords. A POSITA would have found it simple to locate a white paper, technical brief, specification, manual, or other technical document on Intel's website, which would require only a few clicks and a search. For example, searching for the title of Samaan, "High-Speed Serial Bus Repeater Primer," returns a single search result (Ex-1035, 000001) with a webpage (entitled PCI Express® Architecture) providing technical documentation on the PCI Express standard, which has a link to Samaan under the heading "White Papers" (Ex-1033 ("High-Speed Serial Bus Repeater Primer")). Searching with other related search terms such as "Retime & PCI express," "Retimer & PCIe," "Repeater & PCIe," and "retimer repeater" similarly returns results with the PCI Express® Architecture page, with a link to Samaan, exposed on the first page of search results. Ex-1035, 000003, 000007-000008, 000011, 000015.

157. Snapshots taken by the Internet Archive of Intel's PCI Express® Architecture webpage and the link "High-Speed Serial Bus Repeater Primer" confirms that this webpage was available and provided a link for users to access Samaan before the priority date of the '233 patent. Ex-1018, 000105-000106, 000029-30. This same page is cited on a Wikipedia page for the entry PCI Express. Ex-1034, 000028 (under External Links: "'PCI Express Architecture', Developer Network, Intel Ex-1018, 000105-000106, 000029-000030. I note that Cornelius

cites to the very same Wikipedia page on PCI Express, and POSITAs like the inventors of Cornelius would have followed such links to search for more information. Ex-1006, 000002 (“Other Publications”).

158. It was customary for researchers to look up cited references to obtain further details or other information related to a topic of research. Indeed, the Munford declaration further demonstrates that interested members of the public, such as researchers at Texas Instruments, did in fact access Samaan and cite it in their own work before July 1, 2019. Ex-1018, ¶18, ¶¶11-17.

159. **Samaan Overview.** Samaan describes the architecture and usage of SerDes repeaters, including re-drivers and re-timers, in high-speed copper link systems. Ex-1007, ¶¶2-6. Samaan details how re-timers utilize equalization and clock and data recovery to extract bits from an input signal, and then perform pre-equalization and modulation to transmit the signal on the other end. Ex-1007, Fig. 35:



160. Samaan is analogous art to the '233 patent because it is in the same field of endeavor as the '233 patent (high-speed communications), as clearly suggested by Samaan's title. Ex-1007, Title. Samaan explains that it targets professionals working with high-speed serial buses and specialized signal integrity components (re-drivers and re-timers) that ensure optimal performance and reliability in high-speed data transmission environments. Ex-1007, ¶1, ¶¶5-8, ¶¶12-15. Samaan is reasonably pertinent to the problem addressed by the '233 patent because Samaan likewise recognizes the problem of channel loss at high data rates (Ex-1007, ¶¶2-4) teaches pre-equalization/equalization as a solution for high-speed serial communications. Ex-1007, ¶1, ¶¶5-8, ¶¶207-220, Figs. 34-35; *see above* §V.A.2 (explaining the problem addressed by the '233 patent).

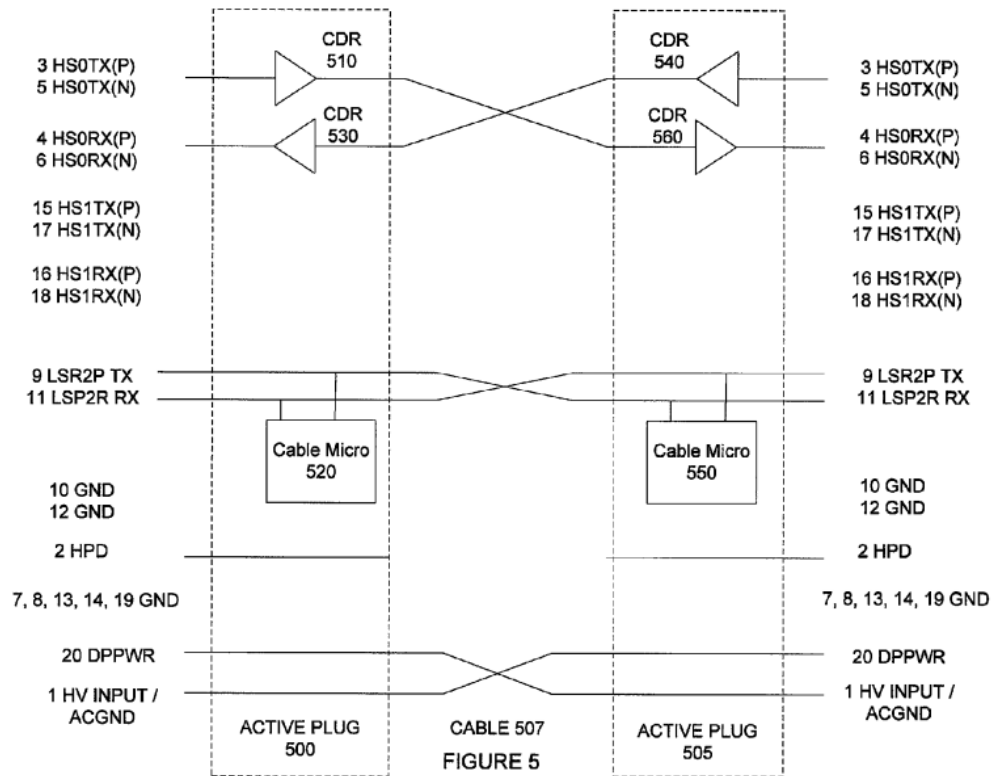
3. Independent Claim 1

161. As an initial matter, for each of the below limitations, the “first” and “second” designations can be swapped between elements at one end of the active cable versus the other. Cornelius' cable design is symmetric to support bi-directional communication; each side has identical components and operation. E.g., Ex-1006, 6:14-23, 8:20-40, Claims 1, 6, Figs. 5-6.

[1pre] A cable that comprises:

162. I understand that a preamble generally does not state a claim limitation. Nonetheless, it is my opinion that Ground 4 teaches it.

163. Cornelius teaches an active cable. Ex-1006, Title, 5:33-39, 6:6-20, 8:20-40, Figs. 5-6, Claims 1-10. Figures 5 and 6 provide exemplary illustrations of the active cable.



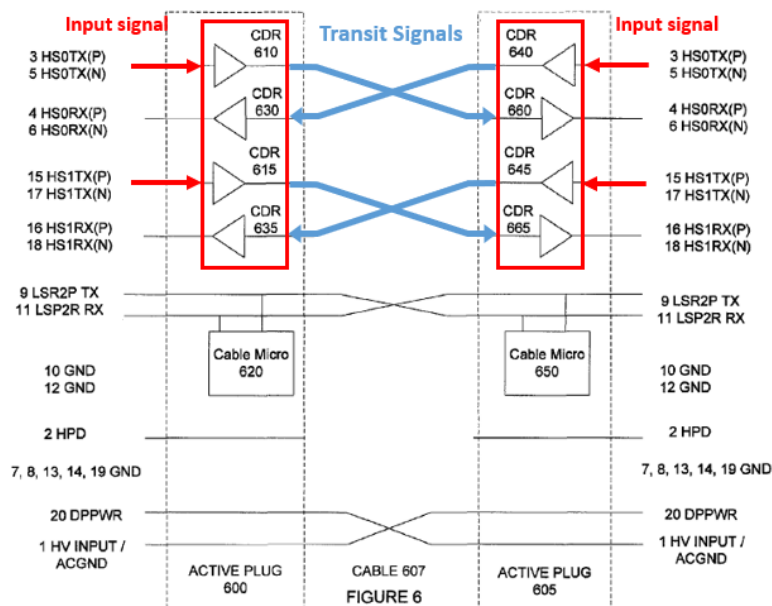
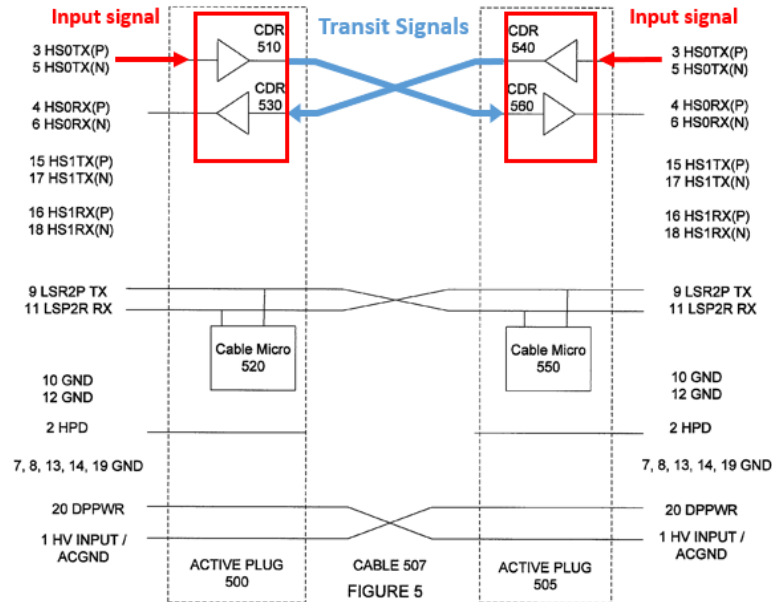
[1a] a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;

164. As an initial matter, Cornelius teaches “active plugs” located at each end of the active cable. Ex-1006, 6:11-20, 8:20-40, Figs. 5-6. “Each active plug includes dual clock and data recovery circuits” (e.g., CDR 510 and 530 in one plug, or 540 and 560 in the other). Ex-1006, 6:11-24, Figs. 5-6. Although referred to as CDR circuits, Cornelius’s “CDR” circuits perform functions beyond merely

recovering clock and data: they also retime data (Ex-1006, 6:15-16) and “employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate.” Ex-1006, 6:30-33.

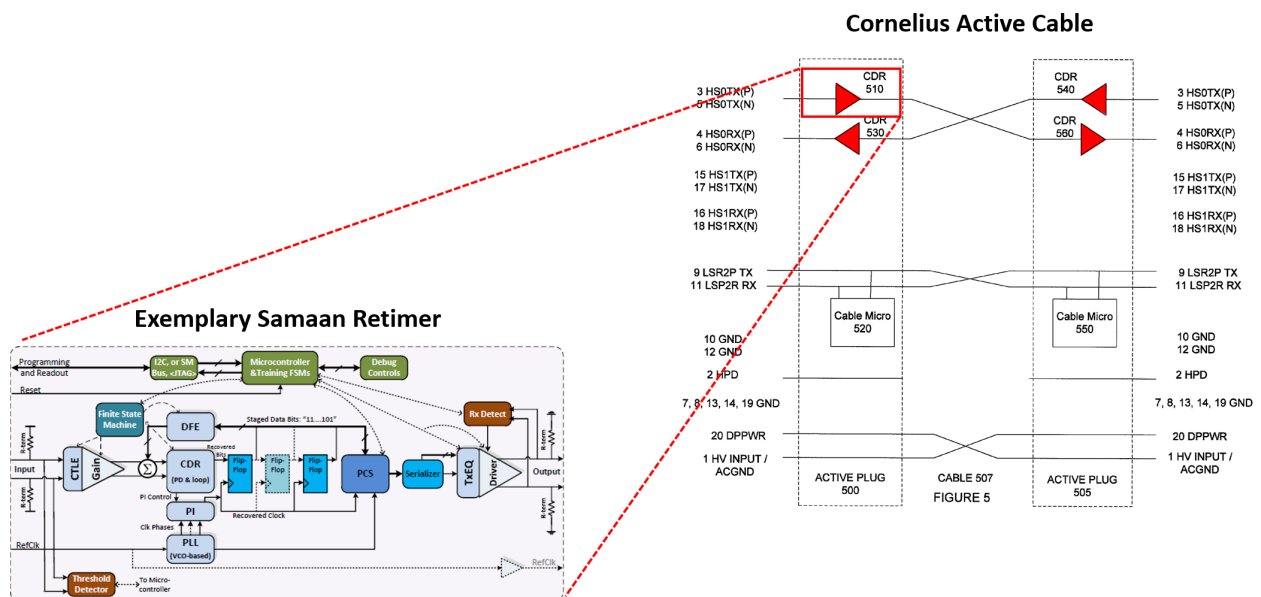
165. Ground 4 teaches a **first DRR device**. For example, Cornelius teaches CDR/retimer circuitry that operate on incoming signals to perform clock and data recovery. Ex-1006, 6:11-24, Figs. 5-6. After recovering data from the input stream, the CDR circuitry then “retime[s]^[8] signals received at an input.” Ex-1006, Claim 1, 6:11-24, 8:20-26. Therefore, Cornelius’ CDR/retimer circuitry re-modulates the input data stream by converting the extracted data bits into a signal for transmission over the communications channel (cable), which has independent jitter and timing characteristics from the input signal. The collective CDR/retimer circuitry in Cornelius’s active plug comprise a DRR device:

⁸ Patent Owner has taken the position that limitation [1a] is satisfied by the presence of retimers in an active cable. Ex-1024, 000003-000005 (highlighting and pointing to Credo’s retimers and their “retiming” capability as evidence of remodulation and data extraction); Ex-1022, 000002-000008 (same, highlighting and pointing to Broadcom’s and Marvell’s retimers); Ex-1023, 000003-000010 (same).

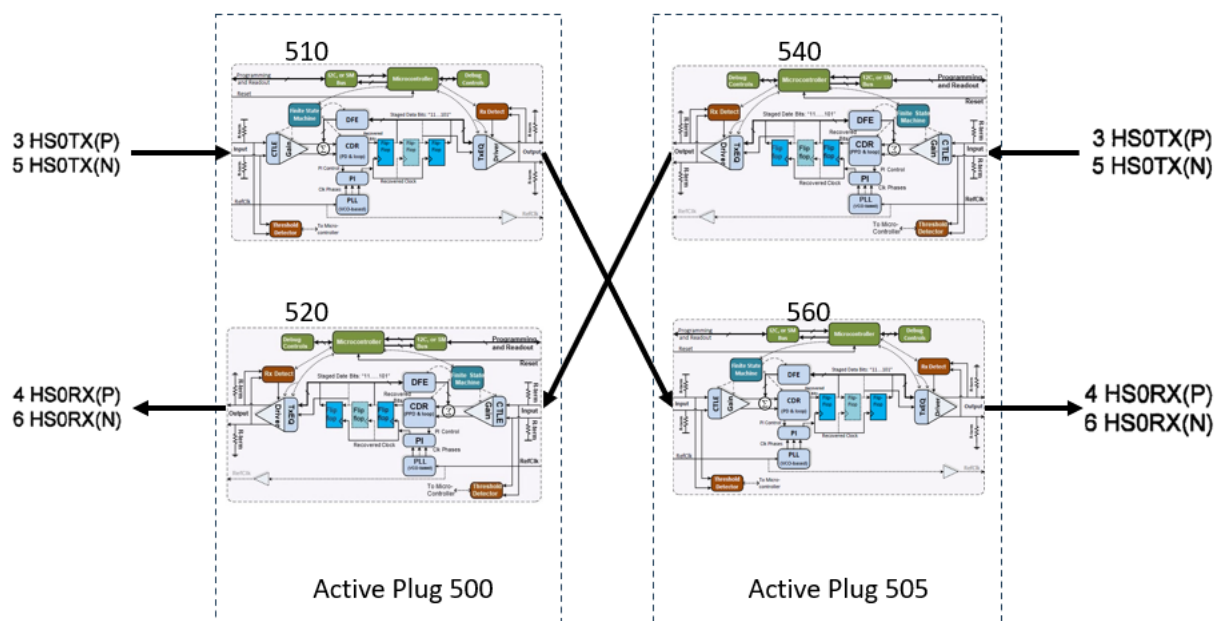


166. Samman provides additional details for the retimer functionality in Cornelius's active plugs. Samaan teaches two flavors of retimers (protocol-aware and unaware); either is sufficient for the combination of Ground 4. Samaan's retimer architectures (both protocol-aware and unaware) provide the functionalities Cornelius describes in its active plug and CDR (Ex-1006, 6:6-32), including

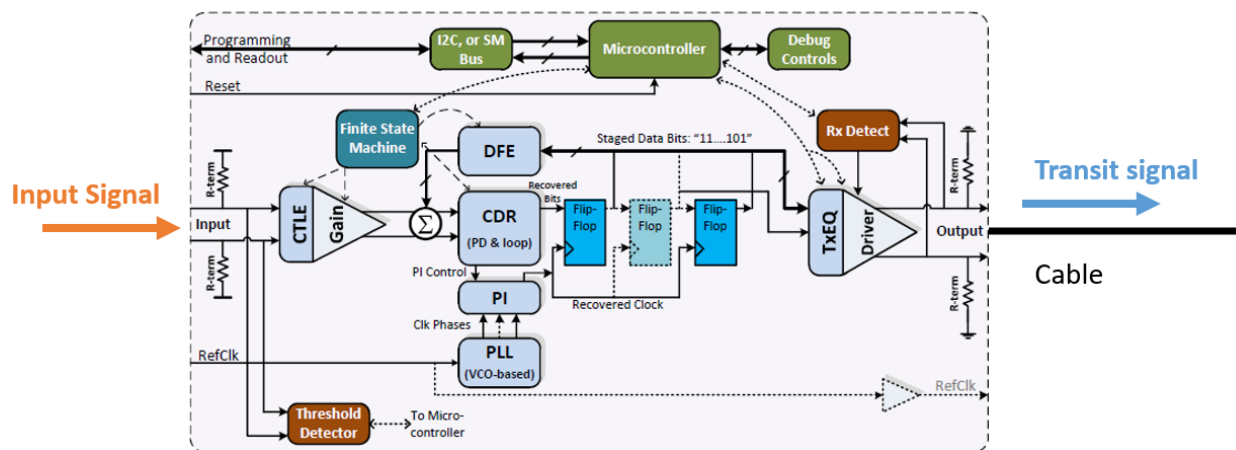
retiming functionality, CDR, equalizer circuits, buffers, emphasis (pre-emphasis, which leads to what Samaan sometimes calls pre-shoot equalization), and de-emphasis circuits (which leads to what Samaan sometimes calls post-shoot equalization). Ex-1007, ¶225, ¶79, ¶91, Figs. 34-35. Thus, a POSITA would have applied Samaan's retimer teachings to Cornelius's active plugs; I have illustrated an example of this combination below. Ex-1006, Fig. 5; Ex-1007, Figs. 34-35.



Cornelius + Samaan

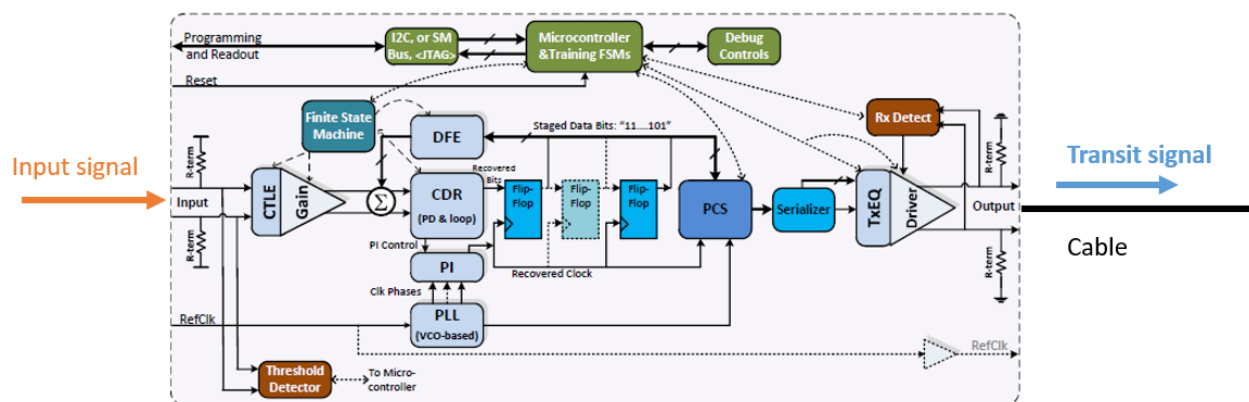


167. Each retimer from Samaan residing in Cornelius’s active plugs performs clock and data recovery (“CDR”) to extract “data bits” (stored in flip flops) from the incoming data stream. Ex-1007, ¶202 (“Re-timer has a Clock Data Recovery circuit....A re-timer converts an incoming analog bit stream into purely digital bits that are stored (staged) internally.”), ¶¶203-207, ¶¶208-212, ¶¶216-217 (“...CDR is a circuit which can extract both clock and the data from an incoming (specially-encoded) data stream.”), Figs. 34-35. Next, the retimer re-modulates the digital bitstream and “re-transmits the digital data anew.” Ex-1007, ¶202. For this re-modulation process, in a protocol-unaware retimer, the data signal flows through TxEQ for output equalization and then the driver. Ex-1007, ¶¶216-231, Fig. 34:



For the re-modulation process in protocol-aware retimers, the data signal flows through the physical coding/decoding sublayer (PCS), serializer, TxEQ, and driver.

Ex-1007, ¶¶218-231, Fig. 35:



168. Both retimer architectures re-modulate the inbound data stream by converting the extracted data bits from the incoming data stream into a signal for transmission over the communications channel (cable), which has independent jitter and timing characteristics from the incoming signal. Ex-1007, ¶15, ¶202.

169. Ground 4 teaches a first DRR device (e.g., CDR/retimer circuitry) **that exchanges inbound and outbound multi-lane data streams**. The '233 patent defines “inbound” and “outbound” from the host device’s perspective. *See* above §IV. The host device transmits outbound data signals to the active cable via the TX pins (3, 5, 15, and 17) and receives inbound data signals from the active cable through the RX pins (4, 6, 16, and 18). Ex-1006, Fig. 3, 4:23-54, 3:33-42, 3:65-4:9. Cornelius describes transmit (Tx) and receive (Rx) from the host’s perspective. Ex-1006, Figs. 3, 5, 6:16-24. The DRR device exchanges Tx and Rx signals from/to the host device through an end connector plug, with pins shown below. Ex-1006, 6:16-24, Ex-1006, 4:22-38 (“High-speed transmit pins 3 and 5, and 15 and 17...[H]igh-speed receive signals may be placed on pins 4 and 6, and 16 and 18.”), Figs. 2-3, 5-6.

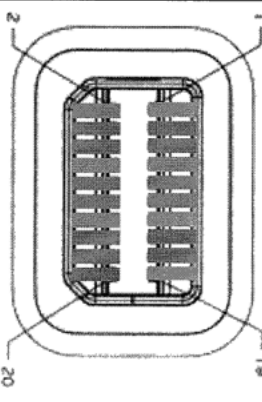
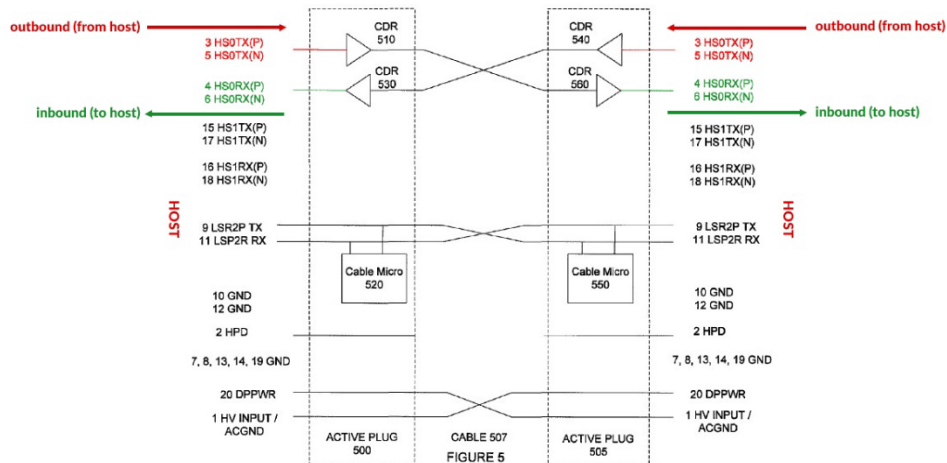
DP	T29	Pin		Pin	T29	DP
HPD	HPD	2		1	HV INPUT / ACGND	GND
CFG1	HS0RX(P)	4		3	HS0TX(P)	DP0(p)
CFG2	HS0RX(N)	6		5	HS0TX(N)	DP0(n)
GND	GND	8		7	GND	GND
DP3(p)	(RESERVED) GND	10		9	LSR2P TX	DPI(p)
DP3(n)	(RESERVED) GND	12		11	LSP2R Rx	DPI(n)
GND	GND	14		13	GND	GND
AUX(p)	HS1RX(P)	16		15	HS1TX(P)	DP2(p)
AUX(n)	HS1RX(N)	18		17	HS1TX(N)	DP2(n)
DPPWR	DPPWR	20		19	GND	GND

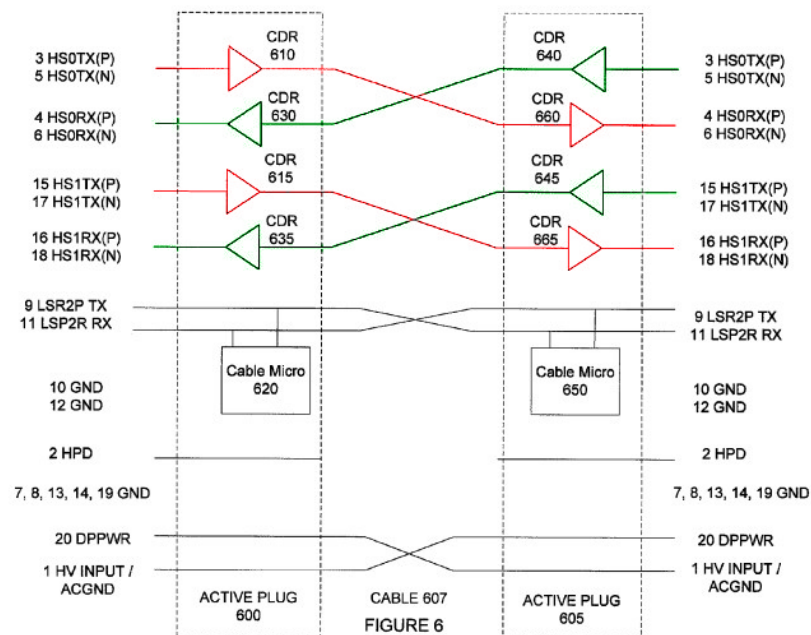
FIGURE 3



170. Cornelius' Figure 5 above shows two CDR circuits in each active plug. Ex-1006, Fig. 5, 6:11-20. Cornelius explains that, from the host's perspective, pins 3 and 5 carry high-speed transmission signals (to CDR 510), while pins 4 and 6 carry high-speed receive signals (from CDR 530). Ex-1006, Fig. 5, 6:11-20. In Figure 6, as shown below, additional clock and data recovery circuits 615 and 635 have been added to active plug 600, while clock and data recovery circuits 645 and 665 have been added to active plug 605." Ex-1006, 8:20-26, Fig. 6. Accordingly, like the active plug 500, active plug 600 carries high-speed transmission signals on pins 3, 5, 15 and 17 (to CDRs 610 and 615), and carries high-speed receive signals on pins 4, 6, 16 and 18 (from CDRs 630 and 635). Ex-1006, 8:20-26, Fig. 6. When Cornelius's figures and specification are considered together, it is clear that data flows from CDR 610 to 660 and from CDR 640 to 630, following the direction of the arrows, which is the normal convention in the

field, and transmitted signals are provided on pins 3, 5, 15, and 17 with received signals are on pins 4, 6, 16, and 18.

171. Each DRR device exchanges more than one lane of inbound and outbound data streams (on pins 4, 6, 16 and 18 for inbound data to the host, and on pins 3, 5, 15 and 17 for outbound data from the host). The signals on these pins carry data streams. As explained above, each CDR/retimer circuitry recovers data, as a stream of bits, sent from the host; it also sends a stream of data bits in the opposite direction, to the host. *See* Ex-1006, Figs. 5-6; Ex-1007, ¶202, Figs. 34-35 (flip flops storing recovered bits in retimer).



172. Cornelius further teaches exchanges inbound and outbound multi-lane data streams **with a first host interface port via a first end connector plug**. For example, Cornelius teaches an “active cable” that “includes two active plugs...one

on each end of cable.” Ex-1006, 6:11-20 (“active plugs 500 and 505, one on each end of cable 507”), 8:20-26 (“active plug 600” and “active plug 605”), Fig. 6 (“cable 607” connecting “active plug 600” and “active plug 605”).

173. Each active plug comprises an end portion that is a connector plug, which is used to connect one end of the active cable to corresponding host devices such as “computer 110 communicating with computer or display 220.” Ex-1006, 8:27-40 (“...a host device connected to plug 600...”), 3:28-42, 3:47-53 (“computer 110 may drive a display of an all-in-one computer, a second computer ... or other type of device.”), Figs. 2-3. Cornelius teaches several exemplary hosts, including computers, displays, and other high-speed I/O sources or sinks. Ex-1006, 6:6-10 (using active cable to connect “an HSIO source or host and an HSIO sink or endpoint.”), 3:37-64, 5:33-39 (“an active cable is required between the HSIO source or host and the HSIO sink or endpoint.”). The host interface port would be the mating interface where the end connector plug is inserted. Cornelius teaches or suggests this, and it would have been obvious because Cornelius teaches a connector pinout for the active plug to exchange inbound and outbound data streams with a host. Ex-1006, 4:22-38, Fig. 3. Without an interface port to connect to, the active cables would not operate as Cornelius teaches.

174. For at least these reasons, Ground 4 teaches limitation [1a].

175. **Motivation to Combine.** As early as 2011, Apple and Intel co-developed high-speed interface and active cable technologies that would later become known as Thunderbolt. Ex-1013, 000001. The collaboration made waves and was much-discussed in the computing industry, with Apple developing and marketing the cable (Ex-1014, 000001; Ex-1013, 000001-000002), and Intel providing the port and retimer architecture used for the active plugs at each end of the cable. Ex-1016, 000001-000002; Ex-1015, 000003 (“Thunderbolt port and controller specification are entirely Intel’s”). Mac computers included Thunderbolt ports starting in 2011 (Ex-1013, 000001), and other vendors began providing Thunderbolt solutions in the years after. Ex-1009, 000001 (describing ISL37231 “retimer for active copper cable applications”); Ex-1008, 000003-000005 (describing ISL37231 retimers in Thunderbolt connectors). Thunderbolt cables were on the market by 2011. Ex-1016, 000001.

176. By 2019, a POSITA interested in developing active cables would have been motivated by Apple and Intel’s collaboration to look to Apple’s cable art (such as Cornelius) and Intel’s technical references addressing transceiver/retimer architecture and implementation (such as Samaan). In particular, a POSITA would have been motivated to apply Samaan’s teachings to Cornelius, including for example, using Samaan’s retimer teachings to implement the “circuits for retiming data” in Cornelius’s active plugs. Ex-1006, 6:11-20, 8:20-26, Figs. 5-6.

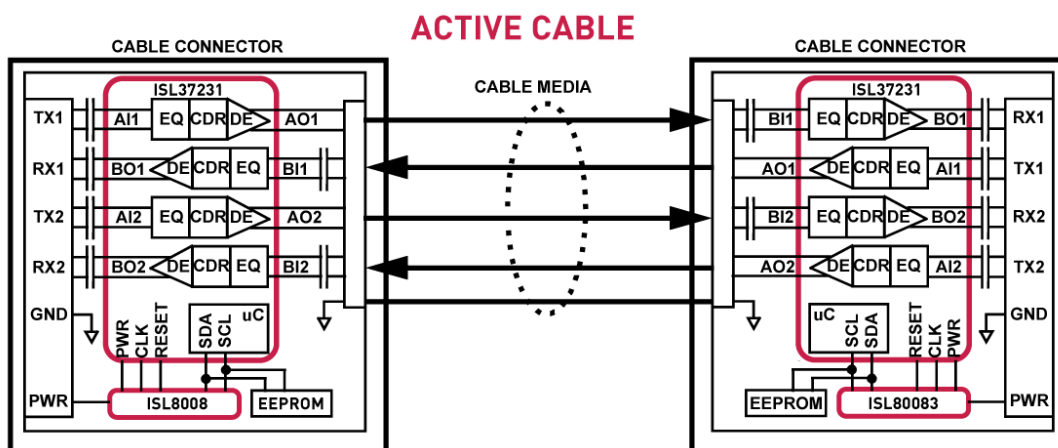
177. A POSITA would have been motivated to combine for several additional reasons, explained below. First, the references provide express motivation to combine. Cornelius teaches that the active plugs at both ends of the cable include CDR circuits that “retime signals.” Ex-1006, Claim 1. To implement such “circuits for retiming data,” Cornelius contemplated designs beyond simple CDR circuits: Cornelius teaches that its particular CDR circuits “employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate,” reflecting a comprehensive approach to signal integrity beyond mere clock and data recovery. Ex-1006, 6:30-32. However, Cornelius does not provide implementation details for those retimers, which was understandable because Apple focused on the broader cable assembly of Thunderbolt while Intel provided the retimer architecture and implementation. Samaan provides the missing implementation details and further enhances the designs contemplated by Cornelius. Cornelius therefore provides motivation to combine its teachings with known retimer implementations, and a POSITA would naturally have looked to known retimer architectures including those from Intel (e.g., Samaan), along with known retimer techniques and applications. Ex-1006, 12:21-34 (providing motivation to modify its teachings). This would have been a combination of prior art elements according to known methods (e.g., as taught by Cornelius and Samaan) to yield predictable results (e.g., a retimer in an active cable, as Cornelius teaches).

178. Similarly, Samaan applies its teachings to cables. For example, when discussing retimer “Hot Plug,” Samaan teaches why re-timers are “usable in a reversible cable (where either end can be plugged into the upstream or downstream component).” Ex-1007, ¶238. Samaan explains how re-timers are used with “SFI” (Ex-1007, ¶204), and elsewhere teaches cable applications for SFI. Ex-1007, ¶72 (“Furthermore, in the Case of USB3, SATA3, and even SFI, the cables or devices connected to a host may vary in length”). When discussing SFI, Samaan cites to the Specification for SFP+, which is the Small Form-factor Pluggable module standard (Ex-1007, 000072, ¶204 (citing “[24]”)) that provides native support for various Ethernet standards, for example, 1Gb/s Ethernet, 10Gb/s Ethernet, etc. Ex-1025, Tbl. 1. SFP+ modules were also frequently used for active Ethernet cables. Ex-1011 (datasheet for TE SFP+ cables, supporting 1 and 10 Gigabit Ethernet), Ex-1012, 000001, 000003-000005, 000008-000009 (various Cisco SFP+ compliant transceiver and cable modules supporting 40 Gigabit Ethernet); Ex-1019, Video Description (“10G SFP+ direct attach copper cable ... or 10G SFP+ DAC cable assembly, is a twinaxial cable assembly that has a length of copper cable and terminates with SFP+ connector modules on either end.”), Ex-1019, Video Description (10G SFP+ direct attach copper cables and transceiver supporting Ethernet protocols). Therefore, the combination applies a known technique (e.g.,

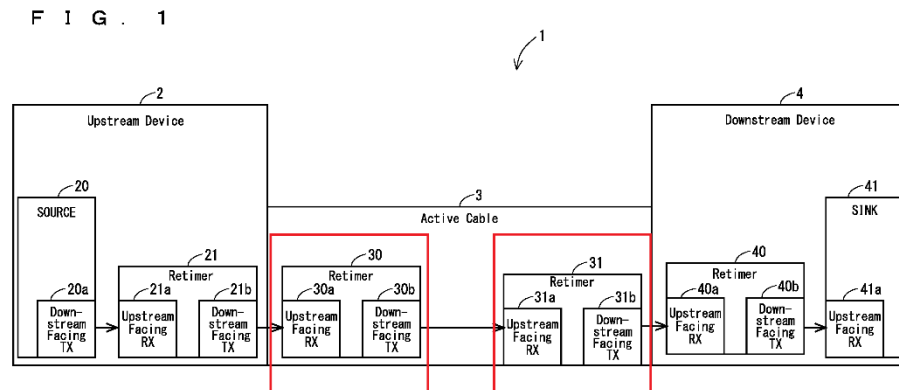
known retimer architectures) to a known device (e.g., active cables) that was ready for improvement to yield predictable results (e.g., a retimer in an active cable).

179. Additionally, a POSITA would have been motivated to use Samaan's retimer teachings in Cornelius's active cables based on the functionality and benefits provided by Samaan's retimer architectures, including for example (1) upstream and downstream signal independence, which provides jitter isolation; (2) enhanced debug capabilities such as eye margining and compliance pattern testing; and (3) increased channel length. Ex-1007, ¶15, ¶202.

180. The prior art provides teaching, suggestion, and motivation to incorporate retimers at both ends of active cables; this was widespread by March 2019. *See, e.g.*, Ex-1009, 000001 (discussing retimer chips installed on an active cable's connectors, providing the benefits of “thinner gauge cable”, “extend[ing] cable reach”, and “improved BER”)., Fig. 1:



Ex-1026 (similar Texas Instrument products). The prior art recognized numerous benefits from using retimers in active cables, including for example that retimers help “avoid high-speed serial bit stream signal quality degradation” and “extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the retimer.” Ex-1010, ¶12, Fig. 1:



181. The combination would not have changed the principle of operation for either reference. Applying Samaan’s retimer teachings would not have changed the principle of operation of Cornelius because Cornelius already teaches retimers in its active cable and suggests a wide variety of protocols, including Ethernet. Ex-1006, 000002 (citing to “Ethernet” under Other Publications), 6:6-20, Claims 1, 6. Cornelius contemplates clock and data recovery circuits that “employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate.” Ex-1006, 6:30-32. Samaan’s retimer is likewise “[a] device which has a Clock & Data Recovery circuit (CDR[])” coupled to equalization circuits—such as a continuous-time linear equalization circuit (CTLE), a discrete-feedback equalization circuit

(DFE), and transmitter linear equalization (TxEQ) (Ex-1007, ¶¶202-231, ¶15)—that perform the emphasis and/or de-emphasis circuits discussed in Cornelius. Ex-1006, 6:30-32; Ex-1007, ¶225. Both retiming and recover data. Cornelius teaches “dual clock and data recovery circuits for retiming data” to provide “easily recoverable data.” Ex-1006, 6:6-16, Claims 1, 6. Samaan “converts an incoming analog bit stream into purely digital bits that are stored (or staged) internally...A re-timer re-transmits data anew, with new equalization, and new jitter content, unrelated analog-wise to the input bit stream.” Ex-1007, ¶15, ¶202, Figs. 34-35. Therefore, Samaan’s retimer teachings were directly applicable to Cornelius’s active plugs, including its CDR and related circuits. Using Samaan’s retimer architecture in an active cable would not have changed the principle of operation for Samaan because it already teaches or suggests the use of cables, and Samaan provides a high-level retimer architecture that was broadly applicable to a range of physical channels, including active electric cables. When used in an active cable, Samaan’s retimer would operate in the same way and for the same purpose as taught in Samaan—to recover bits from one end and re-transmit them on the other.

182. In addition to the reasons explained earlier in this section, a POSITA would have had a reasonable expectation of success in combining teachings from Cornelius and Samaan because retimers and active electric cables had long been used in the art. Samaan’s retimers reflect the common retimer architectures that

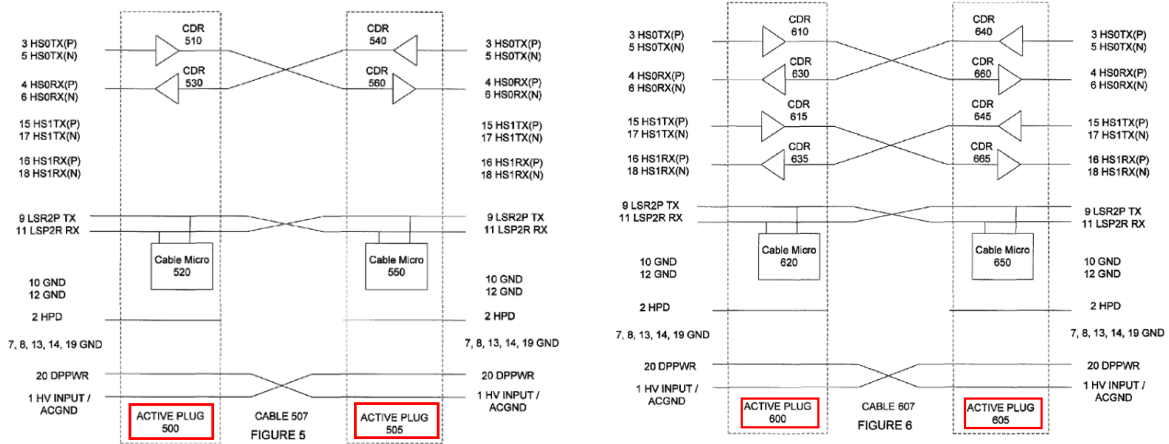
had been used for high-speed serial communications for many years. By the early 2010s, I taught students the same retimer concepts and relevant analog mixed-signal circuit components that are taught by Samaan; therefore, a POSITA with the requisite level of education and experience (*see* above §III) would have known how to use retimers with cables. Active cables were sold on the market and used in data centers by the relevant timeframe (*see* above §II.C). Therefore, a POSITA would have known how to use retimers with active cables.

[1b] second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug
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183. Limitation [1b] mirrors [1a] and differs only by changing “first” to “second.”

184. Ground 4 teaches a symmetric and bidirectional cable with two symmetric DRR devices (one at each end of the cable). Ex-1006, 6:11-20, 8:20-40, Figs. 5-6. As explained above, Cornelius describes that each cable has two active plugs with “one on each end of the cable,” and each active plug further includes CDR/retimer circuitry. Ex-1006, 6:11-20, 8:20-40, Figs. 5-6. The functionalities described apply to both CDR/retimer circuitry. Ex-1006, 6:11-20, 8:20-40, Figs. 5-6. (“[e]ach active plug includes dual clock and data recovery circuits for retiming data.”). This is further illustrated in Figures 5 and 6, which depicts a cable structure

with two identical active plugs located at opposite ends. Ex-1006, 6:11-20, 8:20-40, Figs. 5-6.



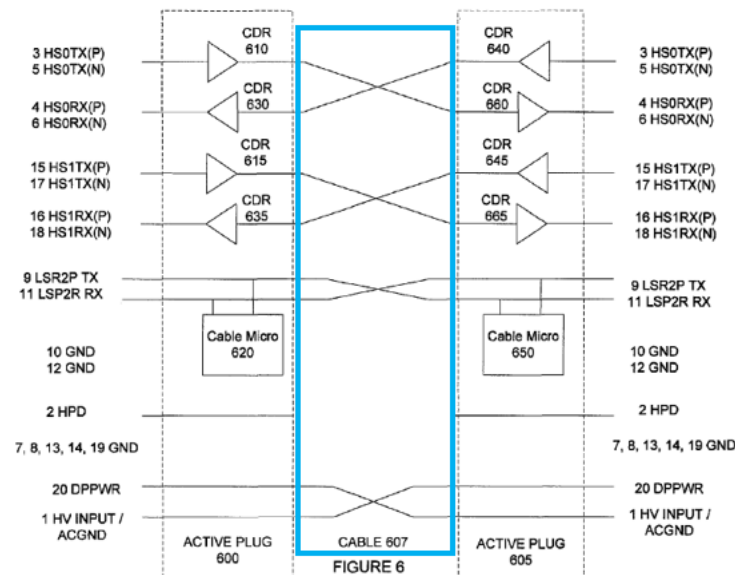
185. Because Cornelius teaches a symmetric cable with two DRR devices, either DRR device would be the first DRR device recited in [1a]; the other would be the second DRR device recited in [1b], for the same reasons explained previously. Ex-1006, 6:11-24, Figs. 5-6. The analysis from [1a] also applies to [1b] and is incorporated here. *See* above §V.B.3[1a]. The interface port and plug for the CDR/retimer circuitry at the other end of the cable would be the second host interface port and second end connector plug.

186. For at least these reasons, Ground 4 teaches limitation [1b].

[1c] electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,

187. Ground 4 teaches **electrical conductors** (e.g., in a cable) **connecting the first and second DRR devices** (e.g., CDR/retimer circuitry in each active plug) **to convey electrical transit signals therebetween**. For example, Cornelius

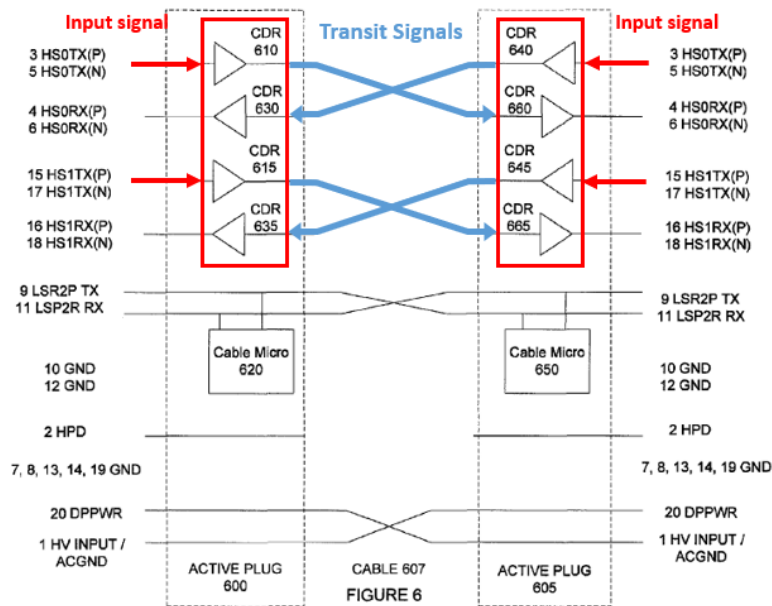
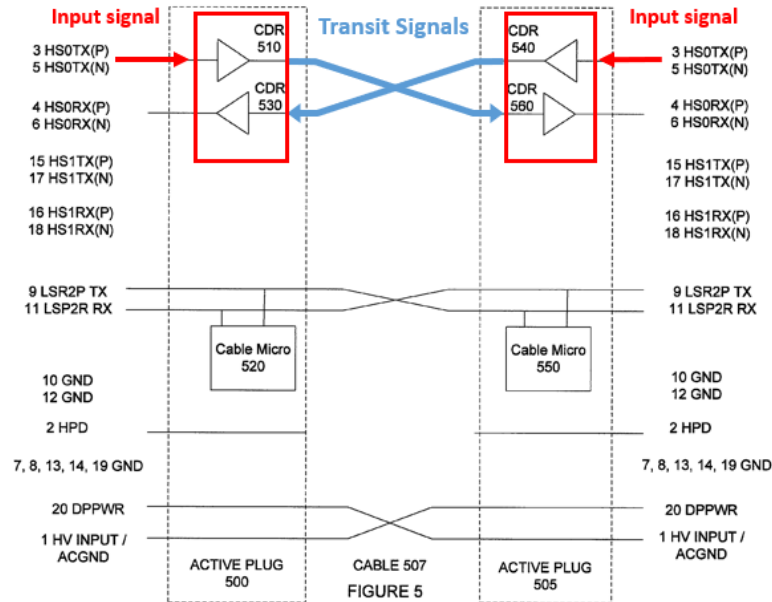
teaches an “active cable” that “includes two active plugs...one on each end of cable.” Ex-1006, 6:11-20 (“active plugs 500 and 505, one on each end of cable 507”), 8:20-26 (“active plug 600” and “active plug 605”), Fig. 6 (“cable 607” connecting “active plug 600” and “active plug 605”). Each active plug includes CDR/retimer circuitry (explained previously, *see* above §V.B.3[1a]). Cornelius teaches pairs of electrical conductors in the cable (blue in figure below) that connect one DRR device (e.g., CDR/retimer circuitry in plug 500/600) to the other DRR device (e.g., CDR/retimer circuitry in active plug 505/605, or vice versa), Figs. 5-6:



188. Cornelius teaches a cable comprising electrical conductors, including “copper or other conductor.” Ex-1006, 7:26-41. Cornelius also includes an option of fiber optics or “a mix of fiber optic and electrical wires” Ex-1006, 6:25-29. A POSITA would have been motivated to apply Cornelius’s teachings for simply

using copper or other conductor, rather than fiber optics, for several reasons, including reduced costs and improved bend radius. *See* Ex-1013, 000001 (Apple switching Thunderbolt from fiber to copper to reduce costs and maintain high performance), Ex-1014, 000002 (same). Furthermore, Apple provided motivation to use copper cabling by moving Thunderbolt cables from their initially envisioned fiber optics (Ex-1013, 000001-000002) to “construct the cable out of copper instead[.]” Ex-1014, 000002; Ex-1013, 000001.

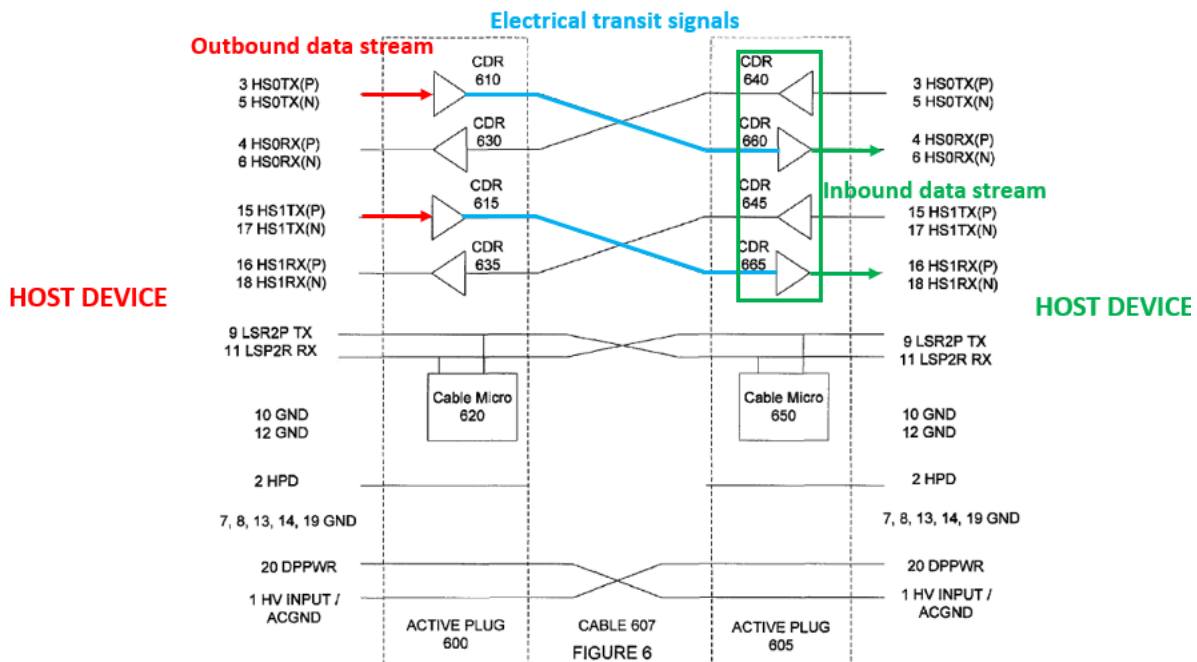
189. The electrical conductors in the cable convey electrical transit signals between the CDR/retimer circuitry. Ex-1006, 7:26-41; Figs. 5-6.



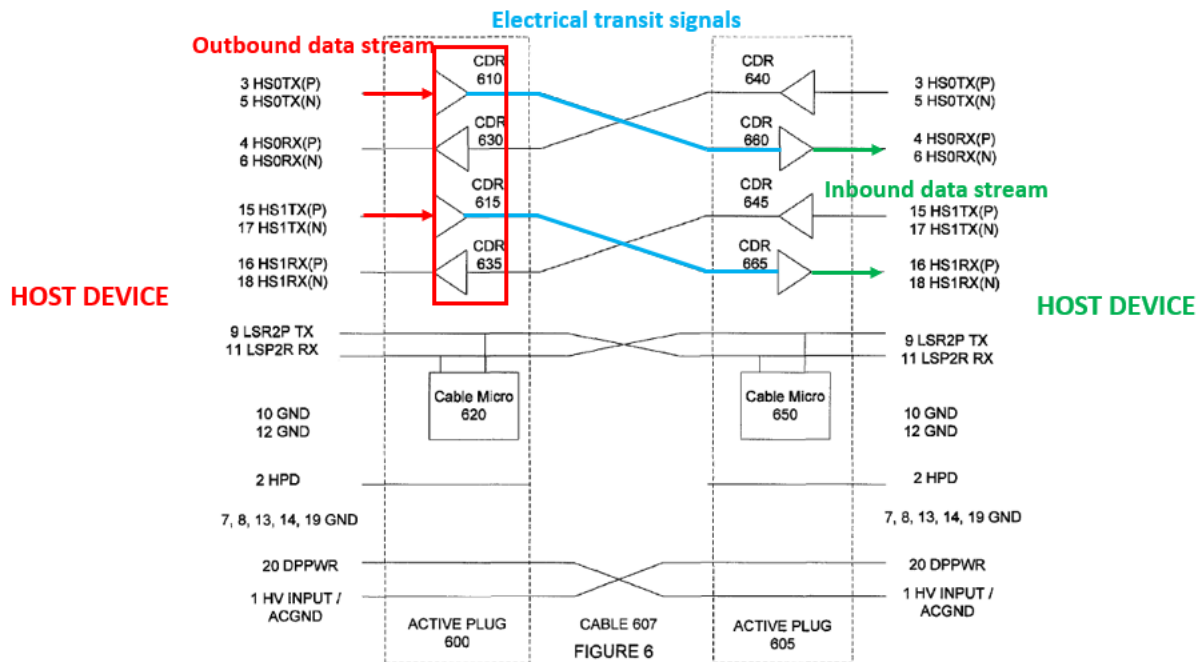
190. For at least these reasons, Ground 4 teaches limitation [1c].

[1d] first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and

191. Ground 4 teaches the **first DRR device** (e.g., CDR/retimer circuitry) **converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port.** For example, after the electrical transit signal traverses the cable and enters the DRR device on the other end, Cornelius performs clock and data recovery to extract data bits from the transit signals; the CDR/retimer circuitry “retime[s] signals received from the cable” (the transit signals), and transmits the converted signals to the host interface port as the inbound data stream (from the perspective of the host). Ex-1006, Claim 1, 6:11-24, 8:20-26, 3:28-64, 6:6-10, 5:33-39, Figs. 2, 5-6.



In the other direction, Cornelius performs clock and data recovery to extract data bits from data stream that is outbound from the host interface port; the CDR/retimer circuitry retimes those signals and transmits the converted signals over the cable as the electrical transit signals. Ex-1006, 6:11-24, Figs. 5-6.



192. Cornelius teaches multiple lanes for the inbound data streams going into the host interface port and the outbound data streams leaving the host interface port. Ex-1006, 6:11-24, 8:20-26, Figs. 5-6. The host interface ports were explained above. *See above §V.B.3[1a].*

193. For at least these reasons, Ground 4 teaches limitation [1d].

[1e] the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,

194. Limitation [1e] mirrors [1d] and differs only by changing “first” to “second.” Ground 4 teaches a cable with two symmetric DRR devices, one at each end of the cable. *See* above §V.B.3[1b] (explaining Cornelius’s symmetric cable design; that analysis applies and is incorporated here). Either DRR device (CDR/retimer circuitry) would be the first DRR device recited in [1d]; the other would be the second DRR device recited in [1e], with corresponding second host interface port, for the same reasons explained previously. The previous analysis also applies to [1e] and is incorporated here. *See* above §V.B.3[1d].

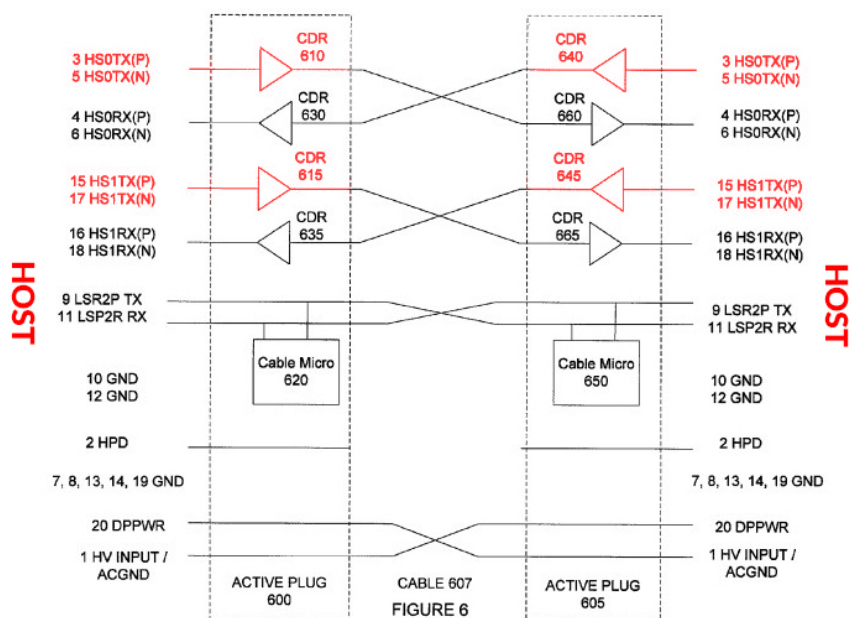
195. For at least these reasons, Ground 4 teaches limitation [1e].

[1f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

196. Ground 4 teaches **the first and second DRR devices** (e.g., CDR/retimer circuitry at respective ends of the cable) **providing pre-equalization of the electrical transit signals**. The DRR devices were explained above (*see* above §V.B.3[1a]-[1b]); for example, Cornelius teaches a bidirectional cable with two symmetric DRR devices (one at each end). *See* above §V.B.3[1b]. The functionalities described apply to both CDR/retimer circuitry. Ex-1006, 6:11-20,

8:20-40, Figs. 5-6. The CDR/retimer circuitry in one active plug is the first DRR device; the other CDR/retimer circuitry in the other plug is the second.

197. Cornelius employs “emphasis, and de-emphasis” in its CDR/retimer circuitry, including on the transmitting side. Ex-1006, 6:30-42, 6:11-20, 8:20-40, Figs. 5-6, Claims 5, 10. This performs pre-equalization by shaping the signal before transmission to account for anticipated channel losses. As explained previously, emphasis and de-emphasis were common ways to implement pre-equalization. *See* above §V.A.3[1f] (explaining pre-equalization). Therefore, Cornelius teaches the first and second DRR devices (e.g., CDR/retimer circuitry) providing pre-equalization of the electrical transit signals.



198. Samaan provides additional support to this limitation. For example, Samaan recognizes the issue of signal distortion in high-speed copper links, and

explains that “a significant fraction of the ... distortion due to channel loss could be compensated for using simple equalization circuits in the transmitter...” Ex-1007, ¶¶5-8. This technique of implementing equalization circuits in the transmitter to compensate channel loss is pre-equalization. As Samaan explains, the protocol-unaware and protocol-aware retimer architectures both include an “output driver with TxEQ”/“output TxEQ driver.” Ex-1007, ¶¶207-220, Figs. 34-35.

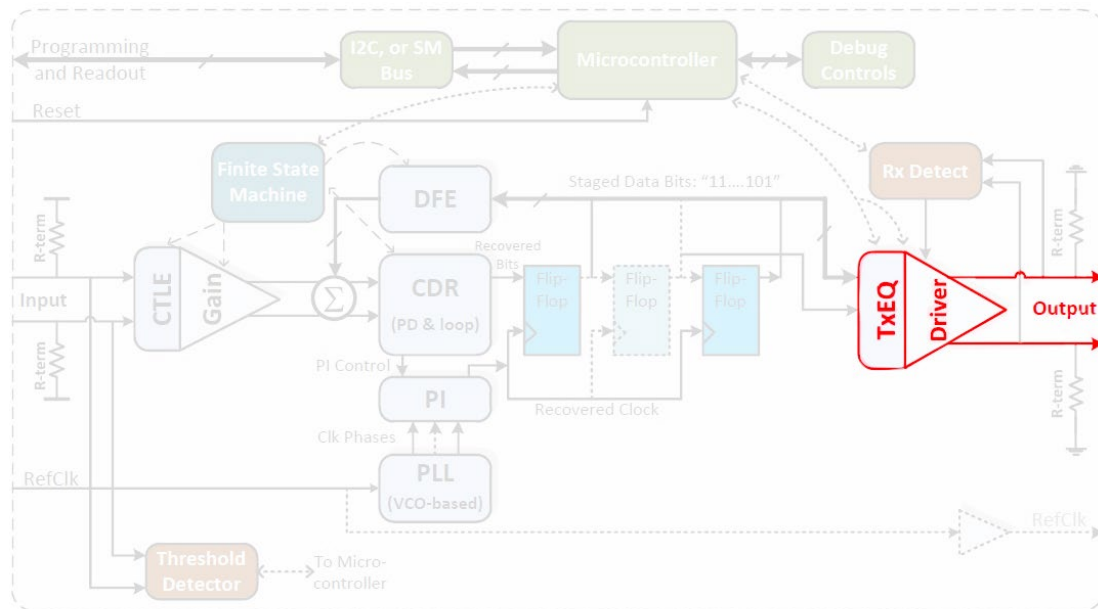


Figure 34 Conceptual micro-architecture of a “Bit Re-timer”, showing input CTLE, AGC, DFE, a CDR, and a data path connected directly to an **output driver with TxEQ**.

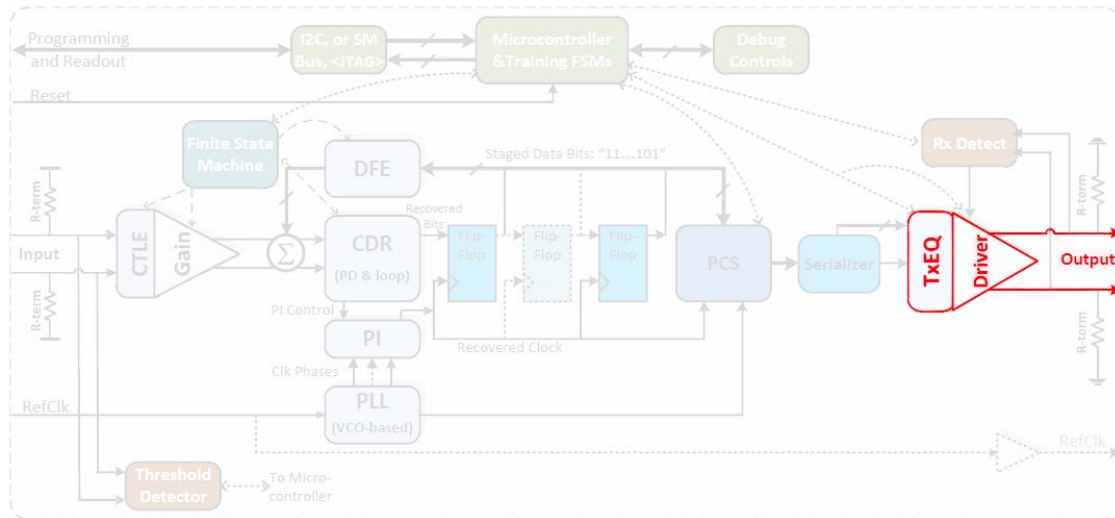
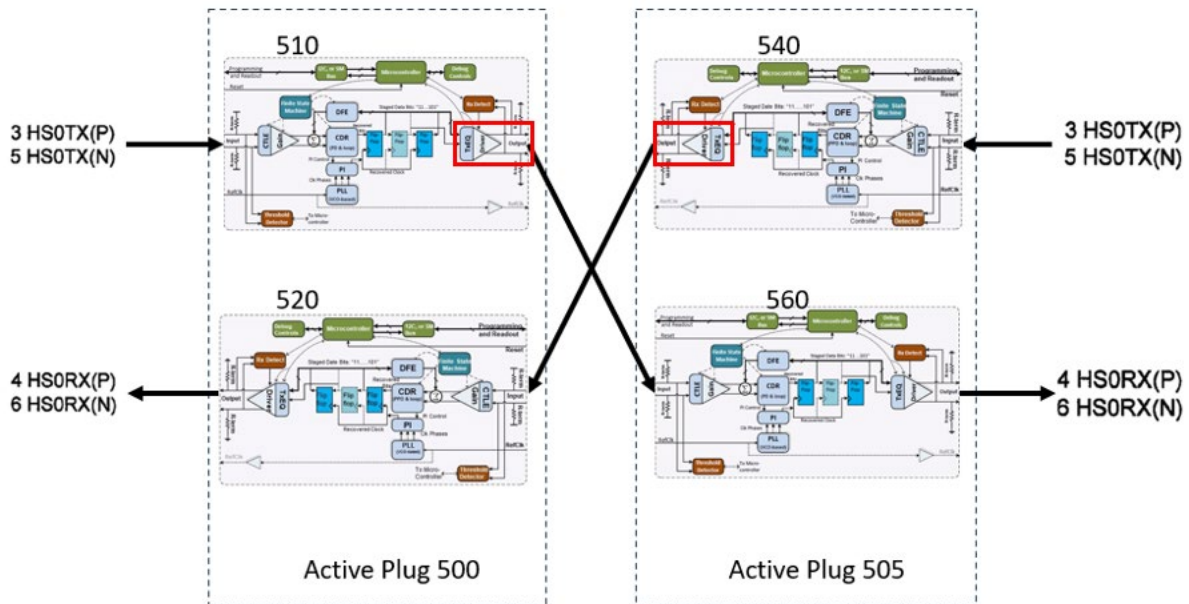


Figure 35 Conceptual micro-architecture of a “Protocol-aware Re-timer”, showing input equalization, a CDR, and a data path connected to a PCS, Serializer, and **output TxEQ driver**, with a Micro-controller.

199. Samaan explains that the “output TxEQ” circuit is “used to add de-emphasis and usually pre-emphasis also to the output.” Ex-1007, ¶225, Fig. 35. For the cable-facing transmitting side of an active plug, the output would be the electrical transit signal that is sent over the cable; I have illustrated an example of this combination with Cornelius below. *See above* §V.B.3[1a] (explaining how and why Samaan’s retimer architectures would have been applied to Cornelius’s active cable). Here, pre-emphasis and de-emphasis both implement pre-equalization, applied at the transmitter, to improve signal-to-noise ratio by emphasizing or de-emphasizing the magnitude of some frequency components before the signals are sent over the channel. Therefore, Samaan also teaches the first and second DRR devices providing pre-equalization of the electrical transit signals.

Cornelius + Samaan



200. Ground 4 teaches the first and second DRR devices providing pre-equalization of the electrical transit signals **using transmit filter coefficient values stored in nonvolatile memories**. For example, Cornelius explains the channel compensation (equalization) circuit “may be adjusted using various parameters,” referring to filter coefficients, which were parameters for equalization, that “may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation.” Ex-1006, 11:45-62. For parameters to be stored as presents during manufacturing, they would obviously have been stored in nonvolatile memory (otherwise the parameters would be lost).As Samaan explains, the output TxEQ circuit (a equalization circuit) “is a true FIR filter,” such as a three-tap FIR filter using filter “coefficients” including “pre-

cursor” and “post-cursor” coefficients. Ex-1007, ¶¶78-81, ¶225, Figs. 21-22,⁹ 34-35. The FIR filter is implemented for transmission and therefore is a transmit filter. Ex-1007, ¶225, ¶¶78-81, Figs. 21-22, 35.

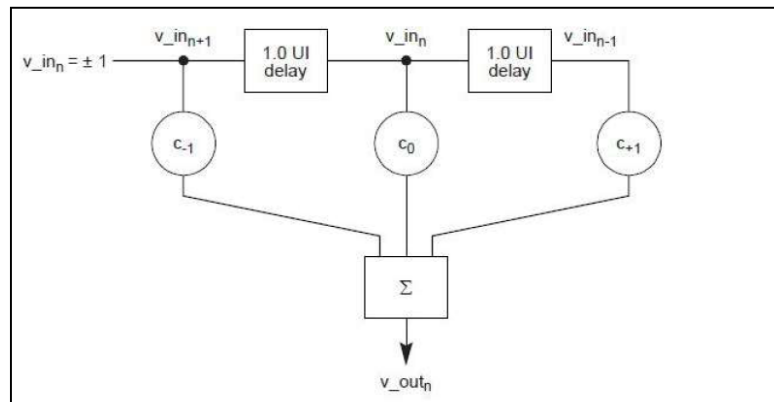


Figure 22 The PCIe 3.0 Tx Equalization FIR filter representation. (Note: The 10G-KR Filter is similar in definition).

201. Gorecki teaches storing transmit filter coefficient values in nonvolatile memories, as explained previously. *See* above §V.A.3[1f] (explaining Gorecki’s teachings for Ground 2; that analysis also applies here)); Ex-1005, 7:18-26 (storing “pre-set” tap coefficient values in various types of nonvolatile memories, including “ROM, PROM, EPROM, [and] EEPROM[.]”). Like Cornelius and Samaan, Gorecki teaches pre-equalization of electrical signals over a cable using an FIR filter with multiple tap coefficient values. Ex-1005, Abstract, 1:12-17, 6:38-41, 8:4-8, 9:3-7. For example, Gorecki teaches a communication system that includes

9 Figure 22 illustrates a PCIe 3.0 Tx Equalization FIR filter, though Samaan makes it clear that the Ethernet 10GBASE KR Equalization Standard uses “an FIR filter which is identical to the one used for PCIe 3.0, and shown previously in Figure 22.” Ex-1007, ¶¶139-142, Fig. 22.

“a transmitter having equalization circuitry to compensate for bandwidth limitations and reflections in high-speed digital communication systems.” Ex-1005, 3:12-16, Abstract, 3:35-38. This equalization circuitry performs pre-equalization because it is located on the transmitter side and conditions the signal before transmission to compensate for limitations and reflections of the channel. Ex-1005, 3:12-16, Abstract, 3:35-38.

202. Therefore, Ground 4 teaches [1f].

203. **Motivation to Combine.** The combination of Cornelius and Samaan teaches an active cable performing pre-equalization using filter coefficient values. Ex-1006, 6:30-42, 11:45-62, Claims 5, 10; Ex-1007, ¶¶5-8, ¶¶207-220, Figs. 34-35. Gorecki teaches storing these types of coefficient values in nonvolatile memory and retrieving the coefficient values using a controller. Ex-1005, 7:1-16, 9:3-15. A POSITA would have been motivated to apply Gorecki’s teachings to Cornelius and Samaan by storing coefficient values in nonvolatile memory, with a reasonable expectation of success, for numerous reasons explained below. The motivation to combine Cornelius and Samaan was explained previously. *See* above §V.B.3[1a] (Motivation to Combine subsection).

204. First, Cornelius provides express motivation to store its coefficients in nonvolatile memory, explaining that the parameters (including equalization coefficients) “may be calibrated or otherwise determined by the manufacture and

stored as presets for loading during operation.” Ex-1006, 11:45-62. For the coefficients to be stored as presets during manufacturing and then loaded during cable operation, it would necessarily and obviously have been stored in nonvolatile memory. Using nonvolatile memory would have been one of two possible solutions (volatile being the other), which a POSITA would have chosen because otherwise the parameters from manufacturing would not be saved and could not be loaded during operation as Cornelius teaches. Ex-1006, 11:45-62; *see above* §V.A.3[1f] (explaining nonvolatile memory being the preferred option to preserve coefficients). Using nonvolatile memory would have had predictable results and a reasonable expectation of success because the types of nonvolatile memory taught by Gorecki (e.g., ROM, PROM, EPROM, and EEPROM) have been used to store data in computers for many decades.

205. Moreover, a POSITA would have been motivated to use nonvolatile memory to store Cornelius and Samaan’s coefficients, so that they are preserved when the cable is disconnected—a common scenario for cables—and available for subsequent use in the manner taught by Cornelius and Samaan. Ex-1006, 11:45-62 (teaching power up and restart of cables); Ex-1007, ¶¶224-225, ¶¶139-147, Figs. 22, 31, Tables 1-2. Otherwise, if stored in volatile memory, the coefficient values would be lost whenever the cable is disconnected and the transceivers lose power, including for example when the cable is shipped from the manufacturer to

customers or when a customer plugs the cable into different computers or switches. For example, in situations where coefficient values are manually determined and entered for the specific cable deployment, storing these values in nonvolatile memory allows them to be saved for future uses. Otherwise, the coefficients would be lost when the cable is disconnected, requiring recalculation and re-entry each time the cable is reconnected.

206. Having the filter coefficient values available in nonvolatile memory would have been advantageous because the cable can simply read and use the values immediately after the cable is connected, without having to determine the values on the fly each time, which takes additional time. Moreover, even if link training was used to adapt coefficient values during operation, a POSITA would nonetheless have been motivated to start with a baseline set of coefficient values to use as a default when the cable is first connected, to provide a level of equalization from the start. *See* Ex-1007, ¶¶123-126 (describing that the calibration starts with equalizer parameters that are “standard presets”). Therefore, a POSITA would have been motivated to use nonvolatile memory to have coefficient values readily available whenever the cable is connected.

207. Additionally, a POSITA would have been motivated to further combine because Cornelius, Samaan, and Gorecki are all directed to high-speed communications, including over a cable. Ex-1006, 3:33-42, 3:54-64, 4:22-31, 4:45-

54, 6:11-24, 8:57-9:6; Ex-1007, Title, ¶1, ¶¶5-8, ¶¶12-15; Ex-1005, Abstract, 1:12-17. Both Cornelius and Gorecki teach transmitting/receiving circuitry at both ends of the cable. Ex-1006, 6:11-24, Figs.5-6; Ex-1005, 4:16-27, 8:1-6, Fig. 3. All three recognize signal loss over the cable and address it with pre-emphasis on the transmitting side. Ex-1006, 11:45-62, 6:30-42; Ex-1007, ¶¶5-8, ¶¶207-220, Figs. 34-35; Ex-1005, Abstract, 3:8-15, 6:38-41, 9:3-7, 19:46-51. Samaan and Gorecki implement an FIR filter for transmission. Ex-1007, ¶¶78-81, ¶225, Figs. 21-22, 35; Ex-1005, 6:8-41, 9:3-7. Gorecki further teaches a trivial detail of storing the FIR filter tap coefficients in nonvolatile memory and reading them with a controller. Ex-1005, 7:11-26. Therefore, the combination uses a known technique (storing data in nonvolatile memory and reading with a controller) to improve similar devices in the same way.

208. The combination would not have changed the principle of operation of any reference. Storing and loading coefficients with a controller is entirely in line with, and in fact, taught by Cornelius (Ex-1006, 11:45-62, Figs. 5-6), while Samaan leaves this trivial detail to the knowledge of a POSITA. Gorecki already applies its teaching in the context of a cable. Ex-1006, 11:45-62.

209. In addition to the reasons explained earlier in this section, a POSITA would have had a reasonable expectation of success in combining teachings from Cornelius and Samaan with Gorecki because computers have, for decades, stored

values they require in nonvolatile memory such as ROM, PROM, EPROM, and EEPROM. This was a trivial implementation detail that would have been well within the level of ordinary skill (*see* §III). Undergraduate students would have been expected to be able to write data to nonvolatile memory, including ROM, PROM, EPROM, and EEPROM.

210. This would have been a combination of prior art elements (e.g., using nonvolatile memory with Cornelius and Samaan's teachings) according to known methods (e.g., saving data in ROM, PROM, EPROM, or EEPROM) to yield predictable results (e.g., data stored in memory). Therefore, a POSITA would have found it obvious to combine Cornelius and Samaan with Gorecki, with a reasonable expectation of success.

4. Dependent Claim 2

2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.

211. Ground 4 teaches claim 2. As explained above, Ground 4 teaches a DRR device (e.g., CDR/retimer circuitry) providing pre-equalization using transmit filter coefficient values stored in the nonvolatile memories. *See* above §V.B.3[1f]. Gorecki teaches the rest of claim 2, as explained above; those reasons also apply here. *See* above §V.A.4 (Ground 2, Claim 2).

212. Cornelius provides additional teachings for this claim. For example, Cornelius teaches using microcontrollers to configure the CDR/retimer circuitry in the active cable. Ex-1006, 6:21-24, 6:43-49, Claims 1, 3, 5,8. Therefore, a POSITA would have been further motivated to include a controller for configuration and to apply Gorecki's controller teachings. *See above* §V.A.4 (Ground 2, Claim 2, explaining how Gorecki teaches a controller for configuring DRR devices).

213. Cornelius teaches that the cable experiences "power-up." Ex-1006, 11:58-62. It would have been obvious for Cornelius's microcontroller to configure the CDR/retimer circuitry in response to a power-on event; in particular, it was obvious to read and configure the equalization coefficients because Cornelius teaches parameters (including equalization coefficients) that are "stored as presets for loading during operation." Ex-1006, 11:45-55.

214. Additionally, Samaan provides additional support for this claim. For example, Samaan teaches that the "output TxEQ" is "usually under micro-controller control...in order to allow the device to participate in ... TxEQ adaption or training." Ex-1007, ¶¶224-225. The micro-controller manages "all the phases of TxEQ adaptation from beginning to the end." Ex-1007, ¶227. In the TxEQ adaptation process, Samaan teaches first setting the equalization parameters to "standard presets" values. Ex-1007, ¶¶123-126. A POSITA would have understood that the "standard presets" values of the coefficients are the values already stored

in the nonvolatile memories that are readily to be retrieved during an power-on event. Since the microcontroller manages the TxEQ adaptation process, it would have been obvious to use the microcontroller to first retrieve the “standard presets” values of the coefficients from the nonvolatile memories as baseline for the training process.

5. Dependent Claim 3

3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

215. This claim recites “the transmit coefficient values” without antecedent basis. To the extent this claim is not indefinite, a POSITA would have understood “the transmit coefficient values” to refer to “the transmit filter coefficient values.”

216. Ground 4 teaches claim 3. As explained above, Ground 4 teaches that the first and second DRR devices (e.g., CDR/retimer circuitry at respective ends of the cable) use transmit filter coefficient values to transmit signals. *See above* §V.B.3[1f] (Motivation to Combine subsection explaining combination).

217. Ground 4 further **teaches the first and second DRR devices are programmed to use the transmit coefficient values**. For example, Cornelius teaches parameters (including equalization coefficients) that are “stored as presets for loading during operation.” Ex-1006, 11:45-55. Cornelius also teaches configuring the DRR devices using microcontrollers. Ex-1006, 6:11-24, 6:43-49,

Claims 1, 3, 5,8. It would have been obvious to program the DRR devices to use the preset equalization coefficients using the microcontrollers. Likewise, Samaan teaches that the TxEQ circuit within the DRR device performs equalization (Ex-1007, ¶¶5-8, ¶¶207-220, ¶225, Figs. 34-35), and that the settings of the “output TxEQ circuit ... have to be programmable[.]” Ex-1007, ¶225. Given all of these teachings, Ground 4 teaches the DRR devices being programmed to use particular transmit pre-equalization coefficient values.

218. The DRR devices are programmed **each time power is supplied to the first and second end connector plugs**. For example, Cornelius describes that power-up occurs when the end portion of the active plug is connected to a host. Ex-1006, 8:27-40 (“...a host device connected to plug 600 may provide power for plugs 600 and 605, as well as a host connected to plug 605.”), 4:32-44, 8:10-15; *see* above §V.B.3[1a] (explaining that each active plug comprises an end portion that is a connector plug). Therefore, when power is supplied to the active plugs, it would have been obvious that both DRR devices are programmed to use their transmit equalization coefficient values so that the equalization circuits can function properly. Ex-1005, 7:18-33; Ex-1006, 6:11-20, 8:27-40. I explained previously how the filter coefficient values are configured; that analysis also applies here. *See* above §V.B.4 (Claim 2).

219. Gorecki also teaches this claim, as explained above. *See above* §V.A.5.

6. Dependent Claim 4

4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.

220. Ground 4 teaches claim 4. As explained above, the combination of Cornelius and Samaan teaches using the transmit filter coefficient values to compensate for channel losses of its active cable. *See above* §V.B.3[1f]. Those values would obviously have been determined after assembly of the active cable; otherwise, the properties of the cable could not be measured because there would not be a cable attached to the transceivers. By measuring and storing the coefficients after cable assembly, the equalization process can be tailored to the specific characteristics of each individual cable, thereby improving the effectiveness of equalization and enhancing overall signal quality performance. This customization would have naturally fit into test and quality assurance (QA) procedures, and it would have been appropriate for applications that demand maximum performance, high data throughput, or extended cable lengths. For example, this would benefit data centers with long cable lengths or high bitrates by more accurately compensating for cable-specific losses and thereby improving signal quality. Thus, it would have been obvious to determine the transmit filter

coefficients after assembly, based on actual cable measurements, and to store them in nonvolatile memories so that they can be reliably accessed during operation in accordance with Cornelius and Samaan's teachings. *See* above §V.B.3[1f] (explaining how and why Cornelius and Samaan would have been combined with Gorecki, including for storing coefficients in nonvolatile memory).

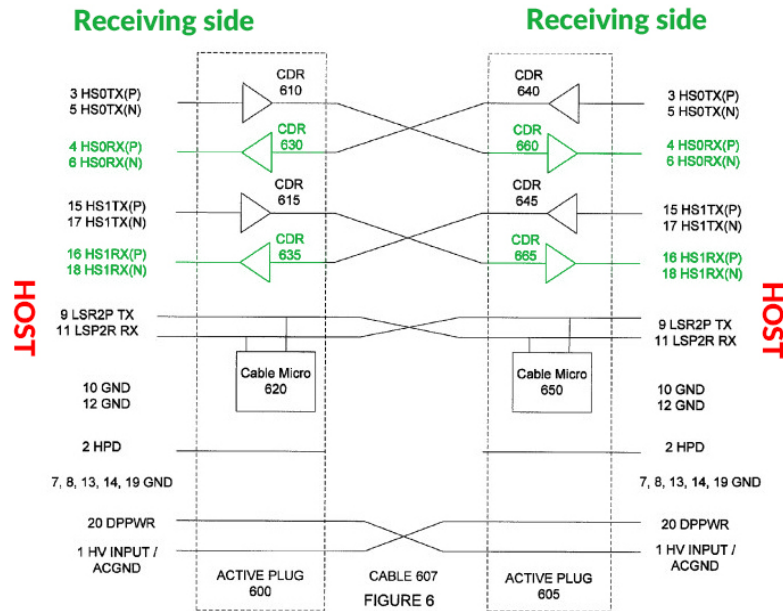
221. As I explained before, Gorecki also teaches this limitation; that analysis also applies here. *See* above §V.A.6 (Ground 1, Claim 4).

7. Dependent Claim 5

5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

222. Ground 4 teaches claim 5. Cornelius teaches **the first and second DRR devices** (e.g., CDR/retimer circuitry at respective ends of the cable) **employ receiver-based equalization of the electrical transit signals**. For example, Cornelius teaches a bidirectional cable with two symmetric DRR devices. *See* above §V.B.3[1b]. Each DRR device employs “equalizer circuits, buffers, emphasis, and de-emphasis circuits[.]” Ex-1006, 6:30-42, Fig. 6, Claims 5, 10. Since the equalizer circuits are also implemented in the CDR/retimer circuitry on the receiving side, the DRR devices employ receiver-based equalization of the electrical transit signals. This allows Cornelius to perform equalization on the

received electrical transit signals to compensate for channel losses occurred during transmission.



223. Samaan provides additional support for this limitation. For example, Samaan recognizes the issue of signal distortion in high-speed copper links, and explains that “a significant fraction of the...distortion due to channel loss could be compensated for using simple equalization circuits in...the receiver...” Ex-1007, ¶¶5-8. Samaan describes implementing Discrete Feedback Equalization (DFE) circuit and CTLE and Gain (or AGC) Stage circuits in the re-timers to perform equalization to “cancel the residual pulse response tails (and ripples) in the incoming analog signal.” Ex-1007, ¶215, ¶220, ¶¶20-21. As explained above, Samaan’s re-timer structure can be can be incorporated into Cornelius’s two active plugs, which are symmetrically positioned on each end of the active cable. *See*

above §V.B.3[1a]-[1b] (explaining how and why Cornelius and Samaan would have been combined). Therefore, the DFE and CTLE circuits in the receiving-side CDR/retimer circuitry perform receiver-based equalization. Ex-1007, ¶¶215, ¶220, ¶¶20-21.

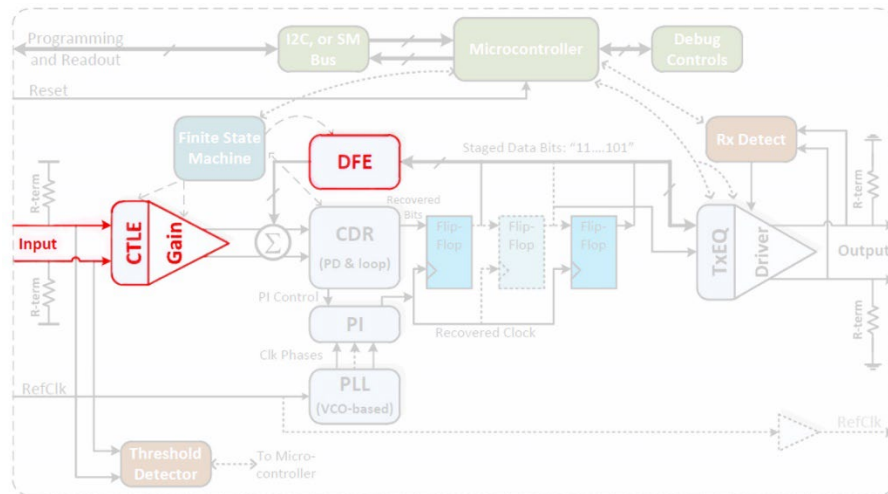
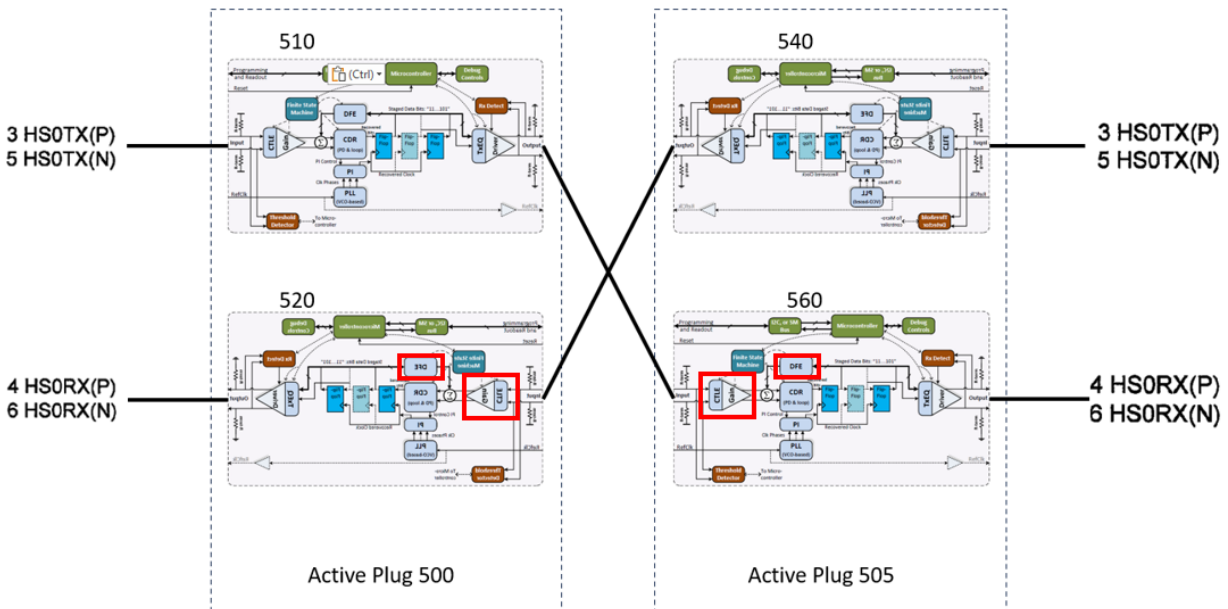


Figure 34 Conceptual micro-architecture of a "Bit Re-timer", showing input CTLE, AGC, DFE, a CDR, and a data path connected directly to an output driver with TxEQ.



224. As I explained before, Gorecki teaches **using coefficient values stored in the nonvolatile memories**; that analysis also applies here. *See* above §V.A.7 (Claim 5).

8. Dependent Claim 6

6. **The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.**

225. Ground 4 teaches claim 6. For example, Cornelius teaches providing “high-speed differential signal paths.” Ex-1006, 1:64-2:2; 9:62-65. Twin-axial conductors they were one of the most commonly used conductors for conveying high-speed differential signals—so much so that twin-axial cabling was generally associated with differential signaling. Therefore, a POSITA would have found it obvious to use twin-axial conductors for Cornelius’s high-speed differential signal paths. Ex-1006, 1:64-2:2.

9. Dependent Claim 7

7. **The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.**

226. Ground 4 teaches claim 7. As I explained before, Gorecki and Samaan teach this claim and that analysis also applies here. *See* above §V.A.9 (Ground 1, Claim 7).

10. Independent Claim 8

[8pre] A cable manufacturing method that comprises:

227. I understand that a preamble generally does not state a claim limitation. Nonetheless, it is my opinion that Ground 4 teaches it.

228. Ground 4 teaches the cable of claim 1. *See* above §V.B.3 (Claim 1). Ground 4 further teaches a method of manufacturing a cable by connecting the components of Cornelius's active cable together, including the steps explained for limitations below. Ex-1006, Title, 5:33-39, 6:6-20, 8:20-40, Figs. 5-6, Claims 1-10.

[8a] connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;

229. Ground 4 teaches [8a]. Most of limitation [8a] mirrors [1a]; Ground 4 teaches the overlapping limitations as explained above. *See* above §V.B.3[1a].

230. Cornelius further teaches **connecting a first connector plug** to the first DRR device (e.g., CDR/retimer circuitry). For example, Cornelius teaches two active plugs located at both ends of the active cable. Ex-1006, 6:11-20, 8:20-40, Figs. 5-6. Each active plug comprises an end portion with pins the CDR/retimer circuitry uses to exchange inbound/outbound data streams with the host. *See* above §V.B.3[1a]; Ex-1006, Figs. 3, 5-6. Each CDR/retimer circuitry is connected to specific connector pins. Ex-1006, Figs. 3, 5-6.

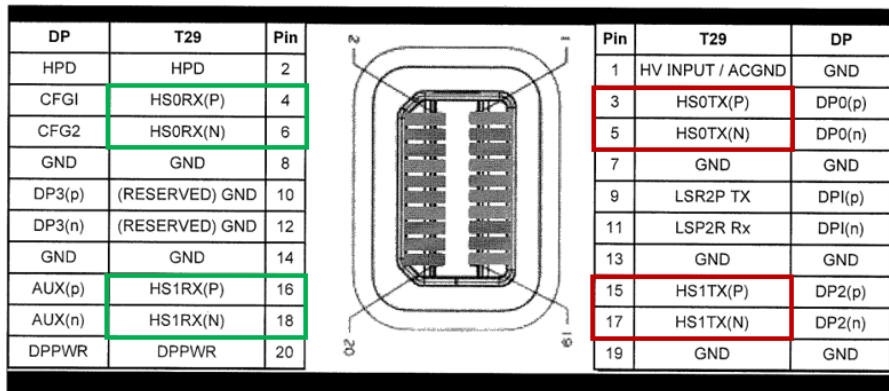
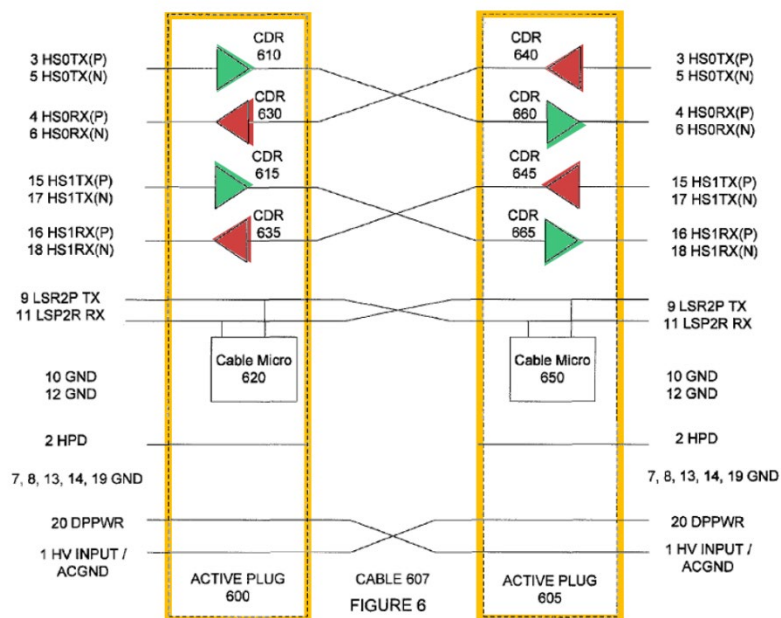


FIGURE 3



231. Therefore, because Cornelius teaches a first connector plug connected to a first DRR device, Cornelius teaches or suggests the step of connecting these components together. At a minimum, it would have been obvious because, in order for the plug and connector to be connected in an assembled cable (as Cornelius

teaches), they would have obviously been connected during manufacturing, when the cable components were assembled into Cornelius's active cable. Figs. 5-6.

[8b] connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;

232. Ground 4 teaches [8b]. Limitation [8b] mirrors [8a], differing only by changing "first" to "second." Cornelius teaches a cable with two symmetric DRR devices (e.g., CDR/retimer circuitry). *See* above §V.B.3[1a]-[1b]. Either of the two CDR/retimer circuitry would be the first DRR device recited in [8a]; the other CDR/retimer circuitry would be the second DRR device recited in [8b], for the same reasons explained previously. *See* above §V.B.10[8a]. That analysis also applies to [8b] and is incorporated here. The interface port and plug for the second DRR device, would be the second host interface port and second connector plug.

233. Therefore, limitation [8b] is satisfied for the same reasons explained for [8a]. *See* above §V.B.10[8a].

[8c] connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,

234. Ground 4 teaches [8c]. Most of limitation [8c] mirrors [1c]; Ground 4 teaches the overlapping limitations as explained above. *See* above §V.B.3[1c].

235. Cornelius also teaches **connecting** electrical conductors to the first and second DRR devices (e.g., CDR/retimer circuitry at respective ends of the

cable). As explained above, Cornelius teaches electrical conductors connecting the first and second DRR devices. *See* above §V.B.3[1c]. Therefore, Cornelius teaches or suggests the step of connecting these components together. Ex-1006, Figs. 5-6. At a minimum, it would have been obvious because, in order for these components to be connected in an assembled cable (as Cornelius teaches), they would have obviously been connected during manufacturing, when the cable components were assembled into Cornelius's active cable. Ex-1006, Figs. 5-6.

- | | |
|-------------|---|
| [8d] | the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and |
| [8e] | the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port, |
| [8f] | the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories. |

236. Ground 4 teaches [8d]-[8f]. The limitations in [8d]-[8f] also appear in limitations [1d]-[1f], respectively, and are satisfied for the same reasons explained previously. *See* above §V.B.3[1d]-[1f].

- 1 [1d] the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and
- 2 [1e] the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,
- 3 [1f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

- 1 [8d] the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and
- 2 [8e] the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,
- 3 [8f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

11. Dependent Claim 9

- | | |
|----|---|
| 9. | The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring |
|----|---|

237. Ground 4 teaches claim 9. Beyond the preamble, claim 9 mostly overlaps with claim 2; Ground 4 teaches the overlapping limitations as explained above. *See* above §V.B.4 (Claim 2).

1 2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.

1 9. The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.

238. Ground 4 also teaches **providing** a first controller **device** because Ground 4 teaches a first controller, which is a device, as part of the active cable. *See* above §V.B.4 (Claim 2). It was obvious to provide a controller to perform the functions Ground 2 teaches..

239. As I explained before, Gorecki teaches **internal** nonvolatile memory; that analysis also applies here. *See* above §V.A.11 (Ground 2, Claim 9).

12. Dependent Claim 10

- | | |
|-----|--|
| 10. | The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs. |
|-----|--|

240. Ground 4 teaches claim 10. The limitation of claim 10 is identical to claim 3, other than a change to verb tense and passive voice (“programmed” to

“programming”). Therefore, claim 10 is satisfied for the same reasons explained previously. *See* above §V.B.5 (Claim 3).

13. Dependent Claim 11

11. The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.

241. Ground 4 teaches claim 11. As explained above, Ground 4 teaches that the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable. *See* above §V.B.6 (Claim 4). Because the assembly of Cornelius’s active cable includes connecting the electrical conductors (*see* above §V.B.10[8c], §V.B.3[1c]), Ground 4 teaches determining the coefficient values and storing them in nonvolatile memories after connecting the electrical conductors.

242. Cornelius, Samaan and Gorecki use pre-equalization to compensate for the loss characteristics of the channel. *See* above §V.B.3[1f]. As Samaan explains, the “equalization circuits in the transmitter” (e.g., FIR filters), are used to compensate signal “distortion due to channel loss.” Ex-1007, ¶8, ¶225. Likewise, Gorecki teaches using transmitter-side equalization circuitry to “compensate for bandwidth limitations and reflections in high-speed digital communication systems.” Ex-1005, 3:8-27. To achieve the desired compensation result, Gorecki

explains that the coefficients used by FIR filters are “pre-programmed or pre-set” so that the introduced “compensation...is ideally the inverse of the effects caused by the communication channel.” Ex-1005, 7:18-33, 9:3-15. Therefore, Ground 4 teaches the obvious step of determining transmit filter coefficient values by characterizing channel characteristics of the electrical conductors, so that Samaan and Gorecki’s pre-equalization filter can compensate for those channel characteristics as taught. Ex-1007, ¶225, ¶¶78-81, Figs. 21-22, 35; Ex-1005, 3:8-27, 7:18-33, 9:3-15.

14. Dependent Claims 12-14

- 12. The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.**
- 13. The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.**
- 14. The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.**

243. Ground 4 teaches claims 12-14. The limitations of claims 12-14 are identical to claims 5-7 and satisfied for the same reasons. *See* above §V.B.7-9 (Claims 5-7).

1 5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.
 2 6. The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.
 3 7. The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

1 12. The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.
 2 13. The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.
 3 14. The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

15. Independent Claim 15

[15pre] A communications method that comprises:

244. I understand that a preamble generally does not state a claim limitation. Nonetheless, it is my opinion that Ground 4 teaches it.

245. Ground 4 teaches **a communications method**. Cornelius teaches “[c]ircuits, methods, and apparatus” (Ex-1006, Abstract, 1:50-51, 1:55-58, 4:66-5:1), including the various methodology details and steps explained below for limitations [15a]-[15c]. Cornelius describes channel configurations for data communications through active cables (*see, e.g.*, Ex-1006, 3:28-42, 60-64, 4:39-44, 5:33-6:5, 6:6-67), methods for facilitating communications between devices connected by the cables (*e.g.*, Ex-1006, 3:28-42, 4:10-21, 4:66-6:5), and routines for calibrating those cables (*e.g.*, Ex-1006, 11:45-12:20). Similarly, Samaan provides detailed explanations of how signals are transmitted through channels containing retimers, including a “method of propagating” messages related to the training of equalization components on retimers serially connected in a “cascaded configuration” (*e.g.*, Ex-1007, ¶¶257-260, Figs. 39-40, Table 3).

246. The communications method taught by Ground 4 further includes the limitations of claim 15 discussed below.

[15a] inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and
--

247. Ground 4 teaches [15a]. Cornelius teaches **inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first DRR device** (e.g., CDR/retimer circuitry). As explained previously, each active plug comprises an end portion that is a connector plug. *See* above §V.B.3[1a]. The active plug's end portion is "inserted" in a first host device. Ex-1006, 7:7-17, 8:27-40 ("...a host device connected to plug 600..."). Additionally, it would have been obvious to insert the plug into the host interface port given the nature of the cable: the plug is inserted into the port. As explained previously, the first CDR/retimer circuitry exchanges inbound/outbound data streams via a first end connector plug and therefore is connected to it. *See* above §V.B.3[1a].

248. The rest of [15a] combines elements recited in [1a], [1c], and [1d]; Ground 4 teaches these limitations for the same reasons explained previously. *See* above §V.B.3[1a], [1c]-[1d].

[15b] inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,

249. Ground 4 teaches [15b]. Limitation [15b] mirrors [15a] and differs only by changing “first” to “second.” Cornelius teaches a cable with two symmetric DRR devices (e.g., CDR/retimer circuitry). *See* above §V.B.3[1a]-[1b]. Either of the two CDR/retimer circuitry would be the first DRR device recited in [15a]; the other CDR/retimer circuitry would be the second DRR device recited in [15b], for the same reasons explained previously. *See* above §V.B.15[15a]. That analysis also applies to [15b] and is incorporated here. The interface port and plug for the second DRR device, would be the second host interface port and second end connector plug.

250. Therefore, limitation [15b] is satisfied for the same reasons explained for [15a]. *See* above §V.B.15[15a].

[15c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

251. Ground 4 teaches [15c]. Limitation [15c] is identical to [1f] and is satisfied for the same reasons. *See* above §V.B.3[1f].

¹ [1f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

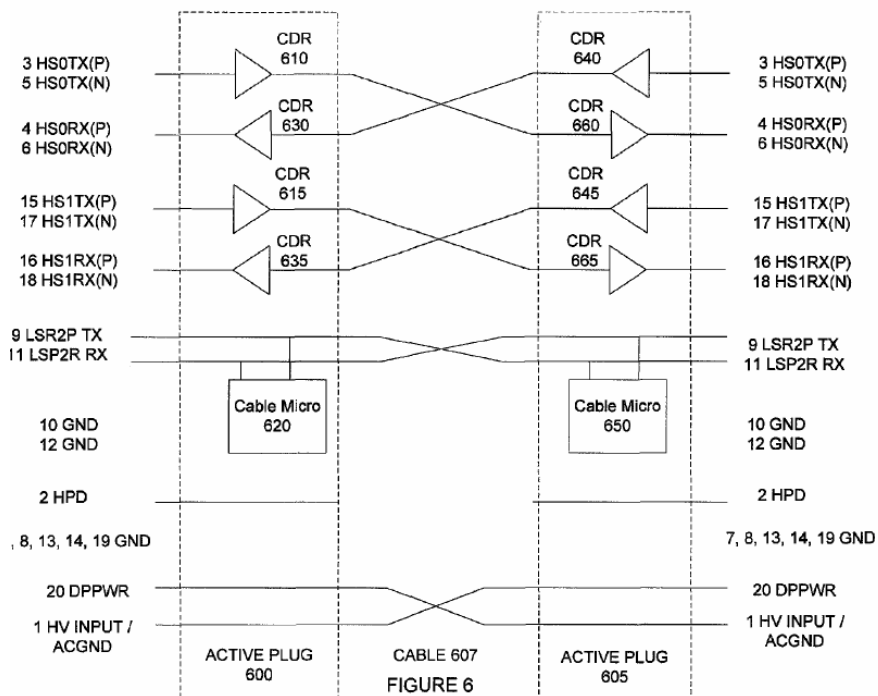
¹ [15c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

16. Dependent Claim 16

16. The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.

252. Ground 4 teaches claim 16. Cornelius teaches **supplying power to the first and second end connector plugs**. For example, Cornelius teaches that “a host device connected to plug 600 may provide power for plugs 600 and 605.” Ex-1006, 8:27-40, 8:10-15. Cornelius also describes ways to save power—for example, when a channel is not used—suggesting that power is being provided. Ex-1006, 7:26-41.

253. Ground 4 teaches **the first and second end connector plugs being connected to first and second controller devices, respectively**. Cornelius teaches a microcontroller in each active plug. Ex-1006, 6:21-24, 6:43-49, Claims 1, 3, 5 and 8, Figs. 5-6. As explained previously, each active plug comprises an end portion that is a connector plug. *See* above §V.B.3[1a]-[1b]. That end connector plug is connected to the microcontroller on pins 9 and 11. Ex-1006, Figs. 3, 5-6.



254. Ground 4 teaches **each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.** Ground 4 teaches that a first controller operates to configure the first DRR device in response to a power-on event, and the configuration includes retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring, for the reasons explained above. *See* above §V.B.4 (Claim 2). Because Cornelius teaches a cable with two symmetric DRR devices (one at each end of the cable), Ground 4 likewise teaches that the second controller devices operates in the same manner as the first controller device. *See* above §V.B.3[1b].

17. Dependent Claims 17-20

- | | |
|-----|--|
| 17. | The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs. |
| 18. | The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable. |
| 19. | The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories. |
| 20. | The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports. |

255. Ground 4 teaches claims 17-20. Claims 17-20 recite identical limitations to claims 3-5 and 7, respectively, and are satisfied for the same reasons explained previously. *See* above §V.B.5-7, 9 (Claims 3-5, and 7).

1 3. The cable of claim 1, wherein the first and second
DRR devices are programmed to use the transmit coefficient
values each time power is supplied to the first and second
end connector plugs.
2 4. The cable of claim 3, wherein the transmit filter
coefficient values are determined and stored in the
nonvolatile memories after assembly of the cable.
3 5. The cable of claim 4, wherein the first and second
DRR devices employ receiver-based equalization of the
electrical transit signals using coefficient values stored
in the nonvolatile memories.
4 7. The cable of claim 1, wherein the first and second
DRR devices do not perform pre-equalization of the multi-
lane data streams provided to the first and second host
interface ports.

1 17. The method of claim 15, wherein the first and
second DRR devices are programmed to use the transmit
coefficient values each time power is supplied to the first
and second end connector plugs.
2 18. The method of claim 17, wherein the transmit filter
coefficient values are determined and stored in the
nonvolatile memories after assembly of the cable.
3 19. The method of claim 18, wherein the first and
second DRR devices employ receiver-based equalization of
the electrical transit signals using coefficient values
stored in the nonvolatile memories.
4 20. The method of claim 15, wherein the first and
second DRR devices do not perform pre-equalization of the
multi-lane data streams provided to the first and second
host interface ports.
5

VI. BACKGROUND AND QUALIFICATIONS

256. I am a tenured full professor of Electrical Engineering at the University of Southern California, where I have been a faculty member since 2011.

As a professor, I research and teach electronic circuit and system design. My research focuses on analog mixed-signal and RF circuit architectures for data converters (both ADC and DAC), transceivers (both wireline and wireless), clock generation (such as PLL and DLL), digital VLSI, SoC, mostly-digital circuits, artificial intelligence (AI) and machine learning (ML) accelerators, analog CAD, and advanced signal processing techniques (e.g. adaptive filter, calibration, equalization, etc.) for analog circuit and systems. My research has been applied to wireline, wireless communications, computing, IoT systems, autonomous vehicles, etc. Among other subjects, I regularly teach courses such as Advanced Data Converters, Advanced Mixed Signal Integrated Circuit Design, Analog and Non-Linear Integrated Circuit Design, and Mixed Signal Integrated Circuit Design.

257. I received my B.S. degree from National Taiwan University, where I graduated as the top student in the upper division. I earned my Ph.D. and M.Sc. in Electrical Engineering and Computer Science from the University of California, Berkeley in 2006 and 2002 respectively. As a graduate student researcher at UC Berkely between 2001 and 2006, I proposed and demonstrated the asynchronous SAR ADC architecture. This architecture has been adopted in the industry for low-power high-speed analog-to-digital conversion products. The subject of my Ph.D. thesis was “High-Speed, Low-Power A/D Converter for a Low-Cost UWB Sub-sampling Radio.”

258. From 2006 to 2010, I was Analog Senior Technical Staff in the Analog IC Group of Atheros Communications (now Qualcomm Atheros), where I designed mixed-signal and RF circuits for various communication devices. In 2011, I joined the faculty of the University of Southern California, initially as an Assistant Professor of Electrical Engineering. I was promoted to the rank of Associate Professor in 2017 and became a full professor in 2021. From 2014 to 2021, I held the position of Colleen and Roberto Padovani Early Career Chair in Electrical and Computer Engineering.

259. My work has been recognized by both academic and commercial entities. I have published over 90 conference, journal, magazine articles, including multiple publications in the IEEE International Solid-State Circuits Conference (ISSCC), IEEE Symposium on VLSI Circuits (VLSIC), IEEE Custom Integrated Circuits Conference (CICC), IEEE European Conference on Solid-State Circuit (ESSCIRC), IEEE Radio Frequency Integrated Circuits Symposium (RFIC), IEEE Journal of Solid-State Circuits (JSSC), and Transactions on Circuit and System I (TCAS-I). For example, my recent conference papers have addressed topics such as “High-Speed Digital-to-Analog Converter Design Towards High Dynamic Range,” “A 24GHz Direct Digital Transmitter Using Multiphase Subharmonic Switching PA Achieving 3.2Gbps Data Rate and -30.8dB EVM in 65nm CMOS,” and “A Millimeter-Wave Mixer-First Receiver with Non-Uniform Time-

Approximation Filter Achieving >45-dB Blocker Rejection.” In 2020, the paper “A 12.8-Gbaud ADC-based Wireline Receiver with Embedded IIR Equalizer” was published as an invited paper in the IEEE Journal of Solid-State Circuits. My research has been funded by the National Science Foundation (NSF), ONR, IARPA, SRC, DARPA and various industry companies. I have also served as a technical consultant for companies including Qualcomm, Tetramem, BAE Systems and Samsung.

260. I have received recognition for my work and research. In 2024, I was honored with the grade of IEEE Fellow to recognize my technical contributions in solid-state circuit society. This grade is reserved for 0.1% of IEEE members. In 2023, I was the co-recipient of the ISSCC Jack Kilby Award for significant advances in analog mixed-signal circuits. In 2022, I was a co-recipient for the RFIC 2022 Best Student Paper Award for my work with students in my laboratory on a circuit prototype. From 2021 to 2023, I was the IEEE Solid-State Circuit Society (SSCS) Distinguished Lecturer. I have been invited to offer seminars, workshops, keynote talks, and panel discussions in major IEEE conferences, IEEE SSCS chapters, and universities on a range of topics covering fundamental to advanced integrated circuit design and how to improve the performance and/or reduce cost of a circuit or system. In 2019, I was also the recipient of Qualcomm Faculty Award, and in 2014 both the NSF Faculty Early Career Development

(CAREER) Award and DARPA Young Faculty Award (YFA). As a student, I was the recipient of a UC Regents' Fellowship at Berkeley in 2000 and the Analog Devices Outstanding Student Award for IC design in 2006.

261. I have extensive experience and familiarity with integrated circuit (IC) design for wireline communication as well as relevant signal processing techniques for such communication systems. As a principal investigator, I have conducted various research projects innovating and prototyping the most critical circuit blocks of wireline transceivers. I have also served in various review panels (e.g. NSF panels, IEEE conferences and journals), reviewing research papers related to wireline or serial link or SerDes circuit, system and signal processing techniques. Lastly, I have been teaching various circuit courses at USC. I teach my students a wide range of circuit and signal processing techniques related to this wireline area, so that they learn how those circuit components can be designed and implemented.

A. Compensation

262. For my efforts in connection with the preparation of this declaration I have been compensated at my standard rate for this type of consulting activity. My compensation is in no way contingent on the results of these or any other proceedings relating to the above-captioned patent.

B. Materials and Other Information Considered

263. I have considered information from various sources in forming my opinions. I have reviewed and considered each of the exhibits listed in the attached Appendix 2 (Materials Considered in the Preparation of This Declaration) in forming my opinions.

VII. UNDERSTANDING OF THE LAW

264. I am not an attorney. In forming my opinions in this Declaration, I applied the relevant legal principles provided to me by counsel, which are summarized in Appendix 4.

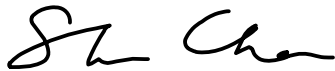
VIII. RESERVATION OF RIGHTS

265. My opinions are based upon the information that I have considered to date. I am unaware of any evidence of secondary considerations with respect to the '233 Patent that would render any of the challenged claims non-obvious. I reserve the right, however, to supplement my opinions in the future to respond to any arguments raised by the owner of the '233 Patent and to take into account new information that becomes available to me.

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

EXECUTED ON 8/1/25.

BY:



MICHAEL SHUO-WEI CHEN

APPENDIX 1: CURRICULUM VITAE OF Michael Shuo-Wei Chen

Mike Shuo-Wei Chen

3737 Watt Way, PHE 622, Los Angeles, CA 90089
Email: shuowei@gmail.com (Alt: swchen@usc.edu)
Phone: 510-517-0052

Curriculum Vitae

EDUCATION

University of California, Berkeley 2002 – 2006

- PhD in Electrical Engineering and Computer Science
- Dissertation: “High-Speed, Low-Power A/D Converter for a Low-Cost UWB Sub-sampling Radio”
- Advisor: Robert W. Brodersen

University of California, Berkeley 2000 – 2002

- Master of Science in Electrical Engineering and Computer Science
- Thesis: “Ultra Wideband Baseband Design and Implementation”

National Taiwan University 1994 – 1998

- Bachelor of Science in Electrical Engineering
- Top 1 student for upper division

ACADEMIC EXPERIENCE

- Full Professor, Department of Electrical Engineering, University of Southern California, 2021 – Present.
- Associate Professor, Department of Electrical Engineering, University of Southern California, 2017 – 2021.
- Colleen and Roberto Padovani Early Career Chair, USC, 2014 – 2021
- Assistant Professor, Department of Electrical Engineering, University of Southern California, 2011 – 2017.
- Graduate Student Researcher, Berkeley Wireless Research Center, Berkeley, CA, 2001 – 2006.

WORK EXPERIENCE

- Analog Senior Technical Staff, Atheros Communications, Santa Clara, CA, 2006–2010.
-Designed RF, analog mixed-signal circuits for various wireless products

CONSULTING EXPERIENCE

- Legal Consulting
(2019-2022): Xilinx-ADI litigation

Legal consultant, working with counsels to prepare/review legal documents, non-infringement arguments, deposition, source codes, PTAB, etc.

(2023-Present): Aptiv-Microchip

Legal expert, working with counsel on IPR expert declaration, source code review for litigation, etc.

(2023-2024): ARM-Qualcomm litigation

Legal expert, working on source code review, expert report, and deposition, testifying expert during trial

(2025-Present): Apple-Vampire Labs

Legal expert, IPR

(2025-Present): BOE – Samsung

Legal expert, IPR

(2025-Present): Marvell – Credo

This matter

(2025-Present): Renesas-Monterey Research

Legal expert, patent re-examination

- Technical Consulting:
Qualcomm, Samsung, BAE system, Tetramem → Provide technical advices on various electronic projects for the client.

HONORS and AWARDS

- IEEE Fellow 2024
- ISSCC 2022 Jack Kilby Award (co-recipient)
- RFIC 2022 Best Student Paper Award – First Place (co-recipient)
- IEEE Solid-State Circuit Society (SSCS) Distinguished Lecturer 2021-2023.
- Qualcomm Faculty Award, 2019.
- DARPA Young Faculty Award (YFA), 2014.
- NSF Faculty Early Career Development (CAREER) Award, 2014.
- Analog Devices Outstanding Student Award, 2006
- UC Regents Fellowship, UC Berkeley, 2000
- Lin's Foundation Award for Top 1 engineering college student over the academic year, 1996-1997
- Presidential Awards, National Taiwan University, 1996-1998
- Member of National Mathematics Team of Taiwan, awarded with Honourable Mention in Asian Pacific Mathematics Olympiad, 1994.

AREA OF INTEREST

I worked on various Analog Mixed-Signal, VLSI, SoC and RF circuit architectures/techniques, covering a wide range of topics/areas in academia and industry, including

- Data Converters (e.g. ADC and DAC)
- RF/mm-Wave Wireless Communications (e.g. WiFi, 5G/6G, Bluetooth, GPS, etc.)

- I/O, Wireline Communications (e.g. SerDes, CDR, Clock generation)
- Computing (e.g. AI/ML accelerators, neuromorphic processor)
- Design Methodology (AI-ML assisted CAD).
- Digital VLSI, SOC, RTL
- Analog Mixed-Signal Circuit
- Power management circuit

PUBLICATIONS

Conferences

1. S. Mahapatra, M. Ayes, C. Yang, M. Palaria, S. Su, A. Zhang, **M. S.-W. Chen**, "A 24GHz Direct Digital Transmitter Using Multiphase Subharmonic Switching PA Achieving 3.2Gbps Data Rate and -30.8dB EVM in 65nm CMOS", IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2025.
2. C. Yang, S. Su, M. Ayes, S. Mahapatra, M. Hamada, V. Chenna, H. Hashemi, **M. S.-W. Chen**, "A Blocker Tolerant Receiver with VCO-based Non-Uniform Multi-Level Time-Approximation Filter With -36dB EVM in 28nm CMOS", IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2025. (to be presented)
3. J. Liu, A. Shabra, S. Ho, G. Manganaro, **M. S.-W. Chen**, "A 16GS/s 10b Time-domain ADC using Pipelined-SAR TDC with Delay Variability Compensation and Background Calibration Achieving 153.8dB FoM in 4nm CMOS" in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technol. Circuits)*, June 2024.
4. Q. Zhang*, S. Su*, B. R. Biswas, S. Gupta, **M. S.-W. Chen**, "Synthesizable 10-bit Stochastic TDC Using Common-Mode Time Dithering and Passive Approximate Adder With 0.012mm² Active Area in 12nm FinFET," in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technol. Circuits)*, June 2024. (* equal contribution)
5. Q. Zhang*, S. Su*, Z. Liu*, H.-C. Cheng, Z. Qiu, M. Palaria, J. Ye, D. Meng, B. Chen, S. Hossain, W. Wu, **M. S.-W. Chen**, "A Stochastic Analog SAT Solver in 65nm CMOS Achieving 6.6μs Average Solution Time with 100% Solvability for Hard 3-SAT Problems," in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technol. Circuits)*, June 2024. (* equal contribution)
6. M. Ayes, S. Mahapatra, C. Yang and **M. S.-W. Chen**, "A 0.072-mm² 18-21GHz Non-Uniform Sub-Sampling Receiver with a Non-Uniform Discrete-Time FIR Filter Achieving 42dB Blocker Rejection in 28nm CMOS", *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2024.
7. M. Palaria, S. Su, H.-C. Cheng, R. Rasul, Q. Zhang, S. Mahapatra, C.-F. Law, S. Hossain, R. Bena, W. Wu, Q. Nguyen, M. S.-W. Chen, "Analog Kalman Filter with Integration and Digitization via a Shared Thyristor-Based VCO for Sensor Fusion in 65 nm CMOS", in *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2023.
8. H.-C. Cheng, S. Su, M. Palaria, Q. Zhang, C. Yang, S. Hossain, R. Bena, B. Chen, Z. Liu, J. Liu, R. Rasul, Q. Nguyen, W. Wu, **M. S.-W. Chen**, "A

- Memristor-Based Analog Accelerator for Solving Quadratic Programming problems,” in IEEE Custom Integrated Circuits Conference (CICC), April 2023.
9. S. Su*, Q. Zhang*, and **M. S.-W. Chen**, “A 2GS/s 8.5-Bit Time-Based ADC Using a Segmented Stochastic Flash TDC,” in 2023 IEEE Custom Integrated Circuits Conference (CICC), Apr. 2023 (* equal contribution)
 10. Q. Zhang, H.-C. Cheng, S. Su, and **M. S.-W. Chen**, “A Fractional-N Digital MDLL with Injection Error Scrambling and Background Third-Order DTC Delay Equalizer Achieving -67dBc Fractional Spur,” in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2023.
 11. Q. Zhang*, S. Su*, and **M. S.-W. Chen**, “A Cost-Efficient Fully Synthesizable Stochastic Time-to-Digital Converter Design Based on Integral Nonlinearity Scrambling,” in 2022 59th ACM/EDAC/IEEE Design Automation Conference (DAC), July 2022. (*contributed equally to this work)
 12. C. Yang, S. Su and **Mike Chen**, “A Millimeter-Wave Mixer-First Receiver with Non-Uniform Time-Approximation Filter Achieving $>45\text{-dB}$ Blocker Rejection,” in IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2022. (Best Student Paper Award – First Place)
 13. S. Su, and **M. S.-W. Chen**, “High-Speed Digital-to-Analog Converter Design Towards High Dynamic Range,” (invited paper) *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2022.
 14. J. Liu, M. Hassanpourghadi, and **M. S.-W. Chen**, “A 10GS/s 8b 25fJ/c-s 2850um² Two-Step Time-domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology“, *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2022.
 15. S. Su, Q. Zhang, M. Hassanpourghadi, J. Liu, R.A. Rasul, and **M. S.-W. Chen**, “Analog/Mixed-Signal Circuit Synthesis Enabled by the Advancements of Circuit Architectures and Machine Learning Algorithms,” (invited paper) *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022.
 16. S. Su, Q. Zhang, J. Liu, M. Hassanpourghadi, R.A. Rasul, and **M. S.-W. Chen**, “TAFA: Design Automation of Analog Mixed-Signal FIR Filters Using Time Approximation Architecture,” *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022.
 17. J. Liu, S. Su, M. Madhusudan, M. Hassanpourghadi, S. Saunders, Q. Zhang, R. Rasul, Y. Li, J. Hu, A. Kumar, S. S. Sapatnekar, R. Harjani, A. Levi, S. Gupta and **M. S.-W. Chen**, “From Specification to Silicon: Towards Analog/Mixed-Signal Design Automation using Surrogate NN Models with Transfer Learning“, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2021.
 18. M. Hassanpourghadi, S. Su, R.A. Rasul, J. Liu, Q. Zhang, and **M. S.-W. Chen**, “Circuit Connectivity Inspired Neural Network for Analog Mixed-Signal Functional Modeling,” *58th ACM/EDAC/IEEE Design Automation Conference (DAC)*, Dec. 2021.(to appear)
 19. R.A. Rasul, and **M. S.-W. Chen**, “A 128×128 SRAM Macro with Embedded Matrix-Vector Multiplication Exploiting Passive Gain via MOS Capacitor for Machine Learning Application,” *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2021.
 20. A. Zhang, M. Ayesh, S. Mahapatra, and **M. S.-W. Chen**, “A 24-28 GHz Concurrent Harmonic and Subharmonic Tuning Class E/F_{2,2/3} Subharmonic

- Switching Power Amplifier Achieving Peak/PBO Efficiency Enhancement,” *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2021.
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 22. A. Zhang, C. Yang, M. Ayes, and **M. S.-W. Chen**, “A 5-6 GHz Current-Mode Subharmonic Switching Digital Power Amplifier for Enhancing Power Back-off Efficiency,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2021.
 23. Q. Zhang, S. Su, J. Liu and **M. S.-W. Chen**, “CEPA: CNN-based Early Performance Assertion Scheme for Analog and Mixed-Signal Circuit Simulation,” in *2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2020.
 24. J. Liu, M. Hassanpourghadi, Q. Zhang, S. Su and **M.S.-W. Chen**, “Transfer Learning with Bayesian Optimization-Aided Sampling for Efficient AMS Circuit Modeling,” in *2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2020.
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 27. T.-F. Wu and **M. S.-W. Chen**, “A 40MHz-BW 76.2dB/78.0dB SNDR/DR noise-shaping nonuniform sampling ADC with single phase-domain level crossing and embedded nonuniform digital signal processor in 28nm CMOS,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2020.
 28. S. Su and **M. S-W Chen**, “A 1–5GHz Direct-Digital RF Modulator with an Embedded Time-Approximation Filter Achieving -43dB EVM at 1024 QAM,” *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, June 2019.
 29. J.W. Nam, **M.S-W Chen**, “A 12.8-Gbaud ADC-based NRZ/PAM4 Receiver with Embedded Tunable IIR Equalization Filter Achieving 2.43-pJ/b in 65nm CMOS,” *IEEE Custom Integrated Circuits Conference (CICC)*, April 2019.
 30. M. Hassanpourghadi, **M.S-W Chen**, “A 2-way 7.3-bit 10 GS/s Time-based Folding ADC with Passive Pulse-Shrinking Cells,” *IEEE Custom Integrated Circuits Conference (CICC)*, April 2019.
 31. A. Zhang and **M. S-W Chen**, “A Watt-Level Phase-Interleaved Multi-Subharmonic Switching Digital Power Amplifier Achieving 31.4% Average Drain Efficiency,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2019.
 32. A. Zhang, **M. S-W Chen**, “A Sub-Harmonic Switching Digital Power Amplifier with Hybrid Class-G Operation for Enhancing Power Back-off Efficiency,” *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, 2018.

33. T.F. Wu, **M. S-W Chen**, "A 200MHz-BW 0.13mm² 62dB-DR VCO-Based Non-Uniform Sampling ADC with Phase-Domain Level Crossing in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, 2018.
34. S. Su and **M. S-W Chen**, "A 16-bit 12GS/s Single/Dual-Rate DAC with Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 within DC to 6GHz Tunable Passbands," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.
35. C.R. Ho, **M. S-W Chen**, "A digital frequency synthesizer with dither-assisted pulling mitigation for simultaneous DCO and reference path coupling," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.
36. C.R. Ho, **M. S-W Chen**, "A fractional-N digital PLL with background dither noise cancellation loop achieving <-62.5dBc worst-case near-carrier fractional spur in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.
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38. C.R. Ho, **M. S-W Chen**, "Interference-Induced DCO Spur Mitigation for Digital Phase Locked Loop in 65-nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2016.
39. J.W. Nam, M. Hassanpourghadi, A. Zhang, **M.S-W Chen**, "A 12-bit 1.6 GS/s Interleaved SAR ADC with Dual Reference Shifting and Interpolation Achieving 17.8 fJ/conv-step in 65nm CMOS," *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, June 2016.
40. C.R. Ho, **M. S-W Chen**, "A Digital PLL with Feedforward Multi-Tone Spur Cancellation Loop Achieving <-73dBc Fractional Spur and <-110dBc Reference Spur in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2016.
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42. T.F. Wu, C.R. Ho, **M. S.-W. Chen**, "A Flash-Based Non-Uniform Sampling ADC Enabling Digital Anti-Aliasing Filter in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep 2015.
43. S. Su, T. Tsai, P. Sharma, **M. S.-W. Chen**, "A 12-bit Hybrid DAC with 8GS/s Unrolled Pipeline Delta-Sigma Modulator achieving >75dB SFDR over 500MHz in 65nm CMOS," *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, June 2014.
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45. J.W. Nam, D. Chiong, and **M. S.W. Chen**, "A 95-MS/s 11-bit 1.36-mW Asynchronous SAR ADC with Embedded Passive Gain in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2013

46. P.K. Sharma, and **M. S.W. Chen**, "A 6b 800MS/s 3.62mW Nyquist AC-coupled VCO Based ADC in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2013
47. **M. S.W. Chen**, "Trend of High-Speed SAR ADC towards RF Sampling," *10th International Conference on Sampling Theory & Applications (SampTA)* (Invited), July. 2013.
48. D. Hand, and **M. S.W. Chen**, "A Non-Uniform Sampling ADC Architecture with Embedded Alias-Free Asynchronous Filter," *Global Telecommunications Conference (GLOBECOM)*, Dec. 2012.
49. **M. S.W. Chen**, "Overhead Minimization Techniques for Digital Phase-Locked Loop Frequency Synthesizer," *IEEE MWSCAS (Invited Session)*, Aug. 2012.
50. **M.S.W. Chen**, **D. Su**, S. Mehta, "A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2010.
51. Nathawad, L.; Zargari, M.; Samavati, H.; Mehta, S.; Kheirkhahi, A.; Chen, P.; Gong, K.; Vakili-Amini, B.; Hwang, J.; **Chen, M.S.W.**; Terrovitis, M.; Kaczynski, B.; Limotyrakis, S.; Mack, M.; Gan, H.; Lee, M.; Abdollahi-Alibeik, S.; Baytekin, B.; Onodera, K.; Mendis, S.; Chang, A.; Jen, S.; Su, D.; **Wooley, B.**, "A Dual-Band CMOS MIMO Radio SoC for IEEE 802.11n Wireless LAN," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2008.
52. A. Fort, **M. S.-W. Chen**, R.W. Brodersen, C. Desset, P. Wambacq, **L. Van Biesen**, "Impact of Sampling Jitter on Mostly-Digital Architectures for UWB Bio-Medical Applications," *IEEE International Conference on Communications (ICC)*, June 2007.
53. A. Fort, **M. S.-W. Chen**, C. Desset, P. Wambacq, **L. Van Biesen**, "Clock offset tracking for subsampling UWB architectures in a body area network," *IEEE International Conference on Ultra-Wideband (ICUWB)*, Sep. 2007.
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2. **M. S.W. Chen**, "Non-uniform Sampling Analog to Digital Converter (ADC) Architecture with Digital Reconfigurable Anti-Aliasing Filter," filed for provisional patent application, No. 61/911,261, Dec., 2013.
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INVITED TALKS/TUTORIALS/WORKSHOPS

1. ITRI, Taiwan, "New Opportunities in Mixed-Signal ICs", June, 2011.
2. UMC, Taiwan, "New Opportunities in Mixed-Signal ICs", June, 2011.
3. HRL Laboratories, LLC: "Enhancing A-to-D Conversion Efficiency". July 2nd, 2012
4. "Analog-to-Digital Interface: A Time Approach" 2013 CMOS Emerging Technologies Research Symposium, Whistler, July 2013.
5. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Sep. 2013, Broadcom.
6. "Analog-Digital Interface Research, really?" Sep. 2013, Qualcomm-Atheros.
7. "Re-shape Future Mixed-Signal IC Design" Oct. 2013. Qualcomm.
8. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Nov. 2013, UT Dallas.
9. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Nov. 2013, Texas Instrument.
10. "Power efficient ADC Topologies towards RF Sampling" 2014 RFIC Tutorial.
11. "Path Towards Direct RF Synthesis: A Hybrid Digital-to-Analog Converter Architecture" 2014 IEEE MWSCAS Conference, Distinguished Speaker Series.
12. "Asynchronous SAR ADC: Past, Present and Beyond" 2014 IEEE MWSCAS Conference Tutorial
13. "Exploring Limits of Mixed-Signal ICs" Sep. 2014, MaxLinear Corp.
14. "Rethinking Analog-Digital Interface Circuit Architectures" Oct. 2014, IC Seminar, Columbia University, NY.
15. "Rethinking Analog-Digital Interface Circuit Architectures" Mar. 2015, IC Seminar, UC Berkeley, CA.
16. "Rethinking Analog-Digital Interface Circuit Architectures" Dec. 2015, IC Seminar, National Taiwan University(NTU)/IEEE Chapter, Taipei, Taiwan.
17. "Rethinking Analog-Digital Interface Circuit Architectures" Feb. 2016, IC Seminar, UT Austin, Texas.
18. "Asynchronous SAR ADC: Past, Present and Beyond", Feb. 2016, EE department Colloquium, UT Austin/IEEE Chapter.
19. "Rethinking Analog-Digital Interface Circuit Architectures" Feb. 2016, IC Seminar, University of Michigan, Ann Arbor.
20. "Rethinking Analog-Digital Boundary from Circuit to System Level towards Reconfigurability of Everything" Mar. 2016, SystemX Seminar, Stanford

21. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, EE department Colloquium. Carnegie Mellon University (CMU).
22. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, IC Seminar, University of California, Los Angeles (UCLA).
23. "IC Research overview," TSMC, 2017
24. "IC Research overview," Intel Lab, 2017
25. "IC Research overview," InPhi, 2017
26. "Advancing Low-Power High-Speed Analog-to-Digital Converters: An Asynchronous Design Approach", VLSI DAT tutorial, 2017
27. "Generic spur cancellation for digital PLL," Qualcomm 2017
28. "Evolutions of SAR ADC: from High Resolution to High Speed Regime," IEEE CICC 2018 tutorial.
29. "Emerging Opportunities in Analog Mixed-Signal Circuit Design Automation," ACM/IEEE ICCAD 2018 workshop.
30. "Analog-to-Digital Converter Architecture Opportunities in Emerging Wireless Systems," RFIC 2018 workshop
31. "How can hardware designers reclaim the spotlight?" moderator/co-organizer of ISSCC 2019 evening panel.
32. "Fundamentals of Analog-to-digital conversion," 2-day tutorial in Shanghai, China 2019.
33. "Digital Fractional-N Phase Locked Loop Design," tutorial, ISSCC Feb 2020
34. "Digital Fractional-N Phase Locked Loop Design," ISSCCedu Feb 2020
35. "Low Spur PLL architectures," MEAD tutorial in EPFL, 2021 (to appear)
36. "Low Spur PLL architectures and techniques," IEEE CICC 2020
37. "New Opportunities in Nonuniform Sampling," IEEE SSCS Webinar Oct 2020.
38. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IESD Keynote June 2021
39. "ADC Evolution via Architectural Rethinking: from Asynchronous SAR to Non-uniform Sampling ADC," IEEE SSCS Tainan Chapter, Oct 2021
40. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IEEE SSCS Atlanta Chapter, Nov. 2021
41. "Asynchronous SAR ADC: Past, Present and Beyond," IEEE Southern Alberta Chapter, Nov. 2021
42. "Non-Uniform Sampling Data Converters: A Journey to Uncharted Circuits and Systems" IEEE VLSI-DAT April 2022
43. "Asynchronous SAR ADC: Past, Present and Beyond," IEEE Swiss Chapter, May 2022
44. "New Opportunities in Nonuniform Sampling," IEEE Penang Chapter, July 2022
45. "Trend in Digital PLL Design and New Opportunities in Spur Cancellation," IEEE Southern Alberta Chapter, Sep. 2022
46. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IEEE Egypt Chapter Nov. 2022
47. "New Opportunities in Nonuniform Sampling," IEEE Taipei Chapter, Dec. 2022
48. "Trend in Digital PLL Design and New Opportunities in Spur Cancellation," IEEE Tainan Chapter, Dec. 2022

PROFESSIONAL SERVICES

Review Panel:

1. IEEE SSCS James D. Meindl Innovators Award
2. NSF Panelist
3. Samsung Research

Journal article review:

1. IEEE Journal of Solid-State Circuits
2. IEEE Solid-State Circuits Letters (SSC-L)
3. IEEE Transactions on Signal Processing
4. IEEE Transactions on Communications
5. IEEE Transactions on Circuits and Systems I
6. IEEE Transactions on Circuits and Systems II
7. IEEE Transactions on Vehicular Technology
8. IEEE Communications Letters
9. Journal of VLSI Signal Processing Systems

USC Department Services:

1. Munishian Series Committee
2. EFC
3. EE Festival reviewer

Conference TPC:

IEEE European Conference on Solid-State Circuits (ESSCIRC) (2022- present)
IEEE International Solid State Circuits Conference (ISSCC) (2018 - present)
IEEE Symposium on VLSI Circuits (VLSIC) (2017 - 2020)
IEEE Custom Integrated Circuits Conference (CICC) (2015 - 2019)
IEEE GlobalSIP (2014)

Organized/Participated Panel/Forum/Workshops for SSCS:

1. Forum: “Emerging Design Techniques for Data Converters” served as organizer at CICC 2017
2. Panel: “What can/should Circuit Designers do to Ride on the Wave of Machine Learning?” served as co-organizer and moderator at CICC 2018
3. Panel: “How can hardware designers reclaim the spotlight?” served as co-organizer and moderator at ISSCC 2019
4. Panel: “Favorite circuit design and testing mistakes of starting engineers?” served as co-organizer at ISSCC 2021
5. VLSI Symposia Mentoring Event June 2021
6. Panel: “How to choose career path, academia, industry, startups?” served as panelist at CICC 2022 (to appear)
7. Panel: “Open Source Systems, Circuits, and Design: Is It the Future?” served as panelist at CICC 2022 (to appear)

Associate Editor:

SSC-L, TCAS-II

Society Membership:
IEEE Fellow

APPENDIX 2: MATERIALS CONSIDERED IN THE PREPARATION OF THIS DECLARATION

Exhibit No.	Description
1001	U.S. Patent No. 10,877,233 to Dai, et al. (“the ’233 patent”)
1002	Certified Prosecution File History for the ’233 patent (“Prosecution History”)
1004	U.S. Patent No. 9,882,706 to Lugthart, et al. (“Lugthart”)
1005	U.S. Patent No. 7,233,617 to Gorecki (“Gorecki”)
1006	U.S. Patent No. 8,516,238 to Cornelius, et al. (“Cornelius”)
1007	Samaan, High-speed Serial Bus Repeater Primer (“Samaan”)
1008	Ars Technica, Why Thunderbolt cables will be expensive until 2013
1009	Intersil, ISL37231 [Datasheet]
1010	U.S. Patent Application Publication No. 2019/0028262 A1 to Kobayashi, et al. (“Kobayashi”)
1011	TE Connectivity, SFP+ High Speed Copper Cable Assemblies
1012	Cisco, Cisco 40GBASE QSFP Modules Data Sheet
1013	AppleInsider, Intel details Thunderbolt, says Apple has full year head start
1014	macstories, Intel: Apple Transferring Thunderbolt Trademark To Us
1015	AnandTech, Intel’s Codename Light Peak Launches as Thunderbolt
1016	Ars Technica, The technology inside Apple’s \$50 Thunderbolt cable
1017	Gasca, et al., CMOS Continuous-Time Adaptive Equalizers for High-Speed Serial Links
1018	Declaration of June Munford re: Samaan
1019	Excerpts from 10G SFP+ Video
1020	Excerpts from Stauffer, High Speed Serdes Devices and Applications (“Stauffer”)
1021	PCI-SIG, PCI Express® Retimers vs. Redrivers An Eye-Popping Difference
1022	<i>Certain Active Electrical Cables and Components Thereof</i> , ITC Investigation 337-TA-1446, Exhibit 37 to Complaint, Credo’s Infringement Claim Chart Showing Molex’s Infringement of the ’233 Patent

Exhibit No.	Description
1023	<i>Certain Active Electrical Cables and Components Thereof</i> , ITC Investigation 337-TA-1446, Exhibit 40 to Complaint, Credo's Infringement Claim Chart Showing TE Connectivity's Infringement of the '233 Patent
1024	<i>Certain Active Electrical Cables and Components Thereof</i> , ITC Investigation 337-TA-1446, Exhibit 65 to Complaint, Credo's Domestic Industry Claim Chart for the '233 Patent
1025	SFF-8431 Rev 4.1 + Addendum
1026	Texas Instruments Technical Article, How to Reduce Jitter and Improve Signal Integrity in Source and Sink System Designs Supporting HDMI 2.0
1027	Intel, Thunderbolt™ Networking Bridging and Routing Instructional White Paper
1028	Intel, PCI Express Ethernet Networking White Paper
1029	U.S. Patent No. 9,231,846 to Sinha, et al. ("Sinha")
1030	<i>Reserved</i>
1031	U.S. Patent No. 8,787,430 to Rhagavan, et al. ("Raghavan")
1032	<i>Reserved</i>
1033	Intel, PCI Express Architecture
1034	Internet Archive Capture, The Wayback Machine, Wikipedia, "PCI Express"
1035	Intel Website Search Results

APPENDIX 3: CHALLENGED CLAIMS

[1pre] A cable that comprises:

[1a] a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;

[1b] a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and

[1c] electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,

[1d] first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and

[1e] the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,

[1f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.

3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.

5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

6. The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

7. The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

[8pre] A cable manufacturing method that comprises:

[8a] connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;

[8b] connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;

[8c] connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,

[8d] the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and

[8e] the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,

[8f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

9. The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring

10. The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

11. The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.

12. The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

13. The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

14. The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

[15pre] A communications method that comprises:

[15a] inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host

interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and

[15b] inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,

[15c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

16. The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.

17. The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

18. The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.

19. The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

20. The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

APPENDIX 4: UNDERSTANDING OF THE LAW

I have applied the following legal principles provided to me by counsel in arriving at the opinions set forth in this report.

Legal Standard for Prior Art

I am not an attorney. I have been informed by attorneys of the relevant legal principles and have applied them to arrive at the opinions set forth in this declaration.

I understand that the petitioner for inter partes review may request the cancellation of one or more claims of a patent based on grounds available under 35 U.S.C. § 102 and 35 U.S.C. § 103 using prior art that consists of patents and printed publications.

Anticipation and Prior Art

I understand that § 102 specifies when a challenged claim is invalid for lacking novelty over the prior art, and that this concept is also known as “anticipation.” I understand that a prior art reference anticipates a challenged claim, and thus renders it invalid by anticipation, if all elements of the challenged claim are disclosed in the prior art reference. I understand the disclosure in the prior art reference can be either explicit or inherent, meaning it is necessarily present or implied. I understand that the prior art reference does not have to use the same words as the challenged claim, but all of the requirements of the claim must

be disclosed so that a person of ordinary skill in the art could make and use the claimed subject-matter.

In addition, I understand that § 102 also defines what is available for use as a prior art reference to a challenged claim.

Under § 102(a)(1), a challenged claim is anticipated if it was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the challenged claimed invention.

Under § 102(a)(2), a challenged claim is anticipated if it was described in an issued patent, or in an application for patent that was published by the USPTO, in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the challenged claimed invention.

I understand that the filing date of a patent is generally the filing date of the application filed in the United States that issued as the patent. However, I understand that a patent may be granted an earlier effective filing date if the patent owner properly claimed priority to an earlier patent application.

I understand that when a challenged claim covers several structures, either generically or as alternatives, the claim is deemed anticipated if any of the structures within the scope of the claim is found in the prior art reference.

I understand that when a challenged claim requires selection of an element from a list of alternatives, the prior art teaches the element if one of the alternatives is taught by the prior art.

Legal Standard for Obviousness

I understand that even if a challenged claim is not anticipated, it is still invalid if the differences between the claimed subject matter and the prior art are such that the claimed subject matter would have been obvious to a person of ordinary skill in the pertinent art at the time the alleged invention.

I understand that obviousness must be determined with respect to the challenged claim as a whole.

I understand that one cannot rely on hindsight in deciding whether a claim is obvious.

I also understand that an obviousness analysis includes the consideration of factors such as (1) the scope and content of the prior art, (2) the differences between the prior art and the challenged claim, (3) the level of ordinary skill in the pertinent art, and (4) “secondary” or “objective” evidence of non-obviousness.

Secondary or objective evidence of non-obviousness includes evidence of: (1) a long felt but unmet need in the prior art that was satisfied by the claimed invention; (2) commercial success or the lack of commercial success of the claimed invention; (3) unexpected results achieved by the claimed invention; (4)

praise of the claimed invention by others skilled in the art; (5) taking of licenses under the patent by others; (6) deliberate copying of the claimed invention; and (7) contemporaneous and independent invention by others. However, I understand that there must be a relationship between any secondary evidence of non-obviousness and the claimed invention.

I understand that a challenged claim can be invalid for obviousness over a combination of prior art references if a reason existed (at the time of the alleged invention) that would have prompted a person of ordinary skill in the art to combine elements of the prior art in the manner required by the challenged claim. I understand that this requirement is also referred to as a “motivation to combine,” “suggestion to combine,” or “reason to combine,” and that there are several rationales that meet this requirement.

I understand that the prior art references themselves may provide a motivation to combine, but other times simple common sense can link two or more prior art references. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may come from market forces.

I understand obviousness to include, for instance, scenarios where known techniques are simply applied to other devices, systems, or processes to improve them in an expected or known way. I also understand that practical and common-

sense considerations should be applied in a proper obviousness analysis. For instance, familiar items may have obvious uses beyond their primary purposes.

I understand that the combination of familiar elements according to known methods is obvious when it yields predictable results. For instance, obviousness bars patentability of a predictable variation of a technique even if the technique originated in another field of endeavor. This is because design incentives and other market forces can prompt variations of it, and predictable variations are not the product of innovation, but rather ordinary skill and common sense.

I understand that a particular combination may be obvious if it was obvious to try the combination. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. This would result in something obvious because the result is the product not of innovation but of ordinary skill and common sense. However, I understand that it may not be obvious to try a combination when it involves unpredictable technologies.

It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, I understand that any need or problem known in the field of

endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

It is my understanding that the Manual of Patent Examining Procedure §2143 sets forth the following as exemplary rationales that support a conclusion of obviousness:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- Choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;

- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

A person of ordinary skill in the art looking to overcome a problem will often use the teachings of multiple publications together like pieces of a puzzle, even though the prior art does not necessarily fit perfectly together. Therefore, I understand that references for obviousness need not fit perfectly together like puzzle pieces. Instead, I understand that obviousness analysis takes into account inferences, creative steps, common sense, and practical logic and applications that a person of ordinary skill in the art would employ under the circumstances.

I understand that a claim can be obvious in light of a single reference, if the elements of the challenged claim that are not explicitly or inherently disclosed in the reference can be supplied by the common sense of one of skill in the art.

I understand that obviousness also bars the patentability of applying known or obvious design choices to the prior art. One cannot patent merely substituting one prior art element for another if the substitution can be made with predictable results. Likewise, combining prior art techniques that are interoperable with respect to one another is generally obvious and not patentable.

In order for a claim to be found invalid based upon a modification or combination of the prior art, there must be reasonable expectation that a person of ordinary skill would have successfully modified or combined the prior art to arrive at the claimed arrangement. This does not mean that it must be certain that a person of ordinary skill would have been successful – the law only requires that the person of ordinary skill in the art would have perceived a reasonable expectation of success in modifying or combining the prior art to arrive at the claimed invention.

In sum, my understanding is that obviousness invalidates claims that merely recite combinations of, or obvious variations of, prior art teachings using understanding and knowledge of one of skill in the art at the time and motivated by the general problem facing the inventor at the time. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of or attempting obvious variations on prior art references in the claimed manner.

Legal Standard for Claim Construction

I understand that before any invalidity analysis can be properly performed, the scope and meaning of the challenged claims must be determined by claim construction.

I understand that a patent may include two types of claims, independent claims and dependent claims. I understand that an independent claim stands alone

and includes only the limitations it recites. I understand that a dependent claim depends from an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to the limitations recited in the claim (or claims) from which it depends.

In comparing the challenged claims to the prior art, I have carefully considered the patent and its file history in light of the understanding of a person of skill at the time of the alleged invention.

I understand that to determine how a person of ordinary skill would have understood a claim term, one should look to sources available at the time of the alleged invention that show what a person of skill in the art would have understood disputed claim language to mean. It is my understanding that this may include what is called “intrinsic” evidence as well as “extrinsic” evidence.

I understand that, in construing a claim term, one should primarily rely on intrinsic patent evidence, which includes the words of the claims themselves, the remainder of the patent specification, and the prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient. I understand that extrinsic evidence may include principles, concepts, terms, and other resources available to those of skill in the art at the time of the invention.

I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else or something more specific. I understand that to determine whether a term has special meaning, the claims, the patent specification, and the prosecution history are particularly important, and may show that the inventor gave a term a particular definition or intentionally disclaimed, disavowed, or surrendered claim scope.

I understand that the claims of a patent define the scope of the rights conferred by the patent. I understand that because the claims point out and distinctly claim the subject matter which the inventors regard as their invention, claim construction analysis must begin with and is focused on the claim language itself. I understand that the context of the term within the claim as well as other claims of the patent can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, how a term is used in one claim can often inform the meaning of the same term in other claims. Differences among claims or claim terms can also be a useful guide in understanding the meaning of particular claim terms.

I understand that a claim term should be construed not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the entire specification. I understand that because the

specification is a primary basis for construing the claims, a correct construction must align with the specification.

I understand that the prosecution history of the patent as well as art incorporated by reference or otherwise cited during the prosecution history are also highly relevant in construing claim terms. For instance, art cited by or incorporated by reference may indicate how the inventor and others of skill in the art at the time of the invention understood certain terms and concepts. Additionally, the prosecution history may show that the inventors disclaimed or disavowed claim scope, or further explained the meaning of a claim term.

With regard to extrinsic evidence, I understand that all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises, can also be considered. For example, technical dictionaries may indicate how one of skill in the art used or understood the claim terms. However, I understand that extrinsic evidence is considered to be less reliable than intrinsic evidence, and for that reason is generally given less weight than intrinsic evidence.

I understand that in general, a term or phrase found in the introductory words or preamble of the claim, should be construed as a limitation if it recites essential structure or steps, or is necessary to give meaning to the claim. For instance, I understand preamble language may limit claim scope: (i) if dependence

on a preamble phrase for antecedent basis indicates a reliance on both the preamble and claim body to define the claimed invention; (ii) if reference to the preamble is necessary to understand limitations or terms in the claim body; or (iii) if the preamble recites additional structure or steps that the specification identifies as important.

On the other hand, I understand that a preamble term or phrase is not limiting where a challenged claim defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention. I understand that to make this determination, one should review the entire patent to gain an understanding of what the inventors claim they invented and intended to encompass in the claims.

I understand that 35 U.S.C. § 112(f) created an exception to the general rule of claim construction called a “means plus function” limitation. These types of terms and limitations should be interpreted to cover only the corresponding structure described in the specification, and equivalents thereof. I also understand that a limitation is presumed to be a means plus function limitation if (a) the claim limitation uses the phrase “means for”; (b) the “means for” is modified by functional language; and (c) the phrase “means for” is not modified by sufficient structure for achieving the specified function.

I understand that a structure is considered structurally equivalent to the corresponding structure identified in the specification only if the differences between them are insubstantial. For instance, if the structure performs the same function in substantially the same way to achieve substantially the same result. I further understand that a structural equivalent must have been available at the time of the issuance of the claim.