

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MARVELL SEMICONDUCTOR, INC.,
Petitioner,

v.

CREDO TECHNOLOGY GROUP LTD.,
Patent Owner.

Case IPR2025-01218
U.S. Patent No. 10,877,233

PATENT OWNER'S RESPONSE

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TABLE OF EXHIBITS

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2001	Credo’s Corrected Unopposed Motion to Partially Terminate the Investigation by Withdrawing Allegations With Respect to U.S. Patent No. 10,877,233, 337-TA-1446
2002	Credo’s and Fish & Richardson P.C.’s Opposition to Non-Party Marvell Semiconductor, Inc.’s Motion to Disqualify, 337-TA-1446 (public version)
2003	In re Certain Active Electrical Cables and Components Thereof, Inv. No. 337-TA-3814, Complaint (Mar. 13, 2025).
2004	“Credo Introduces PAM4 DSP for High Performance Data Centers and Enterprise Networks,” March 17, 2021, https://credosemi.com/credo-introduces-pam4-dsp-for-high-performance-data-centers-and-enterprise-networks/
2005	“AEC Applications,” https://credosemi.com/products/hiwire-aec/applications/
2006	“Credo Introduces 800G HiWire ZeroFlap AECs to Support AI Backend Networks,” October 10, 2024, available at https://s205.q4cdn.com/511065572/files/doc_news/2024/10/credo-introduces-800g-hiwire-zeroflap-aecs-to-support-ai-backend-networks.pdf
2007	“CREDO Receives Cabling Installation & Maintenance Innovators 2019 Gold Award for HiWire™ Active Electrical Cables (AEC),” October 1, 2019, https://credosemi.com/news/credo-receives-cabling-installation-maintenance-innovators-2019-gold-award-for-hiwire-active-electrical-cables-aec/
2008	“Credo Files AEC Patent Infringement Complaint Against Amphenol, Molex, TE Connectivity, and Volex with United States International Trade Commission,” March 13, 2025, https://investors.credosemi.com/news-events/news/news-details/2025/Credo-Files-AEC-Patent-Infringement-Complaint-Against-Amphenol-Molex-TE-Connectivity-and-Volex-with-United-States-International-Trade-Commission/default.aspx
2009	Order No. 21 Granting Corrected Motion to Terminate the Investigation by Withdrawing Allegations With Respect to U.S. Patent No. 10,877,233, 337-TA-1446
2010-2019	RESERVED

Exhibit	Description
2020	Declaration of Tim A. Williams dated May 1, 2026
2021	April 29, 2026 Deposition Transcript of Michael Chen
2022	“Credo and Volex Reach Settlement in Active Electrical Cable Patent Infringement Dispute,” Press Release dated August 26, 2025
2023	“Credo and Amphenol Reach Settlement Agreement in Active Electrical Cable Patent Infringement Disputes,” Press Release dated August 14, 2025
2024	“Credo and 3M Enter Into Patent License Agreement,” Press Release dated January 22, 2026
2025	“Credo and Molex Reach Settlement in Active Electrical Cable Patent Infringement Disputes,” Press Release dated March 26, 2026
2026	“Credo and TE Connectivity Reach Settlement in Active Electrical Cable Disputes,” Press Release dated March 27, 2026
2027	“Credo Licenses its Active Electrical Cable Patents to the Siemon Company,” Press Release dated November 24, 2025
2028	“Credo Announces Production Availability of HiWire Active Electrical Cables,” Press Release dated September 4, 2019, available at https://investors.credosemi.com/news-events/news/news-details/2019/Credo-Announces-Production-Availability-of-HiWire-Active-Electrical-Cables-09-04-2019/default.aspx
2029	Equity Research: Credo Technology Group Holding Ltd: Initiation of Research Coverage, William Blair, dated September 18, 2025, available at https://www.williamblair.com/News/Credo-Technology-Group-Holding-Ltd-Initiation
2030	RESERVED
2031	“This Company Supplying AI Datacenters With Cables Just Minted Two New Billionaires,” Forbes December 1, 2025, available at https://www.forbes.com/sites/emilygarcia/2025/12/01/this-company-supplying-ai-datacenters-with-cables-just-minted-two-new-billionaires/

I. INTRODUCTION

Petitioner Marvell Semiconductor, Inc. challenges the patentability of U.S. Patent No. 10,877,233 (the “’233 patent”). The invention described and claimed in the ’233 patent, assigned to Patent Owner Credo Technology Group Limited, arose from Credo’s creation of a brand new category of Ethernet cables now known as Active Electrical Cables (“AECs”). Credo coined the term Active Electrical Cable when it released its first AEC in 2019. Ex-2028. Until then, data centers typically used optical cables for high-speed connections between components in a server rack. Traditional Ethernet cables could not support the increased demand for data speed, leaving optical cables as the only choice. Pioneering an entirely new market, Credo introduced AECs that are less expensive to buy, require less power to operate, and perform more reliably than optical cables. Ex-2029. Within months, Credo’s AECs won the 2019 Gold Award from the Cabling Installation & Maintenance Innovators. Ex-2007. Since then, Forbes magazine reports that Credo’s distinctive purple AECs, pictured below, “have become indispensable in the AI infrastructure buildout.” Ex-2031.



Recognizing Credo's success, competitors have since entered the AEC market with their own AECs, many of which are now licensed to Credo's patents. Petitioner designs and supplies components that may be used in AECs and is now challenging the '233 patent as well as two other Credo patents related to AECs. For multiple reasons, Petitioner has failed to meet its burden of showing that any claim of the '233 patent is unpatentable.

First, Petitioner relies on nonexistent disclosures. For example, Ground 1 relies on generic boilerplate in the Lugthart reference as alleged teaching of transmit filter coefficients stored in nonvolatile memory. The boilerplate language does not describe the claimed feature. Nor does any other Lugthart disclosure, and for good reason. Lugthart teaches the use of adaptive filter coefficients that would

not be stored in nonvolatile memory because it would be slow and inefficient.

Petitioner fails to address this point.

Second, Petitioner would combine features from different references that are simply incompatible. Recognizing the deficiency in Ground 1 and the Lugthart teachings, Petitioner adds the Gorecki reference in Ground 2, relying on Gorecki for disclosure of the claimed filter coefficients stored in nonvolatile memory. But Petitioner fails to explain why a person of ordinary skill in the art would have used Gorecki's static filter coefficients when Lugthart already teaches using adaptive coefficients that would not be stored in nonvolatile memory. The combination would frustrate the very purpose of Lugthart, which teaches away from the claimed feature.

Third, Petitioner fails to demonstrate a motivation to combine Lugthart and Gorecki in the first place. Unlike Lugthart, Gorecki is directed to data connectivity in the backplane of a server rack, which involves different channel characteristics than Ethernet cables. The channel characteristics of a backplane are known and relatively constant, and Gorecki's predetermined, pre-stored filter coefficients make sense in that application. By contrast, the channel characteristics of Ethernet cables are more dynamic and may change every time the cable is connected and powered up, which is why Lugthart teaches adaptive filter coefficients that would not be stored in nonvolatile memory. Petitioner makes no effort to explain how or

why a person of ordinary skill in the art would have combined features from these two different references to arrive at the claimed invention. The combination makes sense only when viewed through the improper lens of hindsight reconstruction.

Similar deficiencies permeate Grounds 3 and 4, leaving the entire petition short of meeting Petitioner's burden of proving unpatentability. As explained in more detail below, Patent Owner respectfully submits that the Board should affirm the patentability of all twenty claims of the '233 patent.

II. THE '233 PATENT

The '233 Patent is directed to an active Ethernet cable with preset pre-equalization. Ex. 1001, Title. As the abstract explains, the cable “employ[s] preset transmit-side equalization to provide enhanced performance and/or to reduce receive-side equalization requirements.” Ex-1001, Abstract, 1:45-48. The cable of the '233 Patent includes first and second connectors 100, 101 electrically connected via electrical conductors 106. *Id.*, 3:36-40. The electrical conductors 106 can be in a paired form with twinaxial conductors driven with a differential signal. *Id.*

Each connector 100, 101 includes “a powered transceiver that performs clock and data recovery (CDR) and re-modulation of data streams, hereafter called a data recovery and re-modulation (DRR) device.” *Id.*, 3:51-55. “The first and second DRR devices provide pre-equalization of the electrical transit signals

[conveyed by the electrical conductors therebetween] using transmit filter coefficient values stored in nonvolatile memories.” *Id.*, Abstract; 1:44-2:30, 2:43-45.

The ’233 Patent discloses that each of the connectors 100, 101 of the cable illustrated in FIG. 3A includes a DRR device 202, 204 “to perform CDR and re-modulation of the data streams entering and exiting the cable” at the respective connector. Ex-1001, 4:54-59. Each DRR device has “a set 220 of transmitters and receivers for communicating with the host device and a set 222 of transmitters and receivers for sending and receiving via conductor pairs running the length of the cable.” *Id.*, 5:16-20. An “embedded controller 228” in each DRR device “coordinates the operation of the transmitters and receivers” using a “set of registers 208.” *Id.*, 5:27-35.

The transmitter and receiver sets 210 and 212 are described as follows:

In at least some contemplated embodiments, the host-facing transmitter and receiver set 220 employ fixed equalization parameters that are cable-independent, i.e., they are not customized on a cable-by-cable basis. The center-facing transmitter and receiver set 222 preferably employ cable-dependent equalization parameters that are customized on a cable-by-cable basis. The cable-dependent equalization parameters may be adaptive or fixed, and initial values for these parameters may be determined during manufacturer tests of the cable. The equalization parameters may include filter coefficient values for pre-equalizer filters in the transmitters, and gain and filter coefficient values for the receivers.

Ex-1001, 5:36-48.

Each connector 100, 101 also includes “a micro-controller unit (MCU) 206” that is coupled to and configures the operation of the connector’s DRR device. *Id.* at 4:65-5:2. “At power-on, the MCU device 206 loads equalization parameters from Flash memory 207 into the DRR device’s configuration registers 208.” *Id.* at 5:3-5.

The cable illustrated in FIG. 3A forms “a part of a point-to-point communications link between two host devices 302, 304 as shown in the architectural diagram of FIG. 3B.” *Id.* at 5:49-5:52, FIG. 3A-3B. The connectors 100, 101 of the cable illustrated in FIG. 3A have “plugs 200, 201” that fit standard-compliant Ethernet ports of the two host devices. *Id.* at, 4:47-54.

III. PETITIONER’S CHALLENGE TO THE ’233 PATENT

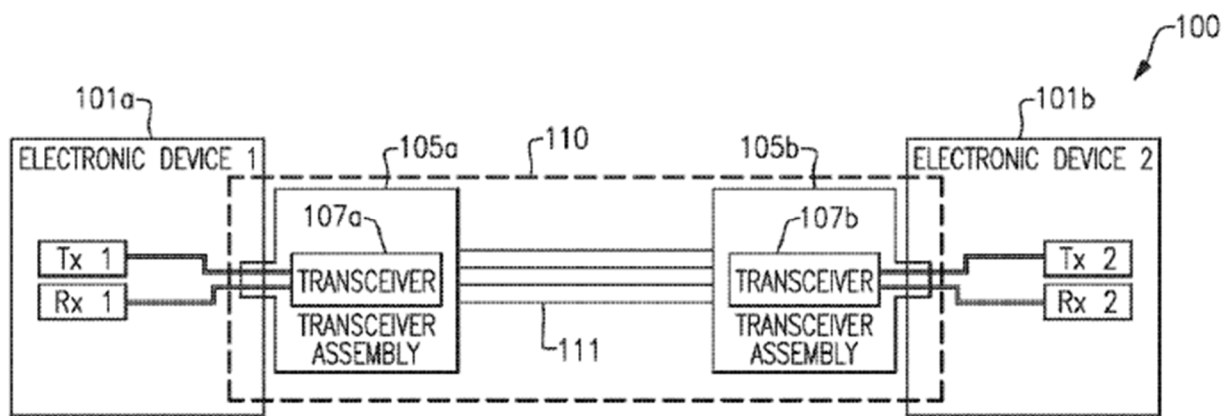
Ground	Claims	Combination
1	1, 6, 8, 13, 15	§103: Lugthart
2	1-20	§103: Lugthart and Gorecki
3	7, 14, 20	§103: Lugthart, Gorecki, and Samaan
4	1-20	§103: Cornelius, Samaan, and Gorecki

A. Lugthart (Ex-1004)

U.S. Patent No. 9,882,706 to Lugthart *et al.* (“Lugthart”) is directed to “[s]ystems and methods for high speed communications,” including “transceiver architectures and techniques for retiming, multiplexing, de-multiplexing and

transmitting data.” Ex-1004, Abstract. Specifically, Lugthart describes a transceiver system that interfaces between a host electronic device (e.g., electronic device 101a) and a line-side medium such as copper cable lines (e.g., cable conducting lines 111) and uses adaptive (*i.e.*, not preset) equalization. Ex-1004, FIGS. 1A, 2A, 4A, 4B, 47:53-64, 48:64-49:37.

Lugthart, FIG. 2A depicts a high-speed point-to-point communication system 100 that includes an active cable 110 connecting a first electronic device 101a and a second electronic device 101b. The cable 110 has “first and second transceiver assemblies 105a, 105b,” including first and second transceivers 107a, 107b, respectively, positioned at either end of conductive lines 111. Ex-1004, 14:9-11, 14:31-34.



Ex-1004 at FIG. 2A

To maintain signal integrity over the cable conducting lines 111, Lugthart specifically provides a transceiver structure (e.g., transceiver 107a) that

compensates for signal degradation. Ex-1004, 6:41-45 (“[t]he performance of communication systems is limited . . . by factors including intersymbol interference (ISI) and other characteristics . . . associated with the cable including loss, noise, dispersion and non-linear response”), 15:5-20 ([i]ntegrating transceivers into a cable can achieve a wide variety of advantages . . . an active cable [having integrated transceiver(s)] can permit communication over longer distance . . . with a thinner cable . . . using an active cable [having integrated transceiver(s)] can decrease jitter, noise, and/or ISI relative to a configuration using a passive cable”).

Lugthart’s transceiver architecture, includes a transceiver 10 that implements first and second transceivers 107a, 107b, is divided into two directional paths—a transmit path (“EGRESS/TRANSMIT”) and a receive path (“INGRESS/RECEIVE”)—each of which includes respective components including equalizers (EQ), finite impulse response (FIR) filters, digital signal processors (DSPs), clock and data recovery (CDR) circuits. Ex-1004, FIGS. 1A, 2A, 9:10-10:22.

Lugthart’s “EGRESS/TRANSMIT” and “INGRESS/RECEIVE” (e.g., in FIGS. 1A and 2A) indicate the direction of signal flow relative to the host device 101a and the cable conducting lines 111. Ex-1004, FIGS. 1A, 2A. For example, a signal travels from a host device (e.g., 101a) through a transceiver module, and to

the cable lines 111 on the EGRESS side, and a signal travels from the cable lines 111 through a transceiver module, and to a host device on the INGRESS side. *Id.*

Lugthart describes efforts to compensate for loss in the cable conducting lines 111. Ex-1004, 6:41-45, 6:55-57, 15:5-10; 9:10-12, 9:65-10:2, 23:59-24:2. According to Lugthart, implementations of the transceivers include “adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).” *Id.*, 29:21-28 Therefore, Lugthart explains that for purposes of establishing a high-speed communication link between two electronic devices, the operating parameters for the equalizers are adjusted during one or more training phases, after a start-up phase. *Id.*, 47:53-64, 48:64-49:37.

B. Gorecki (Ex-1005)

U.S. Patent No. 7,233,617 to Gorecki (“Gorecki”) is directed to backplane technology, not active cables. In particular, Gorecki describes “a technique of, and system for enhancing the performance of high-speed digital communications through a communications channel, for example a backplane.” Ex-1005, Abstract. Gorecki was filed on April 10, 2003 and issued on June 19, 2007. *Id.*, Cover. Gorecki addresses the problem of signal reflections and signal dispersion—also known as intersymbol interference—caused by bandwidth limitations of the

communications channel in backplane environments. Ex-1005, Abstract, 1:33-58, 6:3-22.

Gorecki's solution is transmitter-side equalization circuitry implemented as an analog FIR filter with leading and trailing taps that temporally overlap with the data signal to compensate for pre-cursor and post-cursor intersymbol interference. Ex-1005, Abstract, 6:3-37, 6:38-44, 9:3-15, 10:1-11, 18:35-61, Fig. 5A-5B. Every embodiment in Gorecki is directly applicable to backplane communications and every claim recites backplane applications. *See e.g.*, Ex-1005, 3:8-45, 4:16-27, 4:53-64, 6:3-6, 8:1-8, Figs. 3-4, Claims 1, 11, 22. Gorecki does not describe or suggest any application to active cables. In Gorecki's architecture, the communications channel is a passive medium (a backplane trace) over which the transmitter sends equalized signals to a remote receiver.

C. Cornelius (Ex-1006)

U.S. Patent No. 8,516,238 to Cornelius *et al.* ("Cornelius") is directed to solving the problem of accommodating a legacy standard (*e.g.*, DisplayPort) and newer standards (*e.g.*, HSIO or T29) utilizing the same physical connector. Ex-1006, 3:54-4:9, 5:33-39. In particular, Cornelius describes "[c]ircuits, methods, and apparatus that allow signals that are compliant with multiple standards to share a common connector on an electronic device." Ex-1006, Abstract. Cornelius discloses cables that include "two active plugs...one on each end of cable," each

with “dual clock and data recovery circuits for retiming data” and a cable microcontroller to configure those circuits. Ex-1006, 6:6-24, Figs. 5-6.

To accommodate the dual-standard objective, Cornelius’s core teaching is a connector pinout arrangement and associated circuitry that enables signals from two different standards to share common connector pins without interfering with one another. *See* Ex-1006 at 2:20-26. Cornelius describes how pins for a newer high-speed standard may be arranged to reduce crosstalk and interference among themselves, and how additional circuitry—such as resistors, PiN diodes, multiplexers, coupling capacitors, and inductors—may be used to isolate the signal paths of the two standards from each other. *Id.*

D. Samaan (Ex-1007)

Samaan is a technical paper titled “High-speed Serial Bus Repeater Primer,” authored by Samie B. Samaan, Dan Froelich, and Samuel Johnson of Intel Corporation (“Samaan”) and is dated October 2015. Ex-1007, Cover. The paper provides an overview of SerDes repeaters—specifically re-drivers and re-timers—describing their micro-architecture, properties, applications, and limitations in the context of high-speed serial bus standards such as PCIe 3.0. Ex-1007, ¶¶ 1-8.

Like Lugthart, and unlike the ’233 Patent, Samaan is fundamentally directed to adaptive equalization. Ex-2020, ¶ 60. The central theme of Samaan is that equalization coefficients are determined dynamically through link training and

adaptation protocols, where transmitters and receivers negotiate optimal TxEQ settings in real time. *Id.* For PCIe 3.0, Samaan describes a four-phase TxEQ adaptation protocol in which both link partners exchange information about their supported equalization ranges (Phase 0), establish initial communication (Phase 1), and then iteratively request coefficient changes from each other until each receiver finds an optimal setting (Phases 2 and 3). Ex-1007, ¶¶ 83-87. The “intent of adaptation is to allow both agents to adjust the link partner’s TxEQ to an optimal value for their receiver, and for the specific channel and operating conditions at hand.” Ex-1007, ¶ 78.

IV. LEGAL STANDARDS

A patent claim is unpatentable for obviousness if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). In *Graham v. John Deere Co.*, 383 U.S. 1 (1966), the Supreme Court set out a framework for assessing obviousness that requires consideration of four factors: (1) the “level of ordinary skill in the pertinent art,” (2) the “scope and content of the prior art,” (3) the “differences between the prior art and the claims at issue,” and (4) “secondary considerations”

of non-obviousness such as “commercial success, long felt but unsolved needs, failure of others, etc.” 383 U.S. at 17-18.

V. LEVEL OF SKILL IN THE ART

Petitioner defines a person of ordinary skill in the art (“POSITA”) as an individual who “would have been a person with a bachelor’s degree in electrical or computer engineering with at least three years of experience in the field []. A person with less practical experience but more relevant education may also meet this standard.” Pet. at 14-15. Because the ordinary level of skill in the art does not affect the ultimate analysis, neither Patent Owner nor Dr. Williams takes a position in general with respect to Petitioner’s proposed level of ordinary skill in the art. Solely for the purposes of this proceeding, however, Patent Owner and Dr. Williams employ the same level of skill in the art that Petitioner has proposed. *See also* Ex-2020, ¶¶ 17-18.

VI. CLAIM CONSTRUCTION

In an *inter partes* review filed on or after November 13, 2018, claim terms are construed based on their ordinary and customary meaning. 37 C.F.R. § 42.100(b). Further, the Board should always construe claims to sustain their validity, if possible. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1329 (Fed. Cir. 2005). Patent Owner requests that the Board adopt the ordinary and customary meaning of the claim terms as understood by one of ordinary skill in the art.

VII. THE CHALLENGED CLAIMS ARE NOT UNPATENTABLE

A patent claim “is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *KSR*, 550 U.S. at 418.

An obviousness determination based on a combination of references also requires finding “both ‘that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.’”

Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd., 821 F.3d 1359, 1367-68 (Fed. Cir. 2016) (citation omitted); *see KSR*, 550 U.S. at 418.

Petitioner has failed to show that the cited prior art renders obvious the Challenged Claims and has not articulated any meaningful motivation to combine or a reasonable expectation of success. Petitioner also fails to account for secondary indicia of non-obviousness, which further demonstrates that the original claims of the '233 Patent were patentable. Petitioner selectively relies on different features from different and unrelated references, purporting to combine those features but without explaining how or why one of ordinary skill in the art would have been motivated to do so. Petitioner views the prior art improperly through the lens of hindsight bias, without which one of ordinary skill in the art would not have been motivated to cherry-pick features as Petitioner now proposes. For these and the reasons stated below, the Petition fails.

A. Ground 1: Petitioner has not shown that Lugthart teaches claims 1, 6, 8, 13, or 15

1. Lugthart does not teach pre-equalization “using transmit filter coefficient values stored in nonvolatile memories.”

Ground 1 purports to challenge claims 1, 6, 8, 13, and 15 based on Lugthart alone. However, Ground 1 does not actually address claims 6 or 13, limiting its analysis solely to claims 1, 8, and 15. Patent Owner responds here accordingly.

Claims 1, 8, and 15 (as well as claims 6 and 13) share a common limitation that is not disclosed or rendered obvious by Lugthart: the requirement that the DRR devices provide pre-equalization “using transmit filter coefficient values stored in nonvolatile memories.” This limitation appears as [1f] in claim 1, [8f] in claim 8, and [15c] in claim 15.

a) Lugthart’s generic disclosure does not convey the necessary information to one of skill in the art

Relying on nothing more than generic boilerplate, Petitioner incorrectly asserts that Lugthart teaches storing filter coefficient values in nonvolatile memory, as required by challenged limitations [1f]/[8f]/[15c]. It does not. Lugthart suggests the opposite by teaching adaptive coefficient values that are determined and continuously adjusted during runtime and would not be stored in nonvolatile memory.

In particular, Petitioner’s argument regarding Lugthart’s alleged disclosure of these limitations rests solely on Lugthart’s generic disclosure about computer-readable media found at the end of Lugthart’s detailed description in a boilerplate recitation that is not directed to any embodiment described in Lugthart. *See* Pet. at 36-37 (citing Ex-1004 at 56:62-57:30, 57:30-39, 57:40-67). Closer review of this boilerplate disclosure shows that it at best addresses the general question of where the software implementing the described functionality (e.g., program instructions) could reside. Ex-1004 at 57:40-42 (“If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium.”). This does not teach, suggest, or even mention storing FIR filter coefficients—which are operational parameters, not program instructions—in nonvolatile memory. A person of ordinary skill in the art (“POSITA”) would understand that there is a critical distinction between (a) the program code that *implements* an FIR filter algorithm and (b) the coefficient *values* that the FIR filter uses during operation. Program code is static and does not change during operation; coefficient values, by contrast, are dynamic operational parameters that are determined based on channel conditions and may change frequently. Ex-2020, ¶ 63.

b) Lugthart is directed to adaptive, rather than pre-stored coefficient values

The disclosure of Lugthart actually suggests that any coefficient values would be stored in volatile, rather than nonvolatile memory. Lugthart's specification describes a comprehensive adaptive equalization system in which coefficients are determined dynamically at runtime through channel negotiation. Ex-2020, ¶ 65. Lugthart does not describe storing these adaptive equalization coefficients in nonvolatile memory, likely because one of ordinary skill in the art would have known that it would be inefficient to do so.

Lugthart describes a multi-phase channel negotiation process with three distinct stages. In the start-up phase, the transceivers establish a low-speed communication channel and perform “[a] basic channel test . . . to determine the channel parameters such as, for example, loss, noise, dispersion, non-linearity, etc.” Ex-1004, 48:20-23. In the full speed training phase, “the parameters of the components in the transceivers connected to the first and second electronic devices are adjusted such that NRZ modulated signals at the full baud rate can be transmitted and received at an error rate that is below or equal to a threshold error value.” Ex-1004, 49:1-10. Lugthart specifically identifies the parameters adjusted in this phase as including “the shape of the transmitted pulse” and “operating parameters for the equalizers.” Ex-1004, 49:5-12. In the full functional training

phase, the parameters are “further adjusted such that signals modulated using a multi-level modulation format at the full baud rate can be transmitted and received.” Ex-1004, 51:20-30.

The reference to “operating parameters for the equalizers” in the training phase encompasses the FIR filter tap coefficients used for pre-equalization—these are the parameters that adaptively control the shape and degree of pre-emphasis applied by the FIR filter. Ex-2020, ¶ 67. In particular, a POSITA reading Lugthart would understand that these coefficients are determined through the *adaptive* channel negotiation process, and thus there would be a need for storage of these constantly-changing coefficients in faster, temporary memory (i.e., volatile memory), which is much faster and more efficient than retrieving values from nonvolatile memory. *See id.*

Lugthart further describes its transceivers as having “adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization.” Ex-1004, 29:23-28. The term “self-adaptive” is significant: it indicates that the equalization system—including the pre-emphasis performed by the FIR filter—determines its own parameters automatically, without relying on externally supplied or pre-stored values. Again, this suggests that volatile memory solutions would be used, as opposed to the claimed nonvolatile memory. Ex-2020, ¶ 68.

Additionally, Lugthart teaches that the transceivers “adaptively acquire one or more parameters associated with the communication channel during a second stage of the channel negotiation subsequent to the first stage.” Ex-1004, 28:55-58. This “adaptive acquisition” of channel parameters occurs in real time during link establishment, confirming that Lugthart’s system is designed to determine its equalizer parameters dynamically rather than from stored values. Ex-2020, ¶ 69.

Nowhere in Lugthart’s detailed descriptions of FIR filter operation, DSP processing, channel negotiation, transceiver architecture, or equalizer configuration does the patent describe retrieving FIR coefficients from nonvolatile memory or storage of such coefficients in nonvolatile memory.

c) Petitioner’s suggested motivation to modify Lugthart provides an incomplete analysis

Petitioner, apparently aware of this deficiency, attempts to backfill the teachings of Lugthart with unsupported expert testimony. *See* Pet. at 37. But Dr. Chen’s analysis is incomplete and contradicts the core teaching of Lugthart. Dr. Chen argues that “POSITA would have recognized the need for these coefficient values to be stored so the cable operates as described by Lugthart,” and that “a POSITA would have found it obvious, based on Lugthart’s teachings, to use nonvolatile memory for storing these coefficients.” Ex-1003, ¶ 81; Pet at 37. Dr. Chen’s conclusion is based on impermissible hindsight reconstruction. The

claimed invention—an active cable with pre-equalization coefficients stored in nonvolatile memory—defines a specific design choice. The question under Ground 1 is not whether a POSITA *could have* chosen to store coefficients in nonvolatile memory, but whether Lugthart teaches or suggests doing so. It does not. *See* Ex-2020, ¶ 74.

Dr. Chen attempts to frame nonvolatile memory storage as “one of two possible solutions” (volatile vs. nonvolatile). Ex-1003, ¶ 87. But this framing ignores the third option that Lugthart actually teaches: adaptive determination of coefficients at runtime, where the coefficients reside in the DSP’s operational registers and are never separately “stored” in a persistent memory at all. In Lugthart’s system, coefficients are computed during the channel negotiation process and loaded directly into the FIR filter’s processing elements. There is no teaching or suggestion of a separate storage step in nonvolatile memory. Ex-2020, ¶ 75.

Dr. Chen asserts that storing the coefficients in nonvolatile memory was the “simplest, fastest, and most straightforward implementation of Lugthart’s teachings,” and that “[m]annual re-entry of the coefficients with each reconnection would be impractical.” Ex-1003, ¶¶ 80-81. Again, Dr. Chen ignores the description and purpose of Lugthart. Lugthart’s own specification provides the answer to how coefficients are configured at each connection: through adaptive channel

negotiation, not through manual re-entry or retrieval from nonvolatile memory. Dr. Chen's framing of the problem as a choice between "manual re-entry" and "nonvolatile storage" creates a false dichotomy that ignores Lugthart's actual teaching of adaptive determination. Ex-2020, ¶ 76. Accordingly, Lugthart fails to disclose, teach, or otherwise suggest all of the elements of independent claims 1, 8, and 15.

2. Petitioner provides no analysis with respect to dependent claims 6 and 13

Petitioner asserts that Ground 1 also challenges claims 6 and 13 (*see* Pet. at 16), but it does not. Petitioner's analysis fails to address claims 6 and 13, and Ground 1 provides no specific explanation of how or why claims 6 and 13 are allegedly obvious in view of Lugthart. *See generally*, Pet. Indeed, claim 6 depends from claim 4, which in turn depends from claim 3, and claim 13 depends from claim 11, which depends from claim 10. *See* Ex-1001 at cls. 3, 4, 6, 10, 11, and 13. Ground 1 fails to challenge any of these intermediate dependent claims or to explain how or why Lugthart allegedly teaches these intermediate dependent claims. Accordingly, Lugthart alone fails to disclose, teach, or otherwise suggest all of the elements of claims 6 and 13.

B. Ground 2: Petitioner has not shown that Lugthart should be combined with Gorecki or that the combination teaches claims 1-20

Ground 2 challenges all twenty claims of the '233 patent based on the combination of Lugthart and Gorecki. The Petition relies on Lugthart as the primary reference for the active cable architecture and on Gorecki, which relates to backplane communications rather than cables, to supply the teachings of storing “pre-programmed” or “pre-set” tap coefficient values for a transmitter FIR filter in nonvolatile memories such as “ROM, PROM, EPROM, [or] EEPROM.” Ex-1005, 7:18-26; Petition at 38. Ground 2 fails for two reasons. First, Petitioner fails to establish that a POSITA would have been motivated to selectively combine the features Petitioner cherry-picks from these two different references. Second, even if combined, Lugthart and Gorecki still fail to provide the full invention as claimed.

1. A POSITA would not have been motivated to combine Lugthart with Gorecki

At the outset, one of skill in the art would not have sought to combine Lugthart and Gorecki. Gorecki is directed to an entirely different type of communication system than Lugthart. Gorecki’s disclosure is expressly directed to equalization for backplanes. Ex-1005, 3:8-16. Every independent claim in Gorecki recites “a communications channel, wherein the communications channel includes

a backplane.” Ex-1005, Claims 1, 11, 22. The same is true of Gorecki’s disclosed embodiments, which are all directly applicable to backplanes. *See* Ex-1005, 3:8-45, 4:16-27, 4:53-64, 6:3-6, 8:1-8, Figs. 3-4. Gorecki does not describe, contemplate, or address the challenges unique to cable environments. This deficiency is important because the differences between backplanes and cables present fundamentally different engineering challenges and design constraints. Ex-2020, ¶¶ 80-81.

A backplane is a fixed, semi-permanent installation within an equipment enclosure—such as a server chassis or a switch—where the channel characteristics (trace lengths, impedance, loss profile) are both known and consistent. These channel characteristics are determined at the time of manufacture and remain substantially constant over the life of the equipment. Ex-2020, ¶ 81. In other words, Gorecki teaches that its pre-set coefficients are designed for a backplane environment in which the channel is fixed. Thus, Gorecki explains that these presets represent “compensation that is ideally the inverse of the effects caused by the communications channel.” Ex-1005, 9:3-15. In such an unchanging environment, it makes engineering sense to characterize the channel once, determine optimal equalization coefficients for that channel, and store them as “presets” for repeated use. *Id.*, 7:18-33; Ex-2020, ¶ 81.

By contrast, Ethernet cables typically face more dynamic channel characteristics. Lugthart's cable is a pluggable, portable device designed to be repeatedly connected to and disconnected from different host devices. Ex-1004, 14:14-15, 15:42-52. Each time the cable is connected, it interfaces with potentially different hosts, switches, or electronic devices, each presenting different signal characteristics, trace lengths on the host PCB, and connector properties. *Id.*, 15:42-52. The Lugthart equalizer must compensate for a channel that changes with each connection. *Id.* This is precisely why Lugthart teaches a comprehensive adaptive equalization system with multi-phase channel negotiation—an approach fundamentally at odds with Gorecki's pre-stored coefficient model. Ex-2020, ¶ 82.

The assertion from Petitioner and Dr. Chen that Gorecki is “analogous art” because it is “in the same field of endeavor (high-speed communications)” (Ex-1003, ¶ 45) oversimplifies the inquiry. Both references involve high-speed communications in a general sense, but their specific applications are materially different and present divergent design priorities. A POSITA developing an active cable would not look to backplane equalization techniques as a guide for coefficient management, including because the core design assumptions—fixed channel versus variable channel, permanent installation versus pluggable—diverge so fundamentally. Ex-2020, ¶ 83.

Furthermore, combining Gorecki with Lugthart would not work in practice. The combination Petitioner proposes would require grafting Gorecki's pre-stored coefficient approach onto Lugthart's adaptive equalization architecture. Dr. Chen and Petitioner simply presume that this combination would work without explaining how it would be accomplished or why a POSITA would have attempted it. Lugthart and Gorecki present opposite design philosophies, and a POSITA would recognize that combining them would be technically inappropriate.

Lugthart describes a multi-phase channel negotiation process in which transceiver parameters—including “operating parameters for the equalizers”—are adaptively determined at runtime. Ex-1004, 49:5-12. Lugthart's transceivers feature “self-adaptive digital equalization” (Ex-1004, 29:24-28) and are configured to “adaptively acquire one or more parameters associated with the communication channel during a second stage of the channel negotiation subsequent to the first stage.” Ex-1004, 4:54-58. Lugthart further describes “channel acquisition via filter adaptation” as a core capability of its link negotiation. Ex-1004, 47:42-45.

These descriptions make clear that in Lugthart's system, the FIR filter coefficients are *not* pre-stored values retrieved from nonvolatile memory; they are dynamically computed values derived through real-time interaction between the two transceivers at opposite ends of the cable and the hosts to which they are connected at any given time. Ex-2020, ¶ 86. The negotiation process proceeds

through three phases—a start-up phase, a full speed training phase, and a full functional training phase—completed within “a few milliseconds (e.g., within 5-6 milliseconds).” Ex-1004, 47:60-64. At each phase, equalizer parameters are progressively adapted and refined based on actual channel conditions. *Id.*, 47:65 – 49:37

Adding Gorecki’s pre-stored coefficients to this system would create an internal conflict. Gorecki’s approach assumes that the coefficients are determined in advance and loaded from nonvolatile memory at power-up. Lugthart takes a different approach and teaches away from Gorecki’s pre-stored coefficients. Instead, of using the same static coefficients that are preserved from one session to another, Lugthart provides a mechanism for dynamically determining coefficients after each power-up—through adaptive channel negotiation. A POSITA would recognize that Gorecki’s pre-stored coefficients would be immediately overwritten or rendered superfluous by Lugthart’s adaptive training process, making the combination functionally pointless. Ex-2020, ¶ 87. Accordingly, a POSITA would have no reason to combine Lugthart with Gorecki, rendering Ground 2 deficient at the outset.

**2. The Combination of Lugthart and Gorecki Does Not
Render the Challenged Claims Obvious**

a) Claims 1, 8, and 15

As discussed above, Lugthart alone does not disclose limitations [1f]/[8f]/[15c] (section VII.A), and there is no motivation to combine Lugthart with Gorecki (section VII.B.1). Accordingly, the combination of Lugthart and Gorecki does not disclose, teach, or otherwise suggest the teachings of independent claims 1, 8, or 15.

b) Claims 2, 9, and 16

In addition to the reasons stated above, Petitioner's analysis of claims 2, 9, and 16 demonstrates more fundamental deficiencies in the purported combination of Lugthart and Gorecki. Claims 2, 9, and 16 each require a *controller* that configures the DRR device "in response to a power-on event," including "retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring." Ex-1001, Claims 2, 9, 16. As with the pre-stored coefficients, Petitioner would graft Gorecki's controller into Lugthart's cable without explaining why or how a POSITA would do so. Gorecki teaches a "controller" that distributes coefficients "to the transmitter or set of transmitters" in the context of a backplane communication system. Ex-1005, 7:14-17. This architecture makes sense in Gorecki's environment, where multiple

transmitter/receiver pairs operate simultaneously across a shared backplane channel and where a centralized controller simplifies coordination. Ex-1005, 8:1-6, Fig. 3. But Lugthart’s cable already has self-contained transceivers at each end, each with its own pair of DSPs that independently handle transmit and receive functions, and each operates without need for a separate controller. Ex-1004, Figs. 1A, 4A-4B.

Transposing Gorecki’s controller into Lugthart’s architecture would require adding entirely new hardware—a controller at each end of the cable—that Lugthart never contemplates. Lugthart’s transceiver architecture is described as potentially a “monolithic device” that includes “integrated digital signal processors, ADCs and DACs.” Ex-1004, 41:14-16. Moreover, unlike the Gorecki backplane, Lugthart’s cable connectors are necessarily limited in both space and power, and adding a controller at each end would require more space and more power. In light of these competing concerns and limited resources, Petitioner does not explain why a POSITA would seek to add a separate controller to this already-integrated architecture, nor do they explain how this would be accomplished. Ex-2020, ¶¶ 96-97.

Moreover, the challenged claims require that the controller configure the DRR device specifically “in response to a power-on event,” including retrieving the pre-stored coefficients from nonvolatile memory. By contrast, Lugthart’s

startup sequence involves the transceivers performing their own adaptive channel negotiation to determine the coefficients in real time, which is the opposite of the claimed approach. Ex-1004, 47:24-51:30. Petitioner provides no explanation of how Gorecki's controller would interact with Lugthart's *existing* adaptive startup process, or why a POSITA would add a controller-based coefficient retrieval step to a system that already has a fully defined, self-sufficient startup sequence and adaptive coefficients. Ex-2020, ¶ 98. Accordingly, Petitioner has failed to demonstrate that the combination of Lugthart and Gorecki teaches claims 2, 9, or 16.

c) Claims 3, 10, and 17

Claims 3, 10, and 17 require that “the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.” Ex-1001, Claims 3, 10, 17.

For these claims, the Petition relies on Gorecki's teaching that “the transmitter *may* access the memory to retrieve” coefficient values “during startup/power-up.” Ex-1005, 7:18-33 (emphasis added); *see* Pet. at 44. But this Gorecki teaching is in the context of a backplane system where preset coefficients remain valid across power cycles because the channel does not change. Gorecki provides no teaching or suggestion that this approach would translate to cable applications, where preset coefficients may not remain valid across power cycles.

Nor is there any teaching in Lugthart why a cable should be “programmed” to load the same pre-stored coefficients “each time” power is supplied, particularly when the cable may be connected to a *different* host device at each power-on event (*i.e.*, the channel may change between power-on events). Ex-2020, ¶¶ 100-101. Again, Lugthart’s express teaching of adaptive coefficients that can be changed depending on channel characteristics teaches away from using the same pre-stored values each time Lugthart’s cable is powered up. *Id.* Petitioner has failed to demonstrate that the combination of Lugthart and Gorecki teaches claims 3, 10 or 17.

d) Claims 4, 6, 11, 13, and 18

Each of claims 4, 6, 11, 13, and 18 ultimately depend from one of claims 1, 8, or 15. Thus, for the same reasons discussed in Section VII.B.2.a), the combination of Lugthart and Gorecki fails to disclose, teach, or otherwise suggest dependent claims 4, 6, 11, 13, and 18.

e) Claims 5, 12, and 19

Claims 5, 12, and 19 require that “the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.” Ex-1001, Claims 5, 12, 19.

Petitioner attempts to extend Gorecki’s disclosure of pre-programmed or pre-set tap coefficients to the receive-side equalizer, arguing that it would have been “obvious to store the equalization coefficients values for the receiver in

nonvolatile memories as well.” *See* Pet. at 46-47; Ex-1003, ¶ 107. This extension compounds the deficiencies already identified. Neither Lugthart nor Gorecki teaches storing *receiver*-side equalization coefficients in nonvolatile memory. At best, Gorecki’s pre-stored coefficient teachings are directed to *transmitter*-side equalization circuitry. Ex-1005, 3:8-16, Abstract (“a *transmitter* having equalization circuitry” (emphasis added)). Extending Gorecki’s transmitter-side pre-programmed or pre-set tap coefficients to the receiver side requires an additional inferential step that is not supported by either reference. Ex-2020, ¶¶ 105-06.

f) Claims 7, 14, and 20

Claims 7, 14, and 20 require that “the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.” Ex-1001, Claims 7, 14, 20.

Here, Petitioner relies on Gorecki’s alleged teaching that “the ‘leading and/or trailing taps may be ‘turned off’ or disabled[.]’” Pet. at 49; Ex-1003, ¶¶ 110-111. Petitioner mischaracterizes Gorecki’s disclosure. Gorecki does not teach turning the taps off entirely, as Petitioner’s selective quote suggests. Read in its entirety, the relevant passage suggests swapping one set of taps for another. In particular, Gorecki describes that “a first path of the leading and/or trailing taps may be ‘turned off’ or disabled *and another leading and/or trailing tap path may*

be ‘turned on’ or enabled quite rapidly.” Ex-1005, 18:15-18 (emphasis added).

Looking beyond Petitioner’s selective quotation, it becomes clear that Gorecki actually teaches away from the claimed invention, suggesting that turning off the trailing/leading taps is a condition that should be avoided.

Nevertheless, even assuming that the disabling of the taps could be more than a momentary event, Dr. Chen’s conclusion that “[t]urning off the leading and trailing taps . . . is mathematically equivalent to performing no equalization.” (Ex-1003, ¶ 111) is incorrect. This argument conflates configuring a FIR filter *taps* to produce a null equalization effect with “not performing pre-equalization.” Claim 7 does not recite that the pre-equalization *taps* are set to zero; it recites that the DRR devices “do not perform pre-equalization” *at all* on the host-side data streams. A POSITA would understand that a system with an active FIR filter whose taps are configured to produce no net equalization effect is structurally different from a system that does not perform pre-equalization at all. Ex-2020, ¶ 110. In the former case, the equalization circuitry is still present, powered, and processing the signal—it has merely been configured to pass the signal through unmodified. *See* Ex-2021 at 39:9-40:3. In the latter case, the data stream bypasses equalization circuitry entirely. Ex-2020, ¶ 110. Accordingly, Petitioner has failed to demonstrate that the combination of Lugthart and Gorecki teaches claims 7, 14, or 20.

C. Ground 3: Petitioner has not shown that Cornelius or Samaan Should be Combined with Gorecki or that the Combination of Lugthart, Gorecki, and Samaan teaches claims 7, 14, or 20

Apparently recognizing the deficiencies of its Ground 2 combination as to claims 7, 14, and 20, Petitioner adds a third reference in Ground 3. Here, Petitioner challenges claims 7, 14, and 20 based on Lugthart and Gorecki in further view of Samaan. In particular, Petitioner alleges that Samaan discloses that the first and second DRR devices “do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.” Pet. at 49-50. As Petitioner did in Ground 2 with Gorecki, Petitioner again alleges that setting leading and trailing taps (*i.e.*, Samaan coefficients C_{-1} and C_{+1}) to zero is akin to not performing pre-equalization at all on the multi-lane data streams provided to the host interface ports. *See* Pet. at 49-50. Again, this argument conflates configuring a FIR filter *taps* to produce a null equalization effect with “not performing pre-equalization.” Claim 7 does not recite that the pre-equalization *taps* are set to zero; it recites that the DRR devices “do not perform pre-equalization” at all on the host-side data streams. Accordingly, for these same reasons discussed above in connection with Ground 2, the addition of Samaan does not fill the gap in prior art disclosure. Petitioner has failed to demonstrate that the combination of Lugthart, Gorecki, and Samaan teaches claims 7, 14, or 20.

D. Ground 4: Petitioner has not shown that Cornelius, Samaan or Gorecki teaches claims 1-20

Ground 4 largely parallels the arguments of Grounds 1 and 2, replacing Lugthart with Cornelius and adding Samaan as a third reference. As such, Ground 4 suffers from many of the same problems addressed above with respect to Grounds 1-2, as well as Ground 3. Petitioner has failed to explain why a POSITA—without relying on hindsight reconstruction—would have combined Gorecki with either Cornelius or Samaan to arrive at the claimed invention. And even if a POSITA had been motivated to combine these references, the resulting combination would still have lacked key features required by the claims.

1. Neither Cornelius Nor Samaan Teaches Storing Coefficient Values in Nonvolatile Memory

As a preliminary matter, Cornelius and Samaan share the same core deficiency as Lugthart—they do not teach storing transmit filter coefficient values in nonvolatile memory. This deficiency is critical because all claims share a common limitation that is not disclosed or rendered obvious by the combination: the requirement that the DRR devices provide pre-equalization “using transmit filter coefficient values stored in nonvolatile memories.” This limitation appears as [1f] in claim 1, [8f] in claim 8, and [15c] in claim 15. The remaining dependent claims all depend from one of claims 1, 8, or 15, and therefore inherit limitations [1f]/[8f]/[15c].

With respect to Cornelius, Petitioner relies on the statement that calibration parameters “may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation.” (Pet. at 85 (citing Ex-1006, 11:45-55)). Looking beyond Petitioner’s selective quotation reveals that Cornelius does not make this statement specifically as to equalization coefficients. Rather, it is a generic reference to calibration of various types of circuitry, including “circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry.” Ex-1006, 11:45-52.

Moreover, Cornelius never identifies *where* these “presets” would be stored, never uses the term “nonvolatile memory,” and never specifies any particular memory technology such as EEPROM, ROM, PROM, or flash. *See* Ex-1006, 11:45-62. Furthermore, Cornelius does not even link these generic calibration presets to transmit-side pre-equalization filter coefficient values. The Petition’s bare assertion that these presets “would obviously have been stored in nonvolatile memory (otherwise they would be lost)” (Pet. at 86) is an inferential leap that impermissibly relies upon hindsight bias. *See Metalcraft of Mayville, Inc. v. Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) (“[W]e cannot allow hindsight bias to be the thread that stitches together prior art patches into something that is the claimed invention.”).

Samaan likewise does not teach storing transmit filter coefficient values in nonvolatile memory. Similar to Lugthart, Samaan teaches that coefficients are determined dynamically through link training and adaptation protocols—not pre-stored in nonvolatile memory. For example, in the PCIe 3.0 context, Samaan explains that the host “picks its initial TxEQ setting to use...based on system knowledge of the channel lengths on the motherboard” during Phase 0 of the training protocol. Ex-1007, ¶ 84. Thereafter, both agents engage in Phases 2 and 3 to adaptively optimize TxEQ settings by requesting coefficient changes from each other. Ex-1007, ¶ 86. If anything, these link training and adaptation features suggest storage in volatile memory, which is typically used for short term storage, rather than more permanent nonvolatile memory. Ex-2020, ¶ 118. Accordingly, neither Cornelius nor Samaan teach all of the elements of independent claims 1, 8, or 15.

2. A POSITA Would Not Have Combined Gorecki with Cornelius or Samaan

Just as it attempted to do in Ground 2, Petitioner attempts to make up for the deficiencies in Cornelius and Samaan by cherry-picking features from Gorecki. For similar reasons to those described above, the Gorecki teachings Petitioner cites are incompatible with Cornelius and Samaan, which are directed to fundamentally different technologies and address different problems.

Gorecki is directed to equalization of high-speed signals in backplane environments—not active cables. Gorecki’s Abstract describes “a technique of and system for enhancing the performance of high-speed digital communications through a communications channel, for example a backplane.” Ex-1005, Abstract. Every embodiment in Gorecki is described in the context of backplane communications, where a transmitter is connected to a receiver over a passive communications channel such as a backplane trace. Ex-1005, 3:8-16, 6:3-9, Figs. 3-4. The claims of Gorecki expressly require that “the communications channel includes a backplane.” Ex-1005, Claims 1, 11, 22. Gorecki does not describe, contemplate, or suggest any application to active cables, and there is no disclosure in Gorecki of equalization circuitry housed within a cable connector or plug.

The operational context for Gorecki’s coefficient storage differs materially from the active cable context. In Gorecki, the coefficients may be “pre-programmed or pre-set” in memory including “ROM, PROM, EPROM, EEPROM or the like,” and the transmitter may “access the memory to retrieve the necessary information during start-up/power-up, initialization or re-initialization.” Ex-1005, 7:18-33. But this storage occurs in the context of a stationary backplane system where the transmitter is a fixed component of a host device. *Id.*, 3:8-16, 6:3-9, Figs. 3-4. The coefficients are tailored to a known, static backplane channel that does not change between power cycles. In contrast, an active cable is a removable

component that may be plugged into different host devices and different ports, encountering different channel characteristics each time. A POSITA would have recognized that pre-storing fixed coefficients in nonvolatile memory on a cable—as opposed to determining them dynamically through link training—would not have been an obvious design choice, because the cable-to-host channel characteristics may change each time the cable is plugged in. Ex-2020, ¶ 121.

Petitioner’s motivation to combine is conclusory and fails to account for the differences between these references. The Petition asserts that a POSITA would have applied Gorecki’s teachings because “all three references address high-speed communications, including for cables” and because storing data in nonvolatile memory was a “known technique.” Pet. at 88. But the fact that references share a general field does not, without more, supply a motivation to combine specific teachings from disparate technological contexts. *See Securus Techs., Inc. v. Glob. Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. 2017) (“a broad characterization of [prior art references as] falling within the same alleged field of [art] without more, is not enough for [petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion.”); *Markforged Inc. v. Continuous Composites, Inc.*, No. IPR2022-00679, 2023 WL 6534357, at *10 (P.T.A.B. Sept. 26, 2023) (“merely asserting that two references are drawn from the same field of art is ‘simply too conclusory’ to show that the skilled artisan would have combined

the references in the way of the claimed invention.”). Here, there is no articulated reason why a POSITA working on the HSIO/Thunderbolt active cable of Cornelius, with access to Samaan’s retimer primer for PCIe applications, would have looked to a backplane device for guidance on how to store filter coefficients in nonvolatile memory within an active cable connector. Ex-2020, ¶ 122. For these reasons, Ground 4 does not establish that limitations [1f], [8f], or [15c] would have been obvious.

3. The Combination of Cornelius, Samaan, and Gorecki does not teach the dependent claims of the ’233 Patent

With respect to the dependent claims, the Petition largely incorporates its analyses from Grounds 1-3, and Ground 4 fails for the same reasons addressed above (sections VII.A, VII.B, VII.C). Ground 4 also fails as to the dependent claims for the same reasons that it fails as to independent claims 1, 8, and 15 (sections VII.D.1, VII.D.2).

E. Grounds 1-4: Secondary Indicia of Non-obviousness Further Undermine Petitioner’s Challenges to the ’233 Patent

Secondary indicia of non-obviousness further show that it would not have been obvious at the time of the invention to selectively combine particular teachings from the cited references, as Petitioner urges. “Objective indicia of nonobviousness must be considered in every case where present.” *Apple Inc. v. Samsung Elecs. Co., Ltd.*, 839 F.3d 1034, 1048 (Fed. Cir. 2016). Here, Patent

Owner Credo Technology Group has licensed its AEC technology, including the '233 patent, to multiple manufacturers of active cables. *See* Ex-2022, Ex-2023, Ex-2024, Ex-2025, Ex-2026, Ex-2027. Licensing activity provides “strong probative value” when evaluating secondary considerations of non-obviousness. *See Institut Pasteur & Universite Pierre Et Marie Curie v. Focarino*, 738 F.3d 1337, 1347 (Fed. Cir. 2013). Accordingly, Petitioner’s challenges to the claims of the '233 Patent should be rejected.

VIII. CONCLUSION

For the reasons stated above, Patent Owner respectfully asks the Board to find that the challenged claims of the '233 Patent are not unpatentable.

Date: May 1, 2026

Respectfully submitted,

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**CERTIFICATE OF COMPLIANCE WITH
TYPE-VOLUME LIMITATIONS**

I, the undersigned, do hereby certify that the foregoing Patent Owner Response, including footnotes, contains 8,201 words, as measured by the Word Count function of Microsoft Word as specified by 37 C.F.R. § 42.24(b)(2).

/Charles M. McMahon/

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e)(4), I hereby certify that on May 1, 2026, a true and correct copy of the foregoing was served by electronic mail upon the following counsel of record for Petitioner:

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