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UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

March 27, 2025

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APPLICATION NUMBER: ***16/539,910***
FILING DATE: ***August 13, 2019***
PATENT NUMBER: ***11012252***
ISSUE DATE: ***May 18, 2021***

UNITED STATES PATENT AND TRADEMARK OFFICE · DEPARTMENT OF COMMERCE

Certified by

ACTING DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Yattung LAM
	Art Unit	
	Examiner Name	
	Attorney Docket Number	20160.0039.NPUS00

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	9,322,704	B1	2016-04-26	Neveux	
	2	7,401,985	B2	2008-07-22	Aronson, et al	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
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	First Named Inventor	Yattung LAM
	Art Unit	
	Examiner Name	
	Attorney Docket Number	20160.0039.NPUS00

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Rumer, B. "Fighting Jitter in Fibre-Channel Designs." Electronic Engineering Times, (2001, February 01). Retrieved August 13, 2019, from https://www.eetimes.com/document.asp?doc_id=1277249	
	2	IEEE P802.3cd/D1.2, 3rd February 2017 (Amendment of IEEE Std 802.3-2015 as amended) IEEE Draft Standard for Ethernet Amendment: Media Access Control Parameters for 50 Gb/s, 100 Gb/s and 200 Gb/s Operation. The Institute of Electrical and Electronics Engineers, Inc., 2017; S.l.: IEEE.	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Yattung LAM
	Art Unit	
	Examiner Name	
	Attorney Docket Number	20160.0039.NPUS00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Daniel J. Krueger/	Date (YYYY-MM-DD)	2019-08-13
Name/Print	Daniel J. Krueger	Registration Number	42,771

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/01 (06-12)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	ACTIVE ETHERNET CABLE

As the below named inventor, I hereby declare that:

This declaration is directed to:

[X] The attached application, or

[ ] United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Baohua CHEN Date (Optional) : _____

Signature: Baohua CHEN

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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As the below named inventor, I hereby declare that:

This declaration is directed to:

- [X] The attached application, or
- [ ] United States application or PCT international application number _____

  filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Yattung LAM Date (Optional) :_____

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

■ Practitioners associated with Customer Number: 63467

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

■ The address associated with Customer Number: 63467

OR

☐

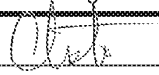
Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address: Credo Technology Group Limited, Ugland House, Grand Cayman Ky1-1104, Cayman Islands

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	2-9-2018
Name	Adam Thorngate-Gottlund	Telephone	408-664-9329 x127
Title	General Counsel		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Yattung LAM and Baohua CHEN

Application No./Patent No.: _____ Filed/Issue Date: _____

Titled: Active Ethernet Cable

Credo Technology Group Limited, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Daniel J . Krueger/	August 13, 2019
Signature	Date
Daniel J . Krueger	42,771
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Docket No.: 20160.0039.NPUS00

WORLDWIDE ASSIGNMENT

WHEREAS, I/WE (hereinafter referred to as the "ASSIGNOR(S)"):

Yattung LAM, c/o Credo Inc., 1600 Technology Drive, Fifth Floor, San Jose, CA 95110
Baohua CHEN, resident of Xiamen City, Fujian Province, China

has/have invented an **ACTIVE ETHERNET CABLE** ("Invention") for which one or more applications for patent, design registration, utility model registration, or other form of protection, rights, or title have been or will be made in certain countries ("Applications"), as further described below:

Patent Office or Country China
Application No. 201910155535.9
Date Filed March 1, 2019

AND WHEREAS, **CREDO TECHNOLOGY GROUP LIMITED**, (hereinafter referred to as the "ASSIGNEE"), a limited company organized under the laws of the Cayman Islands, having a place of business at Ugland House, Grand Cayman KY1-1104, is desirous of acquiring the full and exclusive right, title and interest in and to said Invention, said Applications inclusive of all ancillary rights relating thereto, any and all priority rights derived from said Applications, and all patents, design registrations, utility model registrations and other forms of protection, rights and titles relating to said Invention, in any country or countries and in respect of the whole or any part or parts of or improvements to the Invention;

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Yattung LAM
c/o Credo Inc.
1600 Technology Drive, Fifth Floor
San Jose, CA 95110

STATEMENT BY WITNESS

I, Ke Qin, whose full Post Office address is

Suite 309, Building One, 88 Chenhui Road, Zhangjiang High-Tech Park, Shanghai China.
(Address of Witness)

hereby declare that I was personally present and did see the above-named person, personally known to me to be a person named in the Worldwide Assignment, duly sign and execute same.

Date: 2019-02-27

Ke Qin
(Signature of Witness)

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IN WITNESS WHEREOF, this Worldwide Assignment has been executed below by the undersigned:

Date: Feb 27, 2019

Baohua CHEN

Baohua CHEN
resident of Xiamen City
Fujian Province, China

STATEMENT BY WITNESS

I, Ke Qin, whose full Post Office address is

Suite 308, Building one, 88 Chenhui Road, Zhangjiang High-Tech Park - Shanghai - China
(Address of Witness)

hereby declare that I was personally present and did see the above-named person, personally known to me to be a person named in the Worldwide Assignment, duly sign and execute same.

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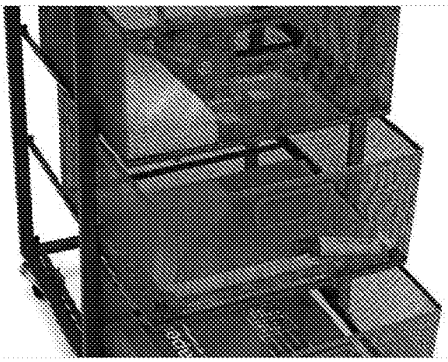
Fighting Jitter in Fibre-Channel Designs

Fighting Jitter in Fibre-Channel Designs

By **Bob Rumer** , 02.01.01 0

Routing multiple serial signals can be a daunting task during the development of fibre channel systems. Fortunately, digitalrepeaters and retimer ICs can clean up signals and counteract jitter in order to ensure spec compliance.

Storage area networking (SAN) and network attached storage (NAS) have garnered a great deal of attention in the communication market as the demand for sophisticated e-commerce and mission-critical systems has exploded over the past year. Estimates of future growth optimistically point to widespread deployment of these systems to distribute databases, Web pages, streaming video, and movies-on-demand.

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A chief concern of designers of SAN and NAS equipment is, of course, fast access to files. Merely locating audio clips, video clips, and large databases is not enough; fast access and loading of the data is critical. To this end, fibre channel has emerged as a fast and reliable method for making SAN and NAS equipment a reality.

Fibre channel uses high-speed serial links at either 1.0625- or 2.125-Gbps data rates to link servers, switches, routers, disk arrays, tape systems, and RAID controllers into complex, redundantly interconnected networks which allow user access to data in the presence of component failures. Fibre channel-derived SAN architectures are now being deployed in increasingly complex and creative ways to solve serious data availability issues which, to-date, have been unsolvable. Designers implementing these systems must ensure physical layer interoperability in order to reliably deliver future scaleability to users.

Unfortunately, designing robust gigabit speed serial links is typically viewed as a black art beyond the skill of most system architects. The most challenging area is jitter, which can adversely affect the reliability of data transfer through the link. As you'll see, repeaters and retimers can be used to mitigate these difficulties and, with care, provide signals that comply with all jitter-related industry specifications. To better illustrate the impact of repeaters and retimers, let's start with a more detailed look at the physical layer of fibre channel links.

Speeding the connection

At the transmit source of a fibre channel architecture, 8 b of raw data are encoded into a 10-b character using the 8B/10B encoding scheme. This encoding scheme provides the encoded data with several critical properties of value in serial data communications. 10-b data is serialized and transmitted through a high-speed, differential output buffer, onto copper cable or into an optical transceiver for conversion to light. This is done with an output buffer that uses either positive emitter coupled logic (PECL) or current mode logic (CML).

At the other end of the fibre channel link, high-speed differential data from the copper cable or output of an optical transceiver is input to a high-speed, differential input buffer that drives a clock and data recovery (CDR) unit. This CDR extracts a bit-rate clock from the serial data, samples the data, then deserializes and decodes it into 8-

b raw data. The deserializer aligns the recovered serial data to the 8-b parallel bus and uses a distinct 7-b comma character (0011111) in the serial stream to identify alignment boundaries. This parallel data is then pro-cessed by higher-level functions.

The 8B/10B encoding aids serial communications by conditioning the transmitted signal in order to ease the receiver implementation. 8B/10B encodes raw data into a 10-b character, which has guaranteed edge density (30% on average) and limited run length (5 b maximum) making the CDR easier to design. Furthermore, 8B/10B also ensures that DC balance is maintained on the copper cable so that the receiver does not see a DC shift at its input. Due to the 8B/10B encoding, links may be AC coupled in order to provide implementation flexibility between vendors at each end of the link.

In most serial protocols, there is an assumption that the transmitting system and receiving system are asynchronous to each other. In fibre channel, each side of the link is normally implemented using oscillators with plus/minus 100 parts per million (PPM) frequency tolerance so that the receiver sees potentially up to plus/minus 200 PPM between the baud rate of the incoming data and that of its local reference clock. All circuit functions that recover data, either serially or in parallel, must accommodate this frequency offset.

All that jitter

By the time the serial signal reaches a receiver, various forms of jitter may have been added to the signal, making reliable, error-free data recovery difficult. Jitter is the displacement of a signal's edge from its ideal location and may be caused by numerous factors. Random jitter is unbounded Gaussian jitter (caused primarily by thermal noise) which is generated in clock multiplier units (CMUs) in transmitters and in optical transceivers.

Due to the presence of random jitter, links are specified for a given bit error rate (BER),which is usually better than 10-12. At 1.0625- Gbps fibre channel rates, this allows a single bit error approximately every 15 minutes. Actual systems perform much better than industry specifications but reliable data communication products assume a worst-case BER and implement reliable recovery mechanisms that result in error-free transmission.

Another consideration is deterministic jitter, timing distortions and irregularities caused by circuit effects in the transmission system. The disturbance is generated by numerous mechanisms in links but is bounded so that a receiver can reliably accommodate deterministic jitter, if under a certain threshold. Most deterministic jitter is generated by the bandwidth limitations of the transmission system and results in data-dependent variations in signal.

In the real world, some pretty awful signals are input to systems and must be reliably recovered by the receiver. In general, receivers are implemented with a CDR that is phase-locked loop (PLL) based. The PLLs in these systems generally feature loop bandwidths in the MHz range, providing decent jitter tolerance. If jitter is considered as a sinusoidal variation in the location of signal edges, then the frequency of jitter refers to the rate at which the edge moves relative to its ideal position. The amplitude of jitter refers to the amount of absolute movement from ideal.

The CDR's PLL can reliably recover sinusoidal jittered serial data that has jitter below a certain amplitude threshold. This threshold amplitude varies with the frequency of jitter. Jitter below the loop bandwidth of the PLL is trackable, while jitter above the loop bandwidth is not. As a rule, the higher the receiver's loop bandwidth, the higher the jitter tolerance.

Complex serial systems

While a typical point-to-point connection addresses the needs of some system integrators, much more useful systems can be built using hubs, switches, and other serial routing functions to connect, steer, and replicate serial signals. Duplex links between systems would then route through more circuitous paths to connect end-user nodes but would provide more flexibility and robustness than point-to-point connections.

One of the more complex subsystems in fibre channel is the just-a-bunch-of-disks (JBOD) disk array. In this array, incoming serial data is routed to all functional drives, isolated from all non-functional drives, and then routed back to the source of data.

Figure 1 < https://m.eet.com/media/1095877/0201fibre1.gif> shows a typical fibre channel arbitrated loop (FC-AL) JBOD. Each drive has two fibre channel links for redundant access in high-availability systems. Two independent sets of circuits are used to connect the incoming serial data (on loop A or loop B) to the disk drives. Repeaters and retimers are used at the incoming and outgoing ports of the system to clean up signals in each direction.

Port bypass circuits (PBCs) are also included in the fibre channel architecture highlighted in **Figure 1 < https://m.eet.com/media/1095877/0201fibre1.gif>**. These circuits serve as high-speed serial multiplexers that steer gigabit signals to the drives.

When combined together, the repeaters, retimers, and PBCs form a virtual FC-AL that includes all functional drives and isolates all non-functional drives. Intermediate repeaters may be required, depending on the size and complexity of the system.

A repeat performance

In this article, the term "repeater" will be used for a CDR circuit where the recovered serial data is retransmitted synchronously to the recovered clock. Repeaters are used to receive and retransmit serial data and, in the process, clean up the signal. Repeaters are not protocol-addressable entities but are considered part of the interconnect. (Please note that in alternate technologies, such as Ethernet, other terms may be used for this function).

In a typical repeater block diagram, serial input data is sent to the repeater PLL and CDR sampling flip-flop (see **Figure 2 < https://m.eet.com/media/1095878/0201fibre2.gif>**). The PLL lines up a 1.0625- or 2.125-GHz clock synchronously to the rising and falling edges of input data as well as a clock 180¼ out of phase with the recovered clock used to resample the data in the flip-flop.

Resampled data is then retransmitted through the output buffer. Some implementations require an external control input, LOCK2REF, which forces the repeater to lock to a local reference clock when not locking on data. Other repeaters do not need a LOCK2REF input or a reference clock.

The repeater is simple, requires fairly low power, and features low latency through the device (usually several bit times). However, jitter below the loop bandwidth of the CDR PLL will be retransmitted without any jitter attenuation. Any jitter above the loop bandwidth of the PLL is attenuated aggressively.

Traditionally, analog repeaters have been employed in fibre channel architectures. However, modern, application-specific, digital repeaters are gaining popularity due to their superior performance. Digital repeaters offer outstanding jitter tolerance, which is the ability of the receiver to reliably recover the data error-free, as well as low jitter transfer, which measures how much of the jitter at the input signal is transferred to the output.

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In general, the higher the loop bandwidth of the receiver, the better the jitter tolerance and the worse the jitter transfer. Typically, one-stage analog repeaters are forced to compromise between high loop bandwidth (resulting in good jitter tolerance but poor jitter transfer) or low loop bandwidth (poor jitter tolerance but good jitter transfer).

Analog vs. digital

Figure 3 < https://m.eet.com/media/1095879/0201fibre3.gif> shows the jitter transfer of an analog and a digital repeater. The X-axis is the frequency of jitter. The Y-axis is the ratio of jitter output versus jitter input measured in dB. The jitter-transfer curve shown in Figure 3 < https://m.eet.com/media/1095879/0201fibre3.gif> for an analog repeater shows high loop bandwidth (~15 MHz) where the loop bandwidth is measured at the -3-dB transfer point.

Any jitter below the loop bandwidth is transferred from the input to the output unattenuated. Furthermore, many analog repeaters exhibit jitter peaking where the input jitter actually excites a higher jitter at the output. In general, this is less than 1 dB, but it does limit the number of repeaters that can be cascaded in real-world systems.

A digital repeater offers several benefits. First, it operates identically over process, voltage, and temperature. A two-stage digital repeater implements a first-stage CDR with high loop bandwidth (approximately 4 MHz) in order to have good jitter tolerance. The second stage features very low loop bandwidth (approximately 75 kHz) in order to minimize the amount of jitter transferred to downstream devices. Also, since they do not peak, they can be cascaded without worry. When these features are combined, this repeater provides good jitter tolerance and good jitter transfer in a non-peaking design.

Retimers

The term "retimer" is used for a CDR that retransmits the recovered serial data synchronously to a local reference clock. This complex retimer function eliminates jitter transfer at the expense of latency.

Due to the potential mismatch between the baud rate of the incoming data and the local reference clock (approximately plus/minus 200 PPM), an add/ drop first in first out (FIFO) is required to insert or delete 40-b ordered sets known as "fill words" to accommodate this rate difference. By eliminating jitter transfer, signal-quality standards compliance is ensured. A block diagram of a typical retimer includes a digital receiver, the add/drop FIFO scheduler, and an output flip-flop for retransmission (see Figure 4 < https://m.eet.com/media/1095880/0201fibre4.gif>).

Data that is added or dropped must be anticipated by the protocol level, in this case fibre channel, which must provide for addable and droppable protocol entities. Since fibre channel was conceived with the idea of complex data paths, retimers were considered at the early stages of protocol development. For example, a transmitting source for fibre channel frames must place at least six idle ordered sets between each frame. At the receiving end, at least two idle ordered sets must be present. This allows intermediated devices to drop a maximum of four idle ordered sets.

Since data in the add/drop FIFO is taken out of the FIFO with a locally-generated reference clock, the jitter at the output will depend on the output stage of the repeater and the internally generated bit-rate clock, but not on the input serial data.

A price is paid for the additional complexity involved in retimers. Obviously, power increases, but more importantly, there is a latency penalty on the order of several hundred bit times due to the FIFO. The efficiency of a network is proportional to the latency of each path. Therefore, the increased latency in the retimer reduces network efficiently.

Which to use?

As a general rule, designers of complex systems should use retimers at the output of their

systems or at any node that customers might view a data eye. This ensures that the customer only sees specification-compliant data eyes at the output of retimers. By using repeaters elsewhere, the latency penalty associated with retimers is avoided and network efficiency is optimized. Although repeaters may transfer some low frequency jitter from the input to the outputs, this frequency is low enough that downstream receivers will reliably recover the data without error.

The basic functions of a fibre channel repeater or retimer can be used in other protocols such as Gigabit Ethernet and Infiniband. In Ethernet, a repeater is equivalent to a fibre channel retimer - an unfortunate naming snafu. Unlike fibre channel, Gigabit Ethernet is dominated by point-to-point links between network interface cards (NICs) and switches.

Ethernet repeaters are used between two subnets in the same collision domain and are most commonly called upon to translate from one media type to another. Consequently, an Ethernet repeater is more complicated than a fibre channel retimer since multiple physical layer protocols must be supported and management is almost always mandatory.

In Infiniband, these functions are addressed by a "retiming repeater," and each link is allowed to contain no more than two retiming repeaters. This function is equivalent to a fibre channel retimer. In order to accommodate frequency offsets between the incoming data and the local transmit clock, retiming repeaters are allowed to add or drop skip symbols (a special 10-b word) within the skip ordered set (initially a 40-b entity) which starts with a K28.5 character. Since Infiniband consists of 1x, 4x, or 12x wide links, the retiming repeater may be designed to perform lane-to-lane deskew as well.

The equivalents of fibre channel repeaters have been used in either Ethernet or Infiniband, although nothing in the specifications preclude their use.

About the Author

Bob Rumer *is the vice president of Storage Communications at Vitesse Semiconductor Corp. Prior to Vitesse, Rumer held engineering positions at Tandon Corp., Philips Ultrasound, and Beckman Instruments. Rumer received his MSEE from the University of California at Berkeley and can be reached at* ***rumer@vitesse.com****.*

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Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	ACTIVE ETHERNET CABLE
First Named Inventor/Applicant Name:	Yattung LAM
Filer:	Daniel Joseph Krueger/Theresa Evenbly
Attorney Docket Number:	20160.0039.NPUS00

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Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
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UTILITY SEARCH FEE	2111	1	330	330
UTILITY EXAMINATION FEE	2311	1	380	380
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	20160.0039.NPUS00
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Title of Invention	ACTIVE ETHERNET CABLE	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	20160.0039.NPUS00
	Application Number	
Title of Invention	ACTIVE ETHERNET CABLE	

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

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Application Information:

Title of the Invention	ACTIVE ETHERNET CABLE		
Attorney Docket Number	20160.0039.NPUS00	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	**Suggested Figure for Publication (if any)**	2

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
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Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)

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Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201910155535.9	CN	2019-03-01	

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Title of Invention	ACTIVE ETHERNET CABLE	

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Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	CREDO TECHNOLOGY GROUP LIMITED		
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Phone Number		Fax Number	
Email Address			

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Assignee Information including Non-Applicant Assignee Information:

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Organization Name	CREDO TECHNOLOGY GROUP LIMITED

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	Ugland House		
Address 2			
City	Grand Cayman	**State/Province**	
Country i	KY	Postal Code	KY1-1104
Phone Number		Fax Number	
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Signature	/Daniel J. Krueger/			Date (YYYY-MM-DD)	2019-08-13
First Name	Daniel J.	Last Name	Krueger	Registration Number	42771

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ACTIVE ETHERNET CABLE

BACKGROUND

[0001] The Institute of Electrical and Electronics Engineers (IEEE) Standards Association publishes an IEEE Standard for Ethernet, IEEE Std 802.3-2015, which will be familiar to those of ordinary skill in the art to which this application pertains. This Ethernet standard provides a common media access control specification for local area network (LAN) operations at selected speeds from 1 Mb/s to 100 Gb/s over coaxial cable, twinaxial cable, twisted wire pair cable, fiber optic cable, and electrical backplanes, with various channel signal constellations. As demand continues for ever-higher data rates, the standard is being extended. Such extensions to the standard must account for increased channel attenuation and dispersion even as the equalizers are forced to operate at faster symbol rates. It is becoming increasingly difficult to provide affordable, mass-manufactured network hardware that assures consistently robust performance as the proposed per-lane bit rates rise beyond 50 Gbps with PAM4 or larger signal constellations.

SUMMARY

[0002] Accordingly, there are disclosed herein architectures and communication methods that enable mass-manufactured cables to perform robustly at per-lane PAM4 symbol rates up to 26.5625 GBd and beyond. One illustrative cable embodiment includes electrical conductors connected between a first connector and a second connector. The first and second connectors are each adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable, and to provide to that host device an electrical output signal conveying an outbound

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data stream from the cable. The first and second connectors each include a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream.

[0003] One illustrative communication method embodiment includes, in a network cable having conductor pairs connecting a first connector to a second connector: receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device; performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream; re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs; receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device; performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream; and re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs.

[0004] One illustrative cable manufacturing method includes: connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver; packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network

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interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device, the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams.

[0005] Each of the foregoing embodiments may be implemented individually or in combination, and may be implemented with one or more of the following features in any suitable combination: 1. the respective transceiver for each of the first and second connectors performs clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable. 2. the respective transceivers each employ fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal. 3. the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal. 4. the cable-dependent equalization parameters are adapted during usage of the cable. 5. said cable-dependent equalization parameters are fixed during normal usage of the cable. 6. said cable-dependent equalization parameters are determined during manufacturer-testing of the cable.

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7. the inbound data stream and the outbound data stream each have a per-lane bit rate of 50 Gbps or more. 8. performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream; and performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream. 9. re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device; and re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device. 10. said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters. 11. cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said performing clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical transit signal. 12. determining said cable-dependent equalization parameters during manufacturer-testing of the network cable. 13. the first and second transceivers are configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable. 14. the first and second transceivers are each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical

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output signals. 15. the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals. 16. the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation. 17. the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation. 18. testing an assembled cable to determine the cable-dependent equalization parameters.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Fig. 1 is a perspective view of an illustrative active Ethernet cable.

[0007] Fig. 2 is a function-block diagram of the illustrative cable.

[0008] Fig. 3 is an architectural diagram for a communications link including the illustrative cable.

[0009] Fig. 4 is a block diagram of a receiver in an illustrative multi-lane transceiver.

[0010] Fig. 5 is a block diagram of a transmitter in an illustrative multi-lane transceiver.

[0011] Fig. 6 is a flow diagram of an illustrative cable manufacturing method.

[0012] Fig. 7 is a perspective view of an illustrative active 1:4 breakout cable.

[0013] Fig. 8 is a function-block diagram of the illustrative 1:4 breakout cable.

DETAILED DESCRIPTION

[0014] While specific embodiments are given in the drawings and the following description, keep in mind that they do not limit the disclosure. On the contrary, they provide the foundation for one of ordinary skill to discern the alternative

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forms, equivalents, and modifications that are encompassed in the scope of the appended claims.

[0015] Fig. 1 is a perspective view of an illustrative cable that may be used to provide a high-bandwidth communications link between devices in a routing network. The routing network may be or include, for example, the Internet, a wide area network, or a local area network. The linked devices may be computers, switches, routers, and the like. The cable includes a first connector 102 and a second connector 104 that are electrically connected via a cord 106. The cord 106 includes electrically conductive wires usually in a paired form such as with twinaxial conductors. Twinaxial conductors can be likened to coaxial conductors, but with two inner conductors instead of one. The inner conductors may be driven with a differential signal and their shared shield operates to reduce crosstalk with other twinaxial conductors in the cable. Depending on the performance criteria, it may be possible to employ other paired or single-ended conductor implementations.

[0016] Pursuant to the Ethernet standard, each conductor pair may provide unidirectional transport of a differential signal. To enable robust performance over even extended cable lengths (greater than, say, 3 m, 6 m, or 9 m), each connector 102, 104 may include a powered transceiver that performs clock and data recovery (CDR) and re-modulation of data streams in each direction. Notably, the transceivers perform CDR and re-modulation not only of the outbound data streams as they exit the cable, but also of the inbound data streams as they enter the cable.

[0017] It is acknowledged here that the inbound data streams may be expected to be compliant with the relevant standard and may be expected to have experienced essentially no deterioration from their traversal of the network interface port's

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receptacle pins and the cable assembly's connector plug pins. Nevertheless, the modulation quality and equalization strategy employed by the electronics manufacturer of the transmitting network interface is generally unknown and the minimum requirements of the standard may be inadequate for transport over an extended cable length, particularly if the electronics manufacturer of the receiving network interface is different than that of the transmitting network interface. As with the transmitting network interface, the equalization and demodulation strategy employed by the electronics manufacturer of the receiving network interface is generally unknown and may be unable to cope with the attenuation and interference caused by signal transport over an extended cable length. By performing CDR and re-modulation of both inbound and outbound data streams, the illustrative cable enables consistently robust data transfer over extended cable lengths can be assured without consideration of the electronics manufacturers of the network interfaces.

[0018] Fig. 2 is a function-block diagram of the illustrative cable of Fig. 1. Connector 102 includes a plug 202 adapted to fit a standard-compliant Ethernet port in a first host device 302 (Fig. 3) to receive an inbound data stream as an electrical input signal from the host device and to provide an outbound data stream as an electrical output signal to the host device. Similarly, connector 104 includes a plug 204 that fits an Ethernet port of a second host device 304. Connector 102 includes a first transceiver 206 to perform CDR and re-modulation of the data streams entering and exiting the cable at connector 102, and connector 104 includes a second transceiver 208 to perform CDR and re-modulation of the data streams entering and exiting the cable at connector 104. The transceivers 206, 208 may be integrated circuits mounted on a printed circuit board and connected to plug pins via circuit

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board traces. The wires of cord 106 may be soldered to corresponding pads on the printed circuit board.

[0019] Each transceiver 206, 208, includes a set 210 of transmitters and receivers for communicating with the host device and a set 212 of transmitters and receivers for sending and receiving via conductor pairs running the length of the cable. The illustrated cable supports four bidirectional communication lanes LN0-LN3, each bidirectional lane formed by two unidirectional connections, each unidirectional connection having a differentially-driven twinaxial conductor pair (with a shield conductor not shown here). The transceivers optionally include a memory 214 to provide first-in first-out (FIFO) buffering between the transmitter & receiver sets 210, 212. A controller 216 coordinates the operation of the transmitters and receivers by, e.g., setting initial equalization parameters and ensuring the training phase is complete across all lanes and links before enabling the transmitters and receiver to enter the data transfer phase.

[0020] In at least some contemplated embodiments, the host-facing transmitter and receiver set 210 employ fixed equalization parameters that are cable-independent, i.e., they are not customized on a cable-by-cable basis. The center-facing transmitter and receiver set 212 preferably employ cable-dependent equalization parameters that are customized on a cable-by-cable basis. The cable-dependent equalization parameters may be adaptive or fixed, and initial values for these parameters may be determined during manufacturer tests of the cable. The equalization parameters may include filter coefficient values for pre-equalizer filters in the transmitters, and gain and filter coefficient values for the receivers.

[0021] The illustrative cable of Fig. 2 may be a part of a point-to-point communications link between two host devices 302, 304 as shown in the

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architectural diagram of Fig. 3. Fig. 3 shows the architecture using the ISO/IEC Model for Open Systems Interconnection (See ISO/IEC 7498-1:1994.1) for communications over a physical medium such as the twinaxial conductor pairs represented by channels 306. The interconnection reference model employs a hierarchy of layers with defined functions and interfaces to facilitate the design and implementation of compatible systems by different teams or vendors. While it is not a requirement, it is expected that the higher layers in the hierarchy will be implemented primarily by software or firmware operating on programmable processors while the lower layers may be implemented as application-specific hardware.

[0022] The Application Layer 308 is the uppermost layer in the model, and it represents the user applications or other software operating on different systems that need a facility for communicating messages or data. The Presentation Layer 310 provides such applications with a set of application programming interfaces (APIs) that provide formal syntax along with services for data transformations (e.g., compression), establishing communication sessions, connectionless communication mode, and negotiation to enable the application software to identify the available service options and select therefrom. The Session Layer 312 provides services for coordinating data exchange including: session synchronization, token management, full- or half-duplex mode implementation, and establishing, managing, and releasing a session connection. In connectionless mode, the Session Layer may merely map between session addresses and transport addresses.

[0023] The Transport Layer 314 provides services for multiplexing, end-to-end sequence control, error detection, segmenting, blocking, concatenation, flow control on individual connections (including suspend/resume), and implementing

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end-to-end service quality specifications. The focus of the Transport Layer 314 is end-to-end performance/behavior. The Network Layer 316 provides a routing service, determining the links used to make the end-to-end connection and when necessary acting as a relay service to couple together such links. The Data link layer 318 serves as the interface to physical connections, providing delimiting, synchronization, sequence and flow control across the physical connection. It may also detect and optionally correct errors that occur across the physical connection. The Physical layer 322 provides the mechanical, electrical, functional, and procedural means to activate, maintain, and deactivate channels 306, and to use the channels 306 for transmission of bits across the physical media.

[0024] The Data Link Layer 318 and Physical Layer 322 are subdivided and modified slightly by IEEE Std 802.3-2015, which provides a Media Access Control (MAC) Sublayer 320 in the Data Link Layer 318 to define the interface with the Physical Layer 322, including a frame structure and transfer syntax. Within the Physical Layer 322, the standard provides a variety of possible subdivisions such as the one illustrated in Fig. 3, which includes an optional Reconciliation Sublayer 324, a Physical Coding Sublayer (PCS) 326, a Forward Error Correction (FEC) Sublayer 328, a Physical Media Attachment (PMA) Sublayer 330, a Physical Medium Dependent (PMD) Sublayer 332, and an Auto-Negotiation (AN) Sublayer 334.

[0025] The optional Reconciliation Sublayer 324 merely maps between interfaces defined for the MAC Sublayer 320 and the PCS Sublayer 326. The PCS Sublayer 326 provides scrambling/descrambling, data encoding/decoding (with a transmission code that enables clock recovery and bit error detection), block and symbol redistribution, PCS alignment marker insertion/removal, and block-level lane synchronization and deskew. To enable bit error rate estimation by components of

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the Physical Layer 322, the PCS alignment markers typically include Bit-Interleaved-Parity (BIP) values derived from the preceding bits in the lane up to and including the preceding PCS alignment marker.

[0026] The FEC Sublayer 328 provides, e.g., Reed-Solomon coding/decoding that distributes data blocks with controlled redundancy across the lanes to enable error correction. In some embodiments (e.g., in accordance with Article 91 or proposed Article 134 for the IEEE Std 802.3), the FEC Sublayer 328 modifies the number of lanes (Article 91 provides for a 20-to-4 lane conversion).

[0027] The PMA Sublayer 330 provides lane remapping, symbol encoding/decoding, framing, and octet/symbol synchronization. The PMD Sublayer 332 specifies the transceiver conversions between transmitted/received channel signals and the corresponding bit (or digital symbol) streams. An optional AN Sublayer 334 is shown as a internal element of the PMD Sublayer 332, and it implements an initial start-up of the communications channels, conducting an auto-negotiation phase and a link-training phase before entering a normal operating phase. The auto-negotiation phase enables the end nodes to exchange information about their capabilities, and the training phase enables the end nodes to adapt both transmit-side and receive-side equalization filters in a fashion that combats the channel non-idealities. A receptacle 336 is also shown as part of the PMD sublayer 332 to represent the physical network interface port.

[0028] The connectors 102, 104, have plugs 202, 204 that mate with the receptacles 336 of the two host devices 302, 304. Within each connector, the transceivers may implement a host-facing Physical Layer 322A, a center-facing Physical Layer 322B, and a Data Link Layer 340 that bridges together the two Physical Layers. More information regarding the operation of the sublayers, as well as the electrical and

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physical specifications of the connections between the nodes and the communications medium (e.g., pin layouts, line impedances, signal voltages & timing), and the electrical and physical specifications for the communications medium itself (e.g., conductor arrangements in copper cable, limitations on attenuation, propagation delay, signal skew), can be found in the current Ethernet standard, and any such details should be considered to be well within the knowledge of those having ordinary skill in the art.

[0029] The MAC, Reconciliation, PCS, FEC, PMA, and PMD Sublayers, may be implemented as application-specific integrated circuitry to enable high-rate processing and data transmission. The receiver and transmitter sets 210, 212, may implement the PMA and PMD sublayers. Figs. 4 and 5 are block diagrams of an illustrative receiver and an illustrative transmitter that may be part of the sets 210, 212.

[0030] In Fig. 4, receiver 400 receives an analog electrical signal (CH_IN) and supplies it to a low noise amplifier (LNA) 402. The LNA 402 provides a high input impedance to minimize channel loading and amplifies the received electrical signal to drive the input of a continuous time linear equalizer (CTLE) filter 404. CTLE 404 provides continuous time filtering to shape the signal spectrum to reduce the length of the channel impulse response while minimizing leading inter-symbol interference (ISI). A decision feedback equalizer (DFE) 406 operates on the filtered signal to correct for trailing ISI and detect each transmitted channel bit or symbol, thereby producing a demodulated digital data stream. Some embodiments employ oversampling. A clock and data recovery (CDR) circuit 408 extracts a clock signal from the filtered signal and/or the digital data stream and supplies it to DFE 406 to control sample and symbol detection timing. A serial-to-parallel circuit 410 groups

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the digital data stream bits or symbols into blocks to enable the use of lower clock rates for subsequent on-chip operations. The symbols or data blocks are placed on the digital receive bus (RXD) for retransmission to the remote end node by a transmitter.

[0031] While certain contemplated cable embodiments do not support auto-negotiation, other contemplated embodiments do support auto-negotiation in accordance with the Ethernet standard. When supported, the auto-negotiation may be implemented as described in PCT/CN2017/075961, titled "Ethernet link extension method and device" by inventors Yifei Dai, Haoli Qian, and Jeff Twombly, and filed 2017-03-08. A detector or packet information extractor 442 monitors the receive signal for the end of the auto-negotiation phase and/or the beginning of the training phase frames.

[0032] During the training phase, a filter adaptation circuit 440 measures an error between the input and output of a decision element in DFE 406, employing that error in accordance with well-known techniques from the literature on adaptive filtering to determine adjustments for the coefficients in CTLE filter 404, DFE 406, and a transmit filter 506 (discussed further below), and to determine whether convergence has been achieved. The locally-generated information (LOCAL_INFO) including the transmit filter coefficient adjustments and the convergence status are provided to the local transmitter 500 that communicates in the reverse direction on the data lane. As discussed below, the local transmitter communicates the transmit filter adjustments and the convergence status via a back-channel to the source of the CH_IN signal. In that vein, the received signal includes back-channel information *from* the source of the CH_IN signal. A packet information extractor 442 detects the back-channel information (BACK_INFO) and passes it to the local

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transmitter. Once convergence is achieved, receiver 400 is ready to begin normal operations.

[0033] In Fig. 5, transmitter 500 receives blocks of channel bits or symbols for transmission to the source of the CH_IN signal (Fig. 4). During normal operations, multiplexer 502 supplies blocks of channel bits or symbols from the remote source (received on the TXD bus) to the parallel to serial (P2S) circuit 504. P2S circuit converts the blocks into a digital data stream. A transmit filter 506, also called a pre-emphasis filter, converts the digital data stream into an analog electrical signal with spectral shaping to combat channel degradation. Driver 508 amplifies the analog electrical signal to drive the channel output (CH_OUT) node.

[0034] If supported, the auto-negotiation phase may be implemented as set forth in Y.Dai et al. During the training phase, multiplexer 502 obstructs information from the TXD bus, instead supplying P2S circuit 504 with training frames from a training controller 540. The training controller 540 generates the training frames based on the convergence status and transmit filter coefficient adjustments (LOCAL_INFO) received from the local receiver 400. That is, in addition to training patterns, the training frames include backchannel information to be used by the remote end of the channel. Note that even after the local receiver indicates filter convergence has occurred, the training controller 540 may prolong the training phase to coordinate training phase timing across lanes and along each link of the channel. The training frames include training sequences as specified by the relevant portions of the current Ethernet standard (IEEE Std 802.3).

[0035] The training controller 540 further accepts the back-channel information (BACK_INFO) extracted by the local receiver from received training frames sent by the local end node. The training controller applies the corresponding adjustments

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to the coefficients of transmit filter 506. Upon conclusion of the training phase, multiplexer 502 begins forwarding TXD blocks to the P2S circuit 504.

[0036] Fig. 6 is a flowchart of an illustrative cable manufacturing method. It begins in block 602 with connecting the ends of the conductor pairs to the first and second transceivers, typically by soldering the wire ends to pads of the circuit boards on which the transceivers are mounted. This and the ensuing steps may be performed by automated manufacturing/testing equipment. In block 604, the equipment packages each transceiver in a respective end connector for the network cable. The connectors are adapted to mate with network interface ports of host devices, and include plugs that electrically connect with matching receptacles in the ports.

[0037] In block 606, the equipment tests the cable to verify compliance with performance specifications and to determine cable-dependent equalization parameters for use by the center-facing transmitter and receiver sets 212. In block 608, the equipment causes the transceivers to store the equalization parameters (including both cable-dependent and cable-independent parameters) in nonvolatile memory. The cable may then be packaged and sold to customers expecting robust performance between host devices made by a range of different manufacturers.

[0038] Though a two-ended cable has been used in the foregoing description, the disclosed principles are also applicable to other cable designs, including the 1:4 breakout cable design of Figs. 7 and 8. Fig. 7 is a perspective view of the breakout cable having a first connector 102 which may be designed for sending and receiving a 200 Gbps Ethernet data stream, e.g., in the form of 4 lanes of 50 Gbps, each lane using PAM4 at 26.5625 GBd. Four cords 906 may each carry 1 lane of 50 Gbps or 2 lanes of 25 Gbps, each lane using PAM4 at 26.5625 GBd or non-return to zero (NRZ)

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signaling at 26.5625 GBd. Each of the connectors 802-808 may be designed for sending and receiving a 50 Gbps Ethernet data stream. Such breakout cables are useful for linking host devices designed to different generations of the Ethernet standard. As another example, the first connector may be designed for sending and receiving 400 Gbps (8 lanes of 50 Gbps PAM4), while each of the remaining connectors may be designed for sending and receiving 100 Gbps (4 lanes of 25 Gbps NRZ).

[0039] Fig. 8 shows a block diagram of the 1:4 breakout cable. In the example of Fig. 8, connector 102 supports 4 lanes while each of the other connectors 802-808 supports one lane. Connectors 802-808 accordingly include transceivers 905 each having a single host-facing lane and a single center-facing lane supported by host-facing transmitter and receiver sets 910 and center-facing transmitter and receiver sets 912. Though not explicitly shown here, the host-facing transmitter and receiver sets 910 may include "gearbox" functions that convert 1 lane of PAM4 symbols into 2 lanes of NRZ symbols, and vice versa. FIFO buffers 914 bridge together the host-facing and center-facing sets, and operation of the transmitter and receiver sets is coordinated by controllers 916.

[0040] Numerous alternative forms, equivalents, and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the claims be interpreted to embrace all such alternative forms, equivalents, and modifications that are encompassed in the scope of the appended claims.

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CLAIMS

What is claimed is:

1. An active Ethernet cable that comprises:

electrical conductors connected between a first connector and a second connector,

each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,

each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream.

2. The active Ethernet cable of claim 1, wherein the respective transceiver for each of the first and second connectors performs clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable.

3. The active Ethernet cable of claim 2, wherein the respective transceivers each employ fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.

4. The active Ethernet cable of claim 3, wherein the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data

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recovery performed on the electrical transit signal.

5. The active Ethernet cable of claim 4, wherein said cable-dependent equalization parameters adapt during usage of the Ethernet cable.

6. The active Ethernet cable of claim 4, wherein said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturer-testing of the Ethernet cable.

7. The active Ethernet cable of claim 6, wherein the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd.

8. A communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector:

receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device;

performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream;

re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs;

receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device;

performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream; and

re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor

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pairs.

9. The communication method of claim 8, further comprising:

performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream;

re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device;

performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream; and

re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device.

10. The communication method of claim 9, wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.

11. The communication method of claim 10, wherein cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said performing clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical transit signal.

12. The communication method of claim 11, wherein said cable-dependent equalization parameters are adaptively updated.

13. The communication method of claim 11, wherein said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters

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during manufacturer-testing of the network cable.

14. The communication method of claim 13, wherein the first inbound data stream has a per-lane symbol rate in excess of 50 GBd.

15. A cable manufacturing method that comprises:

connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver;

packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and

packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device,

the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams.

16. The cable manufacturing method of claim 15, wherein the first and second transceivers are configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first

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transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable.

17. The cable manufacturing method of claim 16, wherein the first and second transceivers are each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals.

18. The cable manufacturing method of claim 17, wherein the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals.

19. The cable manufacturing method of claim 18, wherein the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation.

20. The cable manufacturing method of claim 18, wherein the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters.

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ABSTRACT

Accordingly, there are disclosed herein architectures and communication methods that enable mass-manufactured cables to perform robustly at per-lane PAM4 symbol rates up to 56GBd and beyond. One illustrative cable embodiment includes conductor pairs connected between a first connector and a second connector. The first and second connectors are each adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable, and to provide to that host device an electrical output signal conveying an outbound data stream from the cable. The first and second connectors each include a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the conductor pairs as a respective electrical transit signal conveying a transit data stream.

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FIG. 1

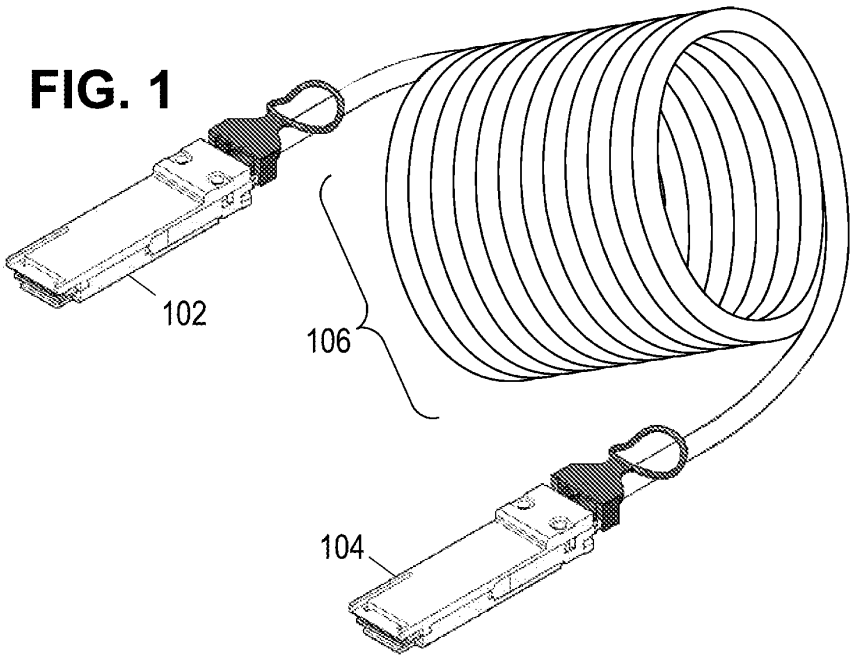
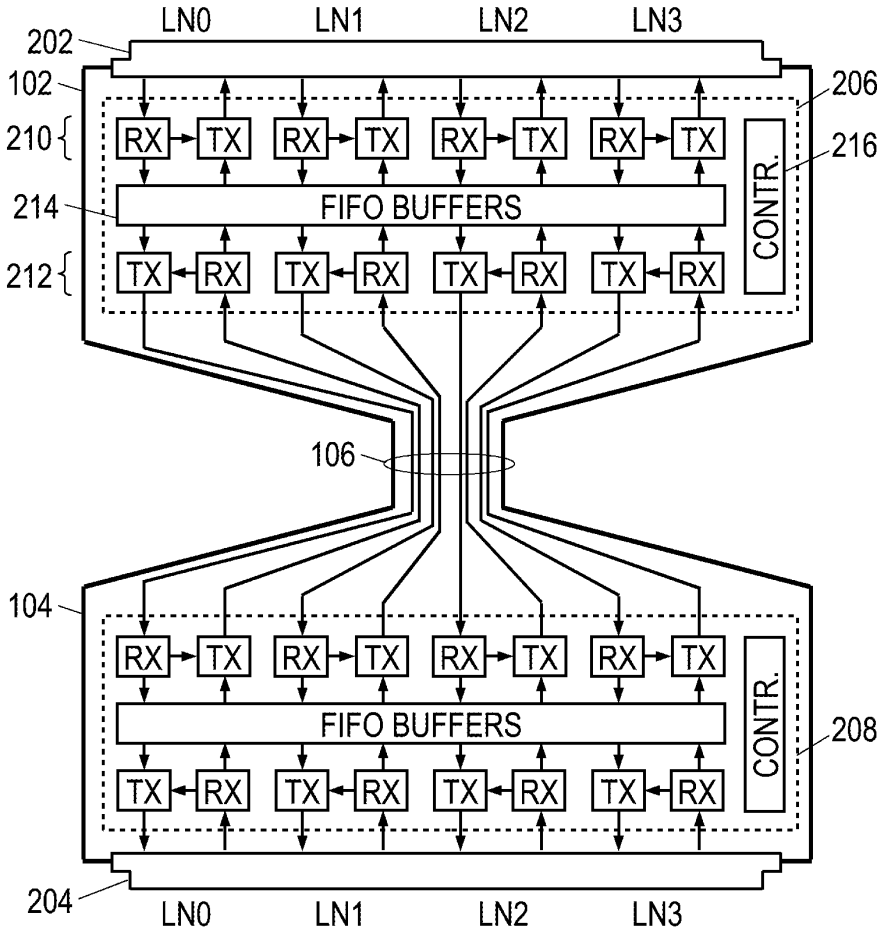

102
106
104

FIG. 2


LN0
LN1
LN2
LN3
202
102
206
210
RX
TX
216
214
FIFO BUFFERS
CONTR.
212
106
104
208
204

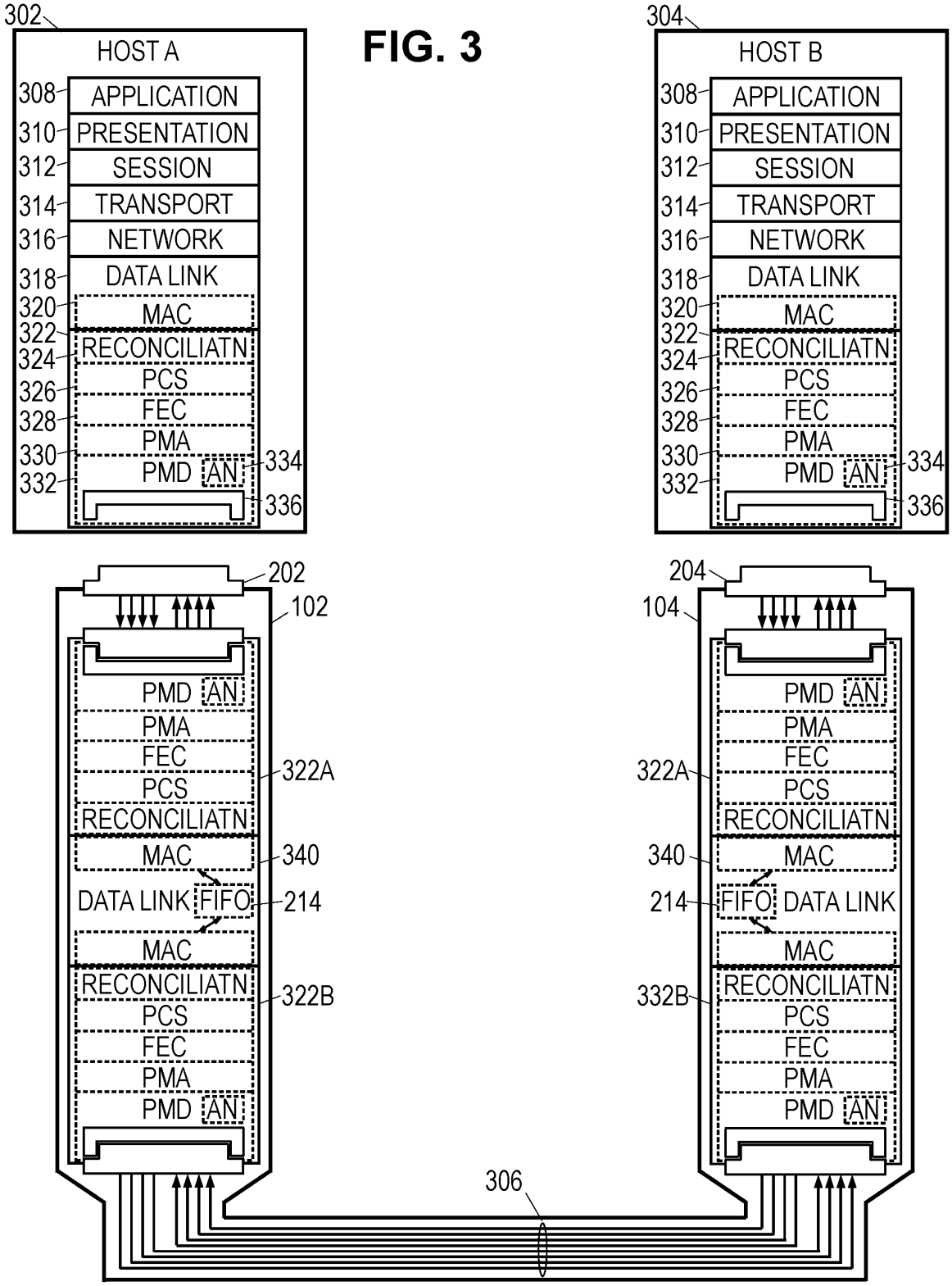
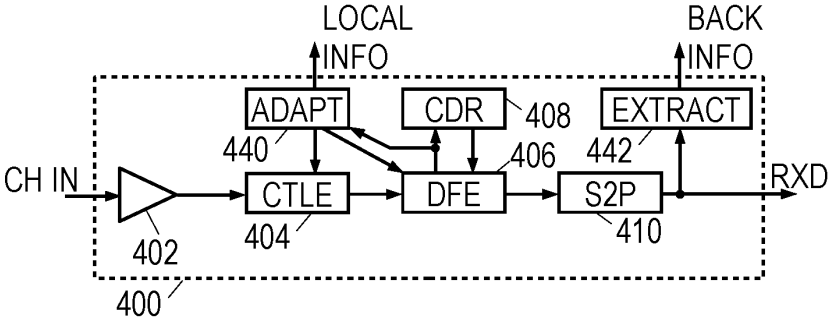

302
HOST A
308
APPLICATION
310
PRESENTATION
312
SESSION
314
TRANSPORT
316
NETWORK
318
DATA LINK
320
MAC
322
RECONCILIATN
324
PCS
326
FEC
328
PMA
330
PMD
AN
334
332
336
304
HOST B
308
APPLICATION
310
PRESENTATION
312
SESSION
314
TRANSPORT
316
NETWORK
318
DATA LINK
320
MAC
322
RECONCILIATN
324
PCS
326
FEC
328
PMA
330
PMD
AN
334
332
336
202
102
PMD
AN
PMA
FEC
PCS
RECONCILIATN
322A
MAC
340
DATA LINK
FIFO
214
MAC
RECONCILIATN
PCS
FEC
PMA
PMD
AN
322B
204
104
PMD
AN
PMA
FEC
PCS
RECONCILIATN
322A
MAC
340
214
FIFO
DATA LINK
MAC
RECONCILIATN
332B
PCS
FEC
PMA
PMD
AN
306

FIG. 3

FIG. 4



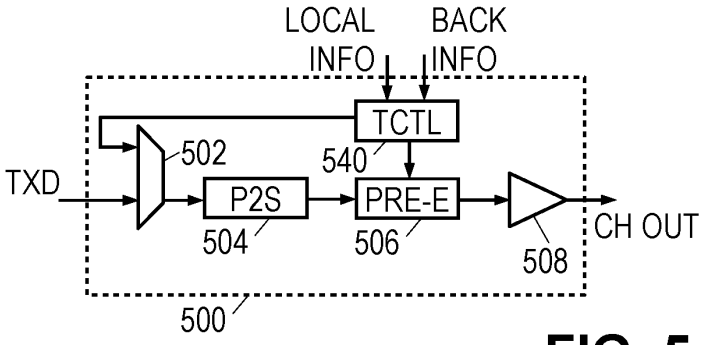


FIG. 5

FIG. 6

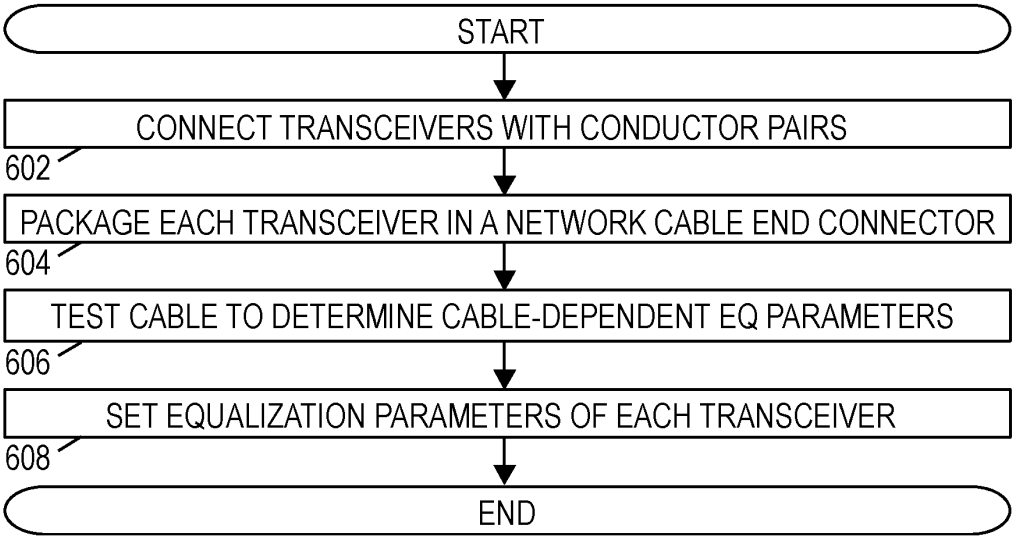


FIG. 7

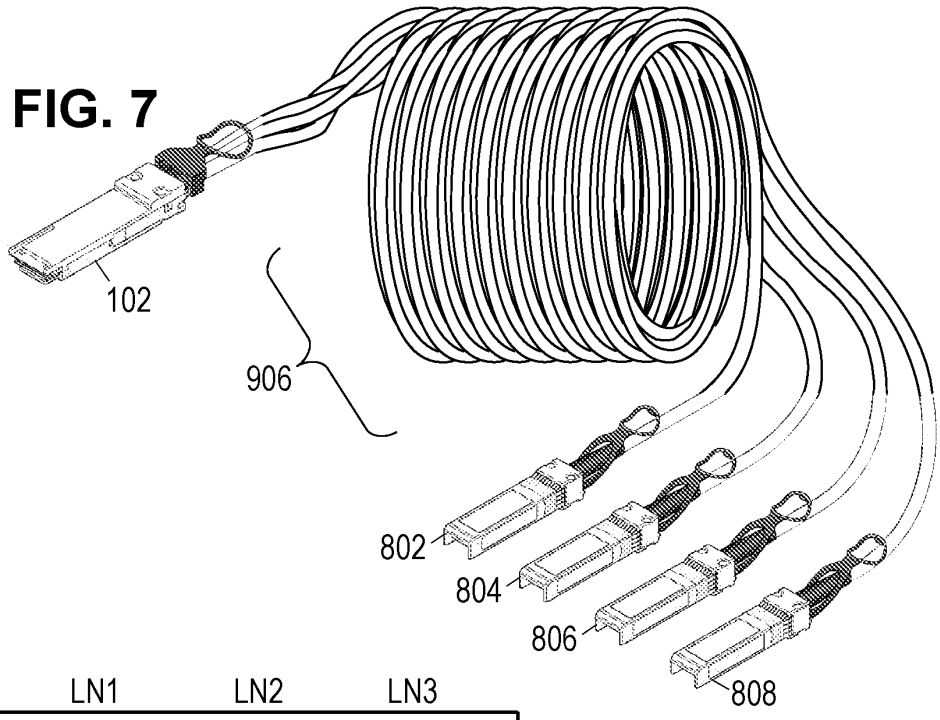
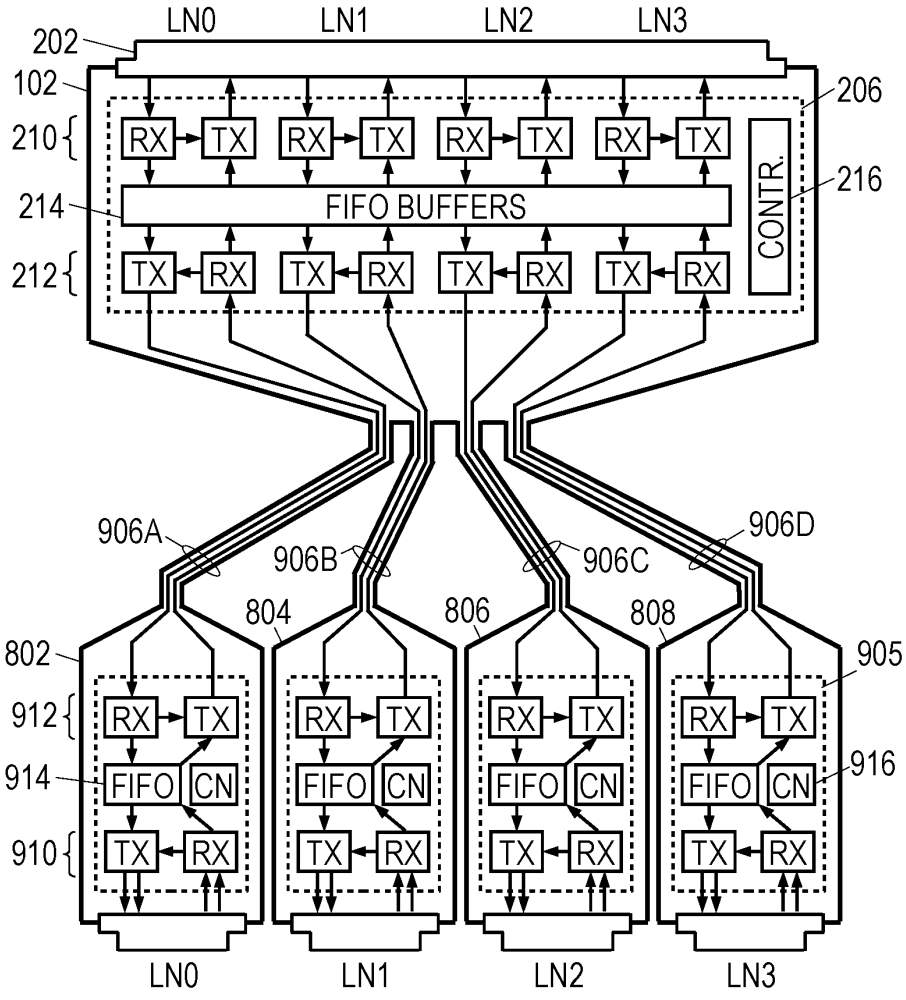

102
906
802
804
806
808

FIG. 8


LN0
LN1
LN2
LN3
202
102
206
210
RX
TX
214
FIFO BUFFERS
216
CONTR.
212
906A
906B
906C
906D
804
806
808
802
905
912
914
FIFO
CN
916
910
LN0
LN1
LN2
LN3

IEEE P802.3cd™/D1.2

Draft Standard for Ethernet Amendment: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation

Prepared by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

This draft is an amendment of IEEE Std 802.3-2015 as amended by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, IEEE Std 802.3bp-2016, IEEE Std 802.3br-2016, IEEE Std 802.3bn-2016, IEEE Std 802.3bz-2016, and [many others]. This amendment defines IEEE 802.3 Media Access Control (MAC) parameters, Physical Layer specifications, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s. Draft D1.2 is prepared for Task Force review. This draft expires 6 months after the date of publication or when the next version is published, whichever comes first.

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Abstract: This amendment to IEEE Std 802.3-2015 adds Clause 131 through Clause 140 and Annex 135A through Annex 136C. This amendment includes IEEE 802.3 Media Access Control (MAC) parameters, Physical Layer specifications, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

Keywords: 50GAUI-1, 50GAUI-2, 50GBASE-CR, 50GBASE-KR, 50GBASE-FR, 50GBASE-LR, 50GBASE-SR, 50 Gigabit Ethernet, 50GMII, 100GAUI-2, 100GAUI-4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100 Gigabit Ethernet, 200GBASE-CR4, 200GBASE-KR4, 200GBASE-SR4, 200 Gigabit Ethernet, Energy Efficient Ethernet (EEE), Ethernet, forward error correction (FEC), IEEE 802.3™, IEEE Std 802.3cd™, LAUI-2, MMF, SMF.

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Introduction

This introduction is not part of IEEE Std 802.3cd-20xx, IEEE Draft Standard for Ethernet. Amendment: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the date of IEEE Std 802.3cd-20xx publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines ser-

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vices and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw™-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by™-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq™-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bp™-2016

Amendment 4—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 97 and Clause 98. This amendment adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable in automotive and other applications not utilizing the structured wiring plant.

IEEE Std 802.3br™-2016

Amendment 5—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 99. This amendment adds a MAC Merge sublayer and a MAC Merge Service Interface to support for Interspersing Express Traffic over a single link.

IEEE Std 802.3bn™-2016

Amendment 6—This amendment adds the Physical Layer specifications and management parameters for symmetric and/or asymmetric operation of up to 10 Gb/s on point-to-multipoint Radio Frequency (RF) distribution plants comprising either amplified or passive coaxial media. It also extends the operation of Ethernet Passive Optical Networks (EPON) protocols, such as Multipoint Control Protocol (MPCP) and Operation Administration and Management (OAM).

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IEEE Std 802.3bz™-2016

Amendment 7—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 125 and Clause 126. This amendment adds new rates of 2.5 Gb/s and 5 Gb/s and new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bu™-201x

Amendment 8—This amendment includes changes to IEEE Std 802.3-2015 to define a methodology for the provision of power via a single twisted pair to connected Data Terminal Equipment (DTE) with IEEE 802.3 single twisted-pair interfaces.

IEEE Std 802.3bv™-201x

Amendment 9—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 115 and Annex 115A. This amendment adds point-to-point 1000 Mb/s Physical Layer (PHY) specifications and management parameters for operation on duplex plastic optical fiber (POF) targeting use in automotive, industrial, home-network, and other applications.

IEEE Std 802.3bs™-201x

This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 116 through Clause 124 and Annex 119A through Annex 120E. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 200 Gb/s and 400 Gb/s.

IEEE Std 802.3[others]™-201x

This amendment includes…

IEEE Std 802.3cd™-201x

This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 131 through Clause 140 and Annex 135A through Annex 136C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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Draft Standard for Ethernet Amendment: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation

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Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

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1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Insert the following new compatibility interfaces after "k) 40 Gb/s Parallel Physical Interface (XLPPI)":

k1) *50 Gb/s Media Independent Interface (50GMII).* The 50GMII is designed to connect a 50 Gb/s capable MAC to a 50 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The 50GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 50GMII. The 50GMII is optional.

k2) *50 Gb/s Attachment Unit Interface (LAUI-2/50GAUI-n).* The LAUI-2/50GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The LAUI-2/50GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of 50GAUI-n are defined: a two-lane version (50GAUI-2) in Annex 135D and Annex 135E, and a one-lane version (50GAUI-1) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the LAUI-2/50GAUI-n. The LAUI-2/50GAUI-n is optional.

Change the compatibility interface "m) 100 Gb/s Attachment Unit Interface (CAUI-n)" as follows:

m) *100 Gb/s Attachment Unit Interface (CAUI-n/100GAUI-n).* The CAUI-n/100GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 100 Gb/s speeds. The CAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Three~~Two~~ widths of CAUI-n are defined: a ten-lane version (CAUI-10) in Annex 83A and Annex 83B, ~~and~~ a four-lane version (CAUI-4/100GAUI-4) in Annex 83D~~, and~~, Annex 83E, Annex 135D, and Annex 135E, and a two-lane version (100GAUI-2) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the CAUI-n/100GAUI-n. The CAUI-n/100GAUI-n is optional.

1.3 Normative references

Change the reference for IEC 61753-022-2 as follows:

IEC 61753-022-2:2012, Fibre optic interconnecting devices and passive components - Performance standard - Part 022-2: Fibre optic connectors terminated on multimode fibre for category C - Controlled environment~~, performance Class M~~.

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1.4 Definitions

Insert the following new definition after 1.4.52 "100GBASE-R encoding":

1.4.52a 100GBASE-CR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

Insert the following new definition after 1.4.54 "100GBASE-CR10":

1.4.54a 100GBASE-DR: IEEE 802.3 Physical Layer specification for 100 Gb/s serial transmission using 100GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 140.)

Insert the following new definition after 1.4.55 "100GBASE-KP4":

1.4.55a 100GBASE-KR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

Insert the following new definition after 1.4.58 "100GBASE-LR4":

1.4.58a 100GBASE-SR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of multimode fiber. (See IEEE Std 802.3, Clause 138.)

Insert the following new definitions after 1.4.72a "40GBASE-T" (as inserted by IEEE Std 802.3bq-2016):

1.4.72a1 50GBASE-CR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

1.4.72a2 50GBASE-FR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 139.)

1.4.72a3 50GBASE-KR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

1.4.72a4 50GBASE-LR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 139.)

1.4.72a5 50GBASE-R: An IEEE 802.3 physical coding sublayer for one-lane 50 Gb/s operation. (See IEEE Std 802.3, Clause 131.)

1.4.72a6 50GBASE-SR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over multimode fiber. (See IEEE Std 802.3, Clause 138.)

1.4.72a7 50 Gb/s Attachment Unit Interface (50GAUI-n, LAUI-2): A physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs over one lane (50GAUI-1) or two lanes (50GAUI-2, LAUI-2), used for chip-to-chip or chip-to-module interconnections. (See IEEE Std 802.3, Clause 135 and Annex 135B through Annex 135G.)

1.4.72a8 50 Gb/s Media Independent Interface (50GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 50 Gb/s operation. (See IEEE Std 802.3, Clause 132)

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1.4.72a9 200GBASE-CR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136)

Insert the following new definition after 1.4.72c "200GBASE-FR4" (as inserted by IEEE Std 802.3bs-201x):

1.4.72c1 200GBASE-KR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

Insert the following new definition after 1.4.72e "200GBASE-R" (as inserted by IEEE Std 802.3bs-201x):

1.4.72e1 200GBASE-SR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of multimode fiber. (See IEEE Std 802.3, Clause 138.)

Modify 1.4.81 as follows:

1.4.81 100 Gb/s Attachment Unit Interface (CAUI-n, 100GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. Three~~Two~~ widths of CAUI-n are defined: a ten-lane version (CAUI-10), ~~and~~ two four-lane versions (CAUI-4, 100GAUI-4), and a two-lane version (100GAUI-2). (See IEEE Std 802.3, Annex 83A and Annex 83B for CAUI-10, ~~or~~ Annex 83D and Annex 83E for CAUI-4, Clause 135, Annex 135D, and Annex 135E for 100GAUI-4, or Clause 135, Annex 135F, and Annex 135G for 100GAUI-2.)

Insert the following new definition after 1.4.203 "fast wake":

1.4.203a FEC lane (FECL): In 50GBASE-R and 100GBASE-R the FEC distributes encoded data to multiple logical lanes, these logical lanes are called FEC lanes. One or more FEC lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 135.)

Modify 1.4.325 (as modified by IEEE Std 802.3bs-201x) as follows:

1.4.325 PCS lane (PCSL): In 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R, the PCS distributes encoded data to multiple logical lanes, these logical lanes are called PCS lanes. One or more PCS lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 83~~and~~, Clause 120, and Clause 135.)

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

100GAUI	100 Gb/s Attachment Unit Interface
50GAUI	50 Gb/s Attachment Unit Interface
50GMII	50 Gb/s Media Independent Interface
FECL	FEC Lane
LAUI	50 Gb/s Attachment Unit Interface

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4. Media Access Control

4.4 Specific implementations

4.4.2 MAC parameters

Change Table 4–2 (as modified by IEEE Std 802.3by-2016, IEEE Std 802.3bz-2016 and IEEE Std 802.3bs-201x) as follows:

Table 4–2—MAC parameters

Parameters	MAC data rate			
	Up to and including 100 Mb/s	1 Gb/s	2.5 Gb/s, 5 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s	10 Gb/s
slotTime	512 bit times	4096 bit times	not applicable	not applicable
interPacketGap[a]	96 bits	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable	not applicable
backoffLimit	10	10	not applicable	not applicable
jamSize	32 bits	32 bits	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	1518 octets	1518 octets
maxEnvelopeFrameSize	2000 octets	2000 octets	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	not applicable	104 bits

[a]References to interFrameGap or interFrameSpacing in other clauses (e.g., 13, 35, and 42) shall be interpreted as interPacketGap.

Change Note 7 below Table 4–2 (as modified by IEEE Std 802.3bs-201x) as follows:

NOTE 7—For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, 50GMII, CGMII, 200GMII, or 400GMII receive signals at the DTE due to clock tolerance and lane alignment requirements.

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30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry in "APPROPRIATE SYNTAX" after the entry for 40GBASE-R:

APPROPRIATE SYNTAX:

...

50GBASE-R	Clause 133 50 Gb/s multi-PCS lane 64B/66B

30.3.2.1.3 aPhyTypeList

Insert the following new entry in "APPROPRIATE SYNTAX" after the entry for 40GBASE-R:

APPROPRIATE SYNTAX:

...

50GBASE-R	Clause 133 50 Gb/s multi-PCS lane 64B/66B

30.3.2.1.5 aSymbolErrorDuringCarrier

Change the fourth paragraph in the "BEHAVIOUR DEFINED AS" section of 30.3.2.1.5 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

For operation at 10 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, it is a count of the number of times the receiving media is non-idle (the time between the Start of Packet Delimiter and the End of Packet Delimiter as defined by 46.2.3 and 81.2.5) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate "Receive Error" on the (see Table 46–4 and Table 81–3).

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entries in "APPROPRIATE SYNTAX" section of 30.5.1.1.2 (as modified by IEEE Std 802.3bs-201x) with the 50G entries going after 40GBASE-FR, the 100G entries going after 100GBASE-ER4 and the 200G entries going after 200GBASE-LR4:

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APPROPRIATE SYNTAX:

...	
50GBASE-R	Multi-lane PCS as specified in Clause 133 with PMA as specified in Clause 135 over undefined PMD
50GBASE-CR	50GBASE-R PCS/PMA over shielded copper balanced cable PMD as specified in Clause 136
50GBASE-KR	50GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
50GBASE-SR	50GBASE-R PCS/PMA over multimode fiber PMD as specified in Clause 138
50GBASE-FR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139
50GBASE-LR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139
...	
100GBASE-CR2	100GBASE-R PCS/PMA over 2-lane shielded copper balanced cable PMD as specified in Clause 136
100GBASE-KR2	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
100GBASE-SR2	100GBASE-R PCS/PMA over 2-lane multimode fiber PMD as specified in Clause 138
100GBASE-DR	100GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 140
...	
200GBASE-CR4	100GBASE-R PCS/PMA over 4-lane shielded copper balanced cable PMD as specified in Clause 136
200GBASE-KR4	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
200GBASE-SR4	100GBASE-R PCS/PMA over 4-lane multimode fiber PMD as specified in Clause 138
...	

Change the last paragraph of the "BEHAVIOUR DEFINED AS" section of 30.5.1.1.2 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

The enumerations 1000BASE-X, 1000BASE-XHD, 1000BASE-XFD, 10GBASE-X, 10GBASE-R, 10GBASE-W, 25GBASE-R, 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R shall only be returned if the underlying PMD type is unknown.;

30.5.1.1.4 aMediaAvailable

Change the sixth paragraph of the "BEHAVIOUR DEFINED AS" section of 30.5.1.1.4 (as modified by IEEE Std 802.3bq-2016 and IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, the enumerations map to value of the link_fault variable within the Link Fault Signaling state diagram (see 81.3.4.1 and Figure 46–11) as follows: the values OK and Link Interruption map to the enumeration "available", the value

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Local Fault maps to the enumeration "not available" and the value Remote Fault maps to the enumeration "remote fault".

30.5.1.1.11 aBIPErrorCount

Change "APPROPRIATE SYNTAX" and first sentence of "BEHAVIOUR DEFINED AS" of 30.5.1.1.11 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 10 000 counts per second for 40 Gb/s and 50 Gb/s implementations and 5 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 40/50/100GBASE-R PHYs and 100GBASE-P PHYS, an array of BIP error counters.

30.5.1.1.12 aLaneMapping

Change the first sentence of "BEHAVIOUR DEFINED AS" of 30.5.1.1.12 (as modified by IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

For 40/50/100/200/400GBASE-R PHYs and 100GBASE-P PHYs, an array of PCS lane identifiers.

30.5.1.1.15 aFECAbility

Change the first sentence of "BEHAVIOUR DEFINED AS" of 30.5.1.1.15 (as modified by IEEE Std 802.3by-2016) as follows:

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an FEC sublayer for forward error correction (see 65.2, Clause 74, Clause 91, ~~and~~ Clause 108, and Clause 134).

30.5.1.1.17 aFECCorrectedBlocks

Change "APPROPRIATE SYNTAX" of 30.5.1.1.17 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

Change the first sentence of the "BEHAVIOUR DEFINED AS" of 30.5.1.1.17 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

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For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of corrected FEC block counters.

30.5.1.1.18 aFECUncorrectableBlocks

Change "APPROPRIATE SYNTAX" of 30.5.1.1.18 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

Change the first sentence of the "BEHAVIOUR DEFINED AS" of 30.5.1.1.18 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of uncorrectable FEC block counters.

30.5.1.1.26 aRSFECBIPErrorCount

Change "APPROPRIATE SYNTAX" and first sentence of "BEHAVIOUR DEFINED AS" of 30.5.1.1.26 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 5 000 counts per second for 50 Gb/s and 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R, and 100GBASE-P PHYs, an array of BIP error counters.

30.5.1.1.27 aRSFECLaneMapping

Change the first sentence of "BEHAVIOUR DEFINED AS" of 30.5.1.1.27 as follows:

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R, and 100GBASE-P PHYs, an array of PCS lane identifiers.

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30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entries in "APPROPRIATE SYNTAX" section of 30.6.1.1.5 with the 50GR entry going after 40GBASE-CR4, and the 100GR2 and 200GR4 entries going after 100GBASE-KP4 as follows:

APPROPRIATE SYNTAX:

50GR	50GBASE-CR as specified in Clause 136 or 50GBASE-KR as specified in Clause 137
100GR2	100GBASE-CR2 as specified in Clause 136 or 100GBASE-KR2 as specified in Clause 137
200GR4	200GBASE-CR4 as specified in Clause 136 or 200GBASE-KR4 as specified in Clause 137

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45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change Table 45–3 (as modified by IEEE Std 802.3bz-2016 and IEEE Std 802.3bs-201x) as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.20	~~Reserved~~ 50G PMA/PMD extended ability	45.2.1.14b1
…		
1.25, ~~1.26~~	~~Reserved~~ PMA/PMD extended ability 2	45.2.1.14f1
1.26	Reserved	
…		
1.500 through 1.515	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 through lane 15	45.2.1.116d, 45.2.1.116e
1.516 through 1.531	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 through lane 15	45.2.1.116f, 45.2.1.116g
…		
~~1.532 through 1.699~~ 1.532 through 1.599	Reserved	
1.600	PMA precoder control down Tx	45.2.1.116h
1.601	PMA precoder control down Rx	45.2.1.116i
1.602	PMA precoder control up Tx	45.2.1.116j
1.603	PMA precoder control up Rx	45.2.1.116k
1.604	PMA precoder request status	45.2.1.116l
1.605	PMA precoder request down	45.2.1.116m
1.606	PMA precoder request up	45.2.1.116n
1.607 through 1.699	Reserved	
…		
1.1110 through 1.1119	Reserved	
1.1120 through 1.1123	BASE-R PAM4 PMD training LP control registers, lanes 0 through 3	45.2.1.118a
~~1.1110 through 1.1199~~ 1.1124 through 1.1199	Reserved	

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Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
…		
1.1210 through 1.1219	Reserved	
1.1220 through 1.1223	BASE-R PAM4 PMD training LP status registers, lanes 0 through 3	45.2.1.119a
~~1.1210 through 1.1299~~ 1.1224 through 1.1299	Reserved	
…		
1.1310 through 1.1319	Reserved	
1.1320 through 1.1323	BASE-R PAM4 PMD training LD control registers, lanes 0 through 3	45.2.1.120a
~~1.1310 through 1.1399~~ 1.1324 through 1.1399	Reserved	
…		
1.1410 through 1.1419	Reserved	
1.1420 through 1.1423	BASE-R PAM4 PMD training LD status registers, lanes 0 through 3	45.2.1.121a
~~1.1410 through 1.1449~~ 1.1424 through 1.1449	Reserved	
…		

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change the row for bits 1.0.5:2 in Table 45–4 (as modified by IEEE Std 802.3by-2016, IEEE Std 802.3bz-2016, and IEEE Std 802.3bs-201x) as follows (unchanged rows not shown):

45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Change the last paragraph of 45.2.1.1.3 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

When bits 5 through 2 are set to 0010 the use of a 40G PMA/PMD is selected; when set to 0011 the use of a 100G PMA/PMD is selected; when set to 0100 the use of a 25G PMA/PMD is selected; when set to 0101 the use of a 50G PMA/PMD is selected; when set to 1000 the use of a 200G PMA/PMD is selected; when set to 1001 the use of a 400G PMA/PMD is selected. More specific selection is performed using the PMA/PMD control 2 register (Register 1.7) (see 45.2.1.6.3).

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Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 400 Gb/s 1 0 0 0 = 200 Gb/s 0 1 1 1 = 5 Gb/s 0 1 1 0 = 2.5 Gb/s 0 1 0 1 = ~~Reserved~~ 50 Gb/s 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
…			

[a]R/W = Read/Write, SC = Self-clearing, RO = Read only

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

45.2.1.2.3 Fault (1.1.7)

Change the fourth sentence of 45.2.1.2.3 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

For 10/25/40/50/100/200/400 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one.

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45.2.1.4 PMA/PMD speed ability (Register 1.4)

Change the row for 1.4.3 in Table 45–6 (as modified by IEEE Std 802.3bn-2016, IEEE Std 802.3bz-2016 and IEEE Std 802.3bs-201x) as follows (unchanged rows not shown):

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.4.3	~~Reserved~~ 50G capable	~~Value always 0~~ 1 = PMA/PMD is capable of operating at 50 Gb/s 0 = PMA/PMD is not capable of operating at 50 Gb/s	RO
…			

[a]RO = Read only

Insert 45.2.1.4.6a after 45.2.1.4.6 as follows:

45.2.1.4.6a 50G capable (1.4.3)

When read as a one, bit 1.4.3 indicates that the PMA/PMD is able to operate at a data rate of 50 Gb/s. When read as a zero, bit 1.4.3 indicates that the PMA/PMD is not able to operate at a data rate of 50 Gb/s.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45–7 (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, IEEE Std 802.3bp-2016, IEEE Std 802.3bn-201x, IEEE Std 802.3bv-2016, IEEE Std 802.3bz-2016, IEEE Std 802.3bs-201x, IEEE Std 802.3cb-201x, and IEEE Std 802.3cc-201x) as follows:

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:10	Reserved	Value always 0	RO
1.7.9	PIASE	PMA ingress AUI stop enable	R/W
1.7.8	PEASE	PMA egress AUI stop enable	R/W
1.7.7	Reserved	Value always 0	RO

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Table 45–7—PMA/PMD control 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.7.6:0	PMA/PMD type selection	6 5 4 3 2 1 0 1 1 x x x x x = reserved 1 0 1 1 1 1 x = reserved 1 0 1 1 1 0 1 = reserved 1 0 1 1 1 0 0 = 400GBASE-LR8 PMA/PMD 1 0 1 1 0 1 1 = 400GBASE-FR8 PMA/PMD 1 0 1 1 0 1 0 = 400GBASE-DR4 PMA/PMD 1 0 1 1 0 0 1 = 400GBASE-SR16 PMA/PMD 1 0 1 1 0 0 0 = reserved 1 0 1 0 1 1 x = reserved 1 0 1 0 1 0 1 = 200GBASE-LR4 PMA/PMD 1 0 1 0 1 0 0 = 200GBASE-FR4 PMA/PMD 1 0 1 0 0 1 1 = 200GBASE-DR4 PMA/PMD 1 0 1 0 0 1 0 = 200GBASE-SR4 PMA/PMD ~~reserved~~ 1 0 1 0 0 0 1 = 200GBASE-CR4 PMA/PMD 1 0 1 0 0 0 0 = 200GBASE-KR4 PMA/PMD ~~1 0 1 0 0 0 x = reserved~~ ~~1 0 0 x x x x x = reserved~~ 1 0 0 1 1 x x = reserved 1 0 0 1 0 1 1 = 100GBASE-DR PMA/PMD 1 0 0 1 0 1 0 = 100GBASE-SR2 PMA/PMD 1 0 0 1 0 0 1 = 100GBASE-CR2 PMA/PMD 1 0 0 1 0 0 0 = 100GBASE-KR2 PMA/PMD 1 0 0 0 1 1 x = reserved 1 0 0 0 1 0 1 = reserved 1 0 0 0 1 0 0 = 50GBASE-LR PMA/PMD 1 0 0 0 0 1 1 = 50GBASE-FR PMA/PMD 1 0 0 0 0 1 0 = 50GBASE-SR PMA/PMD 1 0 0 0 0 0 1 = 50GBASE-CR PMA/PMD 1 0 0 0 0 0 0 = 50GBASE-KR PMA/PMD 0 1 1 1 1 1 x = reserved 0 1 1 1 1 0 1 = BASE-T1 PMA/PMD[b] 0 1 1 1 1 0 0 = 5GBASE-KR PMA/PMD 0 1 1 1 0 1 1 = 2.5GBASE-KX PMA/PMD 0 1 1 1 0 1 0 = 25GBASE-SR PMA/PMD 0 1 1 1 0 0 1 = 25GBASE-KR or 25GBASE-KR-S PMA/PMD 0 1 1 1 0 0 0 = 25GBASE-CR or 25GBASE-CR-S PMA/PMD 0 1 1 0 1 1 1 = 25GBASE-T PMA 0 1 1 0 1 1 0 = 25GBASE-ER PMA/PMD 0 1 1 0 1 0 1 = 25GBASE-LR PMA/PMD 0 1 1 0 1 0 0 = BASE-H PMA/PMD[c] 0 1 1 0 0 1 1 = 10GPASS-XR-U PMA/PMD 0 1 1 0 0 1 0 = 10GPASS-XR-D PMA/PMD 0 1 1 0 0 0 1 = 5GBASE-T PMA 0 1 1 0 0 0 0 = 2.5GBASE-T PMA 0 1 0 1 1 1 1 = 100GBASE-SR4 PMA/PMD 0 1 0 1 1 1 0 = 100GBASE-CR4 PMA/PMD 0 1 0 1 1 0 1 = 100GBASE-KR4 PMA/PMD 0 1 0 1 1 0 0 = 100GBASE-KP4 PMA/PMD 0 1 0 1 0 1 1 = 100GBASE-ER4 PMA/PMD 0 1 0 1 0 1 0 = 100GBASE-LR4 PMA/PMD 0 1 0 1 0 0 1 = 100GBASE-SR10 PMA/PMD 0 1 0 1 0 0 0 = 100GBASE-CR10 PMA/PMD 0 1 0 0 1 1 1 = reserved	R/W

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Table 45–7—PMA/PMD control 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.7.6:0 *(continued)*	PMA/PMD type selection *(continued)*	0 1 0 0 1 1 0 = 40GBASE-T PMA 0 1 0 0 1 0 1 = 40GBASE-ER4 PMA/PMD 0 1 0 0 1 0 0 = 40GBASE-FR PMA/PMD 0 1 0 0 0 1 1 = 40GBASE-LR4 PMA/PMD 0 1 0 0 0 1 0 = 40GBASE-SR4 PMA/PMD 0 1 0 0 0 0 1 = 40GBASE-CR4 PMA/PMD 0 1 0 0 0 0 0 = 40GBASE-KR4 PMA/PMD 0 0 1 1 1 1 1 = 10/1GBASE-PRX-U4 0 0 1 1 1 1 0 = 10GBASE-PR-U4 0 0 1 1 1 0 1 = 10/1GBASE-PRX-D4 0 0 1 1 1 0 0 = 10GBASE-PR-D4 0 0 1 1 0 1 1 = reserved 0 0 1 1 0 1 0 = 10GBASE-PR-U3 0 0 1 1 0 0 1 = 10GBASE-PR-U1 0 0 1 1 0 0 0 = 10/1GBASE-PRX-U3 0 0 1 0 1 1 1 = 10/1GBASE-PRX-U2 0 0 1 0 1 1 0 = 10/1GBASE-PRX-U1 0 0 1 0 1 0 1 = 10GBASE-PR-D3 0 0 1 0 1 0 0 = 10GBASE-PR-D2 0 0 1 0 0 1 1 = 10GBASE-PR-D1 0 0 1 0 0 1 0 = 10/1GBASE-PRX-D3 0 0 1 0 0 0 1 = 10/1GBASE-PRX-D2 0 0 1 0 0 0 0 = 10/1GBASE-PRX-D1 0 0 0 1 1 1 1 = 10BASE-T PMA/PMD 0 0 0 1 1 1 0 = 100BASE-TX PMA/PMD 0 0 0 1 1 0 1 = 1000BASE-KX PMA/PMD 0 0 0 1 1 0 0 = 1000BASE-T PMA/PMD 0 0 0 1 0 1 1 = 10GBASE-KR PMA/PMD 0 0 0 1 0 1 0 = 10GBASE-KX4 PMA/PMD 0 0 0 1 0 0 1 = 10GBASE-T PMA 0 0 0 1 0 0 0 = 10GBASE-LRM PMA/PMD 0 0 0 0 1 1 1 = 10GBASE-SR PMA/PMD 0 0 0 0 1 1 0 = 10GBASE-LR PMA/PMD 0 0 0 0 1 0 1 = 10GBASE-ER PMA/PMD 0 0 0 0 1 0 0 = 10GBASE-LX4 PMA/PMD 0 0 0 0 0 1 1 = 10GBASE-SW PMA/PMD 0 0 0 0 0 1 0 = 10GBASE-LW PMA/PMD 0 0 0 0 0 0 1 = 10GBASE-EW PMA/PMD 0 0 0 0 0 0 0 = 10GBASE-CX4 PMA/PMD	

[a]R/W = Read/Write, RO = Read only
[b]If BASE-T1 is selected, bits 1.2100.3:0 are used to differentiate which BASE-T1 PMA/PMD is selected.
[c]If BASE-H PMA/PMD is selected, register 1.900 is used to differentiate which BASE-H PMA/PMD is selected

Change 45.2.1.6.3 (as modified by IEEE Std 802.3bs-201x) as follows:

45.2.1.6.3 PMA/PMD type selection (1.7.6:0)

The PMA/PMD type of the PMA/PMD shall be selected using bits 6 to 0. The PMA/PMD type abilities of the PMA/PMD are advertised in bits 9 and 7 through 0 of the PMA/PMD status 2 register; the PMA/PMD extended ability register; the 40G/100G PMA/PMD extended ability register; the 50G PMA/PMD extended ability register; the 200G PMA/PMD extended ability register, and the 400G PMA/PMD extended ability register. A PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types

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it has not advertised. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert the following rows after the row for 40GBASE-T (which was inserted by IEEE Std 802.3bq-2016) with the exception of the 100GBASE-DR row which goes after the 100GBASE-SR4 PMD in Table 45–9 as follows (unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
…	
50GBASE-KR, 100GBASE-KR2, 200GBASE-KR4	137.8.9
50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4	136.8.9
50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4	138.5.10
50GBASE-FR, 50GBASE-LR	139.5.8
…	
100GBASE-DR	140.5.8

45.2.1.7.5 Receive fault (1.8.10)

Insert the following rows after the row for 40GBASE-T (which was inserted by IEEE Std 802.3bq-2016) with the exception of the 100GBASE-DR row which goes after the 100GBASE-SR4 PMD in Table 45–10 as follows (unchanged rows not shown):

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Table 45–10—Receive fault description location

PMA/PMD	Description location
…	
50GBASE-KR, 100GBASE-KR2, 200GBASE-KR4	137.8.10
50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4	136.8.10
50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4	138.5.11
50GBASE-FR, 50GBASE-LR	139.5.9
…	
100GBASE-DR	140.5.9

45.2.1.8 PMD transmit disable register (Register 1.9)

Insert the following rows after the row for 40GBASE-T (which was inserted by IEEE Std 802.3bq-2016) with the exception of the 100GBASE-DR row which goes after the 100GBASE-SR4 PMD in Table 45–12 as follows (unchanged rows not shown):

Table 45–12—Transmit disable description location

PMA/PMD	Description location
…	
50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4	137.8.6
50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4	136.8.6
50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4	138.5.7
50GBASE-FR and 50GBASE-LR	139.5.6
…	
100GBASE-DR	140.5.6

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Insert 45.2.1.14b1 before 45.2.1.14c (as inserted by IEEE Std 802.3bz-2016) as follows:

45.2.1.14b1 50G PMA/PMD extended ability (Register 1.20)

The assignment of bits in the 50G PMA/PMD extended ability register is shown in Table 45--17b1.

Table 45–17b1—50G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.20.15	50G PMA remote loopback ability	1 = 50G PMA has the ability to perform a remote loopback function 0 = 50G PMA does not have the ability to perform a remote loopback function	RO
1.20.14:5	Reserved	Value always 0	RO
1.20.4	50GBASE-LR ability	1 = PMA/PMD is able to perform 50GBASE-LR 0 = PMA/PMD is not able to perform 50GBASE-LR	RO
1.20.3	50GBASE-FR ability	1 = PMA/PMD is able to perform 50GBASE-FR 0 = PMA/PMD is not able to perform 50GBASE-FR	RO
1.20.2	50GBASE-SR ability	1 = PMA/PMD is able to perform 50GBASE-SR 0 = PMA/PMD is not able to perform 50GBASE-SR	RO
1.20.1	50GBASE-CR ability	1 = PMA/PMD is able to perform 50GBASE-CR 0 = PMA/PMD is not able to perform 50GBASE-CR	RO
1.20.0	50GBASE-KR ability	1 = PMA/PMD is able to perform 50GBASE-KR 0 = PMA/PMD is not able to perform 50GBASE-KR	RO

[a]RO = Read only

45.2.1.14b1.1 50G PMA remote loopback ability (1.20.15)

When read as a one, bit 1.20.15 indicates that the 50G PMA is able to perform the remote loopback function. When read as a zero, bit 1.20.15 indicates that the 50G PMA is not able to perform the remote loopback function. If a PMA is able to perform the remote loopback function, then it is controlled using the PMA remote loopback bit 1.0.1 (see 45.2.1.1.4).

45.2.1.14b1.2 50GBASE-LR ability (1.20.4)

When read as a one, bit 1.20.4 indicates that the PMA/PMD is able to operate as a 50GBASE-LR PMA/PMD type. When read as a zero, bit 1.20.4 indicates that the PMA/PMD is not able to operate as a 50GBASE-LR PMA/PMD type.

45.2.1.14b1.3 50GBASE-FR ability (1.20.3)

When read as a one, bit 1.20.3 indicates that the PMA/PMD is able to operate as a 50GBASE-FR PMA/PMD type. When read as a zero, bit 1.20.3 indicates that the PMA/PMD is not able to operate as a 50GBASE-FR PMA/PMD type.

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45.2.1.14b1.4 50GBASE-SR ability (1.20.2)

When read as a one, bit 1.20.2 indicates that the PMA/PMD is able to operate as a 50GBASE-SR PMA/PMD type. When read as a zero, bit 1.20.2 indicates that the PMA/PMD is not able to operate as a 50GBASE-SR PMA/PMD type.

45.2.1.14b1.5 50GBASE-CR ability (1.20.1)

When read as a one, bit 1.20.1 indicates that the PMA/PMD is able to operate as a 50GBASE-CR PMA/PMD type. When read as a zero, bit 1.20.1 indicates that the PMA/PMD is not able to operate as a 50GBASE-CR PMA/PMD type.

45.2.1.14b1.6 50GBASE-KR ability (1.20.0)

When read as a one, bit 1.20.0 indicates that the PMA/PMD is able to operate as a 50GBASE-KR PMA/PMD type. When read as a zero, bit 1.20.0 indicates that the PMA/PMD is not able to operate as a 50GBASE-KR PMA/PMD type.

Insert 45.2.1.14f1 after 45.2.1.14f (as inserted by IEEE Std 802.3bs-201x) as follows:

45.2.1.14f1 PMA/PMD extended ability 2 (Register 1.25)

The assignment of bits in the PMA/PMD extended ability 2 register is shown in Table 45–17f1.

Table 45–17f1—PMA/PMD extended ability 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.25.15:1	Reserved	Value always 0	RO
1.25.0	50G extended abilities	1 = PMA/PMD has 50G extended abilities listed in register 1.20 0 = PMA/PMD does not have 50G extended abilities	RO

[a]RO = Read only

45.2.1.14f1.1 50G extended abilities (1.25.0)

When read as a one, bit 1.25.0 indicates that the PMA/PMD has 50G extended abilities listed in register 1.20. When read as a zero, bit 1.25.0 indicates that the PMA/PMD does not have 50G extended abilities.

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45.2.1.101 RS-FEC control register (Register 1.200)

Change Table 45–79 (as modified by IEEE Std 802.3by-2016) as follows:

Table 45–79—RS-FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.200.15:4 ~~1.200.15:3~~	Reserved	Value always 0	RO
1.200.3	Four lane PMD indication	1 = FEC is not being used with a four-lane PMD (the four_lane_pmd variable defined 91.6.2a is set to zero) 0 = FEC is being used with a four-lane PMD (the four_lane_pmd variable defined 91.6.2a is set to one)	R/W
1.200.2	25G RS-FEC enable	1 = The 25GBASE-R Reed-Solomon FEC is enabled 0 = The 25GBASE-R Reed-Solomon FEC is disabled	R/W
1.200.1	FEC bypass indication enable	1 = FEC decoder does not indicate errors to the PCS 0 = FEC decoder indicates errors to the PCS layer	R/W
1.200.0	FEC bypass correction enable	1 = FEC decoder performs error detection without error correction 0 = FEC decoder performs error detection and error correction	R/W

[a]R/W = Read/Write, RO = Read only

Insert 45.2.1.101.aa before 45.2.1.101.a (as inserted by IEEE Std 802.3by-2016) as follows:

45.2.1.101.aa Four-lane PMD (1.200.3)

This bit enables the alignment marker mapping function in the RS-FEC to substitute the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16 (see 91.5.2.6). When this bit is set to zero, the alignment markers corresponding to PCS lanes 17, 18, and 19 are passed through unmodified. The default value of this bit is zero.

45.2.1.102 RS-FEC status register (Register 1.201)

Change the reserved rows for 1.201.7:3 in Table 45–80 as follows (unchanged rows not shown):

Table 45–80—RS-FEC status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.201.7	FEC optional states supported	1 = RS-FEC supports optional states in Figure 91–8 0 = RS-FEC does not support optional states in Figure 91–8	RO
~~1.201.7:3~~ 1.201.6:3	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

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Change 45.2.1.102.1, 45.2.1.102.2 (as modified by IEEE Std 802.3by-2016), and 45.2.1.102.5, and 45.2.1.102.6 as follows

45.2.1.102.1 PCS align status (1.201.15)

Bit 1.201.15 indicates the PCS alignment status of the RS-FEC. For the RS-FEC described in Clause 91 or Clause 134, PCS alignment is defined as block lock, alignment marker lock and deskew of all 20 transmit PCS lanes. For the RS-FEC described in Clause 108, PCS alignment is defined as block lock of the transmit PCS signal. When read as a zero, bit 1.201.15 indicates that the RS-FEC has not obtained PCS alignment. When read as a one, bit 1.201.15 indicates that the RS-FEC has obtained PCS alignment.

45.2.1.102.2 RS-FEC align status (1.201.14)

Bit 1.201.14 indicates the PMA alignment status of the RS-FEC. For the RS-FEC described in Clause 91 or Clause 134, PMA alignment is defined as alignment marker lock and deskew of all four lanes on the PMA service interface. For the RS-FEC described in Clause 108, PMA alignment is defined as codeword marker lock on the PMA service interface. When read as a zero, bit 1.201.14 indicates that the RS-FEC has not obtained PMA alignment. When read as a one, bit 1.201.14 indicates that the RS-FEC has obtained PMA alignment.

45.2.1.102.5 FEC AM lock 1 (1.201.9)

When read as a one, bit 1.201.9 indicates that the RS-FEC described in Clause 91 or Clause 134 has locked and aligned lane 1 of the PMA service interface. When read as a zero, bit 1.201.9 indicates that the RS-FEC has not locked and aligned lane 1 of the PMA service interface. This bit reflects the state of amps_lock[1] (see 91.5.3.1).

45.2.1.102.6 FEC AM lock 0 (1.201.8)

When read as a one, bit 1.201.8 indicates that the RS-FEC described in Clause 91 or Clause 134 has locked and aligned lane 0 of the PMA service interface. When read as a zero, bit 1.201.8 indicates that the RS-FEC has not locked and aligned lane 0 of the PMA service interface. This bit reflects the state of amps_lock[0] (see 91.5.3.1).

Insert 45.2.1.102.6a after 45.2.1.102.6 as follows:

45.2.1.102.6a FEC optional states supported (1.201.7)

When read as a one, bit 1.201.7 indicates that the RS-FEC described in Clause 91 implements the optional states in Figure 91–8. When read as a zero, bit 1.201.7 indicates that the optional states are not implemented.

Change the second sentence of 45.2.1.108 as follows

45.2.1.108 RS-FEC BIP error counter lane 0 (Register 1.230)

The RS-FEC described in Clause 91 or Clause 134 calculates a BIP value for each PCS lane (see 91.5.2.4, 91.6.3).

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Change 45.2.1.116d to 45.2.1.116f (as inserted by IEEE Std 802.3bs-201x) as follows:

45.2.1.116d 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register (Register 1.500)

The assignment of bits in the 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register is shown in Table 45–90ab. The transmitter, receive direction, is the transmitter that sends data towards the MAC.

Table 45–90ab—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.500.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.500.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Requested_eq_c1* = 5 (c(1) ratio +0.25) 1 0 0 *Requested_eq_c1* = 4 (c(1) ratio +0.2) 0 1 1 *Requested_eq_c1* = 3 (c(1) ratio +0.15) 0 1 0 *Requested_eq_c1* = 2 (c(1) ratio +0.1) 0 0 1 *Requested_eq_c1* = 1 (c(1) ratio +0.05) 0 0 0 *Requested_eq_c1* = 0 (c(1) ratio 0)	RO
1.500.11:10	Pre-cursor request	11 10 1 1 *Requested_eq_cm1* = 3 (c(−1) ratio −0.15) 1 0 *Requested_eq_cm1* = 2 (c(−1) ratio −0.1) 0 1 *Requested_eq_cm1* = 1 (c(−1) ratio −0.05) 0 0 *Requested_eq_cm1* = 0 (c(−1) ratio 0)	RO
1.500.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Remote_eq_c1* = 5 (c(1) ratio +0.25) 1 0 0 *Remote_eq_c1* = 4 (c(1) ratio +0.2) 0 1 1 *Remote_eq_c1* = 3 (c(1) ratio +0.15) 0 1 0 *Remote_eq_c1* = 2 (c(1) ratio +0.1) 0 0 1 *Remote_eq_c1* = 1 (c(1) ratio +0.05) 0 0 0 *Remote_eq_c1* = 0 (c(1) ratio 0)	R/W
1.500.6:5	Pre-cursor remote setting	6 5 1 1 *Remote_eq_cm1* = 3 (c(−1) ratio −0.15) 1 0 *Remote_eq_cm1* = 2 (c(−1) ratio −0.1) 0 1 *Remote_eq_cm1* = 1 (c(−1) ratio −0.05) 0 0 *Remote_eq_cm1* = 0 (c(−1) ratio 0)	R/W

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Table 45–90ab—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.500.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Local_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Local_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Local_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Local_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Local_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Local_eq_c1* = 0 (c(1) ratio 0)	R/W
1.500.1:0	Pre-cursor local setting	1 0 1 1 *Local_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Local_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Local_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Local_eq_cm1* = 0 (c(–1) ratio 0)	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.116d.1 Request flag (1.500.15)

The value of this bit indicates the value of the variable *Request_flag* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This indicates whether the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip device is issuing a request to change the remote transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.116d.2 Post-cursor request (1.500.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to 1, this value indicates the ratio of the post-cursor coefficient c(1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction.

45.2.1.116d.3 Pre-cursor request (1.500.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to 1, this value indicates the ratio of the pre-cursor coefficient c(–1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction.

45.2.1.116d.4 Post-cursor remote setting (1.500.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient c(1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and

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120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.116d.5 Pre-cursor remote setting (1.500.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient c(−1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and 120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.116d.6 Post-cursor local setting (1.500.4:2)

The value of these bits sets the variable *Local_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.2 and 120D.3.2.3), which controls the weight of the transmitter equalization post-cursor coefficient c(1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.116d.7 Pre-cursor local setting (1.500.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and 120D.3.1.2), which controls the weight of the transmitter equalization pre-cursor coefficient c(−1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.116e 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 1 through lane 15 registers (Registers 1.501 through 1.515)

The 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 1 through lane 15 registers are defined similarly to register 1.500 (which is used for lane 0, see 45.2.1.116d) but for lanes 1 through 15, respectively. The transmitter, receive direction, is the transmitter that sends data towards the MAC.

45.2.1.116f 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register (Register 1.516)

The assignment of bits in the 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register is shown in Table 45–90ac. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

45.2.1.116f.1 Request flag (1.516.15)

The value of this bit indicates the value of the variable *Request_flag* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This indicates whether the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip device is issuing a request to change the remote transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or

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Table 45–90ac—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.516.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.516.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Requested_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Requested_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Requested_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Requested_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Requested_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Requested_eq_c1* = 0 (c(1) ratio 0)	RO
1.516.11:10	Pre-cursor request	11 10 1 1 *Requested_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Requested_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Requested_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Requested_eq_cm1* = 0 (c(–1) ratio 0)	RO
1.516.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Remote_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Remote_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Remote_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Remote_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Remote_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Remote_eq_c1* = 0 (c(1) ratio 0)	R/W
1.516.6:5	Pre-cursor remote setting	6 5 1 1 *Remote_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Remote_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Remote_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Remote_eq_cm1* = 0 (c(–1) ratio 0)	R/W
1.516.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Local_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Local_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Local_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Local_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Local_eq_c1* = 1 (c(1) ratio–0.05) 0 0 0 *Local_eq_c1* = 0 (c(1) ratio 0)	R/W
1.516.1:0	Pre-cursor local setting	1 0 1 1 *Local_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Local_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Local_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Local_eq_cm1* = 0 (c(–1) ratio 0)	R/W

[a]R/W = Read/Write, RO = Read only

400GAUI-n receiver in the transmit direction is not present in the package, then the value returned for this bit should be zero.

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45.2.1.116f.2 Post-cursor request (1.516.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to 1, this value indicates the ratio of the post-cursor coefficient c(1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction.

45.2.1.116f.3 Pre-cursor request (1.516.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to 1, this value indicates the ratio of the pre-cursor coefficient c(−1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction.

45.2.1.116f.4 Post-cursor remote setting (1.516.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient c(1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.116f.5 Pre-cursor remote setting (1.516.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient c(−1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.116f.6 Post-cursor local setting (1.516.4:2)

The value of these bits sets the variable *Local_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2), which controls the weight of the transmitter equalization post-cursor coefficient c(1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.116f.7 Pre-cursor local setting (1.516.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2), which controls the weight of the transmitter equalization pre-cursor coefficient c(−1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n_x or 400GAUI-n transmitter in the transmit direction is not present in the package, then these bits have no effect.

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45.2.1.116g 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 15 registers (Registers 1.517 through 1.531)

The 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 15 registers are defined similarly to register 1.516 (which is used for lane 0, see 45.2.1.116f) but for lanes 1 through 15, respectively. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

Insert 45.2.1.116h to 45.2.1.116n after 45.2.1.116g (as inserted by IEEE Std 802.3bs-201x) as follows:

45.2.1.116h PMA precoder control down Tx (Register 1.600)

The assignment of bits in the PMA precoder control down Tx register is shown in Table 45–90ad.

Table 45–90ad—PMA precoder control down Tx register bit definitions

Bit(s)	Name	Description	R/W[a]
1.600.15:4	Reserved	Value always 0	RO
1.600.3	Lane 3 down transmitter precoder enable	1 = Lane 3 down Tx precoder enabled 0 = Lane 3 down Tx precoder disabled	RW
1.600.2	Lane 2 down transmitter precoder enable	1 = Lane 2 down Tx precoder enabled 0 = Lane 2 down Tx precoder disabled	RW
1.600.1	Lane 1 down transmitter precoder enable	1 = Lane 1 down Tx precoder enabled 0 = Lane 1 down Tx precoder disabled	RW
1.600.0	Lane 0 down transmitter precoder enable	1 = Lane 0 down Tx precoder enabled 0 = Lane 0 down Tx precoder disabled	RW

[a]R/W = Read/Write, RO = Read only

45.2.1.116h.1 PMA precoder down Tx enable lane 3 (1.600.3)

This bit enables the lane 3 down Tx precoder.

45.2.1.116h.2 PMA precoder down Tx enable lane 2 (1.600.2)

This bit enables the lane 2 down Tx precoder.

45.2.1.116h.3 PMA precoder down Tx enable lane 1 (1.600.1)

This bit enables the lane 1 down Tx precoder.

45.2.1.116h.4 PMA precoder down Tx enable lane 0 (1.600.0)

This bit enables the lane 0 down Tx precoder.

45.2.1.116i PMA precoder control down Rx (Register 1.601)

The assignment of bits in the precoder control down Rx register is shown in Table 45–90ae.

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Table 45–90ae—PMA precoder control down Rx register bit definitions

Bit(s)	Name	Description	R/W[a]
1.601.15:4	Reserved	Value always 0	RO
1.601.3	Lane 3 down receiver precoder enable	1 = Lane 3 down Rx precoder enabled 0 = Lane 3 down Rx precoder disabled	RW
1.601.2	Lane 2 down receiver precoder enable	1 = Lane 2 down Rx precoder enabled 0 = Lane 2 down Rx precoder disabled	RW
1.601.1	Lane 1 down receiver precoder enable	1 = Lane 1 down Rx precoder enabled 0 = Lane 1 down Rx precoder disabled	RW
1.601.0	Lane 0 down receiver precoder enable	1 = Lane 0 down Rx precoder enabled 0 = Lane 0 down Rx precoder disabled	RW

[a]R/W = Read/Write, RO = Read only

45.2.1.116i.1 PMA precoder down Rx enable lane 3 (1.601.3)

This bit enables the lane 3 down Rx precoder.

45.2.1.116i.2 PMA precoder down Rx enable lane 2 (1.601.2)

This bit enables the lane 2 down Rx precoder.

45.2.1.116i.3 PMA precoder down Rx enable lane 1 (1.601.1)

This bit enables the lane 1 down Rx precoder.

45.2.1.116i.4 PMA precoder down Rx enable lane 0 (1.601.0)

This bit enables the lane 0 down Rx precoder.

45.2.1.116j PMA precoder control up Tx (Register 1.602)

The assignment of bits in the precoder control up Tx register is shown in Table 45–90af.

Table 45–90af—PMA precoder control up Tx register bit definitions

Bit(s)	Name	Description	R/W[a]
1.602.15:2	Reserved	Value always 0	RO
1.602.1	Lane 1 up transmitter precoder enable	1 = Lane 1 up Tx precoder enabled 0 = Lane 1 up Tx precoder disabled	RW
1.602.0	Lane 0 up transmitter precoder enable	1 = Lane 0 up Tx precoder enabled 0 = Lane 0 up Tx precoder disabled	RW

[a]R/W = Read/Write, RO = Read only

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45.2.1.116j.1 PMA precoder up Tx enable lane 1 (1.602.1)

This bit enables the lane 1 up Tx precoder.

45.2.1.116j.2 PMA precoder up Tx enable lane 0 (1.602.0)

This bit enables the lane 0 up Tx precoder.

45.2.1.116k PMA precoder control up Rx (Register 1.603)

The assignment of bits in the precoder control up Rx register is shown in Table 45–90ag.

Table 45–90ag—PMA precoder control up Rx register bit definitions

Bit(s)	Name	Description	R/W[a]
1.603.15:2	Reserved	Value always 0	RO
1.603.1	Lane 1 up receiver precoder enable	1 = Lane 1 up Rx precoder enabled 0 = Lane 1 up Rx precoder disabled	RW
1.603.0	Lane 0 up receiver precoder enable	1 = Lane 0 up Rx precoder enabled 0 = Lane 0 up Rx precoder disabled	RW

[a]R/W = Read/Write, RO = Read only

45.2.1.116k.1 PMA precoder up Rx enable lane 1 (1.603.1)

This bit enables the lane 1 up Rx precoder.

45.2.1.116k.2 PMA precoder up Rx enable lane 0 (1.603.0)

This bit enables the lane 0 up Rx precoder.

45.2.1.116l PMA precoder request status (Register 1.604)

The assignment of bits in the precoder request status register is shown in Table 45–90ah.

Table 45–90ah—PMA precoder request status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.604.15:2	Reserved	Value always 0	RO
1.604.1	precoder_request_status_1	1 = Lane 1 precoding requested 0 = Lane 1 precoding not requested	RO
1.604.0	precoder_request_status_0	1 = Lane 0 precoding requested 0 = Lane 0 precoding not requested	RO

[a]R/W = Read/Write, RO = Read only

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45.2.1.116l.1 PMA precoder request status lane 1 (1.604.1)

This bit indicates the lane 1 precoder request status.

45.2.1.116l.2 PMA precoder request status lane 0 (1.604.0)

This bit indicates the lane 0 precoder request status.

45.2.1.116m PMA precoder request down (Register 1.605)

The assignment of bits in the precoder request down register is shown in Table 45–90ai.

Table 45–90ai—PMA precoder request down register bit definitions

Bit(s)	Name	Description	R/W[a]
1.605.15:2	Reserved	Value always 0	RO
1.605.1	precoder_request_down_1	1 = Lane 1 precoder down requested 0 = Lane 1 precoder down not requested	RW
1.605.0	precoder_request_down_0	1 = Lane 0 precoder down requested 0 = Lane 0 precoder down not requested	RW

[a]R/W = Read/Write, RO = Read only

45.2.1.116m.1 PMA precoder request down lane 1 (1.605.1)

This bit enables the request of precoding in the down direction for lane 1.

45.2.1.116m.2 PMA precoder request down lane 0 (1.605.0)

This bit enables the request of precoding in the down direction for lane 0.

45.2.1.116n PMA precoder request up (Register 1.606)

The assignment of bits in the precoder request up register is shown in Table 45–90aj.

Table 45–90aj—PMA precoder request up register bit definitions

Bit(s)	Name	Description	R/W[a]
1.606.15:2	Reserved	Value always 0	RO
1.606.1	precoder_request_up_1	1 = Lane 1 precoder up requested 0 = Lane 1 precoder up not requested	RW
1.606.0	precoder_request_up_0	1 = Lane 0 precoder up requested 0 = Lane 0 precoder up not requested	RW

[a]R/W = Read/Write, RO = Read only

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45.2.1.116n.1 PMA precoder request up lane 1 (1.606.1)

This bit enables the request of precoding in the up direction for lane 1.

45.2.1.116n.2 PMA precoder request up lane 0 (1.606.0)

This bit enables the request of precoding in the up direction for lane 0.

Insert 45.2.1.118a after 45.2.1.118 as follows:

45.2.1.118a BASE-R PAM4 PMD training LP control registers, lanes 0 through 3 (Register 1.1120 through 1.1123)

The BASE-R PAM4 PMD training LP control registers, lanes 0 through 3, reflect the contents of the first 16-bit word of the training frame most recently received from the control channel for each lane. Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123.

The assignment of bits in the BASE-R PAM4 PMD training LP control registers is shown in Table 45–90ak.

Table 45–90ak—BASE-R PAM4 PMD training LP control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1120.15:4]	Reserved	Value always 0	RO
1.1120.13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control	RW
1.1120.11:10	Reserved	Value always 0	RO
1.1120.9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RW
1.1120.7:5	Reserved	Value always 0	RO
1.1120.4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RW
1.1120.1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold	RW

[a]R/W = Read/Write, RO = Read only

Normally the bits in this register are read only; however, when training is disabled the registers become writeable.

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Insert 45.2.1.119a after 45.2.1.119 as follows:

45.2.1.119a BASE-R PAM4 PMD training LP status registers, lanes 0 through 3 (Register 1.1220 through 1.1223)

The BASE-R PAM4 PMD training LP status registers, lanes 0 through 3, reflect the contents of the second 16-bit word of the training frame most recently received from the control channel for each lane. Lane 0 maps to register 1.1220, lane 1 maps to register 1.1221, lane 2 maps to register 1.1222, and lane 3 maps to register 1.1223.

The assignment of bits in the BASE-R PAM4 PMD training LP status registers is shown in Table 45–90al.

Table 45–90al—BASE-R PAM4 PMD training LP status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1220.15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue	RO
1.1220.14:12	Reserved	Value always 0	RO
1.1220.11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RO
1.1220.9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified	RO
1.1220.8	Initial condition status	1 = Updated 0 = Not updated	RO
1.1220.7	Parity	Even parity bit	RO
1.1220.6	Reserved	Value always 0	RO
1.1220.5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RO
1.1220.2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated	RO

[a]R/W = Read/Write, RO = Read only

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Insert 45.2.1.120a after 45.2.1.120 as follows:

45.2.1.120a BASE-R PAM4 PMD training LD control registers, lanes 0 through 3 (Register 1.1320 through 1.1323)

The BASE-R PAM4 PMD training LD control registers, lanes 0 through 3, reflect the contents of the first 16-bit word of the outgoing training frame for each lane. Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, and lane 3 maps to register 1.1323.

The assignment of bits in the BASE-R PAM4 PMD training LP control registers is shown in Table 45–90am.

Table 45–90am—BASE-R PAM4 PMD training LD control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1320.15:41	Reserved	Value always 0	RO
1.1320.13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control	RW
1.1320.11:10	Reserved	Value always 0	RO
1.1320.9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RW
1.1320.7:5	Reserved	Value always 0	RO
1.1320.4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RW
1.1320.1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold	RW

[a]R/W = Read/Write, RO = Read only

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Insert 45.2.1.121a after 45.2.1.121 as follows:

45.2.1.121a BASE-R PAM4 PMD training LD status registers, lanes 0 through 3 (Register 1.1420 through 1.1423)

The BASE-R PAM4 PMD training LD status registers, lanes 0 through 3, reflect the contents of the second 16-bit word of the outgoing training frame for each lane. Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, and lane 3 maps to register 1.1423.

The assignment of bits in the BASE-R PAM4 PMD training LD status registers is shown in Table 45–90an.

Table 45–90an—BASE-R PAM4 PMD training LD status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1420.15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue	RO
1.1420.14:12	Reserved	Value always 0	RO
1.1420.11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RO
1.1420.9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified	RO
1.1420.8	Initial condition status	1 = Updated 0 = Not updated	RO
1.1420.7	Parity	Even parity bit	RO
1.1420.6	Reserved	Value always 0	RO
1.1420.5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RO
1.1420.2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated	RO

[a]R/W = Read/Write, RO = Read only

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45.2.1.124 PRBS pattern testing control (Register 1.1501)

Change the last four sentences of 45.2.1.124 (as inserted by IEEE Std 802.3bs-201x) as follows:

For the 50GBASE-R, 100GBASE-R PAM4, 200GBASE-R, and 400GBASE-R PMAs, the assertion of register 1.1501 bit 13 operates in conjunction with register 1.1501 bits 3 and 1. If neither bit is asserted, then register 1.1501 bit 13 has no effect. Also for the 50GBASE-R, 100GBASE-R PAM4, 200GBASE-R, and 400GBASE-R PMAs, the assertion of register 1.1501 bit 14 operates in conjunction with register 1.1501 bit 3. If bit 1.1501.3 is not asserted, then register 1.1501 bit 14 has no effect. For other PMA/PMD types register 1.1501 bits 13 and 14 have no effect.

45.2.3 PCS registers

45.2.3.1 PCS control 1 register (Register 3.0)

Change the row for bits 3.0.5:2 in Table 45–120 (as modified by IEEE Std 802.3bz-2016) as follows (unchanged rows not shown):

Table 45–120—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
3.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 1 = Reserved 1 0 1 0 = 400 Gb/s 1 0 0 1 = 200 Gb/s 1 0 0 0 = 5 Gb/s 0 1 1 1 = 2.5 Gb/s 0 1 1 0 = 50 Gb/s ~~Reserved~~ 0 1 0 1 = 25 Gb/s 0 1 0 0 = 100 Gb/s 0 0 1 1 = 40 Gb/s 0 0 1 0 = 10/1 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
…			

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

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45.2.3.2 PCS status 1 register (Register 3.1)

45.2.3.2.7 PCS receive link status (3.1.2)

Change the third sentence of 45.2.3.2.7 (as modified by IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016 and IEEE Std 802.3bs-201x) as follows:

When a 10/25/40/50/100/200/400GBASE-R, 10GBASE-W, or any MultiGBASE-T mode of operation is selected for the PCS using the PCS type selection field (3.7.2:0), this bit is a latching low version of bit 3.32.12.

45.2.3.4 PCS speed ability (Register 3.4)

Change the row for 3.4.5 in Table 45–122 (as inserted by IEEE Std 802.3bz-2016) as follows (unchanged rows not shown):

Table 45–122—PCS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
...			
3.4.5	~~Reserved~~ 50G capable	~~Value always 0~~ 1 = PCS is capable of operating at 50 Gb/s 0 = PCS is not capable of operating at 50 Gb/s	RO
...			

[a]RO = Read only

Insert 45.2.3.4.5a after 45.2.3.4.5 (as inserted by IEEE Std 802.3by-2016) as follows:

45.2.3.4.5a 50G capable (3.4.5)

When read as a one, bit 3.4.5 indicates that the PCS is able to operate at a data rate of 50 Gb/s. When read as a zero, bit 3.4.5 indicates that the PCS is not able to operate at a data rate of 50 Gb/s.

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45.2.3.6 PCS control 2 register (Register 3.7)

Change Table 45–123 (as modified by IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, IEEE Std 802.3bz-2016, and IEEE Std 802.3bs-201x) as follows:

Table 45–123—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.7.15:4	Reserved	Value always 0	RO
3.7.3:0	PCS type selection	3 2 1 0 1 1 1 x = reserved 1 1 0 1 = Select 400GBASE-R PCS type 1 1 0 0 = Select 200GBASE-R PCS type 1 0 1 1 = Select 5GBASE-T PCS type 1 0 1 0 = Select 2.5GBASE-T PCS type 1 0 0 1 = Select 25GBASE-T PCS type 1 0 0 0 = Select 50GBASE-R PCS type ~~reserved~~ 0 1 1 1 = Select 25GBASE-R PCS type 0 1 1 0 = Select 40GBASE-T PCS type 0 1 0 1 = Select 100GBASE-R PCS type 0 1 0 0 = Select 40GBASE-R PCS type 0 0 1 1 = Select 10GBASE-T PCS type 0 0 1 0 = Select 10GBASE-W PCS type 0 0 0 1 = Select 10GBASE-X PCS type 0 0 0 0 = Select 10GBASE-R PCS type	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.7 PCS status 2 register (Register 3.8)

Change row for 3.8.8 in Table 45–124a (as modified by IEEE Std 802.3bq-2016) as follows (unchanged rows not shown):

Table 45–124 —PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.8.8	~~Reserved~~ 50GBASE-R capable	~~Value always 0~~ 1 = PCS is able to support 50GBASE-R PCS type 0 = PCS is not able to support 50GBASE-R PCS type	RO

[a]RO = Read only

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Insert 45.2.3.7.3ab after 45.2.3.7.3aa (as inserted by IEEE Std 802.3bq-2016) as follows:

45.2.3.7.3ab 50GBASE-R capable (3.8.8)

When read as a one, bit 3.8.8 indicates that the PCS is able to support the 50GBASE-R PCS type. When read as a zero, bit 3.8.8 indicates that the PCS is not able to support the 50GBASE-R PCS type.

45.2.3.9 EEE control and capability 1 (Register 3.20)

Change the reserved row for 3.20.15:14 in Table 45–125 as follows (unchanged rows not shown):

Table 45–125—EEE control and capability 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.20.15:~~14~~	Reserved	Value always 0	RO
3.20.14	50GBASE-R fast wake	1 = EEE fast wake is supported for 50GBASE-R 0 = EEE fast wake is not supported for 50GBASE-R	RO
…			

[a]R/W = Read/Write, RO = Read only

Insert 45.2.3.9.a before 45.2.3.9.1 as follows:

45.2.3.9.a 50GBASE-R EEE fast wake supported (3.20.14)

If the PCS supports EEE fast wake operation for 50GBASE-R, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.13 BASE-R and MultiGBASE-T PCS status 1 register (Register 3.32)

45.2.3.13.1 BASE-R and MultiGBASE-T receive link status (3.32.12)

Change the last sentence of 45.2.3.13.1 (as modified by IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, IEEE Std 802.3bz-2016, and IEEE Std 802.3bs-201x) as follows:

This bit is a reflection of the PCS_status variable defined in 49.2.14.3 for 10/25GBASE-R, in 126.3.7.1 for 2.5GBASE-T and 5GBASE-T, in 55.3.7.1 for 10GBASE-T, in 113.3.7.1 for 25GBASE-T and 40GBASE-T, in 82.3.1 for 40/50/100GBASE-R, and in 119.3 for 200/400GBASE-R.

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45.2.3.13.4 BASE-R and MultiGBASE-T PCS high BER (3.32.1)

Change third sentence of 45.2.3.13.4 (as modified by IEEE Std 802.3by-2016) as follows:

This bit is a direct reflection of the state of the hi_ber variable in the 64B/66B state diagram and is defined in 49.2.13.2.2 for 10/25GBASE-R and in 82.2.19.2.2 for 40/50/100GBASE-R.

45.2.3.13.5 BASE-R and MultiGBASE-T PCS block lock (3.32.0)

Change third sentence of 45.2.3.13.5 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

This bit is a direct reflection of the state of the block_lock variable in the 64B/66B state diagram and is defined in 49.2.13.2.2 for 5/10/25GBASE-R and in 82.2.19.2.2 for 40/50/100GBASE-R.

45.2.3.14 BASE-R and MultiGBASE-T PCS status 2 register (Register 3.33)

45.2.3.14.1 Latched block lock (3.33.15)

Change 45.2.3.14.1 (as modified by IEEE Std 802.3bq-2016 and IEEE Std 802.3cb-201x) as follows:

When read as a one, bit 3.33.15 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has achieved block lock. When read as a zero, bit 3.33.15 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has lost block lock.

The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 5/10/25/40/50/100GBASE-R and MultiGBASE-T PCS block lock status bit (3.32.0).

45.2.3.14.2 Latched high BER (3.33.14)

Change 45.2.3.14.2 (as modified by IEEE Std 802.3bq-2016, IEEE Std 802.3by-2016, and IEEE Std 802.3cb-201x) as follows:

When read as a one, bit 3.33.14 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has detected a high BER. When read as a zero, bit 3.33.14 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has not detected a high BER.

The latched high BER bit shall be implemented with latching high behavior.

This bit is a latching high version of the 5/10/25/40/50/100GBASE-R and MultiGBASE-T PCS high BER status bit (3.32.1).

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45.2.3.14.3 BER(3.33.13:8)

Change first sentence of 45.2.3.14.3 (as modified by IEEE Std 802.3bq-2016, IEEE Std 802.3by-2016, and IEEE Std 802.3cb-201x) as follows:

The BER counter is a six bit count as defined by the ber_count variable in 49.2.14.2 and 82.2.19.2.4 for 5/10/25/40/50/100GBASE-R and defined by counter lfer_count in 55.3.6.2 for 10GBASE-T and in 113.3.6.2.2 for 25GBASE-T and 40GBASE-T.

45.2.3.14.4 Errored blocks (3.33.7:0)

Change first sentence of 45.2.3.14.4 (as modified by IEEE Std 802.3bq-2016, IEEE Std 802.3by-2016, and IEEE Std 802.3cb-201x) as follows:

The errored blocks counter is an eight bit count defined by the errored_block_count counter specified in 49.2.14.2 for 5/10/25GBASE-R, in 82.3.1 for 40/50/100GBASE-R and defined by counter errored_block_count in 55.3.6.2 for 10GBASE-T and in 113.3.6.2.2 for 25GBASE-T and 40GBASE-T.

45.2.3.17 BASE-R PCS test-pattern control register (Register 3.42)

Change the fifth sentence of 45.2.3.17 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

Scrambled idle test patterns are defined for 25/40/50/100/200/400GBASE-R PCS only.

45.2.7 Auto-Negotiation registers

Change the reserved row 7.49 through 7.59 in Table 45–200 as follows (unchanged rows not shown):

Table 45–200—Auto-Negotiation MMD registers

Register address	Register name	Subclause
7.49	Backplane Ethernet, BASE-R copper status 2	45.2.7.12a
7.4950 through 7.59	Reserved	

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45.2.7.12 Backplane Ethernet, BASE-R copper status (Register 7.48)

Change the title and text of 45.2.7.12.2 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

45.2.7.12.2 Negotiated Port Type (7.48.1, 7.48.2, 7.48.3, 7.48.5, 7.48.6, 7.48.8, 7.48.9, 7.48.10, 7.48.11, 7.48.12, 7.48.13, 7.48.14, 7.48.15, 7.49.0, 7.49.1, 7.49.2)

When the AN process has been completed as indicated by the AN complete bit, these bits in register 7.48 and register 7.49 indicate the negotiated port type.

Insert 45.2.7.12a after 45.2.7.12 as follows

45.2.7.12a Backplane Ethernet, BASE-R copper status 2 (Register 7.49)

The assignment of bits in the Backplane Ethernet, BASE-R copper status 2 register is shown in Table 45–209a.

Table 45–209a—Backplane Ethernet, BASE-R copper status 2 register (Register 7.49) bit definitions

Bit(s)	Name	Description	RO[a]
7.49.15:3	Reserved	Value always 0	RO
7.49.2	200GBASE-KR4 or 200GBASE-CR4	1 = PMA/PMD is negotiated to perform 200GBASE-KR4 or 200GBASE-CR4 0 = PMA/PMD is not negotiated to perform 200GBASE-KR4 or 200GBASE-CR4	RO
7.49.1	100GBASE-KR2 or 100GBASE-CR2	1 = PMA/PMD is negotiated to perform 100GBASE-KR2 or 100GBASE-CR2 0 = PMA/PMD is not negotiated to perform 100GBASE-KR2 or 100GBASE-CR2	RO
7.49.0	50GBASE-KR or 50GBASE-CR	1 = PMA/PMD is negotiated to perform 50GBASE-KR or 50GBASE-CR 0 = PMA/PMD is not negotiated to perform 50GBASE-KR or 50GBASE-CR	RO

[a]RO = Read only

45.2.7.12a.1 Negotiated Port Type

See 45.2.7.12.2.

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45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) interface[1]

45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface

45.5.3.3 PMA/PMD management functions

Insert the following row at the end of the table in (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] N/A [ ]

[1] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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69. Introduction to Ethernet operation over electrical backplanes

69.1 Overview

69.1.1 Scope

Change the second paragraph of 69.1.1 (as modified by IEEE Std 802.3by-201x and IEEE Std 802.3cb-201x) as follows:

Backplane Ethernet supports the IEEE 802.3 full duplex MAC operating at 1000 Mb/s, 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, or 100 Gb/s providing a bit error ratio (BER) better than or equal to 10^{-12} at the MAC/PLS service interface or 200 Gb/s providing a BER better than or equal to 10^{-13} at the MAC/PLS service interface. The following Physical Layers are supported:

Change the list after the second paragraph of 69.1.1 as follows (some unmodified list items are not shown):

- ...
- 40GBASE-KR4 for 40 Gb/s operation over four lanes
- 50GBASE-KR for 50 Gb/s operation over one lane
- 100GBASE-KR4 and 100GBASE-KP4 for 100 Gb/s operation over four lanes
- 100GBASE-KR2 for 100 Gb/s operation over two lanes
- 200GBASE-KR4 for 200 Gb/s operation over four lanes

69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model

Change the first paragraph of 69.1.2 (as modified by IEEE Std 802.3by-201x and IEEE Std 802.3cb-201x) as follows:

Backplane Ethernet couples the IEEE 802.3 MAC to a family of Physical Layers defined for operation over electrical backplanes. The relationships among Backplane Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 69–1, Figure 69–1a, Figure 69–2, ~~and~~ Figure 69–2a, and Figure 69–4.

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Insert Figure 69–4 after Figure 69–2a (as inserted by IEEE Std 802.3cb-201x) as follows:

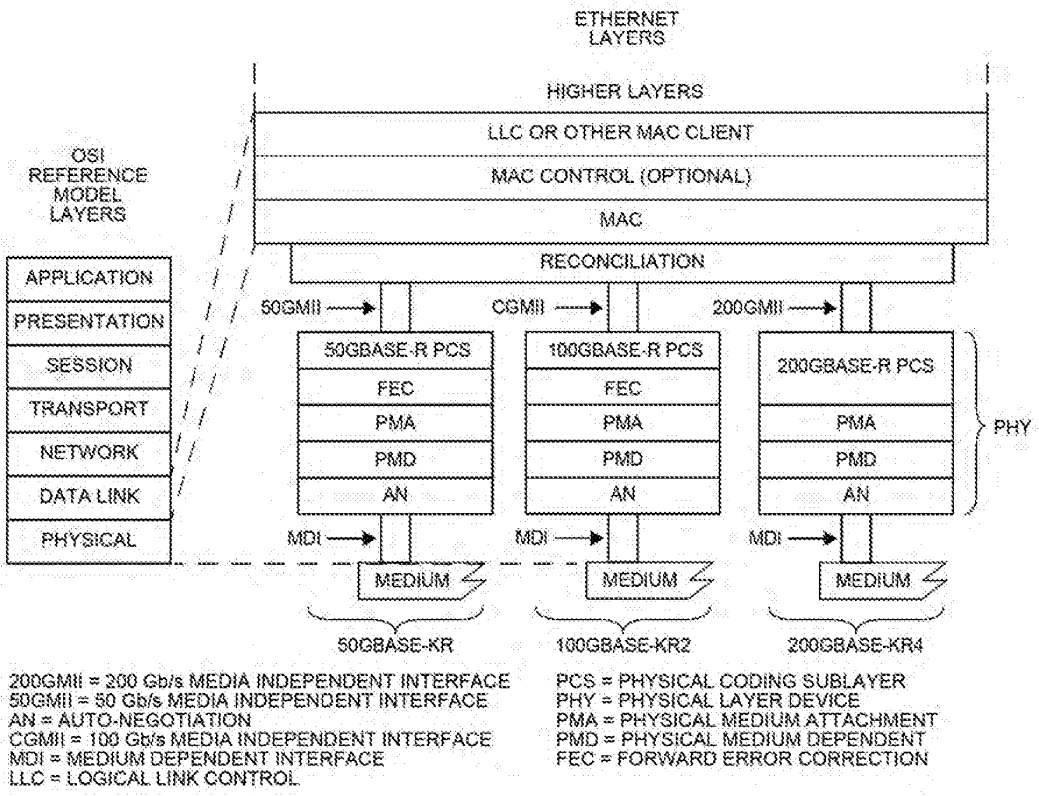


Figure 69–4—Architectural positioning of 50 Gb/s, 100 Gb/s, and 200 Gb/s PAM4 Backplane Ethernet

Change the lettered list after Figure 69–2 (as modified by IEEE Std 802.3by-201x and IEEE Std 802.3cb-201x) as follows (some unchanged rows not shown):

f) The PMA service interface, which, when physically implemented as 25GAUI (25 Gigabit Attachment Unit Interface) or as 50GAUI-1 (50 Gb/s one-lane Attachment Unit Interface) at an observable interconnection port, uses a serial data path as specified in Annex 109A or Annex 135F, respectively.

g) The PMA service interface, which, when physically implemented as LAUI-2/50GAUI-2 (50 Gb/s two-lane Attachment Unit Interface) or as 100GAUI-2 (100 Gb/s two-lane Attachment Unit Interface) at an observable interconnection port, uses a serial two-lane path as specified in Annex 135B, Annex 135D, or Annex 135F, respectively.

h) The PMA service interface, which, when physically implemented as XLAUI (40 Gb/s Attachment Unit Interface), ~~or~~ as CAUI-4 (100 Gb/s four-lane Attachment Unit Interface), or as 200GAUI-4 (200 Gb/s four-lane Attachment Unit Interface) at an observable interconnection port, uses a four-lane data path as specified in Annex 83A, ~~or~~ Annex 83D, or Annex 120D respectively.

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i) The PMA service interface, which, when physically implemented as 200GAUI-8 (200 Gb/s eight-lane Attachment Unit Interface) at an observable interconnection port, uses an eight-lane data path as specified in Annex 120B.

j) The PMA service interface, which, when physically implemented as CAUI-10 (100 Gb/s ten-lane Attachment Unit Interface) at an observable interconnection port, uses a ten-lane data path as specified in Annex 83A.

k) The MDIs for 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KR, 25GBASE-KR, ~~and~~ 25GBASE-KR-S, and 50GBASE-KR use a serial data path ~~while the MDIs for 10GBASE-KX4, 40GBASE-KR4, 100GBASE-KR4, and 100GBASE-KP4 use a four-lane data path~~.

l) The MDI for 100GBASE-KR2 uses a two-lane data path.

m) The MDIs for 10GBASE-KX4, 40GBASE-KR4, 100GBASE-KR4, 100GBASE-KP4, and 200GBASE-KR4 use a four-lane data path.

69.2 Summary of Backplane Ethernet Sublayers

69.2.1 Reconciliation sublayer and media independent interfaces

Change 69.2.1 (as modified by IEEE Std 802.3by-201x) as follows:

The Clause 35 RS and GMII, the Clause 46 RS and XGMII, the Clause 106 RS and 25GMII, ~~and~~ the Clause 81 RS, XLGMII, and CGMII, the Clause 132 RS and 50GMII, and the Clause 117 RS and 200GMII are employed for the same purpose in Backplane Ethernet, that being the interconnection between the MAC sublayer and the PHY.

69.2.3 Physical Layer signaling systems

Insert the following new paragraph after the fourth paragraph in 69.2.3 (as inserted by IEEE Std 802.3cb-201x):

Backplane Ethernet also specifies 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4. The 50GBASE-KR embodiment employs the PCS defined in Clause 133, the RS-FEC defined in Clause 134, the PMA defined in Clause 135, and the PMD defined in Clause 137, and specifies 50 Gb/s operation using 4-level PAM over one differential path in each direction. The 100GBASE-KR2 embodiment employs the PCS defined in Clause 82, the RS-FEC defined in Clause 91, the PMA defined in Clause 135, and the PMD defined in Clause 137, and specifies 100 Gb/s operation using 4-level PAM over two differential paths in each direction. The 200GBASE-KR4 embodiment employs the PCS defined in Clause 119, the PMA defined in Clause 120, and the PMD defined in Clause 137, and specifies 200 Gb/s operation using 4-level PAM over four differential paths in each direction.

Change the last paragraph in 69.2.3 (as modified by IEEE Std 802.3by-201x and IEEE Std 802.3cb-201x) as follows:

Table 69–1, Table 69–1a, Table 69–2, ~~and~~ Table 69–2a, Table 69–2b, Table 69–2c, and Table 69–2d specify the correlation between nomenclature and clauses. A complete implementation conforming to one or more nomenclatures meets the requirements of the corresponding clauses.

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Insert Table 69–2b, Table 69–2c, and Table 69–2d after Table 69–2a (as inserted by IEEE Std 802.3cb-201x):

Table 69–2b—Nomenclature and clause correlation for 50 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause[a]									
	78	132		133	134	135	135A	135B	135C	137
	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	LAUI-2 C2C	50GAUI-2 C2C	50GAUI-1 C2C	50GBASE-KR PMD
50GBASE-KR	O	M	O	M	M	M	O	O	O	M

[a]O = Optional, M = Mandatory.

Table 69–2c—Nomenclature and clause correlation for 100 Gb/s two-lane Backplane Ethernet Physical Layers

Nomenclature	Clause[a]											
	78	81		82	83	83A	83D	91	135	135B	135D	137
	EEE	RS	100GMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10 C2C	CAUI-4 C2C	100GBASE-R RS-FEC	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-2 C2C	100GBASE-KR2 PMD
100GBASE-KR2	O	M	O	M	O	O	O	M	M	O	O	M

[a]O = Optional, M = Mandatory.

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Table 69–2d—Nomenclature and clause correlation for 200 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause[a]							
	78	117		119	128	128B	128D	137
	EEE	RS	200GMII	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-4 C2C	100GBASE-KR4 PMD
200GBASE-KR4	O	M	O	M	M	O	O	M

[a]O = Optional, M = Mandatory.

69.3 Delay constraints

Insert the following paragraph after the fourth paragraph of 69.3:

For 50GBASE-KR, normative delay specifications may be found in 132.1.4, 133.3, 135.5.4, and 137.5, and also referenced in 131.4.

Insert the following paragraphs after the sixth paragraph of 69.3:

For 100GBASE-KR2, normative delay specifications may be found in 81.1.4, 82.5, 135.5.4, and 137.5, and also referenced in 80.4.

For 200GBASE-KR4, normative delay specifications may be found in 117.1.4, 119.5, 120.5.4, and 137.5, and also referenced in 116.4.

69.5 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph of 69.5 (as modified by IEEE Std 802.3by-201x and IEEE Std 802.3cb-201x) as follows:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 70 through Clause 74, Clause 84, Clause 91, Clause 93, Clause 94, Clause 108, Clause 111, Clause 119, Clause 128, Clause 130, Clause 134, Clause 137, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

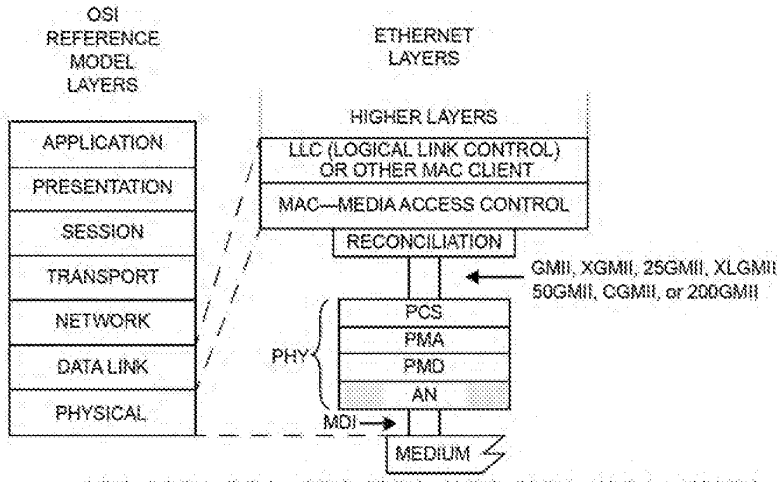
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73. Auto-Negotiation for backplane and copper cable assembly

73.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

Replace Figure 73–1 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) with the following:



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
25GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 73–1—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

73.3 Functional specifications

Change the third paragraph of 73.3 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

These functions shall comply with the state diagrams from Figure 73–9 through Figure 73–11. The Auto-Negotiation functions shall interact with the technology-dependent PHYs through the Technology-Dependent interface (see 73.9). Technology-Dependent PHYs are those supported by the Auto-Negotiation process (see Table 73–4)~~include 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KX4, 10GBASE-KR, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, 25GBASE-CR-S, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-KP4, 100GBASE-KR4, and 100GBASE-CR4~~.

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73.5 DME transmission

73.5.1 DME electrical specifications

Change the second paragraph of 73.5.1 as follows:

For any multi-lane PHY, DME pages shall be transmitted only on lane 0. The transmitters on other lanes should be disabled as specified in 71.6.7, 84.7.7, 85.7.7, 92.7.7, 93.7.7, ~~or~~ 94.3.6.7, 136.8.7, or 137.8.7.

73.6 Link codeword encoding

73.6.4 Technology Ability Field

Change Table 73–4 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

Table 73–4—Technology Ability Field encoding

Bit	Technology
A0	1000BASE-KX
A1	10GBASE-KX4
A2	10GBASE-KR
A3	40GBASE-KR4
A4	40GBASE-CR4
A5	100GBASE-CR10
A6	100GBASE-KP4
A7	100GBASE-KR4
A8	100GBASE-CR4
A9	25GBASE-KR-S or 25GBASE-CR-S
A10	25GBASE-KR or 25GBASE-CR
A11	2.5GBASE-KX
A12	5GBASE-KR
A13	50GBASE-KR or 50GBASE-CR
A14	100GBASE-KR2 or 100GBASE-CR2
A15	200GBASE-KR4 or 200GBASE-CR4
~~A13~~A16 through A22	Reserved for future technology

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Replace the third paragraph of 73.6.4 with a note and change the fourth and fifth paragraphs (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

~~For 25 Gb/s operation the same bits are used to advertise backplane and copper cable assembly operation. For other speeds, a PHY for operation over an electrical backplane (e.g., 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 100GBASE-KP4, 100GBASE-KR4) shall not be advertised simultaneously with a PHY for operation over a copper cable assembly (e.g., 40GBASE-CR4, 100GBASE-CR10, 100GBASE-CR4).~~

NOTE– Previous editions of this standard prohibited advertisement of PHYs that support operation over electrical backplanes with PHYs that support operation over copper cable assemblies.

25GBASE-KR-S abilities are a subset of 25GBASE-KR abilities, and likewise 25GBASE-CR-S abilities are a subset of 25GBASE-CR abilities. To allow interoperation between 25GBASE-KR-S and 25GBASE-KR PHY types, and between 25GBASE-CR-S and 25GBASE-CR PHY types, a device that supports 25GBASE-KR or 25GBASE-CR should advertise both A9 and A10 ability bits during auto-negotiation.

The fields A[22:16~~13~~] are reserved for future use. Reserved fields shall be sent as zero and ignored on receive.

73.7 Receive function requirements

73.7.1 DME page reception

Change 73.7.1 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:

To be able to detect the DME bits, the receiver should have the capability to receive DME signals sent with the electrical specifications of the PHY~~(1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KX4, 10GBASE-KR, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, 25GBASE-CR-S, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-KP4, 100GBASE-KR4, or 100GBASE-CR4)~~. The DME transmit signal level and receive sensitivity are specified in 73.5.1.

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73.7.6 Priority Resolution function

Change Table 73–5 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3cb-201x) as follows:.

Table 73–5—Priority Resolution

Priority	Technology	Capability
1	200GBASE-KR4 or 200GBASE-CR4	200 Gb/s 4 lane, highest priority
2	100GBASE-KR2 or 100GBASE-CR2	100 Gb/s 2 lane
3 ~~1~~	100GBASE-CR4	100 Gb/s 4 lane~~, highest priority~~
4 ~~2~~	100GBASE-KR4	100 Gb/s 4 lane
5 ~~3~~	100GBASE-KP4	100 Gb/s 4 lane
6 ~~4~~	100GBASE-CR10	100 Gb/s 10 lane
7	50GBASE-KR or 50GBASE-CR	50 Gb/s 1 lane
8 ~~5~~	40GBASE-CR4	40 Gb/s 4 lane
9 ~~6~~	40GBASE-KR4	40 Gb/s 4 lane
10 ~~7~~	25GBASE-KR or 25GBASE-CR	25 Gb/s 1 lane
11 ~~8~~	25GBASE-KR-S or 25GBASE-CR-S	25 Gb/s 1 lane, short reach
12 ~~9~~	10GBASE-KR	10 Gb/s 1 lane
13 ~~10~~	10GBASE-KX4	10 Gb/s 4 lane
14 ~~11~~	5GBASE-KR	5 Gb/s 1 lane
15 ~~12~~	2.5GBASE-KX	2.55 Gb/s 1 lane
16 ~~13~~	1000BASE-KX	1 Gb/s 1 lane, lowest priority

73.10 State diagrams and variable definitions

73.10.1 State diagram variables

Insert the following variables in the variable list by adding 50GR, 100GR, and 200GR at the appropriate place.

50GR; represents the 50GBASE-KR or 50GBASE-CR PMD.

100GR2; represents the 100GBASE-KR2 or 100GBASE-CR2 PMD.

200GR4; represents the 200GBASE-KR4 or 200GBASE-CR4 PMD.

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Insert the following entries in the single_link_ready status at the appropriate place and renumber the existing entries:

9) link_status_[50GR] = OK
14) link_status_[100GR2] = OK
15) link_status_[200GR4] = OK

73.10.2 State diagram timers

Change the link_fault_inhibit timer definition as follows:

link_fail_inhibit_timer

Timer for qualifying a link_status=FAIL indication or a link_status=OK indication when a specific technology link is first being established. A link will only be considered "failed" if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire within the timer values given in Table 73–7 ~~40 ms to 50 ms~~ after entering the AN LINK GOOD CHECK state ~~when the link is 1000BASE-KX or 10GBASE-KX4. Otherwise the The link_fail_inhibit_timer shall expire 500 ms to 510 ms after entering the AN LINK GOOD CHECK state~~.

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Change Table 73–7 (as modified by IEEE Std 802.3cb-201x) as follows:

Table 73–7—Timer min/max value summary

Parameter	Min	Value and tolerance	Max	Units
autoneg_wait_timer	25		50	ms
break_link_timer	60		75	ms
clock_detect_min_timer	4.8		6.2	ns
clock_detect_max_timer	6.6		8.0	ns
data_detect_min_timer	1.6		3.0	ns
data_detect_max_timer	3.4		4.8	ns
interval_timer		3.2 ± 0.01%		ns
link_fail_inhibit_timer (when the link is 50GBASE-KR, 50GBASE-CR, 100GBASE-KR2, 100GBASE-CR2, 200GBASE-KR4 or 200GBASE-CR4)	1.6		1.7	s
link_fail_inhibit_timer (when the link is 10GBASE-KR, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, 25GBASE-CR-S, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-KR4, 100GBASE-KP4, 100GBASE-CR4, or 100GBASE-CR10 ~~neither 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, nor 10GBASE-KX4~~)	500		510	ms
link_fail_inhibit_timer (when the link is 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, or 10GBASE-KX4)	40		50	ms
page_test_min_timer	305		330	ns
page_test_max_timer	350		375	ns

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73.11 Protocol implementation conformance statement (PICS) proforma for Clause 73, Auto-Negotiation for backplane and copper cable assembly[2]

73.11.4 PICS proforma tables for Auto-Negotiation for backplane and copper cable assembly

73.11.4.3 Link codeword encoding

Change table to delete PICS item LE18 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
~~LE18~~	~~Incompatible abilities~~	~~73.6.4~~	~~PHYs for operation over electrical backplane are not simultaneously advertised with PHYs for operation over copper cable~~	~~M~~	~~Yes [ ]~~

73.11.4.7 State diagrams and variable definitions

Change Table (as modified by IEEE Std 802.3cb-201x) as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
SD15	link_fail_inhibit_timer	73.10.2	The values in Table 73–7~~500 to 510 ms when the link is not 1000BASE-KX, 2.5GBASE-X, 5GBASE-R or 10GBASE-KX4 and 40 ms to 50 ms otherwise~~	M	Yes [ ]

[2]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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78. Energy-Efficient Ethernet (EEE)

78.1 Overview

78.1.4 PHY types optionally supporting EEE

Change Table 78–1 (as modified by IEEE Std 802.3bs-201x) as follows (some unmodified rows not shown):

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
...	...
40GBASE-ER4[b]	82, 83, 87
50GBASE-KR[b]	133, 134, 137
50GBASE-CR[b]	133, 134, 136
50GBASE-SR[b]	133, 134, 138
50GBASE-FR[b]	133, 134, 139
50GBASE-LR[b]	133, 134, 139
CAUI-4[a]	83D
100GBASE-KP4	82, 91, 94
100GBASE-KR4	82, 83, 91, 93
100GBASE-KR2[b]	82, 135, 137
100GBASE-CR10	82, 83, 85, 74
100GBASE-CR4	82, 83, 91, 92
100GBASE-CR2[b]	82, 135, 136
100GBASE-SR10[b]	82, 83, 86
100GBASE-SR4[b]	82, 83, 91, 95
100GBASE-SR2[b]	82, 135, 138
100GBASE-DR[b]	82, 135, 140
100GBASE-LR4[b]	82, 83, 88
100GBASE-ER4[b]	82, 83, 88
200GBASE-KR4[b]	119, 120, 137
200GBASE-CR4[b]	119, 120, 136
200GBASE-SR4[b]	119, 120, 138
200GBASE-DR4[b]	119, 120, 121
...	...

[a]25GAUI/XLAUI/CAUI-n shutdown is supported only when deep sleep is enabled for the associated PHY.
[b]The deep sleep mode of EEE is not supported for this PHY.

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78.5 Communication link access latency

Insert new row into Table 78–4 below the row for 40GBASE-KR4 (unmodified rows not shown):

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy\_shrink\_tx}$ (max) (μs)	$T_{phy\_shrink\_rx}$ (max) (μs)	$T_{w\_sys\_rx}$ (min) (μs)
…	…	…	…	…	…	…
50GBASE-R fast wake		0.34	0.3	0	0	0.25
…	…	…	…	…	…	…

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80. Introduction to 40 Gb/s and 100 Gb/s networks

80.1 Overview

80.1.3 Relationship of 40 Gigabit and 100 Gigabit Ethernet to the ISO OSI reference model

Change the second paragraph in 80.1.3 as follows:

While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The XLGMII and CGMII, which, when implemented as a logical interconnection port between the MAC sublayer and the Physical Layer (PHY), uses a 64-bit wide data path as specified in Clause 81.

b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.

c) The PMA service interface, which, when physically implemented as XL (40 Gb/s Attachment Unit Interface) or CAUI-4 and 100GAUI-4 (100 Gb/s four-lane Attachment Unit Interface) at an observable interconnection port, uses a 4 lane data path as specified in Annex 83A, Annex 83B, Annex 83D, or Annex 83E.

d) The PMA service interface, which, when physically implemented as CAUI-10 (100 Gb/s ten-lane Attachment Unit Interface) at an observable interconnection port, uses a 10 lane data path as specified in Annex 83A or Annex 83B.

e) The PMA service interface, which, when physically implemented as 100GAUI-2 (100 Gb/s two-lane Attachment Unit Interface) at an observable interconnection port, uses a 2-lane data path as specified in Annex 135F or Annex 135G.

f) The PMD service interface, which, when physically implemented as XLPPI (40 Gb/s Parallel Physical Interface) at an observable interconnection port, uses a 4 lane data path as specified in Annex 86A.

g) The PMD service interface, which, when physically implemented as CPPI (100 Gb/s Parallel Physical Interface) at an observable interconnection port, uses a 10 lane data path as specified in Annex 86A.

h) The MDIs as specified in Clause 89 for 40GBASE-FR and Clause 140 for 100GBASE-DR uses a single lane data path.

i) The MDIs as specified in Clause 85 for 40GBASE-CR4, in Clause 86 for 40GBASE-SR4, in Clause 87 for 40GBASE-LR4 and 40GBASE-ER4, in Clause 88 for 100GBASE-LR4 and 100GBASE-ER4, in Clause 92 for 100GBASE-CR4, and in Clause 95 for 100GBASE-SR4 all use a 4 lane data path.

j) The MDIs as specified in Clause 85 for 100GBASE-CR10, and in Clause 86 for 100GBASE-SR10 use a 10 lane data path.

k) Although there is no electrical or mechanical specification of the MDI for backplane Physical Layers, the PMDs as specified in Clause 84 for 40GBASE-KR4, in Clause 93 for 100GBASE-KR4, and in Clause 94 for 100GBASE-KP4 all use a 4 lane data path.

l) The MDIs as specified in Clause 136 for 100GBASE-CR2, in Clause 137 for 100GBASE-KR2, and in Clause 138 for 100GBASE-SR2 all use a 2-lane data path.

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80.1.4 Nomenclature

Change Table 80–1 as follows (some unchanged rows not shown):

Table 80–1—40 Gb/s and 100 Gb/s PHYs

Name	Description
…	…
40GBASE-ER4	40 Gb/s PHY using 40GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km (see Clause 87)
100GBASE-KR2	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 4-level pulse amplitude modulation over two lanes of an electrical backplane, with a total insertion loss up to 30 dB at 13.28 GHz (see Clause 137)
100GBASE-KR4	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 2-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 35 dB at 12.9 GHz (see Clause 93)
100GBASE-KP4	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 4-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 33 dB at 7 GHz (see Clause 94)
100GBASE-CR2	100 Gb/s PHY using 100GBASE-R encoding and Clause 91 RS-FEC and 4-level pulse amplitude modulation over two lanes of shielded balanced copper cabling, with reach up to at least 5 m (see Clause 136)
100GBASE-CR4	100 Gb/s PHY using 100GBASE-R encoding and Clause 91 RS-FEC over four lanes of shielded balanced copper cabling, with reach up to at least 5 m (see Clause 92)
100GBASE-CR10	100 Gb/s PHY using 100GBASE-R encoding over ten lanes of shielded balanced copper cabling, with reach up to at least 7 m (see Clause 85)
100GBASE-SR10	100 Gb/s PHY using 100GBASE-R encoding over ten lanes of multimode fiber, with reach up to at least 100 m (see Clause 86)
100GBASE-SR2	100 Gb/s PHY using 100GBASE-R encoding over two lanes of multimode fiber, with reach up to at least 100 m (see Clause 138)
100GBASE-SR4	100 Gb/s PHY using 100GBASE-R encoding over four lanes of multimode fiber, with reach up to at least 100 m (see Clause 95)
100GBASE-DR	100 Gb/s PHY using 100GBASE-R encoding over single-mode fiber, with reach up to at least 500 m (see Clause 140)
100GBASE-LR4	100 Gb/s PHY using 100GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 10 km (see Clause 88)
…	…

80.1.5 Physical Layer signaling systems

Change the first paragraph of 80.1.5 as follows:

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This standard specifies a family of Physical Layer implementations. Table 80–2, Table 80–3, ~~and~~ Table 80–4, and Table 80–4a specify the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures must meet the requirements of the corresponding clauses.

Change Table 80–3 as follows:

Table 80–3—Nomenclature and clause correlation (100GBASE copper)

Nomenclature	Clause[a]																		
	73	74	78	81		82	83	83A	83D	86	91	92	93	94	135	135D	135F	136	137
	Auto-Negotiation	BASE-R FEC	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10	CAUI-4	100GBASE-CR10 PMD	RS-FEC	100GBASE-CR4 PMD	100GBASE-KR4 PMD	100GBASE-KP4 PMD	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-2 C2C	100GBASE-CR2	100GBASE-KR2
100GBASE-KR2	M		O	M	O	M		O	O		M				M	O	O		M
100GBASE-KR4	M		O	M	O	M	M	O	O		M		M						
100GBASE-KP4	M		O	M	O	M	O	O	O		M			M					
100GBASE-CR2	M		O	M	O	M		O	O		M				M	O	O	M	
100GBASE-CR4	M		O	M	O	M	M	O	O		M	M							
100GBASE-CR10	M	O	O	M	O	M	M	O	O	M									

[a]O = Optional, M = Mandatory.

Change the title of Table 80–4 as follows:

Table 80–4—Nomenclature and clause correlation (100GBASE-R optical)

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Insert Table 80–4a after Table 80–4 as follows:

Table 80–4a—Nomenclature and clause correlation (100GBASE-P optical)

Nomenclature	Clause[a]															
	78	81		83	83A	83B	83D	83E	91	135	135D	135E	135F	135G	138	140
	EEE	RS	CGMII	100GBASE-R PMA	CAUI-10	CAUI-10	CAUI-4	CAUI-4	RS-FEC	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-4 C2M	100GAUI-2 C2C	100GAUI-2 C2M	100GBASE-SR2	100GBASE-DR
100GBASE-SR2	O	M	O	O	O	O	O	O	M	M	O	O	O	O	M	
100GBASE-DR	O	M	O	O	O	O	O	O	M	M	O	O	O	O		M

[a]O = Optional, M = Mandatory.

80.2 Summary of 40 Gigabit and 100 Gigabit Ethernet sublayers

80.2.1 Physical Coding Sublayer (PCS)

Change the text in 80.2.1 as follows:

The terms 40GBASE-R, 100GBASE-R, and 100GBASE-P refer to a specific family of Physical Layer implementations based upon the 64B/66B data coding method specified in Clause 82 and the PMA specifications defined in Clause 83, ~~or~~ Clause 84, or Clause 135. Clause 82 PCSs perform encoding (decoding) of data from (to) the XLGMII/CGMII to 64B/66B code blocks, distribute the data to multiple lanes, and transfer the encoded data to the PMA.

80.2.3 Forward Error Correction (FEC) sublayers

Change the first paragraph in 80.2.3 as follows:

A Forward Error Correction sublayer ~~is available for all 40GBASE-R and 100GBASE-R copper and backplane PHYs as well as 100GBASE-SR4. It~~ is optional for 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 PHYs and mandatory for 100GBASE-CR2, 100GBASE-CR4, 100GBASE-KR2, 100GBASE-KR4, 100GBASE-KP4, 100GBASE-SR2, ~~and~~ 100GBASE-SR4, and 100GBASE-DR PHYs. The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers.

80.2.4 Physical Medium Attachment (PMA) sublayer

Change the second paragraph of 80.2.4 as follows:

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The 40GBASE-R and 100GBASE-R PMA are specified in Clause 83. The PMA specific to the 100GBASE-KP4 PHY is specified in Clause 94. The PMA for other 100GBASE-P PHYs is specified in Clause 135.

80.2.5 Physical Medium Dependent (PMD) sublayer

Change the second paragraph of 80.2.5 as follows:

The 40GBASE-R, 100GBASE-R, and 100GBASE-P PMDs and their corresponding media are specified in Clause 84 through Clause 89, ~~and~~ Clause 92 through Clause 95, Clause 136 through Clause 138, and Clause 140.

80.2.6 Auto-Negotiation

Change the second paragraph of 80.2.6 as follows:

Clause 73 Auto-Negotiation is used by the 40 Gb/s and 100 Gb/s backplane PHYs (40GBASE-KR4, 100GBASE-KR2, 100GBASE-KP4, and 100GBASE-KR4) and the 40 Gb/s and 100 Gb/s copper PHYs (40GBASE-CR4, 100GBASE-CR2, 100GBASE-CR10, and 100GBASE-CR4).

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80.4 Delay constraints

Change Table 80–5 as follows (some unchanged rows not shown):

Table 80–5—Sublayer delay constraints

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
...	...	...	...	...
100GBASE-R PMA	9216	18	92.16	See 83.5.4.
100GBASE-P PMA	9216	18	92.16	See 135.5.4.
100GBASE-KR2 PMD	4096	8	40.96	Includes allocation of 20 ns for one direction through backplane medium. See 137.5.
100GBASE-KR4 PMD	2048	4	20.48	Includes delay of one direction through backplane medium. See 93.4.
100GBASE-KP4 PMA/PMD	8192	16	81.92	Includes delay of one direction through backplane medium. See 94.2.5.
100GBASE-CR2 PMD	4096	8	40.96	Includes allocation for 20 ns for one direction through cable medium. See 136.5.
100GBASE-CR4 PMD	2048	4	20.48	Does not include delay of cable medium. See 92.4.
100GBASE-CR10 PMD	9728	19	97.28	Does not include delay of cable medium. See 85.4.
100GBASE-SR2 PMD	2048	4	20.48	Includes 2 m of fiber. See 138.3.
100GBASE-SR4 PMD	2048	4	20.48	Includes 2 m of fiber. See 95.3.3.
100GBASE-SR10 PMD	2048	4	20.48	Includes 2 m of fiber. See 86.3.1.
100GBASE-DR PMD	2048	4	20.48	Includes 2 m of fiber. See 140.3.
100GBASE-LR4 PMD	2048	4	20.48	Includes 2 m of fiber. See 88.3.1.
100GBASE-ER4 PMD	2048	4	20.48	Includes 2 m of fiber. See 88.3.1.

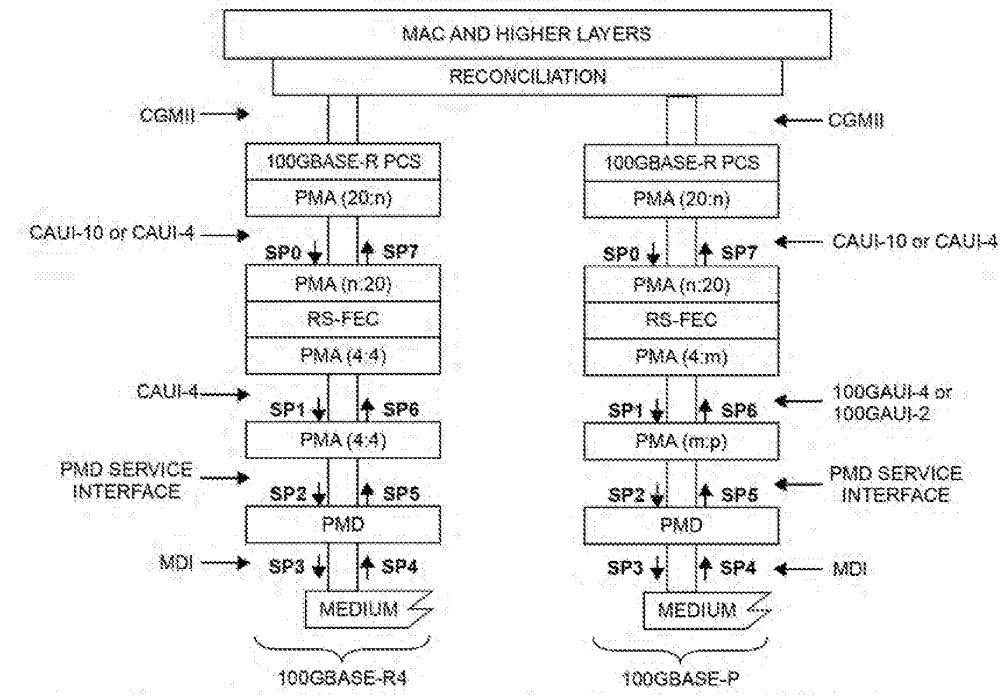
[a] For 40GBASE-R, 1 bit time (BT) is equal to 25 ps and for 100GBASE-R, 1 bit time (BT) is equal to 10 ps. (See 1.4.117 for the definition of bit time.)
[b] For 40GBASE-R, 1 pause_quantum is equal to 12.8 ns and for 100GBASE-R, 1 pause_quantum is equal to 5.12 ns. (See 31B.2 for the definition of pause_quanta.)
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

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80.5 Skew constraints

Replace Figure 80–8 with the following figure:



100GAUI-2 = 100 Gb/s TWO-LANE ATTACHMENT UNIT INTERFACE
100GAUI-4 = 100 Gb/s FOUR-LANE FEC-RATE ATTACHMENT UNIT INTERFACE
CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
m = 2 or 4
n = 4 or 10
p = 1 or 2

Figure 80–8—100GBASE-R Skew points with RS-FEC, CAUI-n, and 100GAUI-n

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Change Table 80–6 as follows (table footnotes not shown):

Table 80–6—Summary of Skew constraints

Skew points	Maximum Skew (ns)	Maximum Skew for 40GBASE-R PCS lane (UI)	Maximum Skew for 100GBASE-R PCS lane (UI)	Notes
SP0	29	N/A	≈ 150	See 83.5.3.1 or 135.5.3
SP1	29	≈ 299	≈ 150	See 83.5.3.2 or 135.5.3
SP2	43	≈ 443	≈ 222	See 83.5.3.4, 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP3	54	≈ 557	≈ 278	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP4	134	≈ 1382	≈ 691	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP5	145	≈ 1495	≈ 748	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP6	160	≈ 1649	≈ 824	See 83.5.3.6 or 135.5.3
SP7	29	N/A	≈ 150	See 83.5.3.8 or 135.5.3
At PCS receive	180	≈ 1856	≈ 928	See 82.2.13
At RS-FEC transmit	49	N/A	≈ 253	See 91.5.2.2
At RS-FEC receive	180	N/A	≈ 4641	See 91.5.3.3
At PCS receive (with RS-FEC)	49	N/A	≈ 253	See 82.2.13

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Change Table 80–7 as follows (table footnotes not shown):

Table 80–7—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation (ns)	Maximum Skew Variation for 10.3125 GBd PMD lane (UI)	Maximum Skew Variation for 25.78125 GBd PMD lane (UI)	Notes
SP0	0.2	≈ 2	N/A	See 83.5.3.1 or 135.5.3
SP1	0.2	≈ 2	N/A	See 83.5.3.2 or 135.5.3
SP2	0.4	≈ 4	≈ 10	See 83.5.3.4, 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP3	0.6	≈ 6	≈ 15	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 136.6, 137.6, 138.3, or 140.4
SP4	3.4	≈ 35	≈ 88	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 136.6, 137.6, 138.3, or 140.4
SP5	3.6	≈ 37	≈ 93	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.4
SP6	3.8	≈ 39	≈ 98	See 83.5.3.6 or 135.5.3
SP7	0.2	≈ 2	N/A	See 83.5.3.8 or 135.5.3
At PCS receive	4	≈ 41	N/A	See 82.2.13
At RS-FEC transmit	0.4	N/A	≈ 10	See 91.5.2.2
At RS-FEC receive	4	N/A	≈ 103	See 91.5.3.1
At PCS receive (with RS-FEC)	0.4	N/A	≈ 10	See 82.2.13

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82. Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R

82.6 Auto-Negotiation

Change the paragraph in 82.6 as follows:

The following requirements apply to a PCS used with a 40GBASE-KR4 PMD, 40GBASE-CR4 PMD, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-KR4, ~~or~~ 100GBASE-KP4, or 100GBASE-KR2 PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

82.7 Protocol implementation conformance statement (PICS) proforma for Clause 82, Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R

82.7.4 PICS Proforma Tables for PCS, type 40GBASE-R and 100GBASE-R

Change the heading number of 82.7.5 "Test-pattern modes" to 82.7.4.5 as follows:

82.7.4.5 Test-pattern modes

Change the heading number of 82.7.6 "Management" to 82.7.4.7 as follows:

82.7.4.7 Management

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82.7.4.11 Auto-Negotiation for Backplane Ethernet functions

Change the table in 82.7.6.4 (renumbered as 82.7.4.11) as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
*AN1	Support for use with a 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-KR4, ~~or~~ 100GBASE-KP4, or 100GBASE-KR2 PMD	82.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN2	AN_LINK.indication primitive	82.6	Support of the primitive AN_LINK.indication(link_status), ~~when the PCS is used with 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-KR4, or 100GBASE-KP4 PMD~~	AN1:M	Yes [ ] N/A [ ]
AN3	link_status parameter	82.6	Takes the value OK or FAIL, as described in 82.6	AN1:M	Yes [ ] N/A [ ]
AN4	Generation of AN_LINK.indication primitive	82.6	Generated when the value of link_status changes	AN1:M	Yes [ ] N/A [ ]

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90. Ethernet support for time synchronization protocols

90.1 Introduction

Change the first paragraph of 90.1 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows:

The TSSI is defined for the full-duplex mode of operation only. It supports MAC operation at various data rates. The MII (Clause 22), GMII (Clause 35), XGMII (Clause 46), 25GMII (Clause 106), XLGMII (Clause 81), 50GMII (Clause 132), CGMII (Clause 81), 200GMII (Clause 117), and 400GMII (Clause 117) specifications are all compatible with the gRS sublayer defined in 90.3.

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91. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs

91.5 Functions within the RS-FEC sublayer

91.5.2 Transmit function

91.5.2.6 Alignment marker mapping and insertion

Change the third and fourth paragraphs of 91.5.2.6 as follows:

For x=0 to 19, amp_tx_x<63:0> is constructed as follows:

a) Set $y = 0$ when $x \leq 3$, set $y = 16$ when $x \geq 16$ and four_lane_pmd, otherwise set $y = x$.
b) amp_tx_x<23:0> is set to M_0, M_1, and M_2 as shown in Figure 82–9 (bits 25 to 2) using the values in Table 82–2 for PCS lane number y. If am_tx_x corresponds to a Rapid Alignment marker, then the M_4, M_5, and M_6 values are used instead (see Figure 82–11).
c) amp_tx_x<31:24> = am_tx_x<33:26>
d) amp_tx_x<55:32> is set to M_4, M_5, and M_6 as shown in Figure 82–9 (bits 57 to 34) using the values in Table 82–2 for PCS lane number y. If am_tx_x corresponds to a Rapid Alignment marker, then the M_0, M_1, and M_2 values are used instead (see Figure 82–11).
e) amp_tx_x<63:56> = am_tx_x<65:58>

This process replaces the fixed bytes of the alignment markers received, possibly with errors, with the values from Table 82–2. In addition it substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 1, 2, and 3 with the fixed bytes for the alignment marker corresponding to PCS lane 0. Similarly when used with a four-lane PMD, it substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16. The variable bytes BIP or CD are unchanged. This process simplifies receiver synchronization since the receiver only needs to search for the fixed bytes corresponding to PCS lane 0 on each FEC lane. When the optional EEE deep sleep capability is supported, the receiver only needs to search for the fixed bytes corresponding to PCS lanes 0 and 16.

91.5.2.7 Reed-Solomon encoder

Change the second sentence of the second paragraph of 91.5.2.7 as follows:

When used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR PHY, the RS-FEC sublayer shall implement RS(544,514).

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91.5.3 Receive function

91.5.3.1 Alignment lock and deskew

Replace Figure 91–8 with the following:

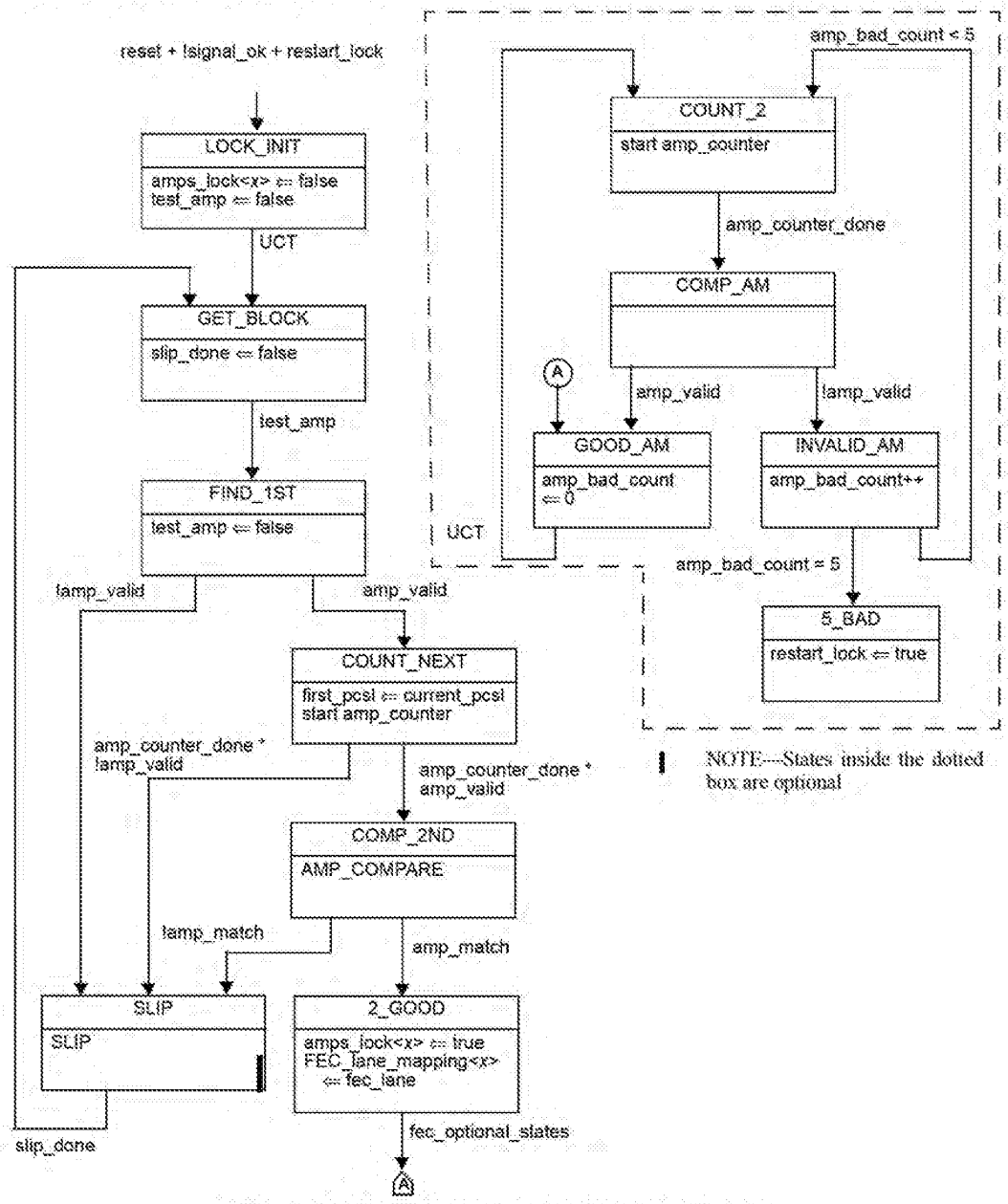


Figure 91–8—FEC synchronization state diagram

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91.5.3.3 Reed-Solomon decoder

Change the second sentence of the second paragraph of 91.5.3.3 as follows:

When used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword.

Change the last sentence of 91.5.3.3 as follows:

When the RS-FEC sublayer used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR PHY, the symbol error threshold shall be K=6380.

91.5.4 Detailed functions and state diagrams

91.5.4.2 State variables

91.5.4.2.1 Variables

Change restart_lock definition as follows:

restart_lock
: Boolean variable that is set by the FEC alignment process to reset the synchronization process on all FEC lanes. It is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) and set to false upon entry into the LOSS_OF_ALIGNMENT state. It is also set to true when 5 Alignment Markers in a row fail to match (5_BAD state) if the optional states are supported in the FEC synchronization process.

Insert fec_optional_states definition after fec_lane as follows:

fec_optional_states
: Boolean variable that is true if the optional states are implemented and false otherwise.

91.5.4.2.3 Counters

Insert new counter amp_bad_count before amp_counter as follows:

amp_bad_count
: Counts the number of consecutive alignment markers that don't match the expected values for a given FEC lane if the optional states are supported in the FEC synchronization process.

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91.6 RS-FEC MDIO function mapping

Change Table 91–2 as follows:.

Table 91–2—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass correction enable	RS-FEC control register	1.200.0	FEC_bypass_correction_enable
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable
Four lane PMD	RS-FEC control register	1.200.3	four_lane_pmd

Insert new row in Table 91–3 after "RS-FEC high SER" row as follows:.

Table 91–3—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
…	…	…	…
FEC optional states supported	RS-FEC status register	1.201.7	fec_optional_states

Insert 91.6.2a after 91.6.2 as follows:

91.6.2a four_lane_pmd

When this variable is set to one, the alignment marker mapping function substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16 (see 91.5.2.6). When this variable is set to zero, the alignment markers corresponding to PCS lanes 17, 18, and 19 are passed through unmodified. The default value of the variable is one which is the value required by the 100GBASE-CR4, 100GBASE-KR4, 100GBASE-KP4, and 100GBASE-SR4 PMDs. This variable is set to zero for the 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, and 100GBASE-DR PMDs. This variable is mapped to the bit defined in 45.2.1.101 (1.200.3).

Insert 91.6.5a after 91.6.5 as follows:

91.6.5a FEC_optional_states

This variable is set to true when the optional states in the FEC synchronization state diagram are implemented.

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91.7 Protocol implementation conformance statement (PICS) proforma for Clause 91, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs[3]

91.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs

91.7.4.1 Transmit function

Change PICS item TF11 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
...	...	...	...	...	...
TF11	Reed-Solomon encoder for 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR	91.5.2.7	RS(544,514)	KP4:M	Yes [ ] N/A [ ]

91.7.4.3 State diagrams

Insert new PICS item SD6 after SD5 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
...	...	...	...	...	...
SD6	FEC synchronization enhancement	91.5.4.3	Check AMs after synchronization is achieved per Figure 91–8	O	Yes [ ] No [ ]

[3]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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116. Introduction to 200 Gb/s and 400 Gb/s networks

116.1 Overview

116.1.2 Relationship of 200 Gigabit and 400 Gigabit Ethernet to the ISO OSI reference model

Change item h as follows:

h) The MDIs as specified in Clause 121 for 200GBASE-DR4, in Clause 122 for 200GBASE-FR4 and 200GBASE-LR4, and in Clause 124 for 400GBASE-DR4, Clause 136 for 200GBASE-CR4, Clause 137 for 200GBASE-KR4, and Clause 138 for 200GBASE-SR4, all use a 4-lane data path.

116.1.3 Nomenclature

Change Table 116-1 as shown (some unchanged rows not shown):

Table 116–1—200 Gb/s PHYs

Name	Description
200GBASE-KR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of an electrical backplane (see Clause 137)
200GBASE-CR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of twinaxial copper cable (see 1.4.407 and Clause 136)
200GBASE-SR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of multimode fiber (see Clause 138)
200GBASE-DR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of single-mode fiber, with reach up to at least 500 m (see Clause 121)
...	...

116.1.4 Physical Layer signaling systems

Change the first paragraph in 116.1.4 as follows:

This standard specifies a family of Physical Layer implementations. Table 116–2a, Table 116–3, and Table 116–4 specify the correlation between PHY types and clauses. Implementations conforming to one or more PHY types must meet the requirements of the corresponding clauses.

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Insert Table 116-2a as shown:

Table 116–2a—PHY type and clause correlation (200GBASE copper)

PHY type	Clause[a]								
	78	117		119	120	120B	120D	136	137
	EEE	RS	200GMII	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-4 C2C	200GBASE-CR4 PMD	200GBASE-KR4 PMD
200GBASE-KR4	O	M	O	M	M	O	O		M
200GBASE-CR4	O	M	O	M	M	O	O	M	

[a]O = Optional, M = Mandatory.

Change Table 116-3 as shown:

Table 116–3—PHY type and clause correlation (200GBASE optical)

PHY type	Clause[a]												
	78	117		119	120	120B	120C	120D	120E	121	122	123	138
	EEE	RS	200GMII	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-8 C2M	200GAUI-4 C2C	200GAUI-4 C2M	200GBASE-DR4 PMD	200GBASE-FR4 PMD	200GBASE-LR4 PMD	200GBASE-SR4 PMD
200GBASE-SR4	O	M	O	M	M	O	O	O	O				M
200GBASE-DR4	O	M	O	M	M	O	O	O	O	M			
200GBASE-FR4	O	M	O	M	M	O	O	O	O		M		
200GBASE-LR4	O	M	O	M	M	O	O	O	O			M	

[a]O = Optional, M = Mandatory.

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116.2 Summary of 200 Gigabit and 400 Gigabit Ethernet sublayers

116.2.5 Physical Medium Dependent (PMD) sublayer

Change the second paragraph in 116.2.5 as shown:

The 200GBASE-R PMDs and their corresponding media are specified in Clause 121, ~~and~~ Clause 122, and Clause 136 through Clause 138. The 400GBASE-R PMDs and their corresponding media are specified in Clause 122 through Clause 124.

116.4 Delay constraints

Change Table 116-5 as shown (some unchanged rows not shown):

Table 116–5—Sublayer delay constraints (200GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
...	...	...	...	...
200GBASE-R PMA	18 432	36	92.16	See 120.5.4.
200GBASE-KR4 PMD	8 192	16	40.96	Includes allocation of 20 ns for one direction through backplane medium. See 137.5.
200GBASE-CR4 PMD	8 192	16	40.96	Includes allocation of 20 ns for one direction through cable medium. See 137.5.
200GBASE-SR4 PMD	4 096	8	20.48	See 138.3.
200GBASE-DR4 PMD	4 096	8	20.48	Includes 2 m of fiber. See 121.3.1.
...	...	...	...	...

[a]For 200GBASE-R, 1 bit time (BT) is equal to 5 ps. (See 1.4.117 for the definition of bit time.)
[b]For 200GBASE-R, 1 pause_quantum is equal to 2.56 ns. (See 31B.2 for the definition of pause_quanta.)
[c]Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

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119. Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R

Insert new subclause 119.6 after subclause 119.5 as follows:

119.6 Auto-Negotiation

The following requirements apply to a PCS used with a 200GBASE-CR4 or 200GBASE-KR4 PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the AN_LINK.indication(link_status) primitive (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

119.7 Protocol implementation conformance statement (PICS) proforma for Clause 119, Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R

119.7.4 PICS proforma tables for Physical Coding Sublayer (PCS) 64B/66B, type 200GBASE-R and 400GBASE-R

Insert new subclause 119.7.4.12 after subclause 119.6.4.11 as follows:

119.7.4.12 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Support for use with a 200GBASE-CR4 or 200GBASE-KR4 PMD	119.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN1	AN_LINK.indication primitive	119.6	Support of the AN_LINK.indication(link_status) primitive	AN:M	Yes [ ] N/A [ ]
AN2	link_status parameter	119.6	Takes the value OK or FAIL, as described in 119.6	AN:M	Yes [ ] N/A [ ]
AN3	Generation of AN_LINK.indication primitive	119.6	Generated when the value of link_status changes	AN:M	Yes [ ] N/A [ ]

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120. Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R

120.5 Functions within the PMA

Insert new heading 120.5.7 and change heading number 120.5.7 to 120.5.7.1 as follows:

120.5.7 PAM4 Encoding

120.5.7.1 Gray coding for PAM4 encoded lanes

Insert new subclause 120.5.7.2 as follows:

120.5.7.2 Precoding for PAM4 encoded lanes

A PMA adjacent to a 200GBASE-CR4 or 200GBASE-KR4 PMD, shall provide 1/(1+D) mod 4 precoding capability on all transmit lanes and may optionally provide 1/(1+D) mod 4 decoding capability on all receive lanes on the PMD service interface. Precoding is implemented as specified in 135.5.7.2.

The precoder is enabled independently for the transmitter and receiver on each lane (0, 1, 2, and 3). Precoding is enabled and disabled using variables precoder_down_tx_enable_*i* and precoder_down_rx_enable_*i* (where *i* is 0, 1, 2, or 3).

If a Clause 45 MDIO is implemented, the variables precoder_down_tx_enable_*i* and precoder_down_rx_enable_*i* are accessible through register 1.600 and 1.601 (see 45.2.1.116h and 45.2.1.116i).

The variables precoder_down_tx_enable_*i* and precoder_down_rx_enable_*i* are always set to 0 in a PMA that is not adjacent to a 200GBASE-CR4 or 200GBASE-KR4 PMD.

The variables precoder_down_tx_enable_*i* and precoder_down_rx_enable_*i* shall be set as determined by the PMD control function on lane *i* (see 136.8.11.7.5). The method by which the PMD control function affects these variables is implementation dependent.

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120.6 PMA MDIO function mapping

Change Table 120–1 as shown (some unchanged rows not shown):

Table 120–1—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PMA remote loopback	PMA/PMD control 1	1.0.1	Remote_loopback_enable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
Lane 0 down transmitter precoder enable	PMA precoder control down Tx	1.600.0	precoder_down_tx_enable_0
Lane 1 down transmitter precoder enable	PMA precoder control down Tx	1.600.1	precoder_down_tx_enable_1
Lane 2 down transmitter precoder enable	PMA precoder control down Tx	1.600.2	precoder_down_tx_enable_2
Lane 3 down transmitter precoder enable	PMA precoder control down Tx	1.600.3	precoder_down_tx_enable_3
Lane 0 down receiver precoder enable	PMA precoder control down Rx	1.601.0	precoder_down_rx_enable_0
Lane 1 down receiver precoder enable	PMA precoder control down Rx	1.601.1	precoder_down_rx_enable_1
Lane 2 down receiver precoder enable	PMA precoder control down Rx	1.601.2	precoder_down_rx_enable_2
Lane 3 down receiver precoder enable	PMA precoder control down Rx	1.601.3	precoder_down_rx_enable_3
PRBS31 pattern enable	PRBS pattern testing control	1.1501.7	PRBS31_enable
…	…	…	…

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120.7 Protocol implementation conformance statement (PICS) proforma for Clause 120, Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R[4]

Insert new subclause 120.7.7 as follows:

120.7.7 Encoding

Item	Feature	Subclause	Value/Comment	Status	Support
*CKR4	PMA is adjacent to a 200GBASE-CR4 or 200GBASE-KR4 PMD.	120.5.7.2		O	Yes [ ] No [ ]
E1	PMA supports Tx precoding	120.5.7.2		CKR4:M	Yes [ ] N/A [ ]
E2	PMA supports Rx precoding	120.5.7.2		CKR4:O	Yes [ ] No [ ] N/A [ ]

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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Insert Clause 131 to Clause 140 as follows:

131. Introduction to 50 Gb/s networks

131.1 Overview

131.1.1 Scope

This clause describes the general requirements for 50 Gigabit Ethernet.

50 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 50 Gb/s, coupled with any IEEE 802.3 50GBASE Physical Layer implementation and is defined for full duplex operation only.

50 Gb/s Physical Layer entities, such as those specified in Table 131–1, provide a frame loss ratio (see 1.4.223) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

131.1.2 Relationship of 50 Gigabit Ethernet to the ISO OSI reference model

50 Gigabit Ethernet couples the IEEE 802.3 MAC to a family of 50 Gb/s Physical Layers. The relationships among 50 Gigabit Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 131–1.

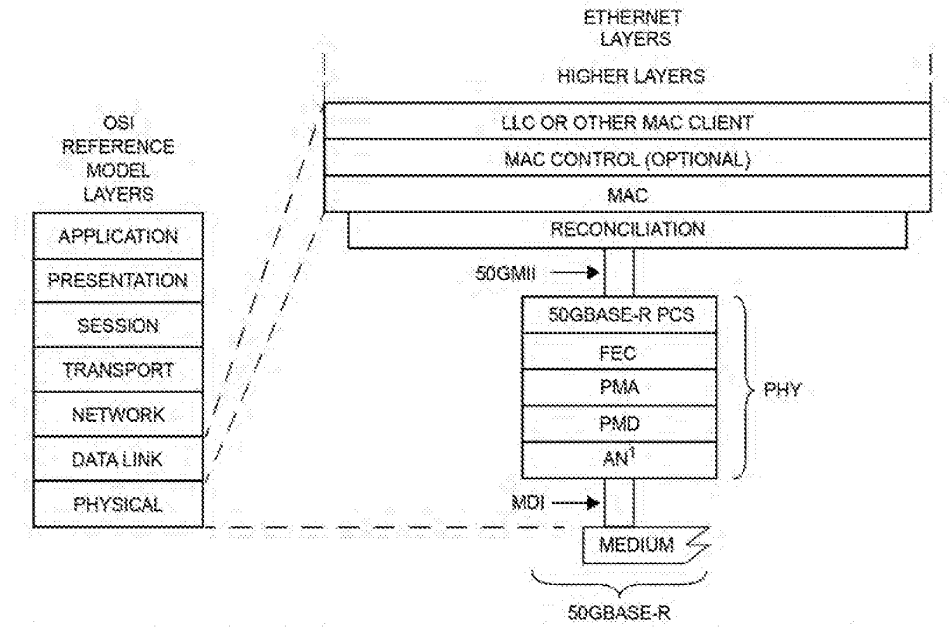


Figure 131–1—Architectural positioning of 50 Gigabit Ethernet

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While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The 50GMII, which, when implemented as logical interconnection point between the MAC sublayer and the Physical Layer (PHY), uses a 64-bit wide data path as specified in Clause 132. Physical instantiations of this interface may use other data-path widths.

b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.

c) The PMA service interface, which, when physically implemented as LAUI-2, as specified in Annex 135B and Annex 135C, or as 50GAUI-2 (50 Gb/s two-lane Attachment Unit Interface), as specified in Annex 135D and Annex 135E, at an observable interconnection port, uses a 2-lane data path.

d) The PMA service interface, which, when physically implemented as 50GAUI-1 (50 Gb/s one-lane Attachment Unit Interface) at an observable interconnection port, uses a 1-lane data path as specified in Annex 135F or Annex 135G.

e) The MDI as specified in Clause 136 for 50GBASE-CR, Clause 137 for 50GBASE-KR, Clause 138 for 50GBASE-SR, and Clause 139 for 50GBASE-FR and 50GBASE-LR use a 1-lane data path.

131.1.3 Nomenclature

The nomenclature employed by the 50 Gb/s Physical Layer is explained as follows.

The alpha-numeric prefix 50GBASE in the port type (e.g., 50GBASE-R) represents a family of Physical Layer devices operating at a speed of 50 Gb/s.

50GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) for 50 Gb/s operation over multiple PCS lanes (see Clause 133). Physical Layer devices listed in Table 131–1 are defined for operation at 50 Gb/s.

Table 131–1—50 Gb/s PHYs

Name	Description
50GBASE-KR	50 Gb/s PHY using 50GBASE-R encoding over an electrical backplane (see Clause 137).
50GBASE-CR	50 Gb/s PHY using 50GBASE-R encoding over twinaxial copper cable (see 1.4.407 and Clause 136).
50GBASE-SR	50 Gb/s PHY using 50GBASE-R encoding over multimode fiber (see Clause 138).
50GBASE-FR	50 Gb/s PHY using 50GBASE-R encoding over single-mode fiber, with reach up to at least 2 km (see Clause 139).
50GBASE-LR	50 Gb/s PHY using 50GBASE-R encoding over single-mode fiber, with reach up to at least 10 km (see Clause 139).

131.1.4 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. Table 131–2 and Table 131–3 specify the correlation between PHY types and clauses. Implementations conforming to one or more PHY types must meet the requirements of the corresponding clauses.

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Table 131–2—PHY types and clause correlation (50GBASE copper)

PHY type	Clause[a]										
	78	132		133	134	135	135B	135D	135F	136	137
	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	LAUI-2 C2C	50GAUI-2 C2C	50GAUI-1 C2C	50GBASE-CR PMD	50GBASE-KR PMD
50GBASE-KR	O	M	O	M	M	M	O	O	O		M
50GBASE-CR	O	M	O	M	M	M	O	O	O	M	

[a]O = Optional, M = Mandatory.

Table 131–3—PHY types and clause correlation (50GBASE optical)

PHY type	Clause[a]														
	78	132		133	134	135	135B	135C	135D	135E	135F	135G	136	139	
	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	LAUI-2 C2C	LAUI-2 C2M	50GAUI-2 C2C	50GAUI-2 C2M	50GAUI-1 C2C	50GAUI-1 C2M	50GBASE-SR PMD	50GBASE-FR PMD	50GBASE-LR PMD
50GBASE-SR	O	M	O	M	M	M	O	O	O	O	O	O	M		
50GBASE-FR	O	M	O	M	M	M	O	O	O	O	O	O		M	
50GBASE-LR	O	M	O	M	M	M	O	O	O	O	O	O			M

[a]O = Optional, M = Mandatory.

131.2 Summary of 50 Gigabit Ethernet sublayers

131.2.1 Reconciliation Sublayer (RS) and Media Independent Interface (50GMII)

The Media Independent Interface specified in Clause 132 provides a logical interconnection between the MAC sublayer and Physical Layer entities (PHY). The Media Independent Interface is not intended to be physically instantiated, rather it can logically connect layers within a device.

The 50GMII supports 50 Gb/s operation through its 64-bit-wide transmit and receive data paths. The Reconciliation Sublayer (RS) provides a mapping between the signals provided at the 50GMII and the MAC/PLS service definition.

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While the 50GMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for the physical coding sublayer defined in Clause 133.

131.2.2 Physical Coding Sublayer (PCS)

50GBASE-R PHYs use the PCS specified in Clause 133. The 50GBASE-R PCS performs encoding of data from the 50GMII to 64B/66B code blocks and transfers the encoded data to the PMA (or FEC) and performs decoding of 64B/66B blocks from the PMA (or FEC) and transfers the decoded data to the 50GMII.

131.2.3 Forward Error Correction (FEC) sublayer

50GBASE-R PHYs use the FEC sublayer specified in Clause 134. The FEC sublayer can be placed between the PCS and PMA sublayers or between two PMA sublayers.

131.2.4 Physical Medium Attachment (PMA) sublayer

The 50GBASE-R PMA specified in Clause 135 provides a medium-independent means for the PCS to support the use of a range of physical media.

The 50GBASE-R PMA performs the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface, the mapping of transmit and receive data streams between the FEC and the PMA via the PMA service interface, and the mapping and multiplexing of transmit and receive data streams between the PMA and PMD via the PMD service interface. In addition, the PMA performs retiming of the received data stream when appropriate, optionally provides data loopback at the PMA or PMD service interface, and optionally provides test-pattern generation and checking.

131.2.5 Physical Medium Dependent (PMD) sublayer

The Physical Medium Dependent sublayer is responsible for interfacing to the transmission medium. The PMD is located just above the Medium Dependent Interface (MDI). The MDI, logically subsumed within each PMD subclause, is the actual medium attachment for the various supported media.

The 50GBASE-R PMDs and their corresponding media are specified in Clause 136 through Clause 139.

131.2.6 Management interface (MDIO/MDC)

The optional MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMDs) and Station Management (STA) entities.

131.2.7 Management

Managed objects, attributes, and actions are defined for all 50 Gigabit Ethernet components. These items are defined in Clause 30.

131.3 Service interface specification method and notation

The service interface specification for the 50GBASE-R Physical Layers is as per the definition in 1.2.2. Note that the 50GBASE-R inter-sublayer service interfaces use multiple scalar REQUEST and INDICATION primitives, to indicate the transfer of multiple independent streams of data units, as defined in 131.3.1 through 131.3.3.

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131.3.1 Inter-sublayer service interface

The inter-sublayer service interface is defined in 116.3.1.

131.3.2 Instances of the inter-sublayer service interface

The inter-sublayer interface can be instantiated between different sublayers, hence a prefix notation is defined to identify a specific instance of an inter-sublayer service interface. The following prefixes are defined:

a) PMD:—for primitives issued on the interface between the PMD sublayer and the PMA sublayer called the PMD service interface.

b) PMA:—for primitives issued on the interface between the PMA sublayer and the PCS or the FEC sublayer called the PMA service interface.

c) FEC:—for primitives issued on the interface between the FEC sublayer and the PCS or the PMA sublayer called the FEC service interface.

Examples of inter-sublayer service interfaces for 50GBASE-R with their corresponding instance names are illustrated in Figure 131–2. For example, the primitives for one instance of the inter-sublayer service interface, named the PMD service interface, are identified as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication.

Primitives for other instances, of inter-sublayer interfaces, are represented in a similar manner as described above.

131.3.3 Semantics of inter-sublayer service interface primitives

The semantics of the inter-sublayer service interface primitives for the 50GBASE-R sublayers are described in 116.3.3.1 through 116.3.3.3.

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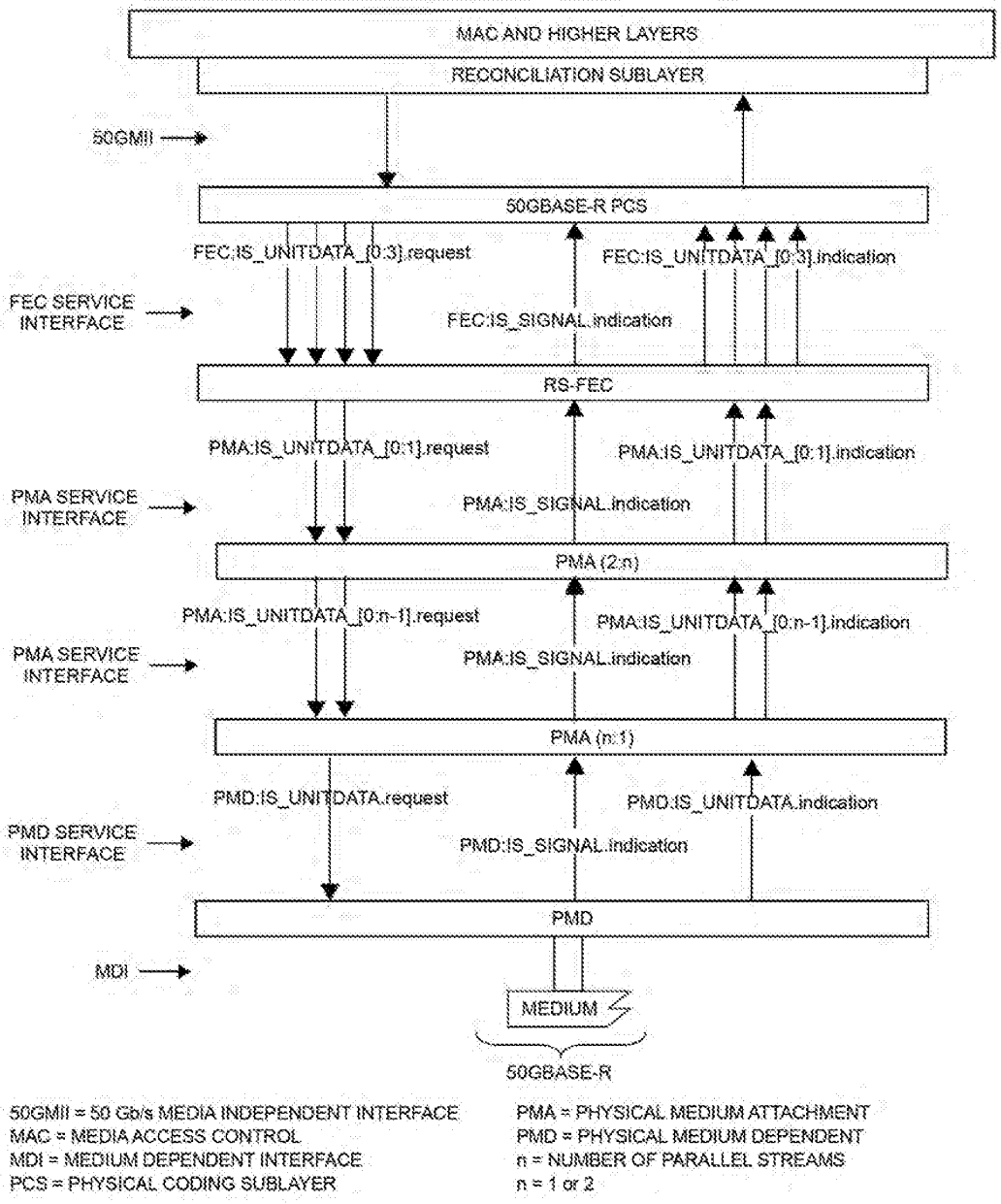


Figure 131–2—50GBASE-R inter-sublayer service interfaces

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131.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 131–4 contains the values of maximum sublayer delay (sum of transmit and receive delays at one end of the link) in bit times as specified in 1.4 and pause_quanta as specified in 31B.2 for 50 Gigabit Ethernet. If a PHY contains an Auto-Negotiation sublayer, the delay of the Auto-Negotiation sublayer is included within the delay of the PMD and medium.

Table 131–4—Sublayer delay constraints (50GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
50G MAC, RS, and MAC Control	16 384	32	327.68	See 132.1.4.
50GBASE-R PCS	11 264	22	225.28	See 133.3.
50GBASE-R RS-FEC	25 600	50	512	See 134.4.
50GBASE-R PMA	4 608	9	92.16	See 135.5.4.
50GBASE-KR PMD	2 048	4	40.96	See 137.5. Includes allocation of 20 ns for the medium.
50GBASE-CR PMD	2 048	4	40.96	See 136.5. Includes allocation of 20 ns for the medium.
50GBASE-SR PMD	1 024	2	20.48	Includes 2 m of fiber. See 138.3.1.
50GBASE-FR PMD	1 024	2	20.48	Includes 2 m of fiber. See 139.3.
50GBASE-LR PMD	1 024	2	20.48	Includes 2 m of fiber. See 139.3.

[a]For 50GBASE-R, 1 bit time (BT) is equal to 20 ps. (See 1.4.117 for the definition of bit time.)
[b]For 50GBASE-R, 1 pause_quantum is equal to 10.24 ns. (See 31B.2 for the definition of pause_quanta.)
[c]Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

See 80.4 for the calculation of bit time per meter of fiber or electrical cable.

See 31B.3.7 for PAUSE reaction timing constraints for stations at operating speeds of 50 Gb/s.

131.5 Skew constraints

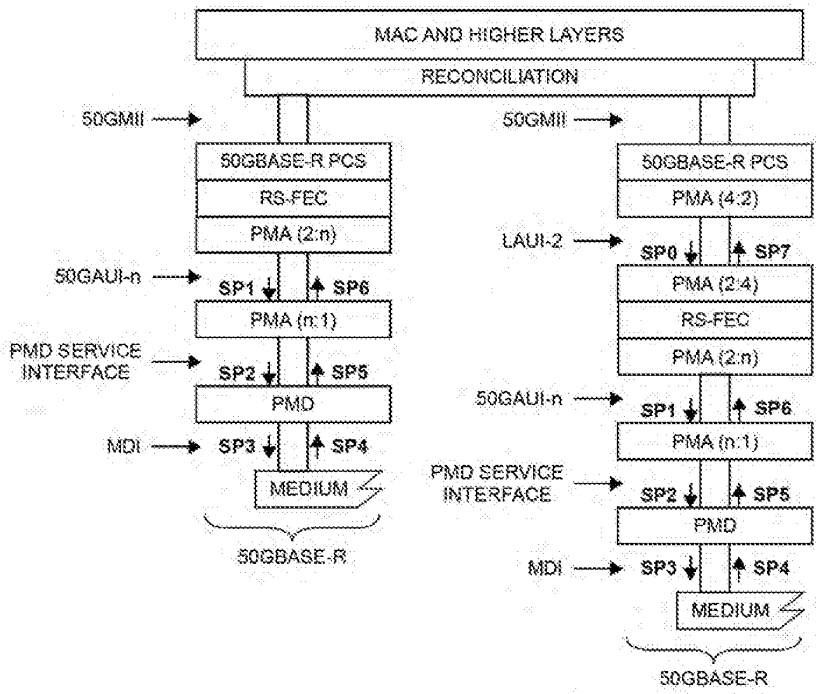
Skew (or relative delay) can be introduced between lanes by both active and passive elements of a 50GBASE-R link. Skew is defined as the difference between the times of the earliest PCS lane and latest PCS lane for the one to zero transition of the alignment marker sync bits. The PCS deskew function (see 133.2.3) compensates for all lane-to-lane Skew observed at the receiver. The Skew between the lanes must be kept within limits as shown in Table 131–5 so that the transmitted information on the lanes can be reassembled by the receive PCS.

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Skew Variation may be introduced due to variations in electrical, thermal or environmental characteristics. Skew Variation is defined as the change in Skew between any PCS lane and any other PCS lane over the entire time that the link is in operation. From the time the link is brought up, Skew Variation must be limited to ensure that each PCS lane always traverses the same lane between any pair of adjacent sublayers while the link remains in operation.

The maximum Skew and Skew Variation at physically instantiated interfaces is specified at Skew points SP0, SP1, SP2, and SP3 for the transmit direction and SP4, SP5, SP6, and SP7 for the receive direction as illustrated in Figure 131–3.



50GAUI-n = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
LAUI-2 = 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = 1 or 2

Figure 131–3—50GBASE-R Skew points

In the transmit direction, the Skew points are defined in the following locations:

- SP0 on the LAUI-2 interface, at the input of the PMA above the RS-FEC;
- SP1 on the 50GAUI-n interface, at the input of the PMA closest to the PMD;
- SP2 on the PMD service interface, at the input of the PMD;
- SP3 at the output of the PMD, at the MDI.

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In the receive direction, the Skew points are defined in the following locations:

- SP4 at the MDI, at the input of the PMD;
- SP5 on the PMD service interface, at the output of the PMD;
- SP6 on the 50GAUI-n interface, at the output of the PMA below to the RS-FEC;
- SP7 on the LAUI-2 interface, at the output of the PMA above the RS-FEC.

The allowable limits for Skew are shown in Table 131–5 and the allowable limits for Skew Variation are shown in Table 131–6.

The Skew requirements for the PCS, PMA and PMD sublayers are specified in the respective clauses as noted in Table 131–5 and Table 131–6.

Table 131–5—Summary of Skew constraints

Skew points	Maximum Skew (ns)[a]	Maximum Skew for 50GBASE-R PCS lane (UI)[b]	Maximum Skew for 50GBASE-R FEC lane (UI)[c]	Notes[d]
SP0	29	≈ 374	—	See 135.5.3.1
SP1	29	—	≈ 771	See 135.5.3.3
SP2	43	—	≈ 1143	See 135.5.3.3, 136.6, 137.6, 138.3.2, 139.3
SP3	54	—	≈ 1435	See 136.6, 137.6, 138.3.2, 139.3
SP4	134	—	≈ 3560	See 136.6, 137.6, 138.3.2, 139.3
SP5	145	—	≈ 3852	See 135.5.3.3, 136.6, 137.6, 138.3.2, 139.3
SP6	160	—	≈ 4250	See 135.5.3.7
SP7	29	≈ 374	—	See 135.5.3.8
At FEC transmit	49	—	≈ 1302	See 134.5.2.2
At FEC receive	180	—	≈ 4782	See 134.5.2.2
At PCS receive	49	≈ 632	—	See 133.2.3

[a]The Skew limit includes 1 ns allowance for PCB traces that are associated with the Skew points.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew in UI based on 1 UI equals 77.5758 ps at PCS lane signaling rate of 12.890625 Gb/s.
[c]The symbol ≈ indicates approximate equivalent of maximum Skew in UI based on 1 UI equals 37.6471 ps at FEC lane signaling rate of 26.5625 Gb/s.
[d]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

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Table 131–6—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation (ns)	Maximum Skew Variation for 25.78125 Gbd lane (UI)[a]	Maximum Skew Variation for 26.5625 Gbd lane (UI)[b]	Notes[c]
SP0	0.2	≈ 6	—	See 135.5.3.1
SP1	0.2	—	≈ 6	See 135.5.3.3
SP2	0.4	—	≈ 11	See 135.5.3.5, 136.6, 137.6, 138.3.2, 139.3
SP3	0.6	—	≈ 16	See 136.6, 137.6, 138.3.2, 139.3
SP4	3.4	—	≈ 91	See 136.6, 137.6, 138.3.2, 139.3
SP5	3.6	—	≈ 96	See 135.5.3.6, 136.6, 137.6, 138.3.2, 139.3
SP6	3.8	—	≈ 101	See 135.5.3.7
SP7	0.2	≈ 6	—	See 135.5.3.8
At FEC transmit	0.4	—	≈ 11	See 134.5.2.2
At FEC receive	4	—	≈ 107	See 134.5.2.2
At PCS receive	0.4	11	—	See 133.2.3

[a]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI based on 1 UI equals 38.7879 ps at LAUI-2 lane signaling rate of 25.78125 GBd.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI based on 1 UI equals 37.6471 ps at 50GAUI-n or PMD lane signaling rate of 26.5625 GBd.
[c]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

131.6 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

Multiple states of a function that have a transition to a common state utilizing different qualifiers (for example, multiple exit conditions to an IDLE or WAIT state) may be indicated by a shared arrow. An exit transition arrow must connect to the shared arrow, and the qualifier must be met prior to termination of the transition arrow on the shared arrow. The shared arrow has no qualifier.

131.7 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 132 through Clause 140, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each

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clause as appropriate. Each of the 50 Gigabit Ethernet PICS conforms to the same notation and conventions used in 21.6.

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132. Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation

132.1 Overview

This clause defines the characteristics of the Reconciliation Sublayer (RS) and the Media Independent Interface between Ethernet media access controllers and various PHYs. Figure 132–1 shows the relationship of the RS and Media Independent Interface to the ISO/IEC OSI reference model. The 50 Gb/s RS has identical logical functionality to the 40 Gb/s RS defined in Clause 81.

The 50GMII is an optional logical interface between the MAC sublayer and the Physical Layer (PHY).

The RS adapts the bit serial protocols of the MAC to the parallel format of the PCS service interface. Though the 50GMII is an optional interface, it is used in this standard as a basis for specification. The Physical Coding Sublayer (PCS) is specified to the 50GMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and 50GMII were implemented.

The 50GMII has the following characteristics:

a) The 50GMII supports a speed of 50 Gb/s.
b) Data and delimiters are synchronous to a clock reference.
c) It provides independent 64-bit wide transmit and receive data paths.
d) It supports full duplex operation only.

132.1.1 Summary of major concepts

The following are the major concepts of the 50GMII:

a) The 50GMII is functionally similar to other media independent interfaces that have been defined for other speeds, as they all define an interface allowing independent development of MAC and PHY logic.
b) The RS converts between the MAC serial data stream and the parallel data paths of the 50GMII.
c) The RS maps the signal set provided at the 50GMII to the PLS service primitives provided at the MAC.
d) Each direction of data transfer is independent and serviced by data, control, and clock signals.
e) The RS generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.
f) The RS participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link, and generating status reports on the transmit path to report detected link faults to the DTE on the remote end of the connecting link.
g) The 50GMII may also support Low Power Idle (LPI) signaling for PHY types supporting Energy Efficient Ethernet (EEE) (see Clause 78).

132.1.2 Application

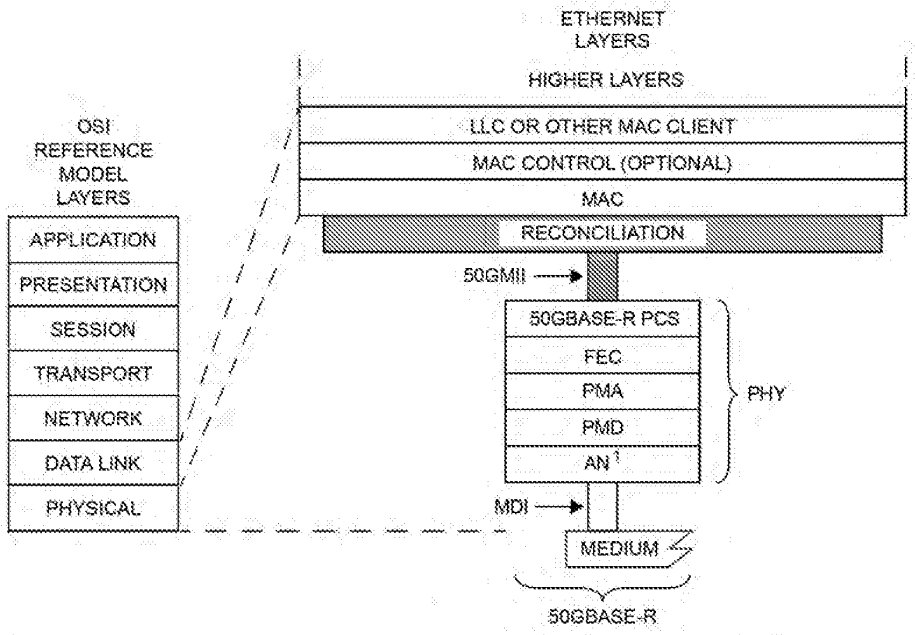
This clause applies to the interface between the MAC and PHY. This logical interface is used to provide media independence so that an identical media access controller may be used with all 50GBASE PHY types.

132.1.3 Rate of operation

The 50GMII is specified to support 50 Gb/s operation.

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50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 132–1—RS and MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

132.1.4 Delay constraints

The maximum cumulative MAC Control, MAC, and RS delay (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 132–1. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

Table 132–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
50 Gb/s MAC, RS, and MAC Control	16 384	32	327.68

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132.1.5 Allocation of functions

The allocation of functions at the 50GMII balances the need for media independence with interface simplicity. The 50GMII maximizes media independence by separating the Data Link and Physical Layers of the OSI seven-layer reference model.

132.1.6 50GMII structure

The 50GMII structure is identical to the CGMII structure specified in 81.1.7.

132.1.7 Mapping of 50GMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the 50GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 50 Gb/s; therefore, PLS service primitives supporting CSMA/CD operation are not mapped through the RS to the 50GMII. This behavior and restrictions are the same as described in 22.7, with the details of the signaling described in 132.3. LPI_REQUEST shall not be set to ASSERT unless the attached link has been operational for at least one second (i.e., link_status = OK, according to the underlying PCS/PMA).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

Mappings for the following primitives are defined for 50 Gb/s:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

The RS maps all primitives in an identical manner as the CGMII does and as specified in 81.1.7.

132.2 50GMII data stream

The 50GMII data stream has the same characteristics as the CGMII data stream described in 81.2.

132.3 50GMII functional specifications

The 50GMII functions identically to the CGMII specified in 81.3.

132.4 LPI assertion and detection

LPI assertion and detection function identically to the CGMII specified in 81.4, with the single exception that the PMA stop signaling is not applicable.

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been deasserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake-up time is enforced by the transmit LPI state diagram using CARRIER_SENSE.indication in an identical manner to that defined in 81.4, with the single exception that the PMA stop signaling described in 81.4.4 is not applicable.

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132.5 Protocol implementation conformance statement (PICS) proforma for Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation[5]

132.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

132.5.2 Identification

132.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

132.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-20xx, Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

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132.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PHY	PHY support of 50GMII	132.2		O	Yes [ ] No [ ]
*RS	Reconciliation Sublayer support of 50GMII	132.2		O	Yes [ ] No [ ]
*LPI	Implementation of LPI	132.4		O	Yes [ ] No [ ]

132.5.3 PICS proforma Tables for Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation

132.5.3.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	PHY support of MAC data rate	132.1	Support MAC data rate of 50 Gb/s	PHY:M	Yes [ ] N/A [ ]
G2	Cumulative MAC Control, MAC, and RS round-trip delay	132.1.4	Per Table 132–1	RS:M	Yes [ ] N/A [ ]

132.5.3.2 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Mapping to Clause 6	132.1.7	RS implements mapping to Clause 6 PLS service primitives	RS:M	Yes [ ] N/A [ ]

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133. Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R

133.1 Overview

133.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) that is common to a family of 50 Gb/s Physical Layer implementations known as 50GBASE-R. The 50GBASE-R PCS is a sublayer of the 50 Gb/s PHYs listed in Table 131–1.

133.1.2 Relationship of 50GBASE-R to other standards

Figure 133–1 depicts the relationships among the 50GBASE-R sublayers, the Ethernet MAC and Reconciliation Sublayers, and the higher layers.

The 50GBASE-R PCS is identical to the 40GBASE-R PCS specified in Clause 82 with the following exceptions:

1) The nominal rate at the FEC or PMA service interface is 12.890625 Gb/s per PCS lane, rather than 10.3125 Gb/s per PCS lane.
2) The alignment marker spacing is modified such that alignment markers are inserted after every 20 479 66-bit blocks on each PCS lane, rather than after every 16 383 66-bit blocks on each PCS lane as described in 82.2.7.
3) The definitions of "current_am", "am_counter", "ber_cnt" and "xus_timer" in the state diagrams defined in 82.2.19 are modified to support the different alignment marker spacing and the different data rate.
4) The optional EEE deep sleep capability is not supported.

133.1.3 Summary of 50GBASE-R sublayers

Figure 133–1 shows the relationship of the 50GBASE-R PCS sublayer (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model.

133.1.3.1 Physical Coding Sublayer (PCS)

The PCS service interface is the 50GMII, which is defined in Clause 132. The 50GMII provides a uniform interface to the Reconciliation Sublayer for all 50 Gb/s PHY implementations

The 50GBASE-R PCS provides all services required by the 50GMII.

133.1.4 Inter-sublayer interfaces

The upper interface of the PCS may connect to the Reconciliation Sublayer through the 50GMII.

The lower interface of the PCS connects to the FEC sublayer. If the optional LAUI-2 interface (see 135B.1 and 135C.1) is physically instantiated directly below the PCS sublayer, then the lower interface of the PCS instead connects to the PMA. The 50GBASE-R PCS is based on 4 PCS lanes and has a nominal rate at the FEC or PMA service interface of 12.890625 Gb/s per PCS lane, which provides capacity for the MAC data rate of 50Gb/s.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

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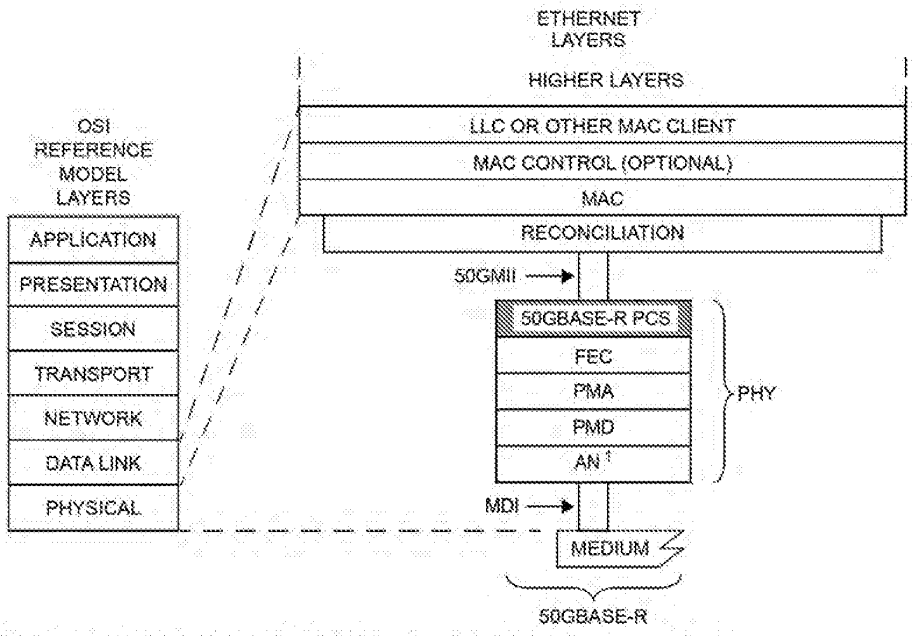


Figure 133–1—50GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

133.1.4.1 PCS service interface (50GMII)

The PCS service interface allows the 50GBASE-R PCS to transfer information to and from a PCS client. The PCS client is the Reconciliation Sublayer. The PCS Service Interface is defined as the 50GMII in Clause 132.

133.1.4.2 Forward Error Correction (FEC) or Physical Medium Attachment (PMA) service interface

The FEC or PMA service interface for the PCS is described in an abstract manner and does not imply any particular implementation. The FEC or PMA Service Interface supports the exchange of encoded data between the PCS and the FEC or PMA sublayer. The FEC service interface is defined in 134.2. The PMA service interface is defined in 135.3.

133.1.5 Functional block diagram

Figure 133–2 provides a functional block diagram of the 50GBASE-R PCS.

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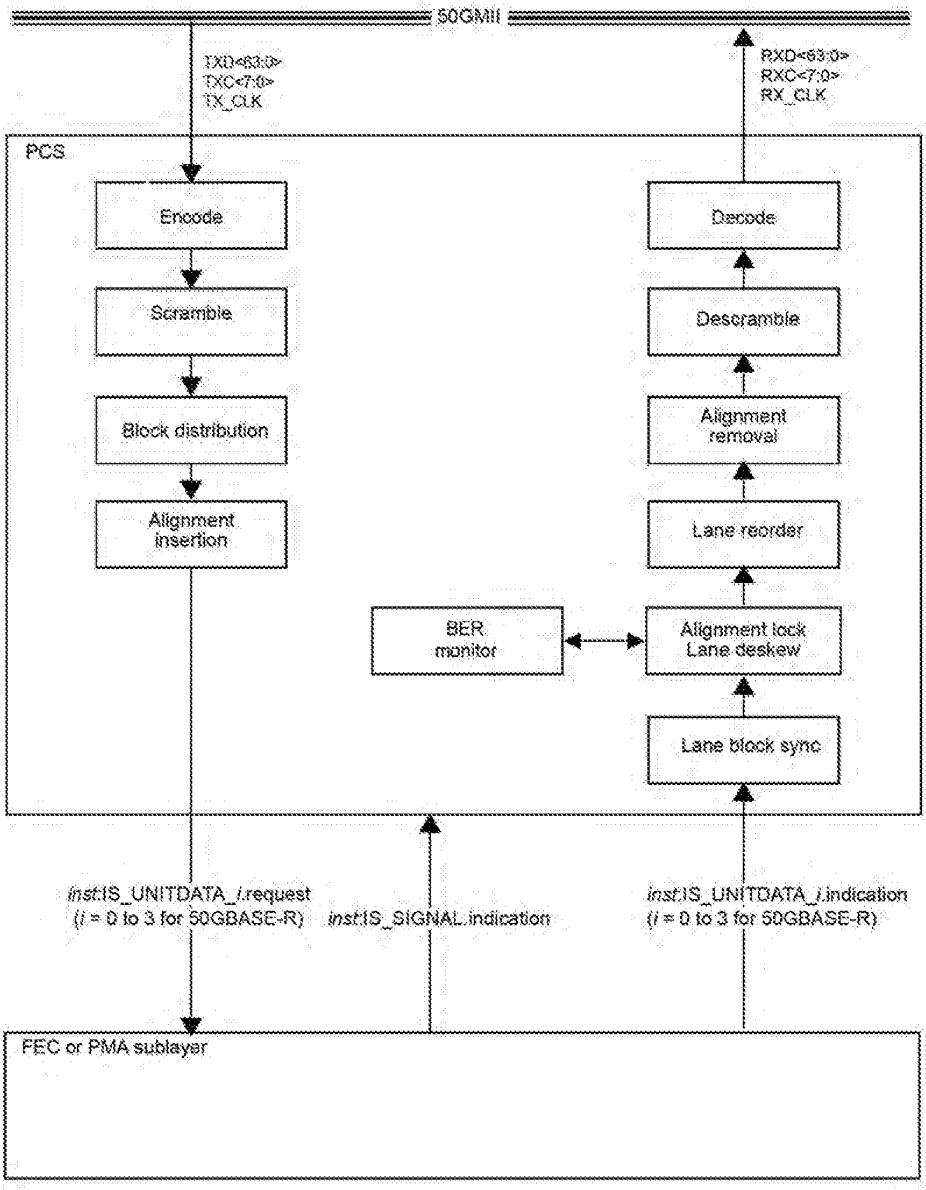


Figure 133–2—50GBASE-R PCS functional block diagram

133.2 Physical Coding Sublayer (PCS)

133.2.1 Functions within the PCS

The 50GBASE-R PCS shall have all of the functionality of the 40GBASE-R PCS specified in Clause 82 with the following exceptions:

1) The nominal rate at the FEC or PMA service interface is 12.890625 Gb/s per PCS lane, rather than 10.3125 Gb/s per PCS lane.

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2) The alignment marker spacing is modified such that alignment markers are inserted after every 20 479 66-bit blocks on each PCS lane, rather than after every 16 383 66-bit blocks on each PCS lane as described in 82.2.7. (See 133.2.2.)

3) The definition of "current_am", "am_counter" "ber_cnt" and "xus_timer" in the state diagrams defined in 82.2.19 are modified to account for the different alignment marker spacing and the different data rate. (See 133.2.4.)

4) The optional deep sleep mode of EEE is not supported.

133.2.2 Alignment marker insertion

The alignment marker insertion for the 50GBASE-R PCS is identical to the alignment marker insertion for the 40GBASE-R PCS described in 82.2.7, with the exception that the alignment markers shall be inserted after every 20 479 66-bit blocks on each PCS lane, rather than after every 16 383 66-bit blocks on each PCS lane as described in 82.2.7. Alignment marker insertion is illustrated in Figure 133–3 and Figure 133–4.

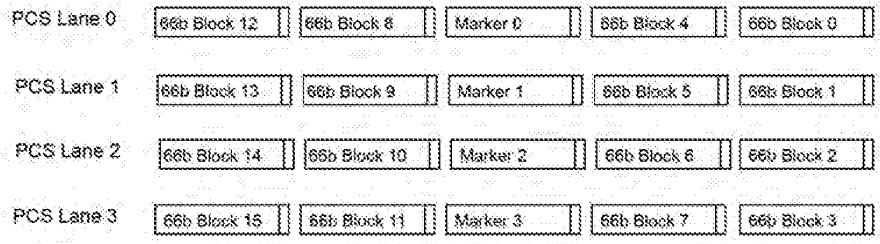


Figure 133–3—Alignment marker insertion

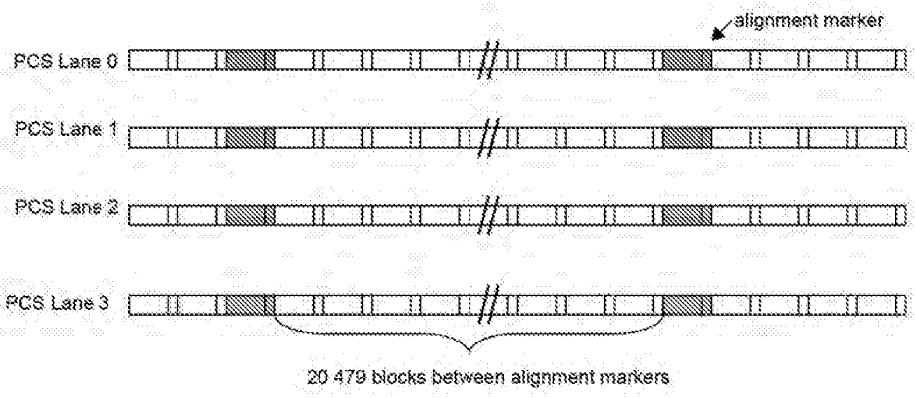


Figure 133–4—Alignment marker insertion period

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The format of the 50GBASE-R PCS alignment markers is identical to the format of the 40GBASE-R PCS alignment markers described in 82.2.7 and shown in Figure 82–9.

The content of the 50GBASE-R PCS alignment markers is identical to the content of the 40GBASE-R PCS alignment markers described in 82.2.7 and shown in Table 82–3.

133.2.3 PCS lane deskew

The 50GBASE-R PCS receiver shall support a maximum Skew of 49 ns and a maximum Skew Variation of 0.4 ns.

Skew and Skew Variation are defined in 131.5.

133.2.4 Detailed functions and state diagrams

The state diagrams are identical to those for the 40GBASE-R PCS defined in 82.2.19 with the exception that some variables, counters and timers are redefined as follows:

current_am
: This variable holds the lane number of the current alignment marker. This is compared to the variable first_am to determine if we have alignment marker lock and is always n × 20 480 66-bit blocks away from the first_am.

am_counter
: This counter counts 66-bit blocks that separate two consecutive alignment markers. The terminal count is 20 479.

ber_cnt
: This counter counts up to a maximum of 97 of the number of invalid sync headers within the current 1 ms period.

xus_timer
: Timer that is triggered every 1 ms +1%, –25%.

133.3 Delay constraints

The maximum delay contributed by the 50GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 11 264 BT (22 pause_quanta or 225.28 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

133.4 Auto-Negotiation

The following requirements apply to a PCS used with a 50GBASE-CR or 50GBASE-KR PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

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133.5 Protocol implementation conformance statement (PICS) proforma for Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R[6]

133.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

133.5.2 Identification

133.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

133.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

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133.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
PCS	Supports 50GBASE-R PCS functionality	133.1.1		M	Yes [ ]
XGE50	50GMII logical interface	132, 133.1.4	Logical interface is supported	O	Yes [ ] No [ ]
*MD	MDIO	45, 82.3	Registers and interface supported	O	Yes [ ] No [ ]
PMA	Supports operation directly connected to a PMA	133.1.4.2		O.1	Yes [ ] No [ ]
FEC	Supports operation directly connected to a FEC sublayer	133.1.4.2		O.1	Yes [ ] No [ ]
*TIM	Supports test-pattern mode	82.2.1		PMA:M	Yes [ ] N/A[ ]

133.5.4 PICS Proforma Tables for Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R

133.5.4.1 Coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder (and ENCODE function) implements the code as specified	82.2.3 and 82.2.19.2.3		M	Yes [ ]
C2	Decoder (and DECODE function) implements the code as specified	82.2.3 and 82.2.19.2.3		M	Yes [ ]
C3	Only valid block types are transmitted	82.2.3.3		M	Yes [ ]
C4	Invalid block types are treated as an error	82.2.3.3		M	Yes [ ]
C5	Only valid control characters are transmitted	82.2.3.4		M	Yes [ ]
C6	Invalid control characters are treated as an error	82.2.3.4		M	Yes [ ]
C7	Idles do not interrupt data	82.2.3.6		M	Yes [ ]
C8	IDLE control code insertion and deletion	82.2.3.6	Insertion or Deletion in groups of 8 /I/s	M	Yes [ ]
C9	Sequence ordered set deletion	82.2.3.9	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ]

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133.5.4.2 Scrambler and Descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	82.2.5	Performs as shown in Figure 49–8	M	Yes [ ]
S2	Descrambler	82.2.16	Performs as shown in Figure 49–10	M	Yes [ ]

133.5.4.3 Deskew and Reordering

Item	Feature	Subclause	Value/Comment	Status	Support
DR1	Deskew	82.2.13, 133.2.3	Able to deskew up to the value in 133.2.3.	M	Yes [ ]
DR2	Reordering	82.2.14	Performs reordering.	M	Yes [ ]

133.5.4.4 Alignment Markers

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Alignment marker insertion	133.2.2	Alignment markers are inserted periodically as described in section 133.2.2	M	Yes [ ]
AM2	Alignment marker format	133.2.2	Alignment markers are formed as described in Figure 82–9 and Table 82–3	M	Yes [ ]
AM3	Lane mapping	82.2.19.3	PCS lane number is captured	MD:M	Yes [ ] N/A [ ]

133.5.4.5 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Scrambled idle transmit test-pattern generator is implemented	82.2.11	Performs as in 82.2.11	JTM:M	Yes [ ] N/A[ ]
JT2	Scrambled idle receive test-pattern checker is implemented	82.2.18	Performs as in 82.2.18	JTM:M	Yes [ ] N/A[ ]
JT3	Transmit and receive test-pattern modes can operate simultaneously	82.2.1		JTM:M	Yes [ ] N/A[ ]

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133.5.4.6 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	133.2.1, 82.2.3.2	Placement of bits into the PCS lanes as shown in Figure 82–3.	M	Yes [ ]
B2	Receive bit order	133.2.1, 82.2.3.2	Placement of bits into the 50GMII as shown in Figure 82–4	M	Yes [ ]

133.5.4.7 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Alternate access to PCS Management objects is provided	82.3		O	Yes [ ] No [ ]

133.5.4.8 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	50GBASE-R Block Lock	133.2.4	Implements 4 block lock processes as depicted in Figure 82–12	M	Yes [ ]
SM2	The SLIP function evaluates all possible bit positions	133.2.4		M	Yes [ ]
SM3	50GBASE-R Alignment Marker Lock	133.2.4	Implements 4 alignment marker lock processes as depicted in Figure 82–13	M	Yes [ ]
SM4	The AM_SLIP functions evaluates all possible blocks	133.2.4		M	Yes [ ]
SM5	50GBASE-R PCS deskew state diagram	133.2.4	Meets the requirements of Figure 82–14	M	Yes [ ]
SM6	50GBASE-R BER Monitor	133.2.4	Meets the requirements of Figure 82–15 with xus_timer_done set to 1 ms	M	Yes [ ]
SM7	50GBASE-R Transmit process	133.2.4	Meets the requirements of Figure 82–16	M	Yes [ ]
SM8	50GBASE-R Receive process	133.2.4	Meets the requirements of Figure 82–17	M	Yes [ ]

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133.5.4.9 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports loopback	82.4	Performs as in 82.4	M	Yes [ ]
L2	When in loopback, transmits what it receives from the 50GMII	82.4	Performs as in 82.4	M	Yes [ ]

133.5.4.10 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS Delay Constraint	133.3	No more than 11 264 BT for sum of transmit and receive path delays for 50GBASE-R	M	Yes [ ]

133.5.4.11 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Support for use with a 50GBASE-CR or 50GBASE-KR PMD	82.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN1	AN_LINK.indication primitive	82.6	Support of the primitive AN_LINK.indication(link_status)	AN:M	Yes [ ] N/A[ ]
AN2	link_status parameter	82.6	Takes the value OK or FAIL, as described in 82.6	AN:M	Yes [ ] N/A[ ]
AN2	Generation of AN_LINK.indication primitive	82.6	Generated when the value of link_status changes	AN:M	Yes [ ] N/A[ ]

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134. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs

134.1 Overview

134.1.1 Scope

This clause specifies a Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs.

The RS-FEC sublayer for 50GBASE-R PHYs is identical to the RS-FEC sublayer for 100GBASE-R PHYs specified in Clause 91 with the following exceptions:

1) The service interface has four PCS lanes instead of 20 PCS lanes
2) It only implements the RS(544,514) Reed-Solomon encoder option defined in 91.5.2.7.
3) The output of the Reed-Solomon encoder is distributed to two FEC lanes, rather than the four FEC lanes described in 91.5.2.8.
4) The alignment marker processing is modified to account for the difference in the alignment marker format between the 50GBASE-R PCS (Clause 133) and the 100GBASE-R PCS (Clause 82), for the fact that the alignment markers are mapped to two FEC lanes rather than four FEC lanes, and for the fact that the alignment marker mapping to the two FEC lanes needs to maintain a 10-bit alignment.
5) The definition of some of the variables and counters for the state diagrams in 91.5.4 are modified to support the different alignment marker spacing and the different number of FEC lanes
6) The states identified as optional in the FEC synchronization state diagram in 91.5.4.3 (Figure 91–8) are mandatory for the 50GBASE-R RS-FEC.
7) The optional EEE deep sleep capability is not supported.
8) The optional FEC bypass correction feature is not supported.

134.1.2 Position of RS-FEC in the 50GBASE-R sublayers

Figure 134–1 shows the relationship of the RS-FEC sublayer to the ISO/IEC Open System Interconnection (OSI) reference model.

134.2 FEC service interface

This subclause specifies the services provided by the RS-FEC sublayer. The service interface is described in an abstract manner and does not imply any particular implementation.

The FEC service interface is provided to allow the PCS to transfer information to and from the RS-FEC. The PCS may be connected to the RS-FEC using an optional instantiation of the PMA service interface (see Annex 135B) in which case a PMA is the client of the FEC service interface.

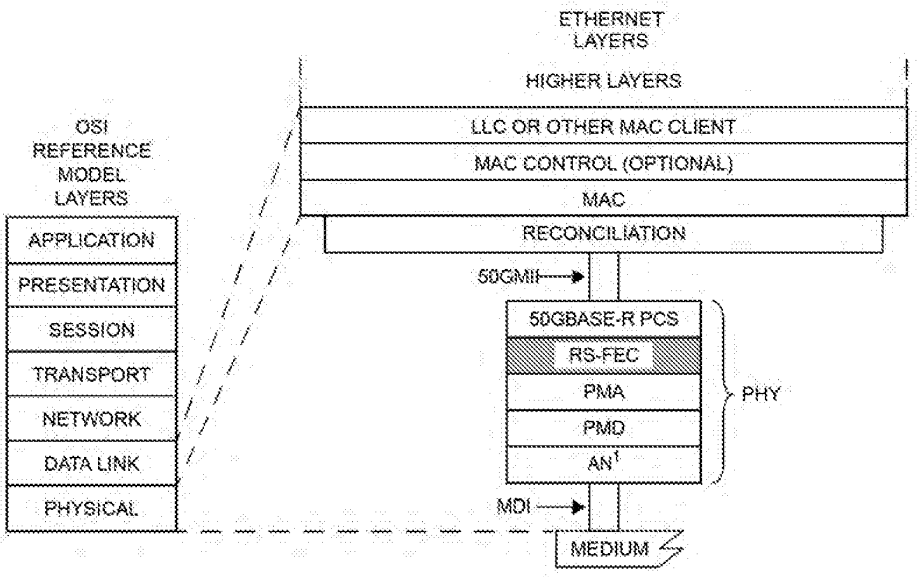
The FEC service interface is an instance of the inter-sublayer service interface defined in 131.3. The FEC service interface primitives are summarized as follows:

FEC:IS_UNITDATA_*i*.request
FEC:IS_UNITDATA_*i*.indication
FEC:IS_SIGNAL.indication

The RS-FEC operates on four parallel bit streams, hence $i = 0$ to 3.

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50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTATION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 134–1—RS-FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The PCS or PMA continuously sends four parallel bit streams to the RS-FEC, one per PCS lane, each at a nominal signaling rate of 12.890625 Gb/s. The RS-FEC continuously sends four parallel bit streams to the PCS or PMA, one per PCS lane, each at a nominal signaling rate of 12.890625 Gb/s.

The SIGNAL_OK parameter of the FEC:IS_SIGNAL.indication primitive can take one of two values: OK or FAIL. The value is set to OK when the FEC receive function has identified codeword boundaries as indicated by fec_align_status equal to true. That value is set to FAIL when the FEC receive function is unable to reliably establish codeword boundaries as indicated by fec_align_status equal to false. When SIGNAL_OK is FAIL, the rx_bit parameters of the FEC:IS_UNITDATA_*i*.indication primitives are undefined.

134.3 PMA compatibility

The RS-FEC sublayer requires that the PMA service interface consist of exactly two upstream FEC lanes and exactly two downstream FEC lanes, with each lane running at a nominal signaling rate of 26.5625 Gb/s. Therefore, the RS-FEC sublayer may be a client of the 50GBASE-R PMA sublayer defined in Clause 135, when the PMA service interface width, *p*, is set to 2.

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134.4 Delay constraints

The maximum delay contributed by the RS-FEC sublayer (sum of transmit and receive delays at one end of the link) shall be no more than 25 600 bit times (50 pause_quanta or 512 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

134.5 Functions within the RS-FEC sublayer

134.5.1 Functional block diagram

A functional block diagram of the RS-FEC sublayer is shown in Figure 134–2.

134.5.2 Transmit function

134.5.2.1 PCS Lane block synchronization

The RS-FEC transmit function forms four bit streams by concatenating the bits from each of the four FEC:IS_UNITDATA_*i*.request primitives in the order they are received. It obtains lock to the 66-bit blocks in each bit stream using the sync headers and outputs 66-bit blocks. Block lock is obtained as specified in the block lock state diagram shown in Figure 82–12, but using the variable definitions from 133.2.4.

134.5.2.2 PCS Alignment lock and deskew

Once the RS-FEC transmit function achieves block lock on a PCS lane, it then begins obtaining alignment marker lock as specified by the alignment marker lock state diagram shown in Figure 82–13, but using the variable definitions from 133.2.4. This process identifies the PCS lane number received on a particular lane of the service interface. After alignment marker lock is achieved on all four PCS lanes, all inter-lane Skew is removed as specified by the PCS deskew state diagram shown in Figure 82–14, but using the variable definitions from 133.2.4. The RS-FEC transmit function shall support a maximum Skew of 49 ns and a maximum Skew Variation of 0.4 ns. Skew and Skew Variation are defined in 131.5.

134.5.2.3 PCS Lane reorder

PCS lanes can be received on different lanes of the service interface from which they were originally transmitted due to Skew between lanes and multiplexing by the PMA. The RS-FEC transmit function shall order the PCS lanes according to the PCS lane number.

134.5.2.4 Alignment marker removal

After all PCS lanes are aligned and deskewed, the PCS lanes are multiplexed together in the proper order to reconstruct the original stream of blocks and the alignment markers are removed from the data stream. Note that an alignment marker is always removed when am_lock is true for a given PCS lane even if it does not match the expected alignment marker value (due to a bit error for example). Repeated alignment marker errors result in am_lock being set to false for a given PCS lane, but until that happens it is sufficient to remove the block in the alignment marker position.

As part of the alignment marker removal process, the BIP_3 field is compared to the calculated Bit Interleaved Parity (BIP) value (see 82.2.8) for each PCS lane. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 1.230 to 1.233) is incremented by one each time the calculated BIP value does not equal the value received in the BIP_3 field. The incoming bit error ratio can be estimated by dividing the BIP block error ratio by a factor of 1 351 680.

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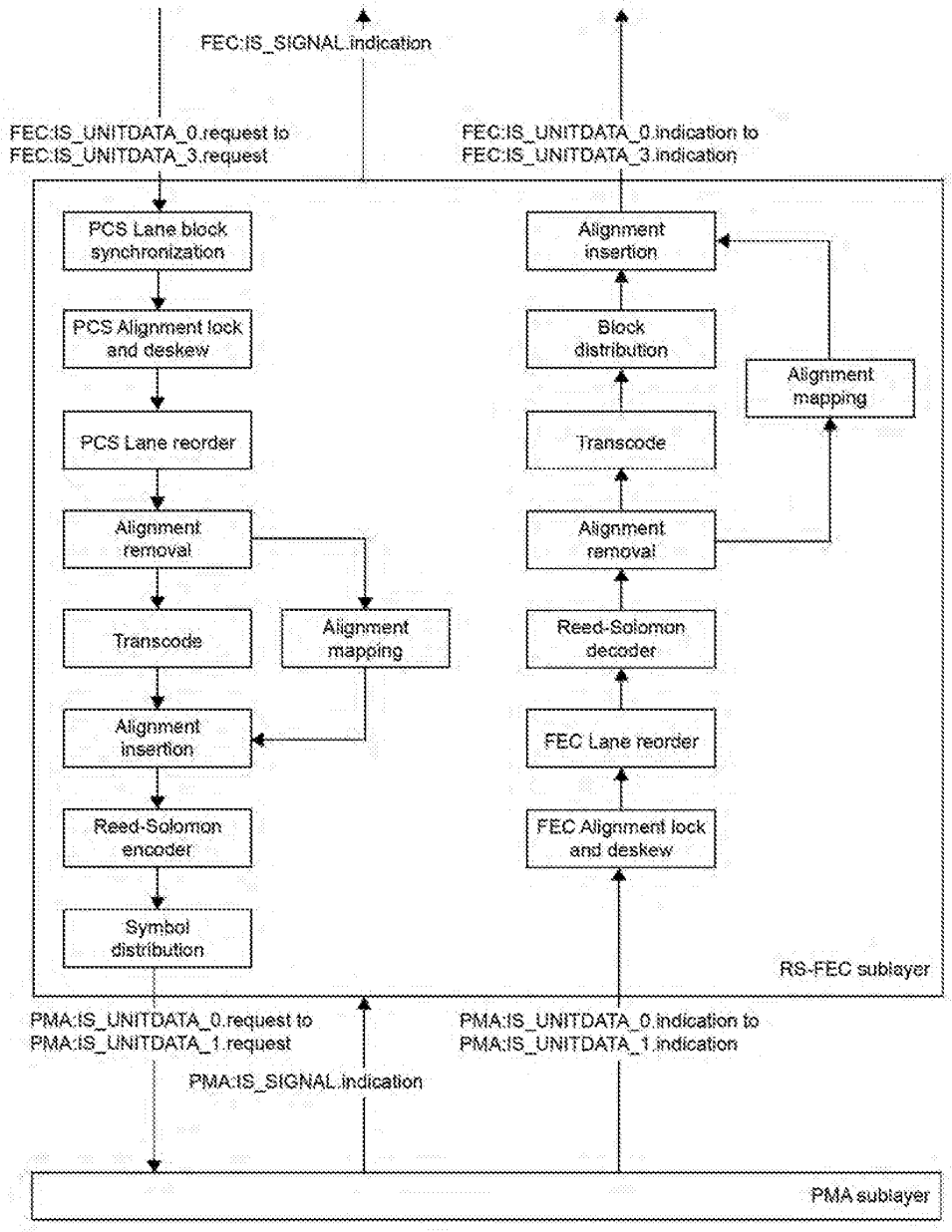


Figure 134–2—Functional block diagram

134.5.2.5 64B/66B to 256B/257B transcoder

The 64B/66B to 256B/257B transcoder is identical to the transcoder for the 100GBASE-R RS-FEC sublayer defined in 91.5.2.5.

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134.5.2.6 Alignment marker mapping and insertion

The alignment markers that were removed per 134.5.2.4 are re-inserted after being processed by the alignment marker mapping function. The alignment marker mapping function compensates for the operation of the symbol distribution function defined in 134.5.2.8 and rearranges the alignment marker bits so that they appear on the FEC lanes intact and in the desired sequence. This preserves the properties of the alignment markers (e.g., DC balance, transition density) and provides a deterministic pattern for the purpose of synchronization at the receiver. The RS-FEC receive function uses knowledge of this mapping to determine the FEC lane that is received on a given lane of the PMA service interface, to compensate for skew between FEC lanes, and to identify RS-FEC codeword boundaries.

The alignment marker mapping function operates on a group of four aligned and reordered alignment markers received from the PCS. Let am_tx_*x*<65:0> be the alignment marker for PCS lane *x*, *x*=0 to 3, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_txmapped<256:0> in a manner that yields the same result as the following process.

For *x*=0 to 3, amp_tx_*x*<63:0> is constructed as follows:

- Set $y = 0$ when $x \leq 1$, otherwise set $y = x$.
- amp_tx_*x*<23:0> is set to M_0, M_1, and M_2 as shown in Figure 82–9 (bits 25 to 2) using the values in Table 82–3 for PCS lane number *y*.
- amp_tx_*x*<31:24> = am_tx_*x*<33:26>
- amp_tx_*x*<55:32> is set to M_4, M_5, and M_6 as shown in Figure 82–9 (bits 57 to 34) using the values in Table 82–3 for PCS lane number *y*.
- amp_tx_*x*<63:56> = am_tx_*x*<65:58>

This process replaces the fixed bytes of the alignment markers received from the PCS, possibly with errors, with the values from Table 82–3. In addition it substitutes the fixed bytes of the alignment markers corresponding to PCS lane 1 with the fixed bytes for the alignment marker corresponding to PCS lane 0. The variable bytes of the alignment markers received from the PCS (BIP_3 and BIP_7) are unchanged. This simplifies the synchronization process at the RS-FEC receiver, as the receiver only needs to search for the fixed alignment marker bytes corresponding to PCS lane 0 on each FEC lane.

am_txpayloads<0,129:0> and am_txpayloads<1,125:0> are then constructed from amp_tx as follows:

- am_txpayloads<0, 63:0> = amp_tx_0<63:0>
- am_txpayloads<0, 127:64> = amp_tx_2<63:0>
- am_txpayloads<0, 129:128> = amp_tx_3<57:56>
- am_txpayloads<1, 63:0> = amp_tx_1<63:0>
- am_txpayloads<1, 119:64> = amp_tx_3<55:0>
- am_txpayloads<1, 125:120> = amp_tx_3<63:58>

This process is an intermediate step in the generation of am_txmapped<256:0>, and is illustrated in Figure 134–3.

Given *i*=0 to 1, *k*=0 to 12, and *y*=*i*+2*k*, am_txmapped<255:0> is constructed from am_txpayloads as follows:

- If ($y < 25$) then am_txmapped<(10*y*+9):10*y*> = am_txpayloads<*i*, (10*k*+9):10*k*>
- am_txmapped<255:250> = am_txpayloads<1, 125:120>

A 1-bit pad is appended to the mapped alignment markers to yield the equivalent of one 257-bit block. The pad bit, am_txmapped<256>, shall be set to 0 or 1 in an alternating pattern.

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am_txmapped<256:0> is inserted into the data path prior to the Reed-Solomon encoder (see Figure 134–4) every 4 × 20 480 66-bit blocks, corresponding to every 1 024 Reed-Solomon codewords. The mapped alignment markers, am_txmapped<256:0> shall be inserted as the first 257 message bits to be transmitted every 1024th codeword. The first 257-bit block inserted after am_txmapped shall correspond to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective PCS lane.

The result of this alignment mapping process is that after Reed-Solomon encoding and symbol distribution (134.5.2.7 and 134.5.2.8 respectively), the alignment marker bit patterns shown in Figure 134–3 appear on the two FEC output lanes and aligned with the start of every 1024th FEC codeword. The FEC receiver uses this information to lock onto the two FEC lanes and to identify the FEC codeword boundaries.

An additional result of this alignment mapping process, is that the BIP_3 and BIP_7 fields from normal PCS alignment markers are carried across the link protected by FEC. These fields cannot be used to monitor errors on the link protected by FEC as 64B/66B to 256B/257B transcoding and Reed-Solomon encoding alters the bit sequence. However, these fields may again be used to monitor errors after the original bit sequence is restored, i.e., following Reed-Solomon decoding and 256B/257B to 64B/66B transcoding.

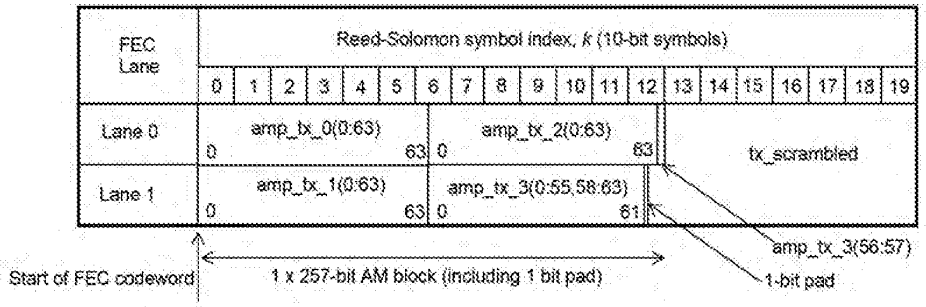


Figure 134–3—Alignment marker mapping to FEC lanes

134.5.2.7 Reed-Solomon encoder

The Reed-Solomon encoder is identical to the RS(544,514) Reed-Solomon encoder defined in 91.5.2.7.

134.5.2.8 Symbol distribution

Once the data has been Reed-Solomon encoded, it is distributed to two FEC lanes, one 10-bit symbol at a time in a round robin distribution from the lowest to the highest numbered FEC lane. The distribution process is shown in Figure 134–4.

134.5.2.9 Transmit bit ordering

The transmit bit ordering is illustrated in Figure 134–4.

134.5.3 Receive function

134.5.3.1 Alignment lock and deskew

The RS-FEC receive function forms two bit streams by concatenating the bits from each of the two PMA:IS_UNITDATA_*i*.indication primitives in the order they are received. It obtains lock to the alignment markers as specified by the FEC synchronization state diagram shown in Figure 91–8, but using the variable definitions from 134.5.4.

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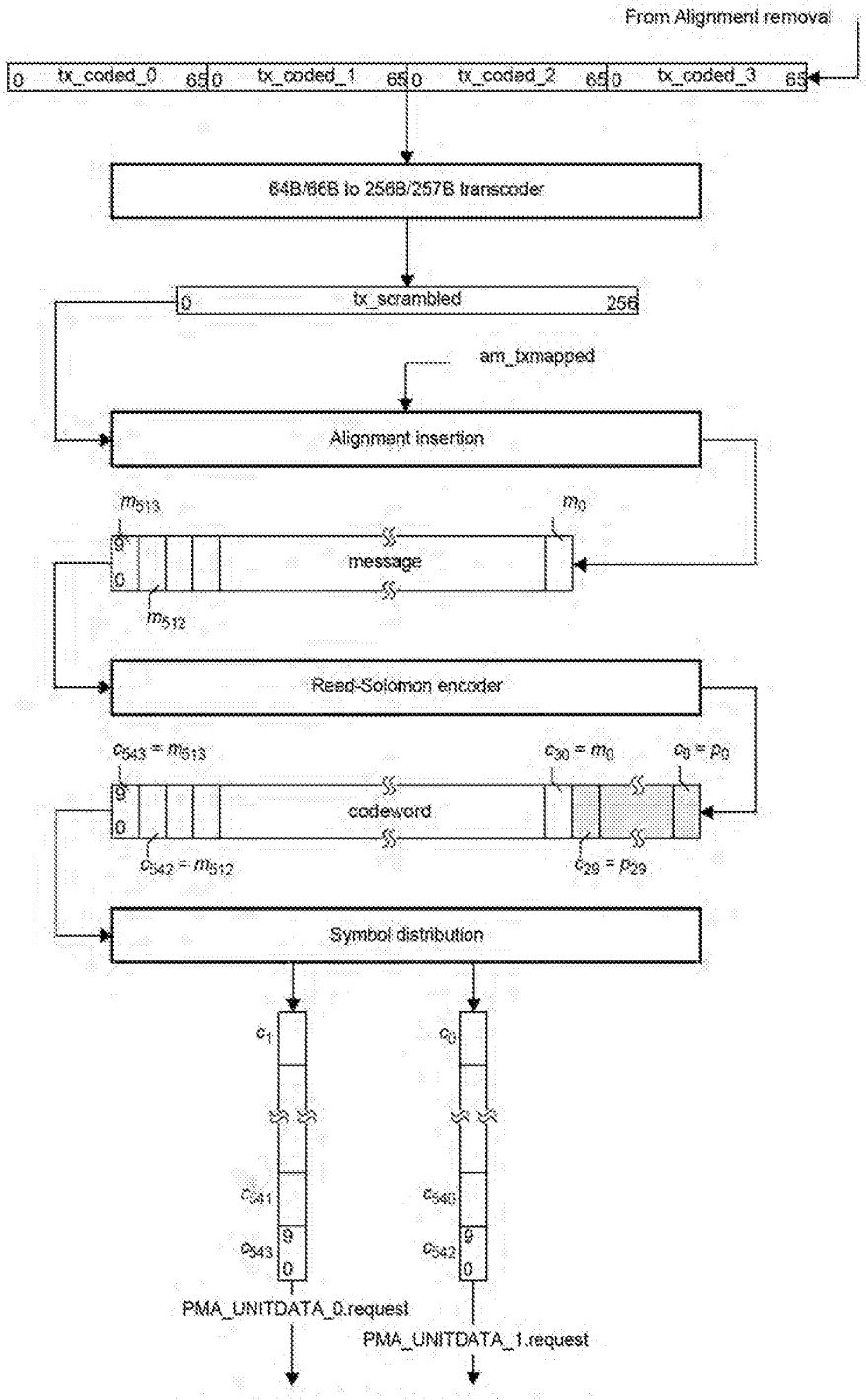


Figure 134–4—Transmit bit ordering

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After alignment marker lock is achieved the two FEC lanes, all inter-lane Skew is removed as specified by the FEC alignment state diagram shown in Figure 91–9. The FEC receive function shall support a maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns.

134.5.3.2 FEC Lane reorder

FEC lanes can be received on different lanes of the service interface from which they were originally transmitted. The FEC receive function shall order the FEC lanes according to the FEC lane number (see 134.5.2.6). The FEC lane number is defined by the sequence of alignment markers that are mapped to each FEC lane.

After all FEC lanes are aligned, deskewed, and reordered, the FEC lanes are multiplexed together in the proper order to reconstruct the original stream of FEC codewords.

134.5.3.3 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols.

The RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when an errored codeword was not corrected. The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10^{-5}. This limit is also expected to apply for t+2 errors, t+3 errors, and so on.

The Reed-Solomon decoder shall indicate errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors that were not corrected, it ensures that for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11. In addition, it shall ensure that rx_coded_0<1:0> corresponding to the second 257-bit block and rx_coded_3<1:0> corresponding to the last (20th) 257-bit block in the codeword are set to 11. Setting rx_coded_0<1:0> to 11 as described causes the PCS to assign R_BLOCK_TYPE=E to the 66-bit block and decode its content as EBLOCK_R (see 49.2.13.2.1 and 49.2.13.2.3). This causes the PCS to discard all frames 64 bytes and larger that are fully or partially contained within the codeword.

The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see 134.6.2). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see 134.6.1).

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the RS-FEC sublayer to reduce the likelihood that errors in a packet are not detected. The Reed-Solomon decoder counts the number of symbol errors detected in consecutive non-overlapping blocks of 8192 codewords. When the number of symbol errors in a block of 8192 codewords exceeds 6380, the Reed- Solomon decoder shall cause synchronization header rx_coded<1:0> of each subsequent 66-bit block that is delivered to the PCS to be assigned a value of 00 or 11 for a period of 60 ms to 75 ms. As a result, the PCS sets hi_ber = true, which inhibits the processing of received packets. When Auto-Negotiation is supported and enabled, assertion of hi_ber causes Auto-Negotiation to restart.

134.5.3.4 Alignment marker removal

The first 257 message bits in every 1024th codeword is the vector am_rxmapped<256:0> where bit 0 is the first bit received. The specific codewords that include this vector are indicated by the alignment lock and deskew function (see 134.5.3.1).

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The vector am_rxmapped shall be removed prior to transcoding.

134.5.3.5 256B/257B to 64B/66B transcoder

The 256B/257B to 64B/66B transcoder is identical to the transcoder for the 100GBASE-R RS-FEC sublayer defined in 91.5.3.5.

134.5.3.6 Block distribution

After the data has been transcoded, it shall be distributed to four PCS lanes, one 66-bit block at a time in a round robin distribution from the lowest to the highest numbered PCS lanes. The distribution process is shown in Figure 82–6.

134.5.3.7 Alignment marker mapping and insertion

The alignment marker mapping function compensates for operation of the lane reorder function (see 134.5.2.3) to derive the PCS lane alignment markers, am_rx_*x*<65:0> for *x*=0 to 3, from am_rx-mapped<256:0> (see134.5.3.4).

The alignment markers shall be derived from am_rxmapped<256:0> in a manner that yields the same result as the following process.

Given *i*=0 to 1, *k*=0 to 12, and *y*=*i*+2*k*, am_rxpayloads is constructed from am_rxmapped as follows:.

— If (*y* < 25) then am_rxpayloads<*i*, (10*k*+9):10*k*> = am_rxmapped<(10*y*+9):10*y*>

— am_rxpayloads<1, 125:120> = am_rxmapped<255:250>

The one bit pad am_rxmapped<256> is ignored by the receiver.

For *x*=0 to 3, amp_rx_*x*<63:0> is constructed from am_rxpayloads as follows:

— amp_rx_0<63:0> = am_rxpayloads<0, 63:0>

— amp_rx_1<63:0> = am_rxpayloads<1, 63:0>

— amp_rx_2<63:0> = am_rxpayloads<0, 127:64>

— amp_rx_3<55:0> = am_rxpayloads<1, 119:64>

— amp_rx_3<57:56> = am_rxpayloads<0, 129:128>

— amp_rx_3<63:58> = am_rxpayloads<1, 125:120

For *x*=0 to 3, am_rx_*x*<65:0> is constructed as follows:

— am_rx_*x*<0>=1 and am_rx_*x*<1>=0.

— am_rx_*x*<25:2> is set to M_0, M_1, and M_2 as shown in Figure 82–9 using the values in Table 82–3 for PCS lane number *x*.

— am_rx_*x*<33:26> = amp_rx_*x*<31:24>.

— am_rx_*x*<57:34> is set to M_4, M_5, and M_6 as shown in Figure 82–9 using the values in Table 82–3 for PCS lane number *x*.

— am_rx_*x*<65:58> = amp_rx_*x*<63:56>

One vector is mapped to four alignment markers every 1 024 Reed-Solomon codewords (see 134.5.3.4). The alignment markers are simultaneously transmitted on the four PCS lanes after every 20 479th column of four 66-bit blocks.

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The alignment markers am_rx_0 to am_rx_3 shall be inserted so that they are immediately followed by rx_coded_0 to rx_coded_3, respectively, as derived from the first 257-bit block following am_rxmapped

134.5.3.8 Receive bit ordering

The receive bit ordering is illustrated in Figure 134–5. This illustration shows the case where the FEC lanes appear across the PMA:IS_UNITDATA_*i*.indication primitives in the correct order.

134.5.4 Detailed functions and state diagrams.

The state diagrams, including the associated definitions of variables, functions and counters, are identical to those for the 100GBASE-R RS-FEC sublayer defined in 91.5.4, with the exception that some of the variables and counters are redefined to account for the differences in alignment marker spacing and number of FEC lanes.

In addition, EEE optional deep sleep capability is not supported for 50GBASE-R PHYs and therefore any reference to the optional EEE deep sleep capability in 91.5.4 can be ignored.

134.5.4.1 State diagram conventions

The state diagram conventions are identical to those defined in 91.5.4.1.

134.5.4.2 State variables

134.5.4.2.1 Variables

This following variables are redefined from what is described in 91.5.4.2.1:

amp_valid
: Boolean variable that is set to true if the received 64-bit block is a valid alignment marker payload. The alignment marker payload, mapped to an FEC lane according to the process described in 134.5.2.6, consists of 48 known bits and 16 variable bits (the BIP3 field and its complement BIP7 see 82.2.7). The bits of the candidate block that are in the positions of the known bits in the alignment marker payload are compared on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles in the alignment marker payload, the candidate block is considered a valid alignment marker payload. Each FEC lane compares the candidate block to the alignment marker payload for PCS lane 0.

amps_lock<x>
: Boolean variable that is set to true when the receiver has detected the location of the alignment marker payload sequence for a given lane on the PMA service interface, where $x = 0:1$.

fec_lane
: A variable that holds the FEC lane number (0 to 1) received on lane x of the PMA service interface when amps_lock<x> = true. The FEC lane number is determined by the alignment marker payloads in the 2nd position of the sequence based on the mapping defined in 134.5.2.6. The 48 bits that are in the positions of the known bits in the received alignment marker payload are compared to the expected values for a given payload position and FEC lane on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles on a given FEC lane, then the FEC lane number is assigned accordingly.

fec_lpi_fw
: Boolean variable that controls the behavior of the Transmit LPI and Receive LPI state dia-

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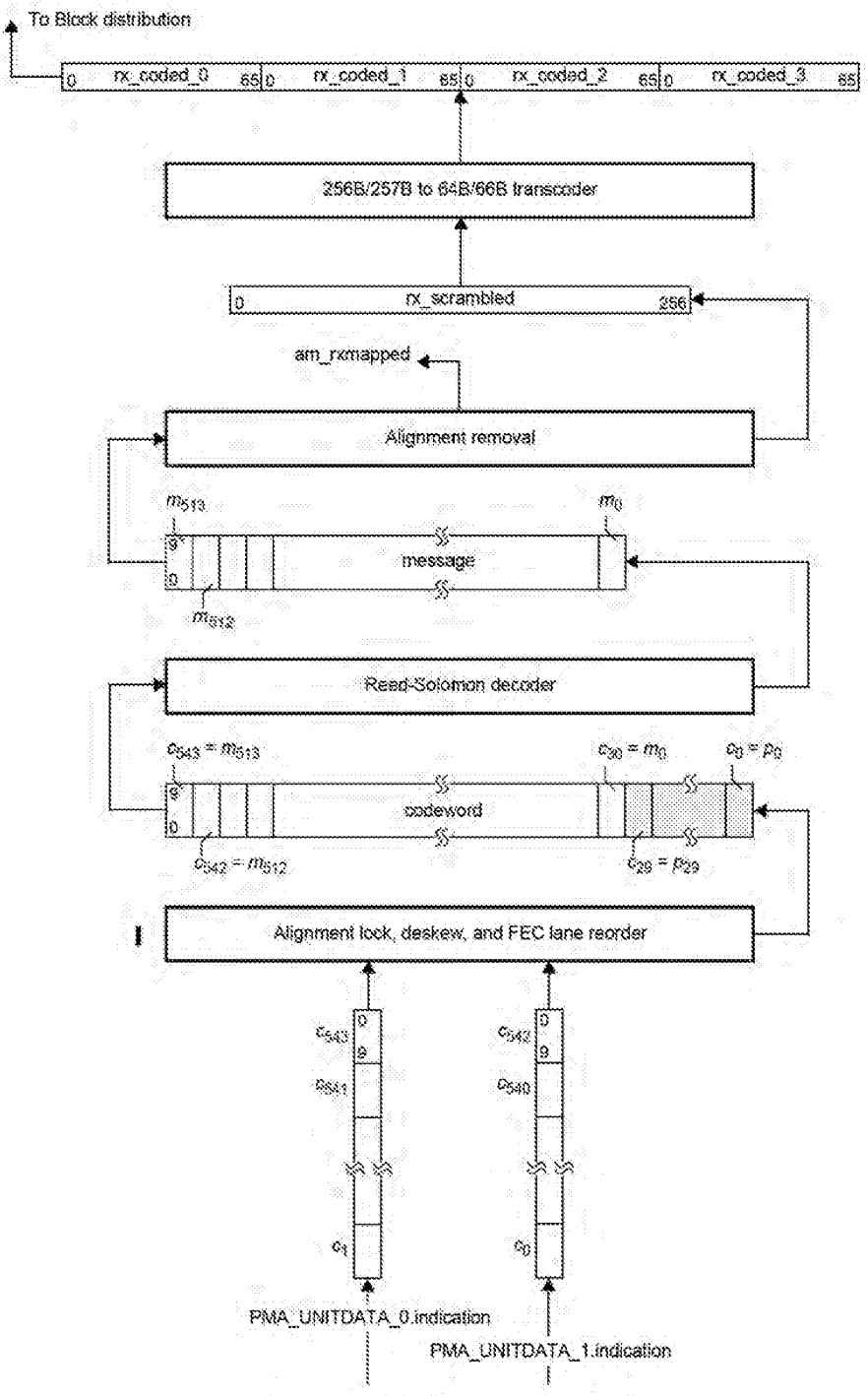


Figure 134–5—Receive bit ordering

grams. This variable is set to true when the local PCS is configured to use the fast wake mechanism and set to false otherwise. This variable shall always be set to true.

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fec_optional_states
: Boolean variable that is always set to true to indicate that the optional states in the FEC synchronization state diagram in Figure 91–8 are implemented.

134.5.4.2.2 Functions

The functions are identical to those defined in 91.5.4.2.2.

134.5.4.2.3 Counters

This following counters are redefined from what is described in 91.5.4.2.3:

amp_counter
: This counter counts the 1 024 FEC codewords that separate the ends of two consecutive normal alignment marker payload sequences. A FEC codeword is 2 720 bits per FEC lane

134.5.4.3 State diagrams

The state diagrams are identical to those defined in 91.5.4.3.

134.6 RS-FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the RS-FEC. If MDIO is implemented, it shall map MDIO control bits to RS-FEC control variables as shown in Table 134–1, and MDIO status bits to RS-FEC status variables as shown in Table 134–2, and if a separated PMA (see 45.2.1) is connected to the FEC service interface (e.g., if the RS-FEC and PCS are separated via a LAUI-2 interface) it shall map additional MDIO status bits to additional RS-FEC status variables as shown in Table 134–3.

Table 134–1—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable

The following subclauses define variables that are not otherwise defined, e.g., for use by state diagrams.

134.6.1 FEC_bypass_indication_enable

This variable is set to one to bypass the error indication function (see 91.5.3.3) when this ability is supported. When this variable is set to zero, the decoder indicates errors to the PCS sublayer. The default value of this variable is zero. This variable is mapped to the bit defined in 45.2.1.101 (1.200.1).

134.6.2 FEC_bypass_indication_ability

The Reed-Solomon decoder may have the option to bypass the error indication function (see 91.5.3.3) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error indication. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.102 (1.201.1).

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Table 134–2—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication ability	RS-FEC status register	1.201.1	FEC_bypass_indication_ability
RS-FEC high SER	RS-FEC status register	1.201.2	hi_ser
FEC AM lock *x*, *x*=0 to 1	RS-FEC status register	1.201.8:9	amps_lock<x>
RS-FEC align status	RS-FEC status register	1.201.14	fec_align_status
FEC corrected codewords	RS-FEC corrected codewords counter register	1.202, 1.203	FEC_corrected_cw_counter
FEC uncorrected codewords	RS-FEC uncorrected codewords counter register	1.204, 1.205	FEC_uncorrected_cw_counter
FEC lane *x* mapping	RS-FEC lane mapping register	1.206	FEC_lane_mapping<x>
FEC symbol errors, FEC lanes 0 to 1	RS-FEC symbol error counter register, FEC lanes 0 to 1	1.210 to 1.213	FEC_symbol_error_counter_*i*

Table 134–3—MDIO/RS-FEC status variable mapping for separated PMA

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
PCS align status	RS-FEC status register	1.201.15	align_status
BIP errors, PCS lanes 0 to 3	RS-FEC BIP error counter register, PCS lanes 0 to 3	1.230 to 1.233	BIP_error_counter_*i*
PCS lane *x* mapping	PCS lane *x* mapping register	1.250 to 1.253	lane_mapping<x>
Block *x* lock	RS-FEC PCS alignment status 1 register	1.280	block_lock<x>
Lane *x* aligned	RS-FEC PCS alignment status 3 register	1.282	am_lock<x>

134.6.3 hi_ser

This variable is defined when the FEC_bypass_indication_ability variable is set to one. When FEC_bypass_indication_enable is set to one, this bit is set to one if the number of RS-FEC symbol errors in a window of 8 192 codewords exceeds the threshold (see 91.5.3.3) and is set to zero otherwise. This variable is mapped to the bit defined in 45.2.1.102 (1.201.2).

134.6.4 amps_lock<x>

These variables are assigned by the FEC alignment state diagram shown in Figure 91–9 (see 91.5.4.3 and 134.5.4). They are mapped to the bits defined in 45.2.1.102 (1.201.8 to 1.201.9 for FEC lanes 0 to 1, respectively).

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134.6.5 fec_align_status

This variable assigned by the FEC alignment state diagram shown in Figure 91–9 (see 91.5.4.3). It is mapped to the bit defined in 45.2.1.102 (1.201.14).

134.6.6 FEC_corrected_cw_counter

A corrected FEC codeword is a codeword that contains errors and was corrected.

FEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.103 (1.202, 1.203).

134.6.7 FEC_uncorrected_cw_counter

An uncorrected FEC codeword is a codeword that contains errors (when the bypass correction feature is supported and enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled).

FEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.104 (1.204, 1.205).

134.6.8 FEC_lane_mapping<*x*>

When the RS-FEC receive function detects and locks to an alignment marker payload on PMA service interface lane *x*, the FEC lane number corresponding to the detected alignment marker payload is assigned to the variable FEC_lane_mapping<*x*>. These variables are mapped to the register defined in 45.2.1.105 (1.206).

134.6.9 FEC_symbol_error_counter_*i*

FEC_symbol_error_counter_*i*, where *i*=0 to 1, is a 32-bit counter that counts once for each 10-bit symbol corrected on FEC lane *i* when fec_align_status is true. These variables are mapped to the registers defined in 45.2.1.106 and 45.2.1.107 (1.210 to 1.213).

134.6.10 align_status

This variable is assigned the value of rx_align_status as defined by the PCS deskew state diagram shown in Figure 82–14 (see 134.5.2.2) It is mapped to the bit defined in 45.2.1.102 (1.201.15).

134.6.11 BIP_error_counter_*i*

BIP_error_counter_*i*, where *i*=0 to 3, is a 16-bit counter that holds the BIP error count for PCS lane *i* as calculated by the RS-FEC transmit function (see 134.5.2.4). These variables are mapped to the registers defined in 45.2.1.108 and 45.2.1.109 (1.230 to 1.233).

134.6.12 lane_mapping<*x*>

When the RS-FEC transmit function detects and locks to an alignment marker on FEC service interface lane *x*, the PCS lane number corresponding to the detected alignment marker is assigned to the variable lane_mapping<*x*>. These variables are mapped to the registers defined in 45.2.1.110 and 45.2.1.111 (1.250 to 1.253).

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134.6.13 block_lock<x>

These variables are assigned by the block lock state diagram shown in Figure 82–12 (see 134.5.2.1). They are mapped to the registers defined in 45.2.1.112 (1.280).

134.6.14 am_lock<x>

These variables are assigned by the alignment marker lock state diagram shown in Figure 82–13 (see 134.5.2.2). They are mapped to the registers defined in 45.2.1.114 (1.282).

134.7 Protocol implementation conformance statement (PICS) proforma for Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs[7]

134.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

134.7.2 Identification

134.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

[7] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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134.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-201x.)	

Date of Statement	

134.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
RS-FEC	Supports 50GBASE-R RS-FEC functionality	134.1.1		M	Yes [ ]
*MD	MDIO capability	45, 134.6	Registers and interface supported	O	Yes [ ] No [ ]
*BEI	Bypass error indication	134.5.3.3	Capability is supported	O	Yes [ ] No [ ]

134.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sub-layer for 50GBASE-R PHYs

134.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Skew tolerance	134.5.2.2	Maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps.	M	Yes [ ]
TF2	Lane reorder	134.5.2.3	Order the PCS lanes according to the PCS lane number	M	Yes [ ]
TF3	64B/66B to 256B/257B transcoder	134.5.2.5	tx_xcoded<256:0> constructed per 134.5.2.5	M	Yes [ ]
TF4	257-bit block transmission order	134.5.2.5	First bit transmitted is bit 0	M	Yes [ ]
TF5	Alignment maker mapping	134.5.2.6	Map to am_tx-mapped<256:0> per 134.5.2.6	M	Yes [ ]
TF6	Pad value	134.5.2.6	Set to 0 or 1 in an alternating pattern	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TF7	Alignment marker insertion	134.5.2.6	First 256 message bits to be transmitted from every 1024th codeword	M	Yes [ ]
TF8	Alignment marker insertion point	134.5.2.6	First 257-bit block inserted after am_txmapped corresponds to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective lane	M	Yes [ ]
TF9	Reed-Solomon encoder	134.5.2.7		M	Yes [ ]
TF10	Symbol distribution	134.5.2.8	Distributed to 2 FEC lanes, one 10-bit symbol at a time in a round robin distribution from the lowest to the highest numbered FEC lane	M	Yes [ ]

134.7.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	134.5.3.1	Maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder	134.5.2.3	Order the FEC lanes according to the FEC lane number	M	Yes [ ]
RF3	Reed-Solomon decoder for RS(544,514)	134.5.3.3	Corrects any combination of up to t=15 symbol errors in a codeword.	M	Yes [ ]
RF4	Reed-Solomon decoder	134.5.3.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF5	Error indication function	134.5.3.3	Corrupts 66-bit block synchronization headers for uncorrected errored codewords.	M	Yes [ ]
RF7	Error monitoring while error indication is bypassed	134.5.3.3	When the number of symbols errors in a block of 8 192 codewords exceeds K, corrupt 66-bit block synchronization headers	BEI:M	Yes [ ] N/A [ ]
RF8	Symbol error threshold for RS(544,514)	134.5.3.3	K=6380	BEI:M	Yes [ ] N/A [ ]
RF9	Alignment marker removal	134.5.3.4	am_rxmapped removed prior to transcoding	M	Yes [ ]
RF10	256B/257B to 64B/66B transcoder	134.5.3.5	rx_coded_j<65:0>, j=0 to 3 constructed per 134.5.3.5	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RF11	Block distribution	134.5.3.7	One 66-bit block at a time in a round robin fashion from the lowest to the highest numbered PCS lane	M	Yes [ ]
RF12	Alignment marker mapping	134.5.3.7	Map to am_rx_*x*, *x*=0 to 3 per 134.5.3.7	M	Yes [ ]
RF13	Alignment marker insertion point	134.5.3.7	Alignment markers immediately followed by the 66-bit blocks derived from the 257-bit blocks immediately following am_rxmapped	M	Yes [ ]

134.7.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	SLIP function	134.5.4.2.2	Ensure that all possible block positions are evaluated	M	Yes [ ]
SD2	Synchronization process	134.5.4.3	One instance per FEC lane per Figure 91–8	M	Yes [ ]
SD3	Alignment process	134.5.4.3	Per Figure 91–9	M	Yes [ ]

134.7.4.4 Delay Constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	RS-FEC Delay Constraint	134.4	No more than 25 600 BT for sum of transmit and receive path delays.	M	Yes [ ]

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135. Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P

135.1 Overview

135.1.1 Scope

This clause specifies the Physical Medium Attachment sublayer (PMA) for the families of 50 Gb/s and 100 Gb/s PAM4 Physical Layer implementations known as 50GBASE-R (see 131.1.3) and 100GBASE-P (see 80.1.4). The PMA allows the PCS (see Clause 133 and Clause 82) and FEC (see Clause 134 and Clause 91) to connect in a media-independent way with a range of physical media. The 50GBASE-R PMA can support any of the 50 Gb/s PMDs in Table 131–1 and the 100GBASE-P PMA can support any of the 100 Gb/s PAM4 PMDs according to Table 80–3 and Table 80–4a.

50GBASE-R and 100GBASE-P PHYs can be extended to support any full duplex medium requiring only that the PMD be compliant with the appropriate PMA interface.

The interfaces for the inputs of the 50GBASE-R and 100GBASE-P PMAs are defined in an abstract manner and do not imply any particular implementation. For 50GBASE-R PMAs, electrical interfaces connecting PMA sublayers, known as LAUI-2 and 50GAUI-n, are defined in Clause 135B through Clause 135G. For 100GBASE-P PMAs, electrical interfaces connecting PMA sublayers, known as 100GAUI-n, are defined in Clause 135D through Clause 135G.

135.1.2 Position of the PMA in the 50GBASE-R and 100GBASE-P sublayers

Figure 135–1 shows the relationship of the PMA sublayer (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model

135.1.3 Summary of functions

The following is a summary of the principal functions implemented (when required) by the PMA in both the transmit and receive directions:

a) Adapt the PCSL/FECL-formatted signal to the appropriate number of abstract or physical lanes.
b) Provide per-input-lane clock and data recovery.
c) Provide bit-level multiplexing.
d) Provide clock generation.
e) Provide signal drivers.
f) Optionally provide local loopback to/from the PMA service interface.
g) Optionally provide remote loopback to/from the PMD service interface.
h) Optionally provide test-pattern generation and checking.
i) Tolerate Skew Variation.
j) Perform PAM4 encoding and decoding when required

PAM4 encoding and decoding is required for 50GBASE-R PMAs where the number of physical lanes is 1 and for 100GBASE-P PMAs where the number of physical lanes is 1 or 2.

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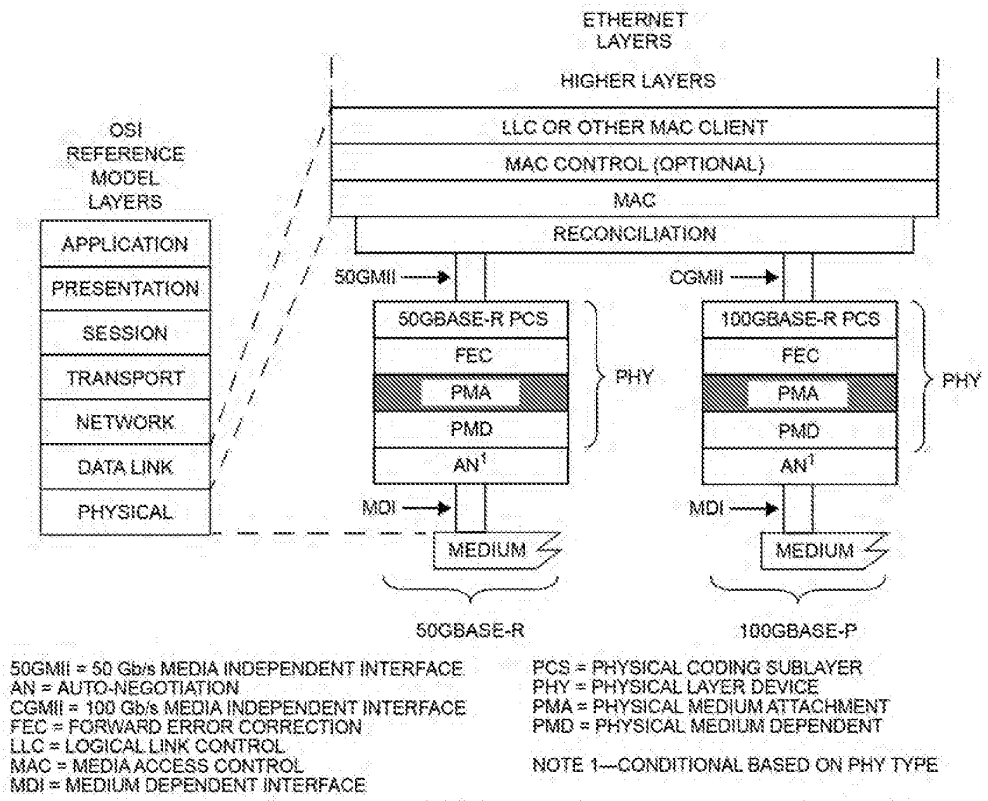


Figure 135–1—50GBASE-R and 100GBASE-P PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

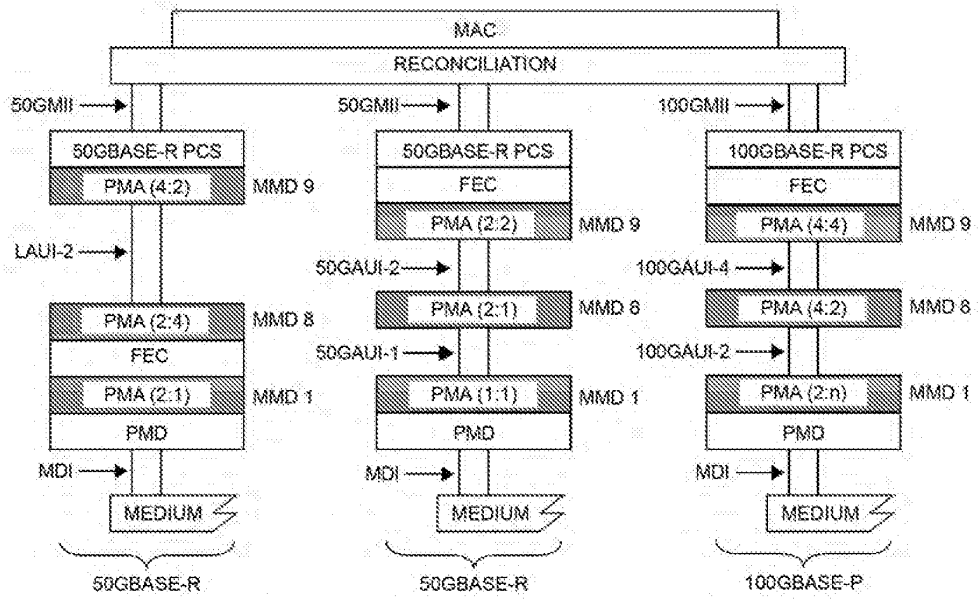
135.1.4 PMA sublayer positioning

An implementation may use one or more PMA sublayers to adapt the number and rate of the PCS lanes to the number and rate of the PMD lanes. The number of PMA sublayers required depends on the partitioning of functionality for a particular implementation. An example is illustrated in Figure 135–2. Additional examples are illustrated in Annex 135A. Each PMA maps the PCSLs/FECLs from p PMA input lanes to q PMA output lanes in the Tx direction, and from q PMA input lanes to p PMA output lanes in the Rx direction.

Management Data Input/Output (MDIO) Manageable Device (MMD) addresses 1, 8, 9, and 10 are available for addressing multiple instances of PMA sublayers (see Table 45–1 for MMD device addresses). If the PMA sublayer that is closest to the PMD is packaged with the PMD, it shares MMD 1 with the PMD. More addressable instances of PMA sublayers, each one separated from lower addressable instances by chip-to-chip interfaces, may be implemented and addressed allocating MMD addresses to PMAs in increasing numerical order going from the PMD toward the MAC. The examples shown in Figure 135–2 could be implemented with three addressable instances: MMD 1 addressing the lowest PMA sublayer (co-packaged with the PMD), MMD 8 addressing the middle PMA sublayer, and MMD 9 addressing the highest PMA sublayer (immediately below the FEC).

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100GAUI = 100 Gb/s ATTACHMENT UNIT INTERFACE
100GMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
50GAUI = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LAUI = 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

n = 1 or 2

Figure 135–2—Example 50GBASE-R and 100GBASE-P PMA layering

The number of input lanes and the number of output lanes for a PMA are always divisors of the number of PCSLs/FECLs. For PMA sublayers supporting 50GBASE-R PMDs, the number of PCSLs (above the FEC) is 4 and the number of FECLs (below the FEC) is 2. For PMA sublayers supporting 100GBASE-P PMDs, the number of FECLs is 4.

The following guidelines apply to the partitioning of PMAs:

a) The inter-sublayer service interface, defined in 131.3.1, is used for the PMA service interfaces supporting a flexible architecture with multiple PMA sublayers.
   1) An instance of this interface can only connect service interfaces with the same number of lanes, where the lanes operate at the same rate.

b) The abstract PMA service interface can be physically instantiated as a LAUI-2, 50GAUI-n, or 100GAUI-n, using associated PMAs to map to the appropriate number of lanes.

c) For physical instantiations of the PMA service interface, the PMA:IS_SIGNAL.indication is conveyed outside of this physically instantiated interface.

d) Physical instantiations of the PMA service interface define electrical and timing specification as well as requiring a receive re-timing function.

e) LAUI-2 is a physical instantiation of the PMA service interface between two adjacent 50GBASE-R PMA sublayers above the FEC.
   1) LAUI-2 provides bit-multiplexing of 4 PCSLs.
   2) LAUI-2 is a 25.78125 GBd by 2 lane NRZ physical instantiation of the 50 Gb/s connection.

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f) 50GAUI-n is a physical instantiation of the PMA service interface between two adjacent 50GBASE-R PMA sublayers below the FEC and contains 2 FECLs.
   1) 50GAUI-n provides bit-multiplexing of 2 FECLs.
   2) 50GAUI-2 is a 26.5625 GBd by 2 lane NRZ physical instantiation of the 50 Gb/s connection.
   3) 50GAUI-1 is a 26.5625 GBd by 1 lane PAM4 physical instantiation of the 50 Gb/s connection.

g) CAUI-n is a physical instantiation of the PMA service interface between two adjacent 100GBASE-R PMA (see Clause 83) sublayers above the FEC for a 100GBASE-P PHY or between adjacent sublayers below the PCS for a 100GBASE-R PHY. CAUI-n is not specified in this clause, but is listed here for completeness.
   1) CAUI-n provides bit-multiplexing of 20 PCSLs.
   2) CAUI-4 is a 25.78125 GBd by 4 lane NRZ physical instantiation of the 100 Gb/s connection. CAUI-4 is specified in Clause 83 and associated annexes.
   3) CAUI-10 is a 10.3125 GBd by 10 lane NRZ physical instantiation of the 100 Gb/s connection. CAUI-10 is specified Clause 83 and associated annexes.

h) 100GAUI-n is a physical instantiation of the PMA service interface between two adjacent 100GBASE-P PMA sublayers below the FEC for a 100GBASE-P PHY.
   1) 100GAUI-n provides bit-multiplexing of 4 FECLs.
   2) 100GAUI-4 is a 26.5625 GBd by 4 lane NRZ physical instantiation of the 100 Gb/s connection.
   3) 100GAUI-2 is a 26.5625 GBd by 2 lane PAM4 physical instantiation of the 100 Gb/s connection.

i) Opportunities for optional test-pattern generation, optional test-pattern detection, optional local loopback and optional remote loopback are dependent upon the location of the PMA sublayer in the implementation. See Figure 135–5.

j) A minimum of one PMA sublayer is required in a PHY.

k) A maximum of four PMA sublayers are addressable as MDIO MMDs.

135.2 PMA interfaces

All PMA variants for 50GBASE-R and 100GBASE-P are based on a generic specification of a bit mux function that applies to all input/output lane counts and each direction of transmission. Each direction of transmission may employ one or more such bit muxes to adapt from the appropriate number of input lanes to the appropriate number of output lanes as illustrated in Figure 135–3.

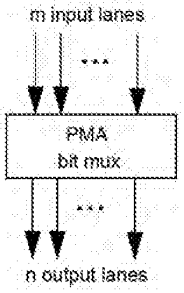


Figure 135–3—PMA bit mux used in both Tx and Rx directions

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Conceptually, the PMA bit mux operates in one direction of transmission by demultiplexing PCSLs/FECLs from m PMA input lanes and remultiplexing them into n PMA output lanes. The mapping of PCSLs/FECLs from input to output lanes is not specified. See 135.5.2 and Figure 135–4 for details.

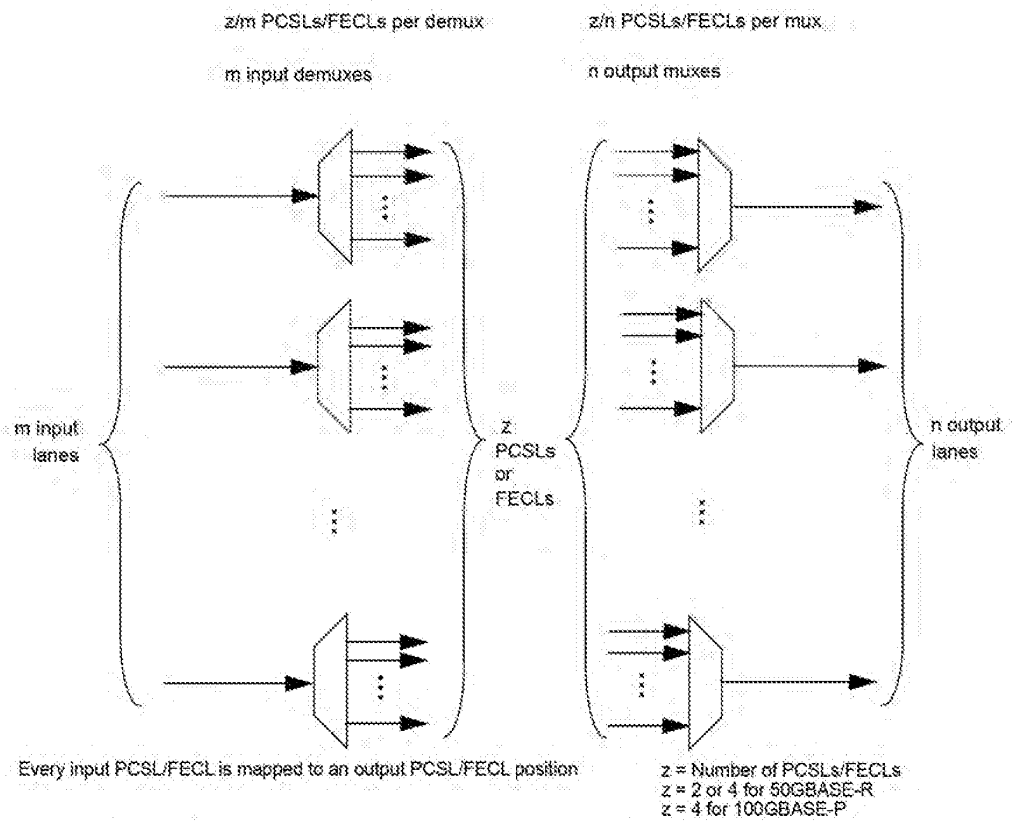


Figure 135–4—PMA bit mux operation used in both Tx and Rx directions

135.3 PMA service interface

The PMA service interface for 50GBASE-R and 100GBASE-P is an instance of the inter-sublayer service interface defined in 131.3.1. The PMA service interface primitives are summarized as follows:

PMA:IS_UNITDATA_*i*.request
PMA:IS_UNITDATA_*i*.indication)
PMA:IS_SIGNAL.indication

For a PMA service interface with p lanes, the primitives are defined for $i = 0$ to $p - 1$.

If the PMA client is the 50GBASE-R PCS, the PMA continuously sends four parallel bit streams to the PCS, each at the nominal signaling rate of the PCSL.

If a PMA client is another PMA, a 50GBASE-R PMA with p=2 physical input lanes receives NRZ symbols on each of its input lanes at 2 times the PCSL/FECL rate. A 50GBASE-R PMA with p=1 physical input lane

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receives PAM4 symbols on each of its input lanes at 2 times the PCSL/FECL rate, with each symbol formed from two bits. The bit stream represented by the input symbols carries z/p bit-multiplexed PCSLs/FECLs on each physical input lane, where z=2 (below the FEC) or z=4 (above the FEC) for 50GBASE-R.

If a PMA client is another PMA, 100GBASE-P PMA with p=4 physical input lanes receives NRZ symbols on each of its input lanes at the FECL rate. A 100GBASE-P PMA with p=1 or p=2 physical input lanes receives PAM4 symbols on each of its input lanes at 4 or 2 times, respectively, the FECL rate, with each symbol formed from two bits. The bit stream represented by the input symbols carries z/p bit-multiplexed FECLs on each physical input lane, where z=4 for 100GBASE-P.

Skew may exist between different PCSLs/FECLs received on the same physical input lane even though all PCSLs/FECLs originate from the same synchronous source, so there is independence of arrival of bits from each PCSL/FECL on each physical input lane.

In the Tx direction, if the symbol from a PMA:IS_UNITDATA_*i*.request primitive is received over a physically instantiated interface (LAUI-2, 50GAUI-n, or 100GAUI-n), clock and data are recovered on the lane receiving the symbol. If necessary, PAM4 symbols are converted to pairs of bits. Bits are routed through the PMA to an output lane through a process that may demultiplex PCSLs/FECLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs/FECLs to output lanes. If necessary, pairs of bits on output lanes are converted to PAM4 symbols. The symbols are sent on an output lane to the sublayer below using the *inst*:IS_UNITDATA_*k*.request (*k* not necessarily equal to *i*) primitive (see 135.4).

In the Rx direction, the PMA passes symbols from the input lanes to the output lanes when data is being received from every input lane from the sublayer below the PMA that has a PCSL/FECL that is routed to a particular output lane at the PMA service interface, and (if necessary) buffers are filled to allow tolerating the Skew Variation that may appear between the input lanes. PCSLs/FECLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and symbols are transferred over each output lane to the PMA client via the PMA:IS_UNITDATA_i.indication primitive. If necessary, PAM4 symbols are converted to pairs of bits on the input lanes and/or pairs of bits are converted to PAM4 symbols on the output lanes.

The PMA:IS_SIGNAL.indication primitive is generated by a Signal Indication Logic (SIL) function that reports signal health based on receipt of the *inst*:IS_SIGNAL.indication from the sublayer below, data being received on all of the input lanes from the sublayer below, buffers filled (if necessary) to accommodate Skew Variation, and symbols being sent to the PMA client on all of the output lanes. When these conditions are met, the SIGNAL_OK parameter sent to the PMA client via the PMA:IS_SIGNAL.indication primitive has the value OK. Otherwise, the SIGNAL_OK primitive has the value FAIL.

135.4 Service interface below PMA

Since the architecture supports multiple PMA sublayers for various PMD lane counts and device partitioning, there are several different sublayers that may appear below a PMA, including the FEC, PMD, or another PMA. The variable *inst* represents whichever sublayer appears below the PMA (e.g., another PMA, FEC, or PMD).

The sublayer below the PMA utilizes the inter-sublayer service interface defined in 131.3. The service interface primitives provided to the PMA are summarized as follows:

inst:IS_UNITDATA_*i*.request
inst:IS_UNITDATA_*i*.indication
inst:IS_SIGNAL.indication

The number of lanes q for the service interface matches the number of lanes expected by the PMA. The *inst*:IS_UNITDATA_*i* primitives are defined for each lane *i* = 0 to q – 1 of the service interface below the

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PMA. Note that electrical and timing specifications of the service interface are defined if the interface is physically instantiated (e.g., LAUI-2, 50GAUI-n, or 100GAUI-n), otherwise the service interface is specified only abstractly. The interface between the PMA and the sublayer below consists of q lanes for data transfer and a status indicating a good signal from the sublayer below the PMA (see Figure 135–5).

In the Tx direction, the PMA transfers symbols from the input lanes to the output lanes when data is being received via the PMA:IS_UNITDATA_i.request primitive from every input lane from the PMA client at the PMA service interface (see 135.3) that has a PCSL/FECL that is routed to this output lane, and (if necessary), buffers are filled to provide the ability to tolerate the Skew Variation that may appear between the input lanes from the PMA client, PCSLs/FECLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and symbols are transferred over each output lane to the sublayer below the PMA.

In the Rx direction, if the symbol is received over a physically instantiated interface (50GAUI-n, 100GAUI-n, or physically instantiated PMD service interface), clock and data are recovered on the lane receiving the symbol. If necessary, PAM4 symbols received on the input lanes are converted to pairs of bits. The bits are routed through the PMA to an output lane toward the PMA client through a process that may demultiplex PCSLs/FECLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs/FECLs to output lanes. If necessary, pairs of bits are converted to PAM4 symbols on the output lanes. Each symbol is sent on an output lane to the PMA client using the PMA:IS_UNITDATA_k.indication (k not necessarily equal to i) primitive at the PMA service interface.

135.5 Functions within the PMA

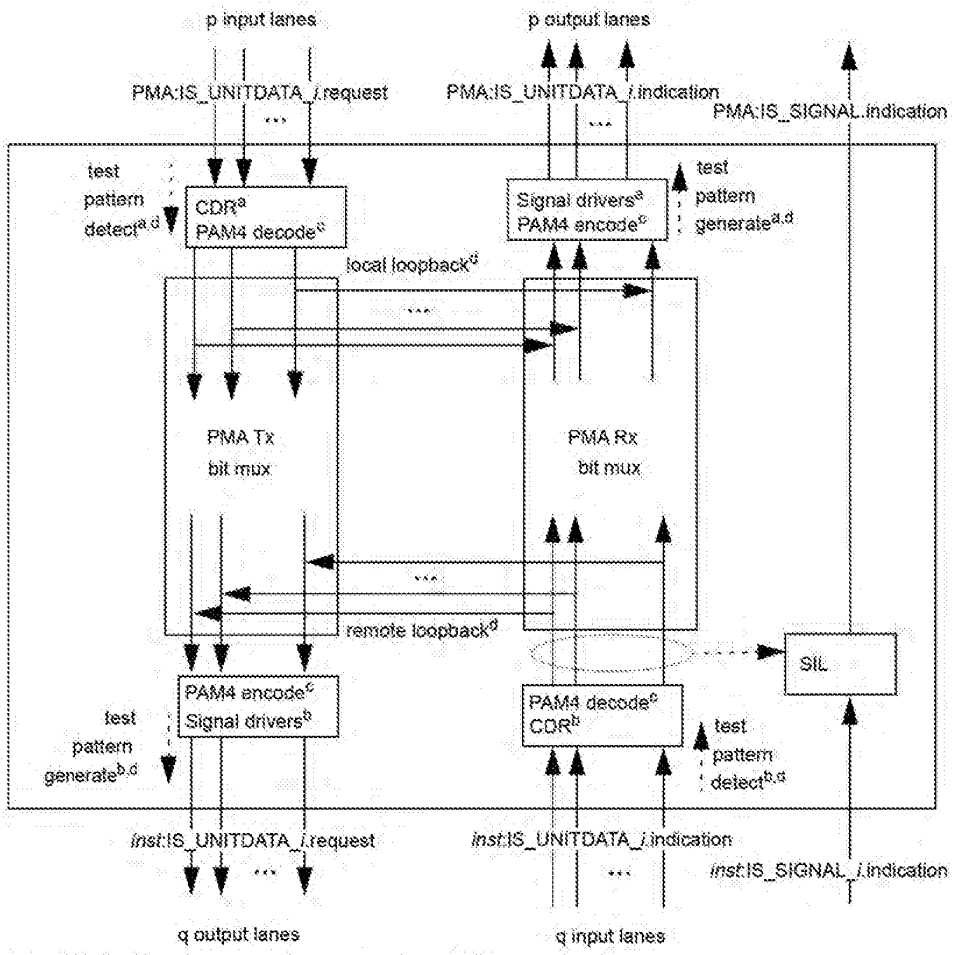
The purpose of the PMA is to adapt the PCSL/FECL-formatted signal to an appropriate number of abstract or physical lanes, to recover clock from the received signal (if appropriate), and optionally to provide test signals and loopback. Each input (Tx direction) or output (Rx direction) lane between the PMA and the PMA client carries one or more PCSLs/FECLs that are bit-multiplexed. All input and output lanes between the PMA and the PMA client carry the same number of PCSLs/FECLs and operate at the same nominal signaling rate. Likewise, each input (Rx direction) or output (Tx direction) lane between the PMA and the sublayer below the PMA carries one or more PCSLs/FECLs that are bit-multiplexed. All input and output lanes between the PMA and the sublayer below the PMA carry the same number of PCSLs/FECLs and operate at the same nominal signaling rate. As described in 135.1.4, the number of input lanes and the number of output lanes for a given PMA are divisors of 2 (below the FEC) or 4 (above the FEC) for 50GBASE-R, or 4 for 100GBASE-P, which are the number of PCSLs/FECLs for the respective PHYs.

Figure 135–5 provides the functional block diagram of a PMA. The parameters of a PMA include the following:

- The numbers of input and output lanes in each direction.
- Whether the PMA is adjacent to a physically instantiated interface (LAUI-2, 50GAUI-n, or 100GAUI-n above or below).
- Whether the PMA is adjacent to the PCS.
- Whether the PMA is adjacent to the PMD.
- Whether the PMA is adjacent to the FEC.

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inst = PMD, PMA, depending on which sublayer is below this PMA
SIL = Signal Indication Logic

[a] If LAUI-2, 50GAUI-n, or 100GAUI-n immediately above this PMA.
[b] If LAUI-2, 50GAUI-n, or 100GAUI-n immediately below this PMA or if this is the closest PMA to the PMD.
[c] If number of input or output lanes is 1 for a 50GBASE-R PMA, or 1 or 2 for a 100GBASE-P PMA.
[d] Optional.

Figure 135–5—PMA Functional Block Diagram

135.5.1 Per input-lane clock and data recovery

If the interface between the PMA client and the PMA is physically instantiated as LAUI-2, 50GAUI-n, or 100GAUI-n, the PMA shall meet the electrical and timing specifications above the PMA in Annex 135B through Annex 135G, as appropriate.

If the interface between the sublayer below the PMA and the PMA is physically instantiated as LAUI-2, 50GAUI-n, or 100GAUI-n, the PMA shall meet the electrical and timing specifications below the PMA at the service interface as specified in Annex 135B through Annex 135G, as appropriate.

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135.5.2 Bit-level multiplexing

The PMA provides bit-level multiplexing in both the Tx and Rx directions. In the Tx direction, the function is performed among the bits received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitives (for PMA client lanes $i = 0$ to $p - 1$) with the result sent to the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes $i = 0$ to $q - 1$), referencing the functional block diagram shown in Figure 135–5. The bit multiplexing behavior is illustrated in Figure 135–4.

The aggregate signal carried by the group of input lanes or the group of output lanes is arranged as a set of PCSLs/FECLs. The number of PCSLs/FECLs z is 2 FECLs (below the FEC) and 4 PCSLs (above the FEC) for 50GBASE-R interfaces and 4 FECLs for 100GBASE-P interfaces. For 50GBASE-R, the nominal bit rate R_{lane} is 12.890625 Gb/s for each PCSL and 26.5625 Gb/s for each FECL. For 100GBASE-P, the nominal bit rate R_{lane} is 26.5625 Gb/s for each FECL.

For a PMA with m input lanes (Tx or Rx direction), each input lane carries, bit multiplexed, z/m PCSLs/FECLs. Each input lane has a nominal bit rate of $z/m \times R_{lane}$. Note that the signaling rate is equal to the bit rate when the signal modulation is NRZ. The signaling rate is equal to half of the bit rate when the signal modulation is PAM4. If necessary, PAM4 symbols are converted to pairs of bits on the input lanes and/or pairs of bits are converted to PAM4 symbols on the output lanes. If bit x received on an input lane belongs to a particular PCSL/FECL, the next bit of that same PCSL/FECL is received on the same input lane at bit position $x+(z/m)$. The z/m PCSLs/FECLs may arrive in any sequence on a given input lane.

For a PMA with n output lanes (Tx or Rx direction), each output lane carries, bit multiplexed, z/n PCSLs/FECLs. Each output lane has a nominal signaling rate of $z/n \times R_{lane}$. Each PCSL/FECL is mapped from a position in the sequence on one of the m input lanes to a position in the sequence on one of the n output lanes. If bit x sent on an output lane belongs to a particular PCSL/FECL, the next bit of that same PCSL/FECL is sent on the same output lane at bit position $x + (z/n)$. The PMA shall maintain the chosen sequence of PCSLs/FECLs on all output lanes while it is receiving a valid stream of bits on all input lanes.

Each PCSL/FECL received in any temporal position on an input lane is transferred into a temporal position on an output lane. As the PCS (see Clause 133 and Clause 82) and FEC (See Clause 91 and Clause 134) have fully flexible receive logic, an implementation is free to perform the mapping of PCSLs/FECLs from input lanes to output lanes without constraint. Figure 135–6 illustrates one possible bit ordering for a 100GBASE-P 4:2 PMA bit mux. Other bit orderings are also valid.

Note that since the number of input lanes and output lanes for a 50GBASE-R or 100GBASE-P PMA is always a power of two, many PMAs converting between different numbers of lanes normally simply multiplex two or four input lanes to one output lane, or demultiplex two or four output lanes from one input lane. However, any PMA implementation which produces an allowable order of bits from all PCSLs/FECLs on the output lanes is valid.

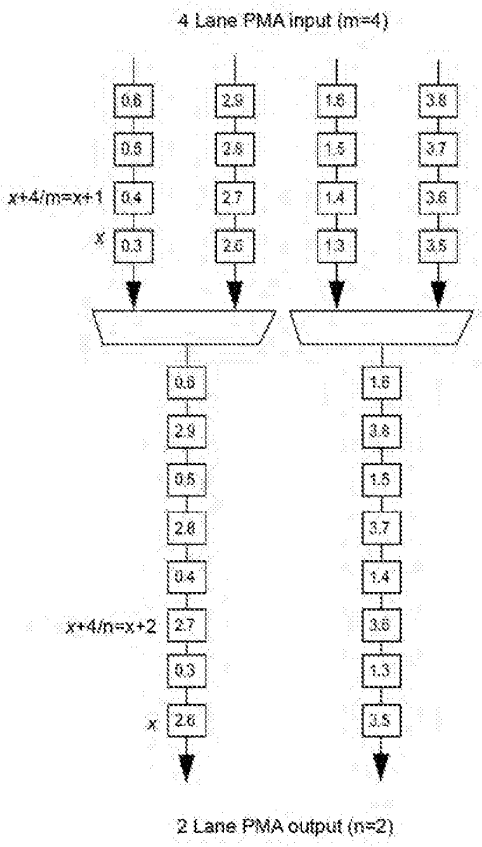
135.5.3 Skew and Skew Variation

The Skew (relative delay) between the PCSLs/FECLs must be kept within limits so that the information on the lanes can be reassembled by the PCS and FEC.

Any PMA that combines PCSLs/FECLs from different input lanes onto the same output lane must tolerate Skew Variation between the input lanes without changing the PCSL/FECL positions on the output. Skew and Skew Variation are defined in 131.5. The limits for Skew and Skew Variation at physically instantiated interfaces are specified at Skew points SP0, SP1, and SP2 in the transmit direction and SP5, SP6, and SP7 in the receive direction as defined in 131.5 and illustrated in Figure 131–3 for 50GBASE-R and as defined in 80.5 and illustrated in Figure 80–8 for 100GBASE-P.

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NOTE—i.k indicates bit k on FECL i. Skew may exist between FECLs.

Figure 135–6—Example 4:2 100GBASE-P PMA bit mux

135.5.3.1 Skew generation toward SP0

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA that sends data in the transmit direction toward the LAUI-2 (SP0 in Figure 131–3) shall produce no more than 29 ns of Skew between PCSLs and no more than 0.2 ns of Skew Variation.

135.5.3.2 Skew tolerance at SP0

In an implementation with an instantiated LAUI-2 interface, the PMA service interface that receives data in the transmit direction from the LAUI-2 (SP0 in Figure 131–3) shall tolerate the maximum amount of Skew Variation allowed at SP0 (0.2 ns) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

135.5.3.3 Skew generation toward SP1

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA that sends data in the transmit direction toward the 50GAUI-n or 100GAUI-n that is closest to the PMD (SP1 in Figure 131–3 and Figure 80–8) shall produce no more than 29 ns of Skew between FECLs toward the 50GAUI-n or 100GAUI-n and no more than 0.2 ns of Skew Variation.

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135.5.3.4 Skew tolerance at SP1

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA service interface that receives data in the transmit direction from the 50GAUI-n or 100GAUI-n (SP1 in Figure 131–3 and Figure 80–8) shall tolerate the maximum amount of Skew Variation allowed at SP1 (0.2 ns) between input lanes while maintaining the bit ordering and position of each FECL on each PMA lane in the transmit direction (toward the PMD).

135.5.3.5 Skew generation toward SP2

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, the PMA adjacent to the PMD service interface shall generate no more than 43 ns of Skew, and no more than 0.4 ns of Skew Variation between output lanes toward the PMD service interface (SP2 in Figure 80–8 and Figure 131–3). If there is a physically instantiated 50GAUI-n or 100GAUI-n as well, then the Skew measured at SP1 is limited to no more than 29 ns of Skew and no more than 0.2 ns of Skew Variation.

135.5.3.6 Skew tolerance at SP5

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, the PMA adjacent to the PMD service interface (SP5 in Figure 131–3 and Figure 80–8) shall tolerate the maximum amount of Skew Variation allowed at SP5 (0.4 ns) between output lanes from the PMD service interface while maintaining the bit ordering and position of each FECL on each PMA lane in the receive direction (toward the MAC).

135.5.3.7 Skew generation at SP6

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, at SP6 (the receive direction of the 50GAUI-n or 100GAUI-n closest to the FEC), the PMA or group of PMAs between the PMD and the 50GAUI-n or 100GAUI-n closest to the FEC shall deliver no more than 160 ns of Skew, and no more than 3.8 ns of Skew Variation between output lanes toward the 50GAUI-n or 100GAUI-n in the Rx direction. If there is a physically instantiated PMD service interface that allows the Skew to be measured, the Skew measured at SP5 is limited to no more than 145 ns of Skew and no more than 3.6 ns of Skew Variation. If there is no physically instantiated PMD service interface, the Skew measured at SP4 is limited to no more than 134 ns of Skew, and no more than 3.4 ns of Skew Variation.

135.5.3.8 Skew tolerance at SP6

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA between the 50GAUI-n or 100GAUI-n closest to the FEC and the FEC shall tolerate the maximum amount of Skew Variation allowed at SP6 (3.8 ns) between input lanes while maintaining the bit order and position of FECLs on lanes sent in the receive direction towards the MAC.

135.5.3.9 Skew generation at SP7

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA that sends data in the receive direction toward the LAUI-2 (SP7 in Figure 131–3) shall produce no more than 29 ns of Skew between PCSLs and no more than 0.2 ns of Skew Variation.

135.5.3.10 Skew tolerance at SP7

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA service interface that receives data in the receive direction from the LAUI-2 (SP7 in Figure 131–3) shall tolerate the maximum amount of Skew Variation allowed at SP7 (0.2 ns) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

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135.5.4 Delay constraints

The maximum cumulative delay contributed by up to three PMA stages in a PHY (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 135–1. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 131.4 and its references.

Table 135–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
50GBASE-R PMA	4608	9	92.16
100GBASE-P PMA	9216	18	92.16

135.5.5 Clocking architecture

A PMA with m input lanes and n output lanes shall clock the output lanes such that the bit rate of the output lanes is m/n times the bit rate of the input lanes. For input or output lanes encoded as PAM4, the symbol rate is half of the bit rate. This applies in both the Tx and Rx directions of transmission. In the case where the interfaces between the PMA client and the PMA and/or the PMA and the sublayer below the PMA are physically instantiated, the PMA may derive its input clock(s) from the electrical interface on one or more of the input lanes, and generate the output clock(s) with an appropriate PLL multiplier/divider circuit.

There is no requirement that the PMA clock all output lanes in unison. Examples of independent clocking of output lanes include the following:

— The case where the number of input and output lanes are equal (the PMA is provided for retiming and regeneration of the signal). This may be implemented without any rearrangement of PCSLs/FECLs between input lanes and output lanes (although rearrangements are allowed). Such a PMA may be implemented by driving each output lane using the clock recovered from the corresponding input lane.
— Since the number of PCSLs/FECLs is a power of 2, whenever the number of input and output lanes are unequal, each input lane could be mapped to multiple output lanes (in the case where the number of output lanes is greater), or multiple input lanes could be mapped to a single output lane.

135.5.6 Signal drivers

For cases where the interface between the PMA client and the PMA or between the PMA and the sublayer below the PMA represent a physically instantiated interface, the PMA provides electrical signal drivers for that interface. The electrical and jitter/timing specifications for these interfaces appear in

— Annex 135B for LAUI-2 C2C applications
— Annex 135C for LAUI-2 C2M applications
— Annex 135D for 50GAUI-2 and 100GAUI-4 C2C applications
— Annex 135E for 50GAUI-2 and 100GAUI-4 C2M applications
— Annex 135F for 50GAUI-1 and 100GAUI-2 C2C applications
— Annex 135G for 50GAUI-1 and 100GAUI-2 C2M applications

The modulation format is NRZ for LAUI-2, 50GAUI-2, and 100GAUI-4 and the modulation format is PAM4 for 50GAUI-1 and 100GAUI-2.

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135.5.7 PAM4 encoding

135.5.7.1 Gray coding for PAM4 encoded lanes

For lanes encoded as PAM4, the PMA transmit process shall map consecutive pairs of bits to one of four Gray-coded symbols as specified in 120.5.7.

135.5.7.2 Precoding for PAM4 encoded lanes

For lanes encoded as PAM4, the PMA shall provide 1/(1+D) mod 4 precoding capability on each transmit lane and may optionally provide 1/(1+D) mod 4 decoding capability on each receive lane.

On each transmit lane, for each Gray-coded symbol G(*j*), a precoded symbol P(*j*) shall be determined by the following algorithm, where *j* is an index indicating the symbol number:

$$P(j) = (G(j) - P(j\text{-}1)) \bmod 4 \qquad (135\text{–}1)$$

On each receive lane, for each precoded symbol P(*j*), a Gray-code symbol G(*j*) shall be determined by the following algorithm:

$$G(j) = (P(j) + P(j\text{-}1)) \bmod 4 \qquad (135\text{–}2)$$

The precoder is enabled independently for the transmitter and receiver on each lane (0 and 1) and interface (up towards the MAC and down towards the PMD). Precoding is enabled and disabled using variables precoder_up_tx_enable_*i*, precoder_up_rx_enable_*i*, precoder_down_tx_enable_*i*, precoder_down_rx_enable_*i* (where *i* is 0 or 1). If a Clause 45 MDIO is implemented, the variables precoder_up_tx_enable_*i*, precoder_up_rx_enable_*i*, precoder_down_tx_enable_*i*, precoder_down_rx_enable_*i* are accessible through register 1.600, 1.601, 1.602, and 1.603 (see 45.2.1.116h through 45.2.1.116k).

The variables precoder_up_tx_enable_i and precoder_up_rx_enable_i are always set to 0 in a PMA that does not have a physical instantiation of its service interface towards the MAC. The variables precoder_down_tx_enable_*i* and precoder_down_rx_enable_*i* are always set to 0 in a PMA that does not have a physical instantiation of its service interface towards the PMD and is not adjacent to a PMD.

In a PMA that is adjacent to a 50GBASE-CR, 50GBASE-KR, 100GBASE-CR2, 100GBASE-KR2, 200GBASE-CR4, or 200GBASE-KR4 PMD, precoder_down_tx_enable_*i* and precoder_down_rx_enable_*i* shall be set as determined by the PMD control function on lane *i* (see 136.8.11.7.5). The method by which the PMD control function affects these variables is implementation dependent.

135.5.8 PMA local loopback mode (optional)

PMA local loopback mode is optional. If it is implemented, it shall be as specified in this subclause.

The PMA sublayer may provide a local loopback function. The function involves looping back each input lane to the corresponding output lane. Each bit received from the PMA:IS_UNITDATA_*i*.request(tx_symbol) primitive is looped back toward the MAC using the PMA:IS_UNITDATA_*i*.indication(rx_symbol) primitive.

During local loopback, the PMA performs normal bit muxing of PCSLs/FECLs per 135.5.2 onto the lanes in the Tx direction toward the service interface below the PMA.

Ability to perform this function is indicated by the Local_loopback_ability status variable. If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.8.0 (45.2.1.7.15).

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A device is placed in local loopback mode when the Local_loopback_enable control variable is set to one, and removed from local loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD control 1 register (bit 1.0.0, see 45.2.1.1.5).

NOTE—Placing a network port into loopback mode can be disruptive to a network.

135.5.9 PMA remote loopback mode (optional)

PMA remote loopback mode is optional. If implemented, it shall be as described in this subclause.

Remote loopback, if provided, should be implemented in a PMA sublayer close enough to the PMD to maintain the bit sequence on each individual PMD lane. When remote loopback is enabled, each symbol received over a lane of the service interface below the PMA via *inst*:IS_UNITDATA_*i*.indication is looped back to the corresponding output lane toward the PMD via *inst*:IS_UNITDATA_*i*.request. Note that the service interface below the PMA can be provided by the PMD, FEC (LAUI-2 only), or another PMA sublayer.

During remote loopback, the PMA performs normal bit muxing of PCSLs/FECLs per 135.5.2 onto the lanes in the Rx direction towards the PMA client.

The ability to perform this function is indicated by the 50G_Remote_loopback_ability status variable for 50GBASE-R 100G_Remote_loopback_ability status variable for 100GBASE-P.

A device is placed in remote loopback mode when the Remote_loopback_enable control variable is set to one and removed from remote loopback mode when this variable is set to zero.

If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.13.15 (45.2.1.12.1).

If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD Control register 1 (bit 1.0.1, see 45.2.1.1.4).

135.5.10 PMA test patterns (optional)

Where the output lanes of the PMA appear on a physically instantiated interface LAUI-2, 50GAUI-n, 100GAUI-n or the PMD service interface (whether or not is physically instantiated), the PMA may optionally generate and detect test patterns. These test patterns are used to test adjacent-layer interfaces for an individual PMA sublayer or to perform testing between a physically instantiated interface of a PMA sublayer and external test equipment.

135.5.10.1 Test patterns for NRZ encoded signals

For a 50GBASE-R PMA with NRZ encoding, the test patterns in this clause may be supported.

135.5.10.1.1 PRBS31 test pattern

A PMA may optionally include a PRBS31 test-pattern generator on output lanes in either direction as specified in 120.5.11.1.1.

A PMA may optionally include a PRBS31 test-pattern checker on input lanes in either direction as specified in 120.5.11.1.1.

135.5.10.1.2 PRBS9 test pattern

A PMA may optionally include a PRBS9 test-pattern generator on output lanes in either direction as specified in 120.5.11.1.2.

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135.5.10.1.3 Square-wave test pattern

A PMA may optionally include a square-wave test-pattern generator on output lanes in either direction as specified in 120.5.11.1.3.

135.5.10.2 Test patterns for PAM4 encoded signals

For a 50GBASE-R PMA with PAM4 encoding, the test patterns described in this clause may be supported.

The PRBS13Q and quaternary square wave test patterns are enabled on a lane-by-lane basis. The patterns PRBS31Q and SSPRQ are enabled on all lanes of an interface at once. If a per-lane pattern is enabled on one or more of the lanes and a per-interface pattern is also enabled, the per-lane patterns are generated only on the indicated lanes and the per-interface pattern is generated on the remaining lanes. The behavior if more than one per-lane pattern is enabled for the same lane or more than one per-interface pattern is enabled is not defined.

Editor's note: JP03A and JP03B test patterns were deleted from P802.3bs. Since these patterns are required only by specifications reference from P802.3bs the related test pattern subclauses, MDIO variables, and other text were removed. This editor's note will be removed in D1.3.

135.5.10.2.1 PRBS13Q test pattern

A PMA may optionally include a PRBS13Q test-pattern generator as specified in 120.5.11.2.1.

135.5.10.2.2 PRBS31Q test pattern

A PMA may optionally include a PRBS31Q test-pattern generator as specified in 120.5.11.2.2.

135.5.10.2.3 SSPRQ test pattern

A PMA may optionally include a short stress pattern random quaternary (SSPRQ) test-pattern generator as specified in 120.5.11.2.3.

135.5.10.2.4 Square wave (quaternary) test pattern

Transmit square wave (quaternary) test-pattern generator optionally applies to each lane of the Tx direction PMA towards a physically instantiated 50GAUI-1 or 100GAUI-1, or towards a PAM4 PMD service interface whether or not it is physically instantiated as specified in 120.11.5.2.4.

135.6 PMA MDIO function mapping

The optional MDIO capability described in Clause 45 describes several variables that provide control and status information for and about the PMA. Since a given implementation may employ more than one PMA sublayer, the PMA control and status information is organized into multiple addressable instances, one for each possible PMA sublayer. See 45.2.1 and 135.1.4 for the allocation of MMD addresses to PMA sublayers. Control and status registers for MMD 8, 9, and 10 use the Extended PMA control and status registers at identical locations to those for MMD 1.

Mapping of MDIO control variables to PMA control variables is shown in Table 135–2. Mapping of MDIO status variables to PMA status variables is shown in Table 135–3. Mapping of MDIO counter to PMA

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counters is shown in Table 135–4. These tables provide the register and bit numbers for the PMA addressed as MMD 1. For implementations with multiple PMA sublayers, additional PMA sublayers use the corresponding register and bit numbers in MMDs 8, 9, and 10 as necessary.

Table 135–2—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PMA remote loopback	PMA/PMD control 1	1.0.1	Remote_loopback_enable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
Lane 1 up transmitter precoder enable	PMA precoder control up Tx	1.602.1	precoder_up_tx_enable_1
Lane 0 up transmitter precoder enable	PMA precoder control up Tx	1.602.0	precoder_up_tx_enable_0
Lane 1 up receiver precoder enable	PMA precoder control up Rx	1.603.1	precoder_up_rx_enable_1
Lane 0 up receiver precoder enable	PMA precoder control up Rx	1.603.0	precoder_up_rx_enable_0
Lane 1 down transmitter precoder enable	PMA precoder control down Tx	1.600.1	precoder_down_tx_enable_1
Lane 0 down transmitter precoder enable	PMA precoder control down Tx	1.600.0	precoder_down_tx_enable_0
Lane 1 down receiver precoder enable	PMA precoder control down Rx	1.601.1	precoder_down_rx_enable_1
Lane 0 down receiver precoder enable	PMA precoder control down Rx	1.601.0	precoder_down_rx_enable_0
PRBS31 pattern enable	PRBS pattern testing control	1.1501.7	PRBS31_enable
PRBS9 pattern enable	PRBS pattern testing control	1.1501.6	PRBS9_enable
PRBS31Q pattern enable	PRBS pattern testing control	1.1501.13	PRBS31Q_pattern_enable
SSPRQ pattern enable	PRBS pattern testing control	1.1501.14	SSPRQ_pattern_enable
Tx generator enable	PRBS pattern testing control	1.1501.3	PRBS_Tx_gen_enable
Tx checker enable	PRBS pattern testing control	1.1501.2	PRBS_Tx_check_enable
Rx generator enable	PRBS pattern testing control	1.1501.1	PRBS_Rx_gen_enable
Rx checker enable	PRBS pattern testing control	1.1501.0	PRBS_Rx_check_enable
Lane 0 SW enable	Square wave testing control	1.1510.0	Square_wave_enable_0
Lane 1 SW enable	Square wave testing control	1.1510.1	Square_wave_enable_1
Lane 2 SW enable	Square wave testing control	1.1510.2	Square_wave_enable_2
Lane 3 SW enable	Square wave testing control	1.1510.3	Square_wave_enable_3

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