Table 135–2—MDIO/PMA control variable mapping *(continued)*

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
Lane 0 PRBS13Q enable	PRBS13Q testing control	1.1512.0	PRBS13Q_enable_0
Lane 1 PRBS13Q enable	PRBS13Q testing control	1.1512.1	PRBS13Q_enable_1
Lane 2 PRBS13Q enable	PRBS13Q testing control	1.1512.2	PRBS13Q_enable_2
Lane 3 PRBS13Q enable	PRBS13Q testing control	1.1512.3	PRBS13Q_enable_3

Table 135–3—MDIO/PMA status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMA status variable
PMA local loopback ability	PMA/PMD status 2	1.8.0	Local_loopback_ability
PMA remote loopback ability	40G/100G PMA extended ability	1.13.15	100G_Remote_loopback_ability
50G PMA remote loopback ability	50G PMA extended ability	1.22.15	50G_Remote_loopback_ ability
PRBS9 Tx generator ability	Test-pattern ability	1.1500.5	PRBS9_Tx_generator_ability
PRBS9 Rx generator ability	Test-pattern ability	1.1500.4	PRBS9_Rx_generator_ability
PRBS31Tx generator ability	Test-pattern ability	1.1500.3	PRBS31_Tx_generator_ability
PRBS31Tx checker ability	Test-pattern ability	1.1500.2	PRBS31_Tx_checker_ability
PRBS31 Rx generator ability	Test-pattern ability	1.1500.1	PRBS31_Rx_generator_ability
PRBS31 Rx checker ability	Test-pattern ability	1.1500.0	PRBS31_Rx_checker_ability
Square wave test ability	Test-pattern ability	1.1500.12	Square_wave_ability
PRBS13Q Tx generator ability	Test-pattern ability	1.1500.11	PRBS13Q_gen_Tx_ability
PRBS13Q Rx generator ability	Test-pattern ability	1.1500.10	PRBS13Q_gen_Rx_ability
PRBS31Q Tx generator ability	Test-pattern ability	1.1500.9	PRBS31Q_gen_Tx_ability
PRBS31Q Rx generator ability	Test-pattern ability	1.1500.7	PRBS31Q_gen_rx_ability
PRBS31Q Tx checker ability	Test-pattern ability	1.1500.8	PRBS31Q_Tx_checker_ability
PRBS31Q Rx checker ability	Test-pattern ability	1.1500.6	PRBS31Q_Rx_checker_ability
SSPRQ Tx generator ability	Test-pattern ability	1.1500.13	SSPRQ_gen_Tx_ability

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Table 135–4—MDIO/PMA counters mapping

MDIO variable	PMA/PMD register name	Register/bit number	PMA status variable
Error counter Tx, lane 0	PRBS Tx pattern testing error counter, lane 0	1.1600	Ln0_PRBS_Tx_test_err_counter
Error counter Tx, lane 1	PRBS Tx pattern testing error counter, lane 1	1.1601	Ln1_PRBS_Tx_test_err_counter
Error counter Tx, lane 2	PRBS Tx pattern testing error counter, lane 2	1.1602	Ln2_PRBS_Tx_test_err_counter
Error counter Tx, lane 3	PRBS Tx pattern testing error counter, lane 3	1.1603	Ln3_PRBS_Tx_test_err_counter
Error counter Rx, lane 0	PRBS Rx pattern testing error counter, lane 0	1.1700	Ln0_PRBS_Rx_test_err_counter
Error counter Rx, lane 1	PRBS Rx pattern testing error counter, lane 1	1.1701	Ln1_PRBS_Rx_test_err_counter
Error counter Rx, lane 2	PRBS Rx pattern testing error counter, lane 2	1.1702	Ln2_PRBS_Rx_test_err_counter
Error counter Rx, lane 3	PRBS Rx pattern testing error counter, lane 3	1.1703	Ln3_PRBS_Rx_test_err_counter

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135.7 Protocol implementation conformance statement (PICS) proforma for Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P[8]

135.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135.7.2 Identification

135.7.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

[8] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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135.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*P50	PMA for 50GBASE-R	135.1.1		O.1	Yes [ ] No [ ]
*P100	PMA for 100GBASE-P	135.1.1		O.1	Yes [ ] No [ ]
*LNU	Number of lanes in direction of MAC	135.1.4	Divisor of number of PCS lanes	P50: M	2 [ ] 1 [ ]
				P100:M	4 [ ] 2 [ ]
*PUN	NRZ modulation used for physically instantiated PMA service interface	135.5.6		(P50*LNU=2)+ (P100*LNU=4):M	Yes [ ] N/A [ ]
*PUP	PAM4 modulation used for physically instantiated PMA service interface	135.5.6		(P50*LNU=1)+ (P100*LNU=2):M	Yes [ ] N/A [ ]
*LND	Number of lanes in the direction of PMD	135.1.4	Divisor of number of PCS lanes	P50: M	2 [ ] 1 [ ]
				P100:M	4 [ ] 2 [ ] 1 [ ]
*PDN	NRZ modulation used for physically instantiated service interface below the PMA	135.5.6		(P50*LND=2)+ (P100*LND=4):M	Yes [ ] N/A [ ]
*PDP	PAM4 modulation used for physically instantiated service interface or PMD service interface below the PMA	135.5.6		(P50*LND=1)+ (P100*LND=2)+: M	Yes [ ] N/A [ ]
MD	MDIO	135.6	Registers and interface supported	O	Yes [ ] No [ ]

135.7.4 PICS proforma tables for Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P

135.7.4.1 Functions

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Maintain lane mapping while link is in operation	135.5.2	Maintain sequence of PCSLs/FECLs on all output lanes	M	Yes [ ]

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135.7.4.2 Timing

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Skew generation toward SP0 in Tx direction	135.5.3.1	≤ 29 ns	PID:M	Yes [ ] N/A [ ]
S2	Skew Variation generation toward SP0 in Tx direction	135.5.3.1	≤ 200 ps	PID:M	Yes [ ] N/A [ ]
S3	Skew Variation tolerance at SP0	135.5.3.2	Minimum 200 ps	PIU:M	Yes [ ] N/A [ ]
S4	Skew generation toward SP1 in Tx direction	135.5.3.3	≤ 29 ns	PID:M	Yes [ ] N/A [ ]
S5	Skew Variation generation toward SP1 in Tx direction	135.5.3.3	≤ 200 ps	PID:M	Yes [ ] N/A [ ]
S6	Skew Variation tolerance at SP1	135.5.3.4	Minimum 200 ps	PIU:M	Yes [ ] N/A [ ]
S7	Skew generation toward SP2 in Tx direction	135.5.3.5	≤ 43 ns	PIP:M	Yes [ ] N/A [ ]
S8	Skew Variation generation toward SP2 in Tx direction	135.5.3.5	≤ 400 ps	PIP:M	Yes [ ] N/A [ ]
S9	Skew Variation tolerance at SP5	135.5.3.6	Minimum 3.6 ns	PIP:M	Yes [ ] N/A [ ]
S10	Skew generation toward SP6 in Rx direction	135.5.3.7	≤ 160 ns	PIU:M	Yes [ ] N/A [ ]
S11	Skew Variation generation toward SP6 in Rx direction	135.5.3.7	≤ 3.8 ns	PIU:M	Yes [ ] N/A [ ]
S12	Skew Variation tolerance at SP6	135.5.3.8	Minimum 3.8 ns	PID:M	Yes [ ] N/A [ ]
S13	Skew generation toward SP7 in Rx direction	135.5.3.9	≤ 160 ns	PIU:M	Yes [ ] N/A [ ]
S14	Skew Variation generation toward SP7 in Rx direction	135.5.3.9	≤ 3.8 ns	PIU:M	Yes [ ] N/A [ ]
S15	Skew Variation tolerance at SP7	135.5.3.10	Minimum 3.8 ns	PID:M	Yes [ ] N/A [ ]
S16	Round-trip delay limit for 50GBASE-R	135.5.4	No more than 18 432 BT or 36 pause_quanta	P50:M	Yes [ ] N/A [ ]
S17	Round-trip delay limit for 100GBASE-P	135.5.4	No more than 36 864 BT or 72 pause_quanta	P100:M	Yes [ ] N/A [ ]

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135.7.4.3 Electrical

Item	Feature	Subclause	Value/Comment	Status	Support
E1	Lane signaling rate for LAUI-2		25.78125 GBd	M	Yes [ ]
E2	Lane signaling rate for 50GAUI-2		26.5625 GBd	M	Yes [ ]
E3	Lane signaling rate for 50GAUI-1		26.5625 GBd	M	Yes [ ]
E4	Lane signaling rate for one-lane 50 Gb/s PMD service interface.		26.5625 GBd	M	Yes [ ]
E5	Lane signaling rate for 100GAUI-4		26.5625 GBd	M	Yes [ ]
E6	Lane signaling rate for 100GAUI-2		26.5625 GBd	M	Yes [ ]
E7	Lane signaling rate for two-lane PMD service interface.		26.5625 GBd	M	Yes [ ]
E8	Lane signaling rate for one-lane PMD service interface.		53.125 GBd	M	Yes [ ]
E9	Electrical and timing requirements of Annex 135B through Annex 135G as appropriate met by upstream LAUI-2, 50GAUI-n or 100GAUI-n	135.5.1, 135.5.5		PIU:M	Yes [ ] N/A [ ]
E10	Electrical and timing requirements of Annex 135B through Annex 135G as appropriate met by downstream LAUI-2, 50GAUI-n or 100GAUI-n	135.5.1, 135.5.5		PID:M	Yes [ ] N/A [ ]

135.7.4.4 Diagnostics

Item	Feature	Subclause	Value/Comment	Status	Support
*LBL	PMA local loopback	135.5.8	Supports local loopback	O	Yes [ ] No [ ]
*LBR	PMA remote loopback	135.5.9	Supports remote loopback	O	Yes [ ] No [ ]
D1	PMA local loopback implemented	135.5.8	Meets the requirements of 135.5.8	LBL:M	Yes [ ] N/A [ ]
D2	PMA remote loopback implemented	135.5.9	Meets the requirements of 135.5.9	LBR:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
D3	Send PRBS31 Tx	135.5.10.1.1		PDN:O	Yes [ ] No [ ] N/A[ ]
D4	Send PRBS31 Rx	135.5.10.1.1		PUN:O	Yes [ ] No [ ] N/A[ ]
D5	Check PRBS31 Tx	135.5.10.1.1		PUN:O	Yes [ ] No [ ] N/A[ ]
D6	Check PRBS31 Rx	135.5.10.1.1		PDN:O	Yes [ ] No [ ] N/A[ ]
D7	Send PRBS9 Tx	135.5.10.1.2		PDN:O	Yes [ ] No [ ] N/A[ ]
D8	Send PRBS9 Rx	135.5.10.1.2		PUN:O	Yes [ ] No [ ] N/A[ ]
D9	Send NRZ square wave Tx	135.5.10.1.3		PDN:O	Yes [ ] No [ ] N/A[ ]
D10	Send PRBS13Q Tx	135.5.10.2.1		PDP:O	Yes [ ] No [ ] N/A[ ]
D11	Send PRBS13Q Rx	135.5.10.2.1		PUP:O	Yes [ ] No [ ] N/A[ ]
D12	Send PRBS31Q Tx	135.5.10.2.2		PDP:O	Yes [ ] No [ ] N/A[ ]
D13	Send PRBS31Q Rx	135.5.10.2.2		PUP:O	Yes [ ] No [ ] N/A[ ]
D14	Check PRBS31Q Tx	135.5.10.2.2		PUP:O	Yes [ ] No [ ] N/A[ ]
D15	Check PRBS31Q Rx	135.5.10.2.2		PDP:O	Yes [ ] No [ ] N/A[ ]
D16	Send SSPRQ Tx	135.5.10.2.3		PDP:O	Yes [ ] No [ ] N/A[ ]
D17	Send quaternary square wave Tx	135.5.10.2.4		PDP:O	Yes [ ] No [ ] N/A[ ]

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135.7.7 Encoding

Item	Feature	Subclause	Value/Comment	Status	Support
E1	PMA supports Gray coding	135.5.7.2		PUP+PDP:M	Yes [ ] N/A [ ]
E2	PMA supports Tx precoding	135.5.7.2		PUP+PDP:M	Yes [ ] N/A [ ]
E3	PMA supports Rx precoding	135.5.7.2		PUP+PDP:O	Yes [ ] No [ ] N/A [ ]

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136. Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136.1 Overview

This clause specifies the 50GBASE-CR PMD, the 100GBASE-CR2 PMD, the 200GBASE-CR4 PMD, and the baseband medium. The specifications for the three PMDs are similar, except for the number of lanes and associated parameters and the MDI.

There are three associated annexes. Annex 136A provides information on parameters with test points that may not be testable in an implemented system. Annex 136B specifies test fixtures. Annex 136C describes 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 host and cable assembly form factors.

When forming a complete Physical Layer, a PMD shall be connected as illustrated in Figure 136–1, to the appropriate sublayers (as specified in Table 136–1, Table 136–2, and Table 136–3), to the medium through the appropriate MDI, and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 136–1—Physical Layer clauses associated with the 50GBASE-CR PMD

Associated clause	50GBASE-CR
132—RS	Required
132—50GMII[a]	Optional
133—PCS for 50GBASE-R	Required
134—RS-FEC	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135D—50GAUI-2 C2C	Optional
135F—50GAUI-1 C2C	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The 50GMII is an optional interface. However, if the 50GMII is not implemented, a conforming implementation must behave functionally as though the RS and 50GMII were present.

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Table 136–2—Physical Layer clauses associated with the 100GBASE-CR2 PMD

Associated clause	100GBASE-CR2
80—RS	Required
80—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R	Optional[b]
83A—CAUI-10	Optional
83D—CAUI-4 C2C	Optional
135—PMA for 100GBASE-P	Required
135D—100GAUI-4 C2C	Optional
135F—100GAUI-2 C2C	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.
[b]PMA for 100GBASE-R is required when either CAUI-10 or CAUI-4 is used.

Table 136–3—Physical Layer clauses associated with the 200GBASE-CR4 PMD

Associated clause	200GBASE-CR4
117—RS	Required
117—200GMII[a]	Optional
119—PCS for 200GBASE-R	Required
120—PMA for 200GBASE-R	Required
120B—200GAUI-8 C2C	Optional
120D—200GAUI-4 C2C	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The 200GMII is an optional interface. However, if the 200GMII is not implemented, a conforming implementation must behave functionally as though the RS and 200GMII were present.

For the 50GBASE-CR and 100GBASE-CR2 PHYs, in order to support the required frame loss ratio (see 1.4.223) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are required to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 10^{-10} after processing by the RS-FEC (Clause 134 or Clause 91) and the PCS (Clause 133 or Clause 82) if there are negligible errors due to other electrical interfaces (50GAUI-n or 100GAUI-n). If the PMD and

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PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 10^{-10}.

For the 200GBASE-CR4 PHY, in order to support the required frame loss ratio (see 1.4.223) of less than 6.2×10^{-11} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are required to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 9.2×10^{-13} after processing by the PCS (Clause 119) if there are negligible errors due to other electrical interfaces (200GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 9.2×10^{-13}.

A compliant input signal is a transmitter output of a compliant PHY that has passed through a compliant cable assembly.

50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Figure 136–1 shows the relationship of the 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMD sublayers and MDIs to the ISO/IEC Open System Interconnection (OSI) reference model.

136.2 Conventions

Clause 136 describes three PMDs, 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMD, which have one, two, and four lanes, respectively. For efficient description, the parameter n is used to describe the number of lanes in a specific PMD. Accordingly, n = 1 for 50GBASE-CR, n = 2 for 100GBASE-CR2, and n = 4 for 200GBASE-CR4.

The parameter *i* is used as an index or a suffix to identify a specific lane, and takes the values 0 to n – 1.

Within this clause, the unqualified term "PMD" refers to any of 50GBASE-CR PMD, 100GBASE-CR2 PMD, or 200GBASE-CR4 PMD.

136.3 PMD service interfaces

This subclause specifies the services provided by the 50GBASE-CR, 100GBASE-CR2 and 200GBASE-CR4 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

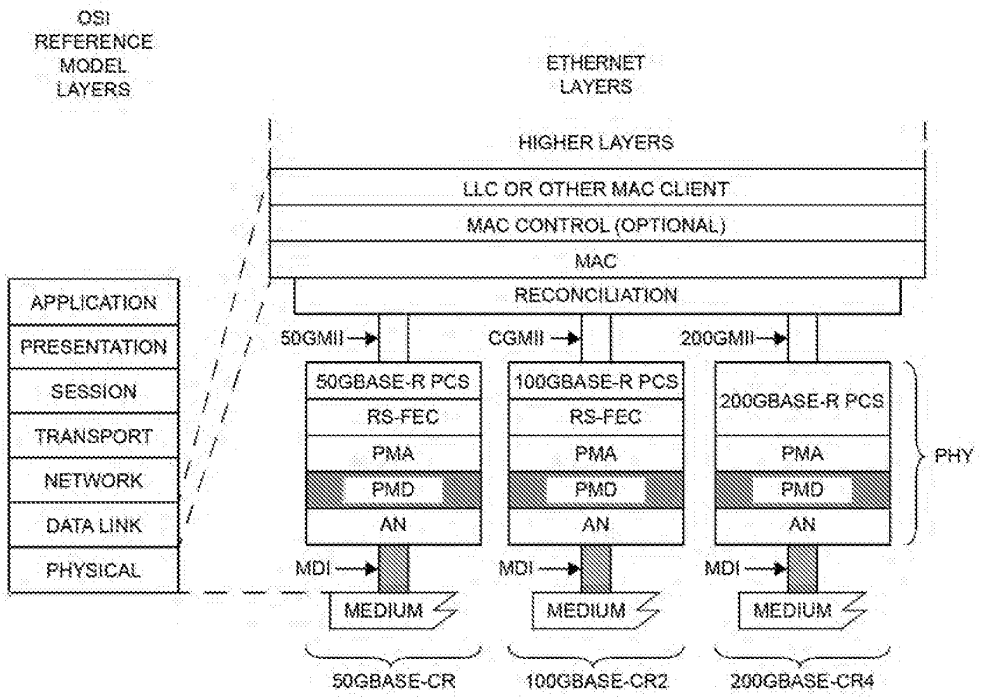
The 50GBASE-CR PMD service interface is an instance of the inter-sublayer service interface defined in 131.3, with a single symbol stream (n = 1).

The 100GBASE-CR2 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with the exception that there are two parallel symbol streams (n = 2).

The 200GBASE-CR4 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with four parallel symbol streams (n = 4).

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200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 136–1—50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 50GBASE-SR PMD has a single symbol stream, hence $i = 0$.

The 100GBASE-SR2 PMD has two parallel symbol streams, hence $i = 0$ to 1.

The 200GBASE-SR4 PMD has four parallel symbol streams, hence $i = 0$ to 3.

In the transmit direction, the PMA continuously sends n streams of PAM4 symbols to the PMD, one per lane, using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.6525 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

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In the receive direction, the PMD continuously sends *n* streams of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, one per lane, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.6525 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable Global_PMD_signal_detect as defined in 136.8.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_OK is FAIL, the PMD:IS_UNITDATA_*i*.indication parameter is undefined.

136.4 PCS requirements for Auto-Negotiation (AN) service interface

The PCSs associated with the 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMDs are required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 133.4, 82.6, and 119.6.)

50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR-4 PHYs may be extended using chip-to-chip (C2C) 50GAUI-n/LAUI-2, 100GAUI-n/CAUI-n, and 200GAUI-n, respectively, as physical instantiations of the inter-sublayer service interface between devices. If such extension is used, then the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

136.5 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the PMD and AN including the medium in one direction shall be no more than the maximum delays listed in Table 136–4. It is assumed that the one-way delay through the medium is no more than 20 ns.

Table 136–4—Delay constraints

PMD	Maximum (bit times)[a]	Maximum (pause_quanta)[b]	Maximum (ns)
50GBASE-CR	2048	4	40.96
100GBASE-CR2	4096	8	40.96
200GBASE-CR4	8192	16	40.96

[a]One bit time is equal to 20 ps for 50GBASE-CR, 10 ps for 100GBASE-CR2, and 5 ps for 200GBASE-CR4. (See 1.4.117 for the definition of bit time.)
[b]One pause_quantum is equal to 10.24 ns for 50GBASE-CR, 5.12 ns for 100GBASE-CR2, and 2.56 ns for 200GBASE-CR4. (See 31B.2 for the definition of pause_quanta.)

Descriptions of overall system delay constraints can be found in 131.4 for 50GBASE-CR, in 80.4 for 100GBASE-CR2, and in 116.4 for 200GBASE-CR4.

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136.6 Skew constraints

The Skew (relative delay) between the PCS or FEC lanes must be kept within limits so that the information on the PCS or FEC lanes can be reassembled by the PCS or FEC. The Skew Variation must also be limited to ensure that a given PCS or FEC lane always traverses the same physical lane.

136.6.1 Skew Constraints for 50GBASE-CR

Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2.

136.6.2 Skew Constraints for 100GBASE-CR2 and 200GBASE-CR4

Skew and Skew Variation are defined in 80.5 and 116.5 and specified at the points SP1 to SP6 shown in Figure 80–8 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5 and 116.5.

136.7 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD

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control variables as shown in Table 136–5, and MDIO status bits to PMD status variables as shown in Table 136–6.

Table 136–5—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 3 to PMD transmit disable 2[a]	PMD transmit disable	1.9.4:3	PMD_transmit_disable_3, PMD_transmit_disable_2
PMD transmit disable 1[b]	PMD transmit disable	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable	1.9.1	PMD_transmit_disable_0
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable
Polynomial identifier 3[a]	PMD training pattern lane 3	1.1453.12:11	identifier_3
Seed 3[a]	PMD training pattern lane 3	1.1453.10:0	seed_3
Polynomial identifier 2[a]	PMD training pattern lane 2	1.1452.12:11	identifier_2
Seed 2[a]	PMD training pattern lane 2	1.1452.10:0	seed_2
Polynomial identifier 1[b]	PMD training pattern lane 1	1.1451.12:11	identifier_1
Seed 1[b]	PMD training pattern lane 1	1.1451.10:0	seed_1
Polynomial identifier 0	PMD training pattern lane 3	1.1450.12:11	identifier_0
Seed 0	PMD training pattern lane 3	1.1450.10:0	seed_0
Initial condition request 3[a]	PMD training LP control lane 3	1.1123.13:12	ic_req (lane 3)
Coefficient select 3[a]	PMD training LP control lane 3	1.1123.4:2	coef_sel (lane 3)
Coefficient request 3[a]	PMD training LP control lane 3	1.1123.1:0	coef_req (lane 3)
Initial condition request 2[a]	PMD training LP control lane 2	1.1122.13:12	ic_req (lane 2)
Coefficient select 2[a]	PMD training LP control lane 2	1.1122.4:2	coef_sel (lane 2)
Coefficient request 2[a]	PMD training LP control lane 2	1.1122.1:0	coef_req (lane 2)
Initial condition request 1[b]	PMD training LP control lane 1	1.1121.13:12	ic_req (lane 1)
Coefficient select 1[b]	PMD training LP control lane 1	1.1121.4:2	coef_sel (lane 1)
Coefficient request 1[b]	PMD training LP control lane 1	1.1121.1:0	coef_req (lane 1)
Initial condition request 0	PMD training LP control lane 0	1.1120.13:12	ic_req (lane 0)
Coefficient select 0	PMD training LP control lane 0	1.1120.4:2	coef_sel (lane 0)
Coefficient request 0	PMD training LP control lane 0	1.1120.1:0	coef_req (lane 0)

[a]Available only in 200GBASE-CR4.
[b]Available only in 100GBASE-CR2 and 200GBASE-CR4.

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Table 136–6—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 2[a]	PMD receive signal detect	1.10.4:3	PMD_signal_detect_3 to PMD_signal_detect_2
PMD receive signal detect 1[b]	PMD receive signal detect	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect	1.10.1	PMD_signal_detect_0
Receiver status 3[a]	BASE-R PMD status	1.151.12	rx_trained_3
Frame lock 3[a]	BASE-R PMD status	1.151.13	local_frame_lock_3
Start-up protocol status 3[a]	BASE-R PMD status	1.151.14	training_3
Training failure 3[a]	BASE-R PMD status	1.151.15	training_failure_3
Receiver status 2[a]	BASE-R PMD status	1.151.8	rx_trained_2
Frame lock 2[a]	BASE-R PMD status	1.151.9	local_frame_lock_2
Start-up protocol status 2[a]	BASE-R PMD status	1.151.10	training_2
Training failure 2[a]	BASE-R PMD status	1.151.11	training_failure_2
Receiver status 1[b]	BASE-R PMD status	1.151.4	rx_trained_1
Frame lock 1[b]	BASE-R PMD status	1.151.5	local_frame_lock_1
Start-up protocol status 1[b]	BASE-R PMD status	1.151.6	training_1
Training failure 1[b]	BASE-R PMD status	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status	1.151.0	rx_trained_0
Frame lock 0	BASE-R PMD status	1.151.1	local_frame_lock_0
Start-up protocol status 0	BASE-R PMD status	1.151.2	training_0
Training failure 0	BASE-R PMD status	1.151.3	training_failure_0
Receiver ready 3[a]	PMD training LP status lane 3	1.1223.15	remote_rx_ready (lane 3)
Modulation and precoding status 3[a]	PMD training LP status lane 3	1.1223.11:10	tp_mode (lane 3)
Receiver frame lock 3[a]	PMD training LP status lane 3	1.1223.9	remote_tf_lock (lane 3)
Initial condition status 3[a]	PMD training LP status lane 3	1.1223.8	ic_sts (lane 3)
Coefficient status 3[a]	PMD training LP status lane 3	1.1223.2:0	coef_sts (lane 3)
Receiver ready 2[a]	PMD training LP status lane 2	1.1222.15	remote_rx_ready (lane 2)
Modulation and precoding status 2[a]	PMD training LP status lane 2	1.1222.11:10	tp_mode (lane 2)
Receiver frame lock 2[a]	PMD training LP status lane 2	1.1222.9	remote_tf_lock (lane 2)
Initial condition status 2[a]	PMD training LP status lane 2	1.1222.8	ic_sts (lane 2)

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Table 136–6—MDIO/PMD status variable mapping *(continued)*

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Coefficient status 2[a]	PMD training LP status lane 2	1.1222.2:0	coef_sts (lane 2)
Receiver ready 1[b]	PMD training LP status lane 1	1.1221.15	remote_rx_ready (lane 1)
Modulation and precoding status 1[b]	PMD training LP status lane 1	1.1221.11:10	tp_mode (lane 1)
Receiver frame lock 1[b]	PMD training LP status lane 1	1.1221.9	remote_tf_lock (lane 1)
Initial condition status 1[b]	PMD training LP status lane 1	1.1221.8	ic_sts (lane 1)
Coefficient status 1[b]	PMD training LP status lane 1	1.1221.2:0	coef_sts (lane 1)
Receiver ready 0	PMD training LP status lane 0	1.1220.15	remote_rx_ready (lane 0)
Modulation and precoding status 0	PMD training LP status lane 0	1.1220.11:10	tp_mode (lane 0)
Receiver frame lock 0	PMD training LP status lane 0	1.1220.9	remote_tf_lock (lane 0)
Initial condition status 0	PMD training LP status lane 0	1.1220.8	ic_sts (lane 0)
Coefficient status 0	PMD training LP status lane 0	1.1220.2:0	coef_sts (lane 0)

[a]Available only in 200GBASE-CR4.
[b]Available only in 100GBASE-CR2 and 200GBASE-CR4.

136.8 PMD functional specifications

136.8.1 Link block diagram

One direction of a 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4 link is shown in Figure 136–2.

Note that the source lane (SL) signals SL_i<p> and SL_i<n> are the positive and negative sides of the transmitter's differential signal pair on lane *i* and the destination lane (DL) signals DL_i<p> and DL_i<n> are the positive and negative sides of the receiver's differential signal pair on lane *i*.

For purposes of system conformance, the PMD sublayer is standardized at the test points described in this subclause.

The electrical transmit signal is defined at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 136.9.3 are made at TP2 utilizing the test fixture specified in 136B.1.1.

The electrical receive signal is defined at TP3. Unless specified otherwise, all receiver measurements and tests defined in 136.9.4 are performed at TP3 utilizing the test fixture specified in 136B.1.1.

A mated connector pair has been included in both the transmitter and receiver specifications defined in 136.9.3 and 136.9.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is provided in 92.8.3.6. Annex 136A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system.

The channel (see 136.9) is defined between the transmitter (TP0) and receiver (TP5) blocks to include the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss, as illustrated in Figure 136–2. All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 136–2. The cable assembly test fixture of 136B.1.1, or its

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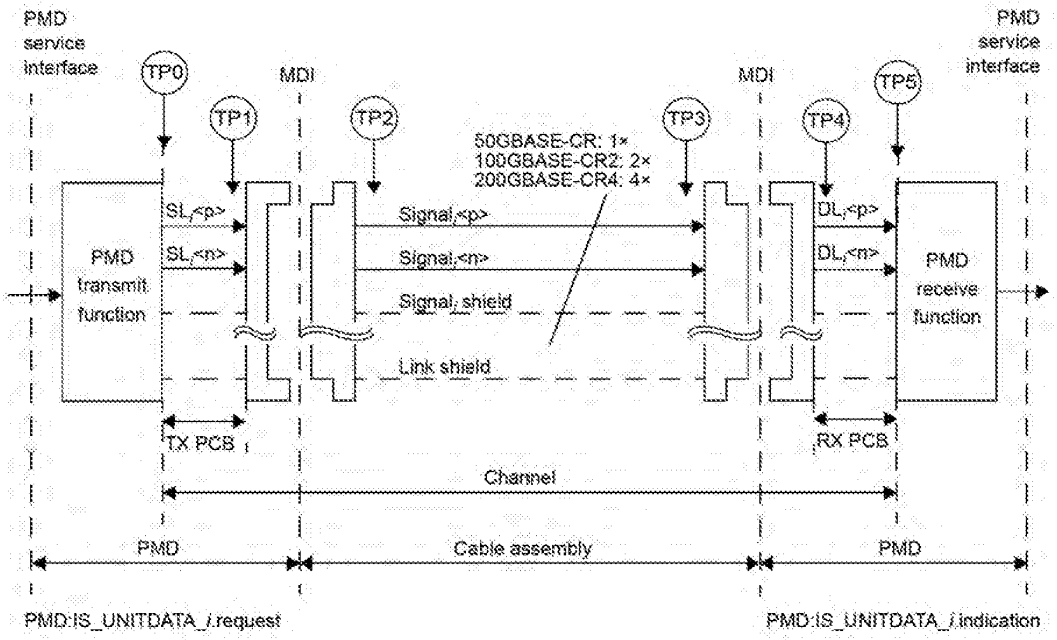


Figure 136–2—50GBASE-CR, 100GBASE-CR2 or 200GBASE-CR4 link (one direction is illustrated)

equivalent, is required for measuring the cable assembly specifications in 136.10 at TP1 and TP4. Two mated connector pairs and the cable assembly test fixture have been included in the cable assembly specifications defined in 136.10. Transmitter and receiver differential controlled impedance printed circuit board insertion losses defined between TP0 and the MDI and between the MDI and TP5, respectively, are provided informatively in 136A.4.

Table 136–7 describes the defined test points illustrated in Figure 136–2.

Table 136–7—Test points

Test points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 136–2. The cable assembly test fixture of 136B.1.1, or its equivalent, is required for measuring the cable assembly specifications in 136.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 136.9.3 and 136.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 92.8.3.6.
TP2	Unless specified otherwise, all transmitter measurements defined in 136.9.3 are made at TP2 utilizing the test fixture specified in 136B.1.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 136.9.4 are made at TP3 utilizing the test fixture specified in 136B.1.1.

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136.8.2 PMD transmit function

The PMD transmit function has two operating modes, DATA and TRAINING. The operating mode is controlled by the PMD control state diagram (Figure 136–7).

When operating in DATA mode, the PMD transmit function shall convert the symbol stream requested by the PMD service interface message PMD:IS_UNITDATA_*i*.request(tx_symbol) of each lane into an electrical signal, and deliver the electrical signals to the MDI, according to the transmit electrical specifications in 136.9.3. The highest differential output voltage (SL_i<p> minus SL_i<n>) shall correspond to tx_symbol = three and the lowest differential output voltage shall correspond to tx_symbol = zero.

When operating in TRAINING mode, the PMD transmit function shall convert the symbol stream generated by the PMD control function of each lane into an electrical signal, and deliver the electrical signals to the MDI, according to the transmit electrical specifications in 136.9.3. The highest differential output voltage (SL_i<p> minus SL_i<n>) shall correspond to the symbol 3 and the lowest differential output voltage shall correspond to the symbol 0.

136.8.3 PMD receive function

The PMD receive function shall convert the electrical signal from each of the lanes on the MDI into a symbol stream for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_*i*.indication(rx_symbol). The highest differential input voltage (DL_i<p> minus DL_i<n>) shall correspond to rx_symbol = three and the lowest differential input voltage shall correspond to rx_symbol = zero.

136.8.4 PMD global signal detect function

For the 50GBASE-CR PMD, the variable Global_PMD_signal_detect is set to PMD_signal_detect_0 (see 136.8.5). For the 100GBASE-CR2 and 200GBASE-CR4 PMDs, the variable Global_PMD_signal_detect is set to the logical AND of the values of PMD_signal_detect_*i* from each of the PMD lanes.

136.8.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function is used by the PMD to indicate the successful completion of the start-up protocol by the PMD control function (see 136.8.11). PMD_signal_detect_*i* shall be set to zero when signal_detect on lane *i* is set to false, and to one when signal_detect on lane *i* is set to true. The signal_detect variables are set independently on each lane by the PMD control state diagram (Figure 136–7).

If training is disabled by the management variable mr_training_enable (see 136.7), PMD_signal_detect_*i* shall be set to one for all lanes.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 136.7.

136.8.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional. When implemented, it allows the transmitters on all lanes to be disabled with a single variable.

When Global_PMD_transmit_disable variable is set to one, this function shall turn off all the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max.) with Tx disabled in Table 136–11.

If a PMD fault (136.8.8) is detected, then the PMD may set Global_PMD_transmit_disable to one.

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136.8.7 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function allows the transmitter in each lane to be selectively disabled.

When a PMD_transmit_disable_*i* variable is set to one, this function shall turn off the transmitter in lane *i* so that it drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max.) with Tx disabled in Table 136–11.

If a PMD fault (136.8.8) is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the transmitter in each lane.

If MDIO is not implemented, an alternative method shall be provided to access the PMD_transmit_disable_*i* variables in order to enable independently disabling each transmit lane for testing purposes.

136.8.8 PMD fault function

PMD_fault is the logical-OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault. If the MDIO interface is implemented, then PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

136.8.9 PMD transmit fault function (optional)

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault.

If PMD_transmit_fault is set to one, then Global_PMD_transmit_disable should also be set to one.

If the MDIO interface is implemented, then PMD_transmit_fault shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

136.8.10 PMD receive fault function (optional)

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall be mapped to the Receive fault bit as specified in 45.2.1.7.5.

136.8.11 PMD control function

The PMD control function performs the PMD start-up protocol. This protocol facilitates timing recovery and equalization while providing a mechanism through which the receiver can configure the transmitter to optimize performance. The protocol supports these functions through the continuous exchange of fixed-length training frames.

The PMD shall implement one instance of the PMD control function described in this subclause for each lane. The PMD control functions operate independently on each lane.

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136.8.11.1 Training frame structure

The training frame is a sequence of PAM4 symbols whose values correspond to the possible values of the tx_symbol and rx_symbol variables (the symbol values 0, 1, 2, and 3 correspond to tx_symbol or rx_symbol values zero, one, two, and three, respectively). The structure of a training frame is shown in Figure 136–3.

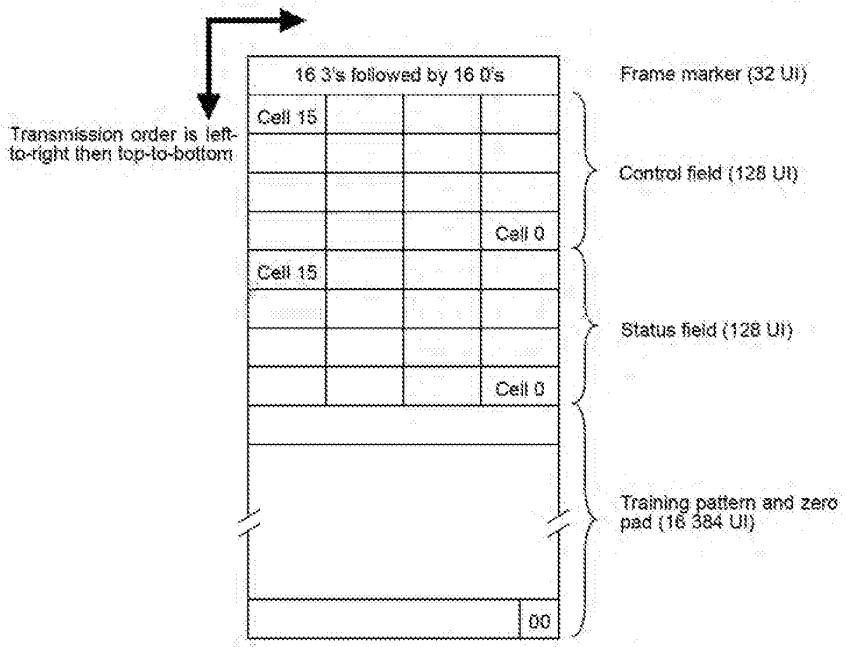


Figure 136–3—Training frame structure

136.8.11.1.1 Frame marker

Training frames are delimited by a specific sequence of PAM4 symbols. The training frame marker is a run of 16 consecutive "3" symbols followed by a run of 16 consecutive "0" symbols. This sequence is not found in the control field, status field, or training pattern and it uniquely identifies the beginning of a training frame.

136.8.11.1.2 Control and status fields

The control field comprises 16 bits with the structure defined in 136.8.11.2. The status field comprises 16 bits with the structure defined in 136.8.11.3.

Each bit of the control and status fields is sent as a differential Manchester encoded cell where each cell is eight unit intervals in length. The specific rules for this encoding follow.

a) A transition from 0 to 3 or from 3 to 0 occurs at the start of the cell.

b) A transition from 0 to 3 or from 3 to 0 at the midpoint of the cell, i.e., four unit intervals from the transition at the beginning of the cell, corresponds to a logical one.

c) The absence of a transition at the midpoint of the cell corresponds to a logical zero.

The control field is transmitted immediately after the frame marker where the first cell transmitted corresponds to the highest bit index in the field. The status field is transmitted immediately after the control field where the first cell transmitted corresponds to the highest bit index in the field.

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136.8.11.1.3 Training pattern

The training pattern is the result of a training pattern generator equivalent to the structure shown in Figure 136–4.

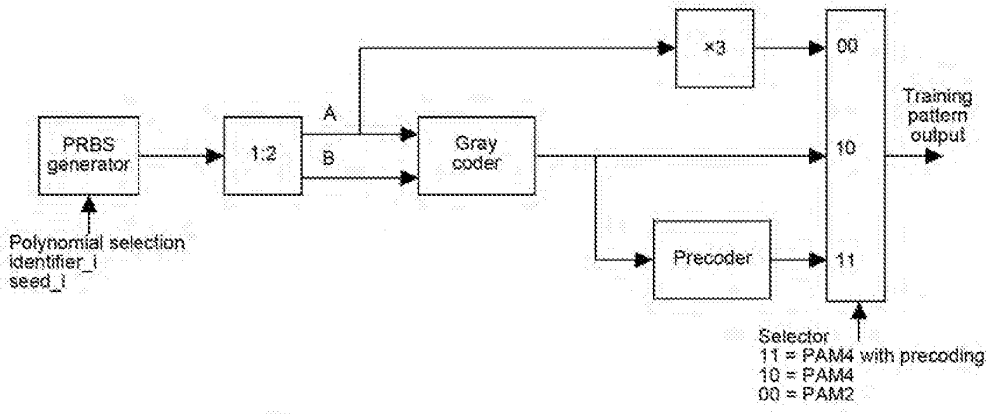


Figure 136–4—Training pattern generator

A set of four PRBS generator polynomials are defined to minimize correlated interference between PMDs, or physical lanes within a PMD, during the start-up protocol. The PRBS generator for each lane shall implement each of four generator polynomials defined in Table 136–8. The polynomial used in each lane *i* is selectable by identifier_*i*. The default identifier for each lane is its lane number (e.g., the default value for identifier_0 is 0 which selects polynomial_0). A sample implementation of the PRBS generator for identifier_*i* = 0 is shown in Figure 136–5.

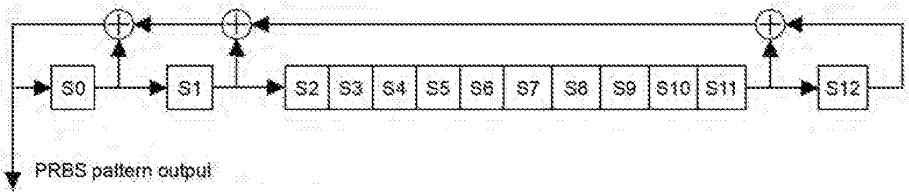


Figure 136–5—Training pattern PRBS generator (identifier_*i* = 0)

At the start of the training pattern, the state of the PRBS generator shall be set to the value seed_*i*. The default value of seed_*i* shall be the value given in Table 136–8 for *n* = *i*. A seed of all zeros is not valid.

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The polynomials for each identifier value *n* and the default seeds, as well as the first 13 symbols of the training pattern for each modulation and precoding mode, using the default seed, are provided in Table 136–8.

Table 136–8—Training patterns

n	Polynomial_*n*, *G*(*x*)	Default seed bits[a]	Initial output, PAM2	Initial output, PAM4	Initial output, PAM4 with precoding
0	$1+x+x^2+x^{12}+x^{13}$	0000010101011	0030330330000	1031320220111[b]	1301200200101
1	$1+x^2+x^5+x^7+x^{13}$	0011101000001	3030303030333	3030213021333	3122012201212
2	$1+x^2+x^4+x^8+x^{13}$	1001000101100	0303333033030	1212332133031	1102120121301
3	$1+x^2+x^3+x^9+x^{13}$	0100010000010	3330300030330	2231210121221	2032013201110

[a]The leftmost bit in the sequence corresponds to the initial value of S0 and the rightmost bit corresponds to the initial value of S12.
[b]This is equivalent to the PRBS13Q test pattern defined in 120.5.11.2.3.

For a given configuration of the PRBS generator, there are three possible training patterns. The construction of each training pattern begins by demultiplexing the PRBS generator output into pairs of bits {A, B} where A corresponds to the 1st, 3rd, 5th, etc. bits output by the PRBS generator and B corresponds to the 2nd, 4th, 6th, etc. bits output by the PRBS generator. There is a new pair of bits each unit interval which implies that the PRBS generator is required to generate bits at twice the signaling rate. Given these pairs of bits, the three different training patterns correspond to three modulation and precoding modes: PAM2, PAM4, PAM4 with precoding.

When the modulation and precoding mode is set to PAM2, the training pattern is the sequence of 16 382 PAM4 symbols derived by mapping only the A bits such that logical 0 is transmitted as 0 and logical 1 is transmitted as 3.

When the modulation and precoding mode is set to PAM4, the training pattern is the sequence of 16 382 PAM4 symbols derived by Gray coding the {A, B} pairs as specified in 135.5.7.1.

When the modulation and precoding mode is set to PAM4 with precoding, the training pattern is the sequence of 16 382 PAM4 symbols derived by Gray coding the {A, B} pairs as specified in 135.5.7.1 and precoding the result as specified in 135.5.7.2. The precoder state is initialized to 0 at the beginning of each training pattern, so that P(j=0) in Equation (135–1) is set to 0.

The modulation and precoding mode is set to PAM2 upon entry to the INITIALIZE state of the PMD control state diagram (see Figure 136–7).

NOTE—Exiting TRAINING mode requires both sides to use PAM4 modulation, thus the request and the status of the modulation and precoding are both required to have values other than PAM2 (either "PAM4" or "PAM4 with precoding").

136.8.11.1.4 Zero pad

Two "0" symbols are transmitted immediately after the training pattern. This zero pad ensures the training frame is DC balanced and helps to delineate the start of the frame marker for the next training frame.

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136.8.11.2 Control field structure

The structure of the control field shall be as shown in Table 136–9.

Table 136–9—Control field structure

Bit(s)	Name	Description
15:14	Reserved	Transmit as 0, ignore on receipt
13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control
11:10	Reserved	Transmit as 0, ignore on receipt
9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2
7:5	Reserved	Transmit as 0, ignore on receipt
4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$
1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold

136.8.11.2.1 Initial condition request

The initial condition request bits are used to select one of the three pre-defined transmitter equalizer configurations (presets) specified in 136.8.11.3.4. When the initial condition request bits are 00, the coefficient select and coefficient request bits are used to update the transmitter equalizer configuration.

136.8.11.2.2 Modulation and precoding request

The modulation and precoding request bits are used to request that the link partner transmitter transmit one of the three training pattern formats defined in 136.8.11.1.3.

136.8.11.2.3 Coefficient select

The coefficient select bits are used to identify the coefficient that is the target of a coefficient request. The value of the field is the two's complement encoding of the coefficient index. For example, binary value 111 corresponds to a coefficient index of –1.

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136.8.11.2.4 Coefficient request

The coefficient request bits are used to change the value of the coefficient specified by the coefficient select bits. A coefficient may be changed by incrementing or decrementing its value or by setting it to "No equalization". The "No equalization" value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.

136.8.11.3 Status field structure

The structure of the status field is shown in Table 136–10.

Table 136–10—Status field structure

Bit(s)	Name	Description
15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue
14:12	Reserved	Transmit as 0, ignore on receipt
11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2
9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified
8	Initial condition status	1 = Updated 0 = Not updated
7	Parity	Even parity bit
6	Reserved	Transmit as 0, ignore on receipt
5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$
2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated

136.8.11.3.1 Receiver ready

The receiver ready bit is used to signal the local receiver state to the link partner. When this bit is 1, it indicates that the local receiver has completed training and is prepared to receive data. When this bit is 0, it indicates that the local receiver is requesting that training continue.

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136.8.11.3.2 Modulation and precoding status

The modulation and precoding status bits acknowledge the modulation and precoding request bits received from the link partner. When a change in the received modulation and precoding request bits are detected, the format of the training pattern is changed accordingly (see 136.8.11.1.3). The modulation and precoding status bits are then updated to confirm that the change to the format of the training pattern was completed.

136.8.11.3.3 Receiver frame lock

When the receiver frame lock bit is set to 1, the receiver is indicating that it has identified training frame marker positions and is in a state where the response time requirements specified in 136.8.11.6 are met.

Receiver frame lock shall be set to 0 upon entering TRAINING mode and shall not be set to 1 until local_tf_lock is true.

136.8.11.3.4 Initial condition status

The initial condition status bit acknowledges the initial condition request bits received from the link partner. The acknowledgment reflects the value of ic_sts resulting from the procedure described in 136.8.11.4.

136.8.11.3.5 Parity bit

The parity bit is calculated based on the other bits in the control field and status field to create even parity for these fields. Even parity ensures that the resulting pattern is DC balanced. This field may be ignored on receipt.

136.8.11.3.6 Coefficient select echo

The coefficient select echo bits acknowledge the coefficient select bits received from the link partner. When a change to the coefficient select bits is detected, the coefficient select echo bits are updated to represent the same coefficient index. This serves as a confirmation to the link partner that subsequent coefficient requests will act on the targeted coefficient.

136.8.11.3.7 Coefficient status

The coefficient status bits acknowledge the coefficient request bits received from the link partner. The acknowledge reflects the value of coef_sts resulting from the procedure described in 136.8.11.5.

136.8.11.4 Initial condition setting

When a change to the initial condition request bits is detected, the coefficients are configured in a manner consistent with the following algorithm.

```
if ic_req = ind_ctl
   ic_sts = not_upd
else
   if ic_req = preset 1
      Set coefficients to preset 1
   else if ic_req = preset 2
      Set coefficients to preset 2
   else if ic_req = preset 3
      Set coefficients to preset 3
   end if
   ic_sts = updated
end if
```

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The variables ic_req and ic_sts are defined in 136.8.11.7.1. The transmitter equalizer coefficients corresponding to each of the three presets shall be within the ranges specified in Table 136–12.

The transmitter equalizer is set to preset 1 upon entry to the INITIALIZE state of the PMD control state diagram.

136.8.11.5 Coefficient update

When a change to the coefficient select or coefficient request bits is detected, the corresponding coefficient update is performed in a manner consistent with the following algorithm.

```
if k in k_list

   if coef_req = INCREMENT
      ck_ask = c(k) + ck_stp
   else if coef_req = DECREMENT
      ck_ask = c(k) - ck_stp
   else if coef_req = NO_EQUALIZATION
      if k = 0
         ck_ask = 1
      else
         ck_ask = 0
      end if
   else
      ck_ask = c(k)
   end if

   if ck_ask > ck_max
      c(k) = ck_max
      if CHECK_EQ(ck_ask,k)
         coef_sts = COEFFICIENT AT LIMIT AND EQUALIZATION LIMIT
      else
         coef_sts = COEFFICIENT AT LIMIT
      end if
   else if ck_ask < ck_min
      c(k) = ck_min
      if CHECK_EQ(ck_ask,k)
         coef_sts = COEFFICIENT AT LIMIT AND EQUALIZATION LIMIT
      else
         coef_sts = COEFFICENT AT LIMIT
      end if
   else if CHECK_EQ(ck_ask,k)
      coef_sts = EQUALIZATION LIMIT
   else
      c(k) = ck_ask
      coef_sts = UPDATED
   end if
else
   coef_sts = COEFFICIENT NOT SUPPORTED
end if
```

The variables coef_req, coef_sts, and k are defined in 136.8.11.7.1. The following additional variables and functions are used.

c(k)
: Variable that contains the current value of the coefficient *c*(k).

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ck_ask
: Variable that contains the value of $c(k)$ that would result from the requested update.

ck_min
: Variable that contains the minimum supported value of $c(k)$.

ck_max
: Variable that contains the maximum supported value of $c(k)$.

ck_stp
: Variable that contains the magnitude of the change in $c(k)$ for one step up or one step down from its current value.

k_list
: The set of valid transmitter equalizer coefficient indices {–2, –1, 0, 1}.

CHECK_EQ(ck_ask,k)
: Compares the transmitter's steady-state voltage that would result from setting transmit equalization coefficient $c(k)$ value to ck_ask, while keeping all other coefficients unchanged, against the transmitter's steady-state voltage (see 136.9.3.1.2) and equalization capability. Returns true if the resulting combination of coefficients would exceed the maximum steady-state voltage or the transmitter's equalization capability. Otherwise returns false.

136.8.11.6 Handshake timing

Changes to the configuration of the transmitter equalizer or the transmitted training pattern may occur at any point between the time the request for the new configuration is received and the time that the request is acknowledged.

The time from the receipt of a new request to the time that request is acknowledged shall be less than 2 ms when the receiver frame lock bit in the status field of transmitted training frames is set to 1. A new request is defined to be a received training frame whose control field differs from the control field of the preceding training frame. An acknowledgment is defined as the first transmitted training frame that contains a status field encoding that is an appropriate response for the requested action. For example, a change in the coefficient select bits in the control field would be acknowledged by a change in the coefficient select echo bits of the status field. Similarly, a change in the modulation and precoding request bits in the control field would be acknowledged by a change in the modulation and precoding status bits in the status field. All timing measurements are referred to a common reference point within the training frame (e.g., the 3 to 0 transition in the training frame marker).

The timing of requests and acknowledgment is illustrated in Figure 136–6.

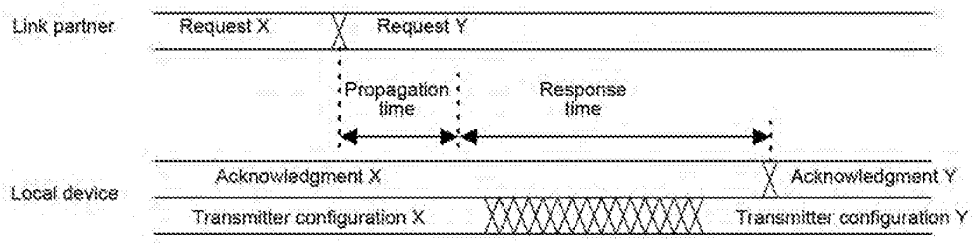


Figure 136–6—Transmitter update timing

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136.8.11.7 Variables, functions, timers, counters, and state diagrams

The PMD implements one instance of each of the PMD control state diagrams, and the set of associated variables, functions, counters and timers defined in this subclause, independently for each of the n physical lanes.

136.8.11.7.1 Variables

coef_req
: Enumerated variable derived from the "coefficient request" bits from the control field of the received training frames (see 136.8.11.2). This variable may be one of the following values: hold, decrement, increment, no equalization.

coef_sel
: Variable derived from the "coefficient select" bits from the control field of the received training frames (see 136.8.11.2). It is assigned a signed integer value that is the two's complement interpretation of the bits.

coef_sts
: Enumerated variable that may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): not updated (not_upd), updated, coefficient at limit, coefficient not supported. This value is assigned by the UPDATE_Cn function and encoded in the status field of transmitted training frames via the ENCODE_STS function.

ic_req
: Enumerated variable derived from the "initial condition request" bits from the control field of the received training frames (see 136.8.11.2). This variable may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): individual control (ind_ctl), preset 1, preset 2, preset 3.

ic_sts
: Enumerated variable that may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): not updated (not_upd), updated.

k
: Variable that stores the most recent value of coef_sel.

local_rx_ready
: Boolean variable that is set to true by the training state diagram when local_trained is asserted and is set to false otherwise. This value is encoded as the "receiver ready" bit in the status field of transmitted training frames.

local_tf_lock
: Boolean variable that is true if the value of training is true and training frame marker positions have been identified and is false otherwise.

local_trained
: Boolean variable that is set to true when the local receiver has determined that the remote transmit and local receive equalizers have been optimized and normal data transmission may commence. It is set to false otherwise. The exact criteria for setting this variable to true are implementation specific.

marker_valid
: Boolean variable that is set to true when the candidate frame marker matches the frame marker pattern defined in 136.8.11.1.1 and is set to false otherwise.

mr_restart_training
: Boolean variable used by system management to restart the start-up protocol. When set to true, it forces the PMD control state diagram to the INITIALIZE state.

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mr_training_enable
: Boolean variable used by system management to enable or disable the start-up protocol. When set to true it enables the start-up protocol, and when set to false it disables the start-up protocol.

new_marker
: Boolean variable that is set to true when a new candidate frame marker is available for testing and is set to false when the TEST_MARKER state is entered. A new frame marker is available for testing when the training frame lock process has accumulated 32 consecutive symbols starting at the candidate frame start position.

remote_rx_ready
: Boolean variable derived from the "receiver ready" bit of the status field of received training frames. If the bit is 1, the value of remote_rx_ready is true, otherwise it is false.

remote_tf_lock
: Boolean variable derived from the "receiver frame lock" bit of the status field of received training frames. If the bit is 1, the value of remote_tf_lock is true, otherwise it is false.

reset
: Boolean variable that resets the PMD. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PMD into low-power mode. It is false otherwise.

signal_detect
: Boolean variable that is set to true when the training process is complete and is set to false otherwise. The value of signal_detect is used by the PMD lane-by-lane signal detect function (136.8.5).

slip_done
: Boolean variable that is set to TRUE when the SLIP requested by the Training frame lock state diagram (Figure 136–8) is completed indicating that the next candidate frame sync position can be tested.

tf_offset
: Boolean variable that is set to true when receiving one full training frame (16 672 symbols, see 136.8.11.1) following the recent frame start position, such that a new frame marker is expected. Otherwise it is set to false

tp_mode
: Enumerated variable that corresponds to the "modulation and precoding status" bits in the status field of received training frames. It may be assigned one of the following values: pam2, pam4, pam4 with precoding.

training
: Boolean variable that is set to true when the start-up protocol is in progress and is set to false otherwise.

training_failure
: Boolean variable that is set to true when training failed to complete successfully within the allotted time limit. Otherwise it is set to false.

136.8.11.7.2 Functions

ENCODE_STS
: Encodes portions of the status field of transmitted training frames. local_tf_lock is mapped to the receiver frame lock bit, k is mapped to the coefficient select echo bits, coef_sts is mapped to the coefficient status bits, ic_sts is mapped to the initial condition status bit, local_rx_ready is mapped to the receiver ready bit, and tp_mode is mapped to modulation and precoding bits (see 136.8.11.3.2).

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SLIP

Causes the next candidate frame marker position to be tested. Repeated invocations of SLIP cause all possible positions to be evaluated. The precise method for determining the next candidate frame marker position is implementation dependent and beyond the scope of this standard.

TRANSMIT(tx_mode)

Controls the output of the PMD transmit function on the current lane. When tx_mode = DATA, the PMD transmit function output is the parameter of the PMD:IS_UNITDATA_*i*.request primitive (see 136.3). When tx_mode = TRAINING, the PMD transmit function output is the stream of symbols generated by the PMD control function.

UPDATE_Cn

Updates the value of *c*(k) based on the current values of the variables k and coef_req. The result of the update is stored in the variable coef_sts. This function implements the algorithm specified in 136.8.11.5.

UPDATE_IC

Updates all transmit equalizer coefficients based on the current value of the variable ic_req. The result is stored in the variable ic_sts. This function implements the algorithm specified in 136.8.11.3.4.

136.8.11.7.3 Timers

holdoff_timer

This timer is started when the PMD control state diagram enters the TIMEOUT state. The terminal count of holdoff_timer is 80 ms ± 2%.

max_wait_timer

This timer sets the limit for how long the PMD start-up protocol is allowed to operate. It is started upon entry to the INITIALIZE state of the PMD control state diagram. If the timer expires before the LINK_READY state is reached, then a failure to train is indicated. The terminal count of max_wait_timer is 1.5 s ± 2%.

wait_timer

This timer is started when the local receiver has completed training and detects that the remote receiver is ready to receive data. The local transmitter sends additional training frames until the timer expires to ensure that the link partner correctly detects the local receiver state. The terminal count of wait_timer is between 25 µs and 125 µs, equivalent to approximately 40 to 200 training frames.

136.8.11.7.4 Counters

bad_markers

Count of the number of consecutive frame marker mismatches.

good_markers

Count of the number of consecutive frame marker matches.

136.8.11.7.5 State diagrams

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter indicates that its value is to be incremented.

The PMD control state diagram (Figure 136–7) defines the operation of the start-up protocol.

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If the LINK_READY state is entered while the modulation and precoding status bits indicate "PAM4 with precoding", then the PMD shall cause the adjacent PMA to transmit all subsequent data on the corresponding lane with precoding (see 135.5.7.2 and 120.5.7.2).

If the LINK_READY state is entered while the modulation and precoding request bits are set to "PAM4 with precoding", then the PMD shall inform the adjacent PMA that all subsequently received data on the corresponding lane includes precoding (see 135.5.7.2 and 120.5.7.2).

The PMD control state diagram is supported by the training frame lock and coefficient update state diagrams. The training frame lock state diagram (Figure 136–8) determines when the PMD control function has detected training frame boundaries. The coefficient update state diagram (Figure 136–9) defines the process for updating the local transmitter equalizer coefficients in response to requests from the link partner.

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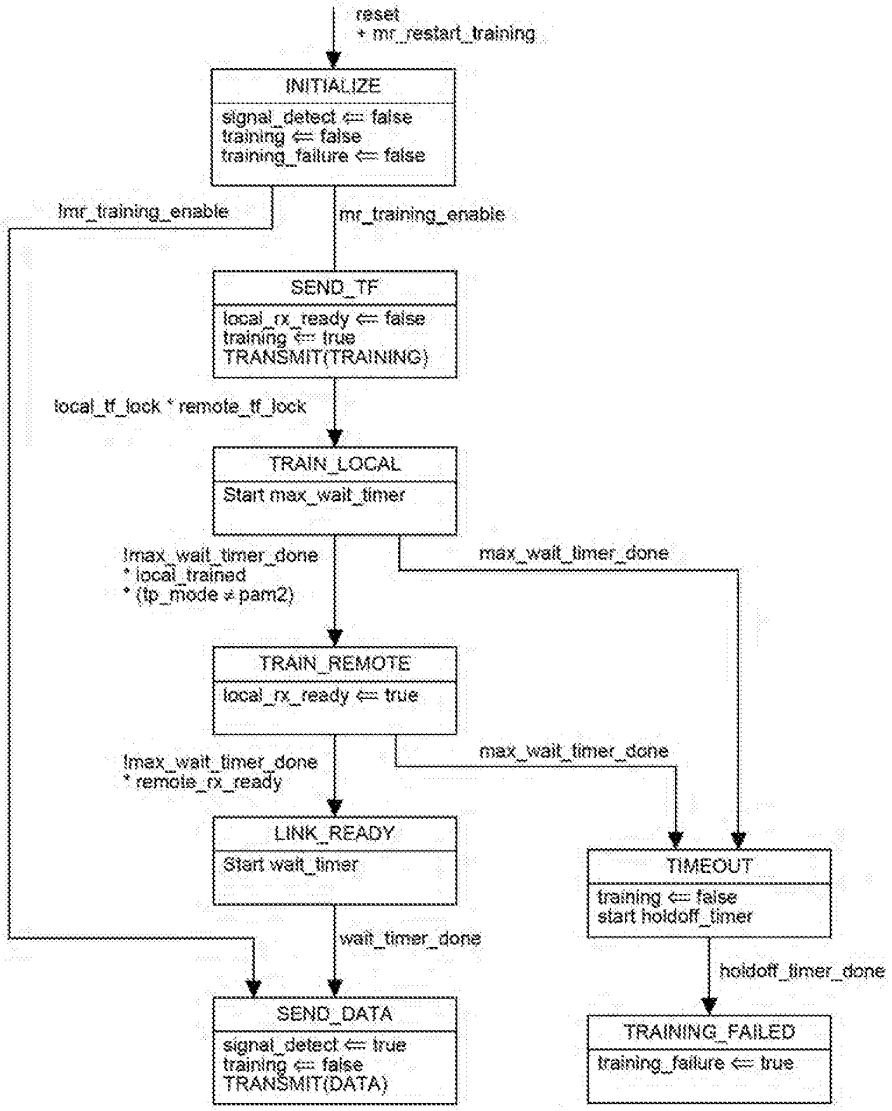


Figure 136–7—PMD control state diagram

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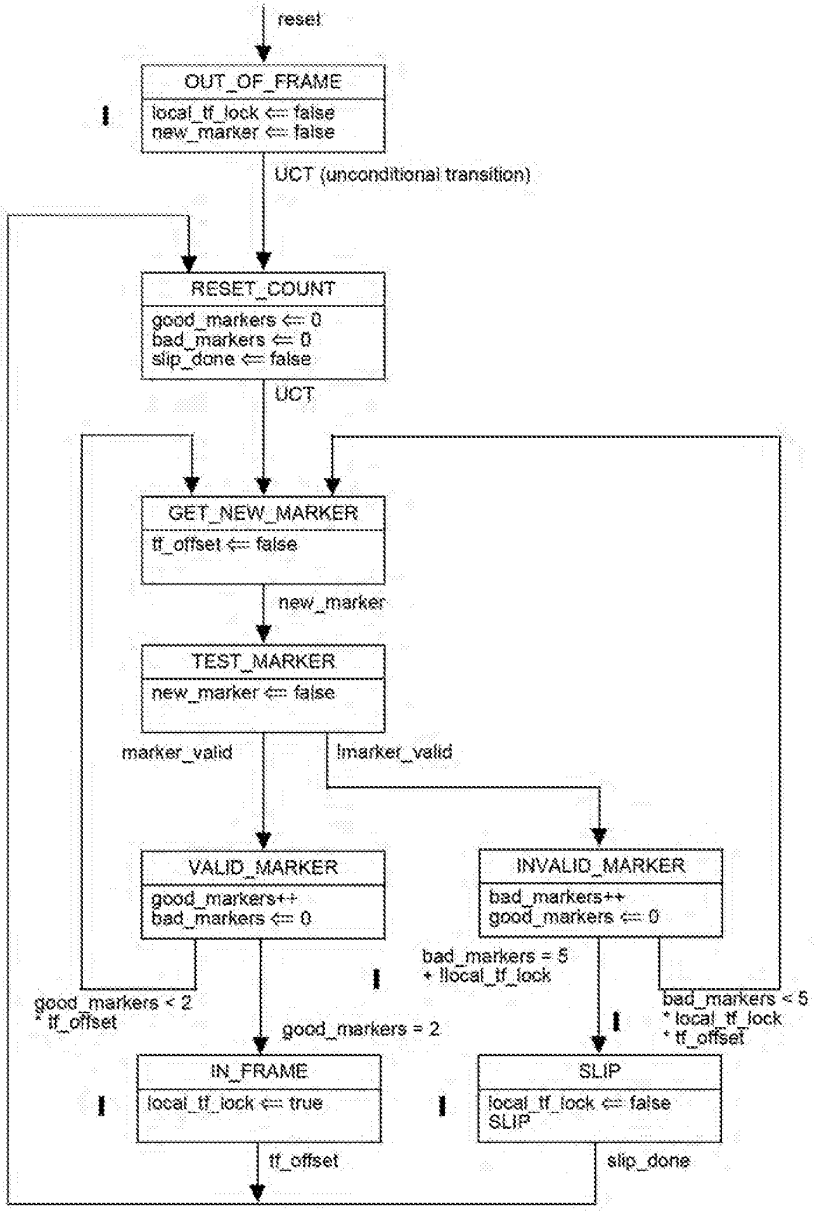


Figure 136–8—Training frame lock state diagram

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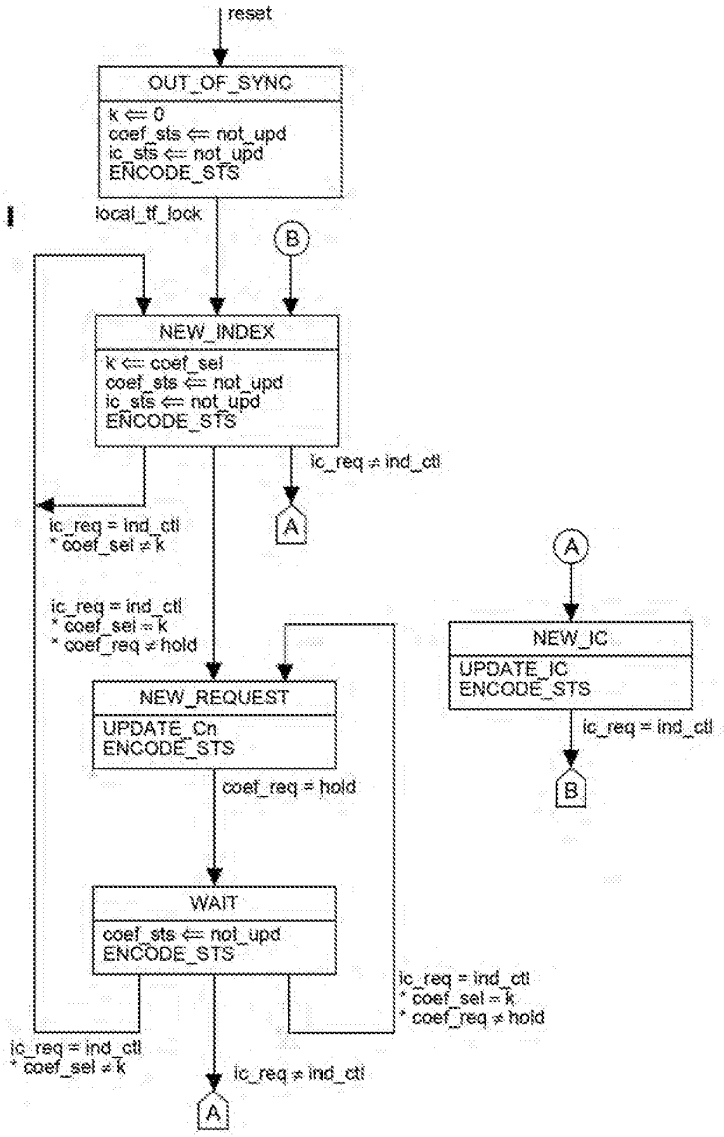


Figure 136–9—Coefficient update state diagram

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136.9 Electrical characteristics

136.9.1 AC-coupling

The MDI (see 136.12) is a low-swing AC-coupled differential interface. AC-coupling within the plug connectors, as defined in 136.12, allows for interoperability between components operating from different supply voltages.

136.9.2 Signal paths

The MDI transmit and receive paths are point-to-point connections. Each path corresponds to one MDI lane and comprises two complementary signals, which form a balanced differential pair.

For 50GBASE-CR, there is one differential path in each direction for a total of two pairs, or four connections. For 100GBASE-CR2, there are two differential paths in each direction for a total of four pairs, or eight connections. For 200GBASE-CR4, there are four differential paths in each direction for a total of eight pairs, or sixteen connections.

136.9.3 Transmitter characteristics

The transmitter on each lane shall meet the specifications given in Table 136–11 and detailed in the referenced subclauses. Unless specified otherwise, all transmitter measurements are made for each lane separately, at TP2, utilizing the test fixtures specified in 136B.1.1, using a test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth.

The transmitter characteristics at TP0 are provided informatively in 136A.2.

Table 136–11—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Differential pk-pk output voltage (max.) with Tx disabled[a]	94.3.12.3	30	mV
DC common-mode voltage (max.)[a]	94.3.12.3	1.9	V
AC common-mode RMS output voltage, v_{ccrms} (max.)[a]	94.3.12.3	30	mV
Differential pk-pk voltage, v_{df} (max.)[a]	94.3.12.3	1 200	mV
Differential output return loss (min.)	92.8.3.2	See Equation (92–1)	dB
Common-mode to differential mode output return loss (min.)	92.8.3.3	See Equation (92–2)	dB
Common-mode to common-mode output return loss (min.)	92.8.3.4	See Equation (92–3)	dB
Transmitter steady-state voltage, v_f (min.) Transmitter steady-state voltage, v_f (max.)	136.9.3.1.2	0.34 0.6	V
Linear fit pulse peak (min.)	136.9.3.1.2	$0.49 \times v_f$	V
Level separation mismatch ratio R_{LM} (min.)	120D.3.1.2.1	330	—

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Table 136–11—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Transmitter output waveform			
abs step size for $c(-1)$, $c(0)$, and $c(1)$ (min.)	136.9.3.1.4	0.005	—
abs step size for $c(-1)$, $c(0)$, and $c(1)$ (max.)	136.9.3.1.4	0.05	—
abs step size for $c(-2)$ (min.)	136.9.3.1.4	0.005	—
abs step size for $c(-2)$ (max.)	136.9.3.1.4	0.025	—
value at minimum state for $c(-1)$ and $c(1)$ (max.)	136.9.3.1.5	−0.25	—
value at maximum state for $c(-2)$ (min.)	136.9.3.1.5	0.1	—
Signal-to-noise-and-distortion ratio (min.)	TBD	TBD	dB
SNR_{FEC} (min.)	120D.3.1.7	30	dB
Output jitter (max.)	120D.3.1.1		
Even-odd jitter, pk-pk		0.019	UI
J_{RMS}		TBD	UI
J4		TBD	UI
Signaling rate		26.5625 ± 100 ppm	GBd
Unit interval nominal		37.64706	ps

[a]Measurement uses the method described in 94.3.12.3 with the exception that the PRBS13Q test pattern is used.

136.9.3.1 Transmitter output waveform

The transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer on each lane is the four-tap transversal filter shown in Figure 136–10.

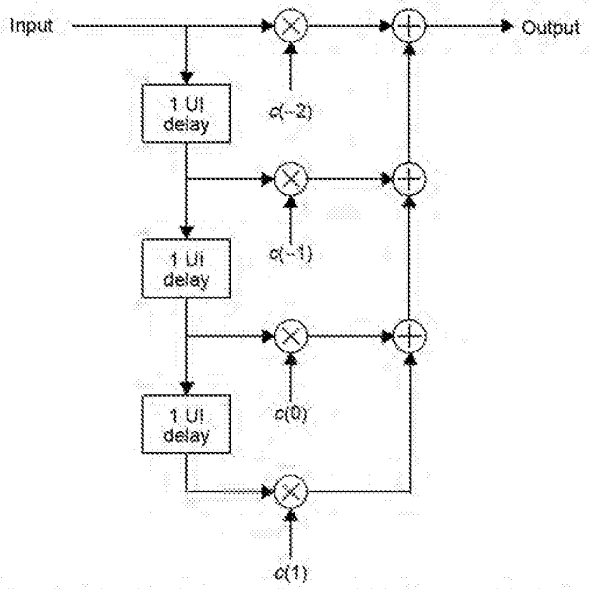


Figure 136–10—Transmit equalizer functional model

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The state of the transmit equalizer and hence the transmitted output waveform may be manipulated via the PMD control function defined in 136.8.11 or via the management interface. The transmit function responds to a set of commands issued by the link partner's receive function and conveyed by a back-channel communications path. This command set includes instructions to increment, decrement, hold, or set to zero a selected coefficient $c(k)$, where $k = -2$ to 1. In addition, it includes commands to set all coefficients to one of three initial conditions.

In response, the transmit function relays status information to the link partner's receive function. The status messages indicate the selected coefficient index k, the status of the coefficient $c(k)$ (updated, not updated, or at limit), and the status of the initial condition (updated or not updated).

136.9.3.1.1 Linear fit to the measured waveform

The following procedure is used to determine the linear fit pulse response, linear fit error, and normalized transmitter coefficient values.

Set the transmitter under test to transmit the PRBS13Q test pattern (defined in 120.5.11.2.1). For each configuration of the transmit equalizer, capture at least one complete cycle of the test pattern at TP2, as specified in 85.8.3.3.4. The clock recovery unit (CRU) used in the measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade.

In the following calculations, M should be an integer not less than 32. Interpolation of the captured waveform may be used to achieve this.

Compute the linear fit pulse response $p(k)$, k=1 to $M \times N_p$, from the captured waveform, as specified in 85.8.3.3.5, with $N_p = 200$ and $D_p = 3$, where the aligned symbols $x(n)$ are assigned normalized amplitudes −1, $-ES$, ES, and 1 to represent the PAM4 symbol values 0, 1, 2, and 3 respectively. ES is defined as $(|ES1| + |ES2|)/2$ where $ES1$ and $ES2$ are calculated according to 120D.3.1.2.

Define $r(k)$ to be the linear fit pulse response when transmit equalizer coefficients have been set to the "preset 1" values. The normalized coefficients for any configuration of the transmit equalizer are computed using the following method.

For each value of m in the range $-M/2$ to $M/2-1$ when M is even and $-(M-1)/2$ to $(M-1)/2$ when M is odd:

a) Define an $M \times N_p$-by-4 matrix R_m. The elements of R_m are assigned values per Equation (136–1) where $i = -2$ to 1 and $j = 1$ to $M \times N_p$.

$$R_m(j, i+3) = \begin{cases} r(m) + j - M \times i & \text{if } 1 \le m + j - M \times i \le M \times N_p \\ 0 & \text{otherwise} \end{cases} \quad (136\text{–}1)$$

b) The normalized coefficients of the transmit equalizer are computed using Equation (136–2).

$$\begin{bmatrix} c_m(-2) \\ c_m(-1) \\ c_m(0) \\ c_m(1) \end{bmatrix} = (R_m^T R_m)^{-1} R_m^T \begin{bmatrix} p(1) \\ \cdots \\ p(M \times N_p) \end{bmatrix} \quad (136\text{–}2)$$

c) The linear fit pulse response is reconstructed from the matrix R_m and the normalized coefficients using Equation (136–3).

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$$\begin{bmatrix} p_m(1) \\ \cdots \\ p_m(M \times N_p) \end{bmatrix} = R_m \begin{bmatrix} c_m(-2) \\ c_m(-1) \\ c_m(0) \\ c_m(1) \end{bmatrix} \quad (136\text{–}3)$$

d) $\varepsilon^2(m)$ is computed using Equation (136–4).

$$\varepsilon^2(m) = \sum_{k=1}^{M \times N_p} (p(k) - p_m(k))^2 \quad (136\text{–}4)$$

The normalized transmit equalizer coefficients $c(i)$ for a given linear fit pulse $p(k)$ are the values $c_m(i)$ for the value of m that minimizes $\varepsilon^2(m)$.

136.9.3.1.2 Steady-state voltage and linear fit pulse peak

The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(k)$ divided by M (refer to 85.8.3.3 step 3). The steady-state voltage shall be greater than or equal to 0.34 V and less than or equal to 0.6 V after the transmit equalizer initial condition has been set to preset 1 (no equalization).

The peak value of $p(k)$ shall be greater than $0.49 \times v_f$ after the transmit equalizer initial condition has been set to preset 1 (no equalization).

Editor's note: the baseline proposal is based on clause 92, which specifies the peak-to-v_f ratio minimum as 0.45. This specification was changed to 0.49 in clause 110 due to consideration of transition time in 802.3by. The editor considers the latter value to be more adequate here.

136.9.3.1.3 Coefficient initialization

When the Coefficient update state diagram (Figure 136–9) is in either the OUT_OF_SYNC state or the NEW_IC state, the coefficients of the transmit equalizer shall be configured to values within the ranges specified in Table 136–12 (according to the value of the variable ic_req). These requirements apply upon the assertion of Initial condition status of "Updated".

Table 136–12—Coefficient initial conditions

Coefficient update state	ic_req	c(−2)	c(−1)	c(0)	c(1)
OUT_OF_SYNC	N/A	0 ± 0.025	0 ± 0.05	1 ± 0.05	0 ± 0.05
NEW_IC	preset 1	0 ± 0.025	0 ± 0.05	1 ± 0.05	0 ± 0.05
	preset 2	0 ± 0.025	0 ± 0.05	0.75 ± 0.05	−0.25 ± 0.05
	preset 3	0 ± 0.025	−0.25 ± 0.05	0.75 ± 0.05	0 ± 0.05

136.9.3.1.4 Coefficient step size

When coef_sel is −1, 0, or 1, the change in the normalized transmit equalizer coefficient c(coef_sel) corresponding to a request to "increment" shall be between 0.005 and 0.05, and the change in the normalized

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transmit equalizer coefficient c(coef_sel) corresponding to a request to "decrement" shall be between –0.05 and –0.005.

When coef_sel is –2, the change in the normalized transmit equalizer coefficient $c(-2)$ corresponding to a request to "increment" shall be between 0.005 and 0.025, and the change in the normalized transmit equalizer coefficient c(coef_sel) corresponding to a request to "decrement" shall be between –0.025 and –0.005.

The change in the normalized transmit equalizer coefficient is defined to be the difference in the value measured prior to the assertion of the "increment" or "decrement" request (i.e., coef_req is "Hold") and the value upon the assertion of a coefficient status of "updated".

136.9.3.1.5 Coefficient range

When sufficient "increment" or "decrement" requests have been received for a given coefficient, the coefficient reaches a lower or upper bound based on the range of that coefficient or the combination of coefficients.

With $c(-2)$ and $c(-1)$ both set to zero and both $c(0)$ and $c(1)$ having received sufficient "decrement" requests so that they are at their respective minimum values, $c(1)$ shall be less than or equal to –0.25.

With $c(-2)$ and $c(1)$ set to zero and both $c(-1)$ and $c(0)$ having received sufficient "decrement" requests so that they are at their respective minimum values, $c(-1)$ shall be less than or equal to –0.25.

With $c(-1)$ and $c(1)$ set to zero, $c(0)$ having received sufficient "decrement" requests so that it is at its minimum value, and $c(-2)$ having received sufficient "increment" requests so that it is at its maximum value, $c(-2)$ shall be greater than or equal to 0.1.

NOTE—a coefficient may be set to zero by asserting a coefficient request of "no equalization" for that coefficient, using the control function specified in 136.8.11, or by implementation specific means.

136.9.4 Receiver characteristics

Receiver electrical characteristics are specified at TP3. The receiver shall meet the return loss requirements specified in 92.8.4.2 and 92.8.4.3. In addition, the requirements in 136.9.4.1, 136.9.4.2, 136.9.4.3 and 136.9.4.4 apply.

The receiver specifications at TP5 are provided informatively in 136A.3.

136.9.4.1 Receiver input amplitude tolerance

When a PMD receiver is connected to a compliant transmitter whose peak-to-peak differential output voltage (see Table 136–11 footnote a) measured at the preset 1 equalizer setting is 1 200 mV, using a compliant cable assembly with the minimum insertion loss specified in 136.11.2, the PMD receiver shall operate at a BER better than 10^{-4}.

Editor's note (to be removed after draft 1.2): The response to comment #146 against draft 1.1 was to replace the reference for peak-to-peak differential output voltage from 92.8.3.1 to 136.9.3. Since 136.9.3 is a general transmitter characteristics subclause, the editor judged that the specific reference to Table 136–11 footnote a would be preferable in this case, and hence the implementation differs from the resolved comment.

The receiver is allowed to control the transmitter equalizer coefficients, using the PMD control function defined in 136.8.11 or an equivalent process, to meet these requirements.

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136.9.4.2 Receiver interference tolerance

Receiver interference tolerance is measured according to the procedure described in 136.9.4.2.1 through 136.9.4.2.5. Receiver interference tolerance test requirements are specified in Table 136–13.

Two tests are defined. Test 1 includes a low-loss channel. Test 2 includes a high-loss channel. The cable assembly used in the test channel (see 110.8.4.2.2) shall meet the cable assembly Channel Operating Margin (COM) as specified in 136.11.7.

Table 136–13—Interference tolerance test parameters

Parameter	Test 1 (low loss)		Test 2 (high loss)		Units
	Min	Max	Min	Max	
Test pattern	Scrambled idle encoded by RS-FEC				
FEC symbol error ratio required[a]	$< 10^{-5}$				
Test channel insertion loss at 13.28 GHz[b]	14.3	14.8	23.21	23.74	dB
Cable assembly insertion loss at 13.28 GHz	8	10	14.06	16.06	dB
COM		3		3	dB
$h_{max}(1)$ used in COM calculation	0.7				
DER_0 used in COM calculation	10^{-4}				

[a]See 136.9.4.2.5 for definition of FEC symbol error ratio.
[b]Insertion loss between the two test references (see Figure 110–3b).

136.9.4.2.1 Test setup

The interference tolerance test is performed with the setup similar to the one described in 110.8.4.2.1. The test setup includes noise injection for all lanes of the pattern generator.

136.9.4.2.2 Test channel

The test channel is the same as the one defined in 110.8.4.2.2, except that the cable assembly meets the requirements of 136.11 and the cable assembly test fixture meets the requirements of 136B.1.1.

136.9.4.2.3 Test channel calibration

The scattering parameters of the test channel are measured at the test references as illustrated in Figure 110–3b using the cable assembly test fixtures specified in 136B.1.1.

The insertion loss at 13.28 GHz of the signal path between the test references in Figure 110–3b is within the limits in Table 136–13.

The COM is calculated using the method and parameters of 136.11.7 with the following considerations:

a) The channel signal path is $SCHS_p$ = cascade($S^{(CTSP)}$, $S^{(HOSP)}$), where cascade() is defined in 93A.1.2.1, $S^{(HOSP)}$ is defined in 136.11.7.1.1, and $S^{(CTSP)}$ is the measured channel between the test references in Figure 110–3b.

b) The COM parameters are as modified by Table 136–13.

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c) COM is calculated using both Test 1 and Test 2 device package model transmission line lengths listed in Table 136–15 on the receiver side. The value of COM is taken as the lower of the two calculated values.

d) The augmented signal path in 93A.1.2 is replaced by S_p determined from Equation (136–7) (effectively omitting the transmitter device package model $S^{(tp)}$). The filtered voltage transfer function $H^{(k)}(f)$ calculated in Equation (93A–19) uses the filter $H_r(f)$ defined by Equation (93A–46), where β is 2 and T_r is the 20% to 80% transition time at the Tx test reference. T_r is measured using the method in 86A.5.3.3, with the exception that the observation filter bandwidth is 33 GHz instead of 12 GHz. T_r is measured with the transmit equalizer turned off (i.e., coefficients set to the preset 1 values, see 136.9.3.1.3).

e) Even-odd jitter, J4, and J_{RMS} without noise injection (see 136.9.4.2.4) are measured at the Tx test reference and comply with the specification in Table 136–11. In the calculation of COM, A_{DD} and σ_{RJ} are calculated from the measured values of J4 and J_{RMS} using Equation (136–5) and Equation (136–6), replacing the values in Table 136–15. It is recommended to adjust the pattern generator jitter such that J4 and J_{RMS} are as close as practical to their limits in Table 136–11.

f) The SNR_{TX} value that results in the required COM value for the test is calculated. The injected noise (see 136.9.4.2.4) is set such that the SNDR matches the calculated SNR_{TX} value. SNDR is measured at the Tx test reference using the procedure in 120D.3.1.6, with the following exceptions:

1) TBD

$$A_{DD} = \frac{\frac{J4}{2} + Q4\sqrt{(Q4^2+1)\times J_{RMS}^2 - \left(\frac{J4}{2}\right)^2}}{Q4^2+1} \quad (136\text{–}5)$$

$$\sigma_{RJ} = \frac{\frac{J4}{2} - A_{DD}}{Q4} \quad (136\text{–}6)$$

where $Q4 = 3.8906$

NOTE—Q4 is an approximated solution of $Q(Q4) = 5\times10^{-5}$, where the Q function is defined in Equation (95–1).

$$S_p = \text{cascade}(SCHS_p, S^{(tp)}) \quad (136\text{–}7)$$

where

cascade()	is defined in 93A.1.2.1
$SCHS_p$	is defined in item a above
$S^{(tp)}$	is defined in 93A.1.2.4

136.9.4.2.4 Pattern generator and noise injection

The pattern generator transmits data to all lanes of the device under test. At the start of transmitter training, the pattern generator output amplitude on all lanes shall be 800 mV peak-to-peak differential when measured on an alternating zero-three pattern. The output amplitude, measured on an alternating zero-three pattern, is not permitted to exceed 800 mV peak-to-peak differential during transmitter training. The output waveform of the pattern generator shall comply with 136.9.3.

Broadband noise is added to the signal before the Tx test reference, with noise level set according to step f in 136.9.4.2.3.

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The broadband noise required for each lane is calibrated. The noise may be added either to one lane at a time or using multiple noise sources to all lanes at the same time.

136.9.4.2.5 Test procedure

The pattern generator is first configured to transmit the training pattern defined in 136.8.11. During this initialization period, the device under test (DUT) configures the pattern generator transmit equalizer to the coefficient settings it would select using the protocol described in 136.8.11 and the receiver is tuned using its optimization method. The coefficient settings may be communicated via the start-up protocol or by other means.

After the pattern generator equalizer has been configured and the receiver tuned, the pattern generator is set to generate the test pattern specified in Table 136–13. During the test, the transmitters in the device under test transmit the same pattern type specified for the test, with equalization turned off (preset 1 condition).

Symbol error ratio is measured using the per-lane RS-FEC symbol error counters (see 91.6) in the adjacent RS-FEC sublayer, or the per-lane PCS symbol error counters (see 119.3.1) in the adjacent PCS, as appropriate.

The FEC symbol error ratio is defined as the sum of the symbol error counters on all lanes divided by the number of symbols transmitted on all lanes, which may be estimated from the test time.

A PHY shall meet the FEC symbol error ratio requirement in all tests defined in Table 136–13 with broadband noise added to all lanes (see 136.9.4.2.4).

NOTE—If noise is applied to each of the n lanes one at a time, results of the n measurements are summed to yield the FEC symbol error ratio. The result may need to be corrected based on the FEC symbol error ratio with no noise added on any lane.

136.9.4.3 Receiver jitter tolerance

136.9.4.3.1 Test setup

Jitter tolerance is measured with a channel meeting the insertion loss of Test 2 as specified in Table 136–13. The pattern generator includes Sinusoidal jitter injection.

136.9.4.3.2 Test procedure

The jitter tolerance test procedure is similar to that of 136.9.4.2, with the exception that no noise is injected (i.e., step f in 136.9.4.2.3 is not performed). Instead, jitter with the specified frequency and amplitude is applied to the pattern generator and the jitter amplitude is adjusted to obtain the peak-to-peak jitter specified for that frequency in Table 120D–7 at the Tx test reference (see Figure 110–3a).

A PHY shall meet the FEC symbol error ratio requirement defined in Table 136–13 for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 120D–7 with jitter added to all lanes (see 136.9.4.2.4).

NOTE—If jitter is applied to each of the n lanes one at a time, results of the n measurements are summed to yield the FEC symbol error ratio. The result may need to be corrected based on the FEC symbol error ratio with no jitter applied on any lane.

136.9.4.4 Signaling rate range

A PHY shall comply with the receiver requirements of 136.9.4.2 and 136.9.4.3 for any signaling rate in the range 26.5625 GBd ± 100 ppm. The corresponding unit interval is approximately 37.64706 ps.

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136.10 Channel characteristics

The channel is defined between TP0 and TP5 to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly as illustrated in Figure 136–2. The channel insertion loss, return loss, COM, and the transmitter and receiver differential controlled impedance printed circuit board parameters are provided informatively in 136A.1 through 136A.4.

Channel definitions apply for links between two PHYs of the same type, 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4.

136.11 Cable assembly characteristics

Cable assemblies defined in this subclause contain insulated conductors terminated in a connector at each end for use as link segments between MDIs. Cable assemblies are primarily intended as point-to-point links between 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4 PHYs using controlled impedance cables.

Three cable assembly types are specified:

a) 50GBASE-CR: Cable assembly that supports single-lane links between two 50GBASE-CR PHYs with achievable cable length of at least 3 m.

b) 100GBASE-CR2: Cable assembly that supports two-lane links between two 100GBASE-CR2 PHYs with achievable cable length of at least 3 m.

c) 200GBASE-CR4: Cable assembly that supports four-lane links between two 200GBASE-CR4 PHYs with achievable cable length of at least 3 m.

NOTE—It may be possible to construct compliant cable assemblies longer than indicated. Length of a cable assembly does not imply compliance to specifications.

Since 50GBASE-CR has two specified MDI connectors, single-lane (SFP28, specified in 110.11.1) and multi-lane (QSFP28, specified in 92.12), there are three possible combinations of the connectors at each end. The possible 50GBASE-CR cable assembly types are described in Annex 136C. 100GBASE-CR2 uses two lanes of the multi-lane QSFP28 (specified in 92.12). 200GBASE-CR4 uses four lanes of the multi-lane QSFP28 (specified in 92.12).

All cable assembly measurements are to be made between TP1 and TP4 with cable assembly test fixtures as specified in Annex 136B. These cable assembly specifications are based upon twinaxial cable characteristics, but other cable types are acceptable if the specifications of this subclause are met.

Table 136–14 provides a summary of the cable assembly characteristics for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4, and references to the subclauses addressing each parameter.

The specifications for the three cable assembly types are identical except the number of lanes.

136.11.1 Characteristic impedance and reference impedance

The nominal differential characteristic impedance of the cable assembly is 100 Ω. The differential reference impedance for cable assembly specifications shall be 100 Ω.

136.11.2 Cable assembly insertion loss

The measured insertion loss of a cable assembly shall be greater than or equal to the minimum cable assembly insertion loss given in Equation (92–26) and illustrated in Figure 92–12.

The measured insertion loss at 13.28 GHz of a cable assembly shall be less than or equal to 16.06 dB.

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Table 136–14—Cable assembly characteristics summary

Description	Reference	Value	Unit
Maximum insertion loss at 13.28 GHz	136.11.2	16.06	dB
Minimum insertion loss at 13.28 GHz	136.11.2	8	dB
Minimum differential return loss at 13.28 GHz	136.11.3	6 Equation (92–27)	dB
Differential to common-mode return loss	136.11.4	Equation (92–28)	dB
Differential to common-mode conversion loss	136.11.5	Equation (92–29)	dB
Common-mode to common-mode return loss	136.11.6	Equation (92–30)	dB
Minimum COM	136.11.7	3	dB

136.11.3 Cable assembly differential return loss

The cable assembly differential return loss shall meet the requirements of 92.10.3.

136.11.4 Differential to common-mode return loss

The cable assembly differential to common-mode return loss shall meet the requirements of 92.10.4.

136.11.5 Differential to common-mode conversion loss

The cable assembly differential to common-mode conversion loss shall meet the requirements of 92.10.5.

136.11.6 Common-mode to common-mode return loss

The cable assembly common-mode to common-mode return loss shall meet the requirements of 92.10.6.

136.11.7 Cable assembly Channel Operating Margin

The cable assembly Channel Operating Margin (COM) for each lane is derived from measurements of the cable assembly signal, near-end crosstalk and far-end crosstalk paths. COM is computed using the path calculations defined in 136.11.7.1 and the procedure in 93A.1, where T_r is 8 ps and β is 2 for $H_r(f)$ as used in Equation (93A–19). The specific paths used depend on cable assembly form factor (see Annex 136C), as described in 136.11.7.2.

COM parameter values for the three cable assembly types are provided in Table 136–15.

Test 1 and Test 2 differ in the value of the device package model transmission line length z_p. COM for any channel within the cable assembly shall be greater than or equal to 3 dB for both Test 1 and Test 2.

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Table 136–15—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step[a]	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface Package transmission line characteristic impedance	 C_d z_p z_p C_p Z_c	 1.8×10^{-4} 12 30 1.1×10^{-4} 90	 nF mm mm nF Ω
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.25 0 0.05	—
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.1 0.025	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 0 1	 dB dB dB
Continuous time filter, DC gain 2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB
Continuous time filter, zero frequencies	f_z f_{z2}	$f_b / 2.5$ $f_b / 40$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b / 2.5$ $f_b / 40$	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.45 0.45 0.63	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB

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Table 136–15—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	—
Normalized DFE coefficient magnitude limit for $n = 1$ for $n = 2$ to N_b	$b_{max}(n)$	 0.7 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	1.64×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-4}	—

[a]For cable lengths greater than 4 m, a frequency step (Δf) no larger than 5 MHz is recommended.

136.11.7.1 Channel signal and crosstalk path calculations

The channel paths between TP0 and TP5 used for calculation of the cable assembly COM consist of measured cable assembly signal and crosstalk paths, representative transmitter PCB signal paths, and representative receiver PCB signal paths.

The transmitter and receiver PCB signal paths are calculated using the method defined in 93A.1.2.3. The scattering parameters for a PCB are defined by Equation (93A–13), Equation (93A–14), and the parameter values given in Table 92–12. The PCB trace length parameter z_p has different value for each specific signal path, as specified in 136.11.7.1.1 and 136.11.7.1.2.

The channel path calculations use the function cascade() defined in 93A.1.2.1.

136.11.7.1.1 Channel signal path

The scattering parameters of the channel signal path from TP0 to TP5 are calculated using Equation (136–8). The transmitter and receiver PCB signal paths are both denoted as $S^{(HOSP)}$ and are calculated from Equation (93A–13) and Equation (93A–14) using $z_p = 151$ mm in length, representing an insertion loss of 6.42 dB at 13.28 GHz on each PCB.

$$SCHS_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOSP)}, S^{(CASP)}), S^{(HOSP)}) \quad (136\text{–}8)$$

where

$SCHS_p^{(k)}$ is the channel signal path

$S^{(HOSP)}$ is the host (transmitter or receiver) PCB signal path

$S^{(CASP)}$ is the cable assembly signal path (TP1 to TP4)

k is equal to zero

136.11.7.1.2 Channel crosstalk paths

The MDI is the significant contributor to crosstalk and is included in and characterized by the cable assembly crosstalk measurements. Crosstalk includes a near-end path where the aggressor is the PMD

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transmitter, and for specific form factors, near-end and alien far-end crosstalk paths where the aggressors are other PMD transmitters that are connected to the same cable assembly.

For the channel crosstalk paths, the receiver PCB model is $S^{(HOSP)}$ as defined in 136.11.7.1.1. The aggressor transmitter host PCB model is denoted as $S^{(HOTxSP)}$ and is calculated from Equation (93A–13) and Equation (93A–14) using z_p = 72 mm in length, representing an insertion loss of 3.1 dB at 13.28 GHz. The transmitter host PCB insertion loss is lower than that used for the signal path, to allow for a reasonable worst-case crosstalk in the COM calculation.

The scattering parameters of the channel near-end crosstalk paths are calculated using Equation (136–9). The scattering parameters of the channel alien far-end crosstalk paths are calculated using Equation (136–10).

$$SCHNXT_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOTxSP)}, S^{(CANXTk)}), S^{(HOSP)}) \quad (136\text{–}9)$$

where

$SCHNXT_p^{(k)}$	is the near-end crosstalk path
$S^{(HOSP)}$	is the host receiver PCB signal path defined in 136.11.7.1.1
$S^{(HOTxSP)}$	is the aggressor transmitter PCB signal path
$S^{(CANXTk)}$	is the cable assembly near-end crosstalk path k (TP1 to TP4)
k	is the index of the near-end crosstalk path

$$SCHAFXT_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOTxSP)}, S^{(CAFXTk)}), S^{(HOSP)}) \quad (136\text{–}10)$$

where

$SCHAFXT_p^{(k)}$	is the alien far-end crosstalk path
$S^{(HOSP)}$	is the host receiver PCB signal path defined in 136.11.7.1.1
$S^{(HOTxSP)}$	is the aggressor transmitter PCB signal path
$S^{(CAFXTk)}$	is the cable assembly far-end crosstalk path k (TP1 to TP4)
k	is the index of the alien far-end crosstalk path

136.11.7.2 Signal and crosstalk paths used in calculation of COM

Cable assemblies have several form factors, as described in Annex 136C. The choice of signal and crosstalk paths for calculation of COM is specific to each cable assembly form factor, as specified in 136.11.7.2.1 through 136.11.7.2.4.

136.11.7.2.1 SFP28 to SFP28

The SFP28 to SFP28 channel structure includes the signal path, one near-end crosstalk path and no alien far-end crosstalk. The signal and near-end crosstalk paths are used in calculation of COM.

The signal path is calculated using Equation (136–8).

The near-end crosstalk path is calculated using Equation (136–9).

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136.11.7.2.2 QSFP28 to SFP28

The QSFP28 to SFP28 channel structure includes the signal path, three alien far-end and one near-end crosstalk path. These five paths are used in calculation of COM. Crosstalk from transmitters on other SFP28 connectors is assumed to be insignificant.

The signal path is calculated using Equation (136–8).

The near-end crosstalk path is calculated using Equation (136–9), with k equal to 1.

The three alien far-end crosstalk paths are calculated using Equation (136–10), with k values from 1 to 3.

136.11.7.2.3 SFP28 to QSFP28

The SFP28 to QSFP28 channel structure includes the signal path, three alien far-end and four near-end crosstalk paths. These eight paths are used in calculation of COM.

The signal path is calculated using Equation (136–8).

The near-end crosstalk paths are calculated using Equation (136–9), with k values from 1 to 4.

The three alien far-end crosstalk paths are calculated using Equation (136–10), with k values from 1 to 3.

136.11.7.2.4 QSFP28 to QSFP28

The QSFP28 to QSFP28 channel structure includes the same paths defined for the SFP28 to QSFP28 channel, and COM is calculated in the same way, as defined in 136.11.7.2.3.

136.12 MDI specifications

This subclause defines the 50GBASE-CR, the 100GBASE-CR2, and the 200GBASE-CR4 Media Dependent Interface (MDIs). The MDI couples the PMD (specified in 136.8 and 136.9) to the cable assembly (specified in 136.11).

For 50GBASE-CR, the mechanical interface between the PMD and the cable assembly may be either a mated pair of connectors meeting the requirements of 110.11.1 (single-lane MDI) or a mated pair of connectors meeting the requirements of 92.12.1.1 (multi-lane MDI). The plug connector is used on the cable assembly and the receptacle is used on the PMD. For the multi-lane MDI, each of the paired transmit and receive lanes (SL0, DL0), (SL1, DL1), (SL2, DL2) or (SL3, DL3) may be used for the transmit and receive connections (SL and DL).

For 100GBASE-CR2 or 200GBASE-CR4, the mechanical interface between the PMD and the cable assembly is a mated pair of connectors meeting the requirements of 92.12.1.1 (multi-lane MDI). The plug connector is used on the cable assembly and the receptacle is used on the PMD. For 100GBASE-CR2 multi-lane MDI, the paired transmit and receive lanes for one PHY shall be (SL0, DL0) and (SL1, DL1), and if a second PHY uses the same MDI connector it uses (SL2, DL2) and (SL3, DL3).

For 50GBASE-CR, 100GBASE-CR2 and 200GBASE-CR4 plug connectors, the receive lanes are AC-coupled; the AC-coupling shall be within the plug connectors. It should be noted that there may be various methods for AC-coupling in actual implementations. The low-frequency 3 dB cutoff of the AC-coupling shall be less than 50 kHz. It is recommended that the value of the coupling capacitors be 100 nF. The capacitor limits the inrush charge and baseline wander.

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136.13 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 14.7.

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136.14 Protocol implementation conformance statement (PICS) proforma for Clause 136, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4[9]

136.14.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 136, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

136.14.2 Identification

136.14.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

136.14.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Clause 136, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

[9] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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136.14.3 Major capabilities/options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
*CR	50GBASE-CR PMD	136.1	Can operate as a 50GBASE-CR PMD	O.1	Yes [ ] No [ ]
*CR2	100GBASE-CR2 PMD	136.1	Can operate as a 100GBASE-CR2 PMD	O.1	Yes [ ] No [ ]
*CR4	200GBASE-CR4 PMD	136.1	Can operate as a 200GBASE-CR4 PMD	O.1	Yes [ ] No [ ]
PMA50	50GBASE-R PMA	136.1	Device implements Clause 135 PMA for 50GBASE-R	CR:M	Yes [ ] N/A [ ]
PMA100	100GBASE-P PMA	136.1	Device implements Clause 135 PMA for 100GBASE-P	CR2:M	Yes [ ] N/A [ ]
PMA200	200GBASE-R PMA	136.1	Device implements Clause 120 PMA for 200GBASE-R	CR4:M	Yes [ ] N/A [ ]
*AUIPMD	50GAUI-n C2C, 100GAUI-n C2C, or 200GAUI-n C2C	136.1	Service interface of PMA adjacent to PMD is physically instantiated	O.2	Yes [ ] No [ ]
AUIFEC	LAUI-2 C2C or CAUI-n C2C	136.1	Service interface of PMA between PCS and RS-FEC is physically instantiated	!CR4:O.2	Yes [ ] No [ ] N/A [ ]
*nGMII	50GMII, CGMII or 200GMII and RS	136.1	Interface is implemented or functionally equivalent	O.2	Yes [ ] No [ ]
AN	Auto-negotiation	136.1	Device implements Auto-negotiation	M	Yes [ ]
FEC50	50GBASE-R RS-FEC	136.1	Device implements Clause 134 RS-FEC	CR* !AUIPMD:M	Yes [ ] N/A [ ]
PCS50	50GBASE-R PCS	136.1	Device implements Clause 133 PCS	CR* nGMII:M	Yes [ ] N/A [ ]
FEC100	100GBASE-R RS-FEC	136.1	Device implements Clause 91 RS-FEC with RS(544,514)	CR2* !AUIPMD:M	Yes [ ] N/A [ ]
PCS100	100GBASE-R PCS	136.1	Device implements Clause 82 100GBASE-R PCS	CR2* nGMII:M	Yes [ ] N/A [ ]
PCS200	200GBASE-R PCS	136.1	Device implements Clause 119 200GBASE-R PCS	CR4* nGMII:M	Yes [ ] N/A [ ]
*EEE	EEE fast wake capability	136.1	Capability is supported	nGMII:O	Yes [ ] No [ ] N/A [ ]
PCSAN	PCS requirements for AN service interface	136.4	PCS supports service interface primitive AN_LINK.indication	nGMII:M	Yes [ ] N/A [ ]
DC	Delay constraints	136.5	Conforms to constraints	M	Yes [ ]
SC	Skew and Skew Variation constraints	136.6	Conforms to constraints	M	Yes [ ]

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Item[a]	Feature	Subclause	Value/Comment	Status	Support
*MD	MDIO capability	136.7	Device implements Clause 45 MDIO	O	Yes [ ] No [ ]
*CBL	Cable assembly	136.11	Item marked with CBL are cable assembly specifications, these items are the only ones applicable to cable assemblies and are not applicable to PHYs.	O	Yes [ ] No [ ]
FFSS	SFP28 to SFP28	136.11.7.2.1	Cable assembly form factor is SFP28 to SFP28	CBL:O.3	Yes [ ] No [ ] N/A [ ]
FFQS	QSFP28 to 4×SFP28	136.11.7.2.2 and 136.11.7.2.3	Cable assembly form factor is QSFP28 to 4×SFP28	CBL:O.3	Yes [ ] No [ ] N/A [ ]
FFQQ	QSFP28 to QSFP28	136.11.7.2.4	Cable assembly form factor is QSFP28 to QSFP28	CBL:O.3	Yes [ ] No [ ] N/A [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

136.14.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136.14.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PF1	Transmit function in DATA mode	136.8.2	Converts each symbol stream from the PMD service interface into an electrical signal as specified, and delivers it to the MDI	M	Yes [ ]
PF2	Transmit function in TRAINING mode	136.8.2	Converts each symbol stream generated by the PMD control function into an electrical signal as specified, and delivers it to the MDI	M	Yes [ ]
PF4	Receive function	136.8.3	Converts each electrical signal from the MDI into a symbol stream as specified, and delivers it to the PMD service interface	M	Yes [ ]
PF5	Lane-by-lane signal detect	136.8.5	Set to one if training is disabled, otherwise set according to signal_detect	M	Yes [ ]
PF6	Global PMD transmit disable	136.8.6	Function is implemented as specified	O	Yes [ ] No [ ]
PF7	Lane-by-lane PMD transmit disable	136.8.7	Function is implemented as specified	M	Yes [ ]
PF8	PMD fault	136.8.8	PMD_fault variable mapped to the fault bit as specified in 45.2.1.7.3	MD:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PF9	PMD transmit fault	136.8.9	Implemented, PMD_transmit_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.4	MD:O	Yes [ ] No [ ] N/A [ ]
PF10	PMD receive fault	136.8.10	Implemented, PMD_receive_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.5	MD:O	Yes [ ] No [ ] N/A [ ]

136.14.4.2 PMD control function

Item	Feature	Subclause	Value/Comment	Status	Support
PC1	PMD control function	136.8.11	Implemented as specified, one instance for each lane, operating independently	M	Yes [ ]
PC2	Training pattern	136.8.11.1.3	Each lane implements four generator polynomials defined in Table 136–8	M	Yes [ ]
PC3	Training pattern	136.8.11.1.3	State set to the value of seed_*i* at the start of the training pattern	M	Yes [ ]
PC4	Control field structure	136.8.11.2	As shown in Table 136–9	M	Yes [ ]
PC5	Receiver frame lock bit	136.8.11.3.3	Initially set to zero, not set to 1 until local_rf_lock is true	M	Yes [ ]
PC6	Initial condition setting	136.8.11.4	When requested, set according to the request, with values per Table 136–12	M	Yes [ ]
PC7	Handshake timing	136.8.11.6	When the transmitted frame lock bit is 1, acknowledge requests within less than 2 ms	M	Yes [ ]
PC8	Transmit precoded data	136.8.11.7.5	PMD causes adjacent PMA to use or not use precoding on transmitted data according to modulation and precoding status bit	M	Yes [ ]
PC9	Receive precoded data	136.8.11.7.5	PMD informs adjacent PMA about precoding of received data according to modulation and precoding request bit	M	Yes [ ]

136.14.4.3 Transmitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Output voltage specifications	94.3.12.3	Per Table 136–11	M	Yes [ ]
TC2	Differential output return loss	92.8.3.2	Meets equation constraints	M	Yes [ ]
TC3	Common-mode to differential mode output return loss	92.8.3.3	Meets equation constraints	M	Yes [ ]
TC4	Common-mode to common-mode output return loss	92.8.3.4	Meets equation constraints	M	Yes [ ]
TC5	Steady-state voltage, v_f	136.9.3.1.2	Per Table 136–11	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC6	Linear fit pulse peak (min)	136.9.3.1.2	Per Table 136–11	M	Yes [ ]
TC7	Level separation mismatch ratio	136D.3.1.2	Per Table 136–11	M	Yes [ ]
TC8	Absolute coefficient step size	136.9.3.1.4	Per Table 136–11	M	Yes [ ]
TC9	Coefficient range	136.9.3.1.5	Per Table 136–11	M	Yes [ ]
TC10	Signal-to-noise-and-distortion ratio	TBD	Per Table 136–11	M	Yes [ ]
TC11	SNR_{fig}	136D.3.1.7	Per Table 136–11	M	Yes [ ]
TC12	Output jitter	136D.3.1.1	Per Table 136–11	M	Yes [ ]
TC14	Transmitter signaling rate	136.9.3	26.5625 GBd ± 100 ppm	M	Yes [ ]

136.14.4.4 Receiver specifications

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential return loss at TP3	92.8.4.2	Meets equation constrains	M	Yes [ ]
RC2	Differential to common-mode return loss at TP3	92.8.4.3	Meets equation constrains	M	Yes [ ]
RC3	Input amplitude tolerance	136.9.4.1	PMD BER better than 10^{-4} under described conditions	M	Yes [ ]
RC4	Interference tolerance	136.9.4.2	PHY meets FEC symbol error ratio requirement in all tests defined in Table 136–13 with the specified test setup and procedure	M	Yes [ ]
RC5	Jitter tolerance	136.9.4.3	PHY meets FEC symbol error ratio requirement with the specified test setup and procedure	M	Yes [ ]
RC6	Signaling rate range	136.9.4.4	PHY complies with receiver requirements for signaling rate of 26.5625 GBd ± 100 ppm	M	Yes [ ]

136.14.4.5 Cable assembly specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CA1	Differential reference impedance	136.11.1	100 Ω	CBL:M	Yes [ ] N/A [ ]
CA2	Minimum insertion loss	136.11.2	Per Equation (92–26)	CBL:M	Yes [ ] N/A [ ]
CA3	Maximum insertion loss at 13.28 GHz	136.11.2	16.06 dB	CBL:M	Yes [ ] N/A [ ]
CA4	Differential return loss	92.10.3	Per Equation (92–27)	CBL:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
CA5	Differential to common-mode input and output return loss	92.10.4	Per Equation (92–28)	CBL:M	Yes [ ] N/A [ ]
CA6	Differential to common-mode conversion loss	92.10.5	Per Equation (92–29)	CBL:M	Yes [ ] N/A [ ]
CA7	Common-mode to common-mode return loss	92.10.6	Per Equation (92–30)	CBL:M	Yes [ ] N/A [ ]
CA8	Cable assembly Channel Operating Margin (COM)	136.11.7	Greater than or equal to 3 dB for both Test 1 and Test 2, for all channels within the cable assembly	CBL:M	Yes [ ] N/A [ ]
CA9	AC-coupling	136.12	Within the plug connector, on the receive lane, 3 dB cutoff frequency less than 50 kHz	CBL:M	Yes [ ] N/A [ ]

136.14.4.6 MDI connector specifications

Item	Feature	Subclause	Value/Comment	Status	Support
MDIS	Single-lane MDI connector	136.12	Device uses SFP28 receptacle as MDI connector	O:4	Yes [ ] No [ ]
MDIQ	Quad-lane MDI connector	136.12	Device uses QSFP28 receptacle as MDI connector	O:4	Yes [ ] No [ ]

136.14.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Environmental specifications	136.13	Conform to applicable requirements of 14.7	M	Yes [ ]

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137. Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4

137.1 Overview

This clause specifies the 50GBASE-KR PMD, the 100GBASE-KR2 PMD, the 200GBASE-KR4 PMD, and the baseband medium. The specifications for the three PMDs are similar, except for the number of lanes and associated parameters and the MDI.

When forming a complete Physical Layer, a PMD shall be connected as illustrated in Figure 137–1, to the appropriate sublayers (as specified in Table 137–1, Table 137–2, and Table 137–3), to the medium through the appropriate MDI, and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 137–1—Physical Layer clauses associated with the 50GBASE-KR PMD

Associated clause	50GBASE-KR
132—RS	Required
132—50GMII[a]	Optional
133—PCS for 50GBASE-R	Required
134—RS-FEC	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135D—50GAUI-2 C2C	Optional
135F—50GAUI-1 C2C	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The 50GMII is an optional interface. However, if the 50GMII is not implemented, a conforming implementation must behave functionally as though the RS and 50GMII were present.

For the 50GBASE-KR and 100GBASE-KR2 PHYs, in order to support the required frame loss ratio (see 1.4.223) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are required to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 10^{-10} after processing by the RS-FEC (Clause 134 or Clause 91) and the PCS (Clause 133 or Clause 82) if there are negligible errors due to other electrical interfaces (50GAUI-n or 100GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 10^{-10}.

For the 200GBASE-KR4 PHY, in order to support the required frame loss ratio (see 1.4.223) of less than 6.2×10^{-11} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are required to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 9.2×10^{-13} after processing by the PCS (Clause 119) if there are negligible errors due to other electrical interfaces (200GAUI-n). If the PMD

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Table 137–2—Physical Layer clauses associated with the 100GBASE-KR2 PMD

Associated clause	100GBASE-KR2
80—RS	Required
80—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R	Optional[b]
83A—CAUI-10	Optional
83D—CAUI-4 C2C	Optional
135—PMA for 100GBASE-P	Required
135D—100GAUI-4 C2C	Optional
135F—100GAUI-2 C2C	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.
[b]PMA for 100GBASE-R is required when either CAUI-10 or CAUI-4 is used.

Table 137–3—Physical Layer clauses associated with the 200GBASE-KR4 PMD

Associated clause	200GBASE-KR4
117—RS	Required
117—200GMII[a]	Optional
119—PCS for 200GBASE-R	Required
120—PMA for 200GBASE-R	Required
120B—200GAUI-8 C2C	Optional
120D—200GAUI-4 C2C	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The 200GMII is an optional interface. However, if the 200GMII is not implemented, a conforming implementation must behave functionally as though the RS and 200GMII were present.

and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 9.2×10^{-13}.

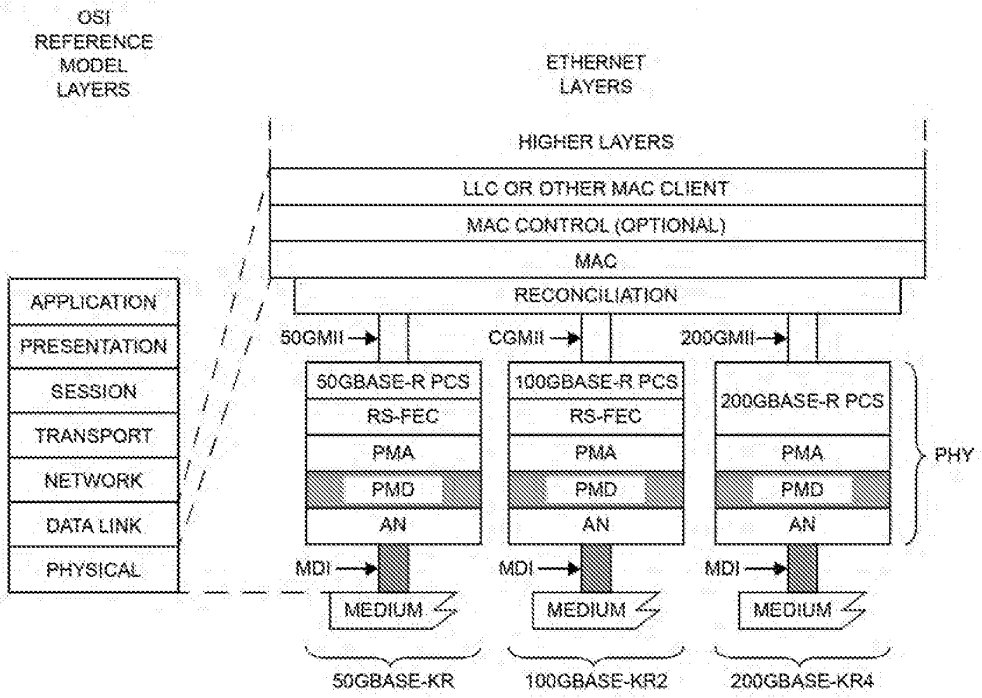
A compliant input signal is a transmitter output of a compliant PHY that has passed through a compliant channel.

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50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Figure 137–1 shows the relationship of the PMD and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 137–1—50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

137.2 Conventions

Clause 137 describes three PMDs, 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4, which have one, two, and four lanes, respectively. For efficient description, the parameter n is used to describe the number of lanes in a specific PMD. Accordingly, n = 1 for 50GBASE-KR, n = 2 for 100GBASE-KR2, and n = 4 for 200GBASE-KR4.

The parameter *i* is used as an index or a suffix to identify a specific lane, and takes the values 0 to n – 1.

Within this clause, the unqualified term "PMD" refers to any of 50GBASE-KR PMD, 100GBASE-KR2 PMD, or 200GBASE-KR4 PMD.

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137.3 PMD service interfaces

The service interfaces of the 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 PMDs are identical to those of the 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMDs, respectively (see 136.3).

137.4 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with the PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. The requirements are the same as those specified in 136.4.

137.5 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the PMD and AN including the medium in one direction shall be no more than the maximum delays listed in Table 137–4. It is assumed that the one-way delay through the medium is no more than 20 ns.

Table 137–4—Delay constraints

PMD	Maximum (bit times)[a]	Maximum (pause_quanta)[b]	Maximum (ns)
50GBASE-KR	2048	4	40.96
100GBASE-KR2	4096	8	40.96
200GBASE-KR4	8192	16	40.96

[a]One bit time is equal to 20 ps for 50GBASE-KR, 10 ps for 100GBASE-KR2, and 5 ps for 200GBASE-KR4. (See 1.4.117 for the definition of bit time.)
[b]One pause_quantum is equal to 10.24 ns for 50GBASE-KR, 5.12 ns for 100GBASE-KR2, and 2.56 ns for 200GBASE-KR4. (See 31B.2 for the definition of pause_quanta.)

Descriptions of overall system delay constraints can be found in 131.4 for 50GBASE-KR, in 80.4 for 100GBASE-KR2, and in 116.4 for 200GBASE-KR4.

137.6 Skew constraints

The Skew (relative delay) between the PCS or FEC lanes must be kept within limits so that the information on the PCS or FEC lanes can be reassembled by the PCS or FEC. The Skew Variation must also be limited to ensure that a given PCS or FEC lane always traverses the same physical lane.

137.6.1 Skew Constraints for 50GBASE-KR

Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

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The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2.

137.6.2 Skew Constraints for 100GBASE-KR2 and 200GBASE-KR4

Skew and Skew Variation are defined in 80.5 and 136.5 and specified at the points SP1 to SP6 shown in Figure 80–8 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5 and 136.5.

137.7 PMD MDIO function mapping

The PMD MDIO function mapping requirements for the PMDs defined in this clause are identical to those of 136.7.

137.8 PMD functional specifications

137.8.1 Link block diagram

One direction of a 50GBASE-KR, 100GBASE-KR2, or 200GBASE-KR4 link is shown in Figure 137–2.

137.8.2 PMD transmit function

The PMD transmit function specification is identical to that of 136.8.2 with the exception that electrical signals are delivered to the MDI, according to the transmit electrical specifications in 137.9.2.

137.8.3 PMD receive function

The PMD transmit function specification is identical to that of 136.8.3.

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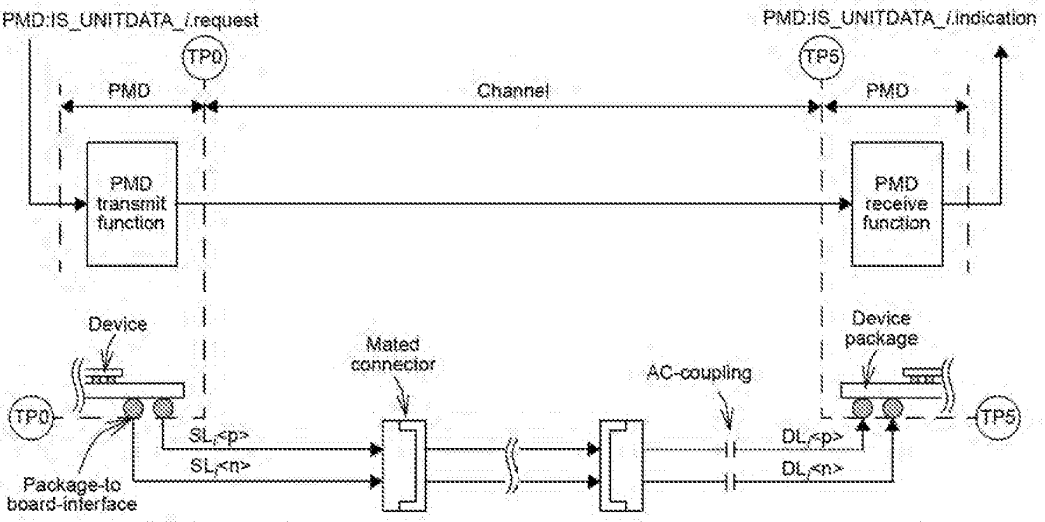


Figure 137–2—50GBASE-KR, 100GBASE-KR2 or 200GBASE-KR4 link (one direction for one lane is illustrated)

137.8.4 PMD global signal detect function

The PMD global signal function specification is identical to that of 136.8.4.

137.8.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal function specification is identical to that of 136.8.5.

137.8.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional. Its specification is identical to that of 136.8.6.

137.8.7 PMD lane-by-lane transmit disable function

The PMD global transmit disable function specification is identical to that of 136.8.7.

137.8.8 PMD fault function

The PMD fault function specification is identical to that of 136.8.8.

137.8.9 PMD transmit fault function (optional)

The PMD transmit fault function is optional. Its specification is identical to that of 136.8.9.

137.8.10 PMD receive fault function (optional)

The PMD receive fault function is optional. Its specification is identical to that of 136.8.10.

137.8.11 PMD control function

The PMD control function specification is identical to that of 136.8.11.

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137.9 Electrical characteristics

137.9.1 MDI

The MDI for the 50GBASE-KR, 100GBASE-KR2 and 200GBASE-KR4 PHYs is an implementation-dependent direct electrical connection between the PMD and the medium. The MDI comprises 2 × n differential pairs, one pair for the transmit function and one pair for the receive function on each lane, marked by TP0 and TP5 in Figure 137–2.

Transmitter and receiver characteristics are defined at TP0a and TP5a, which are connected to the MDI through the test fixtures described in 93.8.1.1 and 93.8.2.1.

137.9.2 Transmitter characteristics

The transmitter shall meet the specifications given in Table 120D–1, with the following exceptions:

1) The value of linear fit pulse peak (min) is $0.75 \times v_f$.
2) The output waveform Pre-cursor equalization and Post-cursor equalization parameters are replaced by the "Transmitter output waveform" specifications summarized in Table 136–11 and detailed in 136.9.3.1.
3) SNR_{ISI} is computed with N_b set to 12 and D_p set to 3.
4) The value of SNR_{ISI} (min) is 43 dB.

Editor's note (to be removed prior to publication): The specified minimum SNDR in Annex 120D is 31 dB, which matches the value of the COM parameter SNR_{TX} in that annex. In this draft, SNR_{TX} in Table 137–5 is 32.5 dB, due to the more challenging channel objectives. It is possible that the SNDR specification becomes another exception to the transmitter characteristics of Annex 120D.

137.9.3 Receiver characteristics

Receiver electrical characteristics are specified at TP5a. The receiver shall meet the specifications given in Table 120D–5 with the following exceptions:

1) The maximum RS-FEC Symbol error ratio values in Table 120D–6 and Table 120D–7 are all 10^{-3}.
2) Insertion loss at 13.28 GHz values for Test 1 are 14.5 (min) and 15.5 (max).
3) Insertion loss at 13.28 GHz values for Test 2 are 29.5 (min) and 30.5 (max).
4) RSS_DFE4 value for Test 1 is 0.05.
5) Receiver jitter tolerance (see 120D.3.2.2) is tested using the test channel in item 3).

In addition, the return loss specifications in 137.9.3.1 apply.

137.9.3.1 Receiver input return loss

The differential return loss, in dB, of the receiver input shall meet Equation (137–1) where f is the frequency in GHz. The reference impedance for differential return loss measurements shall be 100 Ω.

$$RL_d(f) \geq \begin{cases} 12.05 - f & 0.05 \leq f \leq 6 \\ 6.5 - 0.075f & 6 < f \leq 19 \end{cases} \text{ dB} \qquad (137\text{–}1)$$

The differential return loss limit is illustrated by Figure 137–3.

The differential to common-mode return loss, in dB, of the receiver input shall meet Equation (137–2).

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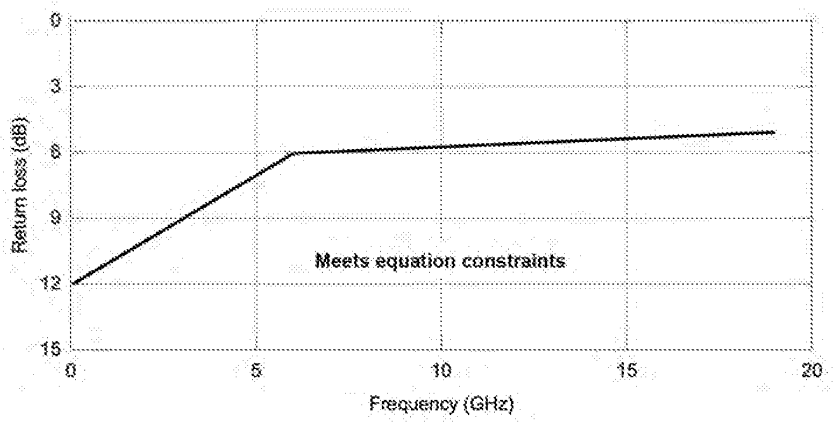


Figure 137–3—Receiver differential return loss limit

$$RL_{cd}(f) = \begin{cases} 25 - 1.44f & 0.05 \le f \le 6.95 \\ 15 & 6.95 < f \le 19 \end{cases} \text{ dB} \qquad (137\text{–}2)$$

The differential to common-mode return loss limit is illustrated by Figure 137–4.

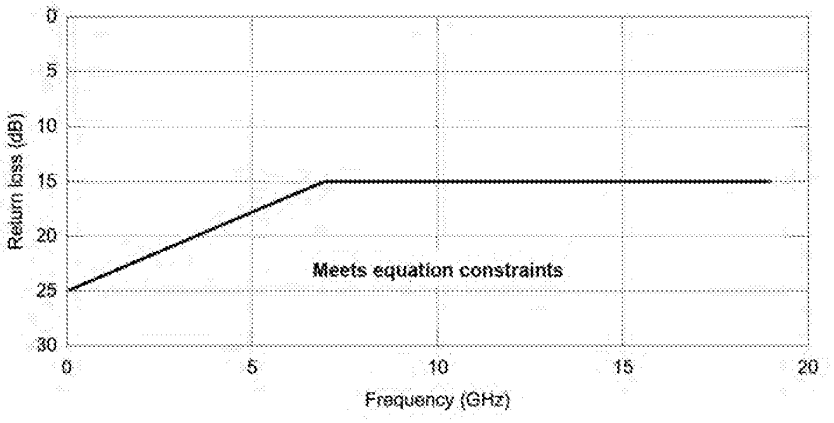


Figure 137–4—Receiver differential to common-mode return loss limit

137.10 Channel characteristics

The Channel Operating Margin (COM) is computed using the procedure in 93A.1 with the values in Table 137–5, where T_r is 12 ps and β is 2 for $H_r(f)$ as used in Equation (93A–19). COM shall be greater than or equal to 3 dB.

Channels shall have AC-coupling as specified in 93.9.4.

Channels are recommended to meet the insertion loss limits in 137.10.1.

Channels shall meet the return loss limits in 137.10.2.

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Table 137–5—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface Package transmission line characteristic impedance	 C_d z_p z_p C_p Z_c	 1.8×10^{-4} 12 30 1.1×10^{-4} 90	 nF mm mm nF Ω
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 -0.25 0 0.05	 — — —
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.1 0.025	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 -0.25 0 0.05	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 -20 0 1	 dB dB dB
Continuous time filter, DC gain 2 Minimum value Maximum value Step size	g_{DC2}	 -6 0 1	 dB dB dB
Continuous time filter, zero frequencies	f_{z1} f_{z2}	$f_b / 2.5$ $f_b / 40$	GHz GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b / 2.5$ $f_b / 40$	GHz GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.45 0.45 0.63	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB

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Table 137–5—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	UI
Normalized DFE coefficient magnitude limit $n = 1$ $n = 2$ to N_b	$b_{max}(n)$	 0.7 0.2	 — —
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	1.64×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-4}	—

137.10.1 Channel insertion loss

The maximum recommended insertion loss of the channel is given by Equation (137–3).

$$IL(f) \le \begin{cases} 1.25 + 3.9\sqrt{f} + 1.095f & 0.01 \le f \le f_b/2 \\ -12.5 + 3.2f & f_b/2 < f \le f_b \end{cases} \text{ (dB)} \qquad (137\text{–}3)$$

Editor's note (to be removed after draft 1.2): The response to comment #77 against draft 1.1 included a modification of Equation (137–3) with the second line being "12.5 - 3.2f". The editor realized that to be consistent with the first line and the previous equation, the expression should be negated, and hence the implementation differs from the resolved comment.

where

f is the frequency in GHz
f_b is the signaling rate (26.5625) in GHz
$IL(f)$ is the insertion loss at frequency f

The insertion loss limit is illustrated by Figure 137–5.

137.10.2 Channel return loss

The minimum differential return loss of the channel is given by Equation (137–4).

$$RL_d(f) \ge \begin{cases} 12 & 0.05 \le f \le f_b/4 \\ 12 - 15\log_{10}(4f/f_b) & f_b/4 < f \le f_b \end{cases} \text{ dB} \qquad (137\text{–}4)$$

where

f is the frequency in GHz
f_b is the signaling rate (26.5625) in GHz
$RL(f)$ is the return loss at frequency f

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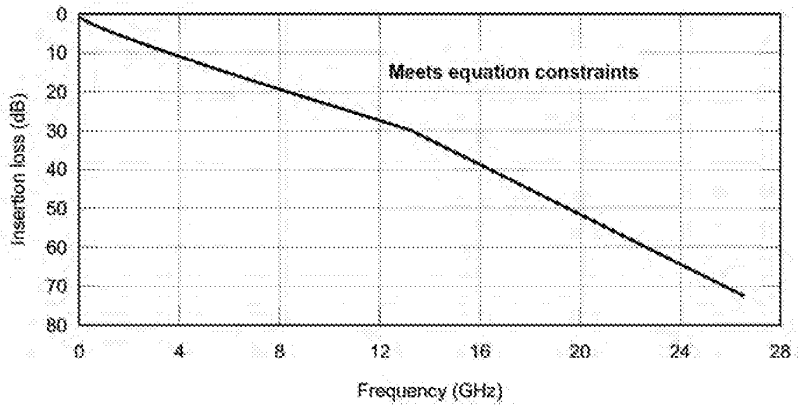


Figure 137–5—Channel insertion loss limit

The differential return loss limit is illustrated by Figure 137–6.

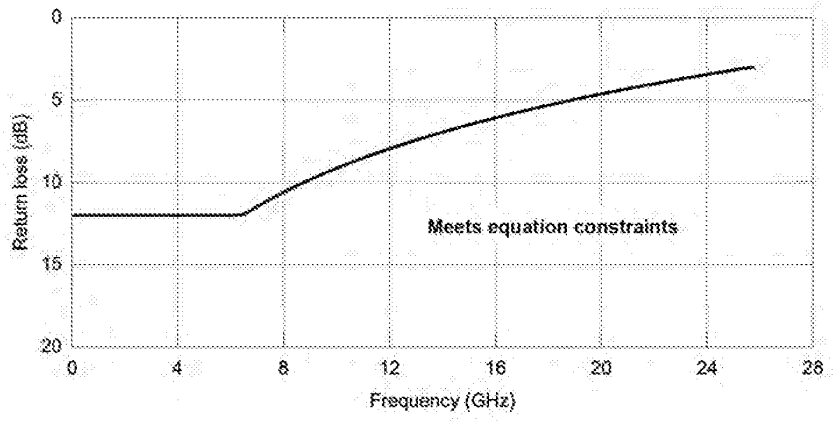


Figure 137–6—Channel differential return loss limit

137.11 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 93.10.

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137.12 Protocol implementation conformance statement (PICS) proforma for Clause 137, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4[10]

137.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 137, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

137.12.2 Identification

137.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

137.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Clause 137, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

137.12.3 Major capabilities/options

[10] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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Item[a]	Feature	Subclause	Value/Comment	Status	Support
*KR	50GBASE-KR PMD	137.1	Can operate as a 50GBASE-KR PMD	O.1	Yes [ ] No [ ]
*KR2	100GBASE-KR2 PMD	137.1	Can operate as a 100GBASE-KR2 PMD	O.1	Yes [ ] No [ ]
*KR4	200GBASE-KR4 PMD	137.1	Can operate as a 200GBASE-KR4 PMD	O.1	Yes [ ] No [ ]
PMA50	50GBASE-R PMA	137.1	Device implements Clause 135 PMA for 50GBASE-R	KR:M	Yes [ ] N/A [ ]
PMA100	100GBASE-P PMA	137.1	Device implements Clause 135 PMA for 100GBASE-P	KR2:M	Yes [ ] N/A [ ]
PMA200	200GBASE-R PMA	137.1	Device implements Clause 120 PMA for 200GBASE-R	KR4:M	Yes [ ] N/A [ ]
*AUIPMD	50GAUI-n C2C, 100GAUI-n C2C, or 200GAUI-n C2C	137.1	Service interface of PMA adjacent to PMD is physically instantiated	O.2	Yes [ ] No [ ]
AUIFEC	LAUI-2 C2C or CAUI-n C2C	137.1	Service interface of PMA between PCS and RS-FEC is physically instantiated	!KR4:O.2	Yes [ ] No [ ] N/A [ ]
*nGMII	50GMII, CGMII or 200GMII and RS	137.1	Interface is implemented or functionally equivalent	O.2	Yes [ ] No [ ]
AN	Auto-negotiation	137.1	Device implements Auto-negotiation	M	Yes [ ]
FEC50	50GBASE-R RS-FEC	137.1	Device implements Clause 134 RS-FEC	KR* !AUIPMD :M	Yes [ ] N/A [ ]
PCS50	50GBASE-R PCS	137.1	Device implements Clause 133 PCS	KR* nGMII:M	Yes [ ] N/A [ ]
FEC100	100GBASE-R RS-FEC	137.1	Device implements Clause 91 RS-FEC with RS(544,514)	KR2* !AUIPMD :M	Yes [ ] N/A [ ]
PCS100	100GBASE-R PCS	137.1	Device implements Clause 82 100GBASE-R PCS	KR2* nGMII:M	Yes [ ] N/A [ ]
PCS200	200GBASE-R PCS	137.1	Device implements Clause 119 200GBASE-R PCS	KR4* nGMII:M	Yes [ ] N/A [ ]
*EEE	EEE fast wake capability	137.1	Capability is supported	nGMII:O	Yes [ ] No [ ] N/A [ ]
PCSAN	PCS requirements for AN service interface	137.4	PCS supports service interface primitive AN_LINK.indication	nGMII:M	Yes [ ] N/A [ ]
DC	Delay constraints	137.5	Conforms to constraints	M	Yes [ ]

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Item[a]	Feature	Subclause	Value/Comment	Status	Support
SC	Skew and Skew Variation constraints	137.6	Conforms to constraints	M	Yes [ ]
*MD	MDIO capability	137.7	Device implements Clause 45 MDIO	O	Yes [ ] No [ ]
*CHNL	Channel	137.10	Item marked with CHNL are channel specifications, these items are the only ones applicable to channels and are not applicable to PHYs.	O	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

137.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4

137.12.4.1 Functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PF1	Transmit function in DATA mode	136.8.2	Converts each symbol stream from the PMD service interface into an electrical signal as specified, and delivers it to the MDI, with the electrical specifications in 137.9.2	M	Yes [ ]
PF2	Transmit function in TRAINING mode	136.8.2	Converts each symbol stream generated by the PMD control function into an electrical signal as specified, and delivers it to the MDI, with the electrical specifications in 137.9.2	M	Yes [ ]
PF4	Receive function	136.8.3	Converts each electrical signal from the MDI into a symbol stream as specified, and delivers it to the PMD service interface	M	Yes [ ]
PF5	Lane-by-lane signal detect	136.8.5	Set to one if training is disabled, otherwise set according to signal_detect	M	Yes [ ]
PF6	Global PMD transmit disable	136.8.6	Function is implemented as specified	O	Yes [ ] No [ ]
PF7	Lane-by-lane PMD transmit disable	136.8.7	Function is implemented as specified	M	Yes [ ]
PF8	PMD fault	136.8.8	PMD_fault variable mapped to the fault bit as specified in 45.2.1.2.3	MD:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PF9	PMD transmit fault	136.8.9	Implemented, PMD_transmit_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.4	MD:O	Yes [ ] No [ ] N/A [ ]
PF10	PMD receive fault	136.8.10	Implemented, PMD_receive_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.5	MD:O	Yes [ ] No [ ] N/A [ ]

137.12.4.2 PMD control function

Item	Feature	Subclause	Value/Comment	Status	Support
PC1	PMD control function	136.8.11	Implemented as specified, one instance for each lane, operating independently	M	Yes [ ]
PC2	Training pattern	136.8.11.1.3	Each lane implements four generator polynomials defined in Table 136–8	M	Yes [ ]
PC3	Training pattern	136.8.11.1.3	State set to the value of seed_*i* at the start of the training pattern	M	Yes [ ]
PC4	Control field structure	136.8.11.2	As shown in Table 136–9	M	Yes [ ]
PC5	Receiver frame lock bit	136.8.11.3.3	Initially set to zero, not set to 1 until local_rf_lock is true	M	Yes [ ]
PC6	Initial condition setting	136.8.11.4	When requested, set according to the request, with values per Table 136–12	M	Yes [ ]
PC7	Handshake timing	136.8.11.6	When the transmitted frame lock bit is 1, acknowledge requests within less than 2 ms	M	Yes [ ]
PC8	Transmit precoded data	136.8.11.7.5	PMD causes adjacent PMA to use or not use precoding on transmitted data according to modulation and precoding status bit	M	Yes [ ]
PC9	Receive precoded data	136.8.11.7.5	PMD informs adjacent PMA about precoding of received data according to modulation and precoding request bit	M	Yes [ ]

137.12.4.3 Transmitter characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	TP0-TP0a test fixture	93.8.1.3	Meets specifications	M	Yes [ ]
TC2	Output voltage specifications	94.3.12.3	Per Table 120D–3	M	Yes [ ]
TC3	Differential output return loss	93.8.1.4	Meets equation constraints	M	Yes [ ]
TC4	Common-mode to common-mode output return loss	93.8.1.4	Meets equation constraints	M	Yes [ ]
TC5	Steady-state voltage, v_f	120D.3.1.4	Per Table 120D–3	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC6	Linear fit pulse peak (min)	137.9.2	$0.75 \times v_f$	M	Yes [ ]
TC7	Level separation mismatch ratio	120D.3.1.2	Per Table 120D–1	M	Yes [ ]
TC8	Absolute coefficient step size	136.9.3.1.4	Per Table 136–11	M	Yes [ ]
TC9	Coefficient range	136.9.3.1.5	Per Table 136–11	M	Yes [ ]
TC10	Signal-to-noise-and-distortion ratio	120D.3.1.6	Per Table 120D–1	M	Yes [ ]
TC11	SNR_{ISI}	137.9.2	Calculated as specified, greater than specified minimum	M	Yes [ ]
TC12	Output jitter	120D.3.1.3	Per Table 136–11	M	Yes [ ]
TC13	Transmitter signaling rate	120D.3.1	26.5625 GBd ± 100 ppm	M	Yes [ ]

137.12.4.4 Receiver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	TP5–TP5a test fixture	93.8.2.1	Meets specifications	M	Yes [ ]
RC2	Input differential return loss	137.9.3.1	Meets equation constrains	M	Yes [ ]
RC3	Input differential to common-mode return loss	137.9.3.1	Meets equation constrains	M	Yes [ ]
RC4	Interference tolerance	137.9.3	PHY meets FEC symbol error ratio requirement in all tests defined in Table 120D–6 with the specified test setup and procedure, and the exceptions listed in 137.9.3	M	Yes [ ]
RC5	Jitter tolerance	137.9.3	PHY meets FEC symbol error ratio requirement in all cases defined in Table 120D–7 with the specified test setup and procedure, and the exceptions listed in 137.9.3	M	Yes [ ]

137.12.4.5 Channel characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Differential return loss	137.10.2	Meets equation constraints	CHNL:M	Yes [ ] N/A [ ]
CC2	Cable assembly Channel Operating Margin (COM)	137.10	Greater than or equal to 3 dB	CHNL:M	Yes [ ] N/A [ ]
CC3	AC-coupling	93.9.4	Between TP0 and TP5, 3 dB cutoff frequency less than 50 kHz	CHNL:M	Yes [ ] N/A [ ]

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137.12.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Environmental specifications	137.11	Conform to applicable requirements of 93.10	M	Yes [ ]

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138. Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4

138.1 Overview

This clause specifies the 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 PMDs together with the multimode fiber medium. The PMD sublayers provide point-to-point 50, 100, and 200 Gigabit Ethernet links over one, two, or four pairs of multimode fiber, with a reach of up to at least 100 m.

When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA, as shown in Table 138–1, Table 138–2, or Table 138–3, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 138–1—Physical Layer clauses associated with the 50GBASE-SR PMD

Associated clause	50GBASE-SR
132—RS	Required
132—50GMII[a]	Optional
133—PCS	Required
134—RS-FEC	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135C—LAUI-2 C2M	Optional
135D—50GAUI-2 C2C	Optional
135E—50GAUI-2 C2M	Optional
135F—50GAUI-1 C2C	Optional
135G—50GAUI-1 C2M	Optional
78—Energy Efficient Ethernet	Optional

[a]The 50GMII is an optional interface. However, if the 50GMII is not implemented, a conforming implementation must behave functionally as though the RS and 50GMII were present.

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Table 138–2—Physical Layer clauses associated with the 100GBASE-SR2 PMD

Associated clause	100GBASE-SR2
80—RS	Required
80—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R	Optional
83A—CAUI-10	Optional
83D—CAUI-4 C2C	Optional
83E—CAUI-4 C2M	Optional
135—PMA for 100GBASE-P	Required
135D—100GAUI-4 C2C	Optional
135E—100GAUI-4 C2M	Optional
135F—100GAUI-2 C2C	Optional
135G—100GAUI-2 C2M	Optional
78—Energy Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.

Table 138–3—Physical Layer clauses associated with the 200GBASE-SR4 PMD

Associated clause	200GBASE-SR4
117—RS	Required
117—200GMII[a]	Optional
119—PCS for 200GBASE-R	Required
120—PMA for 200GBASE-R	Required
120B—200GAUI-8 C2C	Optional
120B—200GAUI-8 C2M	Optional
120D—200GAUI-4 C2C	Optional
120D—200GAUI-4 C2M	Optional
78—Energy Efficient Ethernet	Optional

[a]The 200GMII is an optional interface. However, if the 200GMII is not implemented, a conforming implementation must behave functionally as though the RS and 200GMII were present.

Figure 138–1 shows the relationship of the PMDs and MDIs (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 50 Gigabit Ethernet is introduced in Clause 131 and the purpose of each PHY sublayer is summarized in 131.2. 100 Gigabit Ethernet is intro-

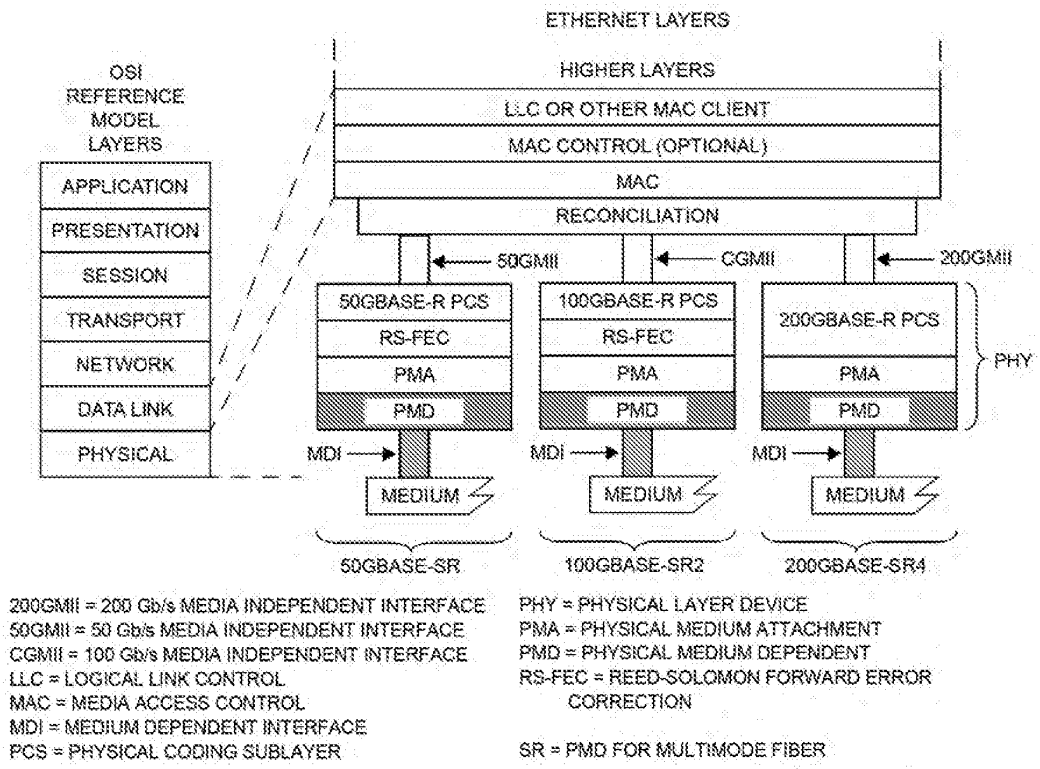
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duced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2. 200 Gigabit Ethernet is introduced in Clause 116 and the purpose of each PHY sublayer is summarized in 116.2.

50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions and abbreviations) and Annex A (bibliography, referenced as [B1], [B2], etc.). The 50GBASE-SR, 100GBASE-SR2 and 200GBASE-SR4 sublayers provide point-to-point 50, 100, and 200 Gigabit Ethernet links over one, two, or four, pairs of multimode fiber, up to at least 100 m.



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

SR = PMD FOR MULTIMODE FIBER

Figure 138–1—50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

138.1.1 Bit error ratio

For the 50GBASE-SR and 100GBASE-SR2 PMDs, the bit error ratio (BER) when processed by the PMA (Clause 135) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.223) of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 134 or Clause 91) and PCS (Clause 133 or Clause 82). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-10} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces. If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap.

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For the 200GBASE-SR4 PMD, the bit error ratio (BER) when processed by the PMA (Clause 120) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.223) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when additionally processed by the PCS (Clause 119). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces. If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.

138.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 50GBASE-SR, 100GBASE-SR2 and 200GBASE-SR4 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The 50GBASE-SR PMD service interface is an instance of the inter-sublayer service interface defined in 131.3, with a single symbol stream (n = 1).

The 100GBASE-SR2 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with two parallel symbol streams (n = 2).

The 200GBASE-SR4 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with four parallel symbol streams (n = 4).

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 50GBASE-SR PMD has a single symbol stream, hence $i = 0$.

The 100GBASE-SR2 PMD has two parallel symbol streams, hence $i = 0$ to 1.

The 200GBASE-SR4 PMD has four parallel symbol streams, hence $i = 0$ to 3.

In the transmit direction, the PMA continuously sends n streams of PAM4 symbols to the PMD, one per lane, using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.6525 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends n streams of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, one per lane, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.6525 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 138.5.4. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_bit parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 138.1.1.

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138.3 Delay and Skew

138.3.1 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation.

The sum of the transmit and receive delays at one end of the link contributed by the 50GBASE-SR PMD including 2 m of fiber in one direction shall be no more than 1 024 bit times (2 pause_quanta or 20.48 ns).

The sum of the transmit and receive delays at one end of the link contributed by the 100GBASE-SR2 PMD including 2 m of fiber in one direction shall be no more than 2 048 bit times (4 pause_quanta or 20.48 ns).

The sum of the transmit and receive delays at one end of the link contributed by the 200GBASE-SR4 PMD including 2 m of fiber in one direction shall be no more than 4 096 bit times (8 pause_quanta or 20.48 ns).

Descriptions of overall system delay constraints and the definitions for bit times and pause_quanta, can be found in 131.4 for 50GBASE-SR, in 80.4 for 100GBASE-SR2, and in 116.4 and its references for 200GBASE-SR4.

138.3.2 Skew constraints

The Skew (relative delay) between the PCS or FEC lanes must be kept within limits so that the information on the PCS or FEC lanes can be reassembled by the PCS or FEC. The Skew Variation must also be limited to ensure that a given PCS or FEC lane always traverses the same physical lane.

138.3.2.1 Skew Constraints for 50GBASE-SR

Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2.

138.3.2.2 Skew Constraints for 100GBASE-SR2 and 200GBASE-SR4

Skew and Skew Variation are defined in 80.5 and 116.5 and specified at the points SP1 to SP6 shown in Figure 80–8 and Figure 116–5.

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If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5 and 116.5.

138.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 138–4, and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 138–5.

Table 138–4—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 3	PMD transmit disable register	1.9.4	PMD_transmit_disable_3
PMD transmit disable 2	PMD transmit disable register	1.9.3	PMD_transmit_disable_2
PMD transmit disable 1	PMD transmit disable register	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable register	1.9.1	PMD_transmit_disable_0

138.5 PMD functional specifications

The 100GBASE-SR4 PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

138.5.1 PMD block diagram4

The PMD block diagram is shown in Figure 138–2. 200GBASE-SR4 consists of four lanes per direction, 100GBASE-SR2 consists of two lanes, and 50GBASE-SR consists of just one lane per direction.

For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a multimode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 138.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 138.10.3). Unless specified otherwise, all receiver measurements and tests defined in 138.8 are made at TP3.

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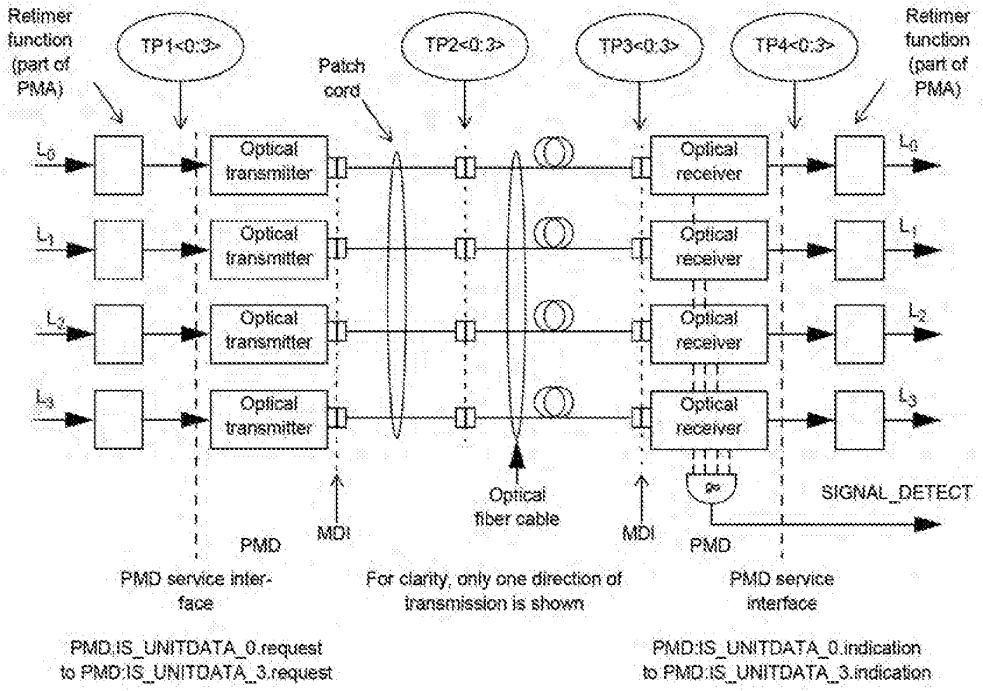


Figure 138–2—Block diagram for 200GBASE-SR4 transmit/receive paths

Table 138–5—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 3	PMD receive signal detect register	1.10.4	PMD_signal_detect_3
PMD receive signal detect 2	PMD receive signal detect register	1.10.3	PMD_signal_detect_2
PMD receive signal detect 1	PMD receive signal detect register	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect register	1.10.1	PMD_signal_detect_0

TP1<0:3> and TP4<0:3> are informative reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

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138.5.2 PMD transmit function

The PMD Transmit function shall convert the one, two, or four signal streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request into one, two, or four separate optical signal streams. Each optical signal stream shall then be delivered to the MDI, which contains one, two, or four parallel light paths for transmit, according to the transmit optical specifications in this clause. The higher optical power level in each signal shall correspond to tx_symbol = three and the lowest shall correspond to tx_symbol = zero.

138.5.3 PMD receive function

The PMD Receive function shall convert the one, two, or four parallel optical signal streams received from the MDI into separate symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_symbol = three and the lowest shall correspond to rx_symbol = zero.

138.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 80.3.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all four lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 138–6. The PMD receiver is not required to verify whether a compliant 50GBASE-SR, 100GBSE-SR2, or 200GBASE-SR4 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 138–6—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –30 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 138–8) AND (compliant 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 signal input)]	OK
All other conditions	Unspecified

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modula-

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tion of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

138.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:3, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 138–6.

138.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

138.5.7 PMD global transmit disable function (optional)

The PMD_global_transmit_disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 138–8.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable to one, turning off the optical transmitter in each lane.

138.5.8 PMD lane-by-lane transmit disable function (optional)

The PMD_transmit_disable_*i* (where *i* represents the lane number in the range 0:3) function is optional and allows the optical transmitter in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 138–8.

b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the optical transmitter in each lane.

If the optional PMD_transmit_disable_*i* function is not implemented in MDIO, an alternative method may be provided to independently disable each transmit lane.

138.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

138.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set PMD_transmit_fault to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4

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138.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

138.6 Lane assignments

There are no lane assignments (within a group of transmit or receive lanes) for 100GBASE-SR2 or 200GBASE-SR4. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the physical ordering of the lanes, as the RS-FEC sublayer is capable of receiving the lanes in any arrangement. The positioning of transmit and receive lanes at the MDI is specified in 138.10.3.1.

138.7 PMD to MDI optical specifications for 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4

The operating range for the 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 PMDs is defined in Table 138–7. A compliant PMD operates on 50/125 μm multimode fibers, type A1a.2 (OM3), type A1a.3 (OM4), or fiber compliant to TIA-492AAAE, according to the specifications defined in Table 138–14. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 50GBASE-SR PMD operating at 120 m meets the operating range requirement of 0.5 m to 100 m).

Table 138–7—Operating range

PMD type	Required operating range[a]
50GBASE-SR 100GBASE-SR2 200GBASE-SR4	0.5 m to 70 m for OM3
	0.5 m to 100 m for OM4
	0.5 m to 100 m for wideband MMF (TIA-492AAAE)

[a]The PCS FEC correction function may not be bypassed for any operating distance.

138.7.1 Transmitter optical specifications

Each lane of a 50GBASE-SR, 100GBASE-SR2 and 200GBASE-SR4 transmitter shall meet the specifications in Table 138–8 per the definitions in 138.8.

138.7.2 Receiver optical specifications

Each lane of a 50GBASE-SR, 100GBASE-SR2 and 200GBASE-SR4 receiver shall meet the specifications in Table 138–9 per the definitions in 138.8.

138.7.3 Illustrative link power budget

An illustrative power budget and penalties for 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 channels are shown in Table 138–10.

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Table 138–8—Transmit characteristics

Description	Value	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm	GBd
Modulation format	PAM4	
Center wavelength (range)	840 to 860	nm
RMS spectral width[a] (max)	0.6	nm
Average launch power, each lane (max)	4	dBm
Average launch power, each lane (min)	–6	dBm
Outer Optical Modulation Amplitude (OMA), each lane (max)	3	dBm
Outer Optical Modulation Amplitude (OMA), each lane (min)[b]	–4 *TBC*	dBm
Launch power in OMA_{outer} minus TDECQ (min)	–5 *TBC*	dBm
Transmitter and dispersion eye closure (TDECQ), each lane (max)	4 *TBC*	dB
Average launch power of OFF transmitter, each lane (max)	–30	dBm
Extinction ratio (min)	3	dB
Optical return loss tolerance (max)	12	dB
Encircled flux[c]	≥ 86% at 19 µm ≤ 30% at 4.5 µm	

[a]RMS spectral width is the standard deviation of the spectrum.
[b]Even if the TDEC < 1 dB, the OMA (min) must exceed this value.
[c]If measured into type A1a.2 or type A1a.3, 50 µm fiber, in accordance with IEC 61280-1-4, or fiber compliant to TIA-492AAAE.

Table 138–9—Receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm	GBd
Modulation format	PAM4	
Center wavelength (range)	840 to 860	nm
Damage threshold[a] (min)	5	dBm
Average receive power, each lane (max)	4	dBm
Average receive power, each lane[b] (min)	–7.9	dBm
Receive power, each lane (OMA_{outer}) (max)	3	dBm
Receiver reflectance (max)	–12	dB
Stressed receiver sensitivity (OMA_{outer}), each lane[c] (max)	–3 *TBC*	dBm
Receiver sensitivity (OMA_{outer}), each lane[d] (max)	-7 *TBC*	
Conditions of stressed receiver sensitivity test:[e]		
Stressed eye closure (SECQ), lane under test	4 *TBC*	dB
OMA_{outer} of each aggressor lane[f]	3	dBm

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[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[b]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Measured with conformance test signal at TP3 (see 138.8.8) for the BER specified in 138.1.1.
[d]Receiver sensitivity is informative.
[e]These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f]Only applies to 100GBASE-SR2 and 200GBASE-SR4.

Table 138–10—Illustrative link power budget

Parameter	OM3	OM4	Wideband MMF (TIA-492AAAE)	Unit
Effective modal bandwidth at 850 nm[a]	2000	4700		MHz.km
Power budget (for max TDECQ)	6 *TBC*			dB
Operating distance	0.5 to 70	0.5 to 100		m
Channel insertion loss[b]	1.8	1.9		dB
Allocation for penalties[c] (for max TDECQ)	4.1 *TBC*			dB
Additional insertion loss allowed	0.1	0		dB

[a]Per IEC 60793-2-10.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 138–7 and cabled optical fiber attenuation of 3.5 dB/km at 850 nm plus an allocation for connection and splice loss given in 138.10.2.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

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138.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

138.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 138–12 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 138–12 may be used to perform that test. The test patterns used in this clause are shown in Table 138–11.

Table 138–11—Test patterns

Pattern	Pattern description	Defined in
3	PRBS31Q	120.5.11.2.4
4	PRBS13Q	120.5.11.2.3
5	Scrambled idle	119.2.4.9
6	SSPRQ	120.5.11.2.5

Table 138–12—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength, spectral width	3, 4, 5, 6, or valid 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 signal	138.8.2
Average optical power	3, 4, 5, 6, or valid 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 signal	138.8.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	138.8.4
Transmitter and dispersion eye closure - quaternary (TDECQ)	6	138.8.5
Extinction ratio	4 or 6	138.8.6
Stressed receiver sensitivity	3, 5, or valid 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 signal	138.8.8
Stressed eye closure (SEC), calibration	6	138.8.8

138.8.1.1 Multi-lane testing considerations

Stressed receiver sensitivity is defined for each lane at the BER specified in 138.1.1. Measurements with Pattern 3 (PRBS31Q) allow lane-by-lane BER measurements. In stressed receiver sensitivity measurements, unstressed lanes may be created by setting the power at the receiver under test well above its sensitivity and/or not stressing those lanes with ISI and jitter, or by other means. Each receive lane is stressed in turn while all are operated. All aggressor lanes are operated as specified. Where relevant, parameters are defined with all co-propagating and counter-propagating lanes operational so that crosstalk effects are included.

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Where not otherwise specified, the maximum amplitude (OMA or VMA) for a particular situation is used, and for counter-propagating lanes, the minimum transition time is used. Alternative test methods that generate equivalent results may be used. While the lanes in a particular direction may share a common clock, the Tx and Rx directions are not synchronous to each other. If Pattern 3 is used for the lanes not under test using a common clock, there is at least 31 UI TBC delay between the PRBS31Q patterns on one lane and any other lane.

138.8.2 Center wavelength and spectral width

The center wavelength and RMS spectral width of each optical lane shall be within the range given in Table 138–8 if measured per TIA/EIA-455-127-A or IEC 61280-1-3. The lane under test is modulated using one of the test patterns specified in Table 138–12.

138.8.3 Average optical power

The average optical power of each lane shall be within the limits given in Table 138–8 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using one of the test patterns defined in Table 138–12, per the set up shown in Figure 53–6.

138.8.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} of each lane shall be within the limits given in Table 138–8 if measured as defined in 121.8.4.

138.8.5 Transmitter and dispersion eye closure - quaternary (TDECQ)

TDECQ is a measure of each optical transmitter's vertical eye closure as measured through an optical to electrical converter (O/E) with a bandwidth equivalent to a combined reference receiver and worst case optical channel, and equalized with the reference equalizer specified in 121.8.5. Table 138–9 specifies the test pattern to be used for measurement of TDECQ.

TDECQ of each lane shall be within the limits given in Table 138–8 if measured using the methods specified in 121.8.5, with the following exceptions:

- The polarization controller and test fiber shown in Figure 121–4 are not used
- The optical channel requirements in 121.8.5.2 do not apply
- The combination of the O/E and the oscilloscope used to measure the optical waveform has a fourth-order Bessel-Thomson filter response with a bandwidth of 12.6 GHz.
- The reference equalizer to be used for TDECQ for 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 is specified in 138.8.5.1.

138.8.5.1 TDECQ reference equalizer

The reference equalizer for 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 is a 5 tap, T/2 spaced, feed-forward equalizer (FFE), where T is the symbol period.

138.8.6 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 138–8 if measured using the methods specified in 121.8.6.

138.8.7 Receiver sensitivity

Receiver sensitivity, which is defined for an ideal input signal, is informative and compliance is not required. If measured, the test signal should have negligible impairments such as intersymbol interference

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(ISI), rise/fall times, jitter and RIN. Instead, the normative requirement for receivers is stressed receiver sensitivity.

138.8.8 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 138–9 if measured using the methodology defined in 121.8.9.1 and 121.8.9.3, with the conformance test signal at TP3 as described in 121.8.9.2, with the following exceptions:

- The test patterns used for stressed receiver sensitivity are specified in Table 138–12
- The signaling rate and the required stressed eye closure (SECQ) of the stressed receiver conformance test signal is specified in Table 138–9
- The applied sinusoidal jitter is specified in 138.8.8.1
- For 100GBASE-SR2 and 200GBASE-SR4, the OMA_{outer} of the aggressor lanes is specified in Table 138–9
- The SECQ of the stressed receiver conformance test signal is measured according to 138.8.5, except that the combination of the O/E and the oscilloscope has a fourth-order Bessel-Thomson filter response with a bandwidth of 19.34 GHz TBC, and the optical splitter and variable reflector shown in Figure 121–4 are not used.

The BER is required to be met for each lane under test on its own. Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Any of the patterns specified for stressed receiver sensitivity in Table 138–12 is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

138.8.8.1 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 138–13.

Table 138–13—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter peak-to-peak (UI)
$f \leq 40$ kHz	Not specified
40 kHz $< f \leq 4$ MHz	$2 \times 10^6/f$
4 MHz $< f \leq 10\ LB$[a]	0.05

[a] LB = loop bandwidth; upper frequency bound for added sinusoidal jitter should be at least 10 times the loop bandwidth of the receiver being tested.

138.9 Safety, installation, environment, and labeling

138.9.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1.

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138.9.2 Laser safety

50GBASE-SR, 100GBASE-SR2 and 200GBASE-SR4 optical transceivers shall conform to Hazard Level TBD laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[11]

138.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

138.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate, in the literature associated with the PHY, the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

138.9.5 Electromagnetic emission

A system integrating a 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

138.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

138.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4).

Labeling requirements for Hazard Level TBD lasers are given in the laser safety standards referenced in 138.9.2.

---

[11] A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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138.10 Fiber optic cabling model

The fiber optic cabling (channel) contains 1, 2, or 4 optical fibers for each direction to support 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4, respectively. The fiber optic cabling interconnects the transmitters at the MDI on one end of the channel to the receivers at the MDI on the other end of the channel. As defined in 138.10.3, the optical lanes appear in defined locations at the MDI but the locations are not assigned specific lane numbers within this standard because any transmitter lane may be connected to any receiver lane.

138.10.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 138–3.

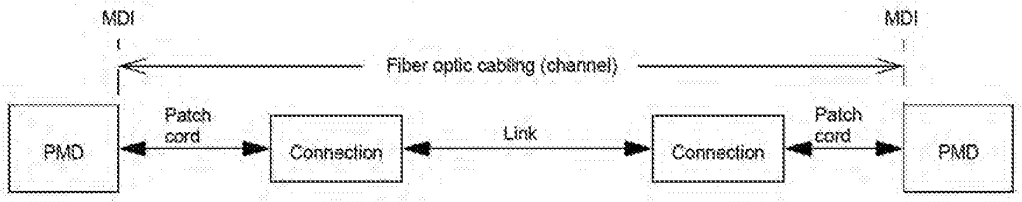


Figure 138–3—Fiber optic cabling model

The channel insertion loss is given in Table 138–14. A channel may contain additional connectors as long as the optical characteristics of the channel (such as attenuation, modal dispersion, reflections and losses of all connectors and splices) meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1:2009. As OM4 and wideband MMF (TIA-492AAAE) optical fiber meet the requirements for OM3, a channel compliant to the "OM3" column may use OM4 or wideband MMF (TIA-492AAAE) optical fiber, or a combination of OM3, OM4 and wideband MMF (TIA-492AAAE). The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term *channel* is used here for consistency with generic cabling standards.

Table 138–14—Fiber optic cabling (channel) characteristics

Description	OM3	OM4	Wideband MMF (TIA-492AAAE)	Unit
Operating distance (max)	70	100		m
Cabling Skew (max)[a]	79			ns
Cabling Skew Variation[a,b] (max)	2.4			ns
Channel insertion loss[c] (max)	1.8	1.9		dB
Channel insertion loss (min)	0			dB

[a]Only applies to 100GBASE-SR2 and 200GBASE-SR4.
[b]An additional 400 ps of Skew Variation could be caused by wavelength changes, which are attributable to the transmitter not the channel.
[c]These channel insertion loss values include cable loss plus 1.5 dB allocated for connection and splice loss, over the wavelength range 840 nm to 860 nm.

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138.10.2 Characteristics of the fiber optic cabling (channel)

The fiber optic cabling shall meet the specifications defined in Table 138–14. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

138.10.2.1 Optical fiber cable

The fiber contained within the fiber optic cabling shall comply with the specifications and parameters of Table 138–15. A variety of multimode cable types may satisfy these requirements, provided the resulting channel also meets the specifications of Table 138–14.

Table 138–15—Optical fiber and cable characteristics

Description	OM3[a]	OM4[b]	Wideband MMF[c]	Unit
Nominal core diameter	50			μm
Nominal fiber specification wavelength	850			nm
Effective modal bandwidth (min)[d]	2000	4700		MHz.km
Cabled optical fiber attenuation (max)	3.5			dB/km
Zero dispersion wavelength (λ_0)	$1295 \le \lambda_0 \le 1340$		$1297 \le \lambda_0 \le 1328$	nm
Chromatic dispersion slope (max) (S_0)	0.105 for $1295 \le \lambda_0 \le 1310$ and $0.000375 \times (1590 - \lambda_0)$ for $1310 \le \lambda_0 \le 1340$		$-412/(840(1-(\lambda_0/840)^4))$	ps/nm^2 km

[a]IEC 60793-2-10 type A1a.2
[b]IEC 60793-2-10 type A1a.3
[c]TIA-492AAAE
[d]When measured with the launch conditions specified in Table 138–8

138.10.2.2 Optical fiber connection

An optical fiber connection, as shown in Figure 138–3, consists of a mated pair of optical connectors.

138.10.2.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an average insertion loss per connection of 0.5 dB. Connections with lower loss characteristics may be used provided the requirements of Table 138–14 are met. However, the loss of a single connection shall not exceed 0.75 dB.

138.10.2.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –20 dB TBC.

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138.10.3 Medium Dependent Interface (MDI)

The 50GBASE-SR, 100GBASE-SR2 or 200GBASE-SR4 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 138–3). Examples of an MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter;

b) PMD receptacle.

NOTE—Compliance testing is performed at TP2 and TP3 as defined in 138.5.1, not at the MDI.

138.10.3.1 Optical lane assignments for 100GBASE-SR2 and 200GBASE-SR4

The two transmit and two receive optical lanes of 100GBASE-SR2 shall occupy the positions depicted in Figure 138–4 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains four active lanes within 12 total positions. The eight center positions are unused. The transmit optical lanes occupy the leftmost two positions. The receive optical lanes occupy the rightmost two positions.

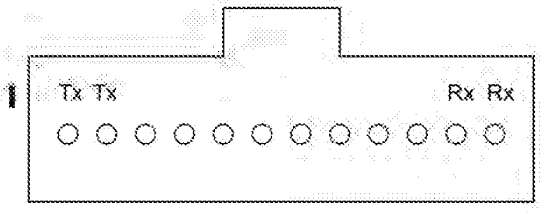


Figure 138–4—Optical lane assignments for 100GBASE-SR2

The four transmit and four receive optical lanes of 200GBASE-SR4 shall occupy the positions depicted in Figure 138–5 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains eight active lanes within 12 total positions. The four center positions are unused. The transmit optical lanes occupy the leftmost four positions. The receive optical lanes occupy the rightmost four positions.

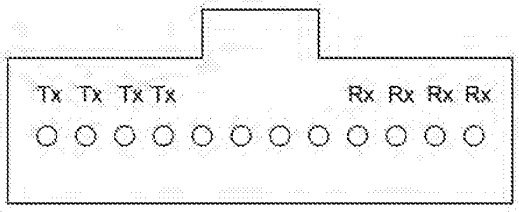


Figure 138–5—Optical lane assignments for 200GBASE-SR4

138.10.3.2 MDI requirements for 50GBASE-SR

The MDI shall optically mate with the compatible plug on the optical fiber cabling. For 50GBASE-SR, when the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2 for performance grade Bm/2m.

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138.10.3.3 MDI requirements for 100GBASE-SR2 and 200GBASE-SR4

The MDI shall optically mate with the compatible plug on the optical fiber cabling. For 100GBASE-SR2 and 200GBASE-SR4 the MDI adapter or receptacle shall meet the dimensional specifications for interface 7-1-3: *MPO adapter interface - opposed keyway configuration*, or interface 7-1-10: *MPO active device receptacle, flat interface*, as defined in IEC 61754-7-1. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-1-4: *MPO female plug connector, flat interface for 2 to 12 fibers*, as defined in IEC 61754-7-1. Figure 138–6 shows an MPO female plug connector with flat interface, and an MDI. The MDI connection shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2 for performance grade Bm/2m.

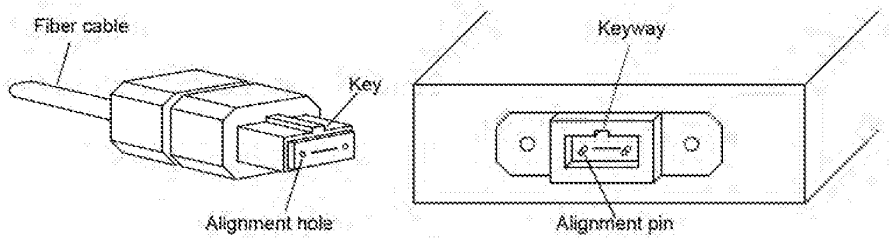


Figure 138–6—MPO female plug with flat interface and MDI active device receptacle with flat interface

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138.11 Protocol implementation conformance statement (PICS) proforma for Clause 138, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4[12]

138.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 138, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

138.11.2 Identification

138.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

138.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-201x, Clause 138, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-201x.)	

Date of Statement	

[12] *Copyright release for PICS proformas:* Users of this standard *may* freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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138.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
SR	50GBASE-SR PMD	138.7	Device supports requirements for 50GBASE-SR PHY	O	Yes [ ] No [ ]
SR2	100GBASE-SR2 PMD	138.7	Device supports requirements for 100GBASE-SR2 PHY	O	Yes [ ] No [ ]
SR4	200GBASE-SR4 PMD	138.7	Device supports requirements for 200GBASE-SR4 PHY	O	Yes [ ] No [ ]
*INS	Installation / cable	138.10.1	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	138.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	138.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	138.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	138.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	138.4	Registers and interface supported	O	Yes [ ] No [ ]

138.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4

138.11.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 50GBASE-R or 100GBASE-R or 200GBASE-R PCS and PMA	138.1		M	Yes [ ]
F2	Integration with management functions	138.1		O	Yes [ ] No [ ]
F3	Bit error ratio	138.1.1	Meets the BER specified in 138.1.1	M	Yes [ ]
F4	Transmit function	138.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
F5	Mapping between optical signal and logical signal for transmitter	138.5.2	Higher optical power is a one	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F6	Receive function	138.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]
F7	Conversion of n optical signals to n electrical signals	138.5.3	For delivery to the PMD service interface	M	Yes [ ]
F8	Mapping between optical signal and logical signal for receiver	138.5.3	Higher optical power is a one	M	Yes [ ]
F9	Global Signal Detect function	138.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	138.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all n lanes	M	Yes [ ]
F11	Lane-by-lane Signal Detect function	138.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 138–6	MD:O	Yes [ ] No [ ] N/A [ ]
F12	PMD reset function	138.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

138.11.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	138.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	138.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD_lane_by_lane_transmit_disable function	138.5.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_*i* variable	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD lane-by-lane transmit disable	138.5.8	Disables each optical transmitter independently if M3 = No	!MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_fault function	138.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M6	PMD_transmit_fault function	138.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
M7	PMD_receive_fault function	138.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

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138.11.4.3 PMD to MDI optical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Transmitter meets specifications in Table 138–8	138.7.1	Per definitions in 138.8	M	Yes [ ]
S2	Receiver meets specifications in Table 138–9	138.7.2	Per definitions in 138.8	M	Yes [ ]

138.11.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	138.8	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and spectral width	138.8.2	Per TIA/EIA-455-127-A or IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	138.8.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA_{outer} measurements	138.8.4	Each lane	M	Yes [ ]
OM5	Transmitter and dispersion eye closure - quaternary (TDECQ)	138.8.5	Each lane	M	Yes [ ]
OM6	Extinction ratio	138.8.6	Per IEC 61280-2-2	M	Yes [ ]
OM7	Stressed receiver sensitivity	138.8.8	See 138.8.8	M	Yes [ ]

138.11.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	138.9.1	Conforms to IEC 60950-1	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level TBD	138.9.2	Conforms to Hazard Level TBD laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	138.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

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138.11.4.6 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	138.10	Meets requirements specified in Table 138–14	INS:M	Yes [ ] N/A [ ]
OC2	Optical fiber characteristics	138.10.1	Per Table 138–15	INS:M	Yes [ ] N/A [ ]
OC3	Maximum discrete reflectance	138.10.2.2	Less than –20 dB	INS:M	Yes [ ] N/A [ ]
OC4	MDI layout for 100GBASE-SR2	138.10.3.1	Optical lane assignments per Figure 138–4	M	Yes [ ]
OC5	MDI layout for 200GBASE-SR4	138.10.3.1	Optical lane assignments per Figure 138–5	M	Yes [ ]
OC6	MDI mating, 50GBASE-SR	138.10.3.2	MDI optically mates with plug on the cabling, performance grade Bm/2m	M	Yes [ ]
OC7	MDI requirements for 50GBASE-SR	138.10.3.2	Per IEC 61753-1 and IEC 61753-022-2	INS:M	Yes [ ] N/A [ ]
OC8	MDI mating, 100GBASE-SR2 and 200GBASE-SR4	138.10.3.3	MDI optically mates with plug on the cabling	M	Yes [ ]
OC9	MDI dimensions	138.10.3.3	Per IEC 61754-7-1 interface 7-1-1	M	Yes [ ]
OC10	Cabling connector dimensions	138.10.3.3	Per IEC 61754-7-1 interface 7-1-1	INS:M	Yes [ ] N/A [ ]
OC11	MDI requirements for 100GBASE-SR2 and 200GBASE-SR4	138.10.3.3	Per IEC 61753-1 and IEC 61753-022-2, performance grade Bm/2m	INS:M	Yes [ ] N/A [ ]

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139. Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR

139.1 Overview

This clause specifies the 50GBASE-FR and the 50GBASE-LR PMDs together with the single-mode fiber medium. The optical signals generated by these two PMD types are modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 139–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 139–1—Physical Layer clauses associated with the 50GBASE-FR and 50GBASE-LR PMDs

Associated clause	50GBASE-FR, 50GBASE-LR
132—RS	Required
132—50GMII[a]	Optional
133—PCS for 50GBASE-R	Required
134—RS-FEC for 50GBASE-R	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135C—LAUI-2 C2M	Optional
135D—50GAUI-2 C2C	Optional
135E—50GAUI-2 C2M	Optional
135F—50GAUI-1 C2C	Optional
135G—50GAUI-1 C2M	Optional
78—Energy Efficient Ethernet	Optional

[a]50GMII is an optional interface. However, if the appropriate interface is not implemented, a conforming implementation must behave functionally as though the RS and 50GMII were present.

Figure 139–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 50 Gigabit Ethernet is introduced in Clause 131 and the purpose of each PHY sublayer is summarized in 139.2.

50GBASE-FR and 50GBASE-LR PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

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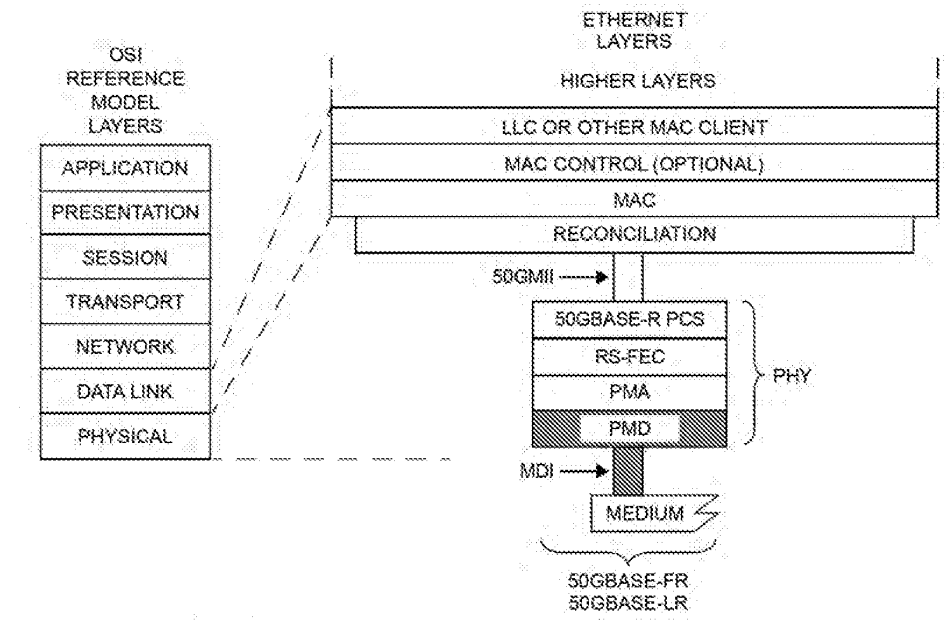


Figure 139–1—50GBASE-FR and 50GBASE-LR PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

139.1.1 Bit error ratio

The bit error ratio (BER) when processed by the PMA (Clause 135) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.223) of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 134) and PCS (Clause 133). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-10} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap.

139.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 50GBASE-FR and 50GBASE-LR PMDs. The service interface for these PMDs is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

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The 50GBASE-FR and 50GBASE-LR PMD service interface is an instance of the inter-sublayer service interface defined in 131.3, with a single symbol stream (n = 1).

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_0.request
PMD:IS_UNITDATA_0.indication
PMD:IS_SIGNAL.indication

In the transmit direction, the PMA continuously sends one stream of PAM4 symbols to the PMD using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.6525 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends one stream of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.6525 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 139.5.4. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_bit parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 139.1.1.

139.3 Delay and Skew

139.3.1 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The sum of the transmit and receive delays at one end of the link contributed by the 50GBASE-FR and 50GBASE-LR PMD2 including 2 m of fiber in one direction shall be no more than 512 bit times (2 pause_quantum or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quantum can be found in 131.4 and its references.

139.3.2 Skew constraints

The Skew (relative delay) between the FEC lanes must be kept within limits so that the information on the lanes can be reassembled by the FEC. The Skew Variation must also be limited to ensure that a given FEC lane always traverses the same physical lane. Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

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If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 80.7.2.

139.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 139–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 139–3.

Table 139–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable

Table 139–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect

139.5 PMD functional specifications

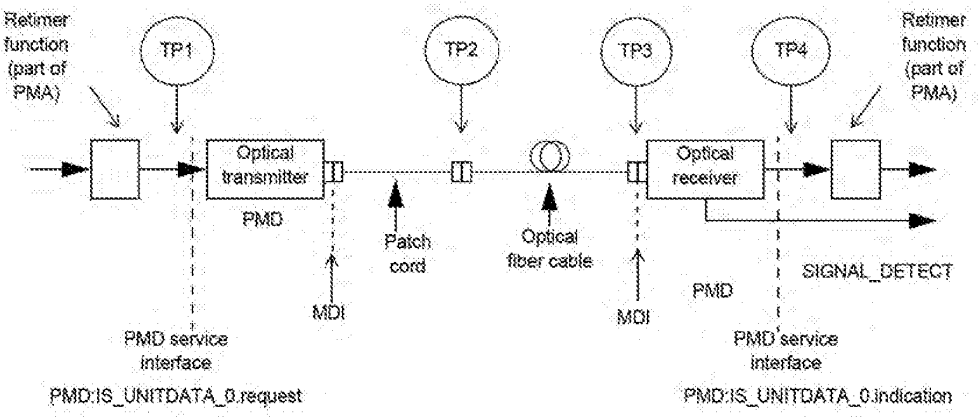
The 50GBASE-FR and 50GBASE-LR PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

139.5.1 PMD block diagram

The PMD block diagram is shown in Figure 139–2 For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 139.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 139.10.3). Unless specified otherwise, all receiver measurements and tests defined in 139.7 are made at TP3.

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For clarity, only one direction of transmission is shown

Figure 139–2—Block diagram for 50GBASE-FR and 50GBASE-LR transmit/receive paths

139.5.2 PMD transmit function

The PMD Transmit function shall convert the symbol stream requested by the PMD service interface messages PMD:IS_UNITDATA_0.request into an optical signal stream. The optical signal stream shall then be delivered to the MDI, according to the transmit optical specifications in this clause. The highest optical power level in the signal stream shall correspond to tx_symbol = three and the lowest shall correspond to tx_symbol = zero.

139.5.3 PMD receive function

The PMD receive function shall convert the optical signal stream received from the MDI into a symbol stream for delivery to the PMD service interface using the message PMD:IS_UNITDATA_0.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_symbol = three and the lowest shall correspond to rx_symbol = zero.

139.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 131.3.

SIGNAL_DETECT shall be a global indicator of the presence of the optical signal. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 139–4. The PMD receiver is not required to verify whether a compliant 50GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

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Table 139–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Average optical power at TP3 ≤ –20 dBm	FAIL
[(Optical power at TP3 ≥ average receive power in Table 139–7) AND (compliant 50GBASE-R signal input)]	OK
All other conditions	Unspecified

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

139.5.5 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

139.5.6 PMD global transmit disable function (optional)

The PMD_global_transmit_disable function is optional and allows the optical transmitter to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of the OFF transmitter in Table 139–6.
b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable to one, turning off the optical transmitter.

139.5.7 PMD fault function (optional)

If the PMD has detected a local fault on the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

139.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

139.5.9 PMD receive fault function (optional)

If the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

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139.6 PMD to MDI optical specifications for 50GBASE-FR and 50GBASE-LR

The operating ranges for the 50GBASE-FR and 50GBASE-LR PMDs are defined in Table 139–5. A 50GBASE-FR or 50GBASE-LR compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 139–13. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 50GBASE-FR PMD operating at 2.5 km meets the operating range requirement of 2 m to 2 km). The 50GBASE-LR PMD interoperates with the 50GBASE-FR PMD provided that the channel requirements for 50GBASE-FR are met.

Table 139–5—50GBASE-FR and 50GBASE-LR operating ranges

PMD type	Required operating range
50GBASE-FR	2 m to 2 km
50GBASE-LR	2 m to 10 km

139.6.1 50GBASE-FR and 50GBASE-LR transmitter optical specifications

The 50GBASE-FR transmitter shall meet the specifications defined in Table 139–6 per the definitions in 139.7. The 50GBASE-LR transmitter shall meet the specifications defined in Table 139–6 per the definitions in 139.7.

Table 139–6—50GBASE-FR and 50GBASE-LR transmit characteristics

Description	50GBASE-FR	50GBASE-LR	Unit
Signaling rate (range)	26.5625 ± 100 ppm		GBd
Modulation format	PAM4		—
Wavelengths (range)	1304.5 to 1317.5		nm
Side-mode suppression ratio (SMSR), (min)	30		dB
Total average launch power (max)	3	4.2	dBm
Average launch power[a] (min)	–5	–4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (max)	2.8	4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (min)[b]	–2	–1	dBm
Launch power in OMA_{outer} minus TDECQ (min)	–3	–2	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ) (max)	2.3	2.5	dB
Average launch power of OFF transmitter (max)	–20		dBm
Extinction ratio (min)	4.5		dB
$RIN_{16.5}OMA$ (max)	–136	—	dB/Hz
$RIN_{15.1}OMA$ (max)	—	–136	dB/Hz
Optical return loss tolerance (max)	16.5	15.1	dB
Transmitter reflectance[c] (max)	–26		dB

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[a]Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Even if the TDECQ < 1 dB, the OMA_{outer} (min) must exceed this value.
[c]Transmitter reflectance is defined looking into the transmitter.

139.6.2 50GBASE-FR and 50GBASE-LR receive optical specifications

The 50GBASE-FR receiver shall meet the specifications defined in Table 139–7 per the definitions in 139.7.
The 50GBASE-LR receiver shall meet the specifications defined in Table 139–7 per the definitions in 139.7.

Table 139–7—50GBASE-FR and 50GBASE-LR receive characteristics

Description	50GBASE-FR	50GBASE-LR	Unit
Signaling rate (range)	26.5625 ± 100 ppm		GBd
Modulation format	PAM4		—
Wavelengths (range)	1304.5 to 1317.5		nm
Damage threshold[a]	5.2	5.2	dBm
Average receive power (max)	3	4.2	dBm
Average receive power[b] (min)	–9	–10.3	dBm
Receive power (OMA_{outer}) (max)	2.8	4	dBm
Receiver reflectance (max)	–26		dB
Receiver sensitivity (OMA_{outer})[c] (max)	–7.3	–8.8	dBm
Stressed receiver sensitivity (OMA_{outer})[d] (max)	–5	–6.3	dBm
Conditions of stressed receiver sensitivity test:[e]			
Stressed eye closure for PAM4 (SECQ)	2.3	2.5	dB

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b]Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity (OMA_{outer}) (max) is informative.
[d]Measured with conformance test signal at TP3 (see 139.7.9) for the BER specified in 139.1.1.
[e]These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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139.6.3 50GBASE-FR and 50GBASE-LR illustrative link power budgets

Illustrative power budgets and penalties for 50GBASE-FR and 50GBASE-LR channels are shown in Table 139–8.

Table 139–8—50GBASE-FR and 50GBASE-LR illustrative link power budgets

Parameter	50GBASE-FR	50GBASE-LR	Unit
Power budget (for maximum TDECQ)	6.6	9.3	dB
Operating distance	2	10	km
Channel insertion loss	4[a]	6.3[b]	dB
Maximum discrete reflectance	See 139.10.2.2	See 139.10.2.2	dB
Allocation for penalties[c] (for maximum TDECQ)	2.6	3	dB
Additional insertion loss allowed	0	0	dB

[a]The channel insertion loss is calculated using the maximum distance specified in Table 139–5 for 50GBASE-FR and fiber attenuation of 0.5 dB/km plus an allocation for connection and splice loss given in 139.10.2.1.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 139–5 for 50GBASE-LR and fiber attenuation of 0.43 dB/km at 1295 nm plus an allocation for connection and splice loss given in 139.10.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

139.7 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

139.7.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 139–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 139–10 may be used to perform that test. The test patterns used in this clause are shown in Table 139–9.

Table 139–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.6
3	PRBS31Q	120.5.11.2.4
4	PRBS13Q	120.5.11.2.3
5	Scrambled idle	82.2.11
6	SSPRQ	120.5.11.2.5

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Table 139–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 50GBASE-R signal	139.7.2
Side mode suppression ratio	3, 5, 6 or valid 50GBASE-R signal	—
Average optical power	3, 5, 6 or valid 50GBASE-R signal	139.7.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	139.7.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	139.7.5
Extinction ratio	4 or 6	139.7.6
$RIN_{15.1}OMA$ and $RIN_{16.5}OMA$	Square wave	139.7.7
Stressed receiver conformance test signal calibration	6	139.7.9.2
Stressed receiver sensitivity	3 or 5	139.7.9

139.7.2 Wavelength

The wavelength shall be within the ranges given in Table 139–6 for 50GBASE-FR and 50GBASE-LR, if measured per TIA/EIA-455-127-A or IEC 61280-1-3. The transmitter is modulated using the test pattern defined in Table 139–10.

139.7.3 Average optical power

The average optical power shall be within the limits given in Table 139–6 for 50GBASE-FR and 50GBASE-LR if measured using the methods given in IEC 61280-1-1.

139.7.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} shall be within the limits given in Table 139–6 for 50GBASE-FR and 50GBASE-LR if measured using a test pattern specified for extinction ratio in Table 139–10. The OMA_{outer} is defined as the difference between the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 139–3.

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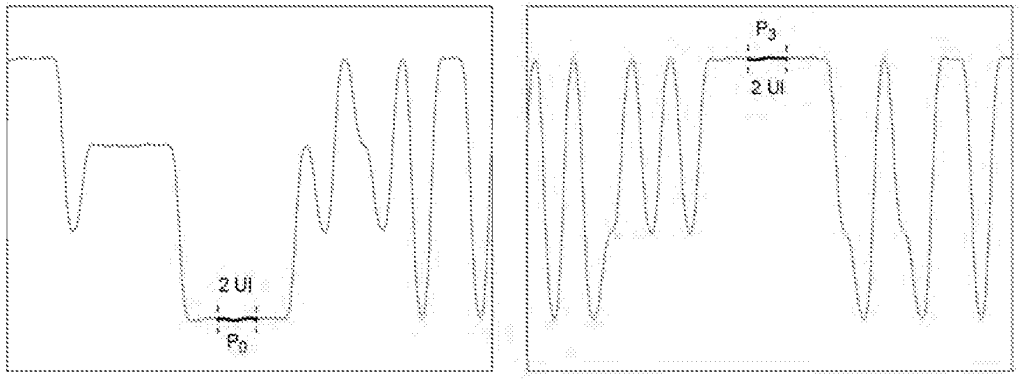


Figure 139–3—Example power levels P_0 and P_3 from PRBS13Q test pattern

139.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

The TDECQ shall be within the limits given in Table 139–6 for 50GBASE-FR and 50GBASE-LR if measured using the methods specified in 139.7.5.1, 139.7.5.2, and 139.7.5.3.

TDECQ is a measure of each optical transmitter's vertical eye closure when transmitted through a worst case optical channel (specified in 139.7.5.2), as measured through an optical to electrical converter (O/E) with a bandwidth equivalent to a reference receiver, and equalized with the reference equalizer (as described in 139.7.5.4). The reference receiver and equalizer may be implemented in software or may be part of the oscilloscope.

Table 139–10 specifies the test patterns to be used for measurement of TDECQ.

139.7.5.1 TDECQ conformance test setup

A block diagram for the TDECQ conformance test is shown in Figure 139–4. Other equivalent measurement implementations may be used with suitable calibration.

The optical splitter and variable reflector are adjusted so that each transmitter is tested with the optical return loss specified in Table 139–11. The state of polarization of the back reflection is adjusted to create the greatest RIN. The signal is tested with the optical channel described in 139.7.5.2. The combination of the O/E and the oscilloscope has a fourth-order Bessel-Thomson filter response with a bandwidth of 19.34 GHz. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The test pattern (specified in Table 139–11) is transmitted repetitively and the oscilloscope is set up to capture the complete pattern for TDECQ analysis as described in 139.7.5.3. The clock recovery unit (CRU) has a corner frequency of 4 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology.

139.7.5.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 139–11.

A 50GBASE-FR or 50GBASE-LR transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in

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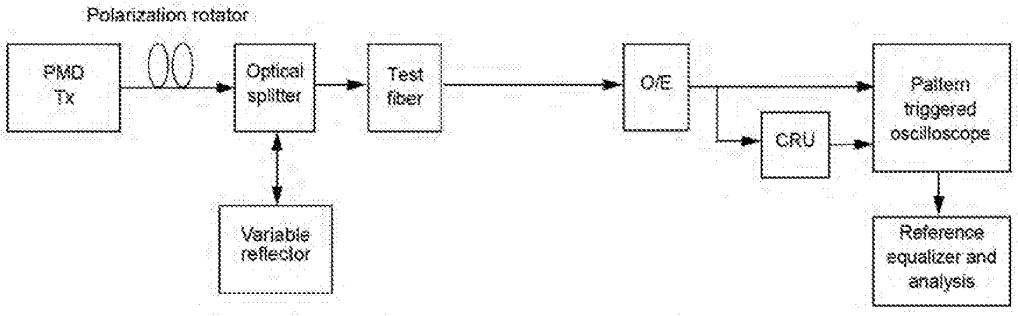


Figure 139–4—TDECQ conformance test block diagram

Table 139–11—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]	Max mean DGD
	Minimum	Maximum			
50GBASE-FR	$0.0465 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.0465 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	17.8 dB	0.8 ps
50GBASE-LR	$0.2325 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.2325 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	15.7 dB	0.8 ps

[a]The dispersion is measured for the wavelength of the device under test (λ in nm). The coefficient assumes 2 km for 50GBASE-FR and 10 km for 50GBASE-LR.
[b]There is no intent to stress the sensitivity of the O/E converter associated with the oscilloscope.
[c]The optical return loss is applied at TP2.

Table 139–11 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 139–11. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than the value specified in Table 139–11.

139.7.5.3 TDECQ measurement method

TDECQ for 50GBASE-FR and 50GBASE-LR is measured as described in 121.8.5.3 with the exception that the reference equalizer is as specified in 139.7.5.4.

139.7.5.4 TDECQ reference equalizer

The reference equalizer for 50GBASE-FR and 50GBASE-LR is a 5 tap, T/2 spaced, feed-forward equalizer (FFE), where T is the symbol period.

NOTE—This reference equalizer is part of the TDECQ test and does not imply any particular receiver equalizer implementation.

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139.7.6 Extinction ratio

The extinction ratio shall be within the limits given in Table 139–6 for 50GBASE-FR and 50GBASE-LR if measured using a test pattern specified for extinction ratio in Table 139–10. The extinction ratio of a PAM4 optical signal is defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 139–3.

139.7.7 Relative intensity noise ($RIN_{16.5}OMA$ and $RIN_{15.1}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 16.5 dB for 50GBASE-FR and 15.1 dB for 50GBASE-LR.
b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 26.6 GHz).
c) The test pattern is according to Table 139–10.

139.7.8 Receiver sensitivity

Receiver sensitivity, which is defined for an ideal input signal, is informative and compliance is not required. If measured, the test signal should have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter and RIN. Instead, the normative requirement for receivers is stressed receiver sensitivity.

139.7.9 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 139–7 for 50GBASE-FR and 50GBASE-LR if measured using the method defined in 139.7.9.1 and 139.7.9.3, with the conformance test signal at TP3 as described in 139.7.9.2, using the test pattern specified for SRS in Table 139–10.

Any of the patterns specified for SRS in Table 139–10 is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

139.7.9.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 139–5. The patterns used for the received conformance signal are specified in Table 139–10. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 139.7.9.2 and has sinusoidal jitter applied as specified in 121.8.9.4. A suitable test set is needed to characterize the signal used to test the receiver. Stressed receiver conformance test signal verification is described in 139.7.9.3.

The low-pass filter is used to create ISI. The combination of the low-pass filter and the E/O converter should have a frequency response that results in at least half of the dB value of the stressed eye closure (SECQ) specified in Table 139–7 for 50GBASE-FR and 50GBASE-LR before the sinusoidal and Gaussian noise terms are added, according to the methods specified in 139.7.9.2. The sinusoidal amplitude interferer causes additional eye closure, but in conjunction with the finite edge rates, also causes some jitter.

The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferer may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferer, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferer, and the low-pass filter are adjusted so that the SECQ specified in Table 139–7 is met, according to the methods specified in 139.7.9.2.

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For improved visibility for calibration, all elements in the signal path (cables, DC blocks, E/O converter, etc.) should have wide and smooth frequency response, and linear phase response, throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be minimized.

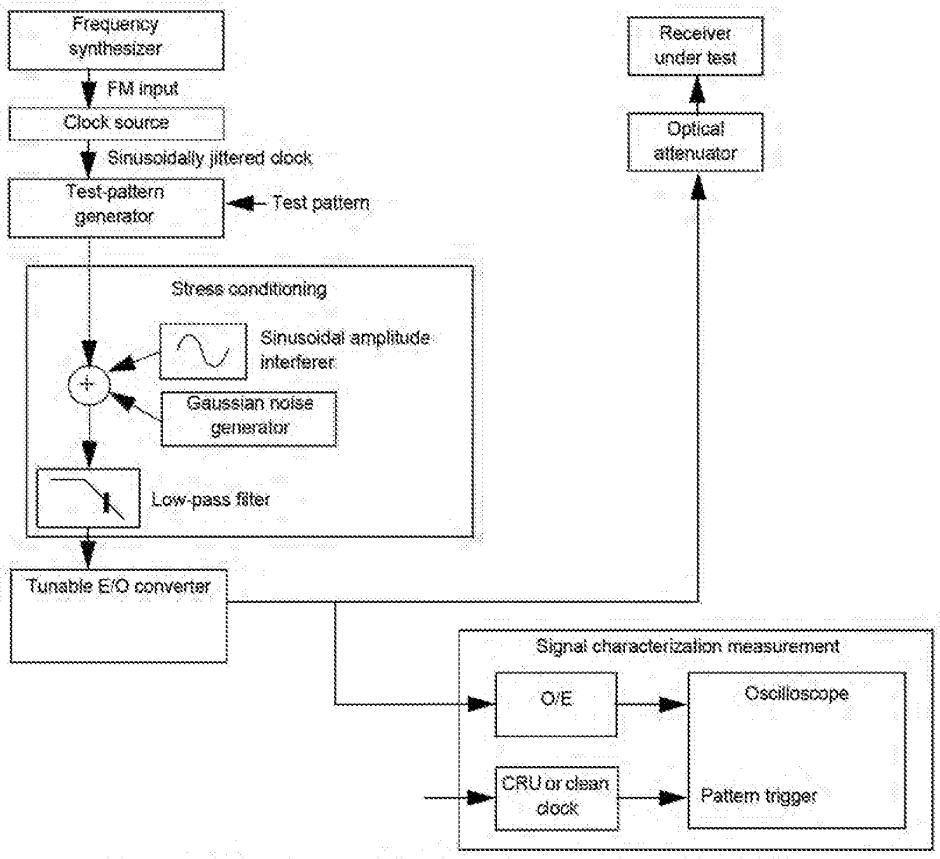


Figure 139–5—Stressed receiver conformance test block diagram

139.7.9.2 Stressed receiver conformance test signal characteristics and calibration

The stressed receiver conformance test signal characteristics and calibration methods are as described in 121.8.9.2 with the following exceptions:

- The SECQ of the stressed receiver conformance test signal is measured according to 139.7.5, except that the test fiber is not used.
- An example stressed receiver conformance test setup is shown in Figure 139–5; however, alternative test setups that generate equivalent stress conditions may be used.
- The signaling rate of the test pattern generator and the extinction ratio of the E/O converter are as given in Table 139–6 for 50GBASE-FR and 50GBASE-LR.
- The required values of the "Stressed receiver sensitivity (OMA_{outer}) (max)" and "Stressed eye closure for PAM4 (SECQ)" are as given in Table 139–7 for 50GBASE-FR and 50GBASE-LR.

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139.7.9.3 Stressed receiver conformance test signal verification

The SECQ of the stressed receiver conformance test signal is measured according to 139.7.5, except that the test fiber is not used. The clock output from the clock source in Figure 139–5 is modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye jitter that includes the sinusoidal jitter component, a separate clock source (clean clock of Figure 139–5) is required that is synchronized to the source clock, but not modulated with the jitter source.

Care should be taken when characterizing the test signal because excessive noise/jitter in the measurement system would result in an input signal that does not fully stress the receiver under test. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. Care should be taken to minimize the noise/jitter introduced by the O/E, filters, and oscilloscope and/or to correct for this noise. While the details of test equipment are beyond the scope of this standard, it is recommended that the implementer fully characterize the test equipment and apply appropriate guard bands to ensure that the stressed receiver conformance input signal meets the stress and sinusoidal jitter specified in 139.7.9.2 and 121.8.9.4.

139.8 Safety, installation, environment, and labeling

139.8.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1.

139.8.2 Laser safety

50GBASE-FR and 50GBASE-LR optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[13]

139.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

139.8.4 Environment

Normative specifications in this clause shall be met by a system integrating a 50GBASE-FR or 50GBASE-LR PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

---

[13] A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

139.8.5 Electromagnetic emission

A system integrating a 50GBASE-FR or 50GBASE-LR PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

139.8.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

139.8.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 50GBASE-FR).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 139.8.2.

139.9 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 139–6.

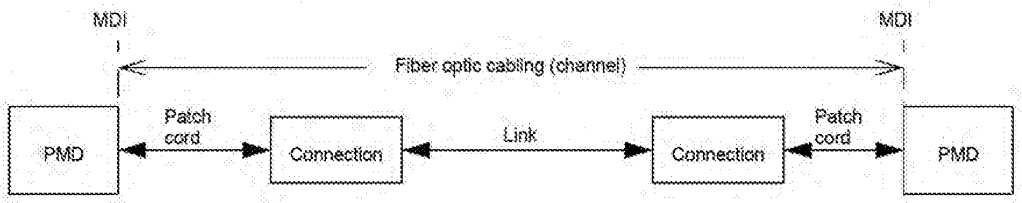


Figure 139–6—Fiber optic cabling model

The channel insertion loss is given in Table 139–12. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with ANSI/TIA/EIA-526-7/method A-1. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

139.10 Characteristics of the fiber optic cabling (channel)

The 50GBASE-FR and 50GBASE-LR fiber optic cabling shall meet the specifications defined in Table 139–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

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Table 139–12—Fiber optic cabling (channel) characteristics

Description	50GBASE-FR	50GBASE-LR	Unit
Operating distance (max)	2	10	km
Channel insertion loss[a, b] (max)	4	6.3	dB
Channel insertion loss (min)	0	0	dB
Positive dispersion[b] (max)	3.2	16	ps/nm
Negative dispersion[b] (min)	–3.7	–18.6	ps/nm
DGD_max[c]	3	8	ps
Optical return loss (min)	25	22	dB

[a]These channel insertion loss values include cable, connectors, and splices.
[b]Over the wavelength range 1304.5 nm to 1317.5 nm for 50GBASE-FR and 50GBASE-LR.
[c]Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system must tolerate.

139.10.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion unshifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 139–13 where they differ.

Table 139–13—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.43[a] or 0.5[b]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a]The 0.43 dB/km at 1304.5 nm attenuation for optical fiber cables is derived from Appendix I of ITU-T G.695.
[b]The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3. Using 0.5 dB/km may not support operation 10 km for 50GBASE-LR.

139.10.2 Optical fiber connection

An optical fiber connection, as shown in Figure 139–6, consists of a mated pair of optical connectors.

139.10.2.1 Connection insertion loss

The maximum link distance for 50GBASE-LR is based on an allocation of 2 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. The maximum link distance for 50GBASE-FR is based on an allocation of 3 dB total connection and splice loss. Connections with different loss characteristics may be used provided the requirements of Table 139–12 are met.

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139.10.2.2 Maximum discrete reflectance

The maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 139–14 corresponding to the number of discrete reflectances above –55 dB within the channel. For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

Table 139–14—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance	
	50GBASE-FR	50GBASE-LR
1	–25 dB	–22 dB
2	–31 dB	–29 dB
4	–35 dB	–33 dB
6	–38 dB	–35 dB
8	–39 dB	–37 dB
10	–40 dB	–38 dB

139.10.3 Medium Dependent Interface (MDI) requirements

The 50GBASE-FR or 400GBASE-LR PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 139–6). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 139.5.1, not at the MDI.

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139.11 Protocol implementation conformance statement (PICS) proforma for Clause 139, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR[14]

139.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 139, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

139.11.2 Identification

139.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

139.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Clause 139, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

[14] *Copyright release for PICS proformas:* Users of this standard *may* freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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139.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*FR	50GBASE-FR PMD	139.6	Device supports requirements for 50GBASE-FR PHY	O.1	Yes [ ] No [ ]
*LR	50GBASE-LR PMD	139.6	Device supports requirements for 50GBASE-LR PHY	O.1	Yes [ ] No [ ]
*INS	Installation / cable	139.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	139.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	139.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	139.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	139.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	139.4	Registers and interface supported	O	Yes [ ] No [ ]

139.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR

139.11.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 50GBASE-R PCS and PMA	139.1		M	Yes [ ]
F2	Integration with management functions	139.1		O	Yes [ ] No [ ]
F3	Bit error ratio	139.1.1	Meets the BER specified in 139.1.1	M	Yes [ ]
F4	Transmit function	139.5.2	Conveys symbols from PMD service interface to MDI	M	Yes [ ]
F6	Mapping between optical signal and logical signal for transmitter	139.5.2	Highest optical power corresponds to tx_symbol = three	M	Yes [ ]
F7	Receive function	139.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F8	Conversion of optical signal to electrical signal	139.5.3	For delivery to the PMD service interface	M	Yes [ ]
F9	Mapping between optical signal and logical signal for receiver	139.5.3	Highest optical power corresponds to rx_symbol = three	M	Yes [ ]
F10	Global Signal Detect function	139.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F11	Global Signal Detect behavior	139.5.4	SIGNAL_DETECT is a global indicator of the presence of an optical signal	M	Yes [ ]
F12	PMD reset function	139.5.5	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

139.11.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	139.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	139.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD_fault function	139.5.7	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD_transmit_fault function	139.5.8	Sets PMD_transmit_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_receive_fault function	139.5.9	Sets PMD_receive_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]

139.11.4.3 PMD to MDI optical specifications for 50GBASE-FR

Item	Feature	Subclause	Value/Comment	Status	Support
FRF1	Transmitter meets specifications in Table 139–6	139.6.1	Per definitions in 139.7	FR:M	Yes [ ] N/A [ ]
FRF2	Receiver meets specifications in Table 139–7	139.6.2	Per definitions in 139.7	FR:M	Yes [ ] N/A [ ]

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139.11.4.4 PMD to MDI optical specifications for 50GBASE-LR

Item	Feature	Subclause	Value/Comment	Status	Support
LRF1	Transmitter meets specifications in Table 139–6	139.6.1	Per definitions in 139.7	LR:M	Yes [ ] N/A [ ]
LRF2	Receiver meets specifications in Table 139–7	139.6.2	Per definitions in 139.7	LR:M	Yes [ ] N/A [ ]

139.11.4.5 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	139.7	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength	139.7.2	Per TIA/EIA-455-127-A or IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	139.7.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA measurements	139.7.4		M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	139.7.5		M	Yes [ ]
OM6	Extinction ratio	139.7.6		M	Yes [ ]
OM7	RIN_{xx}OMA measurement procedure	139.7.7		M	Yes [ ]
OM8	Stressed receiver sensitivity	139.7.9		M	Yes [ ]

139.11.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	139.8.1	Conforms to IEC 60950-1	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	139.8.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	139.8.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

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139.11.4.7 Characteristics of the fiber optic cabling and MD

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	139.10	Meets requirements specified in Table 139–12	INS:M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	139.10.2.2	Meets requirements specified in Table 139–14	INS:M	Yes [ ] N/A [ ]
OC3	MDI requirements	139.10.3	Meets IEC 61753-1-1 and IEC 61753-021-2	INS:M	Yes [ ] N/A [ ]

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140. Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR

140.1 Overview

This clause specifies the 100GBASE-DR PMD together with the single-mode fiber medium. The optical signal generated by this PMD type is modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 140–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 140–1—Physical Layer clauses associated with the 100GBASE-DR PMD

Associated clause	100GBASE-DR
81—RS	Required
81—100GMII[a]	Optional
82—PCS	Required
83—100GBASE-R PMA	Optional
91—RS-FEC	Required
83A—CAUI-10 C2C	Optional
83B—CAUI-10 C2M	Optional
83D—CAUI-4 C2C	Optional
83E—CAUI-4C2M	Optional
135—100GBASE-P PMA	Required
135D—100GAUI-4 C2C	Optional
135E—100GAUI-4 C2M	Optional
135F—100GAUI-2 C2C	Optional
135G—100GAUI-2 C2M	Optional
78—Energy Efficient Ethernet	Optional

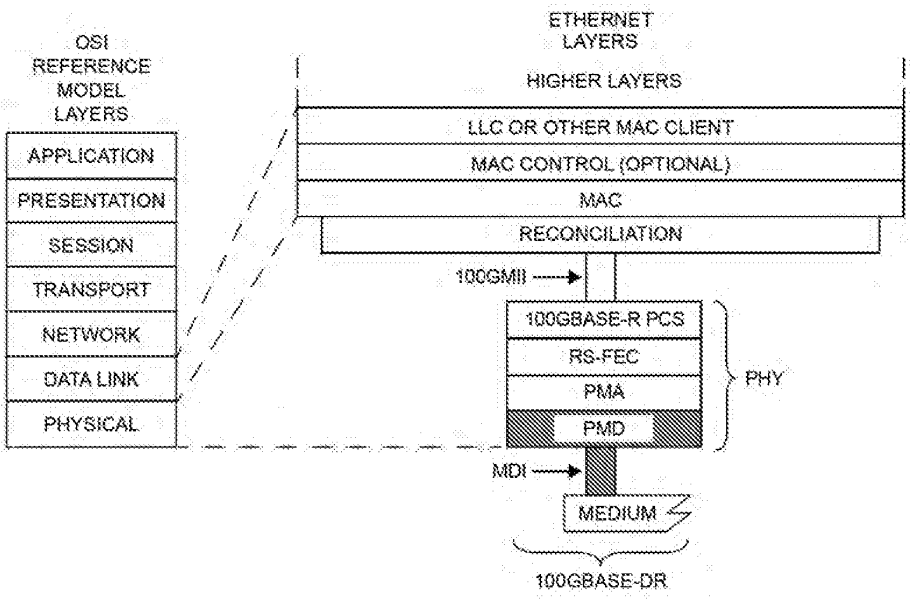
[a]The 100GMII is an optional interface. However, if the 100GMII is not implemented, a conforming implementation must behave functionally as though the RS and 100GMII were present.

Figure 140–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 100 Gigabit Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2.

100GBASE-DR PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

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100GMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
DR = PMD FOR SINGLE-MODE FIBER — 500 m

Figure 140–1—100GBASE-DR PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

140.1.1 Bit error ratio

The bit error ratio (BER) when processed by the PMA (Clause 135) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.223) of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 91) and PCS (Clause 82). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-10} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap.

140.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-DR PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

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The 100GBASE-DR PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with a single symbol stream (n = 1).

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_0.request
PMD:IS_UNITDATA_0.indication
PMD:IS_SIGNAL.indication

In the transmit direction, the PMA continuously sends one stream of PAM4 symbols to the PMD using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.6525 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends one stream of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.6525 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 140.5.4. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_bit parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 140.1.1.

140.3 Delay and Skew

140.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 100GBASE-DR PMD including 2 m of fiber in one direction shall be no more than 2 048 bit times (4 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

140.3.2 Skew constraints

The Skew (relative delay) between the FEC lanes must be kept within limits so that the information on the FEC lanes can be reassembled by the FEC. The Skew Variation must also be limited to ensure that a given FEC lane always traverses the same physical lane. Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

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For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2.

140.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 140–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 140–3.

Table 140–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable

Table 140–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect

140.5 PMD functional specifications

The 100GBASE-DR PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

140.5.1 PMD block diagram

The PMD block diagram is shown in Figure 140–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 140.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 140.10.3). Unless specified otherwise, all receiver measurements and tests defined in 140.7 are made at TP3.

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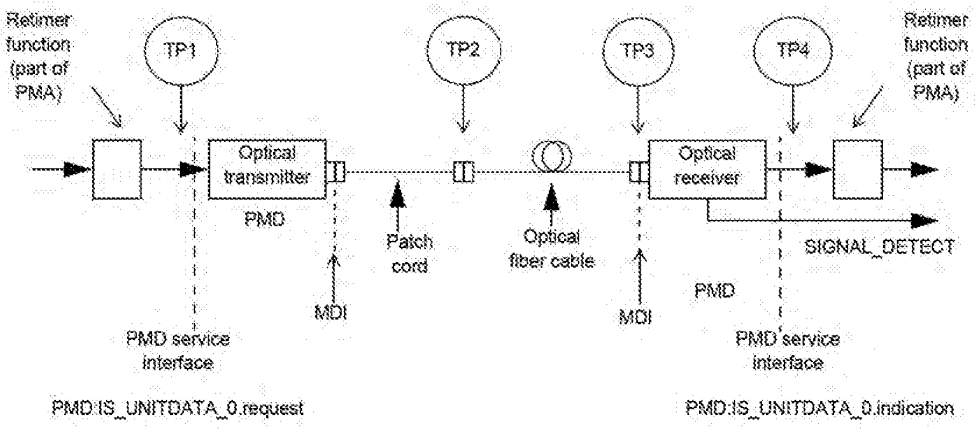


Figure 140–2—Block diagram for 100GBASE-DR transmit/receive paths

140.5.2 PMD transmit function

The PMD Transmit function shall convert the symbol stream requested by the PMD service interface messages PMD:IS_UNITDATA_0.request into an optical signal stream. The optical signal stream shall then be delivered to the MDI, according to the transmit optical specifications in this clause. The highest optical power level in the signal stream shall correspond to tx_symbol = three and the lowest shall correspond to tx_symbol = zero.

140.5.3 PMD receive function

The PMD receive function shall convert the optical signal stream received from the MDI into a symbol stream for delivery to the PMD service interface using the message PMD:IS_UNITDATA_0.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_symbol = three and the lowest shall correspond to rx_symbol = zero.

140.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 131.3.

SIGNAL_DETECT shall be a global indicator of the presence of the optical signal. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 140–4. The PMD receiver is not required to verify whether a compliant 100GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

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Table 140–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Average optical power at TP3 ≤ –20 dBm	FAIL
[(Optical power at TP3 ≥ average receive power (min) Table 140–7) AND (compliant 100GBASE–R signal input)]	OK
All other conditions	Unspecified

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

140.5.5 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

140.5.6 PMD global transmit disable function (optional)

The PMD_global_transmit_disable function is optional and allows the optical transmitter to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of the OFF transmitter in Table 140–6.
b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable to one, turning off the optical transmitter.

140.5.7 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

140.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

140.5.9 PMD receive fault function (optional)

If the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

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140.6 PMD to MDI optical specifications for 100GBASE-DR

The operating range for the 100GBASE-DR PMD is defined in Table 140–5. A 100GBASE-DR compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 140–12. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 100GBASE-DR PMD operating at 600 m meets the operating range requirement of 2 m to 500 m).

Table 140–5—100GBASE-DR operating range

PMD type	Required operating range
100GBASE-DR	2 m to 500 m

140.6.1 100GBASE-DR transmitter optical specifications

The 100GBASE-DR transmitter shall meet the specifications defined in Table 140–6 per the definitions in 140.7.

Table 140–6—100GBASE-DR transmit characteristics

Description	Value	Unit
Signaling rate (range)	53.125 ± 100 ppm	GBd
Modulation format	PAM4	—
Wavelength (range)	1304.5 to 1317.5	nm
Side-mode suppression ratio (SMSR), (min)	30	dB
Average launch power (max)	4	dBm
Average launch power[a] (min)	–2.3	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (max)	4.2	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (min)[b]	–0.2	dBm
Launch power in OMA_{outer} minus TDECQ (min)	–1.2	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ) (max)	2.5	dB
Average launch power of OFF transmitter (max)	–20	dBm
Extinction ratio (min)	5	dB
$RIN_{21.4}OMA$ (max)	–142	dB/Hz
Optical return loss tolerance (max)	21.4	dB
Transmitter reflectance[c] (max)	–26	dB

[a]Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Even if the TDECQ < 1 dB, the OMA_{outer} (min) must exceed these values.
[c]Transmitter reflectance is defined looking into the transmitter.

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140.6.2 100GBASE-DR receive optical specifications

The 100GBASE-DR receiver shall meet the specifications defined in Table 140–7 per the definitions in 140.7.

Table 140–7—100GBASE-DR receive characteristics

Description	Value	Unit
Signaling rate (range)	53.125 ± 100 ppm	GBd
Modulation format	PAM4	—
Wavelengths (range)	1304.5 to 1317.5	nm
Damage threshold[a]	6.5	dBm
Average receive power (max)	4	dBm
Average receive power[b] (min)	–5.3	dBm
Receive power (OMA_{outer}) (max)	4.2	dBm
Receiver reflectance (max)	–26	dB
Receiver sensitivity (OMA_{outer})[c] (max)	–4.5	dBm
Stressed receiver sensitivity (OMA_{outer})[d] (max)	–2	dBm
Conditions of stressed receiver sensitivity test:[e]		
Stressed eye closure for PAM4 (SECQ)	2.5	dB

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
[b]Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity (OMA_{outer}) (max) is informative.
[d]Measured with conformance test signal at TP3 (see 140.7.9) for the BER specified in 140.1.1.
[e]These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

140.6.3 100GBASE-DR illustrative link power budget

An illustrative power budget and penalties for 100GBASE-DR channels are shown in Table 140–8.

Table 140–8—100GBASE-DR illustrative link power budget

Parameter	Value	Unit
Power budget (for max TDECQ)	5.8	dB
Operating distance	500	m
Channel insertion loss[a]	3	dB
Maximum discrete reflectance	See 140.10.2.2	dB
Allocation for penalties[b] (for max TDECQ)	2.8	dB
Additional insertion loss allowed	0	dB

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[a]The channel insertion loss is calculated using the maximum distance specified in Table 140–5 and cabled optical fiber attenuation of 0.5 dB/km at 1304.5 nm plus an allocation for connection and splice loss given in 140.10.2.1.
[b]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

140.7 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

140.7.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 140–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 140–10 may be used to perform that test. The test patterns used in this clause are shown in Table 140–9.

Table 140–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.6
3	PRBS31Q	120.5.11.2.4
4	PRBS13Q	120.5.11.2.3
5	Scrambled idle	119.2.4.9
6	SSPRQ	120.5.11.2.5

Table 140–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 50GBASE-R signal	140.7.2
Side mode suppression ratio	3, 5, 6 or valid 50GBASE-R signal	—
Average optical power	3, 5, 6 or valid 50GBASE-R signal	140.7.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	140.7.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	140.7.5
Extinction ratio	4 or 6	140.7.6
$RIN_{21.4}OMA$	4	140.7.7
Stressed receiver conformance test signal calibration	6	140.7.9
Stressed receiver sensitivity	3 or 5	140.7.9

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140.7.2 Wavelength

The wavelength shall be within the range given in Table 140–6 if measured per TIA/EIA-455-127-A or IEC 61280-1-3. The transmitter is modulated using the test pattern defined in Table 140–10.

140.7.3 Average optical power

The average optical power shall be within the limits given in Table 140–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern defined in Table 140–10, per the test setup in Figure 53–6.

140.7.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} shall be within the limits given in Table 140–6 if measured using a test pattern specified for extinction ratio in Table 140–10. The OMA_{outer} is defined as the difference between the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 140–3.

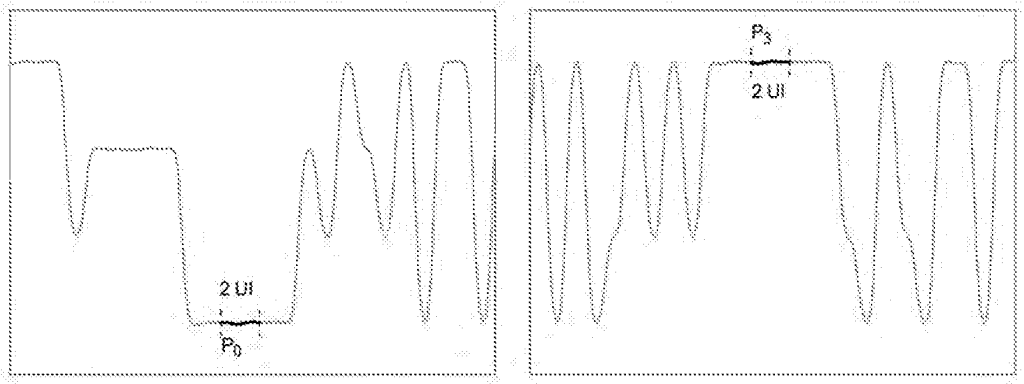


Figure 140–3—Example power levels P_0 and P_3 from PRBS13Q test pattern

140.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

The TDECQ shall be within the limits given in Table 140–6 if measured using the methods specified in 121.8.5.1, 121.8.5.2, and 121.8.5.3 using a reference equalizer as described in 121.8.5.4, with the following exceptions:

- The signaling rate of the test pattern generator is as given in Table 140–6.
- There are no interfering optical lanes and therefore the delay requirement of at least 31 UI between test pattern on one lane and any other lane, as specified in 121.8.5.1, is redundant.
- The combination of the O/E converter and the oscilloscope has a fourth-order Bessel-Thomson filter response with a bandwidth of 38.68 GHz.

140.7.6 Extinction ratio

The extinction ratio shall be within the limits given in Table 140–6 if measured using a test pattern specified for extinction ratio in Table 140–10. The extinction ratio of a PAM4 optical signal is defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 140–3.

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140.7.7 Relative intensity noise (RIN$_{21.4}$OMA)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 21.4 dB.
b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 53.2 GHz).

140.7.8 Receiver sensitivity

Receiver sensitivity, which is defined for an ideal input signal, is informative and compliance is not required. If measured, the test signal should have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter and RIN. Instead, the normative requirement for receivers is stressed receiver sensitivity.

140.7.9 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 140–7 if measured using the method defined in 121.8.9 with the following exceptions:

— The SECQ of the stressed receiver conformance test signal is measured according to 140.7.5, except that the test fiber is not used.
— The signaling rate of the test pattern generator and the extinction ratio of the E/O converter are as given in Table 140–6.
— The required values of the "Stressed receiver sensitivity (OMA_{outer}) (max)" and "Stressed eye closure for PAM4 (SECQ)" are as given in Table 140–7.

140.8 Safety, installation, environment, and labeling

140.8.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1.

140.8.2 Laser safety

100GBASE-DR optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[15]

140.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

[15]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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140.8.4 Environment

Normative specifications in this clause shall be met by a system integrating a 100GBASE-DR PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

140.8.5 Electromagnetic emission

A system integrating a 100GBASE-DR PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

140.8.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

140.8.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 100GBASE-DR).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 140.8.2.

140.9 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 140–4.

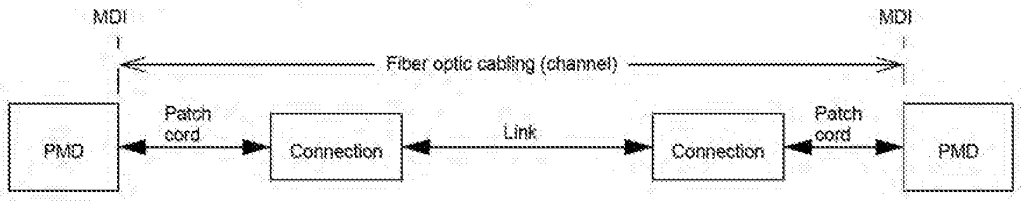


Figure 140–4—Fiber optic cabling model

The channel insertion loss is given in Table 140–11. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with ANSI/TIA/EIA-526-7/method A-1. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

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Table 140–11—Fiber optic cabling (channel) characteristics

Description	100GBASE-DR	Unit
Operating distance (max)	500	m
Channel insertion loss[a, b] (max)	3	dB
Channel insertion loss (min)	0	dB
Positive dispersion[b] (max)	0.8	ps/nm
Negative dispersion[b] (min)	–0.93	ps/nm
DGD_max[c]	2.24	ps
Optical return loss (min)	37	dB

[a]These channel insertion loss values include cable, connectors, and splices.
[b]Over the wavelength range 1304.5 nm to 1317.5 nm
[c]Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system must tolerate.

140.10 Characteristics of the fiber optic cabling (channel)

The 100GBASE-DR fiber optic cabling shall meet the specifications defined in Table 140–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

140.10.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion unshifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 140–12 where they differ.

Table 140–12—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.5[a]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a]The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3.

140.10.2 Optical fiber connection

An optical fiber connection, as shown in Figure 140–4, consists of a mated pair of optical connectors.

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140.10.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 2.75 dB total connection and splice loss. For example, this allocation supports five connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 140–11 are met.

140.10.2.2 Maximum discrete reflectance

The maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 140–13 corresponding to the number of discrete reflectances above –55 dB within the channel. For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

Table 140–13—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance
	100GBASE-DR
1	–37 dB
2	–42 dB
4	–45 dB
6	–47 dB
8	–48 dB
10	–49 dB

140.10.3 Medium Dependent Interface (MDI)

The 100GBASE-DR PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 140–4). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 140.5.1, not at the MDI.

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140.11 Protocol implementation conformance statement (PICS) proforma for Clause 140, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR[16]

140.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 140, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

140.11.2 Identification

140.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

140.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Clause 140, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

[16] *Copyright release for PICS proformas:* Users of this standard *may* freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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140.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*INS	Installation / cable	140.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	140.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	140.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	140.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	140.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	140.4	Registers and interface supported	O	Yes [ ] No [ ]

140.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR

140.11.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 100GBASE-R PCS and PMA	140.1		M	Yes [ ]
F2	Integration with management functions	140.1		O	Yes [ ] No [ ]
F3	Bit error ratio	140.1.1	Meets the BER specified in 140.1.1	M	Yes [ ]
F4	Transmit function	140.5.2	Conveys symbols from PMD service interface to MDI	M	Yes [ ]
F5	Mapping between optical signal and logical signal for transmitter	140.5.2	Highest optical power corresponds to tx_symbol = three	M	Yes [ ]
F6	Receive function	140.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F7	Conversion of optical signal to electrical signal	140.5.3	For delivery to the PMD service interface	M	Yes [ ]
F8	Mapping between optical signal and logical signal for receiver	140.5.3	Highest optical power corresponds to rx_symbol = three	M	Yes [ ]
F9	Global Signal Detect function	140.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	140.5.4	SIGNAL_DETECT is a global indicator of the presence of an optical signal	M	Yes [ ]
F11	PMD reset function	140.5.5	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

140.11.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	140.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	140.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD_fault function	140.5.7	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD_transmit_fault function	140.5.8	Sets PMD_transmit_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_receive_fault function	140.5.9	Sets PMD_receive_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]

140.11.4.3 PMD to MDI optical specifications for 100GBASE-DR

Item	Feature	Subclause	Value/Comment	Status	Support
DR1	Transmitter meets specifications in Table 140–6	140.6.1	Per definitions in 140.7	M	Yes [ ]
DR2	Receiver meets specifications in Table 140–7	140.6.2	Per definitions in 140.7	M	Yes [ ]

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140.11.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	140.7	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength	140.7.2	Per TIA/EIA-455-127-A or IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	140.7.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA measurements	140.7.4		M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	140.7.5		M	Yes [ ]
OM6	Extinction ratio	140.7.6		M	Yes [ ]
OM7	Stressed receiver sensitivity	140.7.9		M	Yes [ ]

140.11.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	140.8.1	Conforms to IEC 60950-1	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	140.8.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	140.8.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

140.11.4.6 Characteristics of the fiber optic cabling and MD

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	140.10	Meets requirements specified in Table 124–11	INS:M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	140.10.2.2	Meets requirements specified in Table 140–13	INS:M	Yes [ ] N/A [ ]

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NOTE—This annex is numbered in correspondence to its associated clause; i.e., Annex 4A corresponds to Clause 4.

Annex 4A

(normative)

Simplified full duplex media access control

4A.4 Specific implementations

4A.4.2 MAC parameters

Change Table 4–2 (as modified by IEEE Std 802.3bs-201x) as follows:

NOTE 4—For 40 Gb/s, 50 Gb/s, 100 Gb/s 200 Gb/s, and 400 Gb/s operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, 50GMII, CGMII, 200GMII, or 400GMII receive signals at the DTE due to clock tolerance and lane alignment requirements.

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Annex 31B

(normative)

MAC Control PAUSE operation

31B.3 Detailed specification of PAUSE operation

31B.3.7 Timing considerations for PAUSE operation

Insert the following new paragraph after the paragraph starting "At operating speeds of 40 Gb/s, …":

At operating speeds of 50 Gb/s, a station shall not begin to transmit a (new) frame more than 394 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

Insert the following calculation for 50 Gb/s operation, after the line "40 Gb/s - max_overrun = 7552 + frame_length.":

50 Gb/s - max_overrun = 25216 + frame_length.

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Annex 93A

(normative)

Specification methods for electrical channels

93A.1 Channel Operating Margin

Insert new row into Table 93A–1 (as modified by IEEE Std 802.3bs-201x) below the row for parameter "Transmitter equalizer, minimum cursor coefficient" (unmodified rows are not shown):

Table 93A–1—COM parameters

Parameter	Reference	Symbol	Units
Transmitter equalizer, 2nd pre-cursor coefficient[a] Minimum value Maximum value Step size	93A.1.4.2	$c(-2)$	 — — —

[a]Some clauses that invoke this method do not provide a value for $c(-2)$. See 93A.1.4.2.

Change Table 93A–2 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bs-201x) as follows (some unmodified rows are not shown):

Table 93A–2—Physical Layer specifications that employ COM

Physical Layer	Parameter values
…	…
25GAUI C2C (Annex 109A)	Table 83D–6
50GBASE-CR (Clause 136)	Table 136–15
50GBASE-KR (Clause 137)	Table 137–5
LAUI-2 C2C (Annex 135B)	Table 83D–6
50GAUI-2 C2C (Annex 135D)	Table 83D–6
50GAUI-1 C2C (Annex 135F)	Table 120D–8
100GBASE-CR4 (Clause 92)	Table 93–8
100GBASE-CR2 (Clause 136)	Table 136–15

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Table 93A–2—Physical Layer specifications that employ COM

Physical Layer	Parameter values
100GBASE-KR4 (Clause 93)	Table 93–8
100GBASE-KP4 (Clause 94)	Table 94–17
100GBASE-KR2 (Clause 137)	Table 137–5
CAUI-4 C2C (Annex 83D)	Table 83D–6
100GAUI-4 (Annex 135D)	Table 83D–6
100GAUI-2 (Annex 135F)	Table 120D–8
200GBASE-CR4 (Clause 136)	Table 136–15
200GBASE-KR4 (Clause 137)	Table 137–5
200GAUI-8 C2C (Annex 120B)	Table 83D–6[a]
...	...

[a]With the exceptions given in 120B.4.

93A.1.4 Filters

93A.1.4.2 Transmitter equalizer

Change the text of 93A.1.4.2 as follows:

$H_{ffe}(f)$ is defined by Equation (93A–21) and is intended to represent the transmitter equalizer. If k corresponds to a near-end crosstalk path, then $c(-2)$, $c(-1)$, and $c(1)$ are all zero regardless of the values used for the other paths. The value of the "cursor" coefficient $c(0)$ is set to ~~$1 - |c(-1)| - |c(1)|$~~ $1 - |c(-2)| - |c(-1)| - |c(1)|$ for any value of $c(-2)$, $c(-1)$ and $c(1)$. If the value of $c(0)$ is less than the specified minimum value, the corresponding combination of $c(-2)$, $c(-1)$, and $c(1)$ is considered invalid and is not used to calculate COM.

Replace Equation (93A–21) with the following equation:

$$H_{ffe}(f) = \sum_{i=-2}^{1} c(i)\exp\left(-j2\pi(i+2)\frac{f}{f_b}\right) \qquad \text{(93A–21)}$$

(93A–21)

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93A.1.6 Determination of variable equalizer parameters

Change the first paragraph of 93A.1.6 (as modified by IEEE Std 802.3bs-201x) and item a) as follows:

COM is a function of the variables c(−2), $c(-1)$, $c(1)$, g_{DC}, and g_{DC2}. The following procedure is used to determine the values of these variables that are used to calculate COM.

a) Compute the pulse response $h_{(k)}(t)$ of each signal path k for a given c(−2), $c(-1)$, $c(1)$, g_{DC}, and g_{DC2} using the procedure defined in 93A.1.5.

Change the last paragraph of 93A.1.6 (as modified by IEEE Std 802.3bs-201x) as follows:

The FOM is calculated for each permitted combination of c(−2), $c(-1)$, $c(1)$, g_{DC}, and g_{DC2} values per Table 93A–1, where any parameters not provided by the clause that invokes this method are set to 0. The combination of values that maximizes the FOM, including the corresponding value of t_s, is used for the calculation of the interference and noise amplitude in 93A.1.7 and the calculation of COM in 93A.1.

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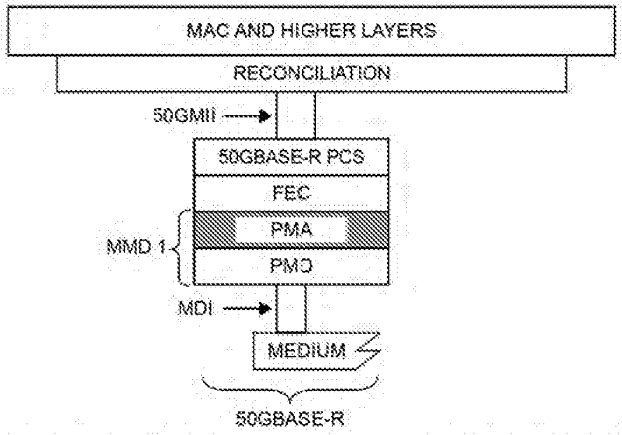
Annex 135A

(informative)

50 Gb/s and 100 Gb/s PMA sublayer partitioning examples

The figures in this annex provide various partitioning examples. Partitioning guidelines and MMD numbering conventions are described in 135.1.4. These partitioning examples are informative and do not specify a particular sublayer combination for any PHY. Specific and compliant sublayer combinations for a particular PHY are provided in the appropriate normative clause.

135A.1 Partitioning examples of 50GBASE-R PHYs

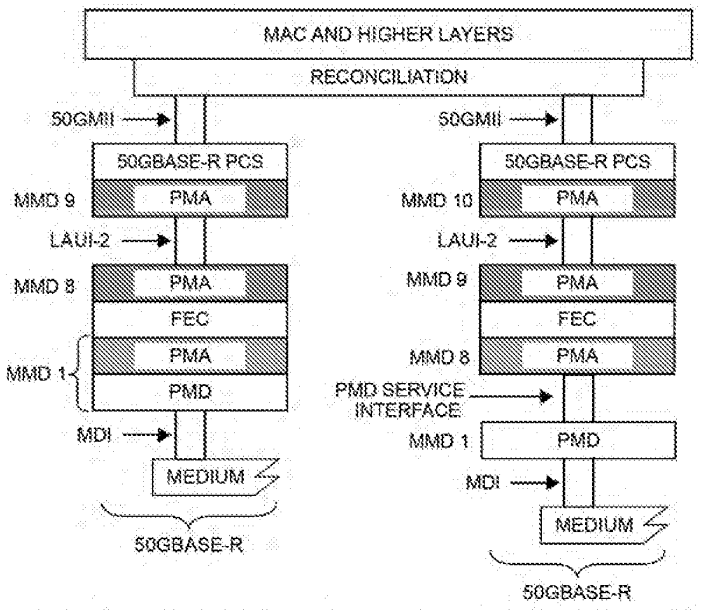


50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135A–1—Example FEC implemented with PCS and PMD

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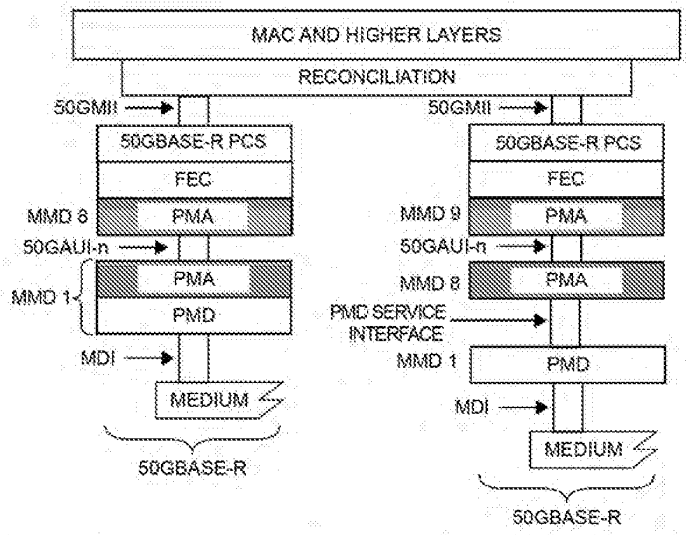


50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LAUI-2= 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135A–2—Example FEC implemented with PMD

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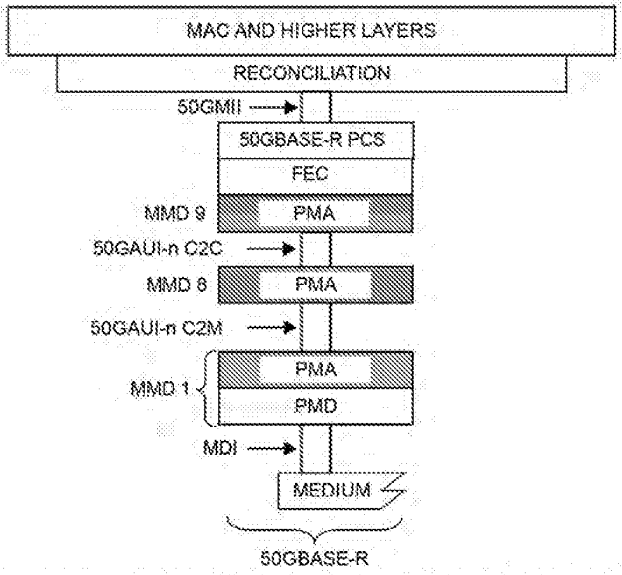


50GAUI-n = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135A–3—Example single 50G, FEC implemented with PCS

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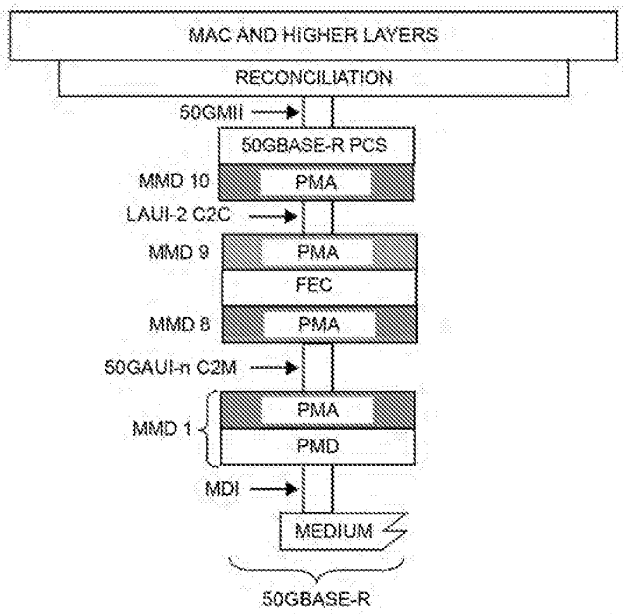


50GAUI-n = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135A–4—Intermediate PMA device for module interface, FEC implemented with PCS.

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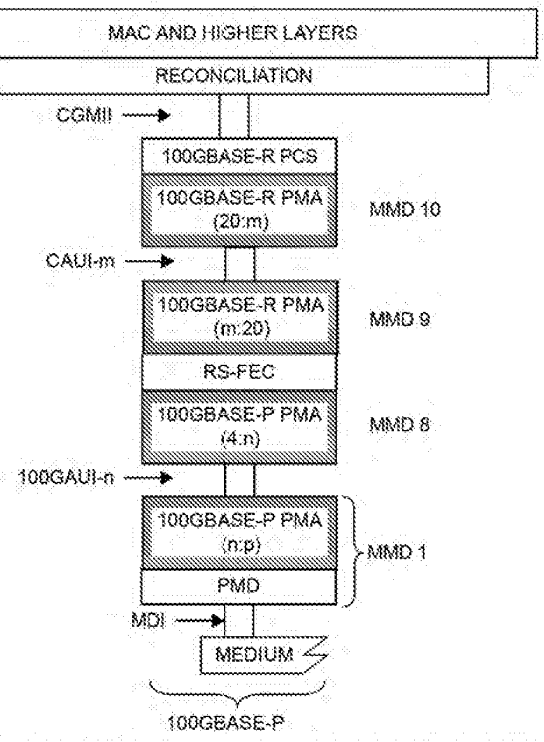
50GAUI-n = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LAUI-2 = 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135A–5—Intermediate PMA device with FEC for module interface.

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135A.2 Partitioning examples of 100GBASE-P PHYs



CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
m = 4 or 10
n = 2 or 4
p = 1 or 2

Figure 135A–8—Example 100GBASE-P PHY with CAUI-n and 100GAUI-n

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Annex 135B

(normative)

Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C)

135B.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2C). Figure 135B–1 shows an example relationship of the LAUI-2 C2C interfaces to the ISO/IEC Open System Interconnection (OSI) reference model, respectively. The LAUI-2 C2C interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.

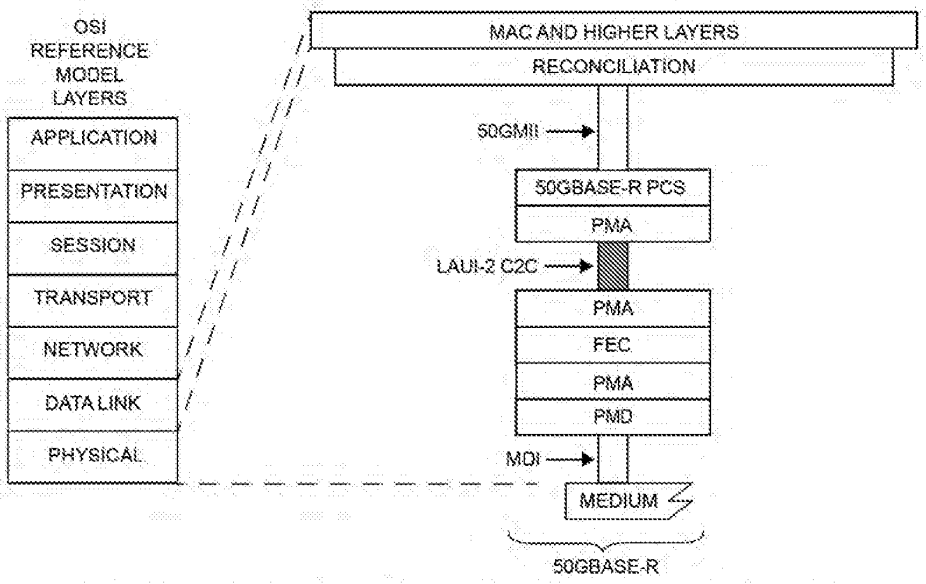


Figure 135B–1—Example LAUI-2 C2C relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

LAUI-2 C2C is a physical instantiation of the PMA service interface between the PCS and the FEC.

The LAUI-2 C2C bidirectional link is described in terms of a LAUI-2 C2C transmitter, a LAUI-2 C2C channel, and a LAUI-2 C2C receiver. Figure 135B–2 depicts a typical LAUI-2 C2C application. The informative differential insertion loss budget associated with the C2C application can be found in

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Equation (83D–1) and Figure 83D–3. The LAUI-2 C2C interface comprises independent data paths in each direction. Each data path contains two differential lanes using NRZ signaling, which are AC-coupled. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

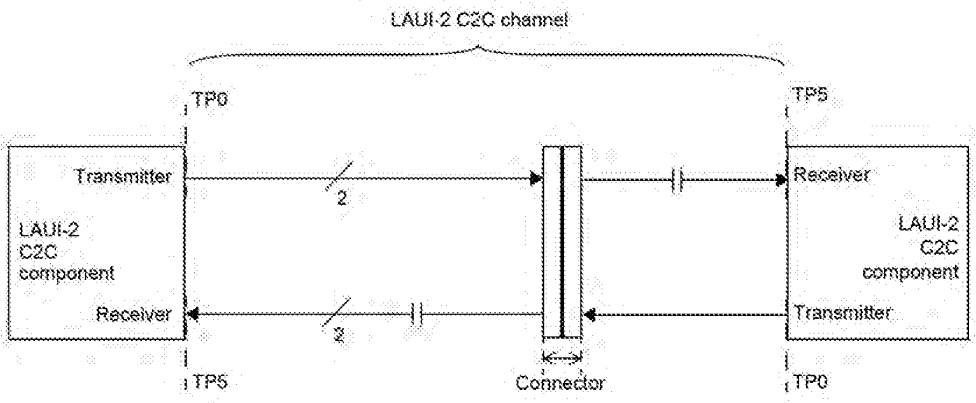


Figure 135B–2—Typical LAUI-2 C2C application

The nominal signaling rate for each lane is 25.78125 GBd. The LAUI-2 C2C transmitter on each end of the link is adjusted to an appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 83D.3.3.2 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

The normative channel compliance is through LAUI-2 C2C channel operating margin (COM) as described in 83D.4. Actual channel loss could be higher or lower than that given by Equation (83D–1) due to the channel ILD, return loss, and crosstalk.

135B.2 LAUI-2 C2C compliance point definition

The compliance points for the LAUI-2 C2C interface is defined in 83D.2.

135B.3 LAUI-2 C2C electrical characteristics

135B.3.1 LAUI-2 C2C transmitter characteristics

A LAUI-2 C2C transmitter shall meet all specifications for two CAUI-4 lanes in 83D.3.1.

135B.3.2 LAUI-2 C2C receiver characteristics

A LAUI-2 C2C receiver shall meet all specifications for two CAUI-4 lanes in 83D.3.3.

If the LAUI-2 C2C receiver supports the optional transmitter equalization feedback, it shall meet all requirements in 83D.3.3.2.

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135B.4 LAUI-2 C2C channel characteristics

The LAUI-2 C2C channel shall meet the requirements specified in 83D.4.

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135B.5 Protocol implementation conformance statement (PICS) proforma for Annex 135B, Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C)

135B.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135B, Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135B.5.2 Identification

135B.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135B.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Annex 135B, Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

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135B.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135B.1	Two independent data paths in each direction	M	Yes [ ]
*CHAN	Channel	135B.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]

135B.5.4 PICS proforma tables for Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C)

135B.5.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	135B.3.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	135B.3.1	1 200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	135B.3.1	Less than or equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	135B.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode output voltage	135B.3.1	12 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	135B.3.1	Meets Equation (93–3) constraints	M	Yes [ ]
TC7	Common-mode output return loss	135B.3.1	Meets Equation (93–4) constraints	M	Yes [ ]
TC8	Output waveform	135B.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC9	Output jitter	135B.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC10	Transmit equalization	135B.3.1	Each successive step results in a monotonic change	M	Yes [ ]

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135B.5.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	135B.3.2	Meets Equation (93–3) constraints	M	Yes [ ]
RC2	Differential to common-mode input return loss	135B.3.2	Meets Equation (93–5) constraints	M	Yes [ ]
RC3	Interference tolerance	135B.3.2	Satisfy requirements in Table 83D–6 with the exceptions in 135B.3.2	M	Yes [ ]
RC4	Jitter Tolerance	135B.3.2	Satisfy requirements in Table 93–7	M	Yes [ ]

135B.5.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	135B.4	Greater than or equal to 2 dB	CHAN:M	Yes [ ] N/A [ ]

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Annex 135C

(normative)

Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2M)

135C.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2M). Figure 135C–1 shows the relationship of the LAUI-2 C2M interface to the ISO/IEC Open System Interconnection (OSI) reference model. The C2M interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable module interfaces.

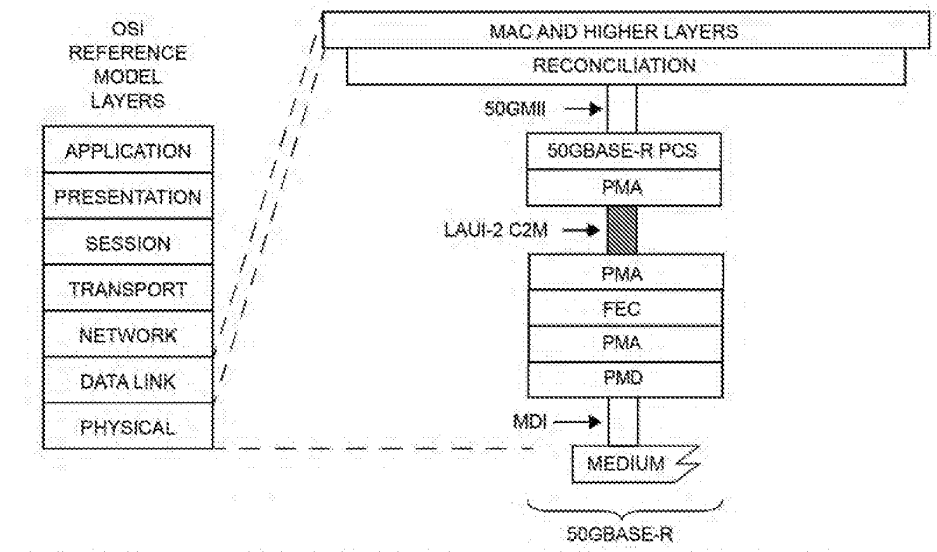


Figure 135C–1—Example LAUI-2 C2M relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

LAUI-2 C2M is a physical instantiation of the PMA service interface between the PCS and the FEC.

The LAUI-2 C2M link is described in terms of a host LAUI-2 C2M component, a LAUI-2 C2M channel with associated insertion loss, and a module LAUI-2 C2M component. Figure 135C–2 depicts a typical LAUI-2 C2M application and summarizes the differential insertion loss budget associated with the C2M application. The supported insertion loss budget is characterized by Equation (83E–1) and illustrated in

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Figure 83E–3. The LAUI-2 C2M interface comprises independent data paths in each direction. Each data path contains two differential lanes using NRZ signaling, which are AC-coupled within the module.

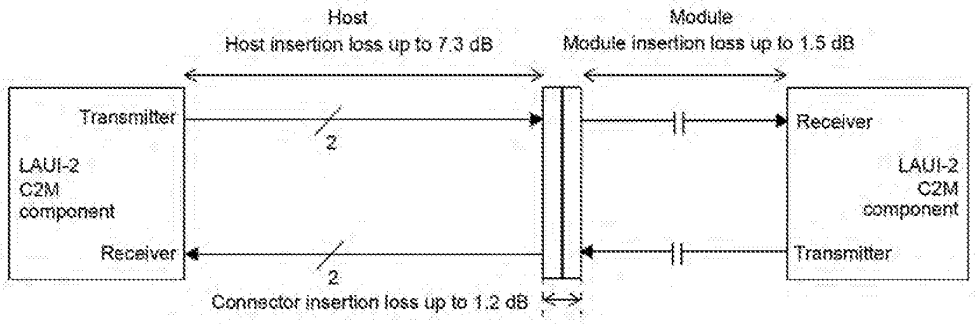


Figure 135C–2—LAUI-2 C2M insertion loss budget at 12.89 GHz

The nominal signaling rate for each lane is 25.78125 GBd. The LAUI-2 C2M interface is defined using a specification and test methodology that is similar to that used for CEI-28G-VSR defined in OIF-CEI-03.1 [B35].

135C.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 10^{-15} with any errors sufficiently uncorrelated to ensure an acceptably high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding.

135C.2 LAUI-2 C2M compliance point definitions

The compliance points for the LAUI-2 C2M interfaces are as defined for two CAUI-4 lanes in 83E.2.

135C.3 LAUI-2 C2M electrical characteristics

135C.3.1 LAUI-2 C2M host output characteristics

A LAUI-2 C2M host output shall meet all specifications for two CAUI-4 lanes in 83E.3.1.

135C.3.2 LAUI-2 C2M module output characteristics

A LAUI-2 C2M module output shall meet all specifications for two CAUI-4 lanes in 83E.3.2.

135C.3.3 LAUI-2 C2M host input characteristics

A LAUI-2 C2M host input shall meet all specifications for two CAUI-4 lanes in 83E.3.3

135C.3.4 LAUI-2 C2M module input characteristics

A LAUI-2 C2M module input shall meet all specifications for two CAUI-4 lanes in 83E.3.4.

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135C.4 LAUI-2 C2M measurement methodology

The LAUI-2 C2M measurement methodology is as defined in 83E.4.

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135C.5 Protocol implementation conformance statement (PICS) proforma for Annex 135C, Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2M)

135C.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135C, Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2M) shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135C.5.2 Identification

135C.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135C.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Annex 135C, Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2M)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

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135C.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135C.1	Two independent data paths in each direction	M	Yes [ ]
BER	Meets BER requirement	135C.1.1		M	Yes [ ]
ADR	Adaptive receiver	135C.3.4	Module receiver does not use *Recommended_CTLE_value*	O	Yes [ ] No [ ]

135C.5.4 PICS proforma tables for Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2M)

135C.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	135C.3.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	Peak-to-peak differential output voltage	135C.3.1	900 mV (max)	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	135C.3.1	Less than or equal to 35 mV	M	Yes [ ]
TH4	DC common-mode output voltage	135C.3.1	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH5	AC common-mode output voltage	135C.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Differential output return loss	135C.3.1	Meets Equation (83E–2) constraints	M	Yes [ ]
TH7	Reference impedance for output return loss	135C.3.1	100 Ω	M	Yes [ ]
TH8	Common to differential mode conversion	135C.3.1	Meets Equation (83E–3) constraints	M	Yes [ ]
TH9	Differential termination mismatch	135C.3.1	Less than 10%	M	Yes [ ]
TH10	Transition time	135C.3.1	Greater than or equal to 10 ps	M	Yes [ ]
TH11	Eye width	135C.3.1	0.46 UI	M	Yes [ ]
TH12	Eye height A	135C.3.1	95 mV	M	Yes [ ]
TH13	Eye height B	135C.3.1	80 mV	M	Yes [ ]
TH14	Crosstalk source	135C.3.1	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 50GBASE-R signal	M	Yes [ ]

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135C.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Signal rate	135C.3.2	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TM2	Peak-to-peak differential output voltage	135C.3.2	900 mV (max)	M	Yes [ ]
TM3	AC common-mode output voltage	135C.3.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM4	Differential output return loss	135C.3.2	Meets Equation (83E–2) constraints	M	Yes [ ]
TM5	Reference impedance for output return loss	135C.3.2	100 Ω.	M	Yes [ ]
TM6	Common to differential mode conversion	135C.3.2	Meets Equation (83E–3) constraints	M	Yes [ ]
TM7	Differential termination mismatch	135C.3.2	Less than 10%	M	Yes [ ]
TM8	Transition time	135C.3.2	Greater than or equal to 12 ps	M	Yes [ ]
TM9	Eye width	135C.3.2	0.57 UI	M	Yes [ ]
TM10	Eye height	135C.3.2	228 mV	M	Yes [ ]
TM11	Crosstalk source	135C.3.2	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 50GBASE-R signal	M	Yes [ ]
TM12	Vertical eye closure	135C.3.2	5.5 dB (max)	M	Yes [ ]

135C.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	Host input characteristics	135C.3.3	Table 83E–6	M	Yes [ ]

135C.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Module input characteristics	135C.3.4	Table 83E–7	M	Yes [ ]
RM2	Module stressed input test BER requirement	135C.3.4	As 83E.1.1 with settings associated with *Recommended_CTLE_value*	M	Yes [ ]

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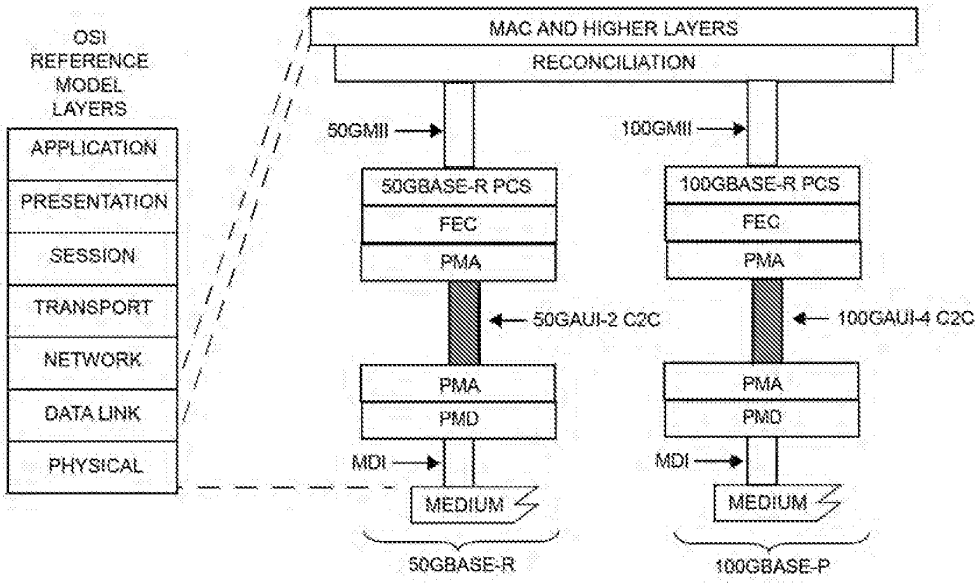
Annex 135D

(normative)

Chip-to-chip 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2C)

135D.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2C). Figure 135D–1 shows example relationships of the 50GAUI-2 C2C and 100GAUI-4 C2C interfaces to the ISO/IEC Open System Interconnection (OSI) reference model, respectively. The 50GAUI-2 C2C and 100GAUI-4 C2C interfaces provide electrical characteristics and associated compliance points, which can optionally be used when designing systems with electrical inter-connect of approximately 25 cm in length.



100GAUI-4 C2C= 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
100GMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
50GAUI-2 C2C = 50 Gb/s TWO-LANE ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135D–1—Example 50GAUI-2 C2C and 100GAUI-4 C2C relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

50GAUI-2 C2C and 100GAUI-4 C2C are physical instantiations of the PMA service interface between the FEC and the PMD.

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The 50GAUI-2 C2C bidirectional link is described in terms of a 50GAUI-2 C2C transmitter, a 50GAUI-2 C2C channel, and a 50GAUI-2 C2C receiver. Figure 135D–2 depicts a typical 50GAUI-2 C2C application and Equation (83D–1) (illustrated in Figure 83D–3) summarizes the informative differential insertion loss budget associated with the 50GAUI-2 C2C application. The 50GAUI-2 C2C interface comprises independent data paths in each direction. Each data path contains two differential lanes using NRZ signaling, which are AC-coupled. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

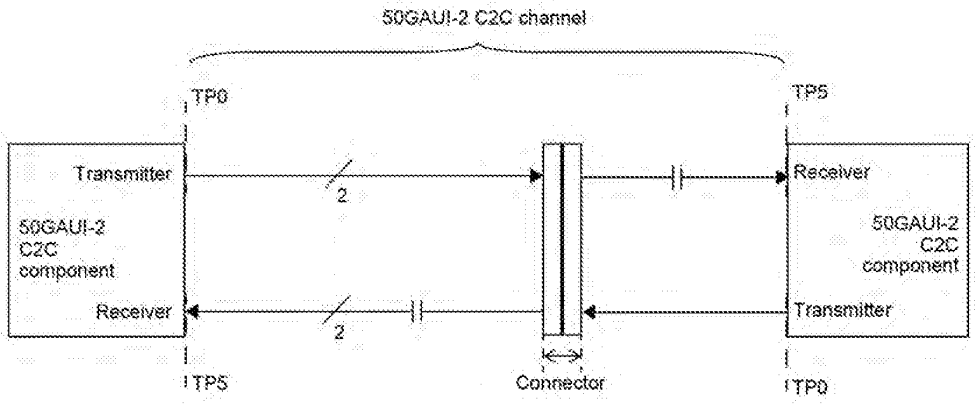


Figure 135D–2—Typical 50GAUI-2 C2C application

The 100GAUI-4 C2C bidirectional link is described in terms of a 100GAUI-4 C2C transmitter, a 100GAUI-4 C2C channel, and a 100GAUI-4 C2C receiver. Figure 135D–3 depicts a typical 100GAUI-4 C2C application, and Equation (83D–1) (illustrated in Figure 83D–3) summarizes the informative differential insertion loss budget associated with the 100GAUI-4 C2C application. The 100GAUI-4 C2C interface comprises independent data paths in each direction. Each data path contains four differential lanes using NRZ signaling, which are AC-coupled. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

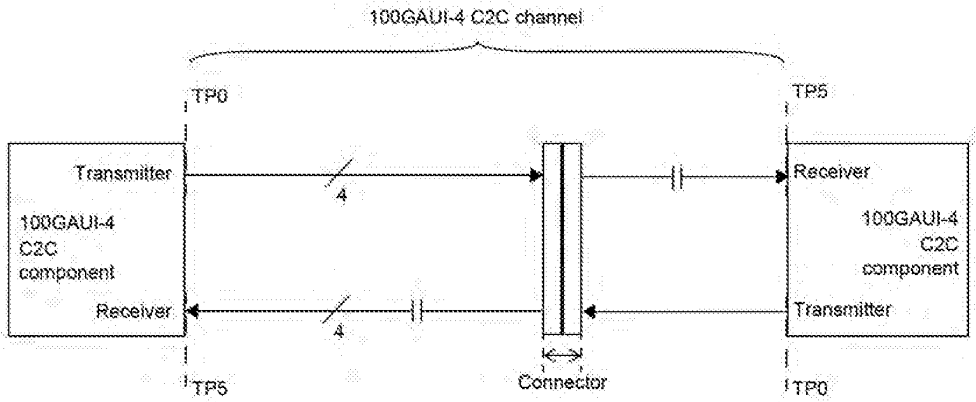


Figure 135D–3—Typical 100GAUI-4 C2C application

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The nominal signaling rate for each lane is 26.5625 GBd. The 50GAUI-2 C2C or 100GAUI-4C2C transmitter on each end of the link is adjusted to an appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 83D.3.3.2 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

The normative channel compliance is through 50GAUI-2 C2C or 100GAUI-4 C2C channel operating margin (COM) as described in 83D.4. Actual channel loss could be higher or lower than that given by Equation (83D–1) due to the channel ILD, return loss, and crosstalk.

135D.2 50GAUI-2 C2C and 100GAUI-4 C2C compliance point definition

The compliance points for the 50GAUI-2 C2C and 100GAUI-4 C2C interfaces are as defined in 83D.2.

135D.3 50GAUI-2 C2C and 100GAUI-4 C2C electrical characteristics

135D.3.1 50GAUI-2 C2C and 100GAUI-4 C2C transmitter characteristics

A 50GAUI-2 C2C or a 100GAUI-4 C2C transmitter shall meet all specifications in 120B.3.1.

135D.3.2 50GAUI-2 C2C and 100GAUI-4 C2C receiver characteristics

A 50GAUI-2 C2C or a 100GAUI-4 C2C receiver shall meet all specifications in 120B.3.2.

135D.4 50GAUI-2 C2C and 100GAUI-4 C2C channel characteristics

The 50GAUI-2 C2C or 100GAUI-4 C2C channel shall meet the requirements specified in 120B.4.

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135D.5 Protocol implementation conformance statement (PICS) proforma for Annex 135D, Chip-to-chip 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2C)[17]

135D.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135D, Chip-to-chip 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2C), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135D.5.2 Identification

135D.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135D.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Annex 135D, Chip-to-chip 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2C)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

[17] *Copyright release for PICS proformas:* Users of this standard *may* freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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135D.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135D.1	two independent data paths in each direction for 50GAUI-2 C2C and four independent data paths in each direction for 100GAUI-4 C2C	M	Yes [ ]
*CHAN	Channel	135D.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]

135D.5.4 PICS proforma tables for Chip-to-chip 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2C)

135D.5.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	135D.3.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	135D.3.1	1 200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	135D.3.1	Less than or equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	135D.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode output voltage	135D.3.1	12 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	135D.3.1	Meets Equation (93–3) constraints	M	Yes [ ]
TC7	Common-mode output return loss	135D.3.1	Meets Equation (93–4) constraints	M	Yes [ ]
TC8	Output waveform	135D.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC9	Output jitter	135D.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC10	Transmit equalization	135D.3.1	Each successive step results in a monotonic change	M	Yes [ ]

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135D.5.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	135D.3.2	Meets Equation (93–3) constraints	M	Yes [ ]
RC2	Differential to common-mode input return loss	135D.3.2	Meets Equation (93–5) constraints	M	Yes [ ]
RC3	Interference tolerance	135D.3.2	Satisfy requirements in Table 83D–3 with the exceptions in 135D.3.2	M	Yes [ ]

135D.5.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	135D.4	Greater than or equal to 3 dB	CHAN:M	Yes [ ] N/A [ ]

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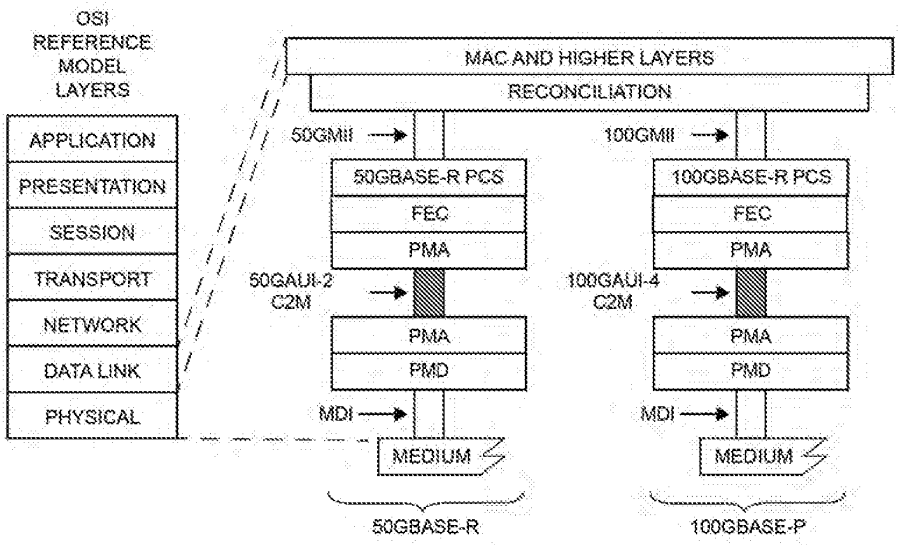
Annex 135E

(normative)

Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2M)

135E.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2M). Figure 135E–1 shows the relationship of the 50GAUI-2 C2M and 100GAUI-4 C2M interfaces to the ISO/IEC Open System Interconnection (OSI) reference model. The C2M interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable module interfaces.



100GAUI-4 C2M = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
100GMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
50GAUI-2 C2M = 50 Gb/s TWO-LANE ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135E–1—Example 50GAUI-2 C2M and 100GAUI-4 C2M relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

50GAUI-2 C2M and 100GAUI-4 C2M are physical instantiations of the PMA service interface between the FEC and the PMD.

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The 50GAUI-2 C2M link is described in terms of a host 50GAUI-2 C2M component, a 50GAUI-2 C2M channel with associated insertion loss, and a module 50GAUI-2 C2M component. Figure 135E–2 depicts a typical 50GAUI-2 C2M application and summarizes the differential insertion loss budget associated with the 50GAUI-2 C2M application. The supported insertion loss budget is characterized by Equation (83E–1) and illustrated in Figure 83E–3. The 50GAUI-2 C2M interface comprises independent data paths in each direction. Each data path contains two differential lanes using NRZ signaling, which are AC-coupled within the module.

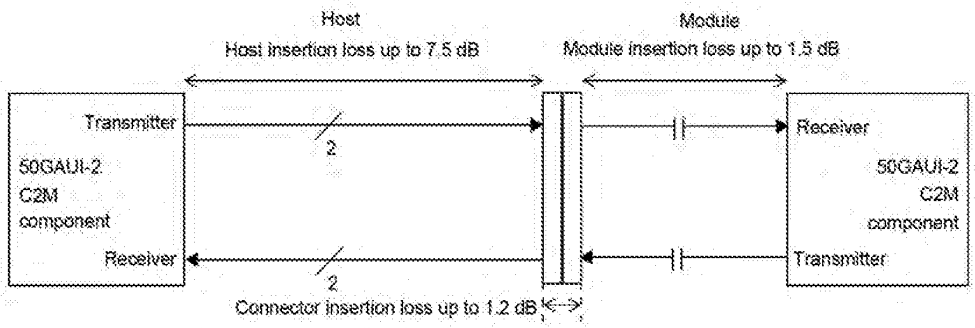


Figure 135E–2—50GAUI-2 C2M insertion loss budget at 13.28 GHz

The 100GAUI-4 C2M link is described in terms of a host 100GAUI-4 C2M component, a 100GAUI-4 C2M channel with associated insertion loss, and a module 100GAUI-4 C2M component. Figure 135E–3 depicts a typical 100GAUI-4 C2M application and summarizes the differential insertion loss budget associated with the C2M application. The supported insertion loss budget is characterized by Equation (83E–1) and illustrated in Figure 83E–3. The 100GAUI-4 C2M interface comprises independent data paths in each direction. Each data path contains four differential lanes using NRZ signaling, which are AC-coupled within the module.

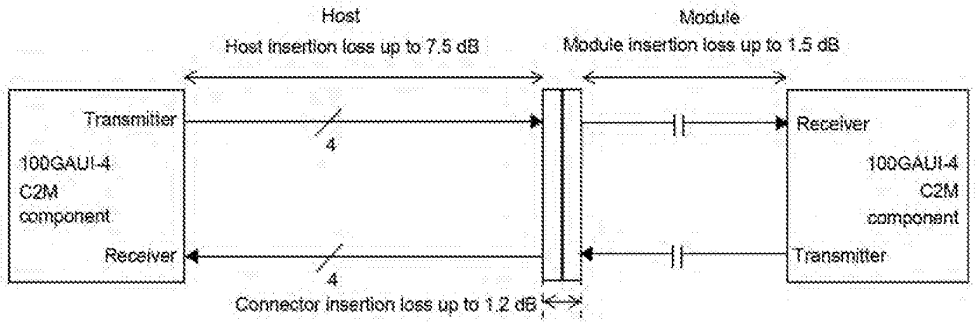


Figure 135E–3—100GAUI-4 C2M insertion loss budget at 13.28 GHz

The nominal signaling rate for each lane is 26.5625 GBd. The 50GAUI-2 C2M and 100GAUI-4 C2M interfaces are defined using a specification and test methodology that is similar to that used for CEI-28G-VSR defined in OIF-CEI-03.1 [D55].

135E.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 10^{-6}.

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135E.2 50GAUI-2 C2M and 100GAUI-4 C2M compliance point definitions

The compliance points for the 50GAUI-2 C2M and 100GAUI-4 C2M interfaces are as defined in 83E.2.

135E.3 50GAUI-2 C2M and 100GAUI-4 C2M electrical characteristics

135E.3.1 50GAUI-2 C2M and 100GAUI-4 C2M host output characteristics

A 50GAUI-2 C2M or 100GAUI-4 C2M host output shall meet all specifications in 120C.3.1.

135E.3.2 50GAUI-2 C2M and 100GAUI-4 C2M module output characteristics

A 50GAUI-2 C2M or a 100GAUI-4 C2M module output shall meet all specifications in 120C.3.2.

135E.3.3 50GAUI-2 C2M and 100GAUI-4 C2M host input characteristics

A 50GAUI-2 C2M or a 100GAUI-4 C2M host input shall meet all specifications in 120C.3.3.

135E.3.4 50GAUI-2 C2M and 100GAUI-4 C2M module input characteristics

A 50GAUI-2 C2M or a 100GAUI-4 C2M module input shall meet all specifications in 120C.3.4.

135E.4 50GAUI-2 C2M and 100GAUI-4 C2M measurement methodology

The 50GAUI-2 C2M and 100GAUI-4 C2M measurement methodology is as defined in 120C.4

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135E.5 Protocol implementation conformance statement (PICS) proforma for Annex 135E, Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2M)[18]

135E.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135E, Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2M), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135E.5.2 Identification

135E.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135E.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Annex 135E, Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2M)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

[18] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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135E.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135E.1	Two independent data paths in each direction for 50GAUI-2 C2M and four independent data paths in each direction for 100GAUI-4 C2M	M	Yes [ ]
BER	Meets BER requirement	135E.1.1	See 135E.1.1	M	Yes [ ]
ADR	Adaptive receiver	135E.3.4	Module receiver does not use *Recommended_CTLE_value*	O	Yes [ ] No [ ]

135E.5.4 PICS proforma tables for Annex 135E, Chip-to-module 50 Gb/s 2-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s 4-lane Attachment Unit Interface (100GAUI-4 C2M)

135E.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	135E.3.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	Peak-to-peak differential output voltage	135E.3.1	900 mV (max)	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	135E.3.1	Less than or equal to 35 mV	M	Yes [ ]
TH4	DC common-mode output voltage	135E.3.1	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH5	AC common-mode output voltage	135E.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Differential output return loss	135E.3.1	Meets Equation (83E–2) constraints	M	Yes [ ]
TH7	Reference impedance for output return loss	135E.3.1	100 Ω.	M	Yes [ ]
TH8	Common to differential mode conversion	135E.3.1	Meets Equation (83E–3) constraints	M	Yes [ ]
TH9	Differential termination mismatch	135E.3.1	Less than 10%	M	Yes [ ]
TH10	Transition time	135E.3.1	Greater than or equal to 10 ps	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TH11	Eye width	135E.3.1	0.46 UI	M	Yes [ ]
TH12	Eye height A	135E.3.1	95 mV	M	Yes [ ]
TH13	Eye height B	135E.3.1	80 mV	M	Yes [ ]
TH14	Crosstalk source	135E.3.1	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 50GBASE-R/100GBASE-R signal	M	Yes [ ]

135E.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Signal rate	135E.3.2	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TM2	Peak-to-peak differential output voltage	135E.3.2	900 mV (max)	M	Yes [ ]
TM3	AC common-mode output voltage	135E.3.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM4	Differential output return loss	135E.3.2	Meets Equation (83E–2) constraints	M	Yes [ ]
TM5	Reference impedance for output return loss	135E.3.2	100 Ω.	M	Yes [ ]
TM6	Common to differential mode conversion	135E.3.2	Meets Equation (83E–3) constraints	M	Yes [ ]
TM7	Differential termination mismatch	135E.3.2	Less than 10%	M	Yes [ ]
TM8	Transition time	135E.3.2	Greater than or equal to 12 ps	M	Yes [ ]
TM9	Eye width	135E.3.2	0.57 UI	M	Yes [ ]
TM10	Eye height	135E.3.2	228 mV	M	Yes [ ]
TM11	Crosstalk source	135E.3.2	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 50GBASE-R/100GBASE-R signal	M	Yes [ ]
TM12	Vertical eye closure	135E.3.2	5.5 dB (max)	M	Yes [ ]

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135E.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	Host input characteristics	135E.3.3	Table 83E–4 with the exceptions in 120C.3.3	M	Yes [ ]

135E.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Module input characteristics	135E.3.4	Table 83E–7 with the exceptions in 120C.3.3	M	Yes [ ]
RM2	Module stressed input test BER requirement	135E.3.4	Meet BER requirement of 135E.1.1 with three values of *Recommended_CTLE_value*	M	Yes [ ]

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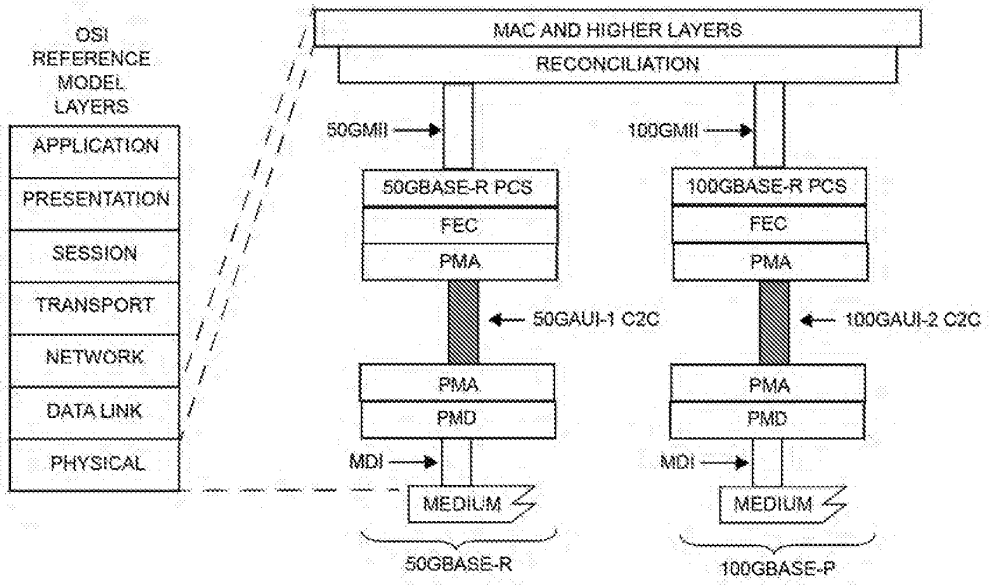
Annex 135F

(normative)

Chip-to-chip 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2C)

135F.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2C). Figure 135F–1 shows example relationships of the 50GAUI-1 C2C and 100GAUI-2 C2C interfaces to the ISO/IEC Open System Interconnection (OSI) reference model, respectively. The 50GAUI-1 C2C and 100GAUI-2 C2C interfaces provide electrical characteristics and associated compliance points, which can optionally be used when designing systems with electrical inter-connect of approximately 25 cm in length.



100GAUI-2 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
100GMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
50GAUI-1 = 50 Gb/s ONE-LANE ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135F–1—Example 50GAUI-1 C2C and 100GAUI-2 C2C relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

50GAUI-1 C2C and 100GAUI-2 C2C are physical instantiations of the PMA service interface between the FEC and the PMD.

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The 50GAUI-1 C2C bidirectional link is described in terms of a 50GAUI-1 C2C transmitter, a 50GAUI-1 C2C channel, and a 50GAUI-1 C2C receiver. Figure 135F–2 depicts a typical 50GAUI-1 C2C application and Equation (120D–1) (illustrated in Figure 120D–5) summarizes the informative differential insertion loss budget associated with the 50GAUI-1 C2C application. The 50GAUI-1 C2C interface comprises independent data paths in each direction. Each data path contains one differential lane using PAM4 signaling, which is AC-coupled. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

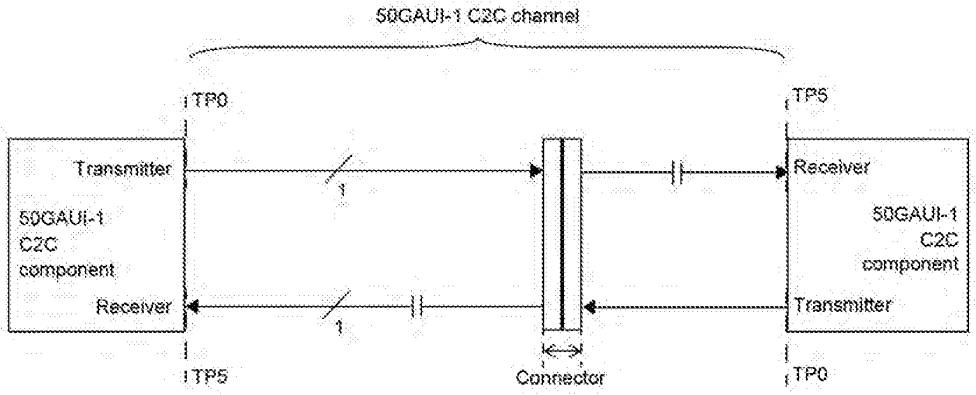


Figure 135F–2—Typical 50GAUI-1 C2C application

The 100GAUI-2 C2C bidirectional link is described in terms of a 100GAUI-2 C2C transmitter, a 100GAUI-2 C2C channel, and a 100GAUI-2 C2C receiver. Figure 135F–3 depicts a typical 100GAUI-2 C2C application and Equation (120D–1) (illustrated in Figure 120D–5) summarizes the informative differential insertion loss budget associated with the 100GAUI-2 C2C application. The 100GAUI-2 C2C interface comprises independent data paths in each direction. Each data path contains two differential lanes using PAM4 signaling, which are AC-coupled. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

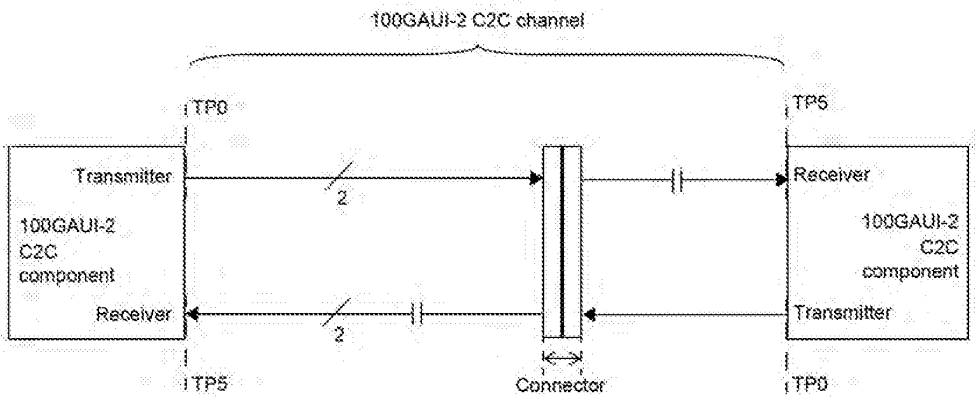


Figure 135F–3—Typical 100GAUI-2 C2C application

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The nominal signaling rate for each lane is 26.5625 GBd. The 50GAUI-1 C2C or 100GAUI-2 C2C transmitter on each end of the link is adjusted to an appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 120D.3.2.3 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

The normative channel compliance is through 50GAUI-1 C2C or 100GAUI-2 C2C channel operating margin (COM) as described in 120D.4. Actual channel loss could be higher or lower than that given by Equation (120D–1) due to the channel ILD, return loss, and crosstalk.

135F.2 50GAUI-1 C2C and 100GAUI-2 C2C compliance point definition

The compliance points for the 50GAUI-1 C2C and 100GAUI-2 C2C interfaces are as defined in 120D.2.

135F.3 50GAUI-1 C2C and 100GAUI-2 C2C electrical characteristics

135F.3.1 50GAUI-1 C2C and 100GAUI-2 C2C transmitter characteristics

A 50GAUI-1 C2C or a 100GAUI-2 C2C transmitter shall meet all specifications in 120D.3.1.

135F.3.2 50GAUI-1 C2C and 100GAUI-2 C2C receiver characteristics

A 50GAUI-1 C2C or a 100GAUI-2 C2C receiver shall meet all specifications in 120D.3.3.

135F.3.2.1 Transmitter precoder request (optional)

The transmitter precoder request is an optional capability for a 50GAUI-1 C2C or 100GAUI-2 C2C receiver. If implemented, it shall operate as described in this subclause.

The transmitter precoder request is generated for each lane (0 and 1) and interface (up towards the MAC and down towards the PMD) independently. The variables that control the transmitter precoding request are specific for each lane and interface.

A 50GAUI-1 C2C or 100GAUI-2 C2C receiver may generate a request to change the precoder state of the remote transmitter by setting the variable request_precoder_up_flag or request_precoder_down_flag to 1. The variables request_precoder_up_*i* and request_precoder_down_*i* (where *i* is 0 or 1) indicate the requested transmitter precoder state for the corresponding interface and lane. A request from a 50GAUI-1 C2C or 100GAUI-2 C2C receiver is generated in an implementation specific manner.

When a 50GAUI-1 C2C or 100GAUI-2 C2C receiver does not request a change of the remote transmitter's transmit setting, it sets request_precoder_up_flag or request_precoder_down_flag to 0. A 50GAUI-1 C2C or 100GAUI-2 C2C receiver that does not implement transmitter precoder request always sets request_precoder_up_flag or request_precoder_down_flag to 0.

If a Clause 45 MDIO is implemented, the variables request_precoder_up_flag, request_precoder_down_flag, request_precoder_up_*i*, and request_precoder_down_*i* are accessible through registers 1.604, 1.605, and 1.606 (see 45.2.1.116l through 45.2.1.116n).

135F.4 50GAUI-1 C2C and 100GAUI-2 C2C channel characteristics

The 50GAUI-1 C2C or 100GAUI-2 C2C channel shall meet the requirements specified in 120D.4.

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135F.5 Protocol implementation conformance statement (PICS) proforma for Annex 135F, Chip-to-chip 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2C)[19]

135F.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135F, Chip-to-chip 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2C), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135F.5.2 Identification

135F.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135F.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Annex 135F, Chip-to-chip 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2C)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

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135F.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135F.1	One independent data path in each direction for 50GAUI-1 C2C and two independent data paths in each direction for 100GAUI-2 C2C	M	Yes [ ]
*CHAN	Channel	135F.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]

135F.5.4 PICS proforma tables for Chip-to-chip 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2C)

135F.5.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	135F.3.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	135F.3.1	1 200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	135F.3.1	Less than or equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	135F.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode output voltage	135F.3.1	12 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	135F.3.1	Meets Equation (93–3) constraints	M	Yes [ ]
TC7	Common-mode output return loss	135F.3.1	Meets Equation (93–4) constraints	M	Yes [ ]
TC8	Output waveform	135F.3.1	Meets Table 120D–1 constraints	M	Yes [ ]
TC9	Output jitter	135F.3.1	Meets Table 120D–1 constraints	M	Yes [ ]
TC10	Transmit equalization	135F.3.1	Each successive step results in a monotonic change	M	Yes [ ]
TC11	Transmitter Output residual ISI	135F.3.1	Meets Table 120D–1 constraints	M	Yes [ ]
TC12	Signal-to-noise-and-distortion ratio	135F.3.1	Meets Table 120D–1 constraints	M	Yes [ ]

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135F.5.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	135F.3.2	Meets Equation (93–3) constraints	M	Yes [ ]
RC2	Differential to common-mode input return loss	135F.3.2	Meets Equation (93–5) constraints	M	Yes [ ]
RC3	Interference tolerance	135F.3.2	Satisfy requirements in Table 120D–6	M	Yes [ ]
RC4	Jitter tolerance	135F.3.2	Satisfy requirements in Table 120D–7	M	Yes [ ]

135F.5.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	135E.4	Greater than or equal to 3 dB	CHAN:M	Yes [ ] N/A [ ]

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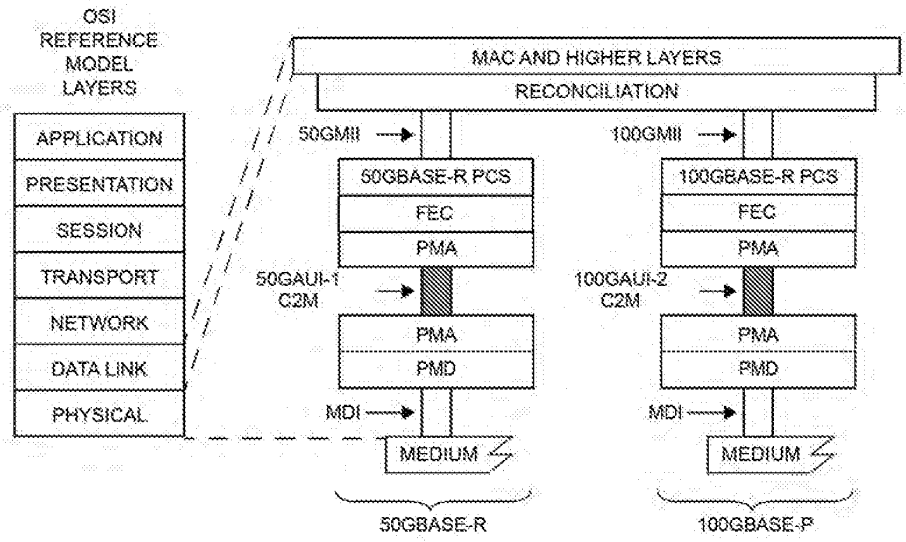
Annex 135G

(normative)

Chip-to-module 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2M)

135G.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2M). Figure 135G–1 shows the relationship of the 50GAUI-1 C2M and 100GAUI-2 C2M interfaces to the ISO/IEC Open System Interconnection (OSI) reference model. The 50GAUI-1 C2M and 100GAUI-2 C2M interfaces provide electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable module interfaces.



100GAUI-2 C2M = 100 Gb/s TWO-LANE ATTACHMENT UNIT INTERFACE
100GMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
50GAUI-1 C2M = 50 Gb/s ONE-LANE ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135G–1—Example 50GAUI-1 C2M and 100GAUI-2 C2M relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

50GAUI-1 C2M and 100GAUI-2 C2M are physical instantiations of the PMA service interface between the FEC and the PMD.

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The 50GAUI-1 C2M link is described in terms of a host 50GAUI-1 C2M component, a 50GAUI-1 C2M channel with associated insertion loss, and a module 50GAUI-1 C2M component. Figure 135G–2 depicts a typical 50GAUI-1 C2M application and summarizes the differential insertion loss budget associated with the 50GAUI-1 C2M application. The supported insertion loss budget is characterized by Equation (120E–1) and illustrated in Figure 120E–4. The 50GAUI-1 C2M interface comprises independent data paths in each direction. The data path contains one differential lane using PAM4 signaling, which is AC-coupled within the module.

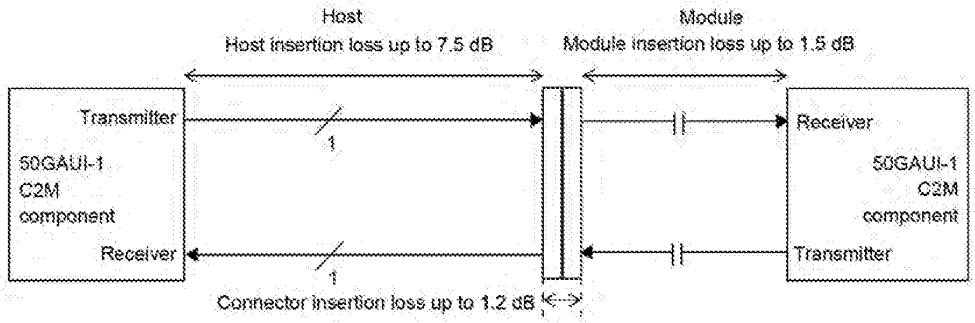


Figure 135G–2—50GAUI-1 C2M insertion loss budget at 13.28 GHz

The 100GAUI-2 C2M link is described in terms of a host 100GAUI-2 C2M component, a 100GAUI-2 C2M channel with associated insertion loss, and a module 100GAUI-2 C2M component. Figure 135G–3 depicts a typical 100GAUI-2 C2M application and summarizes the differential insertion loss budget associated with the 100GAUI-2 C2M application. The supported insertion loss budget is characterized by Equation (120E–1) and illustrated in Figure 120E–4. The 100GAUI-2 C2M interface comprises independent data paths in each direction. Each data path contains two differential lanes using PAM4 signaling, which are AC-coupled within the module.

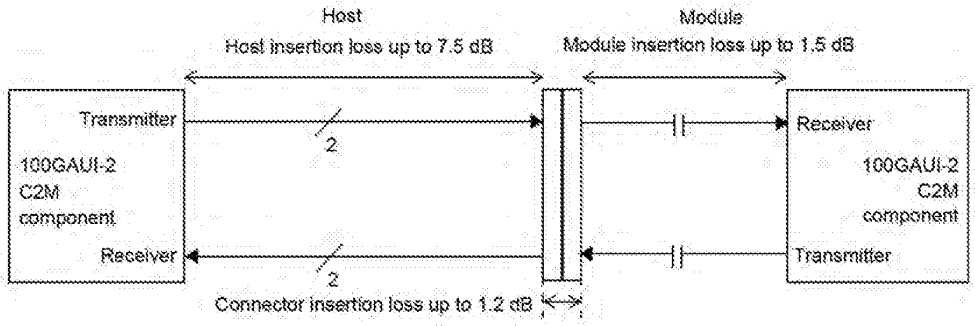


Figure 135G–3—100GAUI-2 C2M insertion loss budget at 13.28 GHz

The nominal signaling rate for each lane is 26.5625 GBd. The 50GAUI-1 C2M and 100GAUI-2 C2M interfaces are defined using a specification and test methodology that is similar to that used for CEI-56G-VSR defined in OIF-CEI-03.2 [D55].

135G.1.1 Bit error ratio

The bit error ratio (BER) when processed according to Clause 135 shall be less than 10^{-5}.

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135G.2 50GAUI-1 C2M and 100GAUI-2 C2M compliance point definitions

The compliance points for the 50GAUI-1 C2M and 100GAUI-2 C2M interfaces are as defined in 120E.2.

135G.3 50GAUI-1 C2M and 100GAUI-2 C2M electrical characteristics

135G.3.1 50GAUI-1 C2M and 100GAUI-2 C2M host output characteristics

A 50GAUI-1 C2M or 100GAUI-2 C2M host output shall meet all specifications in 120E.3.1.

135G.3.2 50GAUI-1 C2M and 100GAUI-2 C2M module output characteristics

A 50GAUI-1 C2M or a 100GAUI-2 C2M module output shall meet all specifications in 120E.3.2.

135G.3.3 50GAUI-1 C2M and 100GAUI-2 C2M host input characteristics

A 50GAUI-1 C2M or a 100GAUI-2 C2M host input shall meet all specifications in 120E.3.3.

135G.3.4 50GAUI-1 C2M and 100GAUI-2 C2M module input characteristics

A 50GAUI-1 C2M or a 100GAUI-2 C2M module input shall meet all specifications in 120E.3.4.

135G.4 50GAUI-1 C2M and 100GAUI-2 C2M measurement methodology

The 50GAUI-1 C2M and 100GAUI-2 C2M measurement methodology is as defined in 120E.4.

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135G.5 Protocol implementation conformance statement (PICS) proforma for Annex 135G, Chip-to-module 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2M)[20]

135G.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135G, Chip-to-module 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2M), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135G.5.2 Identification

135G.5.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135G.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Annex 135G, Chip-to-module 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2M)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

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135G.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135G.1	Eight independent data paths in each direction	M	Yes [ ]
BER	Meets BER requirement	135G.1.1		M	Yes [ ]
ADE	Adaptive Equalizer	135G.3.4		M	Yes [ ]

135G.5.4 PICS proforma tables for Chip-to-module 50 Gb/s 1-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s 2-lane Attachment Unit Interface (100GAUI-2 C2M)

135G.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	135G.3.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	Peak-to-peak differential output voltage	135G.3.1	880 mV (max)	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	135G.3.1	Less than or equal to 35 mV	M	Yes [ ]
TH4	DC common-mode output voltage	135G.3.1	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH5	AC common-mode output voltage	135G.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Differential output return loss	135G.3.1	Meets Equation (83E-2) constraints	M	Yes [ ]
TH7	Reference impedance for output return loss	135G.3.1	100 Ω.	M	Yes [ ]
TH8	Common to differential mode conversion	135G.3.1	Meets Equation (83E-3) constraints	M	Yes [ ]
TH9	Differential termination mismatch	135G.3.1	Less than 10%	M	Yes [ ]
TH10	Transition time	135G.3.1	Greater than or equal to 10 ps	M	Yes [ ]
TH11	Eye width, all 3 eyes	135G.3.1	0.25 UI	M	Yes [ ]
TH12	Eye height, all 3 eyes	135G.3.1	50 mV	M	Yes [ ]
TH13	Crosstalk source	135G.3.1	Asynchronous crosstalk source using PRBS13Q or PRBS31Q pattern, or valid 50GBASE-R / 100GBASE-R signal	M	Yes [ ]
TH14	Vertical eye closure	135G.3.1	5.5 dB (max)	M	Yes [ ]

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135G.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Signal rate	135G.3.2	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TM2	Peak-to-peak differential output voltage	135G.3.2	900 mV (max)	M	Yes [ ]
TM3	AC common-mode output voltage	135G.3.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM4	Differential output return loss	135G.3.2	Meets Equation (83E-2) constraints	M	Yes [ ]
TM5	Reference impedance for output return loss	135G.3.2	100 Ω	M	Yes [ ]
TM6	Common to differential mode conversion	135G.3.2	Meets Equation (83E-3) constraints	M	Yes [ ]
TM7	Differential termination mismatch	135G.3.2	Less than 10%	M	Yes [ ]
TM8	Transition time	135G.3.2	Greater than or equal to 9.5 ps	M	Yes [ ]
TM9	Near-end eye width, all 3 eyes	135G.3.2	0.265 UI	M	Yes [ ]
TM10	Near-end eye height, all 3 eyes	135G.3.2	90 mV	M	Yes [ ]
TM11	Far-end eye width, all 3 eyes	135G.3.2	0.2 UI	M	Yes [ ]
TM12	Far-end eye height, all 3 eyes	135G.3.2	30 mV	M	Yes [ ]
TM13	Crosstalk source	135G.3.2	Asynchronous crosstalk source using PRBS13Q or PRBS31Q pattern, or valid 50GBASE-R / 100GBASE-R signal	M	Yes [ ]

135G.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	Host input characteristics	135G.3.3	Table 120E–4	M	Yes [ ]

135G.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Module input characteristics	135G.3.4	Table 120E–7	M	Yes [ ]

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Annex 136A

(informative)

TP0 and TP5 test point parameters and channel characteristics for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136A.1 Overview

Annex 136A provides information on parameters associated with test points TP0 and TP5 that might not be testable in an implemented system. TP0 and TP5 test points are illustrated in the 50GBASE-CR, 100GBASE-CR2 and 200GBASE-CR4 link block diagram of Figure 136–2. This annex also provides information on channel characteristics.

136A.2 Transmitter characteristics at TP0

The transmitter characteristics at TP0 are constrained at TP0a by 137.9.2.

136A.3 Receiver characteristics at TP5

The receiver characteristics at TP5 are constrained at TP5a by 137.9.3.

136A.4 Transmitter and receiver differential printed circuit board trace loss

The recommended maximum and minimum printed circuit board trace insertion losses are specified in Equation (92A–1) and Equation (92A–2), respectively.

Note that the recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is 7 dB at 13.28 GHz and the recommended minimum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is 1.2 dB at 13.28 GHz. The recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is consistent with the insertion loss TP0 to TP2 or TP3 to TP5 given in Equation (92–8) and an assumed mated connector loss of 1.69 dB.

Note that the recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 is 10.07 dB at 13.28 GHz.

136A.5 Channel insertion loss

This subclause provides information on channel insertion losses for the maximum-loss and minimum-loss cabling topologies.

The maximum channel insertion loss associated with the cable assembly is determined using Equation (136A–1). The channel insertion loss budget at 13.28 GHz is illustrated in Figure 136A–1. Loss budget parameters for all cable topologies are provided in Table 136A–1.

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$$IL_{Chmax}(f) = IL_{Camax}(f) + 2IL_{Host}(f) - 2IL_{MatedTF}(f) \quad \text{(dB)} \quad \text{(136A–1)}$$

for 0.05 GHz $\leq f \leq$ 19 GHz

where

f	is the frequency in GHz
$IL_{Chmax}(f)$	is the maximum channel insertion loss between TP0 and TP5
$IL_{Camax}(f)$	is the maximum cable assembly insertion loss (TP1 to TP4)
$IL_{Host}(f)$	is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (92–8)
$IL_{MatedTF}(f)$	is the nominal insertion loss of the mated test fixture using Equation (136A–2)

The nominal insertion loss of the mated test fixture is determined using Equation (136A–2).

$$IL_{MatedTF}(f) = 0.471\sqrt{f} + 0.1194f + 0.002f^2 \quad \text{(dB)} \quad \text{(136A–2)}$$

for 0.01 GHz $\leq f \leq$ 25 GHz

where

f	is the frequency in GHz

The channel insertion loss associated with the 0.5 m cable assembly and a maximum host channel is determined by Equation (136A–3).

$$IL_{Ch0.5m}(f) = IL_{Camin}(f) + 2IL_{Host}(f) - 2IL_{MatedTF}(f) \quad \text{(dB)} \quad \text{(136A–3)}$$

for 0.05 GHz $\leq f \leq$ 19 GHz

where

f	is the frequency in GHz
$IL_{Ch0.5m}(f)$	is the channel insertion loss between TP0 and TP5 representative of a 0.5 m cable assembly and a maximum host channel
$IL_{Camin}(f)$	is the minimum cable assembly insertion loss (TP1 to TP4) given in Equation (92–26) and illustrated in Figure 92–12
$IL_{Host}(f)$	is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (92–8)
$IL_{MatedTF}(f)$	is the nominal insertion loss of the mated test fixture using Equation (136A–2)

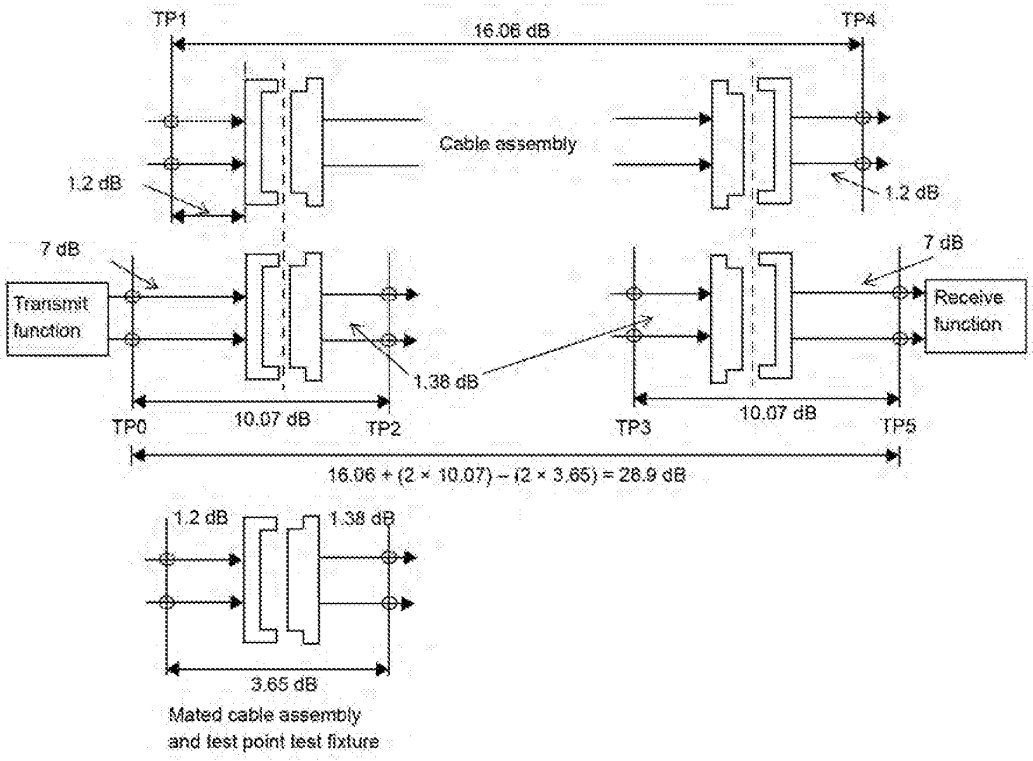
The loss budget parameter values at 13.28 GHz are provided in Table 136A–1.

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Table 136A–1—Cable insertion loss budget values at 13.28 GHz

Parameter	50GBASE-CR	100GBASE-CR2	200GBASE-CR4	Units
IL_{Cmax}	28.9			dB
IL_{Camax}	16.06			dB
$IL_{Ch0.5m}$	21.34			dB
IL_{Camin}	8.3			dB
IL_{Host}	10.07			dB
$IL_{MatedTF}$	3.65			dB



NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Figure 136A–1—28.9 dB channel insertion loss budget at 13.28 GHz

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136A.6 Channel return loss

The recommended return loss for 50GBASE-CR, 100GBASE-CR2 and 200GBASE-CR4 channels is specified in 92A.6.

136A.7 Channel Operating Margin (COM)

The Channel Operating Margin (COM) for the channel between TP0 and TP5, computed using the procedure in 93A.1 and the parameters in Table 136–15, is recommended to be greater than or equal to the Channel Operating Margin (min.) value in Table 136–15 for the cable assembly type being used.

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Annex 136B

(normative)

Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M

136B.1 Test fixtures

Transmitter and receiver measurements at TP2 or TP3 for the 50GBASE-CR PHY in an SFP28 host form factor (see 136C.2.1), and at TP1a or TP4a for the 50GAUI-1 C2M host (see Annex 135G), are made utilizing the test fixture specified in 110B.1.1. Transmitter and receiver measurements at TP2 or TP3 for the 50GBASE-CR, 100GBASE-CR2 or 200GBASE-CR4 PHYs in a QSFP28 host form factor (see 136C.2.2), and at TP1a or TP4a for the 100GAUI-2 C2M host (see Annex 135G), are made utilizing the test fixture specified in 92.11.1.

Editor's Note: Return Loss and ICN for QSFP28 to be considered.

Cable assembly measurements for the SFP28-SFP28 form factor (see 136C.3.1) are made between TP1 and TP4 with cable assembly test fixtures as specified in 110B.1.2 on both ends. Cable assembly measurements for the QSFP28-QSFP28 form factor (see 136C.3.2) are made between TP1 and TP4 with cable assembly test fixtures as specified in 92.11.2 on both ends. Cable assembly measurements for the QSFP28-4×SFP28 form factor (see 136C.3.3) are made between TP1 and TP4 with a cable assembly test fixture as specified in 110B.1.2, for each connector on the SFP28 end, and with a cable assembly test fixture as specified in 92.11.2 for the QSFP28 end.

The test fixtures are specified in a mated state to enable connections to measurement equipment. The reference insertion loss of the mated test fixtures is 3.65 dB (see 136A.1). The requirements in the referenced subclauses are not the MDI connector specifications for an implemented design.

136B.1.1 Mated test fixtures

The TP2 or TP3 and cable assembly test fixtures are specified in a mated state illustrated in Figure 92–18. The mated test fixtures specifications are listed in 92.11.3.

136B.1.1.1 Mated test fixtures differential insertion loss

The differential insertion loss of the mated test fixtures shall meet the requirements of 92.11.3.1.

The FOM_{ILD} of the mated test fixtures shall meet the requirements of 92.11.3.1.

136B.1.1.2 Mated test fixtures differential return loss

The differential return loss of the mated test fixtures shall meet the requirements of 92.11.3.2.

136B.1.1.3 Mated test fixtures common-mode conversion insertion loss

The common-mode conversion insertion loss of the mated test fixtures shall meet the requirements of 92.11.3.3.

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136B.1.1.4 Mated test fixtures common-mode return loss

The common-mode return loss of the mated test fixtures shall meet the requirements of 92.11.3.4.

136B.1.1.5 Mated test fixtures common-mode to differential mode return loss

The common-mode to differential mode return loss of the mated test fixtures shall meet the requirements of 92.11.3.5.

136B.1.1.6 Mated test fixtures integrated crosstalk noise

The SFP28 mated test fixture integrated near-end crosstalk noise voltage for the disturber near-end crosstalk loss is determined according to the method in 110B.1.3.7 using the parameters shown in Table 136B–1 shall meet the specification in Table 110B–1.

Table 136B–1—Mated test fixture integrated near-end crosstalk noise parameters

Description	Symbol	Value	Units
Symbol rate	f_b	26.5625	GBd
3 dB reference receiver bandwidth	f_r	19.92	GHz
Near-end disturber peak differential output amplitude	A_{nt}	600	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	9.27	ps

The QSFP mated test fixtures integrated crosstalk RMS noise voltages determined using Equation (92–44) through Equation (92–48) for the multiple disturber near-end crosstalk loss, and the multiple disturber far-end crosstalk loss and shall meet the specifications in Table 92–13 using the parameters shown in Table 136B–2.

Table 136B–2—Mated test fixture integrated crosstalk noise parameters

Description	Symbol	Value	Units
Symbol rate	f_b	26.5625	GBd
3 dB reference receiver bandwidth	f_r	19.92	GHz
Near-end disturber peak differential output amplitude	A_{nt}	600	mV
Far-end disturber peak differential output amplitude	A_{ft}	600	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	9.27	ps
Far-end disturber 20% to 80% rise and fall times	T_{ft}	9.27	ps

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136B.2 Protocol implementation conformance statement (PICS) proforma for Annex 136B, Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M[21]

136B.2.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 136B, Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

136B.2.2 Identification

136B.2.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

136B.2.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Annex 136B, Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

[21] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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136B.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
HTF1	SFP28 TP2 or TP3 test fixture	110B.1.1		O	Yes [ ] No [ ]
HTF2	QSFP28 TP2 or TP3 test fixture	92.11.1		O	Yes [ ] No [ ]
CATF1	SFP28 Cable assembly test fixture	110B.1.2		O	Yes [ ] No [ ]
CATF2	QSFP Cable assembly test fixture	92.11.2		O	Yes [ ] No [ ]

136B.2.4 PICS proforma tables for test fixtures for Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Mated test fixtures insertion loss	136B.1.1.1	IL and FOM_{ILD} meet the requirements of 92.11.3.1	M	Yes [ ]
TF2	Mated test fixtures differential return loss	136B.1.1.2	Meets the requirements of 92.11.3.2	M	Yes [ ]
TF3	Mated test fixtures common-mode conversion insertion loss	136B.1.1.3	Meets the requirements of 92.11.3.3	M	Yes [ ]
TF4	Mated test fixtures common-mode return loss	136B.1.1.4	Meets the requirements of 92.11.3.4	M	Yes [ ]
TF5	Mated test fixtures common-mode to differential mode return loss	136B.1.1.5	Meets the requirements of 92.11.3.5	M	Yes [ ]
TF6	SFP28 Mated test fixtures integrated near-end crosstalk noise	136B.1.1.6	Meets the requirements of Table 110B–1	M	Yes [ ]
TF7	QSFP28 Mated test fixtures integrated near-end crosstalk noise	136B.1.1.6	Meets the requirements of Table 92–13	M	Yes [ ]

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Annex 136C

(informative)

Host and cable assembly form factors for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136C.1 Overview

This annex describes form factors for the three cable assemblies specified in 136.11 and for hosts with either 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4 Physical Layers.

Hosts have two specified MDI connectors, single-lane (SFP28, specified in 110.11.1) and multi-lane (QSFP28, specified in 92.13). This creates two host interface types and three cable assembly types with different combinations of the connectors at each end. These host and cable assembly types are referred to as form factors, distinguishing both the host receptacle (MDI) and the cable assembly plug.

Cable assemblies denoted as 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4, have a common set of electrical parameters specified in 136.11. These specifications are based on the 100GBASE-CR4 cable assembly specifications (see 92.10) with referenced parameters specified at 13.28 GHz to account for the increase in signaling rate.

The 50GBASE-CR is a single-lane cable assembly, enabling a 3 m length. The 100GBASE-CR2 is a two-lane cable assembly, enabling a 3 m length. The 200GBASE-CR4 is a four-lane cable assembly, enabling a 3 m length.

The possible combinations of host form factors, cable assembly form factors and lengths are summarized in Table 136C–1.

Table 136C–1—Host and cable assembly combinations

Cable assembly form factor	Host, first end	Hosts, second end
SFP28 to SFP28 (see 136C.3.1)	One, SFP28 form factor (see 136C.2.1)	One, SFP28 form factor (see 136C.2.1)
QSFP28 to QSFP28 (see 136C.3.2)	One, QSFP28 form factor (see 136C.2.2)	One, QSFP28 form factor (see 136C.2.2)
QSFP28 to 4×SFP28 (see 136C.3.3)	One, QSFP28 form factor (see 136C.2.1)	Four, SFP28 form factor (see 136C.2.1)

136C.2 Host form factors

136C.2.1 SFP28 host form factor

A host may use the SFP28 receptacle specified in 110.11.1 as the MDI for each 50GBASE-CR. This is referred to as an SFP28 host form factor.

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A SFP28 form factor host can form a single 50 Gb/s link to either another SFP28 form factor host, using an SFP28 to SFP28 form factor cable assembly (see 136C.3.1), or a QSFP28 form factor host (see 136C.2.2), using a QSFP28 to 4×SFP28 form factor cable assembly (see 136C.3.3).

136C.2.2 QSFP28 host form factor

A host may use the QSFP28 receptacle specified in 92.12 as the MDI for one or two 100GBASE-CR2 PHYs or one 200GBASE-CR4 PHY. This is referred to as a QSFP28 host form factor.

A QSFP28 form factor host can also form up to four 50 Gb/s links to either another QSFP28 form factor host, using a QSFP28 to QSFP28 form factor cable assembly (see 136C.3.2), or four separate SFP28 form factor hosts (see 136C.2.1) using a QSFP28 to 4×SFP28 form factor cable assembly (see 136C.3.3).

136C.3 Cable assembly form factors

136C.3.1 SFP28 to SFP28 cable assembly form factor

The SFP28 to SFP28 cable assembly has SFP28 plugs, specified in 110.11.1, on both ends. It may be used to connect two SFP28 form factor hosts (see 136C.2.1) with a single 50 Gb/s link. The cable assembly is illustrated in Figure 136C–1.

The electrical characteristics of a cable assembly for this form factor are specified in 136.11, using the definitions in 136.11.7.2.1.

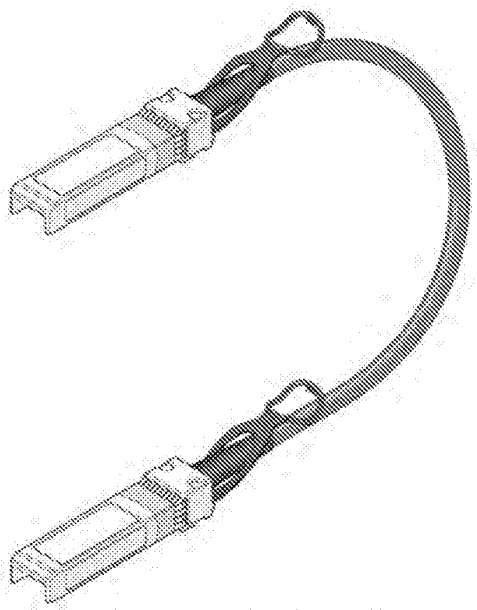


Figure 136C–1—SFP28 to SFP28 cable assembly

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136C.3.2 QSFP28 to QSFP28 cable assembly form factor

The QSFP28 to QSFP28 cable assembly has QSFP28 plugs, specified in 92.12, on both ends. It may be used to connect two QSFP28 form factor hosts (see 136C.2.2) with up to four 50 Gb/s links. The cable assembly is illustrated in Figure 136C–2.

The electrical characteristics of a cable assembly for this form factor are specified in 136.11, using the definitions in 136.11.7.2.4.

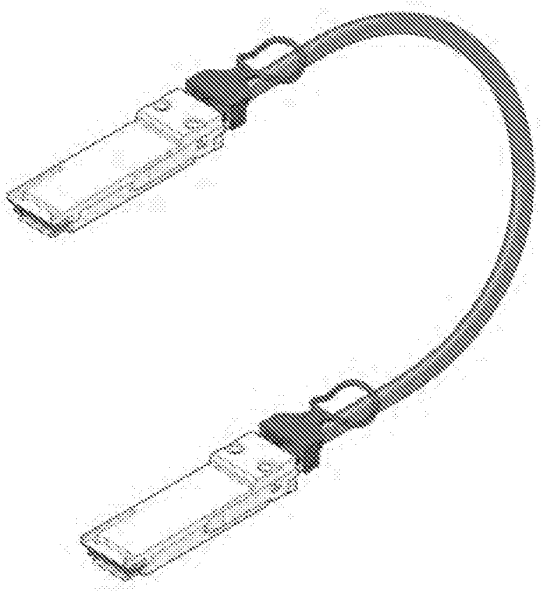


Figure 136C–2—QSFP28 to QSFP28 cable assembly

136C.3.3 QSFP28 to 4×SFP28 cable assembly form factor

The QSFP28 to 4×SFP28 cable assembly has a QSFP28 plug as specified in 92.12 on one end, and four SFP28 plugs as specified in 110.11.1 on the other end. It may be used to connect a QSFP28 form factor host (see 136C.2.2) to up to four SFP28 form factor hosts (see 136C.2.1) with one 50 Gb/s link to each SFP28 host. The cable assembly is illustrated in Figure 136C–3.

The electrical characteristics of a cable assembly for this form factor are specified in 136.11, using the definitions in 136.11.7.2.2 and 136.11.7.2.3.

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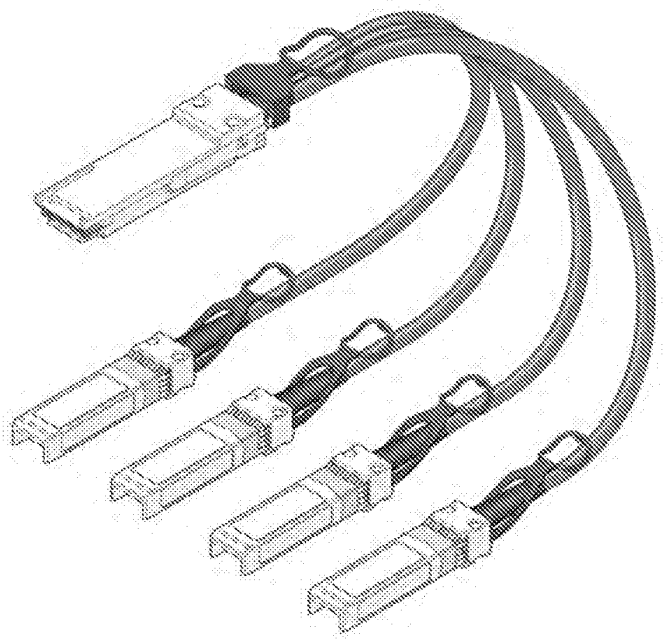


Figure 136C–3—QSFP28 to 4×SFP28 cable assembly

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CD Submission Review Results

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Assignment For Published Patent Application

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Power of Attorney: The patent practitioners associated with Customer Number 63467

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
CHINA 201910155535.9 03/01/2019 No Access Code Provided

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Marvell Semiconductor, Inc. - Ex. 1002, Page 000437

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 08/22/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/539,910**

Projected Publication Date: 09/03/2020

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

ACTIVE ETHERNET CABLE

Preliminary Class

439

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

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Marvell Semiconductor, Inc. - Ex. 1002, Page 000440

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/539,910

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	75		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	330		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	380		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*	x 50 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 230 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	785		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

To: uspto@rameyfirm.com,wramey@rameyfirm.com,tevenbly@rameyfirm.com
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 63467

Aug 26, 2019 03:40:14 AM

Dear PAIR Customer:

Ramey & Schwaller, LLP
5020 Montrose Blvd.
Suite 750
Houston, TX 77006
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 63467 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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Application	Document	Mailroom Date	Attorney Docket No.
16539910	APP.FILE.REC	08/26/2019	20160.0039.NPUS00

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

PLUS Search Results for S/N 16539910, Searched Tue Jan 07 08:49:19 EST 2020

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/539,910	08/13/2019	Yattung LAM	20160.0039.NPUS00	8175

63467 7590 03/11/2020

Ramey & Schwaller, LLP
Ramey & Schwaller
5020 Montrose Blvd.
Suite 800
Houston, TX 77006

EXAMINER
HA, DAC V

ART UNIT	PAPER NUMBER
2633	

NOTIFICATION DATE	DELIVERY MODE
03/11/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tevenbly@rameyfirm.com
uspto@rameyfirm.com
wramey@rameyfirm.com

Marvell Semiconductor, Inc. - Ex. 1002, Page 000444

Office Action Summary	**Application No.** 16/539,910	**Applicant(s)** LAM et al.	
	Examiner DAC V HA	**Art Unit** 2633	**AIA (FITF) Status** Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 08/13/19.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☑ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☑ Claim(s) 1-20 is/are allowed.

7) ☐ Claim(s) _____ is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 08/13/19 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☑ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

2. This application is in condition for allowance except for the following formal matters:

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in China on 03/01/19. It is noted, however, that applicant has not filed a certified copy of the China 201910155535.9 application as required by 37 CFR 1.55.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 25 USPQ 74, 453 O.G. 213, (Comm'r Pat. 1935).

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lett (US 2016/0197434)

Lin et al. (US 2018/0241579)

Zweig et al. (US 7,049,937)

Ward et al. (US 9,230,416)

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAC V HA whose telephone number is (571)272-3040. The examiner can normally be reached on 7-3:30 M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sam Ahn can be reached on 571-272-3044. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DAC V HA/
Primary Examiner, Art Unit 2633

Notice of References Cited	Application/Control No. 16/539,910	Applicant(s)/Patent Under Reexamination LAM et al.	
	Examiner DAC V HA	Art Unit 2633	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20160197434-A1	07-2016	Lett; David B.	H01R13/516	348/373
*	B	US-20180241579-A1	08-2018	Lin; Chun-En	H04L12/10	1/1
*	C	US-7049937-B1	05-2006	Zweig; Jonathan M.	H01R13/641	324/66
*	D	US-9230416-B2	01-2016	Ward; Rafik	G08B5/00	1/1
	E					
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/539,910	LAM et al.
	Examiner	Art Unit
	DAC V HA	2633

CPC - Searched*		
Symbol	Date	Examiner
H04L 12/2801; H04L 25/4917; H04L 25/03885	03/06/2020	DH

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

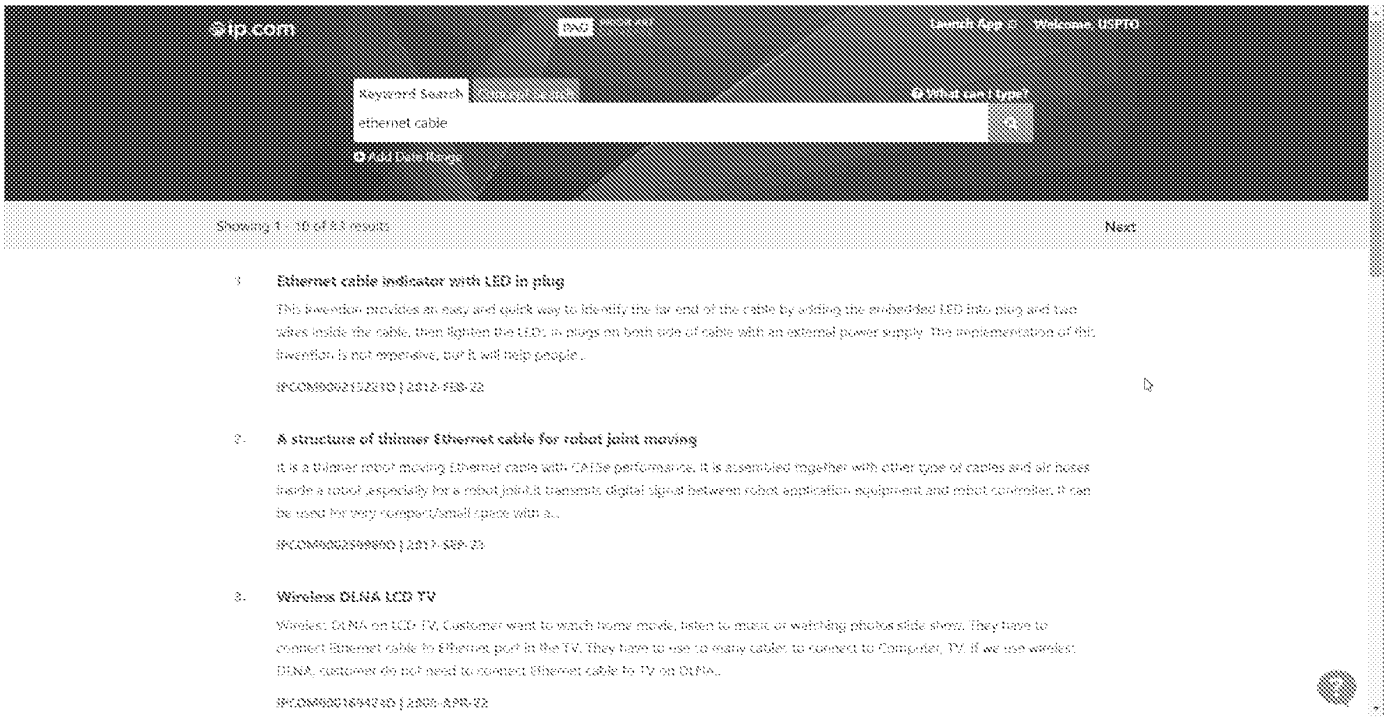
US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
BRS and Inventor's search	03/06/2020	DH
PLUS	03/06/2020	DH
NPL	03/06/2020	DH

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	PGPUB	03/06/2020	DH

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ip.com
Keyword Search
ethernet cable
Showing 1 - 10 of 83 results
Next
1. Ethernet cable indicator with LED in plug
This invention provides an easy and quick way to identify the far end of the cable by adding the embedded LED into plug and two wires inside the cable, then lighten the LEDs in plugs on both side of cable with an external power supply. The implementation of this invention is not expensive, but it will help people ...
IPCOM000021220D | 2012-Feb-22
2. A structure of thinner Ethernet cable for robot joint moving
It is a thinner robot moving Ethernet cable with CAT5e performance. It is assembled together with other type of cables and air hoses inside a robot, especially for a robot joint.It transmits digital signal between robot application equipment and robot controller. It can be used for very compact/small space with a...
IPCOM000239990D | 2017-Sep-25
3. Wireless DLNA LCD TV
Wireless DLNA on LCD TV. Customer want to watch home movie, listen to music or watching photos slide show. They have to connect Ethernet cable to Ethernet port in the TV. They have to use so many cables to connect to Computer, TV. If we use wireless DLNA, customer do not need to connect Ethernet cable to TV on DLNA...
IPCOM000216940D | 2008-Apr-22

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	Yattung LAM
Art Unit	
Examiner Name	
Attorney Docket Number	20160.0039.NPUS00

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	9,322,704	B1	2016-04-26	Neveux	
	2	7,401,985	B2	2008-07-22	Aronson, et al	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	1							

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.V.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Yattung LAM
	Art Unit	
	Examiner Name	
	Attorney Docket Number	20160.0039.NPUS00

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Rumer, B. "Fighting Jitter in Fibre-Channel Designs." Electronic Engineering Times, (2001, February 01). Retrieved August 13, 2019, from https://www.eetimes.com/document.asp?doc_id=1277249	
	2	IEEE P802.3cd/D1.2, 3rd February 2017 (Amendment of IEEE Std 802.3-2015 as amended) IEEE Draft Standard for Ethernet Amendment: Media Access Control Parameters for 50 Gb/s, 100 Gb/s and 200 Gb/s Operation. The Institute of Electrical and Electronics Engineers, Inc., 2017; S.l.: IEEE.	

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EXAMINER SIGNATURE

Examiner Signature	/DAC V HA/	Date Considered	01/15/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.V.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Application Number	
	Filing Date	
	First Named Inventor	Yattung LAM
	Art Unit	
	Examiner Name	
	Attorney Docket Number	20160.0039.NPUS00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Daniel J. Krueger/	Date (YYYY-MM-DD)	2019-08-13
Name/Print	Daniel J. Krueger	Registration Number	42,771

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.V.H/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.V.H/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	706	(ethernet with (link cable)) same (electrica$4 near2 conduct$4)	US-PGPUB; USPAT	OR	ON	2020/03/06 13:34
L5	458	4 and (connect$4 with (transceiv$4 transmit$4 receiv$4))	US-PGPUB; USPAT	OR	ON	2020/03/06 13:34
L6	24	5 and (cdr (clock near3 recover$4))	US-PGPUB; USPAT	OR	ON	2020/03/06 13:35
L7	24	6 and modulat$4	US-PGPUB; USPAT	OR	ON	2020/03/06 13:35
L8	6020	(h04L12/2801 H04L25/4917 h04L25/03885).cpc.	US-PGPUB; USPAT	OR	ON	2020/03/06 13:35
L9	0	7 and L8	US-PGPUB; USPAT	OR	ON	2020/03/06 13:35
L10	81	5 and (ethernet with (link cable)) .clm.	US-PGPUB; USPAT	OR	ON	2020/03/06 13:40
L11	75	10 not 7	US-PGPUB; USPAT	OR	ON	2020/03/06 13:41
L12	50	11 and (pair with (wire twist$4 conduct$4))	US-PGPUB; USPAT	OR	ON	2020/03/06 13:42
L13	24	("2014/0258742").URPN.	USPAT	OR	ON	2020/03/06 13:43
L14	244	g02b6/36.cpc.	USPAT	OR	ON	2020/03/06 13:56
L15	0	4 and 14	USPAT	OR	ON	2020/03/06 13:56
L16	9	14 and ethernet	USPAT	OR	ON	2020/03/06 13:56
L17	89	("20020031955" | "20020048990" | "20030031025" | "20030157842" | "20030199192" | "20030222786" | "20040038564" | "20040160774" | "20050037672" | "20050224585" | "20060134996" | "20060162947" | "20060232385" | "20070105453" | "20070116411" | "20070190863" | "20080020658" | "20080122579" | "20090042431" | "20090269973" | "20100079248" | "20100098425" | "20110043333" | "20110116748" | "20120058689" | "20120064750" |	US-PGPUB; USPAT; USOCR	OR	ON	2020/03/06 13:57

Marvell Semiconductor, Inc. - Ex. 1002, Page 000455

		"20130052860" | "20140035755" | "20160020975" | "20170293102" | "3960428" | "4761720" | "4837488" | "5159316" | "5666453" | "5741152" | "5764043" | "5888100" | "6002331" | "6080007" | "6099345" | "6244908" | "6280232" | "6394853" | "6524128" | "6532328" | "6558204" | "6577243" | "6790096" | "6798183" | "6811445" | "6975242" | "7049937" | "7080945" | "7081808" | "7168994" | "7221284" | "7335066" | "7374458" | "7547150" | "7549886" | "7556536" | "7651361" | "7760094" | "7772975" | "7782202" | "7910833" | "7910834" | "7920764" | "7940182" | "7960648" | "7965186" | "7972183" | "8043124" | "8210755" | "8264355" | "8277260" | "8465317" | "8606972" | "8611234" | "8620123" | "8702453" | "8747141" | "9196975" | "9230416" | "9577904" | "9810859" | "9952258" | "9995432").PN.				
L18	17	17 and ethernet	USPAT	OR	ON	2020/03/06 13:57
S1	6018	(h04L12/2801 H04L25/4917 h04L25/03885).cpc.	US-PGPUB; USPAT	OR	ON	2020/03/03 16:46
S2	21	((yattung near1 lam) (baohua near1 chen)).in.	US-PGPUB; USPAT	OR	ON	2020/03/03 16:46
S4	0	S2 and ethernet.clm.	US-PGPUB; USPAT	OR	ON	2020/03/03 16:48
S5	2	S2 and cable.clm.	US-PGPUB; USPAT	OR	ON	2020/03/03 16:48
S6	1632	(ethernet near2 cable).ab,clm.	US-PGPUB; USPAT	OR	ON	2020/03/04 12:01
S7	1501	S6 and (ethernet near2 cable).clm.	US-PGPUB; USPAT	OR	ON	2020/03/04 12:01
S8	224	S7 and (ethernet near2 cable).ab.	US-PGPUB; USPAT	OR	ON	2020/03/04 12:01
S9	45	S8 and ((ethernet near2 cable) same transceiv$4)	US-PGPUB; USPAT	OR	ON	2020/03/04 12:02
S10	6018	(h04L12/2801 H04L25/4917 h04L25/03885).cpc.	US-PGPUB; USPAT	OR	ON	2020/03/04 12:02
S11	3	S9 and S10	US-PGPUB; USPAT	OR	ON	2020/03/04 12:02
S12	42	S9 not S11	US-PGPUB; USPAT	OR	ON	2020/03/04 12:09
S13	158	S8 and ((ethernet near2 cable) with (coupl$4 connect))	US-PGPUB;	OR	ON	2020/03/04 12:15

Marvell Semiconductor, Inc. - Ex. 1002, Page 000456

			USPAT			
S14	120	S13 not S9	US-PGPUB; USPAT	OR	ON	2020/03/04 12:16
S15	0	S14 and (cdr (clock near3 recover$4))	US-PGPUB; USPAT	OR	ON	2020/03/04 12:17
S16	16	S14 and (ethernet near2 cable).ti.	US-PGPUB; USPAT	OR	ON	2020/03/04 12:19
S17	11	("2017/0346200").URPN.	USPAT	OR	ON	2020/03/04 12:21
S18	104	S14 not S16	US-PGPUB; USPAT	OR	ON	2020/03/04 12:23
S19	66	S8 not S13	US-PGPUB; USPAT	OR	ON	2020/03/04 12:33
S20	15	S19 and ((ethernet near2 cable) with (standard$5))	US-PGPUB; USPAT	OR	ON	2020/03/04 12:34
S21	2	("9322704" "7401985").pn.	US-PGPUB; USPAT	OR	ON	2020/03/04 13:30
S22	77	("7401985").URPN.	USPAT	OR	ON	2020/03/04 13:31
S23	78	("20010035994" | "20020018609" | "20020044746" | "20020049879" | "20020063935" | "20020114590" | "20020136510" | "20020149821" | "20020159725" | "20020160656" | "20030016920" | "20030021580" | "20030034963" | "20030208779" | "20030223756" | "20040008996" | "20040076119" | "20040141695" | "20040184746" | "20040208600" | "20040263941" | "20050036746" | "20050053340" | "20050063707" | "20050063711" | "20050078916" | "20050105910" | "20050105915" | "20050180700" | "20050238358" | "20050249477" | "20050286593" | "20050286893" | "20060008276" | "20060036788" | "20060045437" | "20060049936" | "20060067690" | "20060077778" | "20060083518" | "20060088251" | "20060093280" | "20060142744" | "4427879" | "4768188" | "4902092" | "5337398" | "5497187" | "5515467" | "5530787" | "5631988" | "5668419" | "5732176" | "5926303" | "6036654" | "6179627" | "6217231" | "6220873" | "6267606" | "6446867" | "6458619" | "6461059" | "6478625" | "6502997" | "6540412" | "6607307" | "6758693" | "6774348" | "6793539" | "6905257" | "6914637" | "6941395" | "6952395" | "6965722" | "7065604" | "7088518" | "7162130" | "7217022").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2020/03/04 13:31
S24	1	S21 and (modulat$5 clock$4)	US-	OR	ON	2020/03/04

Marvell Semiconductor, Inc. - Ex. 1002, Page 000457

			PGPUB; USPAT			13:46
S25	381	cable.ab. and cable.clm. and (ethernet near1 port)	USPAT	OR	ON	2020/03/04 13:56
S26	372	S25 and (transceiv$4 transmit$4 receiv$4)	USPAT	OR	ON	2020/03/04 13:56
S27	7	S26 and (cdr (clock near3 recover$4))	US-PGPUB; USPAT	OR	ON	2020/03/04 13:56
S29	4	S27 and modulat$4	US-PGPUB; USPAT	OR	ON	2020/03/04 13:57
S30	142	S26 and modulat$4	US-PGPUB; USPAT	OR	ON	2020/03/04 13:57
S31	500	(active with ethernet with cable)	US-PGPUB; USPAT	OR	ON	2020/03/04 13:58
S32	7	S25 and S31	US-PGPUB; USPAT	OR	ON	2020/03/04 13:58
S33	217	S31 and (transceiv$4 transmit$4 receiv$4)	USPAT	OR	ON	2020/03/04 13:59
S34	55	S33 and (ethernet near1 port)	USPAT	OR	ON	2020/03/04 13:59
S36	48	S34 not S32	US-PGPUB; USPAT	OR	ON	2020/03/04 14:01
S37	500	(active with ethernet with cable)	US-PGPUB; USPAT	OR	ON	2020/03/05 07:53
S38	200	S37 and modulat$4	US-PGPUB; USPAT	OR	ON	2020/03/05 07:53
S39	11	S38 and (cdr (clock near3 recover$4))	US-PGPUB; USPAT	OR	ON	2020/03/05 07:53
S41	8639810	s "37"(ethernet with cable).clm.	US-PGPUB; USPAT	OR	ON	2020/03/05 16:32
S42	500	(active with ethernet with cable)	US-PGPUB; USPAT	OR	ON	2020/03/05 16:32
S43	67	S42 and (ethernet with cable).clm.	US-PGPUB; USPAT	OR	ON	2020/03/05 16:32

3/6/2020 2:01:34 PM
C:\Users\dha\Documents\EAST\Workspace2\16539910.wsp

Marvell Semiconductor, Inc. - Ex. 1002, Page 000458

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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BIB DATA SHEET

CONFIRMATION NO. 8175

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
16/539,910	08/13/2019 **RULE**	375	2633	20160.0039.NPUS00

APPLICANTS
CREDO TECHNOLOGY GROUP LIMITED, Grand Cayman, CAYMAN ISLANDS;

INVENTORS
Yattung LAM, San Jose, CA;
Baohua CHEN, Xiamen City, CHINA;

** **CONTINUING DATA** *************************

** **FOREIGN APPLICATIONS** *************************
CHINA 201910155535.9 03/01/2019

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** ** ** SMALL ENTITY **
08/22/2019

		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed ☑ Yes ❑ No 35 USC 119(a-d) conditions met ❑ Yes ☑ No Verified and Acknowledged /DAC V HA/ Examiner's Signature	❑ Met after Allowance Initials	CA	4	20	3

ADDRESS

Ramey & Schwaller, LLP
Ramey & Schwaller
5020 Montrose Blvd.
Suite 800
Houston, TX 77006
UNITED STATES

TITLE

ACTIVE ETHERNET CABLE

FILING FEE RECEIVED 785	FEES: Authority has been given in Paper No.____________ to charge/credit DEPOSIT ACCOUNT No.____________ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other ________________ ❑ Credit

BIB (Rev. 05/07).

To: uspto@rameyfirm.com,wramey@rameyfirm.com,tevenbly@rameyfirm.com
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 63467

Mar 11, 2020 03:34:52 AM

Dear PAIR Customer:

Ramey & Schwaller, LLP
Ramey & Schwaller
5020 Montrose Blvd.
Suite 800
Houston, TX 77006
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 63467 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
16539910	CTEQ	03/11/2020	20160.0039.NPUS00
	892	03/11/2020	20160.0039.NPUS00
	1449	03/11/2020	20160.0039.NPUS00

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If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

Doc Code: PD.REQ.RETR
Document Description: Request for USPTO to retrieve priority docs

PTO/SB/38 (02-20)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Request to Retrieve Electronic Priority Application(s)

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

COMPLETE IF KNOWN	
Application Number	16/539,910
Filing Date	August 13, 2019
First Named Inventor	Yattung, LAM
Art Unit	2633
Examiner Name	HA, Dac V
Attorney Docket Number	20160.0039.NPUS00

Pursuant to 37 CFR 1.55(i), the undersigned hereby requests that the USPTO retrieve an electronic copy of each of the following foreign applications for which priority has been claimed under 35 U.S.C. 119(a)-(d) from a foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement. This Request must be submitted:

- within the later of sixteen months from the filing date of the prior foreign application or four months from the actual filing date of an application under 35 U.S.C. 111(a),
- within four months from the later of the date of commencement (37 CFR 1.491(a)) or the date of the initial submission under 35 U.S.C. 371 of an application entering the national stage under 35 U.S.C. 371, or
- with a petition under 37 CFR 1.55(e) or (f).

☐ **OPTION A**

Please retrieve the priority application identified in Column C, a certified copy of which is contained in the EP or JP application identified in Columns A and B:

	A	B			C	
	Code for Participating Office (EP or JP only)	Application containing the non-participating priority application			Non-participating priority application to be retrieved	
		App. No.	Filing Date	Access Code (for JP only)	Country Code	App. No.
1						

☑ **OPTION B**

This Request may be used for the infrequent circumstance when a claim for priority to an application filed in a participating foreign intellectual property office was made prior to that foreign intellectual property office becoming a participating foreign intellectual property office.

Please retrieve the priority application identified in Columns A and B:

	A	B		
	Code for Participating Office (e.g., EP) or WIPO DAS Depositing Office (e.g., AU, BR, CN, DK, EA, EE, ES, FI, GB, IB, IN, JP, KR, MA, NL, NZ, SE)	Application to be retrieved		
		App. No.	Filing Date	Access Code (for WIPO DAS Depositing Office)
1	CN	201910155535.9	2019-03-01	008D
2				

The USPTO will not attempt to retrieve the identified priority application(s) unless an identical claim for foreign priority to the application identified above is made pursuant to 37 CFR 1.55(d) or a petition is granted under 37 CFR 1.55(e) or (f). Applicants are advised to consult Private PAIR (accessed through www.uspto.gov) to assure that the retrieval has been successful. The applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period set forth in 37 CFR 1.55(g)(1).

I hereby declare that I have the authority to grant access to the above-identified foreign application(s).

/Dan Krueger/	March 24, 2020
Signature	Date
Daniel J. Krueger	713-426-3923
Printed or Typed Name	Telephone Number
Attorney of Record	42771
Title	Registration Number, if applicable

This collection of information is required by 37 CFR 1.55(d). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 8 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	38951907
Application Number:	16539910
International Application Number:	
Confirmation Number:	8175
Title of Invention:	ACTIVE ETHERNET CABLE
First Named Inventor/Applicant Name:	Yattung LAM
Customer Number:	63467
Filer:	Daniel Joseph Krueger/Shanay Hines
Filer Authorized By:	Daniel Joseph Krueger
Attorney Docket Number:	20160.0039.NPUS00
Receipt Date:	24-MAR-2020
Filing Date:	13-AUG-2019
Time Stamp:	13:32:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2020-03-24_FINAL-ADS.pdf	135498 41da1bf9cb7269e851ece0419a358167d8c5eebc	no	8

Warnings:

Information:					
This is not an USPTO supplied ADS fillable form					
2	Request for USPTO to retrieve priority docs	2020-03-24_Request_to_Retrieve_Priority_Application.pdf	278829 b0571693c0d213a55003448c64e36299421a9bf5	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	414327	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (02-18)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	20160.0039.NPUS00
	Application Number	16/539,910
Title of Invention	ACTIVE ETHERNET CABLE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
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Postal Code		Country	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	20160.0039.NPUS00
	Application Number	16/539,910
Title of Invention	ACTIVE ETHERNET CABLE	

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	63467		
Email Address	uspto@rameyfirm.com	Add Email	Remove Email

Application Information:

Title of the Invention	ACTIVE ETHERNET CABLE		
Attorney Docket Number	20160.0039.NPUS00	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	2

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	63467		