

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Marvell Semiconductor, Inc,

Petitioner,

v.

Credo Technology Group Ltd.,

Patent Owner.

Case No. IPR2025-01219

U.S. Patent 11,012,252

Declaration of Michael S. Chen

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I, Michael Shuo-Wei Chen, declare as follows:

1. My name is Michael Shuo-Wei Chen. I am a Professor in the Department of Electrical Engineering at the University of Southern California. A summary of my background and qualifications can be found in §VI below. My full Curriculum Vitae is attached to this declaration as Appendix 1.

2. I have prepared this report as an expert witness retained by Marvell Semiconductor, Inc. In this report I give my opinions as to whether certain claims of U.S. Patent No. 11,012,252 (“the ’252 patent”) are invalid. I provide technical bases for these opinions as appropriate.

3. This report contains statements of my opinions formed to date and the bases and reasons for those opinions. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses. I make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained herein.

I. OVERVIEW OF THE TECHNOLOGY

4. High-speed serial communications became popular and widespread in the 1990s. In contrast to parallel architectures where multiple lines send different data signals, serial communications send a single signal down a single channel. As transmission speeds increased, parallel buses reached their limits due to limitations

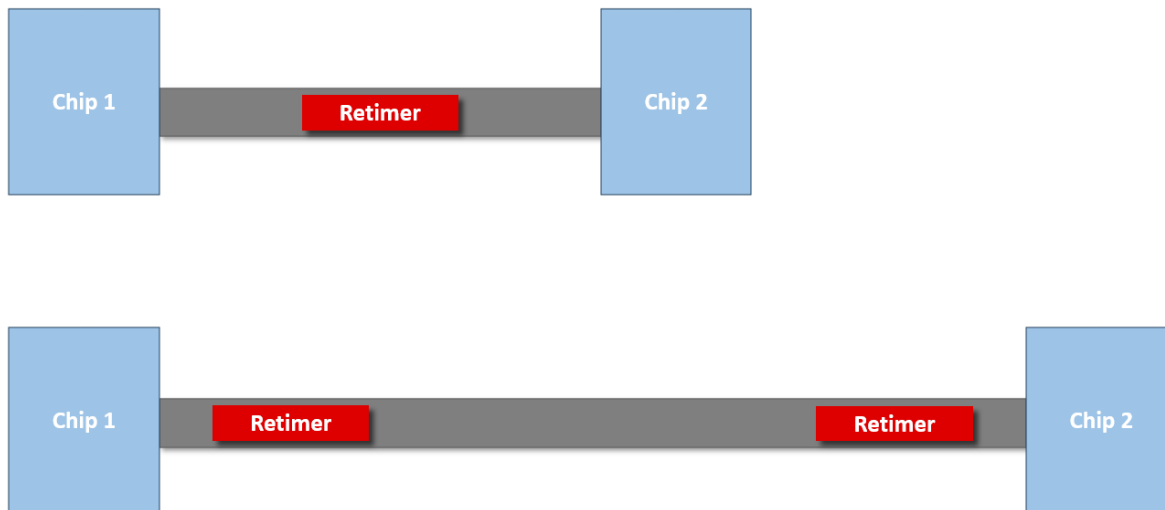
from having to route numerous data lines next to each other (in parallel) along with clock signals. Ex-1020, 000011-12. Parallel signals needed to be synchronized so that all signals and their shared clock arrived at the receiver within a certain window, which became increasingly difficult as bus widths and clock speeds increased. *See* Ex-1020, 000011-14. Serial communications techniques avoid these issues while saving pin count on the integrated circuit (“IC”).

5. By the 2000-2005 timeframe, computer bus and networking protocols had largely transitioned to serial connections, where parallel data within a chip was converted into a serial format, sent over a serial link, and then converted back into a parallel format. This process of serialization and then de-serialization, called “SerDes,” was used in various standardized bus and networking protocols. For example, the parallel ATA standard was replaced by Serial ATA, or “SATA” for short. The parallel PCI standard was replaced by a serial version called PCIe. The Universal Serial Bus (“USB”) replaced various parallel interfaces. And the ubiquitous Ethernet standard had long been implemented using serial cables and CAT-5 plugs. Ex-1020, 000058-61.

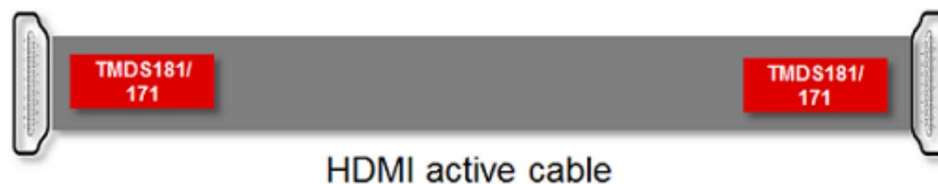
A. Active Cables

6. In serial communications, retimers were often used to extend the length and bandwidth of serial communications links by recovering digital bits from the channel and re-modulating them, eliminating noise from the earlier

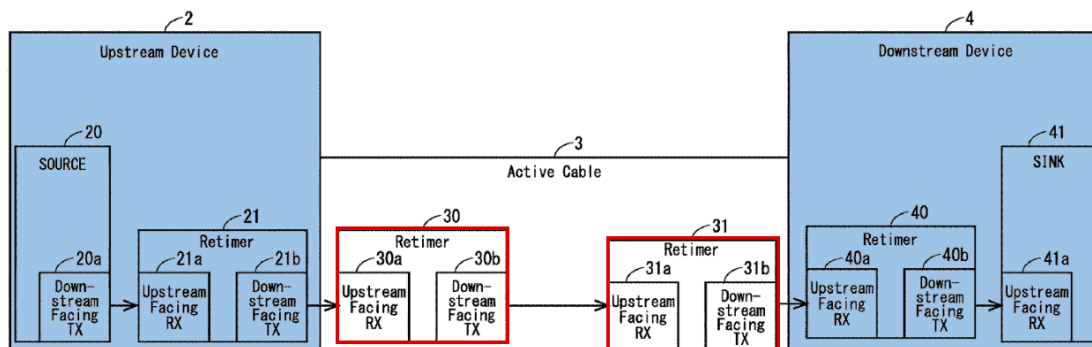
segment of a link and renewing the signal for the next. Ex-1007, ¶¶15-16, ¶202. I prepared the following diagrams to illustrate how retimers were used to extend the length of channels between chips:



7. Active electric cables extended the length of cables by incorporating retimers in the plugs at each end of a cable. Ex-1010, ¶2 (“A retimer is used to extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the retimer.”), ¶13 (“an active cable may have two retimers on both ends of the cable”). For example, Texas Instruments (“TI”) provided a retimer chip (TMDS181) that was included in active HDMI cables. Ex-1026, Fig.1:



Active electric cables commonly included a retimer at each end of the cable. Ex-1010, Fig.1:¹



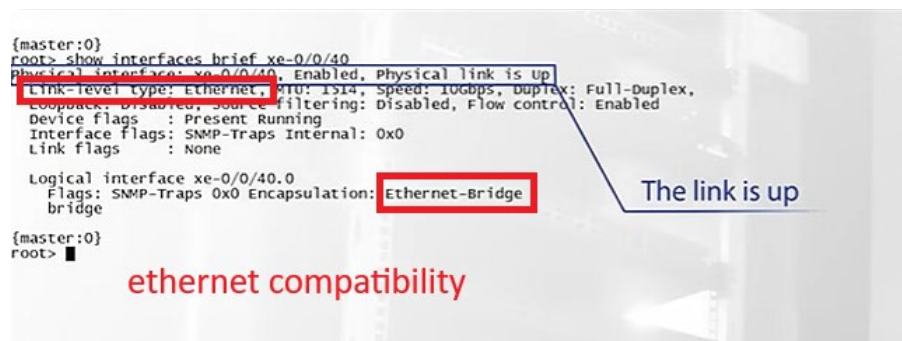
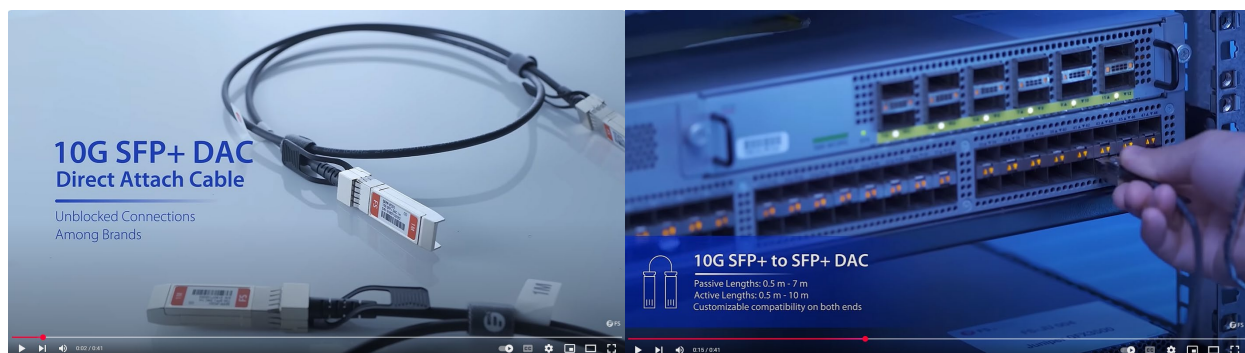
By the early-to-mid 2010s, active cables were used for a variety of common data transmission standards, including DisplayPort, PCIe, USB, and Ethernet.

8. Ethernet was a popular networking standard going back to the 1990s. By the 2010s, Ethernet was widely used for high-speed serial communications in enterprise and data-center networks, scaling from 1 Gigabit Ethernet (GbE) in the early 2000s to the widespread adoption of 10 GbE by 2010. To meet industry demand for higher speeds and longer reach, manufacturers introduced active Ethernet cables, which integrated electronics such as retimers within the cable assembly. Active Ethernet cables have been available on the market from a variety of vendors by at least 2014. *See* Ex-1011 (datasheet for 1/10 Gbit Ethernet TE SFP+ cables); Ex-1012, 000001, 000003, 000004-5, 000008-9 (various 40 Gbit

¹ All emphasis and annotations added unless stated otherwise.

Ethernet Cisco transceiver and cable modules). Petitioner Marvell is a leading supplier of transceiver chips for active Ethernet cables.

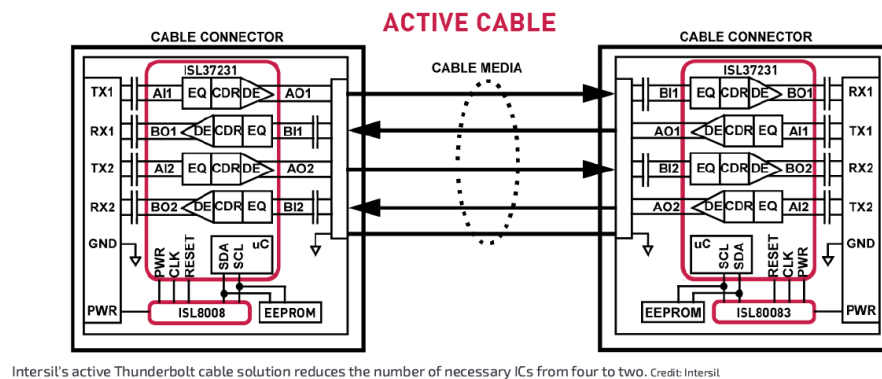
9. Some active Ethernet cables, shown below, use the SFP+ form factor, with a transceiver in a module at both ends. Ex-1019,² Video Description (“10G SFP+ direct attach copper cable...or 10G SFP+ DAC cable assembly, is a twinaxial cable assembly that has a length of copper cable and terminates with SFP+ connector modules on either end.”), 000001, 000002, 000004:



10. One high-profile active cable, called Thunderbolt, came from a collaboration between Apple and Intel. Apple developed and marketed the cable

² I created exhibit 1019 by visiting <https://youtu.be/IeI2DIE4QhQ?si=MERK3x9eFo6FLkUG> and taking screen captures at times 0:02, 0:15, and 0:29. I added annotations in red to the screen capture at time 0:29.

(Ex-1014, 000002; Ex-1013, 000001-2), while Intel provided the port and retimer architectures used in the connector assemblies at each end of the cable. Ex-1016, 000001-2; Ex-1015, 000003 (“Thunderbolt port and controller specification are entirely Intel’s”). Mac computers included Thunderbolt ports starting in 2011 (Ex-1013, 000001), and other vendors began providing Thunderbolt solutions by 2013. Ex-1009, 000001 (describing Intersil retimer chip for Thunderbolt), Ex-1008, 000002-3 (discussing Intersil retimers in Thunderbolt connectors):



B. Equalization

11. As connection protocols shifted to serial links, they adopted established serial communications techniques. One widely used technique was equalization, commonly found in active cables and retimers.
12. Equalization was a well-established serial communication technique. By 2019, and for many years prior, it was one of several common components taught in undergraduate courses on high-speed serial communications. Ex-1020, 000020-24. Textbooks on serial communications typically included a chapter or

section explaining pre-equalization. Ex-1020, 000020-24; Ex-1017, §§1.1.1-1.1.2 at 000025-29.

13. Equalization was performed at the transmitter (“pre-equalization”) to adjust the signal before it was sent over the channel, to compensate for anticipated signal loss. Equalization was also performed at the receiver to adjust for channel losses after the signal crossed the channel. *E.g.*, Ex-1007, Fig.34:

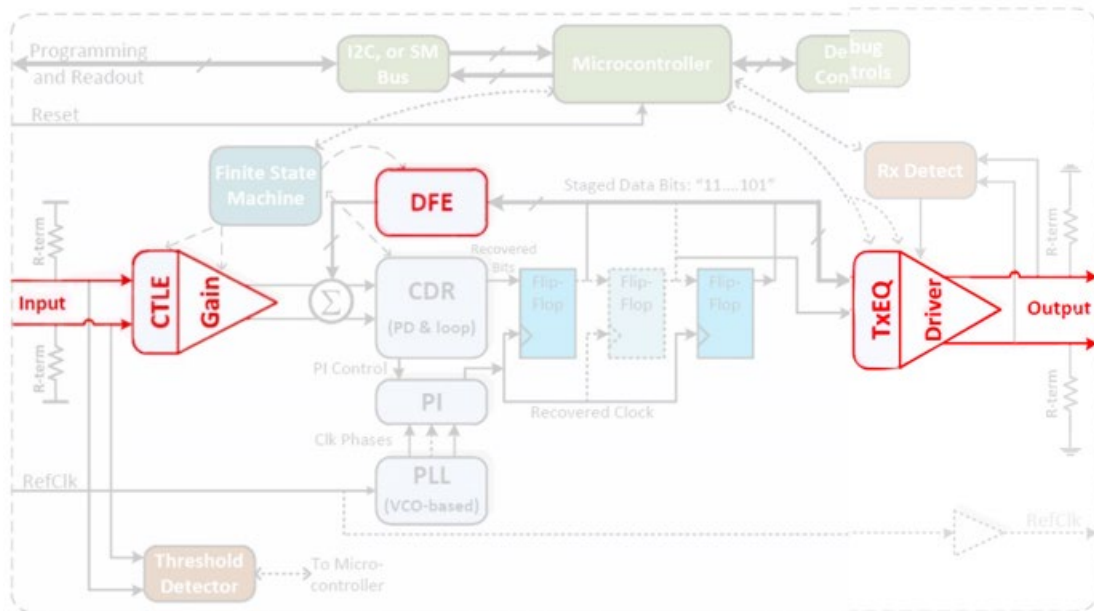


Figure 34 Conceptual micro-architecture of a “Bit Re-timer”, showing input CTLE, AGC, DFE, a CDR, and a data path connected directly to an output driver with TxEQ.

The use of equalization at both sides allowed robust and reliable transmission over noisy channels and at high data rates. Ex-1020, 000020-24.

14. Because a channel affects different frequencies unevenly, pre-equalization boosts the signal at frequencies where greater losses were expected. This compensation counteracted channel losses, so that after traversing the

channel, the received signal more closely matched the original. Ex-1020, 000020-24. The resulting signal at the receiver had a signal spectrum more constant over frequency, resulting in less waveform distortion and reduced inter-symbol interference (“ISI”). Pre-equalization was most commonly performed using “pre-emphasis” to boost certain frequencies; it is illustrated below, where the red boxes show the original waveform without and with pre-emphasis, and the waveforms on the right show the result after passing through the channel. Ex-1020, Figs.1.9-1.10 at 000021:

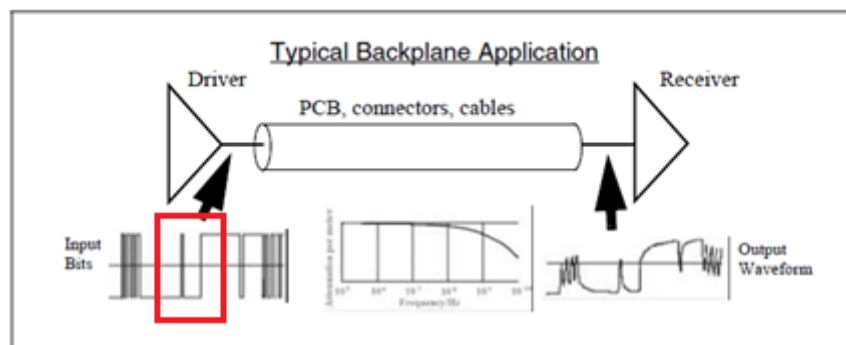


Fig. 1.9 Signal distortion for a typical channel application

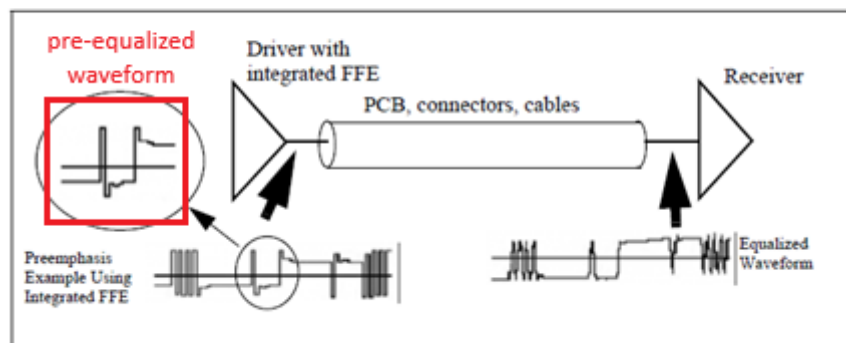


Fig. 1.10 Typical channel application with equalization at the transmitter

15. Equalization was often implemented using a finite impulse response (“FIR”) filter. An FIR filter essentially performs a weighted sum between adjacent

data symbols by multiplying coefficients with adjacent data (also called “taps”) and summing the results. For equalization, the FIR filter coefficients were chosen to boost frequencies that the channel diminishes. This way, when the signal goes through both the filter and the channel, their effects cancel out, helping the signal reach the receiver closer to its original form. Typically, the FIR filter provides more signal gain at higher frequency (so-called pre-emphasis) or attenuates the signal more at lower frequency (so-called de-emphasis) to compensate for the frequency-dependent channel loss. Ex-1020, 000020-21; Ex-1017, 000025-27. These filter coefficients were parameters that controlled the behavior of the equalization filter.

16. In the area of wireline communication, data (typically in the form of digital binary bits: “0” or “1”) is conveyed from one end (transmitting end) to the other end (receiving end) via a physical channel, such as a cable or a trace on a printed circuit board (“PCB”). For example, “0” can be conveyed using low voltage, while “1” can be conveyed using high voltage. If the physical channel is perfect without any loss, the receiver simply needs to detect whether the received voltage level is above or below a certain threshold to recover the transmitted bits. However, in practice, physical channels are not perfect and include various loss mechanisms, such as parasitic resistance, capacitance, skin effects, dielectric loss,

connectors, vias, etc., which attenuate and distort signals transmitted through the physical channel.

17. If such a channel loss were strictly constant over frequency, the lost signal energy would result in smaller signal swing at the receiving end but the transmitted signal waveform can be retained. However, in reality, the channel loss is frequency dependent and can cause distorted signal waveform at the receiving end and interference between data symbols, resulting in inter-symbol interference (“ISI”). Ex-1020, 000072 (“This type of jitter [DDJ], also known as pattern dependent jitter or intersymbol interference (ISI), is observed on nonclocklike waveforms since the frequency spectrum of such signals is continually changing.” “[H]igh baud rates still expose these signals to a significant amount of signal attenuation resulting in DDJ contribution.”), 000071-75. The ISI effect can cause the received waveform smeared to anywhere between the high and low voltage. Sometimes, the supposedly high voltage may be attenuated to a much lower voltage. As a consequence, the receiver is unable to detect the intended data reliably and can cause bit error (i.e. detected as “0” while the transmitted data is “1” and vice versa), often characterized as bit error rate (BER).

18. It was common to use fixed, “pre-programmed or pre-set” values for the equalization parameters (e.g., coefficients) based on a pre-determined, estimated channel response. Ex-1021, 7:18-33, 1:65-67 (FIR filter “typically

includes a one or more taps having fixed or pre-programmed...coefficients.”); Ex-1020, 000020-21 (“FFE tap weights are determined for many applications by design and coded as fixed values....”), Ex-1007, ¶227 (explaining microcontroller “receive[s] any external presets (or user configurations)” for the retimer). Programming fixed values was the simplest approach to designing software or hardware.

19. On the other side of the channel, equalization was used at the receiver to further adjust for channel loss. Some popular equalizers at the receiver end included continuous time linear equalization (CTLE), Feedforward Equalizers (FFE) and Decision Feedback Equalizers (DFE). Like pre-equalization at the transmitter, receiver-based equalization also compensated for the channel loss by equalizing the frequency response distortion of the channel. Having equalization at both the transmitter and receiver reduced the load at any one location by counterbalancing the channel’s effects at two points instead of one. Because transmitted signals passed through the transmitter, physical channel and then the receiver, the effects of the channel were compensated by the cumulative equalization at the transmitter and receiver. Therefore, receiver equalization was useful when transmitter pre-equalization alone was insufficient, or when actual channel loss varied beyond what the transmitter pre-equalizer anticipated.

20. Retimers generally included equalization on their receiver interfaces and pre-equalization on their transmitter interfaces. Ex-1007, ¶215, ¶220, ¶224-225, Figs.34-35; Ex-1009, 000007, Fig.1; Ex-1004, 12:58-67, Fig.1D:

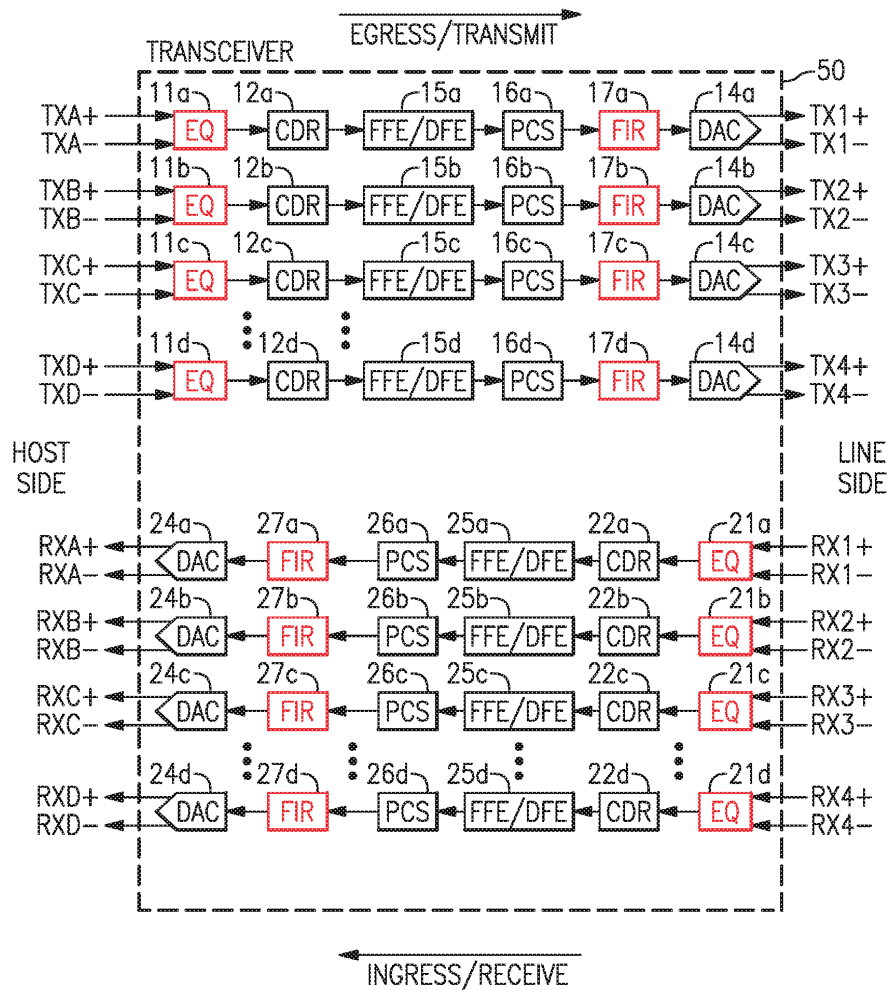


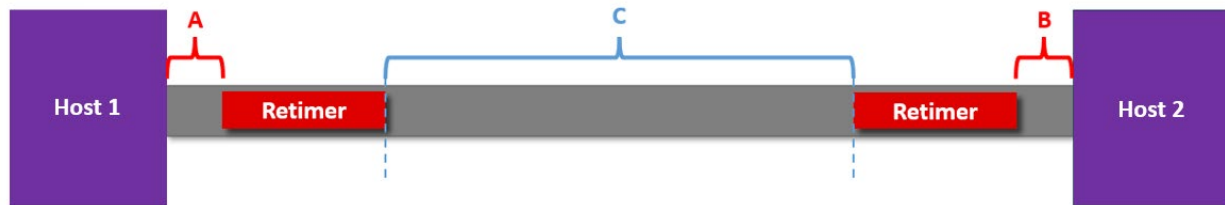
FIG.1D

Equalization at the receiver was often needed to make sure the signal is clear, ensuring a good separation between high and low signals (this is called “opening the signal eye”). This clear separation allowed the downstream clock and data recovery (CDR) circuit to accurately recover incoming data into a stream of bits.

Ex-1007, ¶217 (“[T]o achieve proper detection of zeros and ones, the CDR requires an eye which has been opened by receiver’s equalization resources (such as Gain, CTLE, and DFE).”).

21. Retimers extended link distance by dividing a link into distinct sub-links that were independent from each other from a signal-integrity perspective; this was the main benefit of using retimers. Ex-1007, ¶¶15-16, ¶50. As such, pre-equalization and equalization coefficients for each sub-link were calibrated to the characteristics of that sub-link. *E.g.*, Ex-1007, ¶232 (retimer splitting the link into sub-links, each independently compliant with equalization requirements). By doing so, a retimer effectively divided the link into a series of shorter distances and relaxed the burden of pre-equalization and equalization. Moreover, this approach enhanced the signal integrity (smaller BER) due to less channel loss per sub-link and prevented jitter accumulation along the entire link.

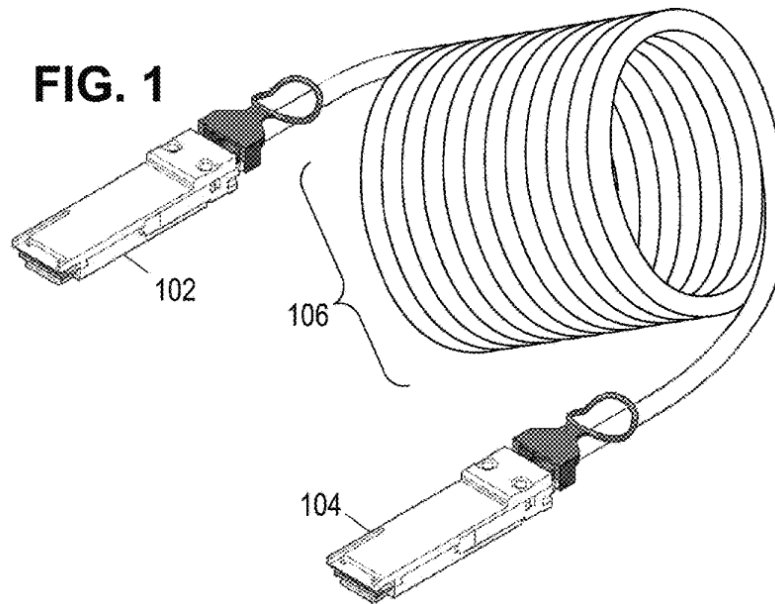
22. Active cables used retimers on both ends, dividing the link between hosts into three sub-links: (A) a path from a host to the nearest retimer, at the near end of the cable; (B) a path from the retimer at the far end of the cable to the far-end host (from the perspective of the first host); and (C) a path over the cable between retimers.



To ensure each sub-link was independent from the rest from a signal integrity perspective, the equalization on each path—both transmitter pre-equalization and receiver equalization—was customized for the channel characteristics of that path. For example, equalization parameters for path C compensated for characteristics of the connecting cable, and such parameters depended on the characteristics of the particular cable. Equalization parameters for paths A and B dealt compensated for channel loss in host-side circuit board traces. These host-side equalization parameters do not depend on any cable properties because they dealt with other sub-links, rather than the cable. *See* Ex-1005, 13:49-54, 14:50-57 (discussing host-facing equalizations).

II. THE '252 PATENT

23. The '252 patent is directed to an “active cable.” Ex-1001, (54) Title, Fig.1:



The patent recognizes challenges with ever-increasing communication speeds: “[a]s demand continues for ever-higher data rates...the standard must account for increased channel attenuation and dispersion even as the equalizers are forced to operate at faster symbol rates.” Ex-1001, 1:14-21. Accordingly, “[i]t is becoming increasingly difficult to provide affordable, mass-manufactured network hardware that assures consistently robust performance as the proposed per-lane bit rates rise beyond 50 Gbps with PAM4 or larger signal constellations.” *Id.*

24. The '252 patent purports to address these challenges by adding transceivers in the cable connectors (one at each end) to retime signals by extracting and re-modulating data streams at each end. Ex-1001, 1:26-42. The use of retimers in the cable accomplishes the patent’s stated goal: “mass-manufactured network hardware that assures consistently robust performance as the proposed per-lane bit rates rise beyond 50 Gbps with PAM4 or larger signal constellation.”

Id. The patent also lists 18 mundane details that follow from the use of retimers. Ex-1001, 2:17-3:16. During prosecution the Examiner rightly rejected this alleged point of novelty as being known in the art, as explained below. In response, the Applicant inserted a limitation into the independent claims requiring equalization for host-side signals using fixed, cable-independent equalization parameters.

25. However, as explained above, active cables already included equalization for each sub-link between hosts, including for signals exchanged between hosts and the nearest retimer in the cable. Because these equalizers operated on the host side, rather than the path through the actual cable, they were known to use fixed, cable-independent parameters. *See* above §I.

A. Prosecution History

26. The '252 patent was filed as U.S. patent application no. 16/539,910. Ex-1002, 000001. During prosecution, the Examiner determined that U.S. Patent No. 9,337,993 (Lugthart-993) disclosed every limitation of as-filed claims 1, 8, and 15 (which became limitations [1pre]-[1c]) and as-filed claims 2, 9, and 16 (which became limitation [1d]). Ex-1002, 000547-558. The Applicant never disputed the Examiner's conclusion; instead, the Applicant amended the claims to import a dependent claim (as-filed claims 3, 10, and 17) (Ex-1002, 000637), which became limitation [1e]: "the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit

data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.” Ex-1002, 000629. The Applicant acknowledged that these amendments were made according to the Examiner’s identification of allowable subject matter in the originally filed claims 3, 10, and 17. Ex-1002, 000637. The Examiner noted this as the reason for allowance. Ex-1002, 000673 (“applicant's REMARKS filed on 12/01/20 is agreed to”).

27. After reviewing the prosecution history, it is my opinion that the examiner erred, first, by not searching for the alleged novelty of these as-filed dependent claims; and second, by failing to identify the plain teachings in the prior art that clearly teach limitation [1e].

28. The examiner’s search parameters were limited to permutations of terms in as-filed claim 1. Ex-1002, 000455-458 (“ethernet,” “cable,” “cdr,” “transceiv*,” “transmit*,” “receiv*,” “active,” “modulat*,” “pair,” “conduct,” etc.). The examiner did not direct his search to the elements unique to as-filed dependent claims 3, 10, and 17 (issued limitation [1e]). For example, the examiner did not search for “equalization,” “equalizer,” or “equalization parameters.” Ex-1002, 000443, 000449-450, 000455-458. The examiner did not include “cable-independent” or “cable-dependent” parameters in his search strategy. *Id.* Without having searched for it, the examiner concluded this limitation was allowable. Ex-1002, 000558.

29. After the Applicant made the amendments to combine claims 1-3, the Examiner employed a similar search strategy that was not directed to the elements of limitation [1e]. *Compare* Ex-1002, 000455-458, *with, id.*, 000514-520 (new keyword searches only adding '252's inventors into the keywords). Nor did the examiner's search employ any alternative terms for this limitation. *See* Ex-1002, 000514-520.

30. However, as I explained above, calibrating equalizer circuits to account for different types and amounts of losses caused by different paths over a cable was widely known and practiced in the industry by March, 2019. *See* above §I.C. Numerous references, including Aronson (*see* below §V.C.2) and Cornelius (*see* below §V.A.1), teach equalizer parameters that account for losses caused by host-side paths. Ex-1005, 13:49-14:5, 14:33-57; Ex-1006, 11:45-62.

31. For example, Aronson explains that its invention “would provide equalization to compensat[e] for high frequency loss in the host board traces” and “preemphasis...to overcome the larger loss on the cable,” which “is [a] well known technique.” Ex-1005, 13:49-14:5. Aronson also teaches providing equalization/emphasis for the host-side printed circuit board (PCB) and for the cables. Ex-1005, 14:33-40, 50-57; *see* above §I.C.

32. Two other patents related to Aronson were disclosed in information disclosure statements both before and after the amendment. Ex-1002, 000002,

000451, 000640. Yet the Examiner initialed these without any evidence that he analyzed the relevant portions. Ex-1002, 000650. The examiner also ran raw patent numbers from the IDS in searches, but failed to consider them for this limitation. *See, e.g.*, Ex-1002, 000457 (search reference # S21), 000686 (search reference # S85). If the examiner had reviewed Aronson for teachings of limitation [1e], the examiner would have reached the same conclusion as any other POSITA—that these Aronson references taught the alleged point of novelty. But there is no indication in the record that the examiner discussed Aronson or that he actually analyzed it in any level of detail.

33. Although patents in the same family as Lugthart (*see* below §V.C.1) and Aronson were disclosed during prosecution, the prosecution history makes it clear that neither of these references were analyzed for limitation [1e]. Cornelius and Samaan were not cited or considered during examination—they are not cited on the face of the patent, nor have I seen these references discussed in the prosecution history.³

³ I observe that Cornelius' Chinese counterpart (CN 202797544) was cited as a relevant reference during prosecution of the '252's counterpart Chinese application (CN 20191015535) (Ex-1030, 000001), but it was not used or discussed during prosecution before the Chinese patent office. Ex-1030, 000001-2, 000036-37. Nor did it appear in the US file history.

B. Priority Date

34. The '252 patent was filed on Aug. 13, 2019, claiming priority to a Chinese application filed on Mar. 1, 2019. For purposes of this Declaration, I have analyzed obviousness as of Mar. 1, 2019. I do not offer an opinion as to whether the '252 patent is entitled to a certain priority date. My invalidity opinions would not change if a later date was determined to be the correct priority date because the prior art relied upon in this declaration would still be prior art.

C. Challenged Claims

35. I understand that Petitioner is challenging the validity of claims 1 through 14 of the '252 patent in the Petition for Inter Partes Review to which this declaration will be attached. Those claims are reproduced in Appendix 3. While this Petition and declaration are directed to the challenged claims, I have considered all claims 1 through 14 of the '252 patent, as well as portions of the '252 patent prosecution history in forming my opinions.

III. LEVEL OF ORDINARY SKILL IN THE ART

36. I have analyzed the '252 patent and determined that the field of the patent is high-speed communications. The specification explains a problem in its field is that “demand continues for ever-higher data rates” and that “equalizers are forced to operate at faster symbol rates.” Ex-1001, 1:3-22. It acknowledges difficulties in “assur[ing] consistently robust performance as the proposed per-lane bit rates rise beyond 50 Gbps....” Ex-1001, 1:18-22. In particular, the goal of

the '252 patent is to provide “architectures and communication methods that enable mass-manufactured cables to perform robustly at per-lane PAM4 symbol rates up to 26.5625 GBd and beyond.” Ex-1001, 1:26-42. And the alleged invention addresses the goal of high-speed communications with equalization in transceivers. Ex-1001, 1:26-42, 9:33-36. The embodiments include a “communication method,” a “cable manufacturing method,” “implemented individually or in combination,” to support such high-speed communications. Ex-1001, 1:42, 1:62, 2:17-20, 2:38-39 (at “a per-lane bit rate of 50 Gbps or more”), Fig.1. The specification describes various high-speed communication embodiments. E.g., 8:38-56 (“sending and receiving a 200 Gbps Ethernet data stream...sending and receiving 400 Gbps...”).

37. In determining the characteristics of a hypothetical person of ordinary skill in the art (“POSITA”) of the '252 patent at the time of the claimed invention, I considered several things, including various prior art techniques relating to the field, the type of problems that such techniques gave rise to, and the rapidity with which innovations were made. I also considered the sophistication of the technologies involved, and the educational background and experience of those actively working in the field at the time. I also considered the level of education that would be necessary to understand the '252 patent. Finally, I placed myself

back in the relevant period of time and considered the engineers and programmers that I have worked with and managed in the field.

38. I came to the conclusion that a POSITA in the field of art of the '252 patent would have been a person with a bachelor's degree in electrical engineering or computer engineering with at least three years of experience in the field (explained above). A person with less practical experience but more relevant education may also meet this standard.

39. In the March 2019 timeframe, a POSITA would have known and had the skills necessary to:

- Understand common high-speed serial components, e.g., equalization, CDR, pre-equalization, modulation, and filters;
- Design high-speed serial communication systems;
- Design active Ethernet cables;
- Design various equalization and pre-equalization filters, including by using an FIR filter and customizing the tap coefficients of the filter;
- Program a DSP to perform common functions in transceivers; and
- Implement protocols for calibrating and setting equalization parameters.

IV. CLAIM CONSTRUCTION

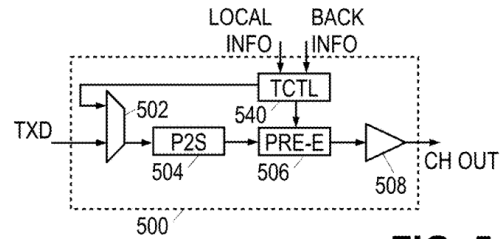
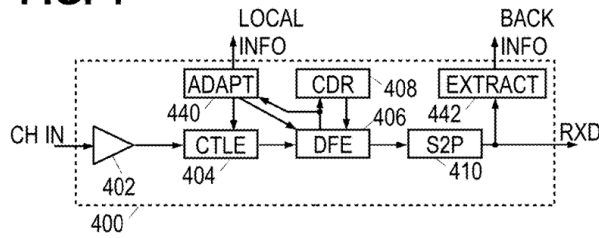
40. For purposes of this inter partes review, I have considered the claim language, specification, and portions of the prosecution history, to determine the meaning of the claim language as it would have been understood by a person of ordinary skill in the art at the time of the invention. The “plain and ordinary meaning” or *Phillips* standard has traditionally been applied in district court litigation, where a claim term is given its plain and ordinary meaning in view of the specification from the viewpoint of a person of ordinary skill in the art.

41. I have applied the *Phillips* standard in my analysis. Unless otherwise stated, I have applied the plain and ordinary meaning to claim terms.

A. “inbound”/“outbound”

42. The '252 patent defines the “inbound” direction from the perspective of the cable. For example, the '252 patent explains that the “the outbound data streams as they exit the cable...[and] the inbound data streams as they enter the cable.”⁴ Ex-1001, 3:66-4:3, 2:27-32 (explaining connectors at the ends of the cables “receive an inbound data stream as an electrical input signal from the host device and [] provide an outbound data stream as an electrical output signal to the host device.”), 1:31-42 (similar), Figs.4-5 (“CH IN”, “CH OUT”):

⁴ All emphasis and annotations added unless stated otherwise.

FIG. 4**FIG. 5**

43. I note that the directions of signal flow referred to by these terms in the '252 patent is the opposite of how they are used in U.S. Patent No. 10,877,233.

B. “each...” (Claim 7)

44. Claim 7 contains a clerical error, where the language “each employ fixed, cable-independent, equalization parameters” was inserted at the time of publication. This language was absent from claim 11 (which issued as claim 7) during prosecution. Ex-1002, 000052 (as-filed claim 11), 000631 (claim 11 not amended in request for reconsideration after non-final rejection). Therefore, a POSITA would have understood that this limitation (“each employ fixed, cable-independent, equalization parameters”) is not part of claim 7.

V. INVALIDITY GROUNDS

45. Based on my review and analysis of the materials cited herein, my opinions regarding the understanding of a POSITA in the 2019 timeframe, and my training and experience, it is my opinion that the challenged claims are invalid based on the following grounds:

Grounds	Claims	Statutory Basis	Prior Art
1	1-4, 6-9, 11-14	§ 103	Cornelius in view of Samaan
2	5, 10	§ 103	Ground 1 in view of Lugthart
3	1-14	§ 103	Lugthart in view of Aronson

A. Ground 1: Claims 1-14 Are Rendered Obvious in View of Cornelius and Samaan.

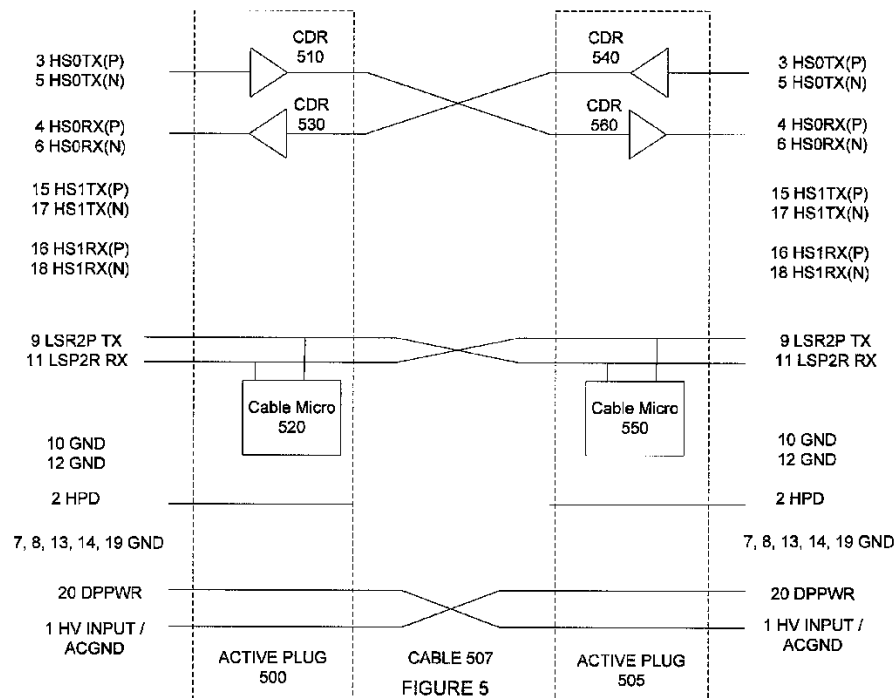
46. It is my opinion that a POSITA would have found claims 1-4, 6-9, 11-14 obvious based on the teachings of Cornelius and Samaan.

47. Cornelius is Apple prior art that teaches an active cable with CDR circuitry that “retime[s] data” and performs equalization. Ex-1006, 6:6-32. Samaan, an Intel paper, teaches retimer details, e.g., for performing CDR, remodulation, and equalization, plus support for common data transmission standards, including Ethernet. Ex-1007, ¶¶208-209, ¶5, ¶238, ¶¶250-267. Ground 1 uses Cornelius’s active cable teachings and applies Samaan’s teachings about general retimer layout and operation.

1. U.S. Patent No. 8,516,238 (“Cornelius”) (Ex-1006)

48. Cornelius is entitled “Circuitry For Active Cable.” Ex-1006, Title. Cornelius was issued on Aug. 20, 2013. Based on the priority date of Mar. 1, 2019 of the ’252 patent, I understand Cornelius is prior art to the ’252 patent under post-AIA §102(a)(1). *See* below, Appendix 4 (Understanding of the Law).

49. Cornelius teaches the use of “an active cable” that has “the ability to retune data at each of its ends” to facilitate data communication between a host device and an endpoint device. Ex-1006, 6:6-10, 3:33-42, Figs.2, 5, 6. To enable data retiming at both ends, Cornelius teaches the inclusion of “dual clock and data recovery circuits” (CDR circuits) within each active plug located at the cable’s ends. Ex-1006, 6:11-20, 21-29, 8:20-26, Figs.6, 5:



50. Cornelius’ CDR circuits provide more than typical clock/data recovery; they also “employ equalizer circuits, buffers, emphasis, and de-emphasis circuits” that can be calibrated to improve “the reliability and accuracy of data connections.” Ex-1006, 6:30-32, 11:45-48. For example, the equalization

parameters may be calibrated “by the manufacture[r] and stored as presets for loading during operation,” or “determined while the system is connected.” Ex-1006, 11:52-57. These calibration methods are applicable across various segments of a communication connection between two hosts, including “the path from a host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host.” Ex-1006, 11:59-62.

51. Cornelius is analogous art to the ’252 patent because it is in the same field of endeavor (high-speed communications) (*see* above §III). Cornelius discloses an active cable that provides a “high-speed connection.” Ex-1006, 3:27-42, 3:54-64, 4:22-31, 4:45-54, 6:11-24, 8:57-9:6. Each of the two active plugs “provides” and “receives high-speed signals.” Ex-1006, 6:11-20, Fig.5. Additionally, the ’252 patent recognized a problem where “ever-higher data rates” caused “increased channel attenuation and dispersion even as the equalizers are forced to operate at faster symbol rates.” Ex-1001, 1:14-22. The claims address this need for more equalization with equalization for each of the transmit and receive paths. Ex-1001, limitation [1e]. Cornelius is reasonably pertinent to the problem addressed by the ’252 patent because it teaches solutions for high-speed active cables that include “equalizer,” “emphasis,” and “deemphasis circuits” in CDR/retimer circuitry on both receive and transmit paths. Ex-1006, 6:30-32, 11:45-62, 12:12-13, claims 1, 6.

2. “High-Speed Serial Bus Repeater Primer: Re-driver and Re-timer Micro-architecture, Properties, and Usage, Intel Corp., Revision 1.2” (“Samaan”)

52. Samaan is a white paper that was published in 2015. Ex-1007, 000001-000072. Based on the priority date of Mar. 1, 2019 of the '252 patent, I understand Samaan is prior art to the '252 patent under post-AIA §102(a)(1).

53. **Prior Art Publication.** A declaration by librarian June Munford confirms Samaan was published and publicly accessible before the priority date of the '252 patent. Ex-1018. Samaan was uploaded to and freely available for download through Intel's website at least by February 2, 2016. Ex-1018, ¶7. Intel was a large corporation that developed many components for computer and networking devices, and had a well-funded research department. Intel published whitepapers on technical topics, including for data transmission. Researchers and academia would seek out such whitepapers to learn about Intel's research and development efforts and trends in industry.

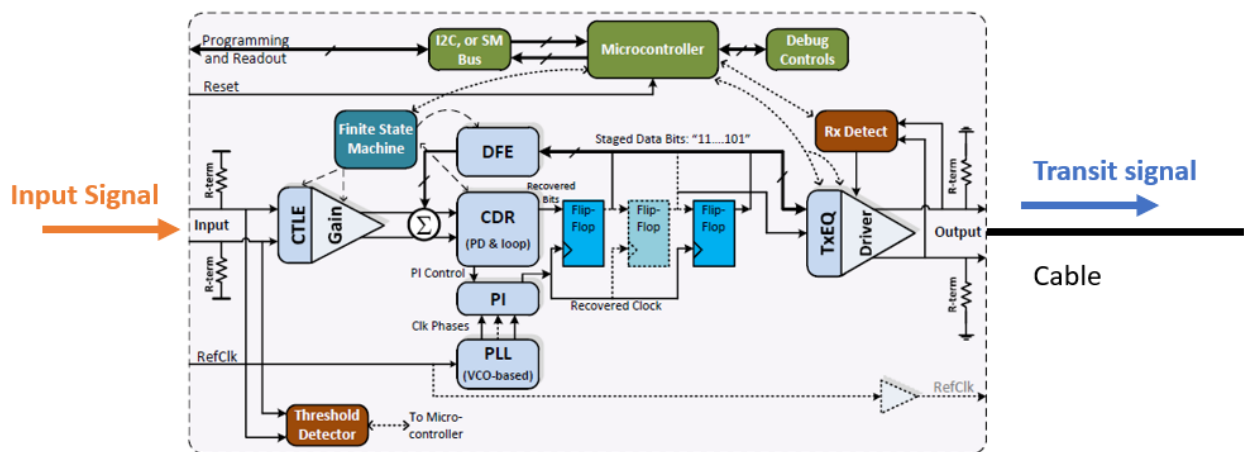
54. In my own research, I have occasionally sought out white papers, datasheets, application notes, or the like that Intel and other large, well-known vendors publish on their websites to disseminate to the public. I recall that Intel's website included search functionality (which it still retains) that allowed a web-surfer to locate information of interest by searching with keywords. A POSITA would have found it simple to locate a white paper, technical brief, specification,

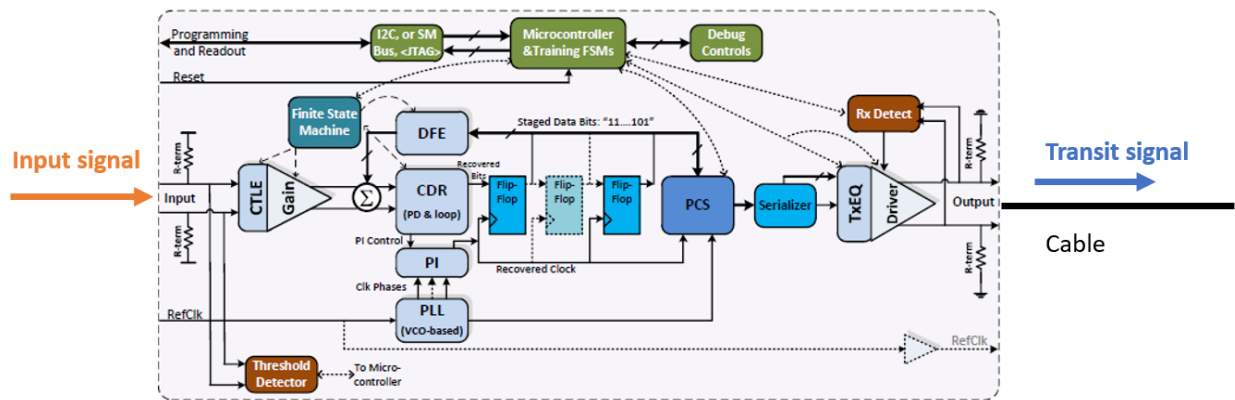
manual, or other technical document on Intel's website, which would require only a few clicks and a search. For example, searching for the title of Samaan, "High-Speed Serial Bus Repeater Primer," returns a single search result (Ex-1035, 000001) with a webpage (entitled PCI Express® Architecture) providing technical documentation on the PCI Express standard, which has a link to Samaan under the heading "White Papers" (Ex-1033, "High-Speed Serial Bus Repeater Primer"). Searching with other related search terms such as "Retime & PCI express," "Retimer & PCIe," "Repeater & PCIe," and "retimer repeater" similarly returns results with the PCI Express® Architecture page, with a link to Samaan, appearing on the first page of search results. Ex-1035, 000003, 000007-8, 000011, 000015.

55. Snapshots taken by the Internet Archive of Intel's PCI Express® Architecture webpage and the link "High-Speed Serial Bus Repeater Primer" confirms that this webpage was available and provided a link for users to access Samaan before the priority date of the '252 patent. Ex-1018, 000105-106, 000029-30. This same page was cited on a Wikipedia page for the entry PCI Express. Ex-1034, 000028 (under External Links: "'PCI Express Architecture', Developer Network, Intel"); Ex-1018, 000153, 000143-53. I note that Cornelius cites to the very same Wikipedia page on PCI Express, and POSITAs like the inventors of Cornelius would have followed such links to search for more information. Ex-1006, 000002 ("Other Publications").

56. It was customary for researchers to look up cited references to obtain further details or other information related to a topic of research. Indeed, the Munford declaration further demonstrates that interested members of the public, such as researchers at Texas Instruments, did in fact access Samaan and cite it in their own work before Mar. 1, 2019. Ex-1018, ¶¶11-17.

57. **Samaan Overview.** Samaan describes the architecture and usage of SerDes repeaters, including redrivers and retimers, in high-speed copper link systems. Ex-1007, ¶¶2-6. Samaan details how retimers utilize equalization and clock and data recovery to extract bits from an input signal, and then perform pre-equalization and modulation to transmit the signal on the other end. Ex-1007, Figs.34-35:





58. Samaan alternates its discussion between redrivers and retimers, which share common components, and Samaan’s teachings regarding those components apply to both applications. As Samaan explains, the retimer architectures employ many of the same components and Samaan relies on its redriver teachings to explain retimers, including, for example, equalizer circuits (Ex-1007, ¶215 (“These circuits are similar to those in a re-driver (section 3.1.2).”), ¶225 (“[I]t is a true FIR filter, as described in section 3.1.5.”)) and various input/output interface circuits. Ex-1007, ¶226, ¶228, ¶229. Samaan introduces many of its protocol discussions mentioning redrivers, including techniques for adapting equalization that likewise apply to retimers. Ex-1007, ¶208, ¶232, ¶78, ¶134. Fundamentally, Samaan’s repeaters—including both redrivers and retimers—are designed to operate in similar environments (SerDes transmission) and serve similar functions, specifically to “‘restore’ the signals mid-flight.” Ex-1007, ¶1, ¶3. As a result, Samaan’s redrivers and retimers share common architectural features, such as support for bidirectional data transmission

(Ex-1007, ¶213) and compatibility with differential signals. Ex-1007, ¶¶17-18, ¶28, ¶226, Figs.3, 34, 35.

59. Samaan is analogous art to the '252 patent because it is in the same field of endeavor (high-speed communications) (*see* above §III), as clearly suggested by Samaan's title. Ex-1007, Title. Samaan explains that it targets professionals working with high-speed serial buses and specialized signal integrity components (redrivers and retimers) that ensure optimal performance and reliability in high-speed data transmission environments. Ex-1007, ¶1, ¶¶5-8, ¶¶12-15. Samaan is also reasonably pertinent to the problem addressed by the '252 patent (*see* above §V.A.1 (explaining the problem)) because Samaan likewise recognizes the problem of channel loss at high data rates (Ex-1007, ¶¶2-4) and teaches the use of equalization in retimers, which were transceivers, for both the transmit and receive paths. Ex-1007, ¶213 ("Re-timers usually come as an identical pair (or pairs) in one package...in order to accommodate both the sending and the receiving directions of one or more lanes (or links)."), ¶1, ¶¶5-8, ¶¶207-220, Figs.34-35. Therefore, a POSITA looking at the problem addressed by the '252 patent would have found Samaan to be reasonably pertinent because Samaan teaches the exact type of transceiver architecture that was used for high-speed serial communications, including for Ethernet and cable applications, to address

the increased channel attenuation and dispersion caused by high data rates. Ex-1007, ¶¶250-251, ¶¶134-135, ¶72, ¶238.

3. Independent Claim 1

60. As an initial matter, for each of the below limitations, the “first” and “second” designations can be swapped between elements at one end of the active cable versus the other. Cornelius’ cable design is symmetric to support bi-directional communication; each side has identical components and operation. *E.g.*, Ex-1006, 6:14-23, 8:20-40, Claims 1, 6, Figs.5-6. Therefore, the connector/host/signal/stream on one end of the cable would serve as the first, while those on the other end would be the second.

[1pre] An active Ethernet cable that comprises:
--

61. I understand that a preamble generally does not state a claim limitation. Nonetheless, it is my opinion that Ground 1 teaches [1pre].

62. For example, Cornelius discloses an “active cable” and explains various details of its composition and function. Ex-1006, Title, 5:33-39, 6:6-20, 8:20-40, Figs.5-6, Claims 1-10. Cornelius applies its teachings broadly to active cables and does not limit its teachings to any specific communication standard or protocol. *See, e.g.*, Ex-1006, 1:15-27 (“The various Universal Serial Bus (USB), Peripheral Component Interconnect Express (PCIe), and DisplayPort (DP) standards are but a few examples.”), 4:1-9. Cornelius cites to several known

communication standards including PCIe, DP, and “Ethernet.” Ex-1006, 000002 (under Other Publications). Therefore, Cornelius teaches or suggests using Ethernet with its active cable, and a POSITA would have found it obvious and been motivated to apply known standards for active cables, such as Ethernet, to Cornelius’ teachings. *See* above §I.B.

63. Ground 1 applies Samaan’s retimer teachings to Cornelius’s active cable. *See* above §V.A (explaining combination). Cornelius teaches retimers in its active cable (Ex-1006, 6:7-9 (“This cable may have the ability to retime data at each of its ends.”), 6:15-16), and Samaan teaches Ethernet support in retimers. For example, Samaan teaches an Ethernet-compatible retimer that facilitates communications between “two ethernet ports.” Ex-1007, ¶¶250-251, ¶¶134-135. Samaan teaches retimer support for equalization training, for example, optional equalization training for Ethernet standards. Ex-1007, ¶208, ¶¶139-147. Hence, Samaan teaches using retimers with various protocols, including Ethernet, for a variety of channels, including cables, and the combination of Cornelius and Samaan teaches or suggests Ethernet support for an active cable. Ex-1007, ¶72, ¶238.

64. **Motivation to Combine**. As early as 2011, Apple and Intel co-developed high-speed interface and active cable technologies that would later become known as Thunderbolt. Ex-1013, 000001. The collaboration made waves

and was widely discussed in the computing industry, with Apple developing and marketing the cable (Ex-1014, 000002-000003; Ex-1013, 000001-000002), and Intel providing the port and retimer architecture used for the connectors at each end of the cable. Ex-1016, 000001-000002 (industry expert confirming transceiver chips were integrated at both ends of thunderbolt cables); Ex-1015, 000003 (“Thunderbolt port and controller specification are entirely Intel’s.”). Mac computers included Thunderbolt ports starting in 2011 (Ex-1013, 000001), and other vendors began providing Thunderbolt solutions in the years after. Ex-1009, 000001 (describing ISL37231 “retimer for active copper cable applications”); Ex-1008, 000003-000005 (describing ISL37231 retimers in Thunderbolt connectors). Thunderbolt cables were on the market by 2011. Ex-1016, 000001.

65. By 2019, a POSITA interested in developing active cables would have been motivated by Apple and Intel’s collaboration to look to Apple’s cable art (such as Cornelius) and Intel’s technical references addressing transceiver/retimer architecture and implementation (such as Samaan). In particular, a POSITA would have been motivated to apply Samaan’s teachings to Cornelius, including for example, using Samaan’s retimer teachings to implement the “circuits for retiming data” in Cornelius’ active plugs. Ex-1006, 6:11-20, 8:20-26, Figs.5-6.

66. A POSITA would have been motivated to combine these teachings for several additional reasons, explained below. First, the references provide express

motivation to combine. Cornelius teaches that the active plugs at both ends of the cable include CDR circuits that “retime signals.” Ex-1006, Claim 1, 6:6-10. To implement such “circuits for retiming data,” Cornelius contemplated designs beyond simple CDR circuits: Cornelius teaches that its particular CDR circuits “employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate,” reflecting a comprehensive approach to signal integrity beyond mere clock and data recovery. Ex-1006, 6:30-32. However, Cornelius does not provide implementation details for those retimers, which was understandable because Apple focused on the broader cable assembly of Thunderbolt while Intel provided the retimer architecture and implementation. Samaan provides the missing implementation details and further enhances the designs contemplated by Cornelius. Cornelius therefore provides motivation to combine its teachings with known retimer implementations, and a POSITA would naturally have looked to known retimer architectures including those from Intel (e.g., Samaan), along with known retimer techniques and applications. *See* Ex-1006, 12:21-33 (providing motivation to modify its teachings). This would have been a combination of prior art elements according to known methods (e.g., as taught by Cornelius and Samaan) to yield predictable results (e.g., a retimer in an active cable, as Cornelius teaches). This would also have been a simple substitution of one known element

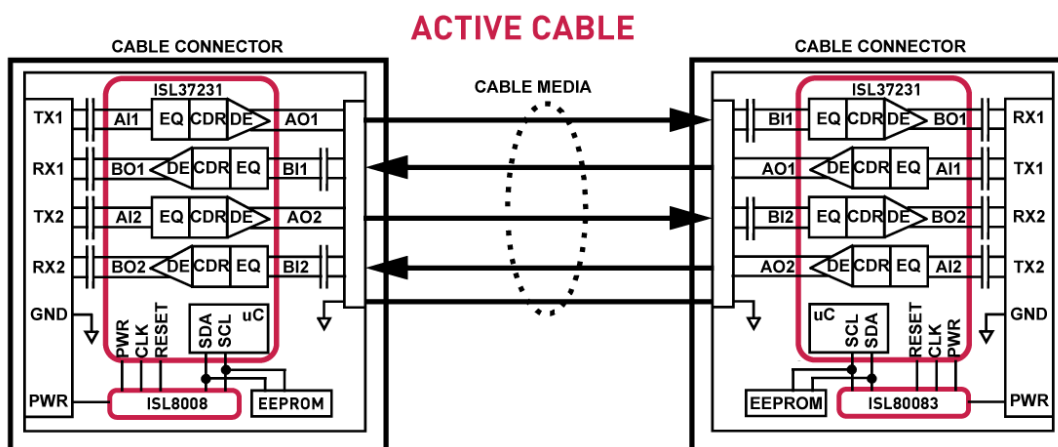
(e.g., Cornelius’ retimers) for another (e.g., Samaan’s retimers) to obtain predictable results.

67. Similarly, Samaan applies its teachings to cables. For example, when discussing retimer “Hot Plug,” Samaan teaches why retimers are “usable in a reversible cable (where either end can be plugged into the upstream or downstream component).” Ex-1007, ¶238. Samaan explains how retimers are used with “SFI” (Ex-1007, ¶204), and elsewhere teaches cable applications for SFI. Ex-1007, ¶72 (“Furthermore, in the Case of USB3, SATA3, and even SFI, the cables or devices connected to a host may vary in length”). When discussing SFI, Samaan cites to the Specification for SFP+, which is the Small Form-factor Pluggable module standard (Ex-1007, 000072, ¶204 (citing “[24]”)) that provides native support for various Ethernet standards, for example, 1Gb/s Ethernet, 10Gb/s Ethernet, etc. Ex-1025, 000019, Tbl. 1. SFP+ modules were also frequently used for active Ethernet cables. Ex-1011 (datasheet for TE SFP+ cables, supporting 1 and 10 Gigabit Ethernet), Ex-1012, 000001, 000003-5, 000008-9 (various Cisco SFP+ compliant transceiver and cable modules supporting 40 Gigabit Ethernet); Ex-1019, Video Description (“10G SFP+ direct attach copper cable...or 10G SFP+ DAC cable assembly, is a twinaxial cable assembly that has a length of copper cable and terminates with SFP+ connector modules on either end.”), 000002-4 (10G SFP+ direct attach copper cables and transceiver supporting Ethernet protocols).

Therefore, the combination applies a known technique (e.g., known retimer architectures) to a known device (e.g., active cables) that was ready for improvement to yield predictable results (e.g., a retimer in an active cable).

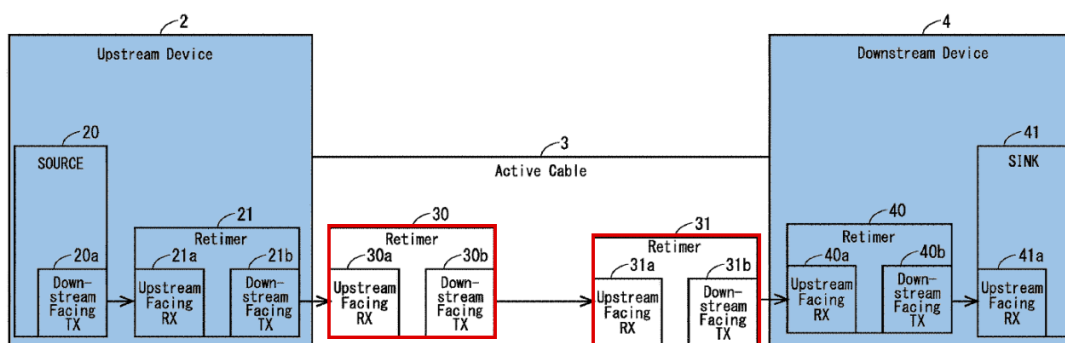
68. Additionally, a POSITA would have been motivated to use Samaan's retimer teachings in Cornelius' active cables based on the functionalities and benefits provided by Samaan's retimer architectures, including for example (1) upstream and downstream signal independence, which provides jitter isolation; (2) enhanced debug capabilities such as eye margining and compliance pattern testing; and (3) increased channel length. Ex-1007, ¶15, ¶202.

69. The prior art provides teaching, suggestion, and motivation to incorporate retimers at both ends of active cables; this was widespread by March 2019. *See, e.g.*, Ex-1009, 000001 (discussing retimer chips installed on an active cable's connectors, providing the benefits of "thinner gauge cable", "extend[ing] cable reach", and "improved BER".), Fig.1.



Ex-1009, Fig.1 (red in original); Ex-1026 (similar Texas Instrument products).

70. The prior art recognized numerous benefits from using retimers in active cables, including for example that retimers help “avoid high-speed serial bit stream signal quality degradation” and “extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the retimer.” Ex-1010, ¶2, Fig.1:



71. As another example, Samaan teaches the use of Ethernet (explained above), and a POSITA would have been motivated to apply those teachings to Cornelius’s active cable teachings for the benefits of supporting Ethernet. As explained above, Cornelius teaches a wide variety of protocols, including Ethernet (Ex-1006, 000002 (Other Publications)), and by March of 2019, active Ethernet cables were already sold commercially. *See* above §I.B; Ex-1011, 000001 (TE active cable assemblies supporting 10 Gigabit Ethernet protocol); Ex-1012, 000001, 000003-000005, 000008-000009 (various Cisco SFP+ compliant transceiver and cable modules supporting 40 Gigabit Ethernet); Ex-1019, Video

Description (“10G SFP+ direct attach copper cable). Given the market for active Ethernet cables, a POSITA would also have been motivated to apply Ethernet (which Samaan teaches) to Cornelius’ active cables, resulting in an active Ethernet cable, with corresponding ports (where the cables are connected) being ports that support Ethernet. This would have applied a known technique (e.g., Ethernet) to a known device (e.g., Cornelius’ active cable), which was ready for improvement to support Ethernet capabilities, to yield predictable results (e.g., an active Ethernet cable).

72. Moreover, Ethernet had long been used for a variety of physical channels, and common retimer architectures (e.g., with equalization, CDR, and then remodulation) were used across a variety of different physical channels such as backplanes and cables. Ex-1007, ¶5, ¶15 (discussing cables as a common form of copper-based serial links that introduce signal losses that retimers are designed to address), ¶134 (Ethernet backplane using retimers), ¶238 (incorporating the retimer to a reversible cable). Therefore, the combination uses a known technique (e.g., Ethernet) to improve similar devices (retimers in active cables or other devices) in the same way. This combination would have had predictable results, without changing the principle of Cornelius’ operation, given the wide range of physical channels and connectors used with Ethernet (*see* below §V.A.3[1b] (analyzing Cornelius’ connector/wire and comparing with CAT-5)), and Cornelius’

support for a wide range of protocols. Ex-1006, 1:19-22, 4:4-9. Nor would Ethernet have changed the principle of operation for Samaan, which already teaches Ethernet, and whose general retimer architecture was applicable to a variety of protocols. Ex-1007, ¶208, ¶¶232-233, ¶¶250-255.

73. The combination would not have changed the principle of operation for either reference. Applying Samaan's retimer teachings would not have changed the principle of operation of Cornelius, because Cornelius already teaches retimers in its active cable and suggests a wide variety of protocols, including Ethernet. Ex-1006, 000002 (citing to "Ethernet" under Other Publications), 6:6-20, claims 1, 6. Cornelius contemplates clock and data recovery circuits that "employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate." Ex-1006, 6:30-32. Samaan's retimer is likewise "[a] device which has a Clock and Data Recovery circuit (CDR[...])" coupled to equalization circuits—such as a continuous-time linear equalization circuit (CTLE), a discrete-feedback equalization circuit (DFE), and transmitter linear equalization (TxEQ) (Ex-1007, ¶¶202-231, ¶15)—that perform the emphasis and de-emphasis discussed in Cornelius. Ex-1006, 6:30-32; Ex-1007, ¶225. Both retime and recover data. Cornelius teaches "dual clock and data recovery circuits for retiming data" to provide "easily recoverable data." Ex-1006, 6:6-16, claims 1, 6. Samaan "converts an incoming analog bit stream into purely digital bits that are stored (or staged) internally. ...A re-timer re-transmits

data anew, with new equalization, and new jitter content, unrelated analog-wise to the input bit stream.” Ex-1007, ¶15, ¶202, Figs.34-35. Therefore, Samaan’s retimer teachings were applicable to Cornelius’ active plugs, including its CDR and related circuits. Using Samaan’s retimer architecture in an active cable would not have changed the principle of operation for Samaan because it already teaches or suggests the use of cables, and Samaan provides a high-level retimer architecture that was broadly applicable to a range of physical channels, including active electric cables. When used in an active cable, Samaan’s retimer would operate in the same way and for the same purpose as taught in Samaan—to recover bits from one end and re-transmit them on the other.

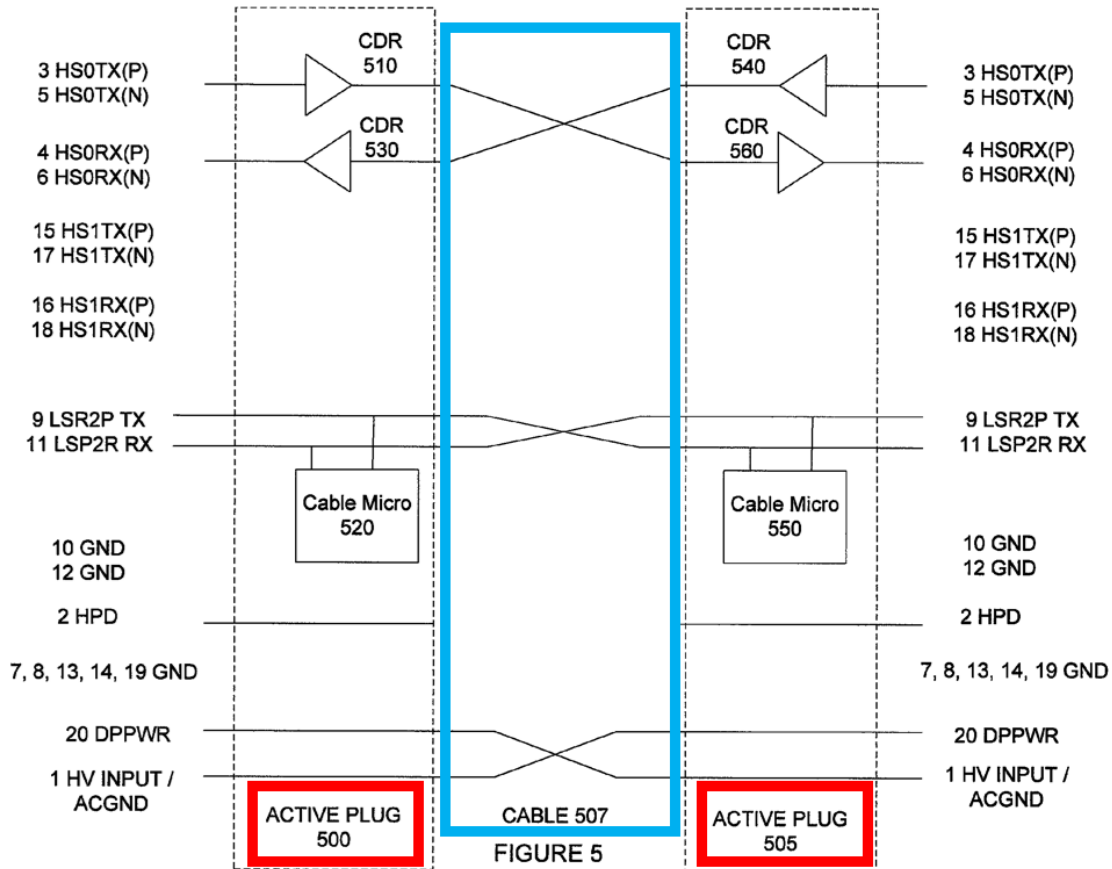
74. In addition to the reasons explained earlier in this section, a POSITA would have had a reasonable expectation of success in combining teachings from Cornelius and Samaan because retimers and active electric cables had long been used in the art. Samaan’s retimers reflect the common retimer architectures that had been used for high-speed serial communications for many years. By the early 2010s, I taught students the same retimer concepts that are taught by Samaan; therefore, a POSITA with the requisite level of education and experience (*see* above §III) would have known how to use retimers with cables. Ethernet had also been used in the art for decades, and Active Ethernet cables with retimers were sold on the market and used in data centers by the relevant timeframe (*see* above

§II.C). Therefore, a POSITA would have known how to use retimers with Ethernet, including for active Ethernet cables.

75. For at least these reasons, [1pre] is obvious in view of Ground 1. The active Ethernet cable taught by Ground 1 further comprises the elements discussed below for limitations [1a]-[1e].

[1a] electrical conductors connected between a first connector and a second connector,

76. Cornelius teaches **electrical conductors** (e.g., in a cable) **connected between a first connector and a second connector** (e.g., active plugs). For example, Cornelius teaches an “active cable” that “includes two active plugs...one on each end of cable.” Ex-1006, 6:11-20 (“active plugs 500 and 505, one on each end of cable 507”), Fig.5, 8:20-26 (“active plug 600” and “active plug 605”), Fig.6 (“cable 607” connecting “active plug 600” and “active plug 605”). Cornelius teaches several pairs of electrical conductors that go over the cable (blue in figure below) between a first connector (e.g., plug 500/600) and a second connector (e.g., plug 505/605, or vice versa), Fig.5:



Because Cornelius has a symmetric cable design, either plug satisfies the first connector, with the other plug being the second connector. The plugs serve to connect the cable to host devices at either end. Ex-1006, 1:15-17, 7:7-17, 7:22-25, 8:1-9. I explain these connectors in further detail below for limitation [1b]. *See* below §V.A.3[1b].

77. Cornelius teaches a cable comprising electrical conductors, including “copper or other conductor.” Ex-1006, 7:26-41. Cornelius also includes an option of fiber optics or “a mix of fiber optic and electrical wires” Ex-1006, 6:25-29. A POSITA would have been motivated to apply Cornelius’ teachings for simply

using copper or another conductor, rather than fiber optics, for several reasons, including reduced costs and improved bend radius. *See* Ex-1013, 000001 (Apple switching Thunderbolt from fiber to copper to reduce costs and maintain high performance), Ex-1014, 000002 (same). Furthermore, Apple provided motivation to use copper cabling by moving Thunderbolt cables from their initially envisioned fiber optics (Ex-1013, 000001-000002) to “construct the cable out of copper instead[.]” Ex-1014, 000002; Ex-1013, 000001.

78. For at least these reasons, Ground 1 teaches [1a].

[1b] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,

79. Ground 1 teaches **each of the first and second connectors** (e.g., active plugs) **being adapted to fit into an Ethernet port of a corresponding host device**. For example, Cornelius’ active plugs are used to connect each of the two ends of the cable to corresponding host devices, including, for example, “computer 110 communicating with computer or display 220.” Ex-1006, 3:28-42, 3:47-53 (“computer 110 may drive a display of an all-in-one computer, a second computer...or other type of device.”), Fig.2. Cornelius teaches several exemplary hosts, including computers, displays, and other high-speed I/O sources or sinks. *See* Ex-1006, 6:6-10 (using active cable to connect “an HSIO source or host and an

HSIO sink or endpoint.”), 3:33-64, 5:33-39 (“an active cable is required between the HSIO source or host and the HSIO sink or endpoint.”).

80. Cornelius teaches that these plugs connect to the host devices, which “provide ports where power and data signals can be shared with other devices.” Ex-1006, 1:15-17, 3:44-46, 4:55-65, Figs.2-3. Because the plugs are plugged into the ports and designed for that purpose, the plugs are adapted to fit into these ports. Cornelius provides details of an exemplary connector port design that shows the physical dimensions and the electrical pin specifications. Ex-1006, 3:65-4:9, 4:22-38 (“high-speed receive signals may be placed on pins 4 and 6, and 16 and 18...high-speed receive pins 16 and 18 may be isolated by ground 14 and power pin 20...High-speed transmit pins 3 and 5, and 15 and 17, may be isolated by ground pins 1, 7, 13, and 19.”), Fig.3:

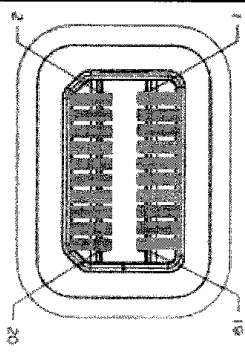
DP	T29	Pin		Pin	T29	DP
HPD	HPD	2		1	HV INPUT / ACGND	GND
CFG1	HS0RX(P)	4		3	HS0TX(P)	DP0(p)
CFG2	HS0RX(N)	6		5	HS0TX(N)	DP0(n)
GND	GND	8		7	GND	GND
DP3(p)	(RESERVED) GND	10		9	LSR2P TX	DPI(p)
DP3(n)	(RESERVED) GND	12		11	LSP2R Rx	DPI(n)
GND	GND	14		13	GND	GND
AUX(p)	HS1RX(P)	16		15	HS1TX(P)	DP2(p)
AUX(n)	HS1RX(N)	18		17	HS1TX(N)	DP2(n)
DPPWR	DPPWR	20		19	GND	GND

FIGURE 3

The pin arrangement on the cable corresponds to the pins on the port where the cable is connected. Ex-1006, 4:39-44 (“In a specific embodiment of the present invention, pin 20 at a first end of cable connects to pin 1 at a second end of the cable.”), 8:10-15 (same), 6:16-24 (“[s]pecifically, active plug 500 provides high-speed transmission signals on pins 3 and 5, and receives high-speed signals on pins 4 and 6.”), Figs.5-6. The active plugs are plugged into the connector ports to convey such power and data transmissions; therefore, each of the plugs are adapted to fit the ports on a corresponding host device (e.g., the host device into which it is plugged in). Ex-1006, 1:15-17, 7:7-17, 7:22-25, 8:1-9.

81. Cornelius does not limit its teaching to any one protocol (Ex-1006, 000002, 1:15-27, 4:3-4), and as explained above, Ground 1 teaches an active cable for Ethernet communications; that analysis also applies here. *See above* §V.A.3[1pre] (explaining how and why Cornelius and Samaan would be combined). When the active cable supports Ethernet communications, the corresponding port would supports Ethernet also; otherwise, the cable and port would not be compatible, and they would not function correctly. Therefore, Ground 1 teaches Ethernet ports⁵ for active Ethernet cables.

⁵ I note that Ethernet refers to a MAC protocol standard, rather than a physical connector. Ethernet was used over a variety of physical connectors, including the popular CAT-5 connector, but in many cases other connectors were used, including SFP, which supported Ethernet as one of several standards. Ex-1025, 000019, Tbl.

82. Cornelius' active plug design is readily compatible with Ethernet. As one example, Cornelius' port includes at least one pair of high-speed transmit lines (pins 3, 5) and receive lines (pins 4, 6). Ex-1006, 4:22-31, Figs.3, 5, 6 (second pair of transmit lines on pins 15, 17 and receive on 16, 18). Likewise, Ethernet is a high-speed input/output protocol with one pair of transmit lines and one pair of receive lines; therefore, it would have been obvious to use Cornelius' HSIO lines for Ethernet. *See* above §V.A.3[1pre]. Ethernet is often used with CAT-5, a simple connector with pairs of transmit and receive pins connected to twisted pair cables. Cornelius' Tx and Rx pins and wires could easily have served the same purpose. The legacy lines (such as pins 9-12) would also have worked for this purpose. As another example, Cornelius teaches or suggests Thunderbolt. Ex-1006, 1:19-22, 4:1-9. By March 2019, it was well known in the industry that it supported Ethernet. Ex-1027, 000004 ("Thunderbolt™ Networking allows for the connection of two or more computers through a Thunderbolt cable...uses the existing operating system's network sharing functionality to connect the systems as an Ethernet connection.").

83. And Samaan also teaches an Ethernet port. *See* above §V.A.3[1pre] (Motivation subsection explaining how and why Cornelius and Samaan would be

1. The '252 patent, for example, does not disclose CAT-5 and instead shows an SFP connector in its embodiments. Ex-1001, Fig.1.

combined). Samaan's retimers facilitate the process of "two Ethernet ports attempt[ing] to establish a connection." Ex-1007, ¶251, ¶250, ¶¶252-267, ¶¶139-143, ¶208. Additionally, Samaan teaches an SFP connector (Ex-1007, ¶204 (citing "[24] 'Specification for SFP+'")) which was a known standard that supported Ethernet.

84. Cornelius further teaches each plug is adapted to fit the host device's port **to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable.**

For example, Cornelius teaches first and second plugs that "retime signals received at an input of the [first/second] plug." Ex-1006, claim 1. Each host device sends a signal conveying an inbound data stream to the plug over the TX pins (e.g., 3, 5) and receives a signal conveying an outbound data stream from the plug over the RX pins (e.g., 4, 6). Ex-1006, Fig.3, 4:23-54, 3:33-42, 3:65-4:9. Cornelius describes transmit (Tx) and receive (Rx) from the host's perspective; the active plug receives the Tx signals and sends the Rx signals. Ex-1006, Figs.3, 5, 6:16-24.

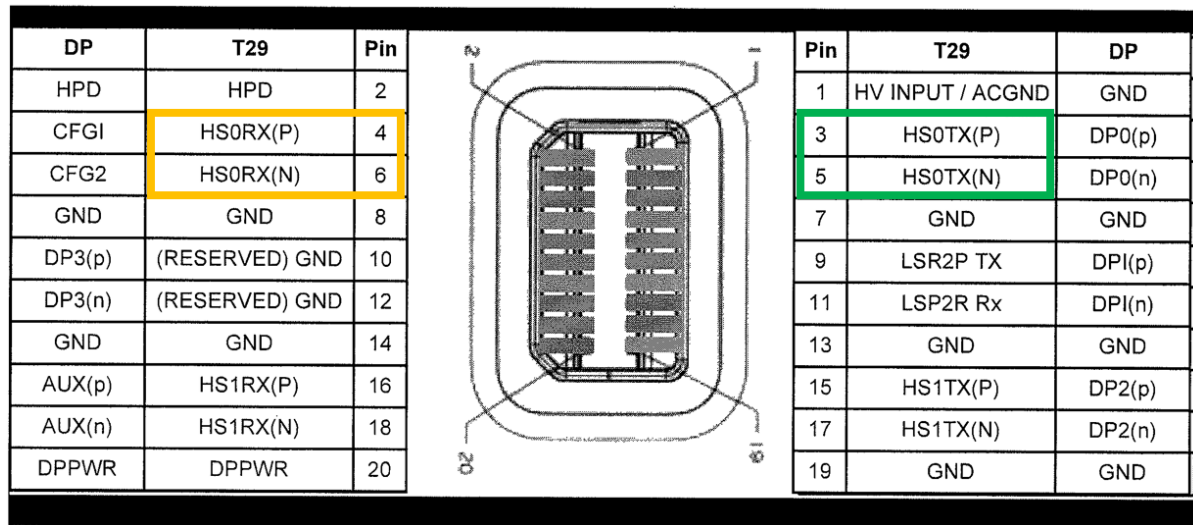
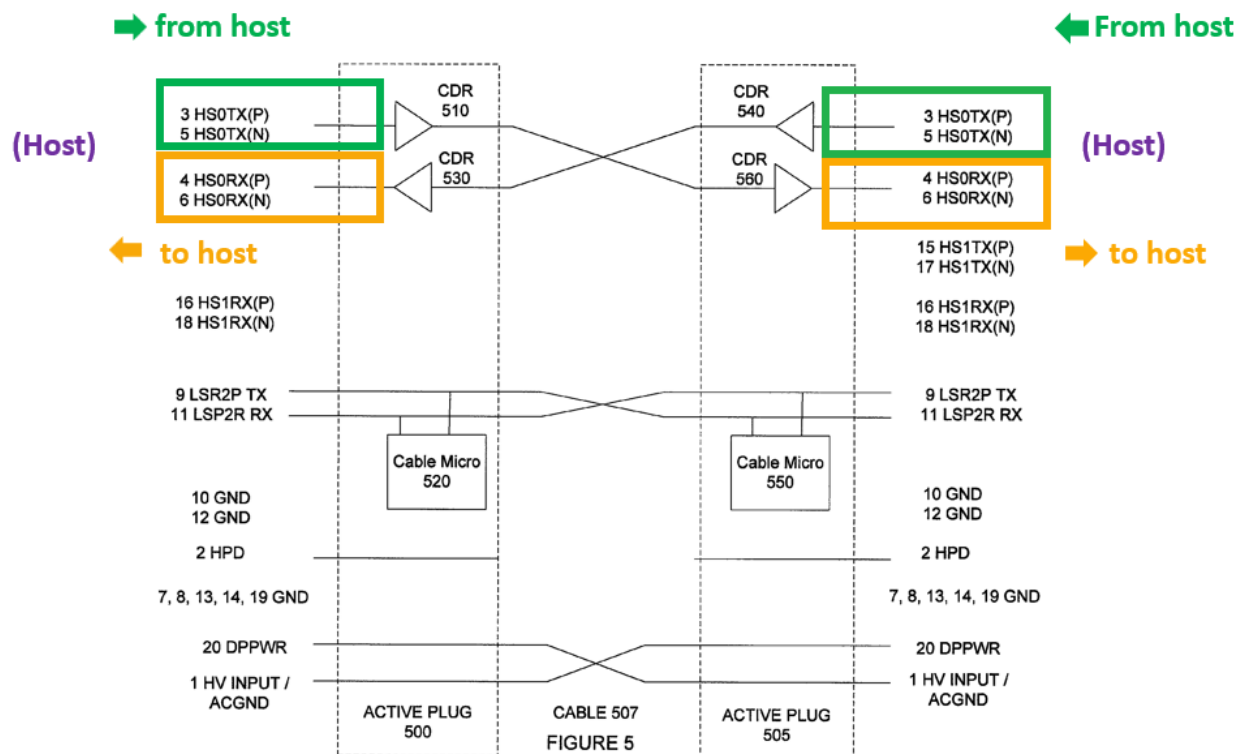


FIGURE 3



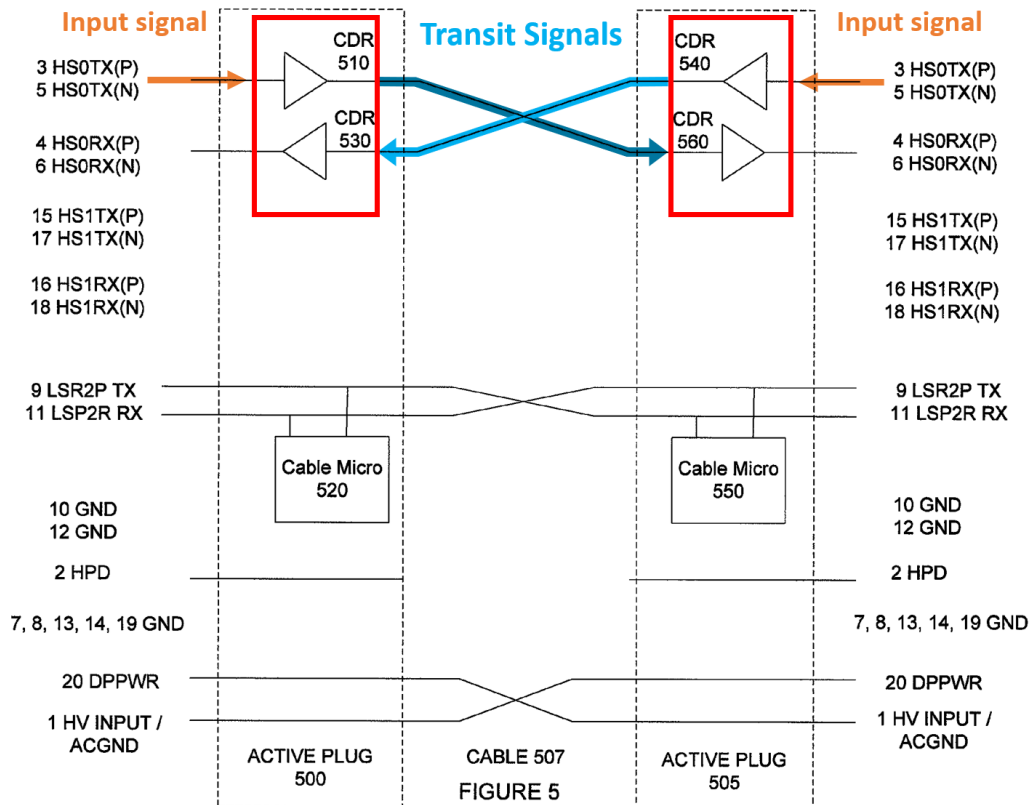
85. The Tx and Rx signals are conveyed to/from each active plug through the connector interface. Ex-1006, 6:16-24. Thus, each plug obtains an electrical input signal that conveys an inbound data stream from a host to the active cable (e.g., over Tx pins 3, 5) and sends an output signal conveying an outbound data stream from the active cable to a host (e.g., over Rx pins 4, 6. Ex-1006, 4:22-38 (“High-speed transmit pins 3 and 5, and 15 and 17...[H]igh-speed receive signals may be placed on pins 4 and 6, and 16 and 18.”)), Figs.2-3, 6.

86. For at least these reasons, Ground 1 teaches [1b].

[1c] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,
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87. Ground 1 teaches **each of the first and second connectors** (e.g., active plugs) **including a respective transceiver that performs clock and data recovery on the electrical input signal**. For example, Cornelius teaches that “[e]ach active plug includes dual clock and data recovery circuits” (e.g., CDR 510, 540), which operate on the incoming electrical input signal. Ex-1006, 6:11-24, Figs.5-6. Here, Cornelius’ “CDR” circuit performs a broader function, not limited to only CDR: it also retimes data (Ex-1006, 6:15-16) and “employ[s] equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate.” Ex-1006, 6:30-32. Therefore, the dual CDR circuitry in each plug is a transceiver because it

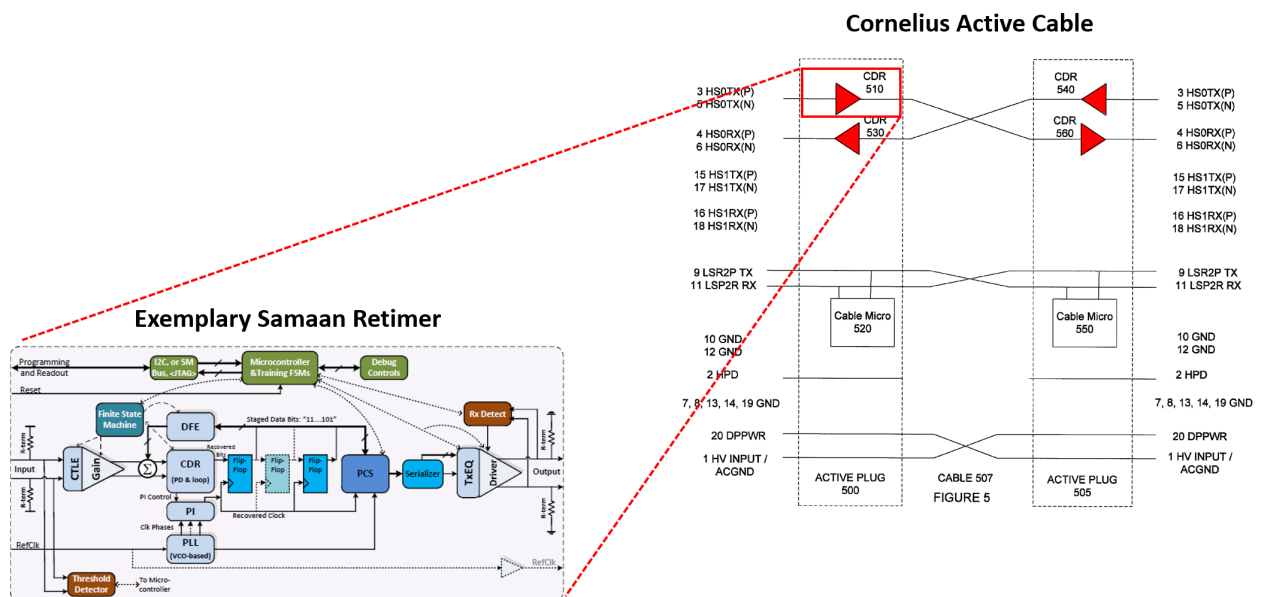
receives a signal and transmits a signal; this applies to an individual CDR component, which receives on one side and transmits on the other, and also to the dual CDR circuitry as a whole, which transmits and receives on each side. Ex-1006, 6:6-33, 8:20-26, claim 1, Fig.5:



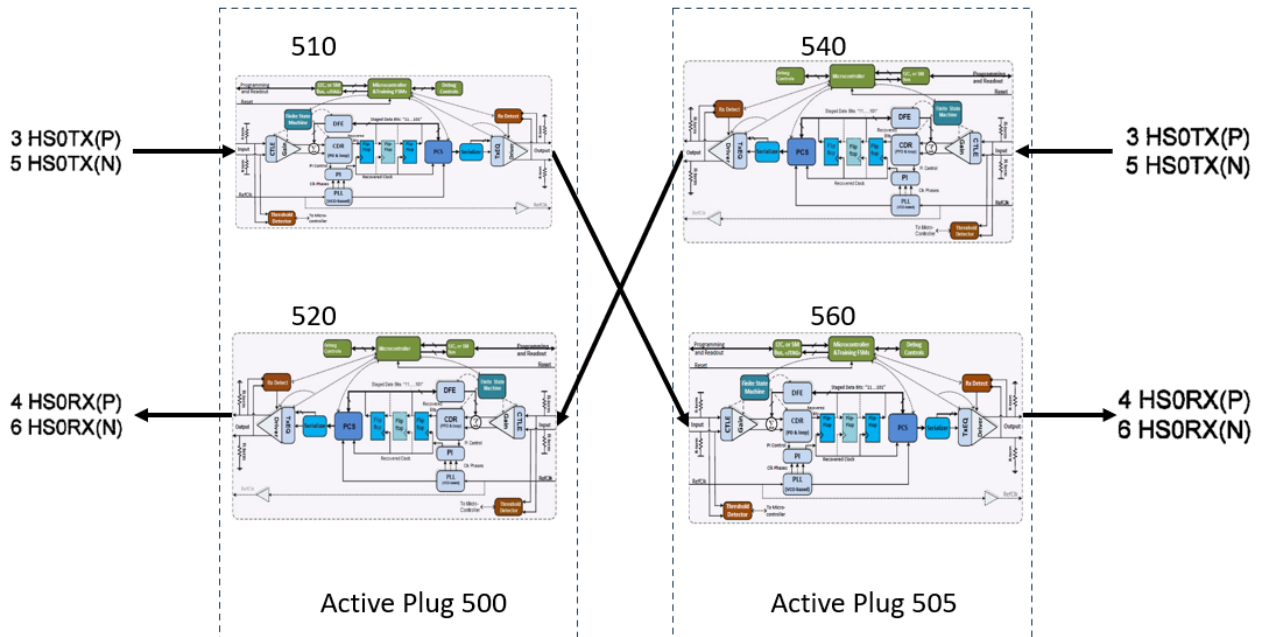
Cornelius' cable is bidirectional and symmetrical. Ex-1006, 6:11-24.

88. Additionally, the combination with Samaan further teaches this limitation. I previously explained how and why a POSITA would have applied Samaan's retimer teachings to Cornelius; that analysis applies here. *See above* §V.A.3[1pre] (Motivation to Combine subsection). Samaan teaches retimer architectures with the same functionality that Cornelius (Ex-1006, 6:6-32)

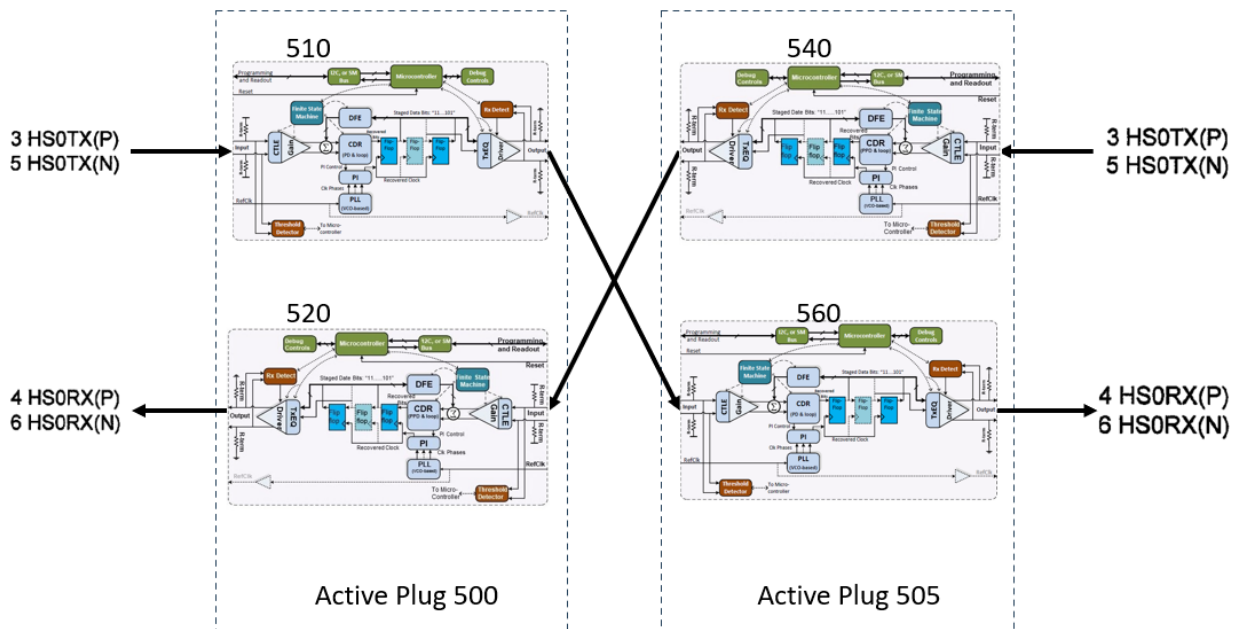
describes in its active plug and CDR, including retiming functionality, CDR, equalizer circuits, buffers, emphasis (pre-emphasis), and de-emphasis circuits. *E.g.*, Ex-1007, ¶225, ¶79, ¶91, ¶114, Figs.34-35. Thus, a POSITA would have applied Samaan's retimer teachings to Cornelius' active plugs; I have illustrated an example below showing Samaan's overall layout applied for functions taught or suggested by Cornelius). Ex-1006, Fig.5; Ex-1007, Figs.34-35.



Cornelius + Samaan



Cornelius + Samaan



89. Cornelius+Samaan teaches each active plug including a transceiver (e.g., Cornelius's dual CDR/retimer circuitry, combined with additional details form Samaan's retimer architectures) that performs CDR on the electrical input

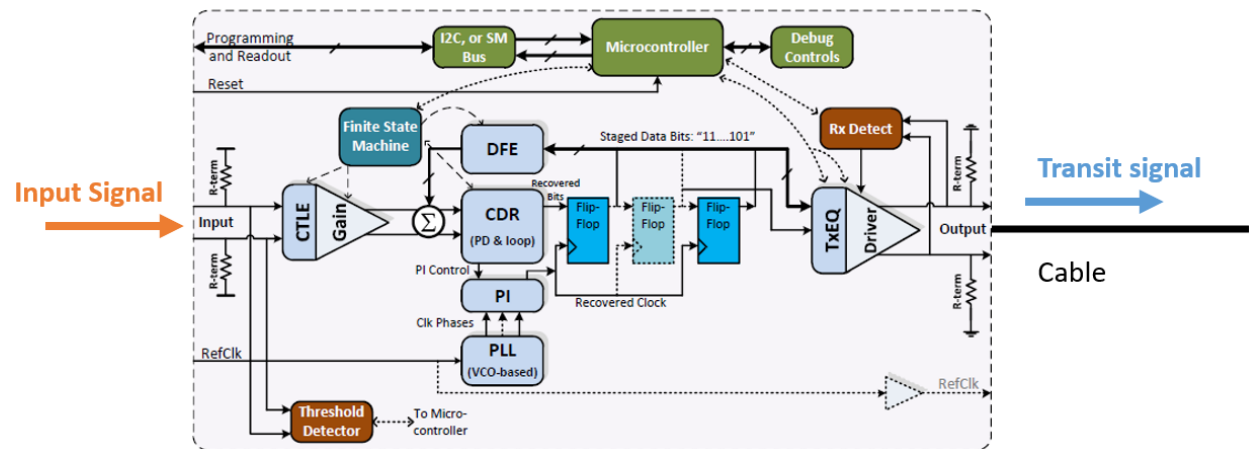
signal (on pins 3, 5). Samaan teaches CDR in its retimer architectures. Ex-1007, ¶¶202 (“A Re-timer has a Clock Data Recovery circuit.”), ¶15, ¶¶216-217.

90. Each transceiver does this to **extract and re-modulate the inbound data stream**. Cornelius performs clock and data recovery, which extracts bits from the inbound data stream; the CDR component then “retime[s]^[6] signals received at an input.” Ex-1006, claim 1, 6:11-24, 8:20-26. Therefore, Cornelius re-modulates the inbound data stream by converting the extracted data bits into a signal for transmission over the communications channel (cable), which has independent jitter and timing characteristics from the inbound signal.

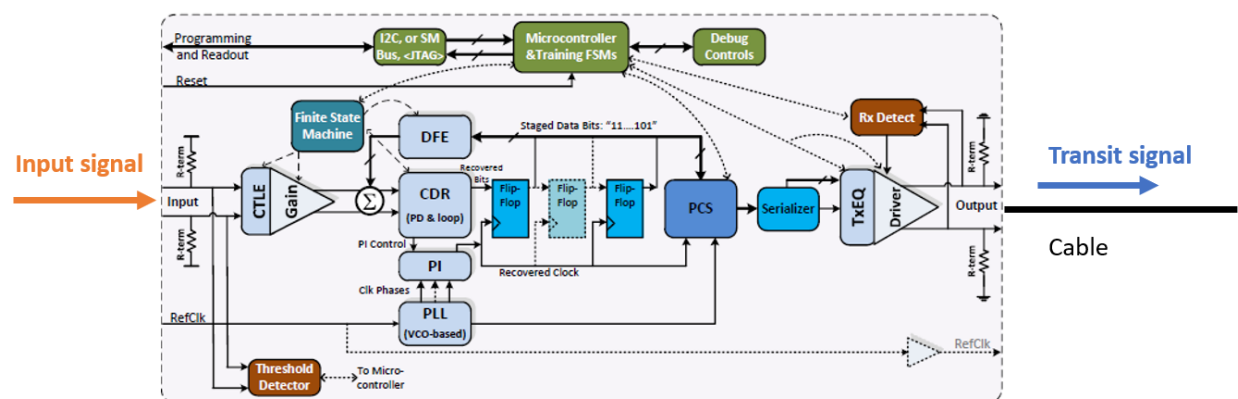
91. Similarly, with Samaan’s additional retimer details, each transceiver extracts and re-modulates the inbound data stream. For example, each retimer performs clock and data recovery (“CDR”) to extract “data bits” (stored in flip flops) from the inbound data stream. Ex-1007, ¶202 (“Re-timer has a Clock Data Recovery circuit.... A re-timer converts an incoming analog bit stream into purely digital bits that are stored (staged) internally.”), ¶¶203-207, ¶¶208-212, ¶¶216-217 (“...CDR is a circuit which can extract both clock and the data from an incoming (specially-encoded) data stream.”), Figs.34-35. Next, the retimer re-modulates the

⁶ Patent Owner has taken the position that limitation [1c] is satisfied by the presence of retimers in an active cable. Ex-1024, 000004-5 (highlighting and pointing to Credo’s retimers and their “retiming” capability as evidence of remodulation and data extraction); Ex-1022, 000004-9 (same, highlighting and pointing to Broadcom’s and Marvell’s retimers); Ex-1023, 000004-9 (same).

digital bitstream and “re-transmits the digital data anew.” Ex-1007, ¶202, ¶15. For this re-modulation process, the data signal flows through TxEQ for output equalization and then the driver. Ex-1007, ¶¶216-231, Fig.34:



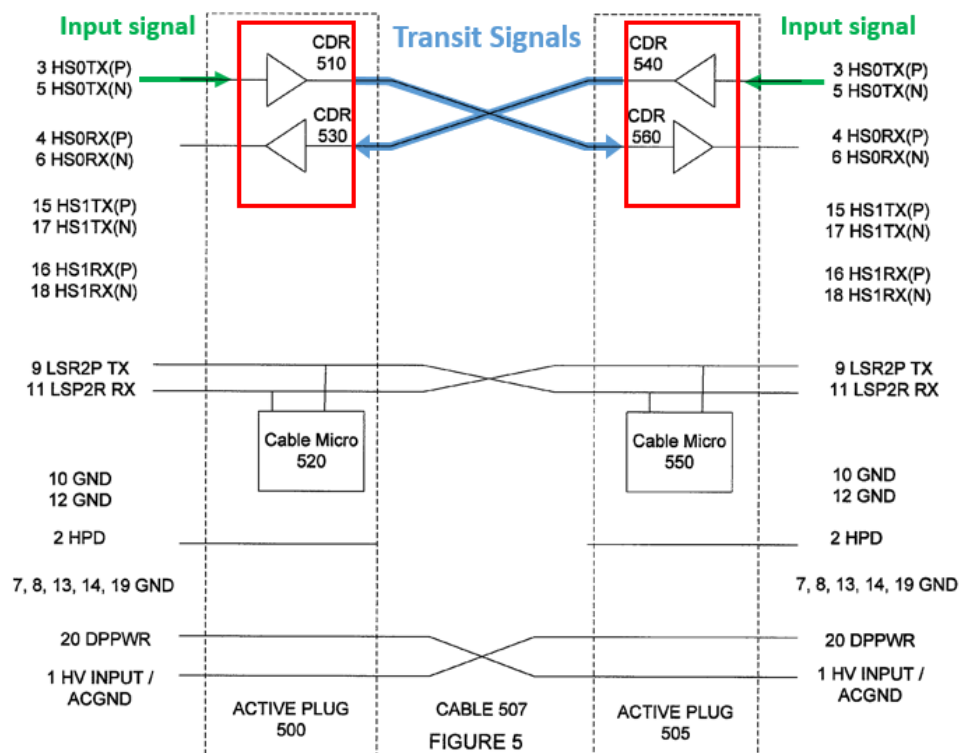
For the remodulation process, Samaan’s protocol-aware retimers follow the same steps, but the data signal additionally flows through the physical coding/decoding sublayer (PCS) and serializer before entering TxEQ and the driver. Ex-1007, ¶¶218-231, Fig.35:



Both retimer architectures re-modulate the inbound data stream by converting the extracted data bits from the inbound data stream into a signal for transmission over

the communications channel (cable), which has independent jitter and timing characteristics from the inbound signal. Ex-1007, ¶15, ¶202.

92. The data stream is extracted and re-modulated **for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream**. For example, the retimed outputs of CDR 510 and CDR 540 are transmitted across cable 507, which, as explained above, comprises electrical conductors; therefore, the outputs are electrical transit signals. Ex-1006, 6:21-29, 7:26-41 (“copper or other conductor...in the cable itself.”), Fig.5:



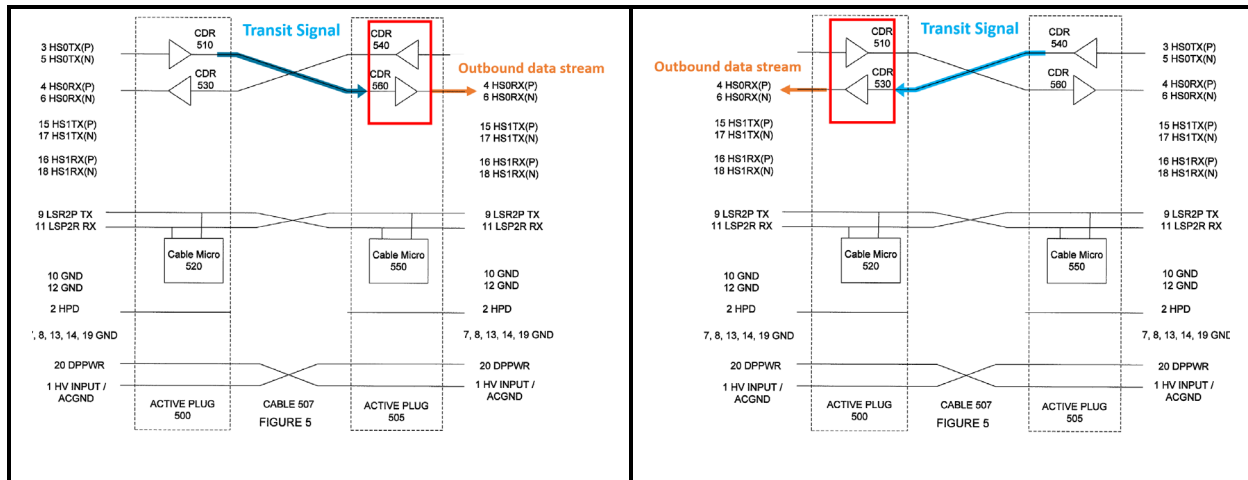
See also above §V.A.3[1a]. Each transit signal conveys a transit data stream that represents a stream of data in transit over the cable comprising the data that was

sent from the host to the active plug. Cornelius' CDR "retime[s] signals received at an input" and sends them over the cable. Ex-1006, Claim 1, 6:11-24, 8:20-26, Figs.5-6. Samaan likewise teaches that the retimer "re-transmits the digital data anew." Ex-1007, ¶202.

93. For at least these reasons, Ground 1 teaches [1c].

[1d] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, and

94. Ground 1 teaches **the respective transceiver for each of the first and second connectors (e.g., active plugs) performing clock and data recovery on the respective electrical transit signal**. As I explained for [1c], each active plug includes a transceiver: Cornelius's dual CDR/retimer circuitry, combined with additional details from Samaan's retimer architectures. *See* above at §V.A.3[1c]. The dual CDR/retimer circuitry in each active plug performs a variety of functions (Ex-1006, 6:30-33) and is a transceiver because it receives a signal (e.g., the transit signal that crossed the cable) and transmits a signal (e.g., the output signal to the host). *See* above at §V.A.3[1c]; Ex-1006, 6:11-24, Figs.6, 5:

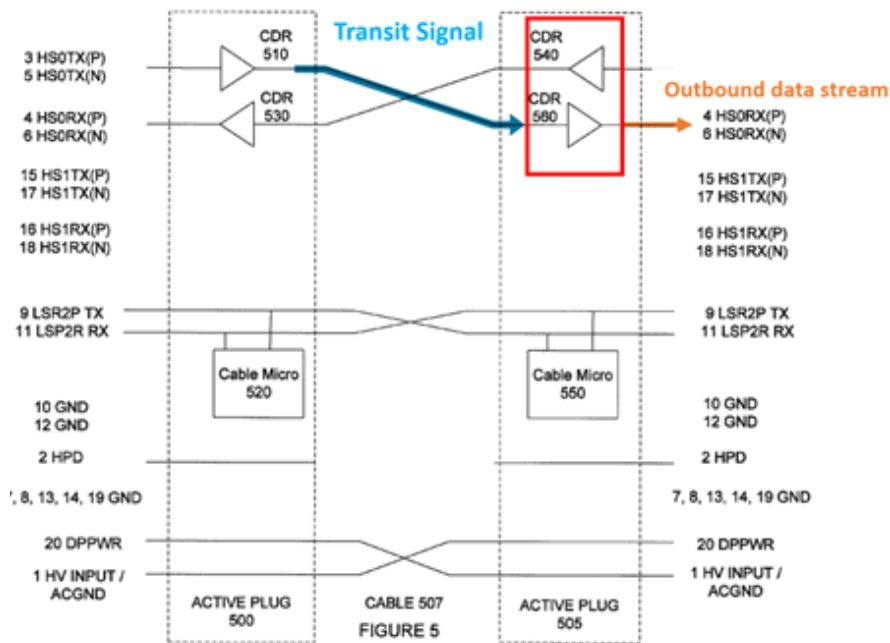


95. The dual CDR circuitry in each plug receives the electrical transit signal that was sent across the cable (Ex-1006, 6:11-32, claims 1, 6, Figs.5-6), performs CDR on that signal, and retimes it. Ex-1006, 6:6-10, 14-16, claims 1, 6.

96. The transceivers perform CDR to **extract and re-modulate the transit data stream as the outbound data stream from the cable**. For example, Cornelius performs clock and data recovery, which extracts bits from the transit data stream; the CDR component then “retime[s]^[7] signals received from the cable” which is the transit signal. Ex-1006, claim 1, 6:11-24, 8:20-26. Therefore, Cornelius re-modulates the transit data stream by converting the extracted data bits into a signal for transmission over the communications channel (cable), which has independent jitter and timing characteristics from the inbound signal.

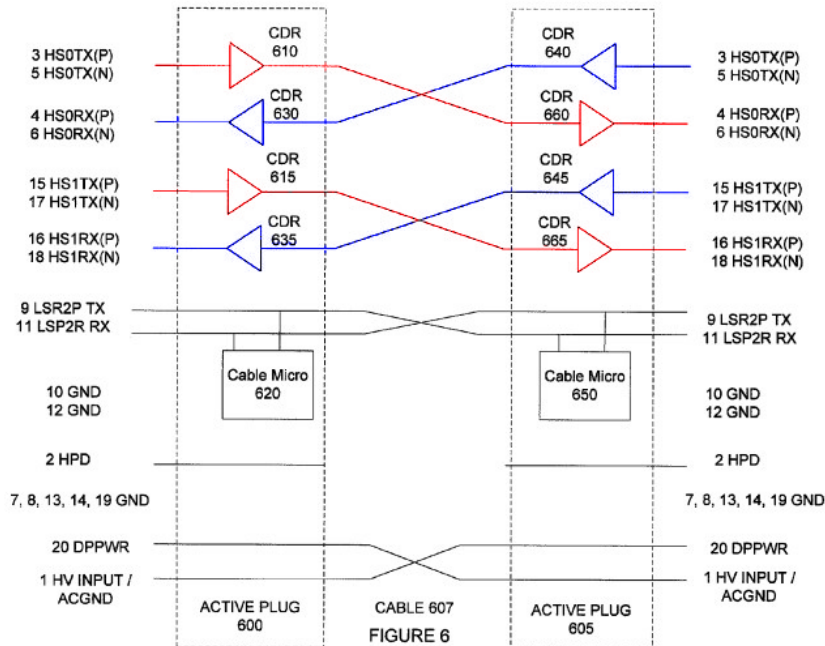
⁷ Patent Owner has taken the position that limitation [1d] is satisfied by the presence of retimers in an active cable. Ex-1024, 000006-7 (highlighting and pointing to Credo’s retimers and their “retiming” capability as evidence of remodulation and data extraction); Ex-1022, 000009-12 (same, highlighting and pointing to Broadcom’s and Marvell’s retimers); Ex-1023, 000009-12 (same).

97. Cornelius explains CDR circuit 560 receives the transit data stream in the electrical transit signal transmitted from CDR circuit 510 via cable 507. Ex-1006, 6:11-24, claim 1, Fig.5. Following extraction and remodulation at CDR 560 (and 530), the remodulated data stream is output on pins 4 and 6 as the outbound data stream from the active cable. Ex-1006, 6:11-24 (“high-speed signals on pins 4 and 6.”), Fig.5:



98. Cornelius’ Figure 5 above only shows two CDR circuits in each active plug. Ex-1006, Fig.5, 6:11-24. Cornelius explains that, from the host’s perspective, pins 3 and 5 carry high-speed transmission signals (to CDR 510), while pins 4 and 6 carry high-speed receive signals (from CDR 530). In Figure 6, as shown below, “additional clock and data recovery circuits 615 and 635 have been added to active plug 600, while clock and data recovery circuits 645 and 665 have been added to

active plug 605.” *Id.*, 8:20-26, Fig.6. Accordingly, from the cable’s perspective, active plug 600 carries high-speed transmission signals on pins 3, 5, 15 and 17 (CDRs 610 and 615), and carries high-speed signals on pins 4, 6, 16 and 18 (CDRs 630 and 635). *See Id.*

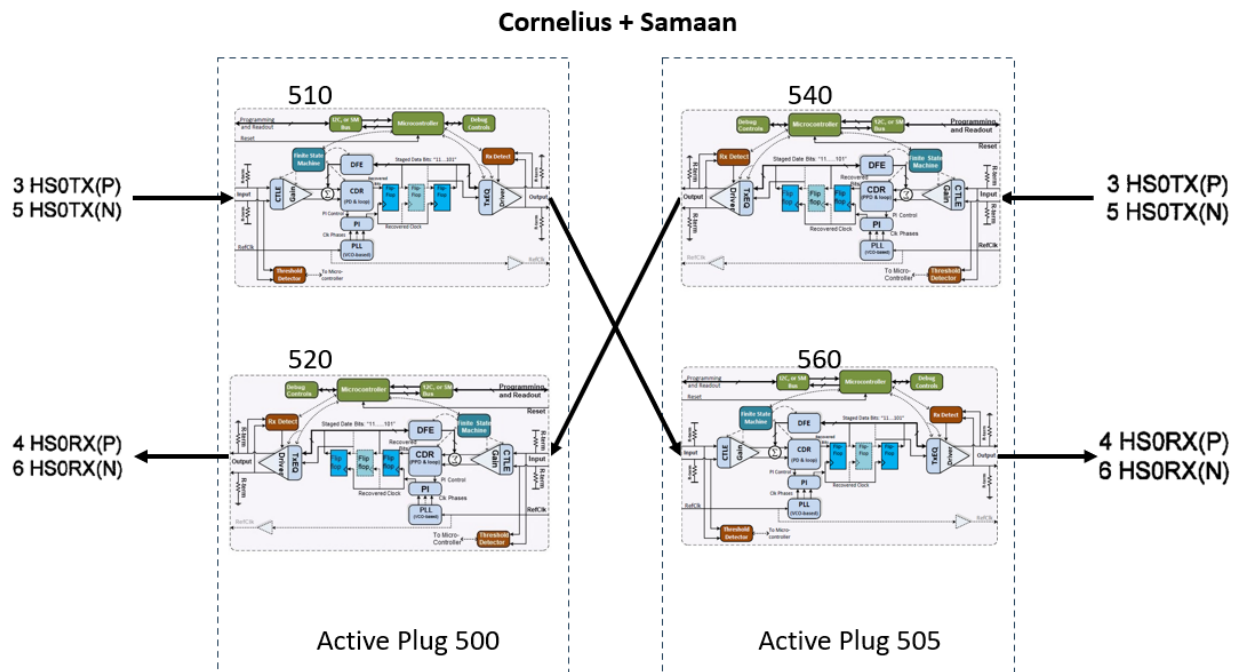


99. When Cornelius’s figures and specification are considered together, it is clear that data flows from CDR 610 to 660 (510 to 560 in Figure 5) and from CDR 640 to 630 (540 to 530 in Figure 5), following the direction of the arrows, which is the normal convention in the field, and transmitted signals (from the host) are provided on pins 3, 5, 15, and 17 and received signals (by the host) are on pins 4, 6, 16, and 18.

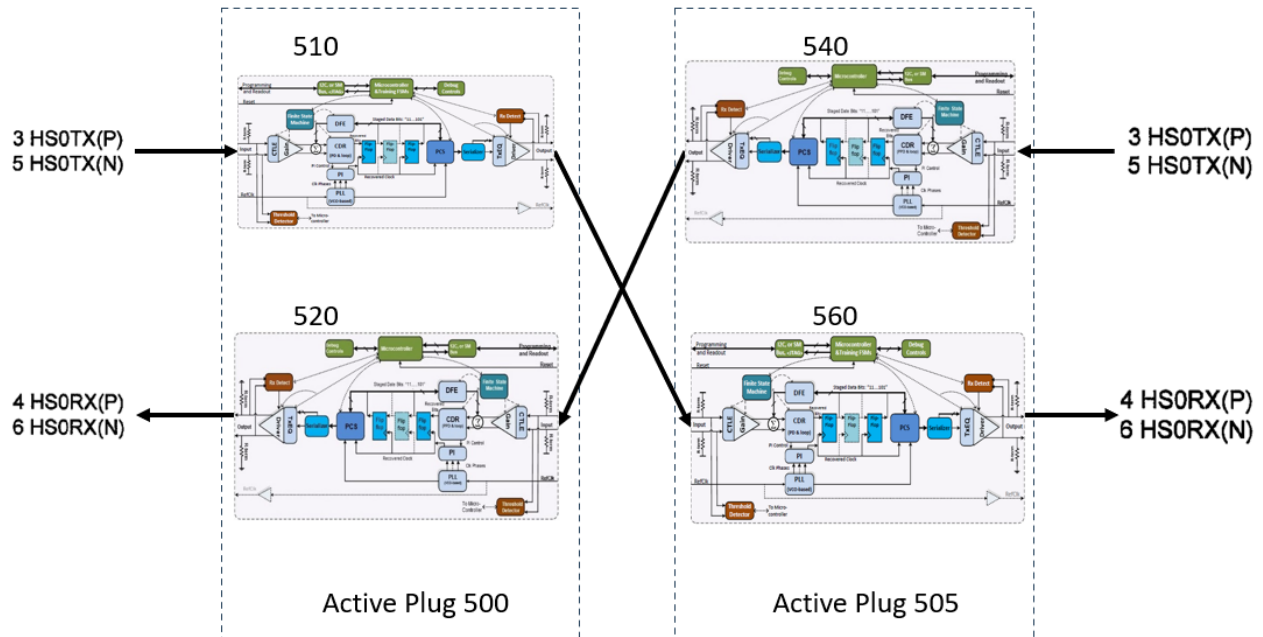
100. Cornelius’ cable is bidirectional and the same process is mirrored in the other direction for CDR 530 that retimes the transit data stream received over

cable 507 and outputs an outbound data stream to pins 4 and 6 of active plug 500 connected with the host device on the left. Ex-1006, 6:11-20, Fig.5.

101. Additionally, I explained above how and why a POSITA would have applied Samaan's retimer teachings to Cornelius's active plugs; that analysis applies here. *See* above §V.A.3[1pre] (Motivation subsection explaining how and why Cornelius and Samaan would be combined), §V.A.3[1c] (applying Samaan's retimer teachings to Cornelius)); Ex-1006, Fig.5; Ex-1007, Figs.34, 45.

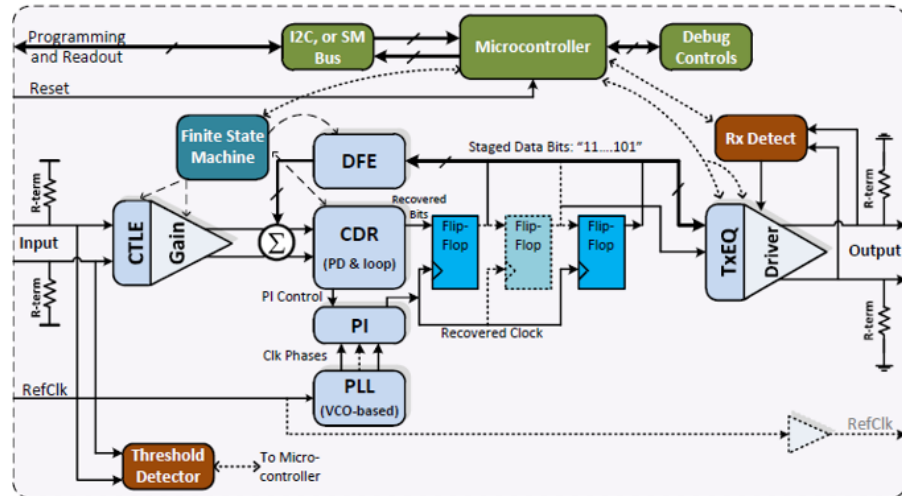


Cornelius + Samaan

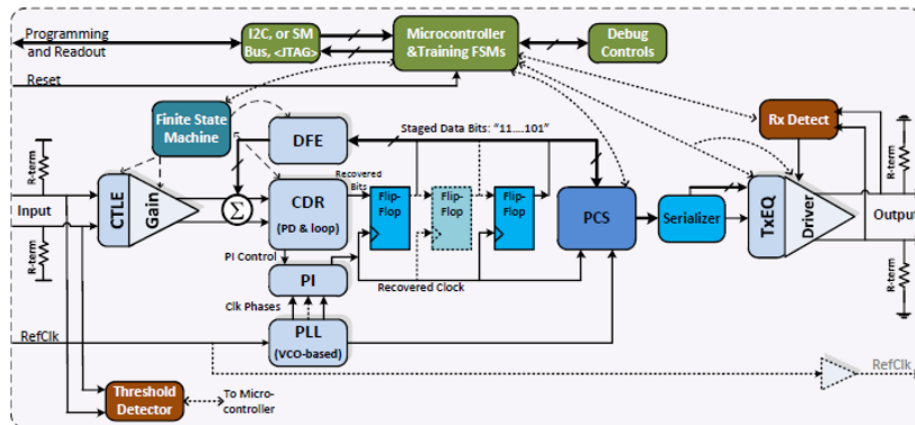


102. Cornelius+Samaan teaches [1d] in a similar manner as already explained for [1c], but with the input being the transit signal from the cable and the output going to the respective host; therefore, the previous analysis for extraction and remodulation apply here. *See* above §V.A.3[1c]. Cornelius+Samaan teaches each active plug including a transceiver (e.g., the retimers, collectively, in each plug) that performs “CDR” on the electrical transit signal that crossed the cable, which arrives as input to the retimer, to extract “data bits” (stored in flip-flops) from that signal and re-modulate the transit data stream as the outbound data stream from the cable (the output of the retimer, which exits the plug on pins 4, 6). Ex-1007, ¶202 (“A Re-timer has a Clock Data Recovery circuit.”), ¶15, ¶203-212, ¶¶216-217 (teaching CDR in its retimer architectures), Figs.34-35. For this re-

modulation process, the data signal flows through TxEQ for output equalization and then the driver. Ex-1007, ¶¶217-231, Fig.34:



For the remodulation process, Samaan's protocol-aware retimers follow the same steps, but the data signal additionally flows through the physical coding/decoding sublayer (PCS) and serializer before entering TxEQ and the driver. Ex-1007, ¶¶218-231, Fig.35:



Both retimer architectures re-modulate the input transit stream by converting the extracted data bits from the stream into a signal for transmission over the

communications channel to the host, which has independent jitter and timing characteristics from the input transit signal. Ex-1007, ¶¶15-16, ¶¶202-208.

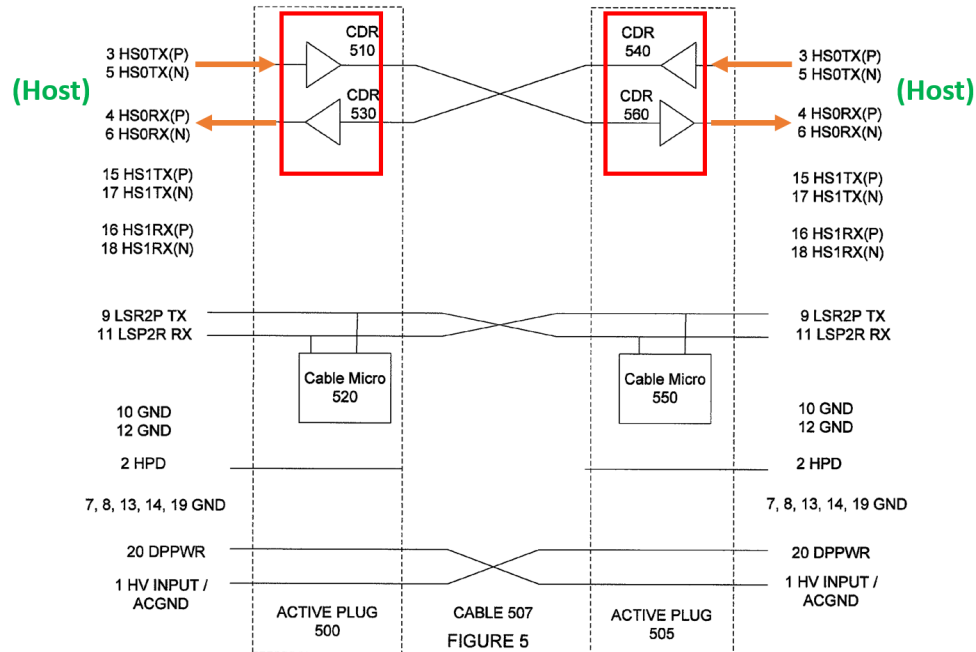
103. **Motivation to Combine.** I explained how and why a POSITA would have been motivated to combine Cornelius' active plug and cable teachings, including its CDR circuits, with Samaan's retimer teachings. *See above* §§V.A.3[1pre], [1b] (motivation to combine subsections). As I explained above, a POSITA would have been motivated to apply Samaan's retimer teachings to Cornelius' active cables, to function in place of Cornelius' CDR circuits. *Id.* The same reasons apply here. Moreover, Cornelius teaches CDR circuits "employ[ing] equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate." Ex-1006, 6:30-33. Because Cornelius contemplates the use of such circuitry found within Samaan's retimers in its CDR circuits, a POSITA would have found it obvious to use Samaan's retimers in Cornelius' active plugs. This would have been a simple substitution of one known element for another to obtain predictable results.

104. I also explained how the combination would not change the principle of operation for each reference and how a POSITA would have had a reasonable expectation of success in making the combination. *See above* §§V.A.3[1pre], [1b] (motivation to combine subsections). The same analysis applies here for the reasons explained above.

105. For at least these reasons, Ground 1 teaches [1d].

[1e] the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.

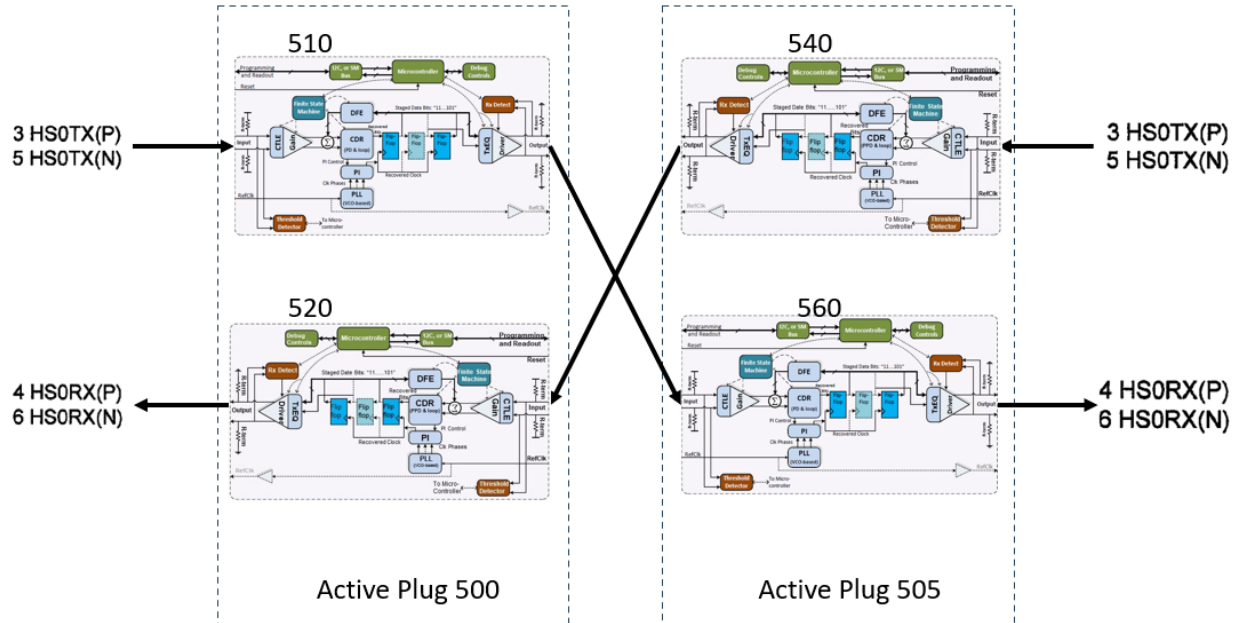
106. Ground 1 teaches **the respective transceivers each employing equalization parameters for the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.** For example, each transceiver (explained above, *see* §§V.A.3[1c]-[1d]) employs equalization for signals exchanged with the host. Cornelius explains how its “CDR” component retimes data (Ex-1006, 6:15-16) and employs “equalizer circuits, buffers, emphasis, and de-emphasis circuits[.]” Ex-1006, 6:30-33; *see* above §V.A.3[1c]. Inbound and outbound signals are exchanged with the host on pins 3-6. *See* above §V.A.3[1b].



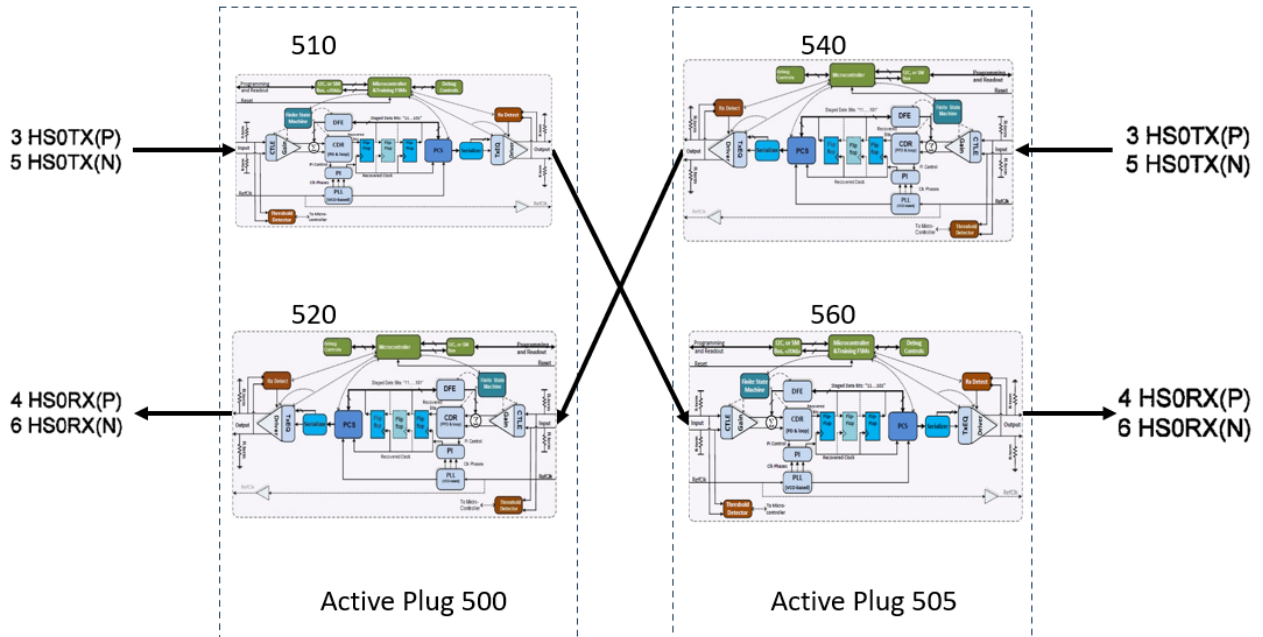
107. Ground 1 also applies Samaan’s retimer teachings (*see* above §V.A (explaining combination), §V.A.3[1pre] (Motivation subsection explaining how and why Cornelius and Samaan would be combined), §V.A.3[1c] (applying Samaan’s retimer teachings to Cornelius)), each transceiver uses transmit linear equalization (TxEQ) on transmitted signals and other equalization on received signals, for example, continuous time linear equalization (CTLE) and discrete feedback equalization (DFE). Ex-1007, ¶4 (TxEQ), ¶204, ¶208, ¶20 (CTLE), ¶207, ¶215, ¶¶216-217, ¶8 (DFE), ¶¶219-221. Each of these equalization functions employ parameters that control the equalization. *E.g.*, Ex-1007, ¶221 (“This digital state machine usually has a proprietary algorithm which manages adjusting the input Gain (AGC), CTLE, DFE settings, and other parameters,”) ¶215, ¶¶20-21

(CTLE's “programmed” “setting”), ¶220 (“amplitude of each DFE tap” and “number of DFE taps”), ¶¶225, ¶¶26-27, Figs.34-35; Ex-1006, Fig.5.

Cornelius + Samaan

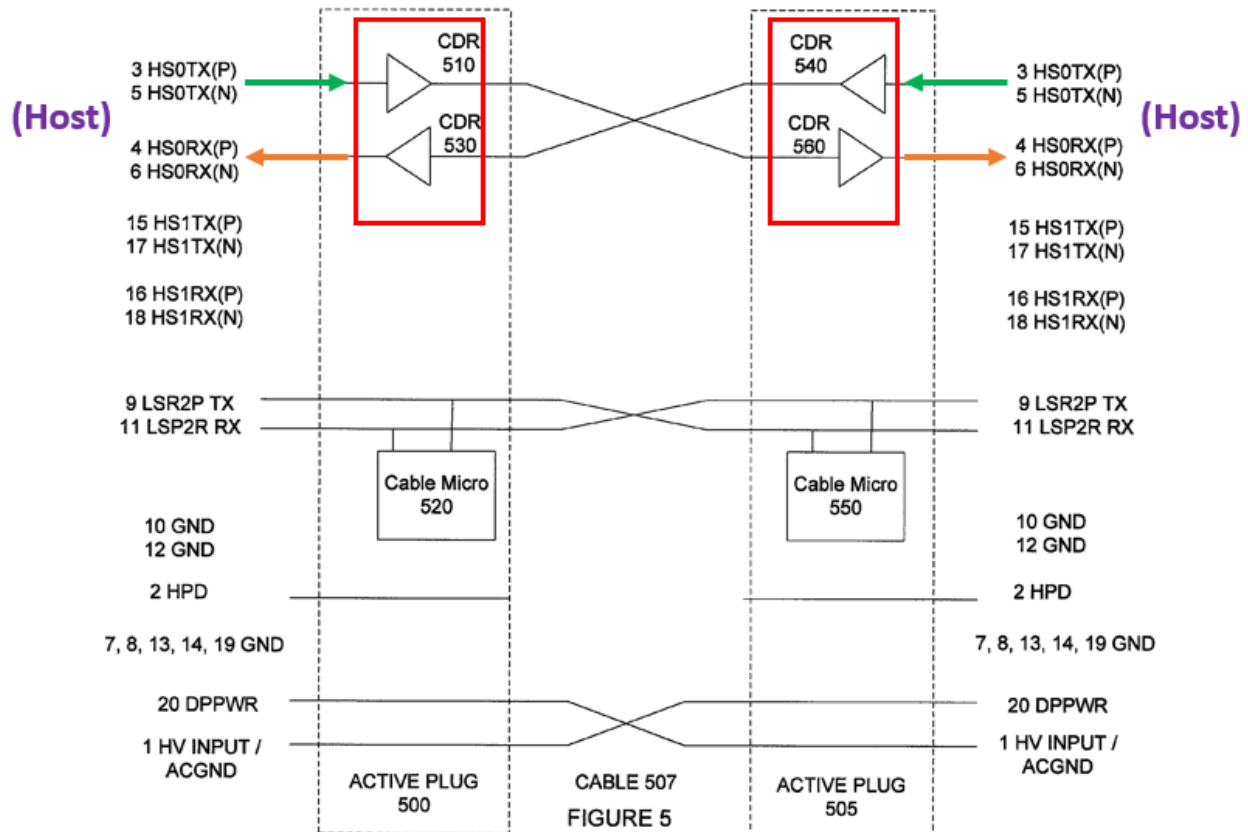


Cornelius + Samaan



108. Cornelius teaches **employing fixed, cable-independent equalization parameters**. Cornelius teaches calibrating equalization circuitry, which “may be adjusted using various parameters.” Ex-1006, 11:45-52. Next, Cornelius teaches two approaches for setting the parameters. First, the “parameters for these circuits may be calibrated or otherwise determined by the manufacture[r] and stored as presets for loading during operation.” *Id.*, 11:52-55. Second, “[i]n other embodiments...these parameters may be determined while the system is connected” including “during power up, restart, or other periodical or event-based time.” *Id.*, 11:55-59. Therefore, Cornelius teaches two distinct approaches. One employs parameters fixed at manufacturing; these do not change during normal usage of the cable because Cornelius presents it as an alternative embodiment to parameters that are determined/trained when the cable is connected. *Id.*, 11:52-59.

109. Cornelius teaches using these routines—including the manufacturer presets approach—for host-side paths, “to calibrate the path from a host to a near end of the cable,” and, for the other plug, “the path from the cable to a device or other host.” Ex-1006, 11:59-62. The calibration of these equalization parameters does not depend on any characteristics of the connecting cable because Cornelius teaches that they are for paths on the host side of a transceiver, meaning PCB traces to/from the host chip, rather than the path through the cable (507). *Id.*, Fig.5:



110. Equalization parameters for these signal paths account for channel properties on the host-side path.⁸ They do not compensate for cable paths and do not depend on the properties of any particular connecting cable.⁹ Ex-1006, Figs.5-

⁸ Patent Owner argued that parameters for these host-side paths satisfy cable-independent parameters because they “are independent of communications through the cable”. Ex-1022, 000014-15 (pointing to pre-equalized filters for “chip-to-module connection,” which refers to the path from the host to the closest transceiver); *see also* Ex-1023, 000017-9 (same); Ex-1024, 000009-10 (same).

⁹ Patent Owner alleged that allowing the host to select from a fixed, pre-defined set of equalization parameters makes them cable-independent. Ex-1022, 000016-18 (pointing to the “pre-determined or host-provisioned” Tx input and Rx output equalizations of CMIS); *see also* Ex-1023, 000019-21 (same); Ex-1024, 000011-13 (same).

6. Accordingly, it would not have made sense to customize these parameters for individual cables, given Cornelius's teachings of fixed parameters, set by the manufacturer for paths that are independent of individual cables, and Cornelius's teaching of preset parameters as an alternative to determining the parameters during cable operation. Ex-1006, 11:45-62. To customize the parameters for individual cables, the parameters would need to be tested on an assembled cable, while the cable is "connected," to measure the particular channel characteristics of the individual cable; Cornelius teaches this as an alternative to preset parameters. *Id.* Therefore, Cornelius teaches or suggests fixed, cable-independent parameters for host-side equalization that are preset during manufacturing and not customized for individual cables. *Id.*

111. **Motivation to Combine.** While Cornelius teaches alternative approaches for equalization parameters, a POSITA would have been motivated, and found it obvious, to apply Cornelius's teachings of using pre-set equalization parameters for host-side paths that are stored during manufacturing and not customized on a cable-by-cable basis when the cable is connected. Ex-1006, 11:45-62. As explained above, this is the most sensible approach for host-side paths whose channel characteristics do not depend on the connecting cable. Cornelius presents this as one of a finite number of options (two in total), and a POSITA would have had ample reason to choose preset parameters with a reasonable

expectation of success because it simply required storing the same parameters across cables. Therefore, a POSITA would have found it sufficient and obvious, as a matter of common sense, to simply use the same preset equalization parameters for these host-side equalization for all cables, rather than to customize them. Moreover, A POSITA would have been motivated to apply Cornelius’s teachings of pre-set parameters because it was a common approach in the art, and the prior art provides motivation to apply this textbook approach. Ex-1020, 000020-21 (“FFE tap weights are determined for many applications by design and coded as fixed values within system software”); Ex-1021, 7:18-26 (“coefficients of the tap(s)...may be pre-programmed or pre-set”), 1:65-67 (FIR filter “typically includes a one or more taps having fixed or pre-programmed...coefficients.”). As another example, SFF-8636—a widely adopted standard for SFP+ environments—required preset input and output equalization levels. Ex-1032, 000012, Tbls. 39-40:

TABLE 39 - INPUT EQUALIZATION (ADDRESS 234-235)

Code	Transmitter Input Equalization	
	Nominal	Units
1xxx	Vendor Specific	
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	dB

TABLE 40 - OUTPUT DE-EMPHASIS CONTROL (ADDRESS 236-237)

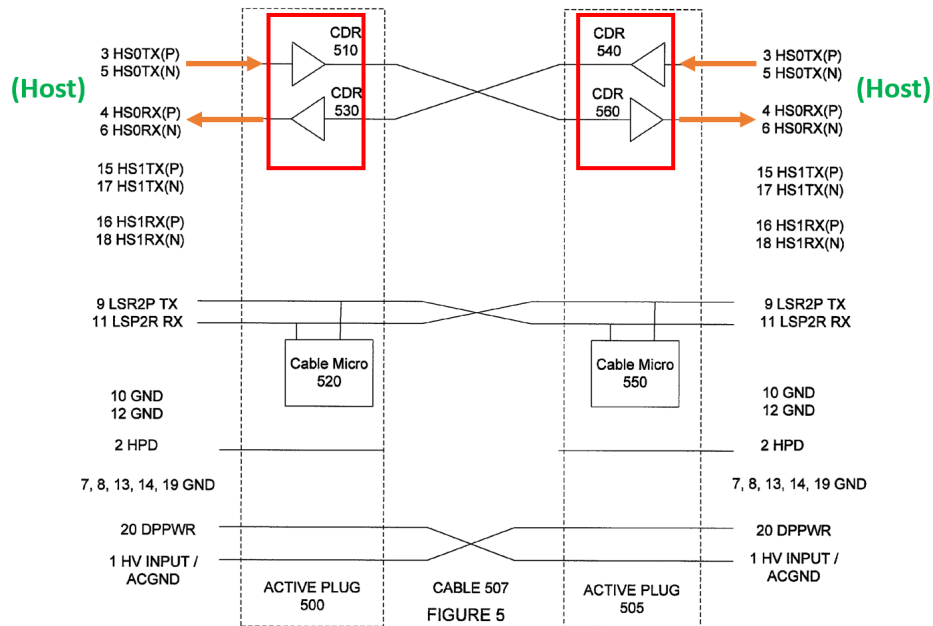
Code	Receiver Output De-emphasis At nominal Output Amplitude	
	Nominal	Units
1xxx	Vendor Specific	
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	dB

Given the widespread use of preset equalization parameters, a POSITA would have recognized the advantages of implementing specified equalization presets to improve device compatibility across various environments. Therefore, a POSITA would have been motivated to apply Cornelius's preset teachings by calibrating the host-side equalization parameters once for a given active cable design and then, during manufacturing, use those same parameters across all active cables of that design. *See* Ex-1006, 11:59-62.

112. For these particular host-side paths in Cornelius's active cable, Cornelius teaches two approaches, and a POSITA would have been motivated to use the first approach with preset coefficients. Doing so would have been simpler and more cost-effective than customizing the parameters for every individual active cable, because these host-side parameters operate on host-side traces and are not affected by differences in cable characteristics. Ex-1006, 11:45-62. In more

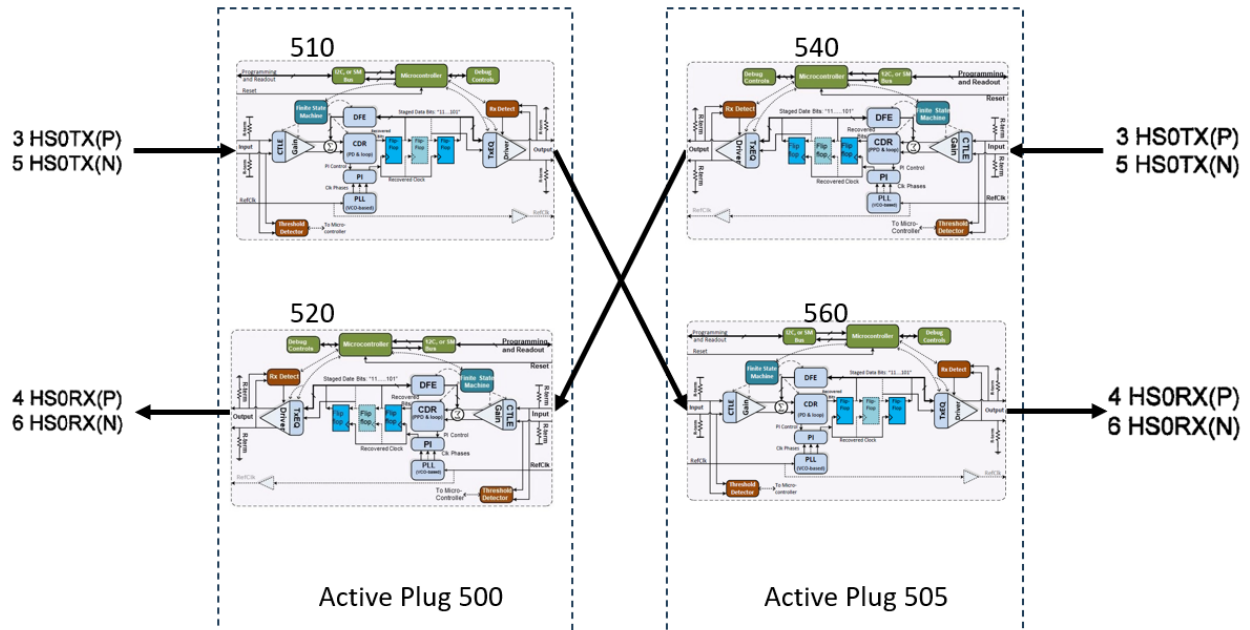
generic circumstances, retimer designs may incorporate more complex training or adaptation features to handle a range of unknown channels, such as when used in the middle of a long backplane or between two long passive cables. For these multi-purpose retimer designs, the increased time, cost, and complexity of advanced training/adaptation algorithms can be justified. However, for Ground 1, Cornelius teaches a specific active cable application where retimers serve a defined purpose in each active plug. In this context, Cornelius teaches that either of two approaches can be used. Ex-1006, 11:51-59. And as explained above, these particular host-side paths are well-suited for Cornelius's first approach—using preset equalization parameters—because they involve short paths to a nearby host chip rather than long cable distances. Therefore, a POSITA would have been motivated to simply use preset equalization parameters as discussed.

113. The equalization parameters are employed **for each of the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal**. As explained above, the equalization discussed in this section is host-facing, which applies to the electrical input signal received from the host and the outbound data stream transmitted to the host (Ex-1006, Figs.5-6), and Ground 1 uses equalization for received and transmitted signals, including those received from, and sent to, a host.

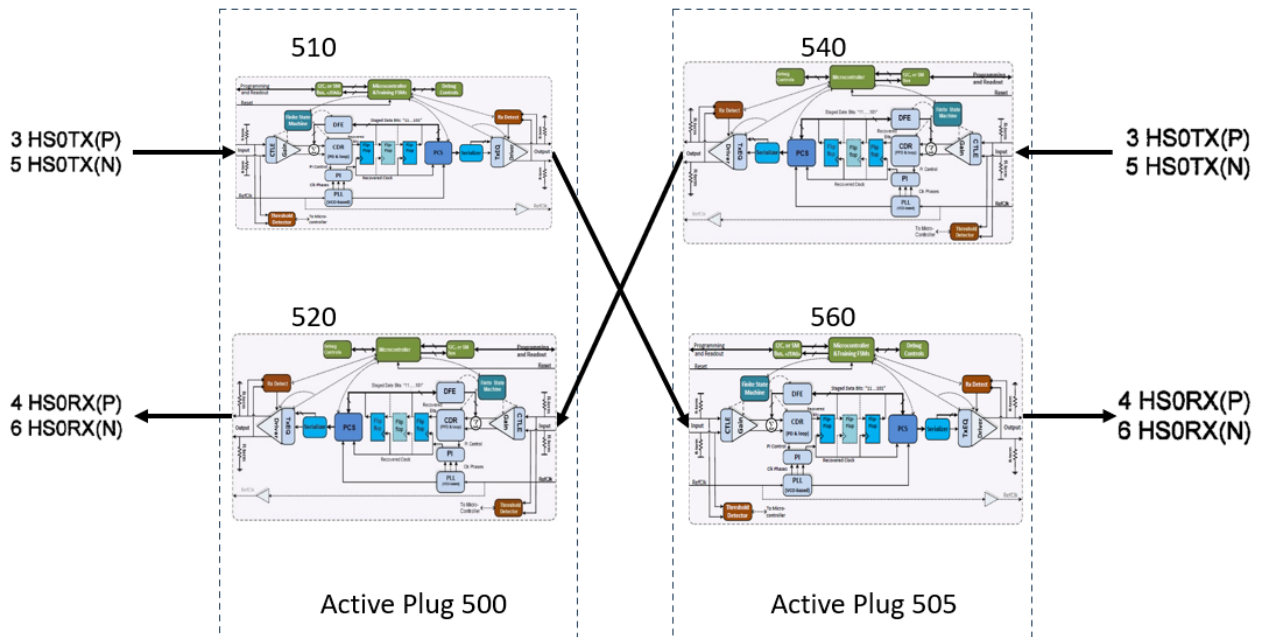


114. When applied to Cornelius' active cable, Samaan's retimer architecture applies equalization (e.g., TxEQ) to the remodulated outbound data stream to the host and equalization (e.g., CTLE and DFE) for the CDR performed on the electrical input signal from the host. Ex-1007, Figs.34-35; Ex-1006, Figs.5-6.

Cornelius + Samaan



Cornelius + Samaan



115. I previously explained the remodulation of the transit data stream as the outbound data stream (*see above §§V.A.3[1d]*) and the clock and data recovery performed on the electrical input signal (§V.A.3[1c]).

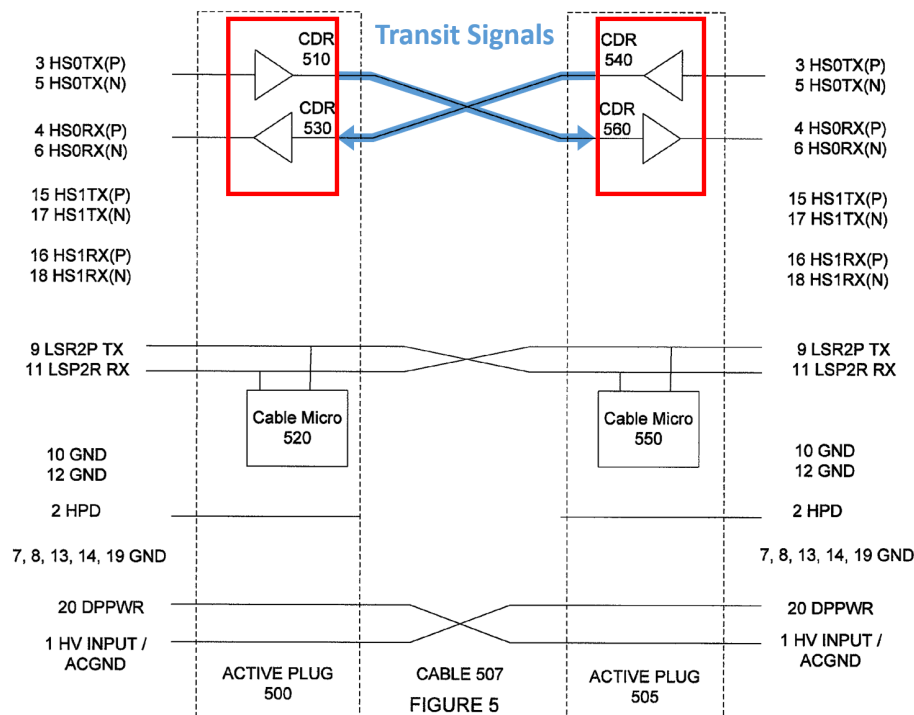
116. For at least these reasons, Ground 1 teaches [1e].

4. Dependent Claim 2

2. The active Ethernet cable of claim 1, wherein the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal.

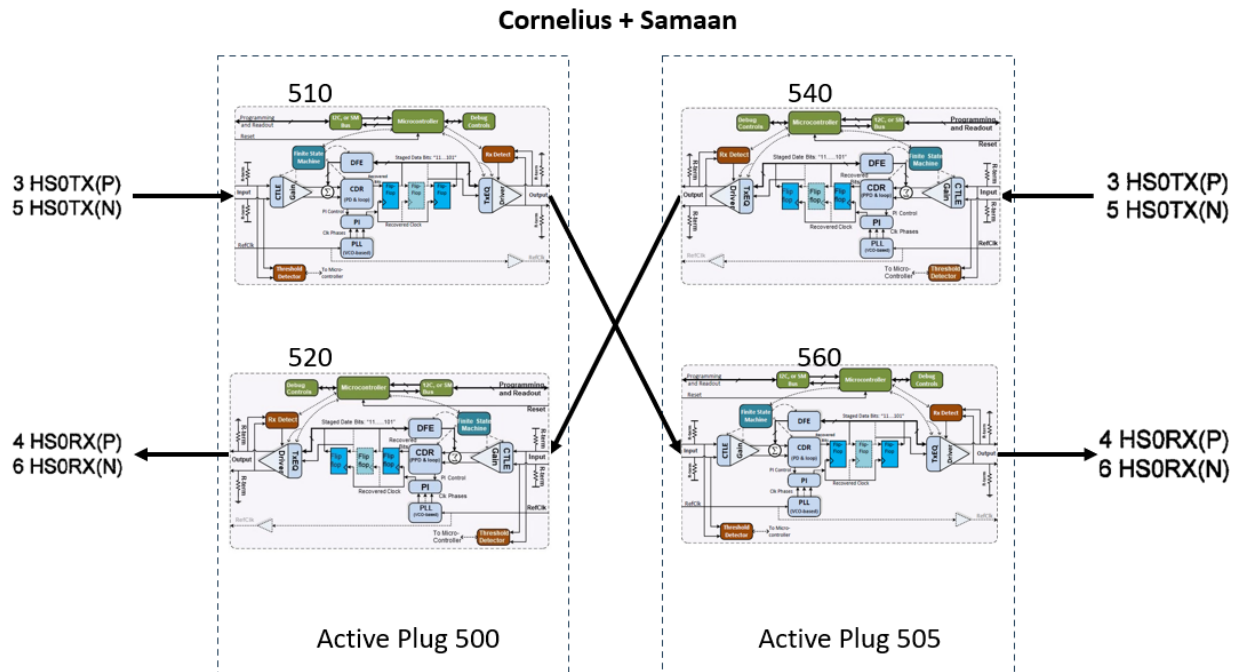
117. As an initial matter, Ground 1 teaches respective transceivers (e.g., dual CDR/retimer circuitry) each employ equalization parameters. *See* above §V.A.3[1e]. And I previously explained the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal. *See* above §V.A.3[1c] (explaining the remodulation of inbound data stream), §V.A.3[1d] (explaining the CDR of the electrical transit signal).

118. Each transceiver (explained above, *see* §§V.A.3[1c]-[1d]) employs equalization for the transit signals exchanged over the cable. Cornelius’ “CDR” components retime data (Ex-1006, 6:15-16) and employ “equalizer circuits, buffers, emphasis, and de-emphasis circuits[.]” Ex-1006, 6:30-33, Fig.5; *see* above §V.A.3[1c].

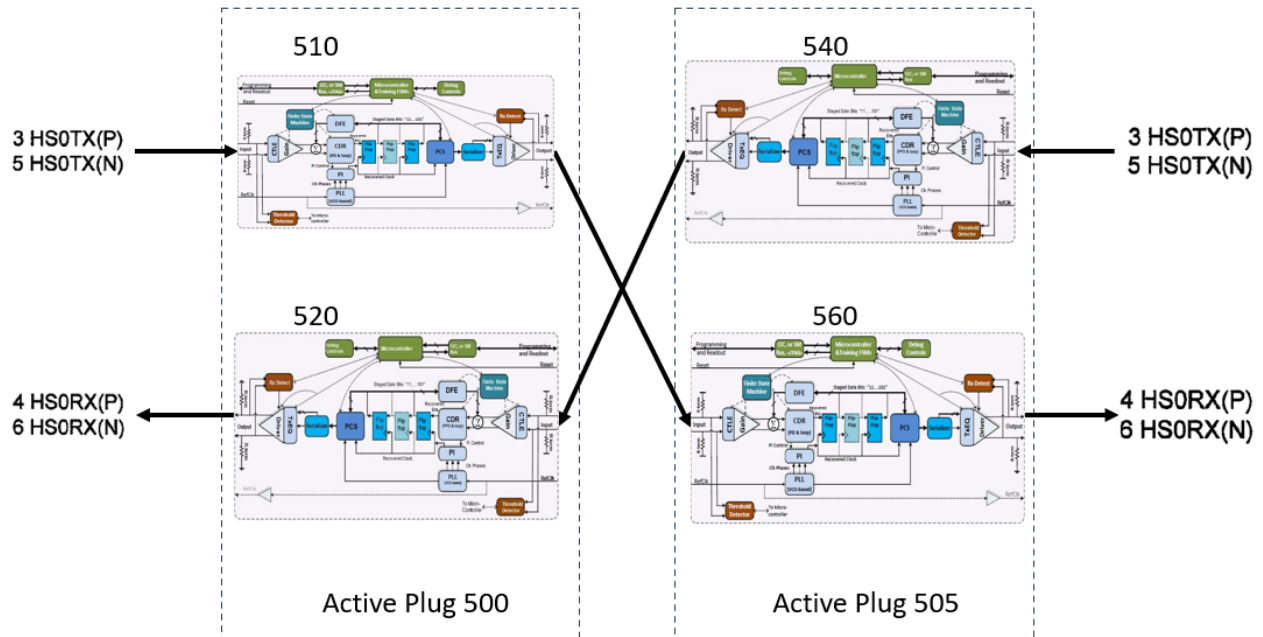


119. Similarly, when combined with Samaan’s additional retimer details (see above §V.A.3[1pre] (Motivation subsection explaining how and why Cornelius and Samaan would be combined), §V.A.3[1c] (applying Samaan’s retimer teachings to Cornelius)), each transceiver uses transmit linear equalization (TxEQ) on signals output for transmission over the cable and other equalization on transit signals received from the cable, for example, continuous time linear equalization (CTLE) and discrete feedback equalization (DFE). Ex-1007, ¶4 (TxEQ), ¶204, ¶208, ¶20 (CTLE), ¶207, ¶215, ¶¶216-217, ¶8 (DFE), ¶¶219-221. For the remodulation of transit signals, Samaan teaches equalization (e.g., TxEQ); for CDR of transit signals, Samaan teaches equalization (e.g., CTLE and DFE). *Id.* Each of these equalization functions employs parameters. *E.g., Id.*, ¶221 (“This

digital state machine usually has a proprietary algorithm which manages adjusting the input Gain (AGC), CTLE, DFE settings, and other parameters”), ¶215, ¶¶20-21 (CTLE’s “programmed” “setting”), ¶220 (“amplitude of each DFE tap” and “number of DFE taps”), ¶225, ¶¶26-27.



Cornelius + Samaan



120. Cornelius teaches the additional limitation of employing **cable-dependent equalization parameters** for the remodulation and clock and data recovery that I just discussed. As an initial matter, Cornelius teaches calibration routines that adjust the equalizer parameters, calibrating them to “the path through the cable.” Ex-1006, 11:45-62. These equalization parameters compensate for the loss characteristics of individual cables and depend on the characteristics of that particular connecting cable.

121. Indeed, Cornelius teaches parameters being determined “while the system is connected”; “[t]his training or calibration may occur during power up, restart, or other periodical or event-based time.” Ex-1006, 11:55-59. Additionally, Samaan teaches on-the-fly training that changes starting parameters “in search of better ones.” Ex-1007, ¶127. Samaan teaches equalizer adaptation routines that

“adjust the link partner’s TxEQ...to an optimal value for their receiver, and for the specific channel and operating conditions at hand.” *Id.*, ¶78, ¶208. Therefore, Cornelius and Samaan both teach determining equalization parameters when an individual cable is connected and in operation; therefore, the parameters are customized for each individual cable. Accordingly, Ground 1 teaches employing cable-dependent equalization parameters (for communications over the cable) that are determined during cable operation and therefore trained based on the particular characteristics of the cable and customized on a cable-by-cable basis.

122. **Motivation to Combine.** I previously explained why and how a POSITA would have been motivated to combine Cornelius and Samaan. *See* above §V.A.3[1pre] (Motivation subsection explaining how and why Cornelius and Samaan would be combined), §V.A.3[1c] (applying Samaan’s retimer teachings to Cornelius). A POSITA would have found it obvious and been motivated to combine the above-described teachings from Cornelius and Samaan to determine equalization parameters on an actual active cable that has been assembled and connected. This was advantageous because the transmission characteristics (e.g., signal attenuation, noise susceptibility) of the path through the cable varies from cable to cable. Unlike the host-side paths, which are normally inches long, cables were typically several feet or longer, exacerbating physical differences. Due to manufacturing variation, the exact physical properties such as length and width

will vary from cable to cable, and their effect on signal loss will therefore vary between cables. The components in the active plugs, including the filters in the transceivers will also vary in operation due to impurities and silicon manufacturing variations. The conventional approach to addressing all these variations in cables was to use calibration/training techniques on an actual connected cable, which would include on-the-fly training as Samaan teaches or alternatively calibration at some other “event-based time” as Cornelius teaches. Ex-1006, 11:55-59. In either case, the equalization parameters are tailored to the particular cable. This would have been particularly beneficial for usage models that demand maximum performance, high data throughput, or extended cable lengths. For example, this would benefit data centers with long cable lengths or high bitrates by more accurately compensating for cable-specific losses and thereby improving signal quality.

123. For at least these reasons, Ground 1 teaches Claim 2.

5. Dependent Claim 3

3. The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters adapt during usage of the Ethernet cable.
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124. As I explained above for claim 2, Cornelius and Samaan teach cable-dependent equalization parameters that are adapted to the cable using calibration routines during usage of the cable. *See* above §V.A.4.

125. Ground 1 teaches the additional limitation of claim 3. As I explained, Cornelius and Samaan teach cable-side parameters that are determined during cable operation and therefore trained based on the particular characteristics of the cable. For example, Cornelius teaches using its calibration routines to determine the equalization parameters “while the system is connected,” e.g., the cable is connected between hosts. Ex-1006, 11:55-62. Cornelius explains that “this training or calibration occur[s] during power up, restart, or other periodical or event-based time,” which are different points of time during the usage/operation of the cable. *Id.* These cable-dependent equalization parameters are trained while the system is connected to adapt to real time performance changes during use. Samaan’s teachings reinforce Cornelius; I explained them previously. Ex-1007, ¶208, ¶211, ¶78, ¶127, ¶¶225-227, ¶¶234-236, ¶¶250-255.

126. For at least these reasons, Ground 1 teaches Claim 3.

6. Dependent Claim 4

4. The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable.

127. As I explained previously, Cornelius and Samaan teach **cable-dependent equalization parameters** for equalization across the connecting cable. *See* above §V.A.4 (explaining cable-dependent parameters for claim 2). The

combination of Cornelius and Samaan teaches the cable-dependent equalization parameters **are fixed during normal usage of the Ethernet cable** and **determined during manufacturing-testing of the Ethernet cable**. As explained previously, Ground 1 teaches determining parameters while an assembled active cable is connected. *E.g.*, Ex-1006, 11:55-59; *supra* §V.A.4 (claim 2). Samaan suggests that it can be sufficient to simply use a link with preset equalization instead of more advanced negotiation or live training features happening link operation. *See* Ex-1007, ¶149 (suggesting “to forego both [Auto Negotiation] and Training, and simply use an engineered link that is forced to 10G.”), ¶208 (discussing training support as optional and expensive). Even in such a case, the cable would have to meet certain equalization values to be “specification-compliant.” Ex-1007, ¶88. Therefore, Samaan provides a motivation to modify Cornelius’s teachings by simply taking the parameters that were determined for a connected cable (*see* Ex-1006, 11:55-59) and “stor[ing] as presets” during manufacturing (*see* Ex-1006, 11:51-55).

128. **Motivation to Combine.** I explained above why a POSITA would have been motivated to customize equalization parameters to an individual cable, while it is connected. *See* above §V.A.4 (Claim 2 motivation to combine subsection). A POSITA would have found it obvious and been motivated to store these calibrated values at manufacturing time, for example, for manufacturers that

did not want to invest time and money implementing protocols to support on-the-fly training during live operation. This would have reduced the time for development as well as reducing the engineering costs that must be recovered through sales of the cable. As another example, some users or consumers only needed a simple and reliable active cable, without the overhead or complexity of on-the-fly training. This approach was beneficial in environments where cable channel characteristics remained stable over time, for example data centers or structured enterprise networks with known noise or thermal characteristics constrained by distance or shielding requirements or best practices. Thus, using these fixed, pre-calibrated equalization parameters would have addressed these types of market demands while still providing equalization tailored to the individual cable.

129. Moreover, a POSITA would have recognized that the type of individualized calibration suggested by Cornelius and Samaan would have readily been incorporated into a quality assurance (“QA”) process for verifying that assembled cables operate correctly. Combining existing calibration methods with established QA processes would have simply combined prior art elements according to known methods to yield predictable results. Indeed, such testing to ensure compliance with engineering specifications and standards was a common practice as taught by Samaan. Ex-1007, ¶90 (discussing “standard compliance

testing for devices” and the requirements “to produce all the other equalizations values tabulated in” a standard, which “is done by testing it for a selected subset of values.”). Given Samaan’s teaching that compliance is verified by testing select equalization values, a POSITA would reasonably expect such an approach to be successful. Thus, Ground 4 simply combined prior art elements (e.g., determining parameters while the cable is connected and storing presets, both of which Cornelius teaches) according to known methods to yield predictable results (e.g., preset parameters).

130. For at least these reasons, Ground 1 teaches Claim 4.

7. Independent Claim 6

131. Claim 6 largely mirrors the language of claim 1, but claims a method comprising a network cable. Therefore, claim 6 is satisfied for reasons that I explained above for claim 1.

[6pre] A communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector:
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132. I understand that a preamble generally does not state a claim limitation. Nevertheless, it is my opinion that Ground 1 teaches [6pre].

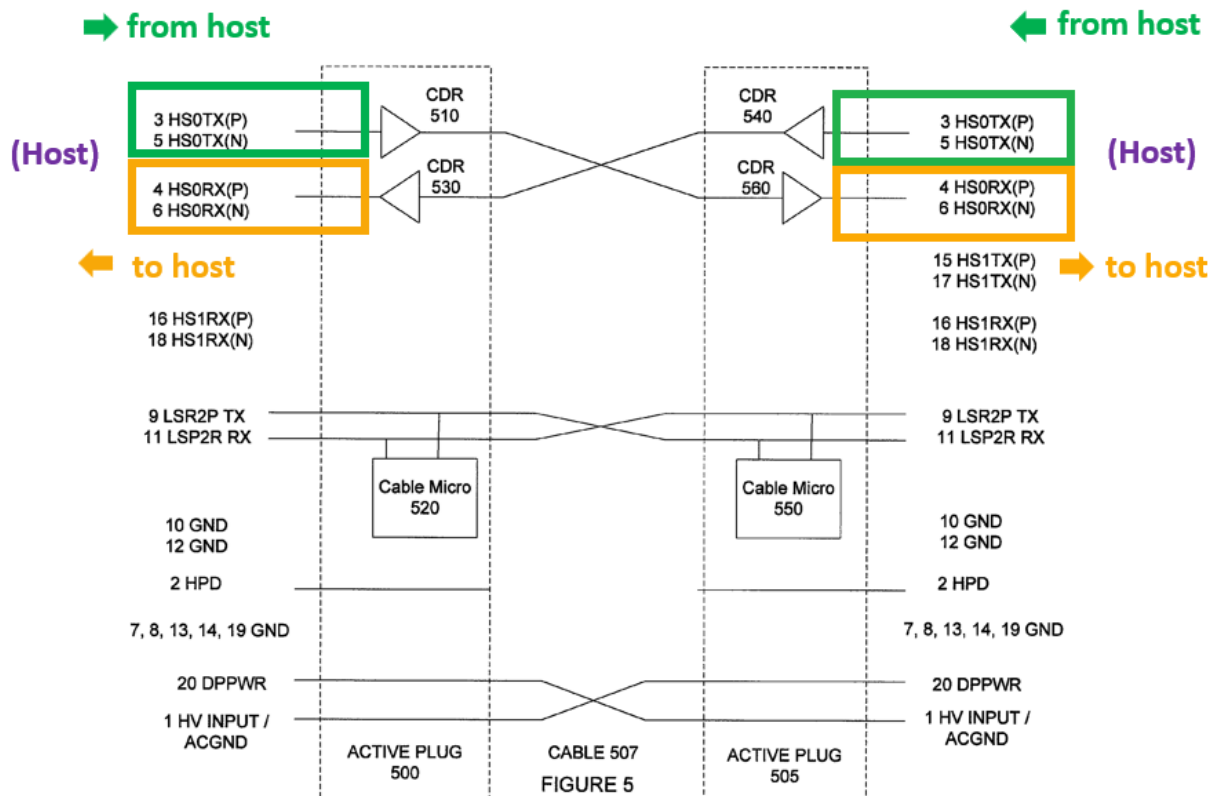
133. Ground 1 teaches a **communication method**. For example, Cornelius teaches “[c]ircuits, methods, and apparatus” (Ex-1006, Abstract, 1:50-51, 1:55-58), including the various methodology details and steps explained below for

limitations [6pre]-[6k]. Cornelius describes channel configurations for data communications through active cables (*see, e.g.*, Ex-1006, 3:28-42, 3:60-64, 4:39-44, 5:33-6:5, 6:6-67), methods for facilitating communications between devices connected by the cables (*e.g.*, Ex-1006, 3:28-42, 4:10-21, 4:66-6:5), and routines for calibrating those cables. Ex-1006, 11:45-11:62. Similarly, Samaan provides detailed explanations of how signals are transmitted through channels containing retimers, including a method of propagating messages related to the training of equalization components on a series of retimers. Ex-1007, ¶259, ¶255, ¶86, ¶118, ¶208.

134. Ground 1 teaches **a network cable**. As explained, Ground 1 teaches an active Ethernet cable; this is a network cable because Ethernet is a networking protocol and the active Ethernet cable taught by Ground 1 is used for conveying Ethernet communications. *See* above §V.A.3[1pre].

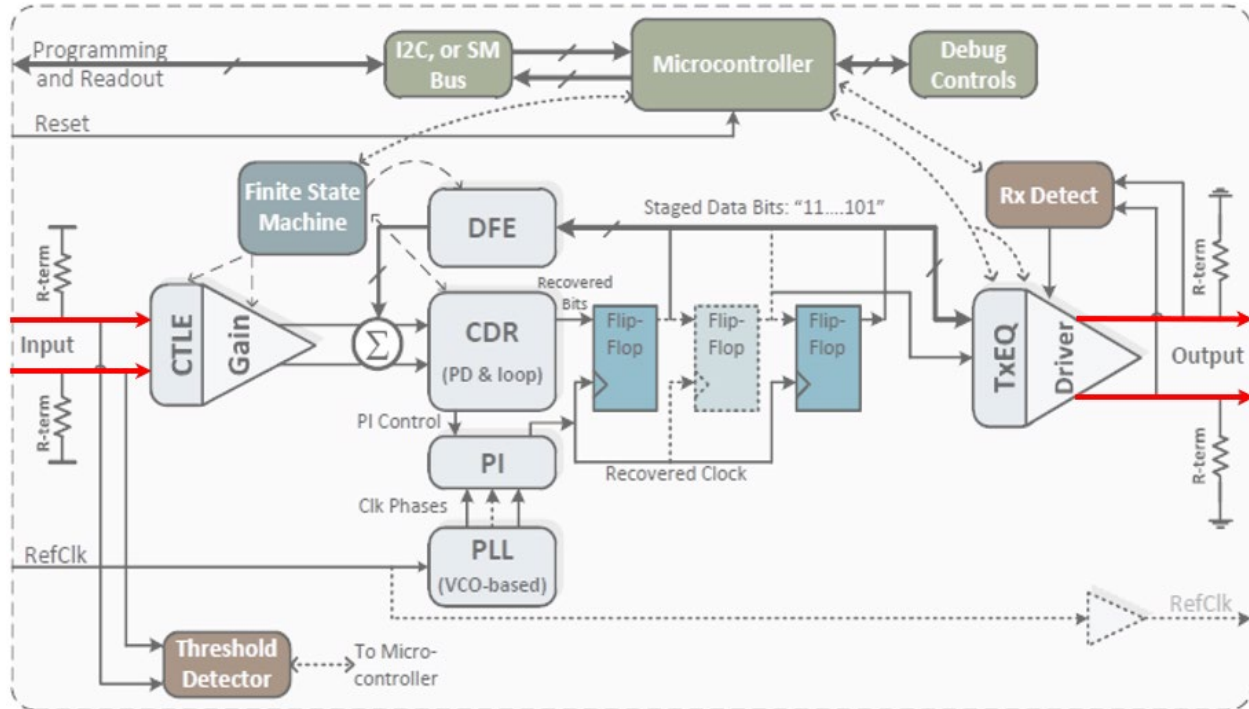
135. The network cable includes **conductor pairs electrically connecting a first connector to a second connector**. For example, Cornelius teaches “high-speed differential signal paths,” where a pair of conductors is used to transmit a signal from one connector to the other. Ex-1006, 1:67-2:2. In differential signaling, a signal is transmitted as the difference between the voltages on a pair of wires; this reduces the voltage swing on any individual wire and has been widely used for decades in cables, networking, and various transmission channels. It has long been

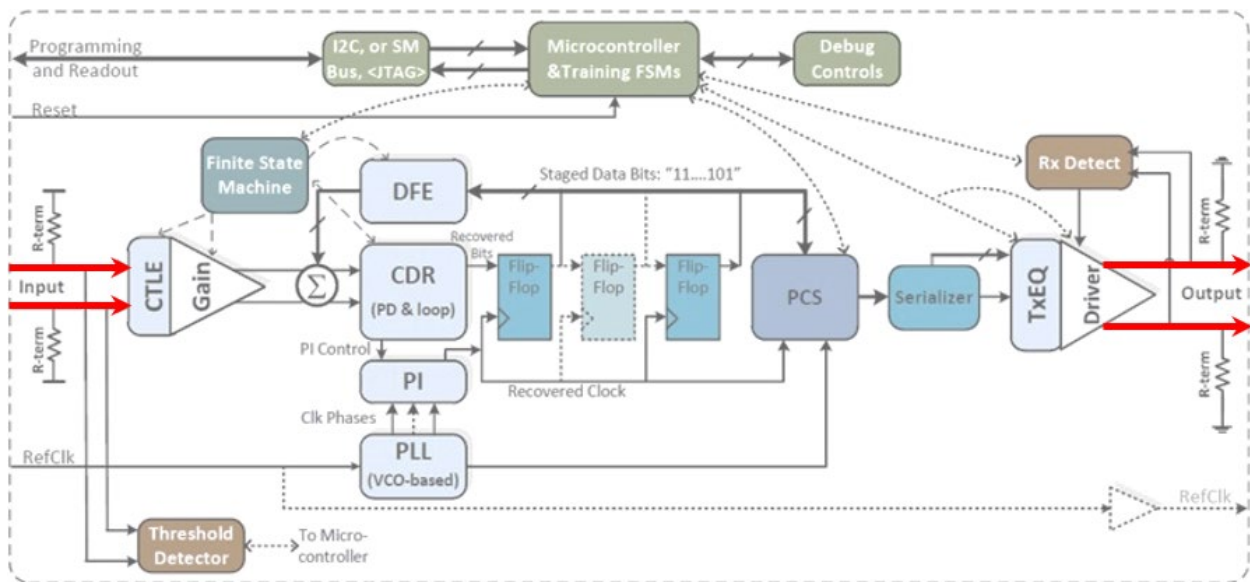
industry convention to denote differential signal pairs as Positive (“P”) and Negative (“N”), and Cornelius consistently uses these designations throughout its specification, for example, with the high speed transmit pair HS0TX(P) and HS0TX(N), and high speed receive pair HS0RX(P) and HS0RX(N). Ex-1006, Figs.3, 5-6. Cornelius includes at least one high-speed differential signal pair that connects inbound TX pins 3 and 5, via the cable, to outbound RX pins 4 and 6 on the opposite connector (e.g., 505). Conversely, there is also at least one differential signal pair that connects inbound TX pins 3 and 5 on the other connector, through the cable, to outbound RX pins 4 and 6 on the first connector (e.g., 500). Ex-1006, 6:6-7:25, 8:10-15, Figs.6, 5:



Therefore, Cornelius teaches conductor pairs electrically connecting an active plug to a second active plug. I previously explained how Ground 1 teaches electrical conductors that connect the first and second connectors. *See above §V.A.3[1a].*

136. Samaan also teaches differential signaling across the channel. Both retimer architectures include a differential pair of signals as input and a pair of differential signals as output. Ex-1007, Figs.34-35 (differential paths highlighted in red)





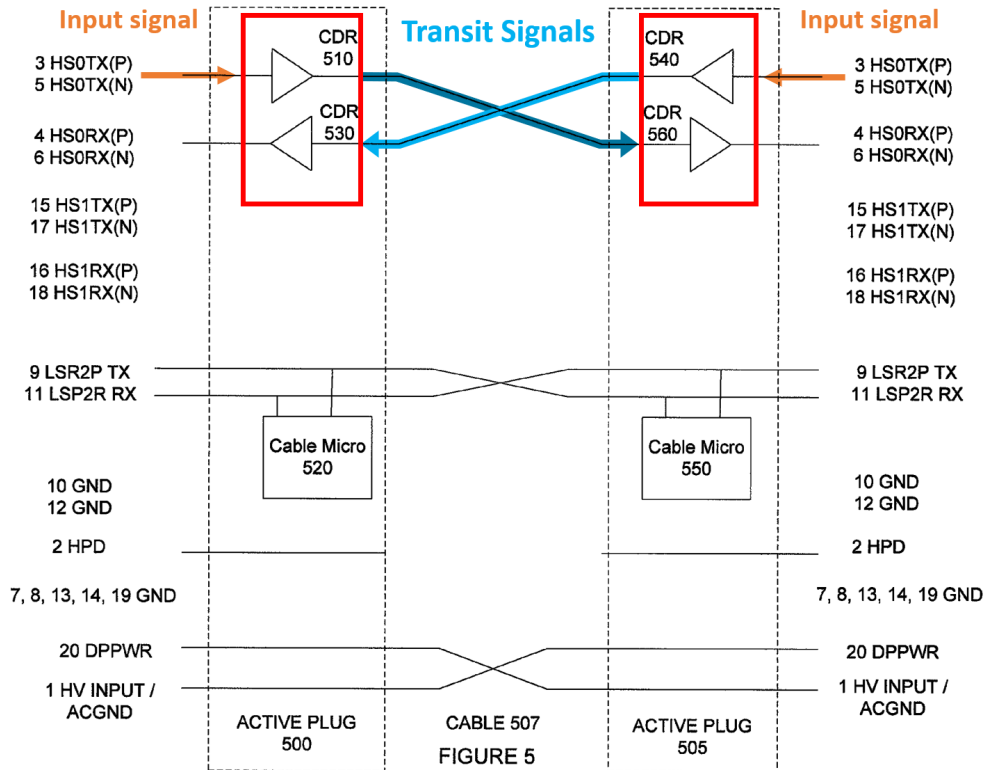
In earlier portions, Samaan explains generally how this type of input and output is differentially signaled using a pair of electrical conductors for each signal. Ex-1007, Figs.3, 13, ¶¶55-56. Moreover, the various protocols supported by Samaan’s retimers are designed to operate with differential signaling paths. *See Id.*, ¶134 (“There is an N to P side (differential) skew requirement which must be less than the minimum transition time.”), ¶146 (“the peak-to-peak differential output voltage is equal to, or exceeds, 800 mV for a 1010... pattern”), ¶224.

137. For at least these reasons, Ground 1 teaches [6pre].

[6a] receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device;

138. The elements in [6a] also appear in [1b] and are satisfied for the same reasons. *See* above §V.A.3[1b]. Either of Cornelius’s active plugs is the first connector; the other active plug is the second connector. The first electrical input

signal and inbound data stream are the ones received by the first connector from its corresponding host (recited in [1b]), which is the first host device. As explained previously, the first connector (active plug) includes a first transceiver inside. *Id.*



[6b] performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream;

139. The elements in [6b] also appear in [1c], and my analysis for [1c] already explained this limitation for both the first and second connectors; the first input signal, data stream, and host device are the ones that correspond to the first connector. Therefore, limitation [6e] is satisfied for the same reasons explained previously. *See above §V.A.3[1c].*

[6c] re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs;

140. The elements in [6c] also appear in [1c] and are satisfied for the same reasons. *See* above §V.A.3[1c]. For [1c], I explained how Ground 1 teaches an electrical transit signal (conveying a transit data stream) going over the conductors in one direction, and another transit signal going in the opposite direction. Here, the first transit data stream is the stream conveyed by the (first) transit signal going from the first connector to the second connector. *Id.* As explained, the output of the first connector is transmitted over a (first) conductor pair to the second connector. *See* above §V.A.7[6pre].

[6d] receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device;

141. Limitation [6d] mirrors [6a] and differs only by changing “first” to “second.” Like [6a], the elements in [6d] also appear in [1b], and my analysis for [1b] already explained this limitation for both the first and second connectors; the second input signal, data stream, and host device are the ones that correspond to the second connector. Therefore, limitation [6d] is satisfied for the same reasons explained previously. *See* above §V.A.3[1a].

[6e]	performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream;
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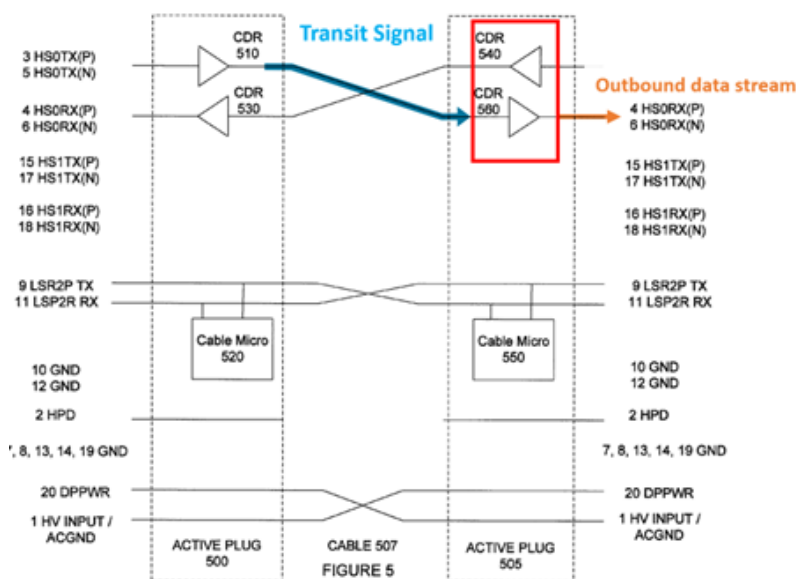
142. Limitation [6e] mirrors [6b] and differs only by switching “first” and “second.” Like [6b], the elements in [6e] also appear in [1c], and my analysis for [1c] already explained this limitation for both the first and second connectors; the second input signal, data stream, and host device are the ones that correspond to the second connector. Therefore, limitation [6e] is satisfied for the same reasons explained previously. *See* above §V.A.3[1c].

[6f]	re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs;
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143. Limitation [6f] mirrors [6c] and differs only by switching “first” and “second.” Like [6c], the elements in [6f] also appear in [1c] and are satisfied for the same reasons, with the second electrical input signal and inbound data stream being those received by the second connector, and the second transit data stream being the one conveyed from the second connector to the first. *See* above §V.A.3[1c]. As explained, the output of the second connector is transmitted over a (second) conductor pair to the first connector. *See* above §V.A.7[6pre].

[6g] performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream;

144. The elements in [6g] also appear in [1d] and are satisfied for the same reasons, with the first electrical transit signal being the one conveyed from the first transceiver in the first connector to the second transceiver in the second connector through the cable. *See above §V.A.3[1d].*



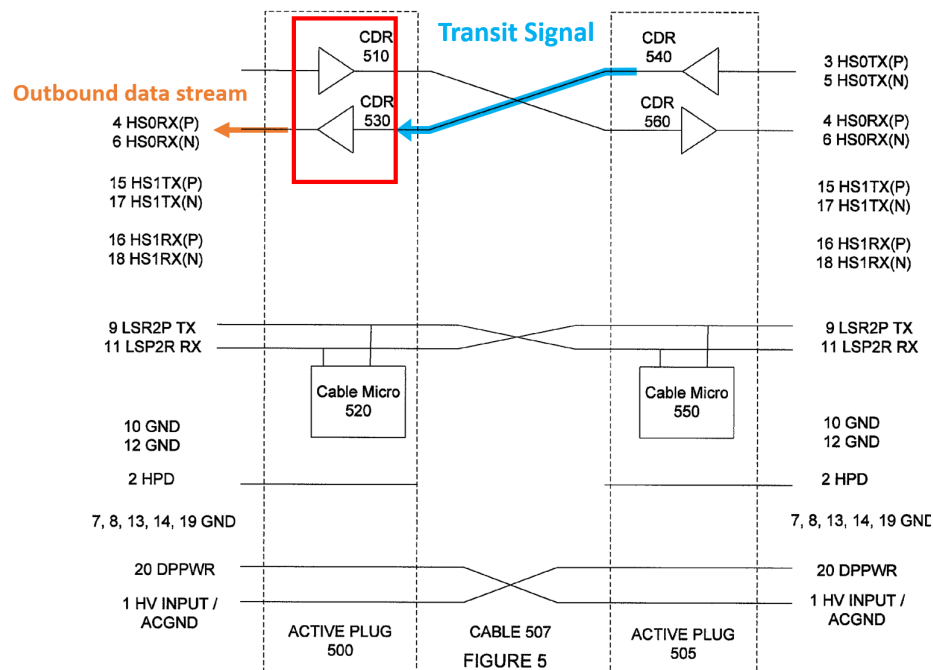
[6h] re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device;

145. The elements in [6h] also appear in [1d] and are satisfied for the same reasons, with the first transit data stream being the transit data stream that the second transceiver received from the cable, and the second outbound data stream being the data stream output by the second transceiver to the corresponding host

through the second connector. *See* above §V.A.3[1d]. As explained previously for [1b], the second outbound data stream is conveyed by an electrical output signal from the second transceiver to the second host device. *See* above §V.A.3[1b].

[6i] performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream; and

146. Limitation [6i] mirrors [6g] and differs only by switching “first” and “second.” Like [6g], the elements in [6i] also appear in [1d], and my analysis for [1d] already explained both the first and second transceivers along with their respective signals, streams, and host devices; therefore, limitation [6i] is satisfied for the same reasons explained previously. *See* above §V.A.3[1d].



[6j] re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device,

147. Limitation [6j] mirrors [6h] and differs only by switching “first” and “second.” Like [6h], the elements in [6j] also appear in [1d] and [1b], and my analysis for [1d] and [1b] already explained both the first and second transceivers along with their respective signals, streams, and host devices; therefore, limitation [6j] is satisfied for the same reasons explained previously. *See* above §§V.A.3[1d], [1b].

[6k] wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.
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148. The elements in [6k] also appear in [1e] and are satisfied for the same reasons. *See* above §V.A.3[1e]. Specifically, the first and second transit data streams correspond to the transit data streams received by the second and first transceivers, respectively, and the first and second electrical input signals are those received by the first and second transceivers, respectively from the first and second hosts.

8. Dependent Claim 7

- 7. The communication method of claim 6, wherein cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said performing clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.**

149. As I explained for claim 2, Ground 1 teaches cable-dependent equalization parameters are employed for the re-modulating of inbound data streams and the clock and data recovery on the transit signals. *See* above §V.A.4.

150. Because Ground 1's cables are bidirectional and symmetrical in operation (*see* above §V.A.3 (introduction explaining Cornelius's symmetry)), Cornelius teaches employing cable dependent equalization parameters for remodulation of both the first and second inbound data streams and for clock and data recovery of both the first and second transit signals.

151. Therefore, Ground 1 employs cable-dependent equalization parameters for at least one of the recited re-modulation or CDR operations.

152. For at least these reasons, Ground 1 teaches Claim 7.

9. Dependent Claim 8

8. The communication method of claim 7, wherein said cable-dependent equalization parameters are adaptively updated.

153. Ground 1 teaches the additional limitation of claim 8. Ground 1 teaches the cable-dependent equalization parameters are adaptively updated by being adapted using calibration routines during usage of the cable. Therefore, the same reasons that I explained above for claim 3 apply here. *See* above §§V.A.5 (claim 3), §V.A.4 (claim 2).

154. For at least these reasons, Ground 1 teaches claim 8.

10. Dependent Claim 9

9. The communication method of claim 7, wherein said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable.

155. Claim 9 shares elements with claim 4 that are satisfied for the same reasons. Claim 9 recites **manufacturer-testing**, instead of manufacturing-testing. The manufacturing-testing I explained for claim 4 is manufacturer-testing, because it is carried out by the manufacturer. Ex-1006, 11:51-55 (“calibrated or otherwise determined by the manufacture[r]”). Therefore, Ground 1 teaches this element and the rest of claim 9 for the same reasons that I previously explained above. *See* above §V.A.6.

156. For at least these reasons, Ground 1 teaches claim 9.

11. Independent Claim 11

[11pre] A cable manufacturing method that comprises:

157. I understand that a preamble generally does not state a claim limitation. Nevertheless, it is my opinion that Ground 1 teaches [11pre].

158. Ground 1 teaches **a cable manufacturing method** that comprises the steps in claim 11, which mostly connect and package elements in the configurations described for claim 1.

159. Cornelius teaches claim 1 and explains that the “devices shown or discussed may be manufactured,” including “the connections...incorporat[ing] embodiments of the present invention.” Ex-1006, 3:5-16. And Cornelius teaches active Ethernet cables described for claim 1, with elements connected and packaged as recited. Ex-1006, 6:6-42, 8:10-40. Cornelius further discusses the various circuits that are included in its active plugs (Ex-1006, 6:6-67), the pin arrangements in the connector ports the plugs fit in (Ex-1006, 3:65-4:65), and the materials used to construct the cables. Ex-1006, 6:25-29, 7:36-41.

160. Cornelius teaches steps that are carried out “by the manufacture[r]” such as the tuning/calibration of the circuits included in the plugs. Ex-1006, 11:45-11:62. Cornelius teaches aspects of its active cable that are “useful in test and manufacturing as well.” *See, e.g.*, Ex-1006, 7:31-32, 7:7-17.

161. The manufacturing method further includes the subsequent limitations as I explain below.

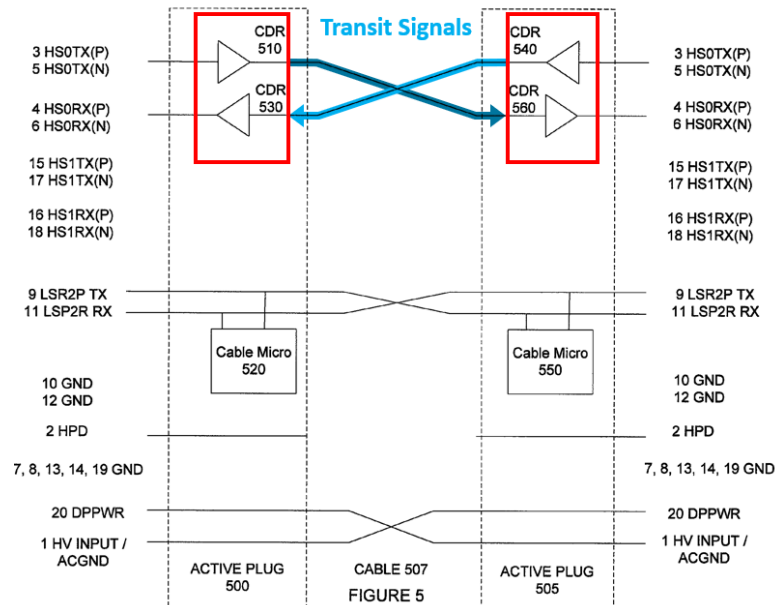
162. For at least these reasons, Ground 1 teaches [11pre].

[11a] connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver;

163. The elements in [11a] also appear in [1a], [1c], and [1d] and are satisfied for the same reasons. *See* above §§V.A.3[1a], [1c]-[1d]. The first and second connectors in claim 1 respectively include the first and second transceivers. The transit signals output by the first and second transceivers correspond respectively to the first and second electrical transit signals. Ex-1006, 6:6-33, 8:20-26, claim 1, Fig.5.

164. I have also explained how Ground 1's cable includes conductor pairs electrically connecting a first connector to a second connector and the TX pins to RX pins. *See* above §V.A.7[6pre]. For the same reasons, Ground 1 teaches **connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver**. For example, Cornelius discloses that transceivers (e.g., the dual CDR/retimer circuitry), are included in the connectors to "retime signals received from the cable" and to "provide and receive signals." Ex-1006, claims 1 & 6, 6:11-29. The dual CDR circuits are connected to ends of

the conductor pairs within the cable to receive from and provide signals to the cable, as illustrated in Figure 5:



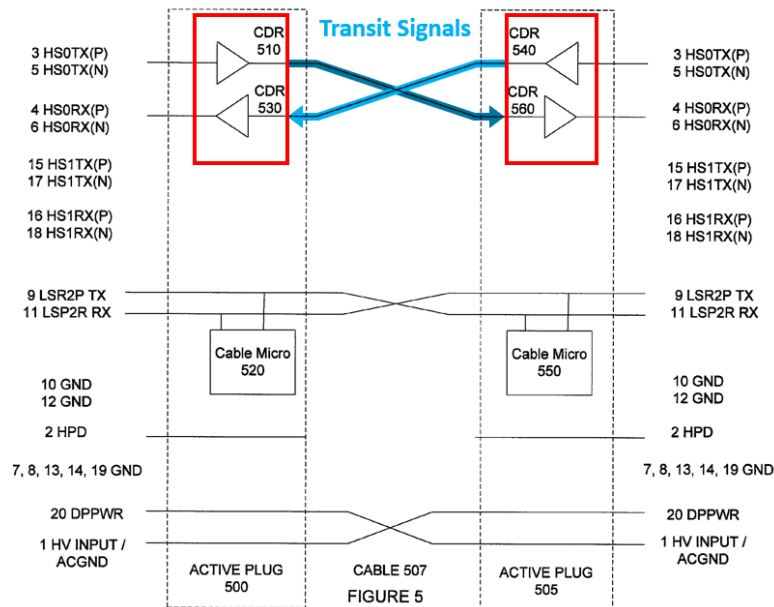
165. Cornelius teaches or suggests the connecting step because, in order for the plugs and conductors to be connected in an assembled cable (as Cornelius teaches), they would have been connected during manufacturing, when the cable components were assembled. It would have been obvious to connect the dual CDR circuits with the ends of the conductor pairs because Cornelius teaches that they are connected.

166. For at least these reasons, Ground 1 teaches [11a].

- | |
|---|
| <p>[11b] packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and</p> <p>[11c] packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device,</p> |
|---|

167. The elements in limitation [11b] and [11c] also appear in limitations [1b] and [1c], and are satisfied for the same reasons. My analysis for [1b] and [1c] explained both the first and second transceivers along with their respective signals, streams, and host devices—the first and second of each are those that correspond to the first and second connectors, respectively; Ground 1 teaches they are coupled in this way. Therefore, those apply here to limitations [11b] and [11c], which are satisfied for the same reasons explained previously. *See* above §§V.A.3[1b], [1c].

168. Cornelius also teaches **packaging** the transceivers into their respective connectors. For example, Cornelius teaches the respective transceivers (e.g., dual CDR/retimer circuitry) are packaged inside their respective connectors (e.g., active plugs). Ex-1006, 6:11-24, Figs.5-6.



Ex-1006, Fig.5.

169. Because the dual CDR/retimer circuitry has been packaged inside the active plug, Cornelius teaches or suggests the step of packaging the circuitry that way. Ex-1006, 6:11-24, Figs.5-6. At a minimum, it would have been obvious because, in order for the first and second transceivers to be assembled in active plugs connecting via a cable (as Cornelius teaches), they would have been packaged during manufacturing, when the cable components were assembled.

170. I also explained how Ground 1 teaches an Ethernet port (*see* above §V.A.3[1b]), which is a network interface port because Ethernet is a networking protocol and interfacing is the function of an Ethernet port.

171. For at least these reasons, Ground 1 teaches [11b] and [11c].

[11d] the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals.

172. Limitation [11d] recites elements set forth in limitations [1c], [1d], and [1e], and are therefore satisfied for the same reasons. *See* above §V.A.3[1c], [1d], [1e]. Cornelius’ and Samaan’s teachings of respective transceivers, respective signals, and data streams that I explained for claim 1 correspond to the first and second transceivers, first and second signals, and first and second data streams as recited in limitation [11d].

173. As I previously explained, Ground 1 teaches the remodulation of the transit data stream as the outbound data stream. *See* above §§V.A.3[1d], [1e]. Ground 1’s remodulation of the data stream **generates** electrical output signals conveying the remodulated data stream—Ground 1 teaches transceivers (e.g., dual CDR/retimer circuitry) “re-transmit[] data anew, with new equalization” and “re-establishes signal shape” (Ex-1007, ¶15, ¶202), which is generating electrical output signals when performed on the transit signals received from the cable.

174. For at least these reasons, Ground 1 teaches [11d].

12. Dependent Claim 12

12. The cable manufacturing method of claim 11, wherein the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals.

175. I explained how Ground 1 teaches the cable manufacturing method of claim 11. *See* above §V.A.11. Ground 1 teaches the additional limitation of claim 12, which recites overlapping elements with claim 2 that are satisfied for the same reasons. *See* above §V.A.4.

176. Beyond the preambles, claim 12 recites “generating the...electrical transit signals” instead of “remodulation of the inbound data stream for transit” (claim 2). Ground 3 generates electrical transit signals by remodulating the inbound data stream for transit. *See* above §V.A.3[1c]; *see also* §V.A.11[1d]. Ground 1 teaches transceivers (e.g., dual CDR/retimer circuitry) “re-transmit[] data anew, with new equalization” and “re-establishes signal shape” (Ex-1007, ¶15, ¶202), which is generating electrical output signals when performed on the transit signals received from the cable.

177. Claim 12 also recites that the transceivers are “**configured** to employ” cable-dependent equalization parameters for both generating the electrical transit signals and also CDR on them, where claim 2 only requires employing them for “at

least one of” the recited operations. I explained above how Ground 1 teaches both (see above §V.A.4 (claim 2)); as Cornelius explains, the transceivers are **configured** to do this. Ex-1006, 6:50-57 (“operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured.”), 6:11-24, 6:43-49, claims 1, 6; Ex-1007, ¶227.

178. For at least these reasons, Ground 1 teaches claim 12.

13. Dependent Claim 13

13. The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation.

179. I explained how Ground 1 teaches the cable manufacturing method of claim 12. See above §V.A.12. Ground 1 teaches the additional limitation of claim 13, which recites overlapping elements with claim 3 that are satisfied for the same reasons. See above §V.A.5.

180. Beyond the preambles, claim 13 recites “the first and second transceivers are each **configured** to adapt the cable-dependent equalization parameters” as compared to “said cable-dependent equalization parameters adapt” (claim 3). I previously explained how, for Ground 1, the dual CDR/retimer pairs each employ cable-dependent equalization parameters and adapt these during usage, and how they are configured to do this. That analysis applies here. See above §V.A.5 (claim 3); §V.A.12 (claim 12); Ex-1006, 6:50-57, 6:11-49, claims 1,

6. Claim 13 also requires the adaptation to occur “during **operation**” instead of “during usage” (claim 3). When using the cable, the cable is in operation. Ground 1 teaches these limitations when the cable is in use/operation; that analysis applies here. *See* above §V.A.5 (claim 3). Moreover, Ground 1 teaches adaption during operation. Ex-1006, 6:50-57 (“operational parameters...and other aspects and characteristics of the plug circuitry may be configured...The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications”). For at least these reasons, Ground 1 teaches claim 13.

14. Dependent Claim 14

14. The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters.

181. Ground 1 teaches the additional limitation of claim 14. I explained above how Ground 1 teaches **the first and second transceivers are each configured to employ** (e.g., use) **cable-dependent equalization parameters**. *See* above §V.A.12 (claim 12); §V.A.4 (claim 2). Ground 1 further teaches these equalization parameters being **presets** used **during operation**. For example, Cornelius teaches equalization parameters that are “calibrated or otherwise determined by the manufacture[r] and stored as presets for loading during

operation.” Ex-1006, 11:51-55. Having been loaded during operation, the presets are then used during operation for equalization as the transceivers retime data transmitted over the cable while it is used. As I explained previously, the combination of Cornelius and Samaan teaches cable-dependent equalization parameters, that are presets. *See* above §V.A.6 (claim 4).

182. Ground 1 also teaches **testing an assembled cable to determine the cable-dependent equalization parameters**. I explained previously how Ground 1 teaches or suggests testing an assembled cable during manufacturing to determine the preset parameters for that particular cable using calibration routines. *See* above §V.A.6 (claim 4). Ground 1 teaches testing an assembled cable to determine the cable-dependent equalization parameters for the same reasons. *See* above §V.A.6 (explaining how and why Cornelius and Samaan would have been combined). For at least these reasons, Ground 1 teaches claim 14.

B. Ground 2: Claims 5 and 10 are Rendered Obvious in View of Cornelius, Samaan, and Lugthart.

183. It is my opinion that a POSITA would have found Claims 5 and 10 obvious based on the combined teachings of Cornelius, Samaan, and Lugthart. Dependent claims 5 and 10 recite a particular symbol rate. Lugthart teaches this rate for active cables. The motivation to combine Lugthart’s teaching with Cornelius and Samaan is explained below. *See* below §V.B.2. Lugthart is introduced in the following section. *See* below §V.C.1.

1. Dependent Claim 5

5. The active Ethernet cable of claim 4, wherein the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd.

184. Ground 1 teaches **an active Ethernet cable** with an **inbound data stream** (from host to cable) and an **outbound data stream** (from cable to host), as explained previously. *See* above §V.A.3[1pre], [1b].

185. Ground 2 teaches an active Ethernet cable where the inbound data stream and the outbound data stream **each have a per-lane symbol rate in excess of 50 GBd**. Lugthart teaches setting inbound and outbound data streams for an active Ethernet cable up to 300 Gb/s. Lugthart teaches an input signal IN at “a data rate between about 100 Mbits/s to about 300 Gbit/s.” Ex-1004, 35:36-38. Input signal IN is “a differential signal” or “a single-ended signal.” Ex-1004, 35:29-33, Fig.2A. Lugthart provides examples of “an NRZ modulated signal or PAM-4 signal.” Ex-1004, 35:31-38.

186. As Lugthart explains, baud rate corresponds to the “number of symbols/second.” Ex-1004, 31:52-55. Because PAM-4 uses four distinct voltage levels,¹⁰ each symbol can take on one of four values, meaning each symbol can represent two bits of data ($2^2=4$), e.g., 00, 01, 10, and 11. *See* Ex-1004, 31:28-46.

¹⁰ PAM refers to Pulse Amplitude Modulation because it modulates the amplitude of a signal. PAM-4 refers to Pulse Amplitude Modulation with 4 amplitude levels.

With each PAM-4 symbol carrying 2 bits, a bitrate of 100 Gbit/s corresponds to a baud (symbol) rate of $(100 \frac{G \text{ bits}}{s}) \times (\frac{1 \text{ Symbol}}{2 \text{ bits}}) = 50 \text{ GBd}$. Any bitrate higher than 100 Gb/s has a baud rate higher than 50 GBd using PAM-4. For NRZ, signals use two voltage levels, meaning each symbol is either high or low, 1 or 0. With each NRZ symbol carrying 1 bit, a bitrate of 50 Gbit/s corresponds to 50 GBd; any bitrate higher than 50 Gb/s has a baud rate higher than 50 GBd. Lugthart teaches transceiver configurations operating with per-lane rates of “100 Gbit/s PAM-4.” Ex-1004, 13:13-48. Furthermore, Lugthart teaches that “a wide variety of other configurations including those supporting additional data rates are possible.” Ex-1004, 13:49-14:6 (suggesting “400 Gbit/s, and 448 Gbit/s, and/or be capable of operation at data rates greater than any of these amounts”). Therefore, Lugthart teaches a maximum baud rate in excess of 50 GBd for both PAM-4 and NRZ.

187. Cornelius and Lugthart both teach or suggest using symmetric symbol rates for inbound and outbound data streams. They both teach symmetric cable designs with identical transceivers on both sides (*see* §V.A.3 (introduction explaining Cornelius’s symmetry), §V.C.3 (introduction explaining Lugthart’s symmetry)), with inbound and outbound data streams using the same modulation schemes, for example NRZ or PAM4. Ex-1004, 8:50-60, 12:1-6. Data input at one end of the cable is output at the other end at the same rate. Ex-1004, Figs.2A, 4A; Ex-1006, Figs.5-6. Lugthart explains that its data rate teachings apply in both

directions (ingress and egress): “While only the egress/transmit direction of data transmission is referred to in the above [data rate] examples, it will be appreciated that the transceivers have both egress/transmit and ingress/receive paths.” Ex-1004, 13:49-57. This is due to the symmetry of ingress and egress paths: “each of the transceivers described above as implementing a multiplexing function in the egress/transmit direction will be capable of performing a corresponding demultiplexing function in the ingress/receive direction to generate the appropriate number of host-side lanes, as described herein.” *Id.* Therefore, when an inbound data stream is applied at a per-lane symbol rate exceeding 50 GBd, the outbound data stream would likewise be at the same rate, each being in excess of 50 GBd.

188. **Motivation to Combine.** The motivation to combine for Ground 1 (Cornelius and Samaan) was explained previously. *See* above §V.A.3[1pre] (Motivation to Combine subsection). A POSITA would have been further motivated to apply Lugthart’s teachings by configuring the active Ethernet cable taught by Cornelius and Samaan to operate above 50 GBd. Lugthart teaches operational speeds for active Ethernet cables in excess of 50 GBd, and a POSITA would have been motivated to use the maximum transmission speed to increase data transfer rates in data centers and high-performance computing applications. Cornelius suggests using higher transmission rates/speeds because it is directed at high-speed communications. Ex-1006, 1:67-2:2, 4:10-31, 8:65-9:4. Because the

combination of Cornelius and Samaan teaches an active Ethernet cable, a POSITA would have been motivated to configure the cable to operate at known speeds. This would have used a known technique (running an active cable above 50 GBd) to improve similar devices (active Ethernet cables) in the same way.

189. Additionally, Lugthart teaches that its CDR, including the modulation schemes and speeds, “can be used in a wide variety of systems.” Ex-1004, 35:24-28. Like Lugthart, Cornelius teaches an active cable with CDRs/retimers in each active plug. Ex-1006, 5:33-39, 6:6-20, Figs.5-6. Therefore, a POSITA would have been motivated to apply Lugthart’s teachings to the combination of Cornelius and Samaan, with a reasonable expectation of success given the shared context of active cables using retimers at both ends.

190. For at least these reasons, Ground 2 teaches claim 5.

2. Dependent claim 10

10. The communication method of claim 9, wherein the first inbound data stream has a per-lane symbol rate in excess of 50 GBd.

191. Apart from depending from claim 9 instead of claim 4, the limitations of claim 10 also appear in claim 5 and are satisfied for the same reasons. *See* above §V.B.1.

C. Ground 3: Claims 1-14 Are Rendered Obvious in View of Lugthart and Aronson.

192. It is my opinion that a POSITA would have found Claims 1-14 obvious based on the teachings of Lugthart and Aronson.

193. Lugthart teaches the active Ethernet cable of claim 1, including limitations [1pre]-[1d]. Lugthart teaches equalization parameters for host-side inbound and outbound data streams. Aronson teaches these configuration details, including fixed, cable-independent host-side parameters for active cables, and cable-dependent parameters for the cable-side. The motivation to combine is explained below. *See below §V.C.3[1e].*

1. U.S. Patent No. 9,882,706 (“Lugthart”) (Ex-1004)

194. Lugthart was filed on December 28, 2016 and issued on January 30, 2018, claiming priority to December 27, 2013. Based on the priority date of Mar. 1, 2019 of the '252 patent, I understand Lugthart is prior art to the '252 patent under post-AIA §102(a)(1). *See below, Appendix 4 (Understanding of the Law).*

195. Lugthart describes an active cable with transceivers at each end to facilitate high-speed, bi-directional communication between devices. Ex-1004, Figs.1A-2A, 6:65-7:3, 13:49-57, 14:7-31. Each transceiver includes equalization, CDR, pre-equalization, and re-modulation. Ex-1004, 21:35-42, 7:66-8:7, 9:10-10:22, 15:64-16:10, Figs.1A, 4A.

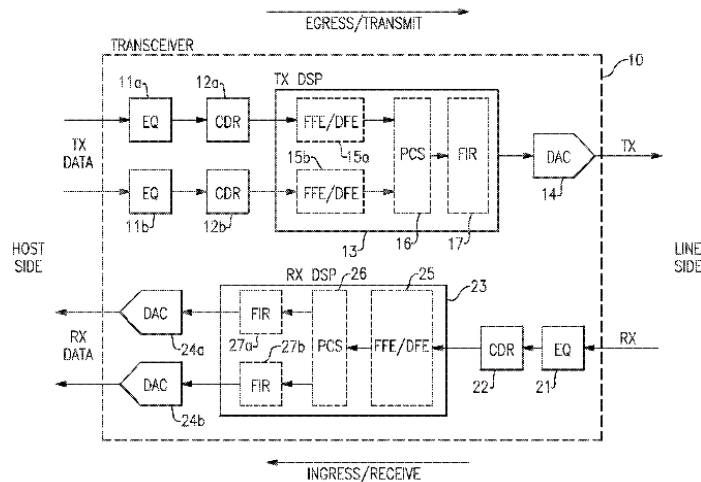


FIG. 1A

196. Lugthart is analogous art to the '252 patent because it is in the same field of endeavor (*see* above §III). Lugthart is directed to “methods for high speed communications,” which can be used to “achieve reliable high-speed point-to-point communication between different electronic devices, computing devices, storage devices and peripheral devices.” Ex-1004, Abstract, 3:12-16, 4:10-12, 6:55-7:5, 14:29-31. The objective of Lugthart is to “establish high-speed point-to-point links” between different electronic devices, computing devices, storage devices and peripheral devices. *Id.*, 47:24-27. Lugthart is also reasonably pertinent to the problem addressed by the '252 patent (*see* above §V.A.1 (explaining the problem)) because it teaches equalizations in the transmitter and receiver for serial architectures to account for signal degradation caused by channel loss. Ex-1004, 22:40-49, 21:35-42, Figs.1A, 4A.

2. U.S. Patent No. 7,445,389 (“Aronson”) (Ex-1005)

197. Aronson was filed on April 10, 2006 and issued on November 4, 2008. Based on the priority date of Mar. 1, 2019 of the '252 patent, I understand Cornelius is prior art to the '252 patent under post-AIA §102(a)(1). *See below, Appendix 4 (Understanding of the Law).*

198. Aronson discloses an active cable with driver and receiver ICs at each end of the cable to facilitate bi-directional data-transmission. Ex-1005, 13:51-14:1, 14:10-13, 14: 22-51. Aronson teaches setting parameters to provide “fixed, adjustable or adaptive equalization.” Ex-1005, 14:34-41, 13:49-14:5, 14:50-57.

199. Aronson is analogous art to the '252 patent because it is in the same field of endeavor. *See above §III.* Aronson is directed to bi-directional high-speed communication over a cable. Ex-1005, Abstract, 2:22-31, 4:55-62, 6:46-48, 13:23-27. Aronson is also reasonably pertinent to the problem addressed by the '252 patent (*see above §V.A.1 (explaining the problem)*) because Aronson recognizes the issue of signal loss during transmission over various paths on a transmission connection like the '252 patent (Ex-1005, 11:32-48, 13:66-14:5, 14:33-40) and addresses it by adjusting equalization circuits on both transmit and receive paths to account for cable characteristics and reduce jitter. *E.g.*, Ex-1005, Figs.12A, 12B, 11:32-67, 13:49-14:9, 14:26-57.

3. Independent Claim 1

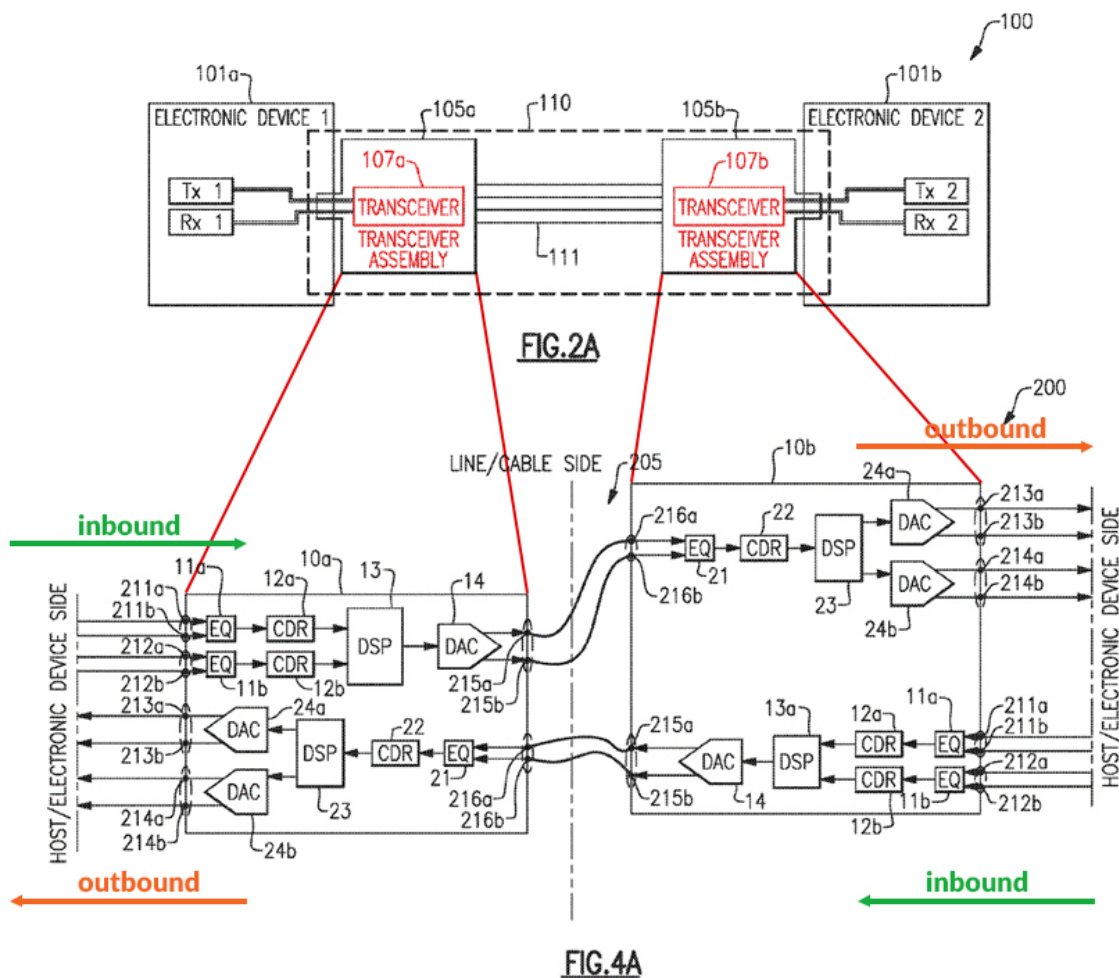
200. As an initial matter, for each of the below limitations, the “first” and “second” designations can be swapped between elements at one end of Lugthart’s active cable versus the other. Both Lugthart and Aronson teach symmetric cable designs to support bi-directional communication; each side has identical components and operation. *E.g.*, Ex-1004, 7:13-20, 6:65-7:3, 13:49-57, Figs.1A, 2A, 4A; Ex-1005, 5:13-35, 5:36-55, 6:42-49, 13:3-17, 13:23-27. Therefore, the connector/host/signal/stream on one end of the cable can serve as the first, while those on the other end would be the second.

[1pre] An active Ethernet cable that comprises:
--

201. I understand that a preamble generally does not state a claim limitation. Nonetheless, it is my opinion that Ground 3 teaches [1pre].

202. For example, Lugthart teaches an active cable that includes “electrical conducting lines” connecting “a first electronic device” and “a second electronic device.” Ex-1004, 16:11-15, Figs.2A, 3A-3B, 4A, 3:12-16, 4:10-12, 6:65-7:3, 10:4-22, 14:7-34. Lugthart explains that “[t]he cable can be implemented in a wide variety of ways,” and one such implementation would be “an electrical cable including one or more pairs of differential micro coaxial cables or conductors.” Ex-1004, 6:65-7:5. The active cable includes a transceiver assembly at each end (Ex-1004, Fig.2A); power is supplied to the transceiver assemblies. Ex-1004, 14:29-31,

17:26-29, 17:57-59. The active cable is shown in Figure 2A, with additional transceiver details shown in Fig.4A.



203. Lugthart further teaches the active cable including cabling to support “gigabit Ethernet.” Ex-1004, 16:31-36, 53:36-39 (teaching “40 Gigabit Ethernet” embodiment for rack servers). Lugthart also teaches Cat-5, Cat-5e, and Cat-6 cabling, all of which were commonly used for Ethernet (Ex-1004, 19:29-33), and interfaces that support Ethernet communications. *E.g.*, Ex-1004, 29:6-20 (Thunderbolt, SFP+, QSFP). Therefore, Lugthart teaches or suggests an active

Ethernet cable, including but not limited to cabling that supports gigabit Ethernet with SFP, SFP+, or QSFP modules at each end.

204. **Motivation to Combine.** A POSITA would have found it obvious and been motivated to apply these teachings to support Ethernet in Lugthart's active cable because Lugthart teaches it, or at least suggests it, by teaching cables and modules that support Ethernet. Ex-1004, 16:31-36, 19:29-33, 29:6-20. Lugthart aims to provide communications for data centers (Ex-1004, 1:49-55, 53:36-39), where gigabit Ethernet was the predominant protocol. In data centers, SFP, SFP+, and QSFP modules were often used for active Ethernet cables. *See* above §I.A (explaining active Ethernet cables); Ex-1019 (exemplary active Ethernet cable):



Therefore, the prior art provides express motivation to apply Lugthart's Ethernet teachings to its active cable.

205. For at least these reasons, Ground 3 teaches [1pre].

[1a] electrical conductors connected between a first connector and a second connector,

206. Lugthart teaches **electrical conductors connected between a first connector and a second connector**. For example, Lugthart teaches “first and second transceiver assemblies...positioned at either end of the conductive lines.” Ex-1004, 14:29-42, 10:4-8, 10:17-22. Lugthart’s transceiver assemblies are connected by electrical conductors, including, for example, “paired micro coaxial cables” which are electrical conductors conducting differential electric signals. Ex-1004, 16:27-36, 14:43-46, 37:32-48. “The conducting lines 111 can include metal (e.g., copper) conductors.” Ex-1004, 16:19-26, 16:11-18. Lugthart’s first and second transceiver assemblies are first and second connectors; each is electrically connected to a host, which Lugthart refers to as an “electronic device.” Ex-1004, 14:29-42, 14:47-53, 15:42-47, Fig.2A:

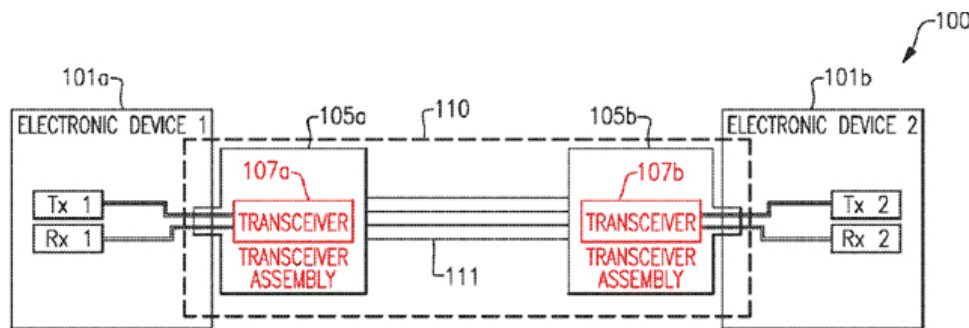


FIG.2A

207. Each transceiver assembly is a “pluggable module” that “include[s] a...transceiver[.]” Ex-1004, 4:10-16, Fig.2A, 15:30-31 (each transceiver “enclosed

in a packaging”). As shown in Figure 2A, the transceiver assemblies connect the cable to two host devices, enabling communication between them. Ex-1004, Fig.2A. I explain how the transceiver assemblies are connectors in detail for [1b].

208. For at least these reasons, Ground 3 teaches [1a].

[1b] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,

209. Lugthart teaches **each of the first and second connectors** (e.g., transceiver assemblies) **being adapted to fit into an Ethernet port of a corresponding host device**. For example, each transceiver assembly is “a [] pluggable module.” Ex-1004, 4:10-14, Fig.2A, 15:30-31 (each transceiver “enclosed in a packaging”). Each transceiver assembly “has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device[,]” referring to the host device. *Id.*, 15:42-52 (also teaching exemplary connectors such as SFP, SFP+, or QSFP), 14:14-15 (referring to electronic devices 101a and 101b as “host devices”), Fig.2A. Therefore, each transceiver assembly is adapted to mechanically and electrically fit into an Ethernet port of a host device.

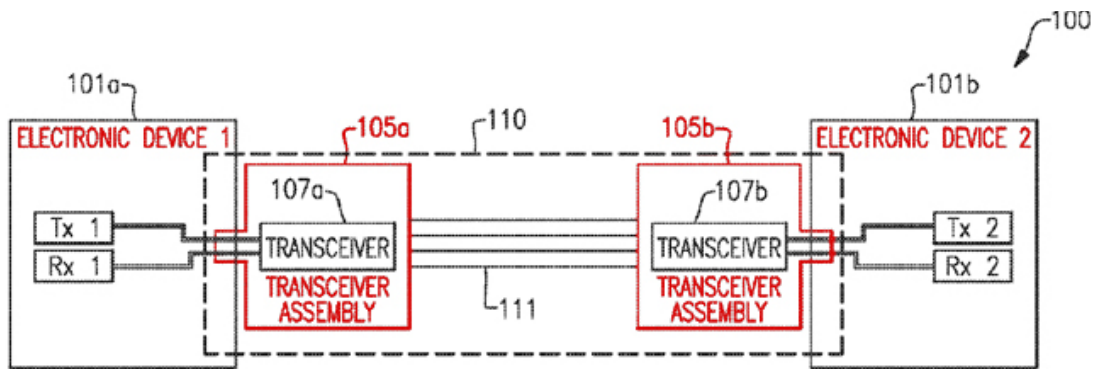
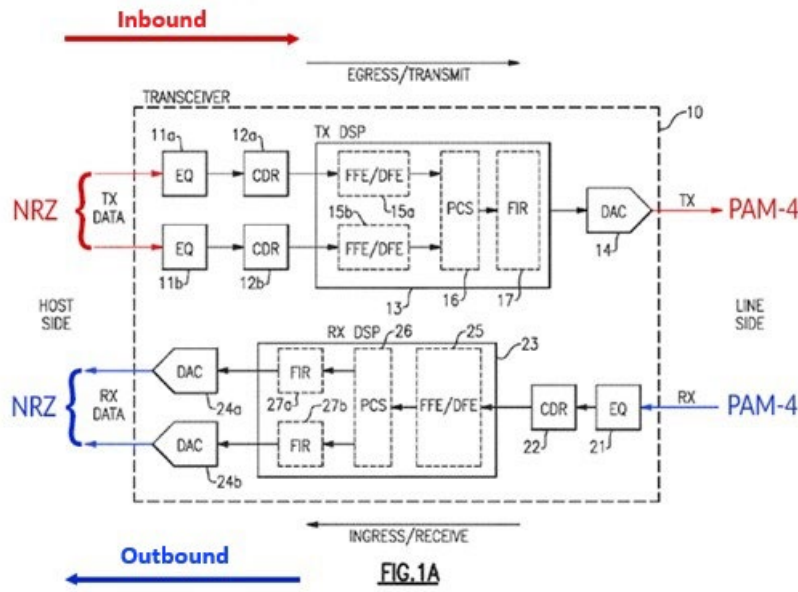


FIG. 2A

210. Lugthart teaches the ports of the host devices are Ethernet ports. Because Lugthart teaches an active Ethernet cable (*see* above §V.C.3[1pre] (explaining Lugthart’s Ethernet teachings)) that connects to a corresponding port on the host device (*Id.*, Fig. 2A, 15:42-52), the host port would be an Ethernet port. Lugthart teaches or suggests this, and it would have been obvious to a POSITA, because otherwise, Lugthart’s active cable would have been inoperable without a compatible Ethernet host port. Indeed, Lugthart teaches form factors that were adapted to fit into Ethernet ports, including SFP, SFP+, and QSFP. *Id.*, 15:42-52.

211. For each corresponding host device, each connector **receives from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable**. Each transceiver assembly “include[s] a [] transceiver” (Ex-1004, 4:10-14) with an “egress/transmit path” “capable of receiving...signals on the host side and multiplexing these signals...for

transmission to the line side over the cable.” Ex-1004, 8:48-60, 15:64-16:3, 19:56-60, Figs.1A, 4A. This means that input signals conveying inbound data streams from the host are received by the transceiver and transmitted over the cable using its egress/transmit path. Ex-1004, 9:26-37. Lugthart also teaches a path going the other way through the cable: each transceiver includes an “ingress/receive path” that is “capable of receiving...on the line side and demultiplexing this signal...for communication to the host side.” Ex-1004, 8:48-60, 16:4-10, 19:56-60, Figs.1A, 4A. Each of the signals conveys a respective inbound (host-to-cable) or outbound (cable-to-host) data stream. *See, e.g.*, Ex-1004, 8:48-60, 9:26-37, Fig.1A. In other words, output signals conveying outbound data streams from the cable to the host are received by the transceiver (in the transceiver assembly) and transmitted to the host via the ingress/receive path. Ex-1004, 9:26-37. I have prepared the following diagram to illustrate the inbound and outbound data streams on one of the transceivers. Ex-1004, Fig.1A:



212. For at least these reasons, Ground 3 teaches [1b].

[1c] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,

213. Lugthart teaches **each of the first and second connectors** (e.g., transceiver assemblies) **including a respective transceiver that performs clock and data recovery on the electrical input signal**. For example, Lugthart teaches that the first and second transceiver assemblies include first and second transceivers. Ex-1004, 14:47-53, 15:25-27. Each transceiver receives input signals through an “egress[/transmit] path from the electronic device side to the cable side” that includes “a pair of equalizers...a pair of CDR circuits...a DSP...and a DAC.” Ex-1004, 21:35-38, 7:66-8:7, 8:13-22, 12:26-57. “The CDR

circuits...digitize the incoming signals as well as [] implement timing recovery to recover a clock and a data signal from the incoming differential signals.” Ex-1004, 21:43-52. This extracts the inbound data stream by “recover[ing] the clock and data signals in the digital domain.” Ex-1004, 21:43-22:2. “[T]he CDR circuits 12a-12b can include analog to digital converters (ADCs),” (Ex-1004, 21:55-57) employing “a first or data recovery ADC [] and a second or clock recovery ADC[.]” Ex-1004, 26:63-66, 1:63-2:3, 21:53-57, 9:26-37, 33:23-28, 10:64-66, 12:27-32, 21:43-46, Figs.1A, 4A, 8. The transceiver also includes “an equalizer configured to...generate a clock and data recovery (CDR) input signal.” Ex-1004, 2:13-16.

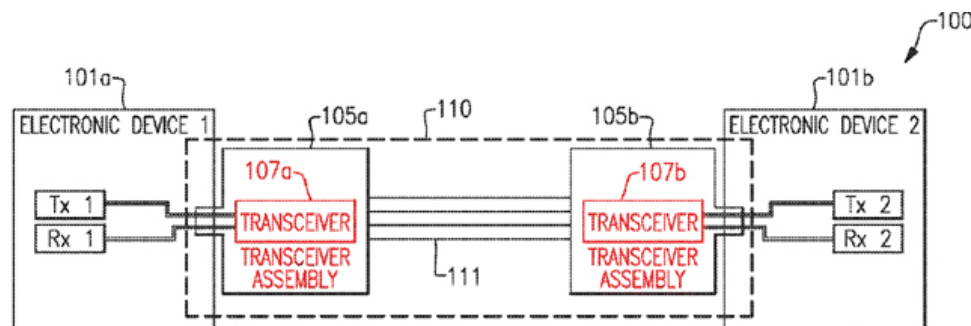
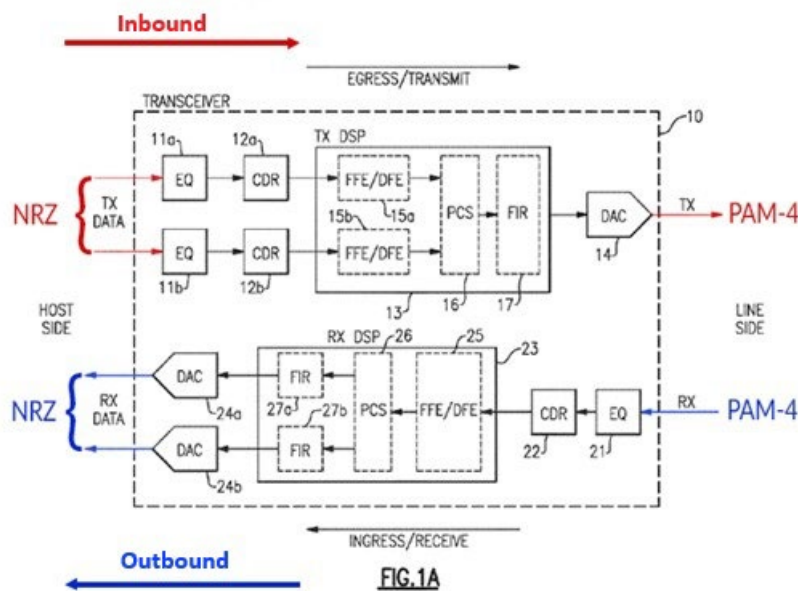


FIG. 2A

214. Lugthart’s transceivers perform CDR **to extract and re-modulate the inbound data stream for transit via the electrical conductors** (e.g., via the cable) **as a respective electrical transit signal conveying a transit data stream.** After clock and data recovery, the transceiver performs remodulation, including for example modulating a PAM-4 signal for transit over the cable. Lugthart describes a

“multi-level modulation encoding” process in which “each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable,” or “vice versa.” Ex-1004, 7:13-30, 7:24-33, 8:40-60, 15:64-16:10, 23:44-58, 24:17-23, Figs.1A, 4B. In other words, Lugthart’s transceiver performs CDR on input NRZ signals to extract an inbound data stream from the host and remodulate the recovered data stream into a PAM-4 electrical transit signal that conveys a transit data stream over the cable; the transit data stream comprises the multiplexed data from inbound data stream from the host. Ex-1004, 8:48-60, 9:52-60, 9:39-42. Therefore, Lugthart’s transceiver performs remodulation by converting a data signal for transmission over a communications channel (e.g., the cable). Ex-1004, Figs.1A, 4A:



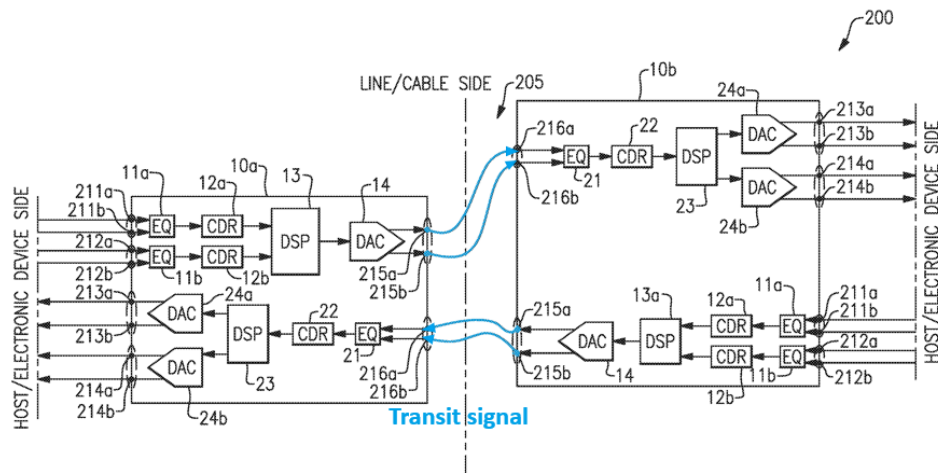


FIG.4A

215. Lugthart further explains the process of data recovery and remodulation in figures 6A-6B. At step 303, the transceivers first “recover[] digital clock and digital data signals from the converted digital signal,” and then “convert[] the multiplexed digital signal to an analog differential signal having a suitable modulation format” “and output the multiplexed analog differential signal into a cable” at step 305. Ex-1004, 30:20-55, Figs.6B, 6A:

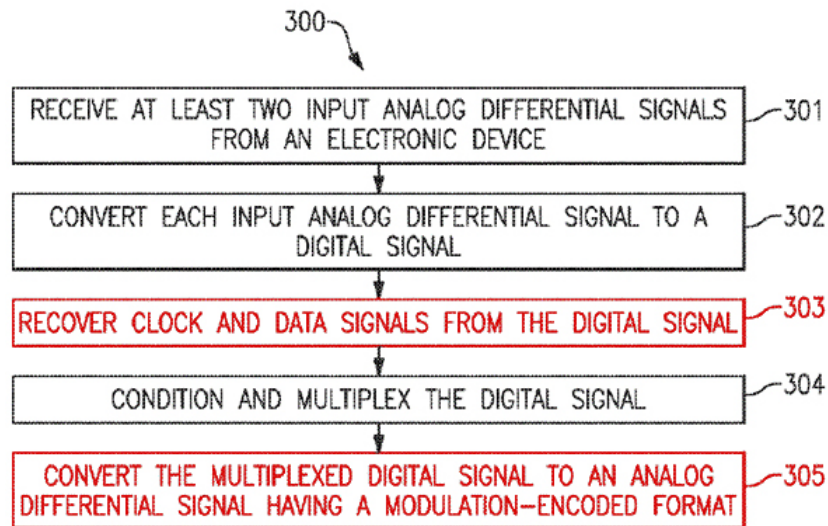


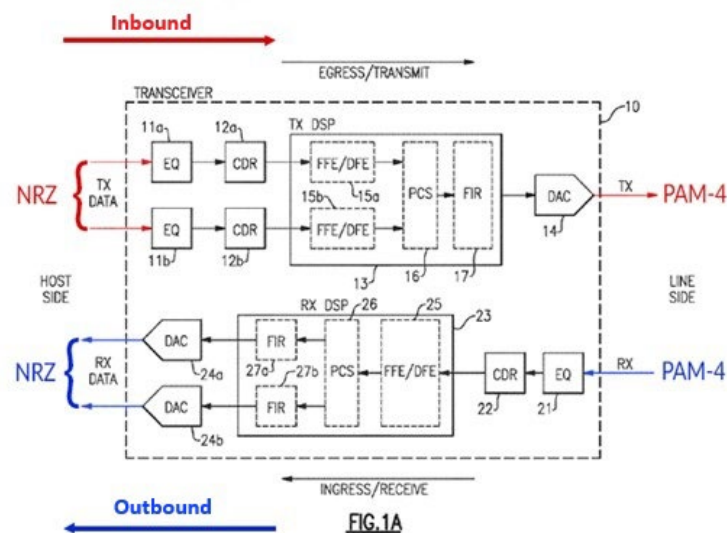
FIG.6A

216. For at least these reasons, Ground 3 teaches [1c].

[1d] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, and

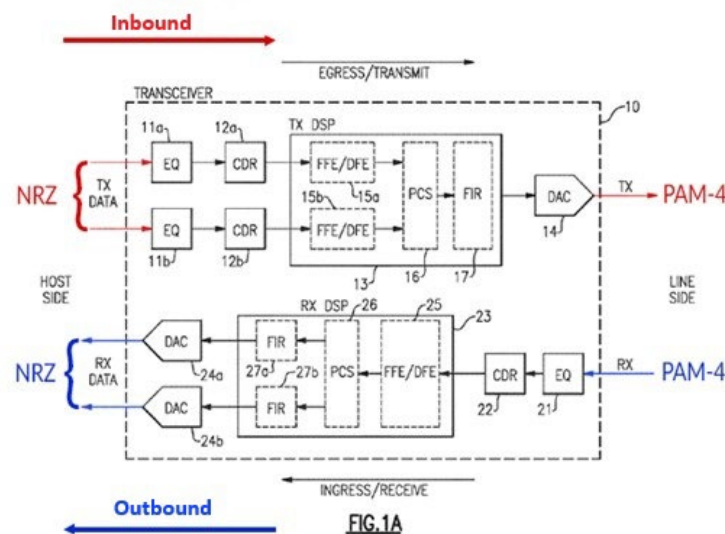
217. Lugthart teaches the **respective transceiver for each of the first and second connectors** (e.g., transceiver assemblies) **performing clock and data recovery on the respective electrical transit signal**. For example, Lugthart teaches that each transceiver receives a transit signal through “the ingress path from the cable side to the electronic device side” that consists of “an equalizer 21, a CDR circuit 22, a DSP 23, and a pair of DACs 24a, 24b.” Ex-1004, 22:40-49, 7:66-8:7, 8:22-32, 9:10-10:22, 12:42-57. The CDR circuit “is configured to digitize the incoming signals as well as to implement timing recovery to recover a clock and a data signal from the incoming differential signals.” Ex-1004, 22:50-55, 9:26-

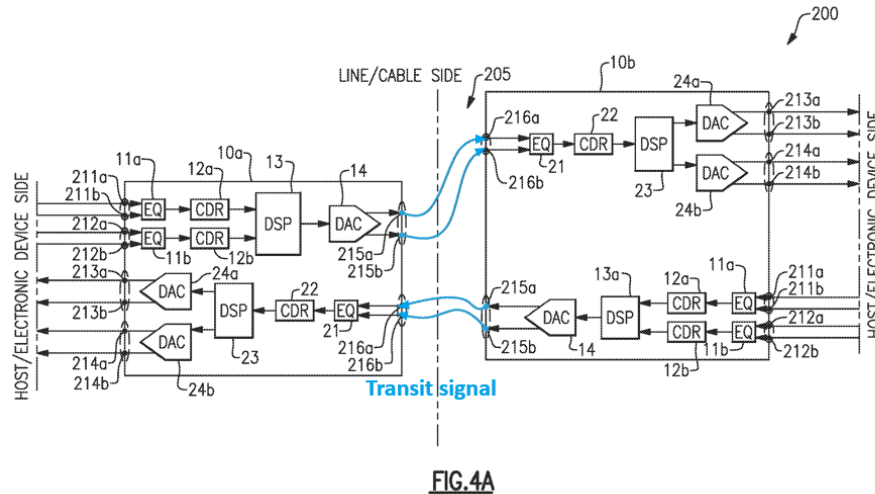
47. “To recover clock and data signals digitally, in some arrangements, the CDR circuit 22 includes analog to digital converters (ADCs).” Ex-1004, 22:57-59, 9:26-47, Figs.1A, 4A, 8. The transceiver also includes “an equalizer configured to...generate a clock and data recovery (CDR) input signal,” that is used in the CDR process. Ex-1004, 2:13-16. The CDR process extracts the transit data stream by “recover[ing] clock and data signals in the digital domain.” Ex-1004, 22:55-57, 9:26-37.



218. Lugthart’s transceivers perform CDR to extract and re-modulate the transit data stream as the outbound data stream from the cable. The transceiver performs remodulation on the data extracted with CDR, including for example modulating it into an NRZ signal for “communication to the host side.” Ex-1004, 8:56-60. Lugthart teaches “an ingress/receive path of the transceiver 10 is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and

demultiplexing this signal into dual 20 Gbit/s NRZ signals.” Ex-1004, 8:56-60, 11:39-51, 24:20-23, 26:13-17, 30:56-59, Figs.1A, 4B. In other words, Lugthart’s transceiver performs CDR on transit PAM-4 signals to extract a transit data stream from the cable and remodulates the recovered data stream into NRZ electrical output signals conveying the data as an outbound data stream to the host; the outbound data stream comprises the data from the inbound data stream. Ex-1004, 8:56-60, 9:65-10:3. Therefore, Lugthart’s transceiver remodulates the transit data stream by modulating the extracted digital data into an NRZ electrical signal for transmission to the host (e.g., the electronic devices). Ex-1004, Figs.1A, 4A-4B:





219. Lughart details the process of data recovery and remodulation in connection with figures 6A-6B. At step 353, the transceivers first “recover[] digital clock and digital data signals from the converted digital signal.” Ex-1004, 30:66-31:2. Then, at step 355, the transceivers “convert[] the de-multiplexed digital signal to a plurality of de-multiplexed analog differential signals having a modulation-encoded format[]” Ex-1004, 31:17-22, Figs.6B, 6A.

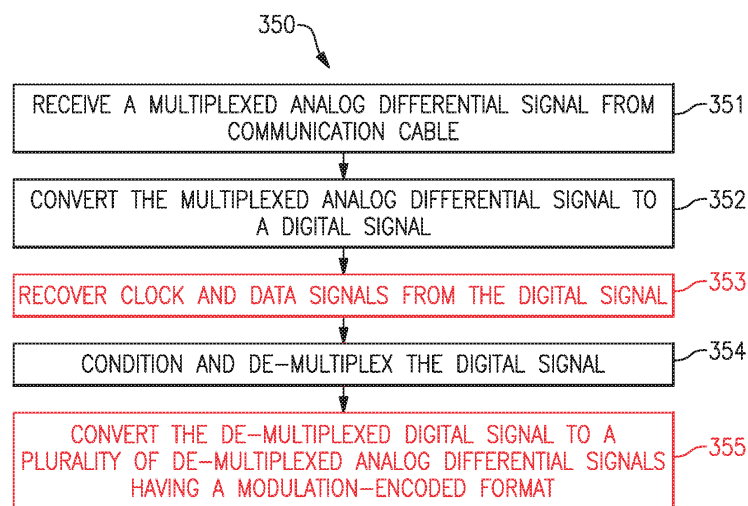


FIG. 6B

Ex-1004, Fig.6B.

220. For at least these reasons, Ground 3 teaches [1d].

[1e] the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.

221. Ground 3 teaches the respective transceivers (e.g., transceivers in the transceiver assemblies) carrying out the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal. *See* above §§V.C.3[1c], [1d] (explaining transceivers performing CDR and remodulation).

222. Ground 3 teaches **the respective transceivers each employing equalization parameters for the remodulation as the outbound data stream and the CDR on the electrical input signal**. For example, Lugthart teaches using equalization its ingress/receive paths as part of recovering the inbound data stream, preconditioning the recovered data stream, and remodulating it for output to the host. Ex-1004, 22:40-49, 24:17-29. Likewise, on the egress/transmit path, Lugthart teaches equalization for the CDR to extract bits from the input signal. Ex-1004, 15:64-16:3, 21:35-38, 23:59-63, Figs.4A-B, 1A:

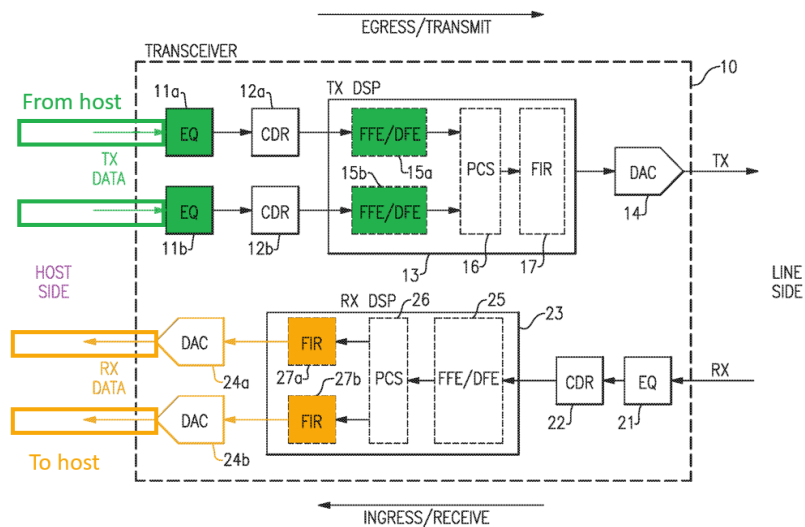


FIG. 1A

223. Lugthart teaches multiple equalization functions for the host-side paths. As shown in orange in the figures above and below, for RX data (outbound data stream from the cable to the host), pre-equalization is used for remodulating the stream before transmission, including for example with FIR filters in the DSP. Ex-1004, 29:21-28, 23:59-64, 23:66-24:2, 9:39-49, Figs.1A, 4B. As shown in green in the figures above and below, for TX data (input signal going from host into the cable), equalizers are used as part of recovering the clock signal and data bits from the electrical input signal, including EQ (11a/11b) and FFE/DFE (15a/15b). Ex-1004, 21:35-38, 7:66-8:7, 8:13-32, 9:10-10:22, 12:26-57, Fig.4A:

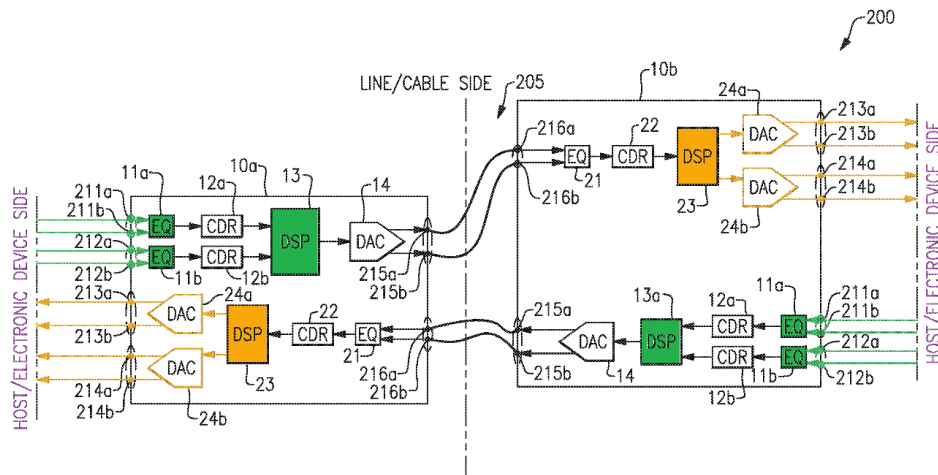


FIG. 4A

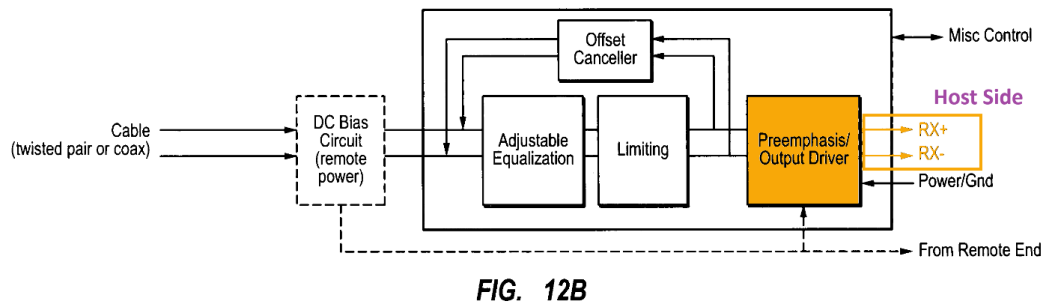
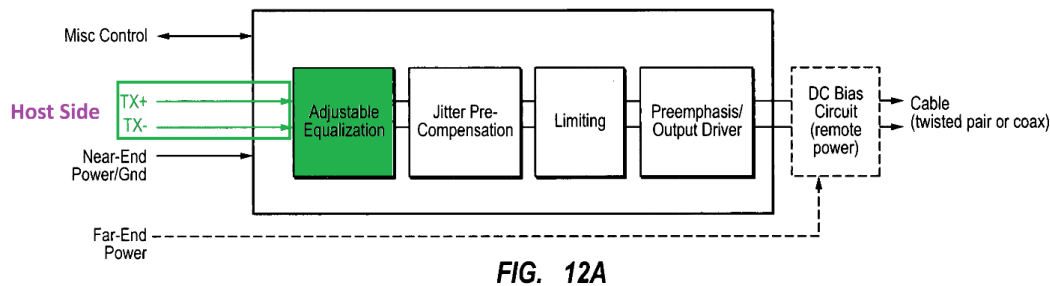
224. Lugthart teaches that these equalization processes use “operating parameters” such as filter coefficients. Ex-1004, 49:8-12 (adjusting “operating parameters for the equalizers”), 49:30-34 (same), 22:12-28 (explaining using FIR tap coefficients to “generate symbol sequence for the multiplexed signal” “before being output to the cable”). Lugthart teaches that FFE/DFE equalization filters were configurable; the parameters used for configuring those filters were equalization parameters. Ex-1004, 23:39-40 (“FFE/DFE blocks 15a-15b can implement one or more digital filters configured to equalize the incoming signal”), 22:5-16. Lugthart’s equalization blocks were textbook equalizer functions that included parameters such as filter coefficients, which a POSITA with experience or coursework in serial communications would have understood. Likewise, Aronson teaches equalization parameters such as “degrees of equalization and/or preemphasis” that specify the gain or level of equalization. Ex-1005, 11:32-48,

13:66-14:5. These teachings all describe equalization parameters that control the effects of the equalization filters, including for example the frequency response and amount of equalization. *See* Ex-1004, 9:10-25, 22:43-48. Therefore, a POSITA would have understood Lugthart's and Aronson's teachings to refer to equalization parameters.

225. Ground 3 teaches that the parameters for equalization are **fixed, cable-independent equalization parameters**. As an initial matter, Lugthart teaches "equalization to compensate for transmission line losses on the host side." Ex-1004, 9:10-25. The parameters for Lugthart's host-side equalization are used to account for channel losses in paths on the host side, rather than cable and therefore do not depend on the characteristics of any particular connecting cable. Moreover, Lugthart's transceivers perform retiming functions that provide separation between the signals on the host- side versus cable- side. Ex-1004, 12: 58–67, Abstract.

226. Aronson teaches using fixed equalization for host-side traces in both directions (Tx and Rx). Ex-1005, 13:52-56, 14:50-57. For the transmit direction (inbound to the cable), Aronson teaches "[t]he first block in this IC would provide equalization to compensation for high frequency loss in the host board traces." Ex-1005, 13:49-54 "Such equalization could be fixed[" Ex-1005, 13:54-56. On the receive side, the host-facing preemphasis block provides equalization for outbound signals to the host. Ex-1005, 14:50-57 ("[F]or driving the host PCB traces at this

end of the cable, an output driver is provided with optional preemphasis. ...The preemphasis could be fixed...”), Figs.12A, 12B:



227. Figures 12A-B include a label for “Adjustable Equalization” but the corresponding specification description teaches several options including using it for fixed equalization. Ex-1005, 13:54-56. The motivation to use fixed equalization is explained in the Motivation subsection below. Additionally, Aronson uses “adjustable” to refer to “adjustment at the factory,” which is fixed during normal usage. Ex-1005, 14:54-57, 14:37-41.

228. Aronson teaches parameters for host-side equalization that compensate for loss from host-side board traces, rather than the connecting cable: “[d]ifferent host systems may require different degrees of equalization and/or preemphasis because of the particular length or other nature of the electrical

interconnect between the cable receptacle and the next IC elements.” Ex-1005, 11:32-48. These host-side equalization parameters do not operate on any cable signals and do not relate to any properties of the connecting cable.¹¹ It would not have made sense to customize these host-side parameters on a cable-by-cable basis, based on the characteristics of individual connecting cables, given Aronson’s teaching and suggestion that it would not be beneficial. Therefore, the combination of Lugthart and Aronson teaches or suggests fixed, cable-independent equalization parameters for host-side paths. Additionally, a POSITA would also have found this obvious for reasons explained below.

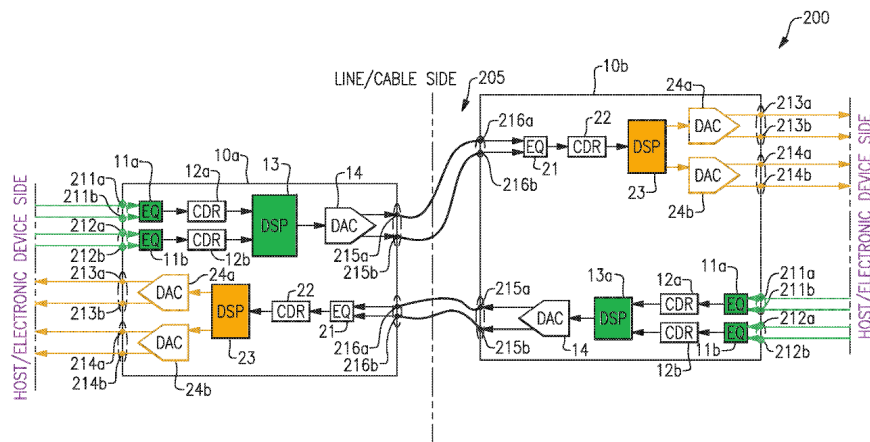


FIG. 4A

¹¹ Patent Owner argued that parameters for these host-side paths satisfy cable-independent parameters because they “are independent of communications through the cable”. Ex-1022, 13-14 (pointing to pre-equalized filters for “chip-to-module connection,” which refers to the path from the host to the closest transceiver); *see also* Ex-1023, 16-18 (same); Ex-1024, 8-9 (same).

229. **Motivation to Combine.** A POSITA would have been motivated, and found it obvious, to combine Lugthart with Aronson to use the same fixed parameters for host-side equalization across different cables. Aronson teaches fixed equalization parameters (Ex-1005, 14:34-41, 13:49-14:5, 14:50-57), and ultimately, there are only two possibilities for setting those fixed parameters: (1) use the same parameters across different cables, or (2) customize the parameters on a cable-by-cable basis. Here, both Lugthart and Aronson provide motivation to use the same parameters, by teaching that host-side equalization parameters do not vary between different connecting cables. Ex-1005, 11:32-48; Ex-1004, 9:10-25. Therefore, there was little justification for the extra complication, time, or cost of customizing these parameters for properties of individual cables, when it would be equally effective to simply use the same host-side parameters for all active cables of a given design. While multi-purpose retimer designs may incorporate more complex training or adaptation features to handle a range of unknown channels, such as when used in the middle of a long backplane or between two long passive cables, Ground 3 teaches a specific active cable application with express teachings of using fixed equalization parameters for host-side paths (Ex-1005, 13:52-56, 14:50-57), which were well-suited for using fixed, common equalization parameters because they involve short paths to a nearby host chip rather than long cable distances. In summary, this was a simple choice from a

finite number of identified, predictable solutions for setting equalization parameters, with a reasonable expectation of success because it simply involved setting the same fixed parameters that Aronson teaches. Ex-1005, 13:49-56, 13:66-14:5, 14:33-40, 14:50-57.

230. Lugthart teaches an active Ethernet cable with equalizer parameters. *E.g.*, Ex-1004, 8:66-9:32, 9:10-51, 21:35-42, 22:3-16. Therefore, a POSITA would have looked to references disclosing such details in the context of active cables, such as Aronson. Aronson provides those details for active Ethernet cables and teaches or suggests common approaches in the industry for setting equalization parameters, including the use of the same, preset parameters for the host-side and customized parameters for the cable side. Ex-1005, 13:49-56, 13:66-14:5, 14:33-40 14:50-57. A POSITA would have been motivated to combine these teachings, which simply combines prior art elements according to known methods to yield predictable results. Moreover, this was simple, common sense because, as explained above, these host-side parameters do not depend on the individual properties of the connecting cable.

231. Furthermore, the prior art provides teaching, suggestion, and motivation to use preset equalization parameters as taught by Aronson. Ex-1007, ¶¶124-126; Ex-1032, Tbls. 39-40; Ex-1020, 000020-21 (“FFE tap weights are determined for many applications by design and coded as fixed values within

system software”); Ex-1021, 7:18-33 (“coefficients of the tap(s)...may be pre-programmed or pre-set”), 1:65-67 (FIR filter “typically includes a one or more taps having fixed or pre-programmed...coefficients.”).

232. A POSITA would have found Aronson’s equalizer teachings to be applicable to Lugthart’s equalizers because they address losses in corresponding portions of active cables and hosts. For example, in the transmit path (Tx), Lugthart teaches equalization to address signal losses caused by the host-side paths (Ex-1004, 15:64-16:3), specifically describing “transmit path equalizers” to “provide signal equalization to compensate for transmission line losses on the host side” (Ex-1004, 9:10-15) and “FFE/DFE” to “equalize the incoming signal [from the host]” (Ex-1004, 38-42). In the transmit path, closer to the cable, Lugthart further teaches using a FIR filter to “condition the signal and forward the processed signal” for re-transmission over the cable, thereby “perform[ing] emphasis on the signal to compensate for channel losses.” Ex-1004, 23:59-63, 15:64-16:3, Fig.1A:

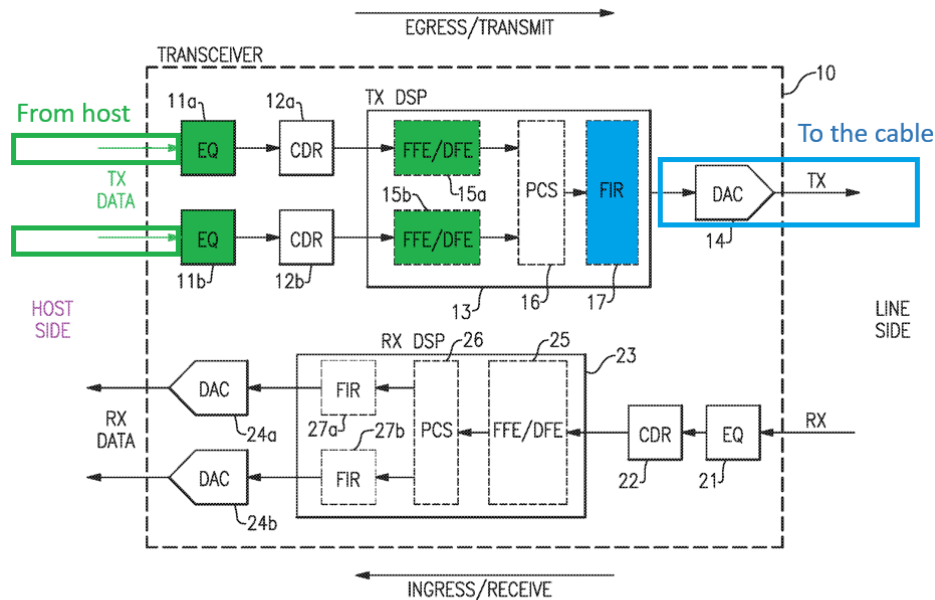


FIG. 1A

233. Aronson likewise teaches host- and cable-facing equalizers. For example, on the driver IC (Tx), “[t]he first block in this IC [facing the host side] would provide equalization to compensate for high frequency loss in the host board traces,” while “[t]he final block [facing the cable] provides preemphasis to...overcome the larger [signal] loss on the cable” (Ex-1005, 13:49-14:5). Therefore, for the transmit path, Aronson’s equalization in the first block corresponds to Lugthart’s equalizer and FFE/DFE, with both addressing host-side losses, while Aronson’s final block and Lugthart’s FIR filter both apply pre-equalization or pre-emphasis to address cable losses. Ex-1005, Fig.12A:

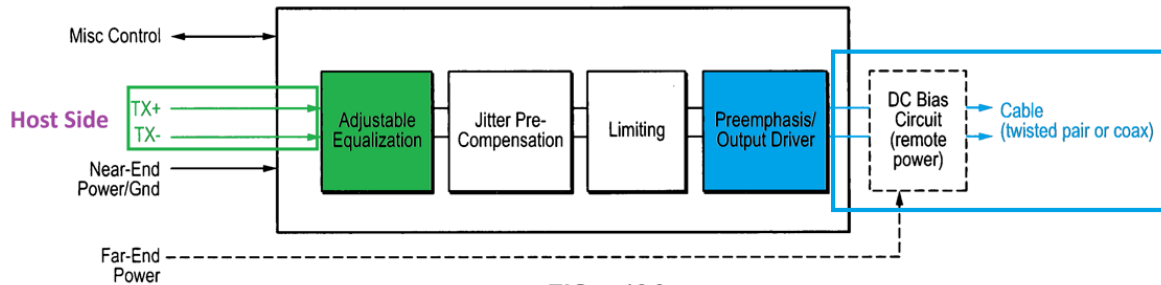


FIG. 12A

234. The same observation applies to the ingress/receive path, as Lugthart's and Aronson's receive paths incorporate corresponding components to those in their respective transmit paths, with the receive path "follow[ing] somewhat in the reverse" of the transmit path. Ex-1005, 14:22-51; Ex-1004, 8:22-32, 23:17-23, 24:3-4. In the ingress/receive paths, Lugthart's equalizer and FFE/DFE block functionally correspond to the equalization block on Aronson's receiver IC, as both handle transit signals from the cable. Ex-1004, 9:10-15, 8:22-32; Ex-1005, 14:33-40. And Lugthart's receive path FIR corresponds to Aronson's preemphasis block on the receiver IC, as both pre-equalize signals to be transmitted to the host. Ex-1005, 14:50-57, Fig.12B; Ex-1004, 8:26-32, 9:38-10:3, Fig.1A.

235. In view of the correspondence between Aronson's and Lugthart's equalizers, a POSITA would have been motivated to apply Aronson's teachings regarding the calibration of equalization parameters to Lugthart's similarly positioned equalizers. In this way, Aronson's teachings provide additional details suggested by Lugthart.

236. The combination would not have changed the principle of operation for either reference. Applying Aronson's calibration teachings to Lugthart simply fills in implementation details for Lugthart which already teaches equalization in an active cable. Ex-1004, 8:66-9:51, 21:35-42, 22:3-16. Using Aronson's teachings of fixed, cable-independent equalization parameters with Lugthart is entirely consistent, as Aronson already provides those teachings in the context of active cables, for equalization of the same host-side paths. Ex-1005, 13:49-56, 14:50-57, Figs.12A, 12B. While the combination affects when equalization parameters are set, the actual equalization functions would operate as before.

237. In addition to the reasons explained earlier in this section, a POSITA would have had a reasonable expectation of success in combining teachings from Lugthart and Aronson because the combination simply determines the time when equalization parameters are set, along with simple configuration and selection techniques taught by Aronson. These minor changes would not affect the principle of operation. Moreover, having fixed, cable-independent parameters is a trivial matter of saving the same parameters in non-volatile memory, which is a basic programming task within the capability of undergraduate students. Using hard-coded parameters was simple and well-known and widely used in the art for decades before 2019. *See* Ex-1020, 000020-21 ("FFE tap weights are determined for many applications by design and coded as fixed values...."); Ex-1021, 7:18-33,

1:65-67; Ex-1032, Tbls. 39-40. These were used in a variety of industry standards and taught in undergraduate courses.

238. For at least these reasons, Ground 3 teaches [1e].

4. Dependent Claim 2

2. The active Ethernet cable of claim 1, wherein the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal.

239. As an initial matter, I previously explained how Ground 3 teaches the respective transceivers each employing equalization parameters. *See above* §V.C.3[1e]. And I previously explained the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal. *See above* §§V.C.3[1c], V.C.3[1d] (explaining the remodulation and CDR), Ex-1004, Fig.4A:

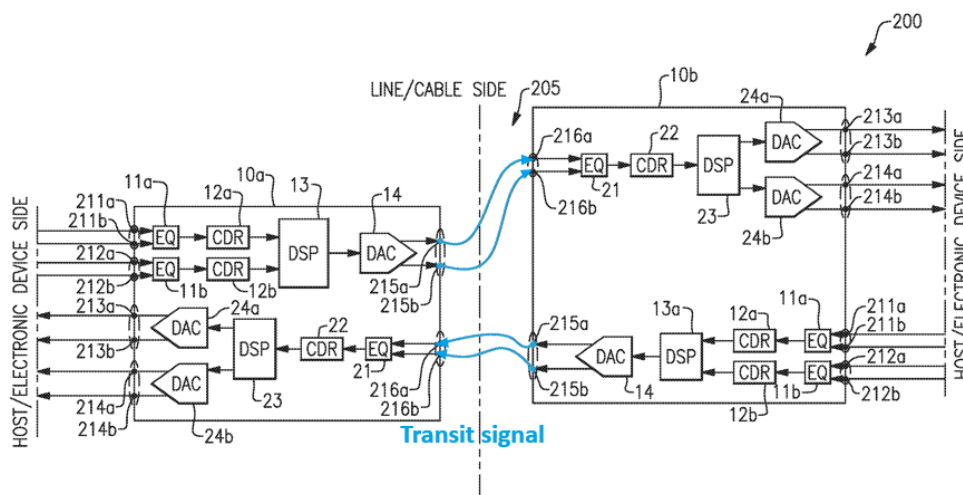


FIG. 4A

240. Lugthart teaches **employing equalization parameters for the remodulation of the inbound data stream for transit and data recovery performed on the electrical transit signal**. For example, Lugthart teaches multiple equalization functions for the path over the cable. In the transmitting direction (from the host's perspective), after extracting the inbound data stream from the host (*supra* §V.C.3[1c]), each of Lugthart's transceivers includes an FIR filter 17 in DSP 13 to "condition the [input] signal" for re-transmitting "over the cable" (Ex-1004, 15:64-16:3) "as a multi-level modulated signal." (Ex-1004, 23:59-63). Ex-1004, 7:6-20. The FIR filter performs equalization for the remodulation of the inbound data stream for transit. Figs.4A, 1A:

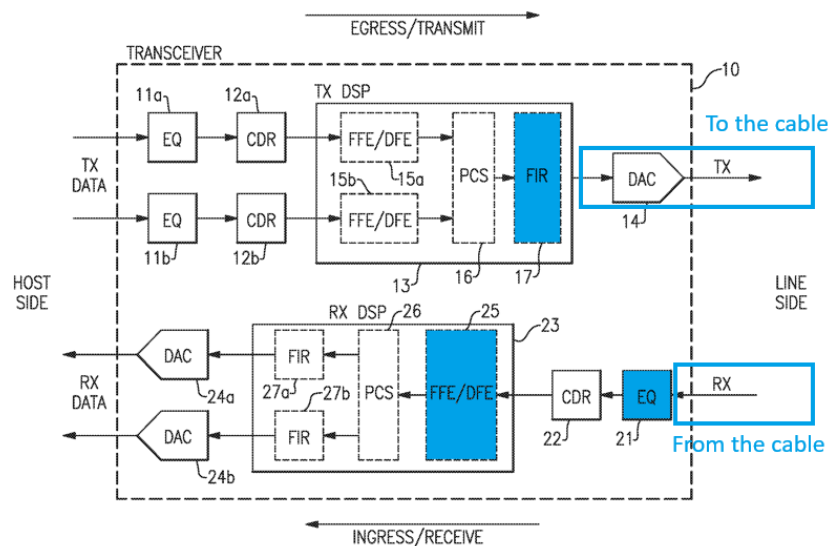


FIG. 1A

In the other direction (receiving direction from the host's perspective) for the ingress/receive path, to recover bits from the data stream, Lugthart's transceivers

use equalizer (21) to “compensate for losses occurring during transmission over the cable” (Ex-1004, 22:43-59, 8:19-32), while FFE/DFE (25) in the DSP provides additional equalization to “reduce signal distortion resulting from ISI or other signal impairments” (Ex-1004, 28:30-35, 24:3-16, 23-38-43). Ex-1004, Figs.1A, 4A:

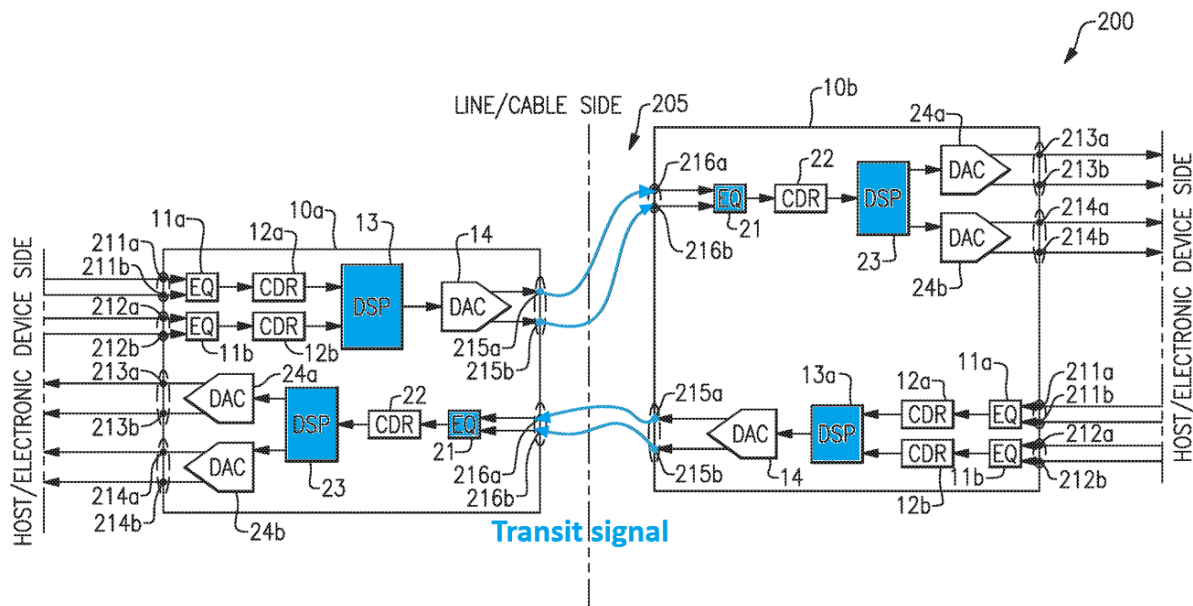


FIG.4A

241. As I explained above, Lugthart and Aronson teach that these equalization functions (e.g., FIR pre-equalization, EQ, DFE/FFE) employ various parameters that control their operation; since the transceivers are used symmetrically, that analysis likewise applies here. *See above* §V.C.3[1e]; Ex-1004, 22:12-16, 49:8-12, 49:30-34; Ex-1005, 11:32-48, 13:66-14:5. Equalization parameters are used to configure the equalizer to compensate for losses from the

connecting cable. Ex-1004, 22:43-45 (“The equalizer 21 can be configured to compensate for losses occurring during transmission over the cable....”).

242. Ground 3 further teaches **employing cable-dependent equalization parameters** for remodulation of the inbound data stream and the clock and data recovery performed on the electrical transit signal. Lugthart uses equalization to “compensate for losses occurring during transmission over the cable” (e.g., losses related to the specific cable used in the transmission). Ex-1004, 22:40-49.

Therefore, these equalization parameters compensate for the loss characteristics of the particular connecting cable and depend on its characteristics.

243. Ground 3 combines Lugthart with Aronson. *See* above §V.C (explaining combination). Aronson teaches that the final block of the driver (Tx) IC “provides preemphasis to the...transmitted signal to overcome the larger loss on the cable” and setting the preemphasis “individually to match the particular length of the characteristics of the copper cabling.” Ex-1005, 13:66-14:5. Here, Aronson uses preemphasis to perform pre-equalization before transmission. On the receive (Rx) IC side, Aronson discloses the “adjustable equalization” block “compensate[s] for the cable high frequency rolloff, rather than the host PCB traces in the case of the driver.” Ex-1005, 14:33-40. “[A]djustable but factory set equalization is of particular interest because the cable length and characteristics will be established at the time of the cable manufacture.” Ex-1005, 14:22-41.

Therefore, Aronson teaches cable-side equalization parameters that depend on the characteristics of the individual connecting cable (at the time of manufacture), including its exact length and other characteristics. Aronson teaches adjusting those parameters for the particular characteristics of an individual cable, on a cable-by-cable basis. Therefore, Ground 3 teaches or suggests employing cable-dependent equalization parameters. Additionally, Ground 3 teaches particular implementations of cable-dependent equalization parameters, explained below. *Infra* §V.C.5 (claim 3), §V.C.6 (claim 4).

244. **Motivation to Combine.** A POSITA would have found it obvious and been motivated to combine these teachings from Lugthart and Aronson. The references provide express motivation to apply Aronson's adjustments, which match equalization parameters to cable characteristics, by teaching that cable-side equalization compensates for losses caused by the connecting cable. *E.g.*, Ex-1004, 22:40-49; Ex-1005, 13:66-14:5, 14:33-40; Ex-1005, 13:66-14:5, 14:22-41. Due to manufacturing variation, the exact physical properties such as length and width will vary from cable to cable, and their effect on signal loss will therefore vary between cables. Therefore, a POSITA would have been motivated to customize cable-side equalization parameters for the particular cable, tailored the characteristics of that individual cable as Aronson teaches. Ex-1005, 13:66-14:5, 14:22-41. This would have applied a known technique to improve similar devices

in the same way because Aronson taught this parameter adjustment for active cables. *See* above §V.C.3[1e] (Motivation subsection explaining correspondence between Aronson’s and Lugthart’s equalizers).

245. The application of Aronson’s cable-side adjustments to Lugthart would have improved the effectiveness of equalization and enhanced overall signal quality performance. This would have been appropriate for applications that demanded maximum performance, high data throughput, or extended cable lengths. For example, this would benefit data centers requiring long cable lengths or high bitrates by more accurately compensating for cable-specific losses and thereby improving signal quality. For at least these reasons, Ground 3 teaches Claim 2.

5. Dependent Claim 3

3. The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters adapt during usage of the Ethernet cable.

246. I explained how Ground 3 teaches an active Ethernet cable (*see* above §V.C.3[1pre]) and transceivers that employ cable-dependent equalization parameters (*see* above §V.C.4).

247. Ground 3 teaches **said cable-dependent equalization parameters adapt during usage of the Ethernet cable**. For example, Lugthart teaches training phases to account for determined “channel parameters such as...loss, noise, dispersion, non-linearity, etc.” Ex-1004, 48:20-27, Fig.15. “[T]he parameters of the

components in the transceivers” are adjusted to the cable’s transmission characteristics so that “signals at the full baud rate can be transmitted and received at an error rate that is below or equal to a threshold error value.” Ex-1004, 48:64-49:19, 49:20-37, Fig.15 (steps 902, 903). This includes the “phase of the recovered clock, the shape of the transmitted pulse, levels for the thresholder/automatic gain controller in the receiver, operating parameters for the equalizers, etc.” Ex-1004, 49:8-14, 49:30-34 (same). Because the adjustment of the parameters accounts for the characteristics of the communication channel, the adjustment adapts the equalization parameters. Lugthart teaches carrying out the training after “Start-Up” while “establishing a high-speed communication link between a first electronic device and a second electronic device.” Ex-1004, 47:53-65, Fig.15. A POSITA would have understood that establishing a high-speed communication link occurs during usage of the Ethernet cable because it occurs when the cable is connected, and communication links are established to carry out communication and transmit data over cables.

248. Aronson reinforces Lugthart with its teachings of “adaptive equalization.” Ex-1005, 11:32-48, 14:33-40. Aronson teaches equalization that is “automatically adaptive.” Ex-1005, 13:49-14:5.

249. **Motivation to Combine.** A POSITA would have been motivated to apply Aronson’s adaptive equalization teachings to Lugthart’s equalizers for

several reasons. First, Aronson reinforces Lugthart, which already teaches equalizer training and includes analogous equalizer functions to Aronson, as previously explained. *See* above §V.C.3[1e] (Motivation to Combine subsection). Additionally, Aaronson’s teachings automatically adapt equalization parameters to changing conditions. Therefore, while parameter training adds complexity, the tradeoff is often made when high signal quality is needed or for environments with unpredictable electromagnetic interference and thermal issues, for example, a data center with noisy devices that lack electromagnetic interference (“EMI”) shielding or have limited cooling capacity. As another example, large EMI is expected in long cables that are routed by noisy equipment in a data center. For at least the reasons explained above, Ground 3 teaches Claim 3.

6. Dependent Claim 4

4. **The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable.**

250. As I explained previously, Lugthart and Aronson teach **cable-dependent equalization parameters**. *See* above §V.C.4 (explaining cable-dependent parameters).

251. Ground 3 teaches the cable-dependent equalization parameters **are fixed during normal usage of the Ethernet cable** having been **determined**

during manufacturing-testing of the Ethernet cable. For example, Aronson teaches “fixed...equalization” for its adjustable equalization block. Ex-1005, 14:34-41. “Adjustable but factory set equalization is of particular interest because the cable length and characteristics will be established at the time of the cable manufacture.” *Id.* Likewise, the pre-equalization “can be adjusted at factory setup individually to match the particular length of the characteristics of the copper cabling.” Ex-1005, 13:65-14:5. Aronson explains, that the equalization parameters could be fixed, for example, to provide “gains of 12 dB or larger.” Ex-1005, 14:1-5. Aronson teaches or suggests that all of these parameters are determined and fixed during “factory setup” “at the time of the cable manufacture” which includes manufacturing-testing to adjust equalization parameters for individual cables to match the particular length and characteristics of the copper cabling. Ex-1005, 14:1-41.

252. **Motivation to Combine.** A POSITA would have would have been motivated to apply Aronson’s teachings, as explained above, to determine and store fixed equalization parameters during manufacturing. This would have simply combined prior art elements (e.g., determining equalization parameters for individual cables and then storing them as fixed values for Lugthart’s active cable) according to known methods to yield predictable results (e.g., fixed parameters). Moreover, this approach would have been beneficial for example for

manufacturers that do not want to invest time and money implementing protocols for adaptive training, reducing engineering time and costs that must be recovered through sales of the cable. As another example, some users or consumers only needed a simple and reliable active cable, without the overhead or complexity of adaptive training. This approach was beneficial in environments where cable channel characteristics remained stable over time, for example data centers or structured enterprise networks with known noise or thermal characteristics constrained by distance or shielding requirements or best practices. Using fixed equalization parameters, adjusted at the factory for individual cables, would have addressed these types of market demands while still providing equalization tailored to the individual cable. Moreover, a POSITA would have recognized that Aronson's teachings would have readily been incorporated into QA process for verifying that assembled cables operate correctly. Combining Aronson's teachings with established QA processes would have simply combined prior art elements according to known methods to yield predictable results. For at least the reasons explained above, Ground 3 teaches claim 4.

7. Dependent Claim 5

5. The active Ethernet cable of claim 4, wherein the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd.

253. Ground 3 teaches an active Ethernet cable with an inbound data stream (from host to cable) and an outbound data stream (from cable to host), as I explained previously. *See* above §§V.C.3[1b], V.C.3[1c].

254. I have also explained above how Lugthart teaches the active Ethernet cable of claim 4, wherein the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd. While that analysis was provided in the context of Ground 2, it likewise applies here because Ground 3 uses Lugthart as the primary reference. *See* above at §V.B.1.

255. For at least these reasons, Ground 3 teaches claim 5.

8. Independent Claim 6

256. Claim 6 largely mirrors the language of claim 1, but claims a *method* comprising a network cable. Therefore, claim 6 is satisfied for reasons that I explained above for claim 1.

[6pre] A communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector:

257. I understand that a preamble generally does not state a claim limitation. Nevertheless, it is my opinion that Ground 3 teaches [6pre].

258. Lugthart teaches a **communication method that comprises a network cable**. For example, Lugthart is directed to “methods for high speed communications” to “achieve reliable high-speed point-to-point communication between different electronic devices, computing devices, storage devices and peripheral devices.” Ex-1004, Abstract. Lugthart teaches a communications method for active Ethernet cables with the various components and techniques I explained above for claim 1. *See* above §V.C.3. Aronson likewise teaches methods for “the use of a communication cable.” Ex-1005, 4:36-54. As I explained for claim 1 above, Ground 3 teaches an active Ethernet cable; this is a network cable because Ethernet is a networking protocol and the cable is used to convey Ethernet communications. *See* above §V.C.3[1pre].

259. Ground 3 teaches the network cable including **conductor pairs electrically connecting a first connector to a second connector** (e.g., transceiver assemblies). For example, Lugthart teaches “the cable can correspond to an electrical cable including one or more pairs of differential micro coaxial cables or conductors.” Ex-1004, 6:65-7:5, 17:35-19:33 (“pairs of conducting lines 141-142”), Figs.3A-3C. The “electrical conducting lines...transport electrical signals” between the transceiver assemblies. Ex-1004, 16:11-36, Fig.4A. “Each of the pairs of conducting lines [] can be configured for differential signal transmission” for inbound data from a first transceiver assembly to a second assembly and vice

versa. Ex-1004, 17:43-45, 18:35-39, 14:7-28, Figs.2A-2B. I previously explained how Ground 3 teaches electrical conductors that connect the first and second connectors. *See* above §V.C.3[1a].

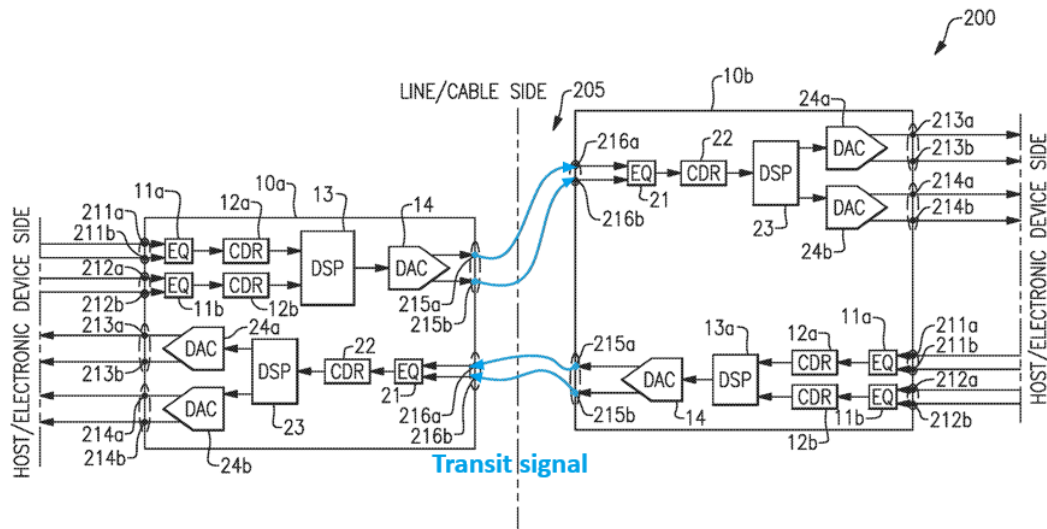


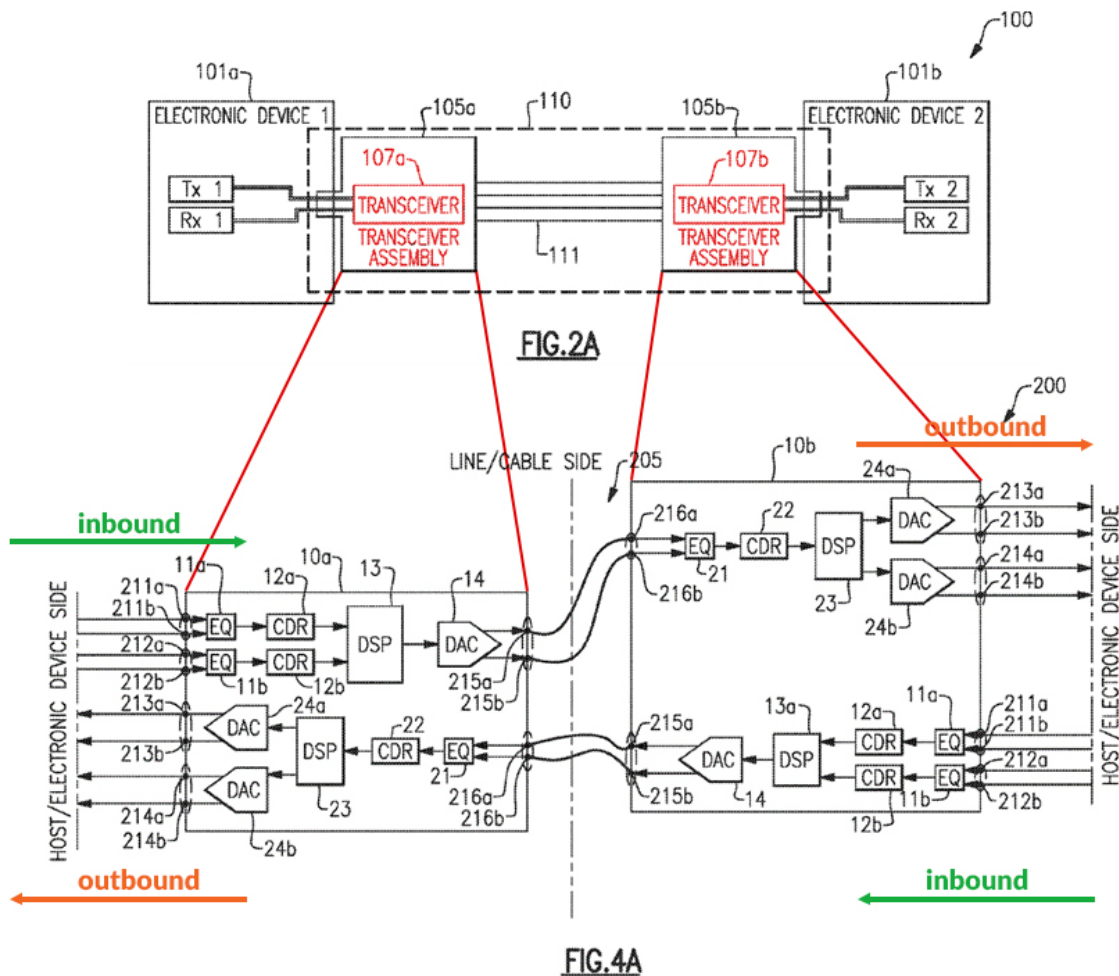
FIG. 4A

260. For at least these reasons, Ground 3 teaches [6pre].

[6a] receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device;

261. The elements in [6a] also appear in [1b] and are satisfied for the same reasons. *See* above §V.C.3[1b]. Either of Lugthart's transceiver assemblies is the first connector; the other active plug is the second connector. The first electrical input signal and inbound data stream are the ones received by the first connector from its corresponding host (recited in [1b]), which is the first host device. As

explained previously, the first connector (active plug) includes a first transceiver inside. *Id.*



[6b] performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream;

262. The elements in [6b] also appear in [1c], and my analysis for [1c] already explained this limitation for both the first and second connectors; the first input signal, data stream, and host device are the ones that correspond to the first

connector. Therefore, limitation [6b] is satisfied for the same reasons explained previously. *See* above §V.C.3[1c].

[6c] re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs;

263. The elements in [6c] also appear in [1c] and are satisfied for the same reasons. *See* above §V.C.3[1c]. For [1c], I explained how Ground 1 teaches an electrical transit signal (conveying a transit data stream) going over the conductors in one direction, and another transit signal going in the opposite direction. Here, the first transit data stream is the stream conveyed by the (first) transit signal going from the first connector to the second connector. *Id.* As explained, the output of the first connector is transmitted over a (first) conductor pair to the second connector. *See* above §V.C.8[6pre].

[6d] receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device;
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264. Limitation [6d] mirrors [6a] and differs only by changing “first” to “second.” Like [6a], the elements in [6d] also appear in [1b], and my analysis for [1b] already explained this limitation for both the first and second connectors; the second input signal, data stream, and host device are the ones that correspond to the second connector. Therefore, limitation [6d] is satisfied for the same reasons explained previously. *See* above §V.C.3[1b].

[6e]	performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream;
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265. Limitation [6e] mirrors [6b] and differs only by switching “first” and “second.” Like [6b], the elements in [6e] also appear in [1c], and my analysis for [1c] already explained this limitation for both the first and second connectors; the second input signal, data stream, and host device are the ones that correspond to the second connector. Therefore, limitation [6e] is satisfied for the same reasons explained previously. *See* above §V.C.3[1c].

[6f]	re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs;
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266. Limitation [6f] mirrors [6c] and differs only by switching “first” and “second.” Like [6c], the elements in [6f] also appear in [1c] and are satisfied for the same reasons, with the second electrical input signal and inbound data stream being those received by the second connector, and the second transit data stream being the one conveyed from the second connector to the first. *See* above §V.C.3[1c]. As explained, the output of the second connector is transmitted over a (second) conductor pair to the first connector. *See* above §V.C.8[6pre].

[6g] performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream;

267. The elements in [6g] also appear in [1d] and are satisfied for the same reasons, with the first electrical transit signal being the one conveyed from the first transceiver in the first connector to the second transceiver in the second connector through the cable. *See* above §V.C.3[1d].

[6h] re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device;

268. The elements in [6h] also appear in [1d] and are satisfied for the same reasons, with the first transit data stream being the transit data stream that the second transceiver received from the cable, and the second outbound data stream being the data stream output by the second transceiver to the corresponding host through the second connector. *See* above §V.C.3[1d]. As explained previously for [1b], the second outbound data stream is conveyed by an electrical output signal to the second host device. *See* above §V.C.3[1b].

[6i] performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream; and

269. Limitation [6i] mirrors [6g] and differs only by switching “first” and “second.” Like [6g], the elements in [6i] also appear in [1d], and my analysis for

[1d] already explained both the first and second transceivers along with their respective signals, streams, and host devices; therefore, limitation [6i] is satisfied for the same reasons explained previously. *See* above §V.C.3[1d].

[6j] performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream; and
--

270. Limitation [6j] mirrors [6h] and differs only by switching “first” and “second.” Like [6h], the elements in [6j] also appear in [1d] and [1b], and my analysis for [1d] and [1b] already explained both the first and second transceivers along with their respective signals, streams, and host devices; therefore, limitation [6j] is satisfied for the same reasons explained previously. *See* above §§V.C.3[1d], V.C.3[1b].

[6k] wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.
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271. The elements in [6k] also appear in [1e] and are satisfied for the same reasons. *See* above §V.C.3[1e]. Specifically, the first and second transit data streams correspond to the transit data streams received by the second and first transceivers, respectively, and the first and second electrical input signals are those received by the first and second transceivers, respectively from the first and second hosts.

9. Dependent Claim 7

- 7. The communication method of claim 6, wherein cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said performing clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.**

272. As I explained for claim 2, Ground 3 teaches cable-dependent equalization parameters are employed for the re-modulating of inbound data streams and the clock and data recovery on the transit signals. *See* above §V.C.4.

273. Because the cables are bidirectional and symmetrical in operation (*see* above §V.C.3 (introduction explaining Lugthart's and Aronson's symmetry)), Ground 3 teaches employing cable dependent equalization parameters for remodulation of both the first and second inbound data streams and for clock and data recovery of both the first and second transit signals.

274. Therefore, Ground 3 employs cable-dependent equalization parameters for at least one of the recited re-modulation or CDR operations.

275. For at least these reasons, Ground 3 teaches Claim 7.

10. Dependent Claim 8

8. The communication method of claim 7, wherein said cable-dependent equalization parameters are adaptively updated.

276. Ground 3 teaches claim 8. Ground 3 teaches the cable-dependent equalization parameters are adapted during usage of the Ethernet cable, e.g, with Lugthart's training routines, as explained above for claim 3. Therefore, the same analysis that I explained above for claim 3 applies here. *See* above §V.C.5 (claim 3), §V.C.4 (claim 2).

277. For at least these reasons, Ground 3 teaches claim 8.

11. Dependent Claim 9

9. The communication method of claim 7, wherein said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable.

278. Claim 9 shares elements with claim 4 that are satisfied for the same reasons. Claim 9 recites **manufacturerer-testing**, instead of manufacturinging-testing. The manufacturing-testing I explained for claim 4 is manufacturer-testing, because the testing to determine the cable's characteristics is carried out by the manufacturer at the factory. Ex-1005, 13:66-14:5 ("factory setup"), 14:33-40. Therefore, Ground 3 teaches this element and the rest of claim 9 for the same reasons that I previously explained above. *See* above §V.C.6.

279. For at least these reasons, Ground 3 teaches claim 9.

12. Dependent claim 10

10. The communication method of claim 9, wherein the first inbound data stream has a per-lane symbol rate in excess of 50 GBd.

280. Apart from depending from claim 9 instead of claim 4, the limitations of claim 10 also appear in claim 5 and are satisfied for the same reasons. *See* above §§V.C.7, V.B.1.

13. Independent Claim 11

[11pre] A cable manufacturing method that comprises:

281. I understand that a preamble generally does not state a claim limitation. Nonetheless, it is my opinion that Ground 3 teaches [11pre].

282. Ground 3 teaches the cable of claim 1. *See* above §V.C.3. Lugthart further teaches or suggests a method of manufacturing a cable by connecting the components of Lugthart's active cable together. Ex-1004, Figs.2A, 4A, 6:65-67, 7:66-8:7. Aronson similarly teaches manufacturing methods that involve, for example, setting equalization parameters at factory setup. Ex-1005, 13:66-14:5, 14:50-57.

283. The method taught by Ground 3 further includes the steps explained for the subsequent limitations below. For at least these reasons, Ground 1 teaches [11pre].

[11a] connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver;

284. The elements in [11a] also appear in [1a], [1c], and [1d] and are satisfied for the same reasons. *See* above §§V.C.3[1a], [1c]-[1d]. The first and second connectors in claim 1 respectively include the first and second transceivers. The transit signals output by the first and second transceivers correspond respectively to the first and second electrical transit signals. Ex-1004, 14:29-42, 15:64-16:3, Fig.4A.

285. I have also explained how Ground 3's network cable includes conductor pairs electrically connecting a first connector to a second connector (e.g., transceiver assemblies). *See* above §V.C.8[6pre]. For the same reasons, Ground 3 teaches **connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver**. For example, Lugthart teaches that "each of the transceiver assemblies...includes a transceiver." Ex-1004, 15:25-27. Lugthart further teaches that the "pair of transceivers [are] provided at respective ends of the cable" to receive signals from and provide signals to the cable; they are connected to ends of the conductor pairs within the cable, as illustrated in figure 4A. *Id.*, 6:65-67, 7:21-33, Figs.2A, 4A:

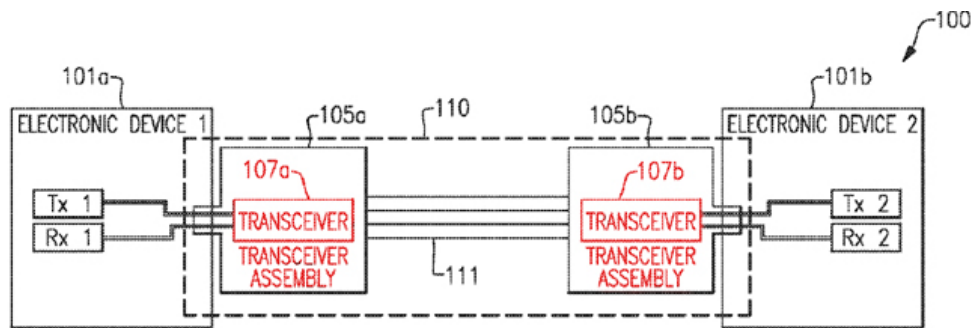


FIG. 2A

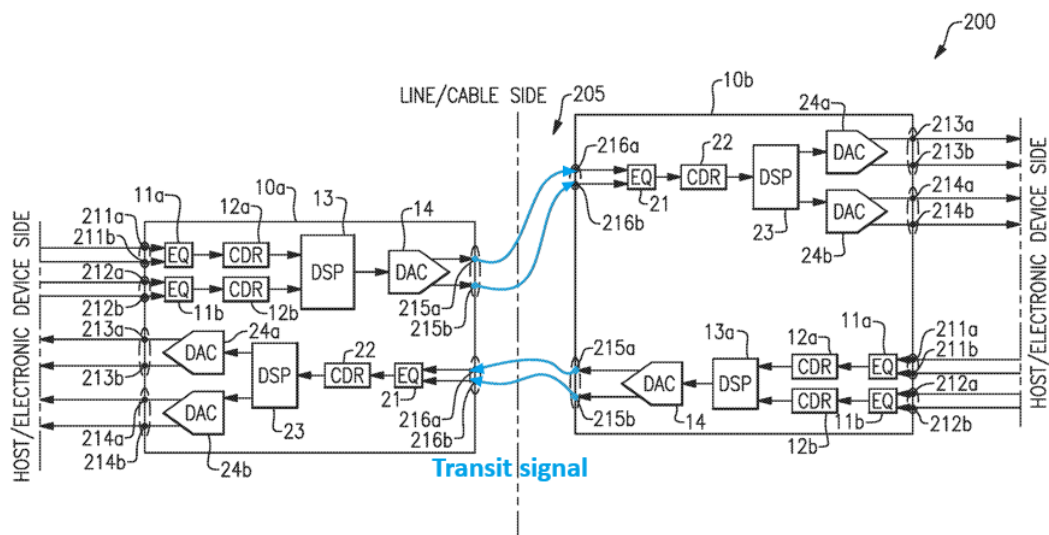


FIG. 4A

286. Lugthart teaches or suggests the connecting step because, in order for the plugs and conductors to be connected in an assembled cable (as Lugthart teaches), they would have been connected during manufacturing, when the cable components were assembled. It would have been obvious to connect Lugthart's transceivers with the ends of the conductor pairs because Lugthart teaches they are connected.

287. For at least these reasons, Ground 1 teaches [11a].

- | |
|---|
| <p>[11b] packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and</p> <p>[11c] packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device,</p> |
|---|

288. The elements in limitation [11b] and [11c] also appear in limitations [1b] and [1c], and are satisfied for the same reasons. My analyses for [1b] and [1c] explained both the first and second transceivers along with their respective signals, streams, and host devices—the first and second of each are those that correspond to the first and second connectors, respectively; Ground 1 teaches they are coupled in this way. Therefore, those apply here to limitations [11b] and [11c], which are satisfied for the same reasons explained previously. *See* above §§V.C.3[1b], [1c].

289. Lugthart also teaches **packaging** the transceivers into their respective connectors. For example, Lugthart teaches the respective transceivers are each “enclosed in a packaging”—the respective connectors (e.g., transceiver assemblies). Ex-1004, 15:25-31, 14:47-53, Fig.2A:

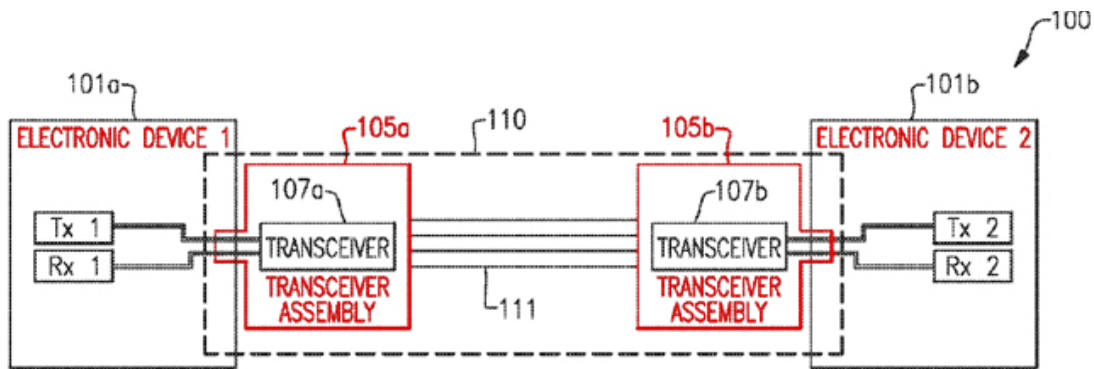


FIG. 2A

290. Because the transceivers have been packaged inside the transceiver assemblies in the assembled active cable, Lugthart teaches or suggests the step of packaging the circuitry that way. Ex-1004, 15:25-31, 14:47-53, Fig. 2A. At a minimum, it would have been obvious because, in order for the first and second transceivers to be assembled in transceiver assemblies connecting via a cable (as Lugthart teaches), they would have been packaged during manufacturing, when the cable components were assembled.

291. I have explained how Ground 3 teaches an Ethernet port (*see above* §V.C.3[1b]), which is a network interface port because Ethernet is a networking protocol and interfacing is the function of an Ethernet port.

292. For at least these reasons, Ground 1 teaches [11b] and [11c].

[11d] the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals.

293. Limitation [11d] consists of the elements set forth in limitations [1c], [1d], and [1e], and are therefore satisfied for the same reasons. Lugthart's and Aronson's teachings of respective transceivers, respective signals, and data streams that I explained for claim 1 correspond to the first and second transceivers, first and second signals, and first and second data streams as recited in limitation [11d].

294. As I previously explained, Ground 3 teaches the remodulation of the transit data stream as the outbound data stream. *See* above §§V.C.3[1d], [1e]. Such remodulation of the data stream **generates** electrical output signals conveying the remodulated data stream. More specifically, Lugthart teaches transceivers that "include outputs that generate host side receive data (RX DATA)[,]" which is "converted to an analog [output] signal by the DACs...before being transmitted to the electronic device." Ex-1004, 23:10-12, 8:8-32.

295. For at least these reasons, Ground 1 teaches [11d].

14. Dependent Claim 12

12. The cable manufacturing method of claim 11, wherein the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals.

296. I explained how Ground 3 teaches the cable manufacturing method of claim 11. *See* above §V.C.13. Ground 3 teaches claim 12, which recites overlapping elements with claim 2 that are satisfied for the same reasons explained previously. *See* above §V.C.4 (claim 2).

297. Beyond the preambles, claim 12 recites “**generating** the...electrical transit signals.” Ground 3 generates electrical transit signals by remodulating the inbound data stream for transit. *Supra* §V.C.3[1c]; *see also* §V.C.13[1d]. More specifically, Lugthart teaches that “[t]he transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX),” which is generating the electrical transit signals. Ex-1004, 8:19-22, 10:4-13.

298. Claim 12 also recites that the transceivers are “**configured** to employ” cable-dependent equalization parameters for both generating the electrical transit signals and also CDR on them, where claim 2 only requires employing them for “at least one of” the recited operations. I explained above how Ground 3 teaches both (*see* above §V.C.4 (claim 2)); as Lugthart explains, they are **configured** to do this.

Ex-1004, 22:40-49 (“The equalizer 21 can be configured to compensate for losses occurring during transmission over the cable”), 7:21-33 (“configurable” transceiver), 21:35-42 (equalizers), 22:3-16 (buffer), 22:50-57 (CDR), claim 1 (CDR circuits “configured” to retiming signals and processing signals over a cable).

299. For at least these reasons, Ground 3 teaches claim 12.

15. Dependent Claim 13

13. The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation.

300. I explained how Ground 3 teaches the cable manufacturing method of claim 12. *See* above §V.C.14; Ex-1004, 22:40-49 (teaching configuration), 7:21-33, 21:35-22:16, 22:50-57, claim 1. Ground 3 teaches claim 13, which recites overlapping elements with claim 3 that are satisfied for the same reasons. *See* above §V.C.5.

301. Beyond the preambles, claim 13 recites “the first and second transceivers are each **configured** to adapt the cable-dependent equalization parameters” as compared to “said cable-dependent equalization parameters adapt” (claim 3). I previously explained how the transceivers in Ground 3 each employ cable-dependent equalization parameters and adapt these during usage; I also explained that they are **configured** to do this. *See* above §V.C.5; §V.C.14. Lugthart explains how the transceivers are “configured” to do this. Ex-1004,

22:40-49, 7:21-33, 21:35-42, 22:3-16, 22:50-57, claim 1. Claim 13 also recites that the adaptation occurs “during **operation**” as compared to “during usage” (claim 3). When using Ground 3’s cable, the cable is in operation. Ground 3 teaches these limitations when the cable is in use/operation; that analysis applies here. *See* above §V.C.5 (claim 3). Moreover, Ground 3 teaches adaption during operation. Ex-1004, 29:39-43 (“Various implementations of the transceivers have electronic device side interfaces that are capable of adaptive operation over high loss PCB channels permitting flexibility in board and connector design for low cost solutions.”).

302. For at least these reasons, Ground 3 teaches claim 13.

16. Dependent Claim 14

14. The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters.

303. Ground 3 teaches claim 14. I explained above how Ground 3 teaches **the first and second transceivers are each configured to employ cable-dependent equalization parameters**. *See* above §V.C.14 (claim 12); §V.C.4 (claim 2). These parameters are used while the cable is in operation, when signals are being transmitted, and the transceivers retime the signals being transmitted (*see* above §§V.C.3[1b]-[1e]); Ground 3 teaches they are used **during operation**.

304. Ground 3 further teaches these equalization parameters being **presets** and **testing an assembled cable to determine the cable-dependent equalization parameters**. For example, Aronson teaches “factory set equalization” parameters. Ex-1005, 14:38-40. As explained previously, Lugthart and Aronson teach cable-dependent equalization parameters, including factory-preset parameters adjusted to match the characteristics of individual cables. *See* above §V.C.3[1e] (explaining factory-preset parameters), §V.C.4 (explaining cable-dependent parameters). Aronson teaches these presets are “adjusted at factory setup individually to match the particular length of the characteristics of the copper cabling” for each cable. Ex-1005, 13:49-14:5, 14:33-41. Therefore, Aronson tests assembled cables during manufacturing to adjust the equalization parameters to the precise characteristics of the assembled cable. *Id.* Therefore, Aronson teaches or suggests the manufacturer testing an assembled cable to determine equalization parameters adjusted for the particular cable, on a cable-by-cable basis. A POSITA would have been motivated to combine Lugthart’s and Aronson’s teachings in this manner to “reduce total link jitter” during transmission over the cable. Ex-1005, 11:32-48 This would have been appropriate for applications that demand maximum performance, high data throughput, or extended cable lengths, including for example, data centers with long cable lengths or high bitrates. And since Aronson teaches “factory set equalization” performed by the manufacturer (Ex-1005, 14:34-41), a POSITA

would have recognized that this type of individualized cable calibration would have naturally fit into test and quality assurance (QA) procedures after a cable is assembled, to ensure that it functions correctly while improving its performance. *See above §§V.C.3.[1a], [1e]* (explaining how and why Lugthart and Aronson would have been combined).

305. For at least these reasons, Ground 3 teaches claim 14.

VI. BACKGROUND AND QUALIFICATIONS

306. I am a tenured full professor of Electrical Engineering at the University of Southern California, where I have been a faculty member since 2011. As a professor, I research and teach electronic circuit and system design. My research focuses on analog mixed-signal and RF circuit architectures for data converters (both ADC and DAC), transceivers (both wireline and wireless), clock generation (such as PLL and DLL), digital VLSI, SoC, mostly-digital circuits, artificial intelligence (AI) and machine learning (ML) accelerators, analog CAD, and advanced signal processing techniques (e.g., adaptive filter, calibration, equalization, etc.) for analog circuit and systems. My research has been applied to wireline, wireless communications, computing, IoT systems, autonomous vehicles, etc. Among other subjects, I regularly teach courses such as Advanced Data Converters, Advanced Mixed Signal Integrated Circuit Design, Analog and Non-Linear Integrated Circuit Design, and Mixed Signal Integrated Circuit Design.

307. I received my B.S. degree from National Taiwan University, where I graduated as the top student in the upper division. I earned my Ph.D. and M.Sc. in Electrical Engineering and Computer Science from the University of California, Berkeley in 2006 and 2002 respectively. As a graduate student researcher at UC Berkely between 2001 and 2006, I proposed and demonstrated the asynchronous SAR ADC architecture. This architecture has been adopted in the industry for low-power high-speed analog-to-digital conversion products. The subject of my Ph.D. thesis was “High-Speed, Low-Power A/D Converter for a Low-Cost UWB Sub-sampling Radio.”

308. From 2006 to 2010, I was Analog Senior Technical Staff in the Analog IC Group of Atheros Communications (now Qualcomm Atheros), where I designed mixed-signal and RF circuits for various communication devices. In 2011, I joined the faculty of the University of Southern California, initially as an Assistant Professor of Electrical Engineering. I was promoted to the rank of Associate Professor in 2017 and became a full professor in 2021. From 2014 to 2021, I held the position of Colleen and Roberto Padovani Early Career Chair in Electrical and Computer Engineering.

309. My work has been recognized by both academic and commercial entities. I have published over 90 conference, journal, magazine articles, including multiple publications in the IEEE International Solid-State Circuits Conference

(ISSCC), IEEE Symposium on VLSI Circuits (VLSIC), IEEE Custom Integrated Circuits Conference (CICC), IEEE European Conference on Solid-State Circuit (ESSCIRC), IEEE Radio Frequency Integrated Circuits Symposium (RFIC), IEEE Journal of Solid-State Circuits (JSSC), and Transactions on Circuit and System I (TCAS-I). For example, my recent conference papers have addressed topics such as “High-Speed Digital-to-Analog Converter Design Towards High Dynamic Range,” “A 24GHz Direct Digital Transmitter Using Multiphase Subharmonic Switching PA Achieving 3.2Gbps Data Rate and -30.8dB EVM in 65nm CMOS,” and “A Millimeter-Wave Mixer-First Receiver with Non-Uniform Time-Approximation Filter Achieving >45-dB Blocker Rejection.” In 2020, the paper “A 12.8-Gbaud ADC-based Wireline Receiver with Embedded IIR Equalizer” was published as an invited paper in the IEEE Journal of Solid-State Circuits. My research has been funded by the National Science Foundation (NSF), ONR, IARPA, SRC, DARPA and various industry companies. I have also served as a technical consultant for companies including Qualcomm, Tetramem, BAE Systems and Samsung.

310. I have received recognition for my work and research. In 2024, I was honored with the grade of IEEE Fellow to recognize my technical contributions in solid-state circuit society. This grade is reserved for 0.1% of IEEE members. In 2023, I was the co-recipient of the ISSCC Jack Kilby Award for significant

advances in analog mixed-signal circuits. In 2022, I was a co-recipient for the RFIC 2022 Best Student Paper Award for my work with students in my laboratory on a circuit prototype. From 2021 to 2023, I was the IEEE Solid-State Circuit Society (SSCS) Distinguished Lecturer. I have been invited to offer seminars, workshops, keynote talks, and panel discussions in major IEEE conferences, IEEE SSCS chapters, and universities on a range of topics covering fundamental to advanced integrated circuit design and how to improve the performance and/or reduce cost of a circuit or system. In 2019, I was also the recipient of Qualcomm Faculty Award, and in 2014 both the NSF Faculty Early Career Development (CAREER) Award and DARPA Young Faculty Award (YFA). As a student, I was the recipient of a UC Regents' Fellowship at Berkeley in 2000 and the Analog Devices Outstanding Student Award for IC design in 2006.

311. I have extensive experience and familiarity with integrated circuit (IC) design for wireline communication as well as relevant signal processing techniques for such communication systems. As a principal investigator, I have conducted various research projects innovating and prototyping the most critical circuit blocks of wireline transceivers. I have also served in various review panels (e.g., NSF panels, IEEE conferences and journals), reviewing research papers related to wireline or serial link or SerDes circuit, system and signal processing techniques. Lastly, I have been teaching various circuit courses at USC. I teach my students a

wide range of circuit and signal processing techniques related to this wireline area, so that they learn how those circuit components can be designed and implemented.

A. Compensation

312. For my efforts in connection with the preparation of this declaration I have been compensated at my standard rate for this type of consulting activity. My compensation is in no way contingent on the results of these or any other proceedings relating to the above-captioned patent.

B. Materials and Other Information Considered

313. I have considered information from various sources in forming my opinions. I have reviewed and considered each of the exhibits listed in the attached Appendix 2 (Materials Considered in the Preparation of This Declaration) in forming my opinions.

VII. UNDERSTANDING OF THE LAW

314. I am not an attorney. In forming my opinions in this Declaration, I applied the relevant legal principles provided to me by counsel, which are summarized in Appendix 4.

VIII. RESERVATION OF RIGHTS

315. My opinions are based upon the information that I have considered to date. I am unaware of any evidence of secondary considerations with respect to the '252 Patent that would render any of the challenged claims non-obvious. I reserve the right, however, to supplement my opinions in the future to respond to any

arguments raised by the owner of the '252 Patent and to take into account new information that becomes available to me.

316. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on 8 / 7, 2025.

By:

A handwritten signature in black ink, appearing to read 'Michael S. Chen', written over a horizontal line.

Michael S. Chen

APPENDIX 1: CURRICULUM VITAE OF MICHAEL SHUO-WEI CHEN

Mike Shuo-Wei Chen

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Email: shuowei@gmail.com (Alt: swchen@usc.edu)
Phone: 510-517-0052

Curriculum Vitae

EDUCATION

University of California, Berkeley 2002 – 2006

- PhD in Electrical Engineering and Computer Science
- Dissertation: “High-Speed, Low-Power A/D Converter for a Low-Cost UWB Sub-sampling Radio”
- Advisor: Robert W. Brodersen

University of California, Berkeley 2000 – 2002

- Master of Science in Electrical Engineering and Computer Science
- Thesis: “Ultra Wideband Baseband Design and Implementation”

National Taiwan University 1994 – 1998

- Bachelor of Science in Electrical Engineering
- Top 1 student for upper division

ACADEMIC EXPERIENCE

- Full Professor, Department of Electrical Engineering, University of Southern California, 2021 – Present.
- Associate Professor, Department of Electrical Engineering, University of Southern California, 2017 – 2021.
- Colleen and Roberto Padovani Early Career Chair, USC, 2014 – 2021
- Assistant Professor, Department of Electrical Engineering, University of Southern California, 2011 – 2017.
- Graduate Student Researcher, Berkeley Wireless Research Center, Berkeley, CA, 2001 – 2006.

WORK EXPERIENCE

- Analog Senior Technical Staff, Atheros Communications, Santa Clara, CA, 2006–2010.
-Designed RF, analog mixed-signal circuits for various wireless products

CONSULTING EXPERIENCE

- Legal Consulting
(2019-2022): Xilinx-ADI litigation

Legal consultant, working with counsels to prepare/review legal documents, non-infringement arguments, deposition, source codes, PTAB, etc.

(2023-Present): Aptiv-Microchip

Legal expert, working with counsel on IPR expert declaration, source code review for litigation, etc.

(2023-2024): ARM-Qualcomm litigation

Legal expert, working on source code review, expert report, and deposition, testifying expert during trial

(2025-Present): Apple-Vampire Labs

Legal expert, IPR

(2025-Present): BOE – Samsung

Legal expert, IPR

(2025-Present): Marvell – Credo

This matter

(2025-Present): Renesas-Monterey Research

Legal expert, patent re-examination

- Technical Consulting:
Qualcomm, Samsung, BAE system, Tetramem → Provide technical advices on various electronic projects for the client.

HONORS and AWARDS

- IEEE Fellow 2024
- ISSCC 2022 Jack Kilby Award (co-recipient)
- RFIC 2022 Best Student Paper Award – First Place (co-recipient)
- IEEE Solid-State Circuit Society (SSCS) Distinguished Lecturer 2021-2023.
- Qualcomm Faculty Award, 2019.
- DARPA Young Faculty Award (YFA), 2014.
- NSF Faculty Early Career Development (CAREER) Award, 2014.
- Analog Devices Outstanding Student Award, 2006
- UC Regents Fellowship, UC Berkeley, 2000
- Lin's Foundation Award for Top 1 engineering college student over the academic year, 1996-1997
- Presidential Awards, National Taiwan University, 1996-1998
- Member of National Mathematics Team of Taiwan, awarded with Honourable Mention in Asian Pacific Mathematics Olympiad, 1994.

AREA OF INTEREST

I worked on various Analog Mixed-Signal, VLSI, SoC and RF circuit architectures/techniques, covering a wide range of topics/areas in academia and industry, including

- Data Converters (e.g. ADC and DAC)
- RF/mm-Wave Wireless Communications (e.g. WiFi, 5G/6G, Bluetooth, GPS, etc.)

- I/O, Wireline Communications (e.g. SerDes, CDR, Clock generation)
- Computing (e.g. AI/ML accelerators, neuromorphic processor)
- Design Methodology (AI-ML assisted CAD).
- Digital VLSI, SOC, RTL
- Analog Mixed-Signal Circuit
- Power management circuit

PUBLICATIONS

Conferences

1. S. Mahapatra, M. Ayes, C. Yang, M. Palaria, S. Su, A. Zhang, **M. S.-W. Chen**, “A 24GHz Direct Digital Transmitter Using Multiphase Subharmonic Switching PA Achieving 3.2Gbps Data Rate and -30.8dB EVM in 65nm CMOS“, IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2025.
2. C. Yang, S. Su, M. Ayes, S. Mahapatra, M. Hamada, V. Chenna, H. Hashemi, **M. S.-W. Chen**, “A Blocker Tolerant Receiver with VCO-based Non-Uniform Multi-Level Time-Approximation Filter With -36dB EVM in 28nm CMOS“, IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2025. (to be presented)
3. J. Liu, A. Shabra, S. Ho, G. Manganaro, **M. S.-W. Chen**, “A 16GS/s 10b Time-domain ADC using Pipelined-SAR TDC with Delay Variability Compensation and Background Calibration Achieving 153.8dB FoM in 4nm CMOS” in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technol. Circuits)*, June 2024.
4. Q. Zhang*, S. Su*, B. R. Biswas, S. Gupta, **M. S.-W. Chen**, “Synthesizable 10-bit Stochastic TDC Using Common-Mode Time Dithering and Passive Approximate Adder With 0.012mm² Active Area in 12nm FinFET,” in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technol. Circuits)*, June 2024. (* equal contribution)
5. Q. Zhang*, S. Su*, Z. Liu*, H.-C. Cheng, Z. Qiu, M. Palaria, J. Ye, D. Meng, B. Chen, S. Hossain, W. Wu, **M. S.-W. Chen**, “A Stochastic Analog SAT Solver in 65nm CMOS Achieving 6.6 μ s Average Solution Time with 100% Solvability for Hard 3-SAT Problems,” in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technol. Circuits)*, June 2024. (* equal contribution)
6. M. Ayes, S. Mahapatra, C. Yang and **M. S.-W. Chen**, “A 0.072-mm² 18-21GHz Non-Uniform Sub-Sampling Receiver with a Non-Uniform Discrete-Time FIR Filter Achieving 42dB Blocker Rejection in 28nm CMOS“, *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2024.
7. M. Palaria, S. Su, H.-C. Cheng, R. Rasul, Q. Zhang, S. Mahapatra, C.-F. Law, S. Hossain, R. Bena, W. Wu, Q. Nguyen, M. S.-W. Chen, “Analog Kalman Filter with Integration and Digitization via a Shared Thyristor-Based VCO for Sensor Fusion in 65 nm CMOS“, in *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2023.
8. H.-C. Cheng, S. Su, M. Palaria, Q. Zhang, C. Yang, S. Hossain, R. Bena, B. Chen, Z. Liu, J. Liu, R. Rasul, Q. Nguyen, W. Wu, **M. S.-W. Chen**, “A

- Memristor-Based Analog Accelerator for Solving Quadratic Programming problems,” in IEEE Custom Integrated Circuits Conference (CICC), April 2023.
9. S. Su*, Q. Zhang*, and **M. S.-W. Chen**, “A 2GS/s 8.5-Bit Time-Based ADC Using a Segmented Stochastic Flash TDC,” in 2023 IEEE Custom Integrated Circuits Conference (CICC), Apr. 2023 (* equal contribution)
 10. Q. Zhang, H.-C. Cheng, S. Su, and **M. S.-W. Chen**, “A Fractional-N Digital MDLL with Injection Error Scrambling and Background Third-Order DTC Delay Equalizer Achieving -67dBc Fractional Spur,” in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2023.
 11. Q. Zhang*, S. Su*, and **M. S.-W. Chen**, “A Cost-Efficient Fully Synthesizable Stochastic Time-to-Digital Converter Design Based on Integral Nonlinearity Scrambling,” in 2022 59th ACM/EDAC/IEEE Design Automation Conference (DAC), July 2022. (*contributed equally to this work)
 12. C. Yang, S. Su and **Mike Chen**, “A Millimeter-Wave Mixer-First Receiver with Non-Uniform Time-Approximation Filter Achieving $>45\text{-dB}$ Blocker Rejection,” in IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2022. (Best Student Paper Award – First Place)
 13. S. Su, and **M. S.-W. Chen**, “High-Speed Digital-to-Analog Converter Design Towards High Dynamic Range,” (invited paper) *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2022.
 14. J. Liu, M. Hassanpourghadi, and **M. S.-W. Chen**, “A 10GS/s 8b 25fJ/c-s 2850um² Two-Step Time-domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology“, *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2022.
 15. S. Su, Q. Zhang, M. Hassanpourghadi, J. Liu, R.A. Rasul, and **M. S.-W. Chen**, “Analog/Mixed-Signal Circuit Synthesis Enabled by the Advancements of Circuit Architectures and Machine Learning Algorithms,” (invited paper) *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022.
 16. S. Su, Q. Zhang, J. Liu, M. Hassanpourghadi, R.A. Rasul, and **M. S.-W. Chen**, “TAFA: Design Automation of Analog Mixed-Signal FIR Filters Using Time Approximation Architecture,” *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022.
 17. J. Liu, S. Su, M. Madhusudan, M. Hassanpourghadi, S. Saunders, Q. Zhang, R. Rasul, Y. Li, J. Hu, A. Kumar, S. S. Sapatnekar, R. Harjani, A. Levi, S. Gupta and **M. S.-W. Chen**, “From Specification to Silicon: Towards Analog/Mixed-Signal Design Automation using Surrogate NN Models with Transfer Learning“, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2021.
 18. M. Hassanpourghadi, S. Su, R.A. Rasul, J. Liu, Q. Zhang, and **M. S.-W. Chen**, “Circuit Connectivity Inspired Neural Network for Analog Mixed-Signal Functional Modeling,” *58th ACM/EDAC/IEEE Design Automation Conference (DAC)*, Dec. 2021.(to appear)
 19. R.A. Rasul, and **M. S.-W. Chen**, “A 128×128 SRAM Macro with Embedded Matrix-Vector Multiplication Exploiting Passive Gain via MOS Capacitor for Machine Learning Application,” *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2021.
 20. A. Zhang, M. Ayesh, S. Mahapatra, and **M. S.-W. Chen**, “A 24-28 GHz Concurrent Harmonic and Subharmonic Tuning Class E/F_{2,2/3} Subharmonic

- Switching Power Amplifier Achieving Peak/PBO Efficiency Enhancement,” *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2021.
21. Q. Zhang, S. Su, C.-R. Ho, and **M. S.-W. Chen**, “A Fractional-N Digital MDLL with Background Two-Point DTC Calibration Achieving -60dBc Fractional Spur,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2021.
 22. A. Zhang, C. Yang, M. Ayesh, and **M. S.-W. Chen**, “A 5-6 GHz Current-Mode Subharmonic Switching Digital Power Amplifier for Enhancing Power Back-off Efficiency,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2021.
 23. Q. Zhang, S. Su, J. Liu and **M. S.-W. Chen**, “CEPA: CNN-based Early Performance Assertion Scheme for Analog and Mixed-Signal Circuit Simulation,” in *2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2020.
 24. J. Liu, M. Hassanpourghadi, Q. Zhang, S. Su and **M.S.-W. Chen**, “Transfer Learning with Bayesian Optimization-Aided Sampling for Efficient AMS Circuit Modeling,” in *2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2020.
 25. C. Yang, M. Ayesh, A Zhang, T.F. Wu, **M. S.-W. Chen**, “A 29-mW 26.88-GHz Non-Uniform Sub-Sampling Receiver Front-End Enabling Spectral Alias Spreading,” *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June, 2020.
 26. S. Su and **M. S.-W. Chen**, “A SAW-Less Direct-Digital RF Modulator with Tri-Level Time-Approximation Filter and Reconfigurable Dual-Band Delta-Sigma Modulation,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2020.
 27. T.-F. Wu and **M. S.-W. Chen**, “A 40MHz-BW 76.2dB/78.0dB SNDR/DR noise-shaping nonuniform sampling ADC with single phase-domain level crossing and embedded nonuniform digital signal processor in 28nm CMOS,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2020.
 28. S. Su and **M. S-W Chen**, “A 1–5GHz Direct-Digital RF Modulator with an Embedded Time-Approximation Filter Achieving -43dB EVM at 1024 QAM,” *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, June 2019.
 29. J.W. Nam, **M.S-W Chen**, “A 12.8-Gbaud ADC-based NRZ/PAM4 Receiver with Embedded Tunable IIR Equalization Filter Achieving 2.43-pJ/b in 65nm CMOS,” *IEEE Custom Integrated Circuits Conference (CICC)*, April 2019.
 30. M. Hassanpourghadi, **M.S-W Chen**, “A 2-way 7.3-bit 10 GS/s Time-based Folding ADC with Passive Pulse-Shrinking Cells,” *IEEE Custom Integrated Circuits Conference (CICC)*, April 2019.
 31. A. Zhang and **M. S-W Chen**, “A Watt-Level Phase-Interleaved Multi-Subharmonic Switching Digital Power Amplifier Achieving 31.4% Average Drain Efficiency,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2019.
 32. A. Zhang, **M. S-W Chen**, “A Sub-Harmonic Switching Digital Power Amplifier with Hybrid Class-G Operation for Enhancing Power Back-off Efficiency,” *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, 2018.

33. T.F. Wu, **M. S-W Chen**, "A 200MHz-BW 0.13mm² 62dB-DR VCO-Based Non-Uniform Sampling ADC with Phase-Domain Level Crossing in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, 2018.
34. S. Su and **M. S-W Chen**, "A 16-bit 12GS/s Single/Dual-Rate DAC with Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 within DC to 6GHz Tunable Passbands," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.
35. C.R. Ho, **M. S-W Chen**, "A digital frequency synthesizer with dither-assisted pulling mitigation for simultaneous DCO and reference path coupling," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.
36. C.R. Ho, **M. S-W Chen**, "A fractional-N digital PLL with background dither noise cancellation loop achieving <-62.5dBc worst-case near-carrier fractional spur in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.
37. R. Rasul, P. Teimouri, and **M. S-W Chen**, "A Time Multiplexed Network Architecture for Large-Scale Neuromorphic Computing," *IEEE MWSCAS*, August 2017.
38. C.R. Ho, **M. S-W Chen**, "Interference-Induced DCO Spur Mitigation for Digital Phase Locked Loop in 65-nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2016.
39. J.W. Nam, M. Hassanpourghadi, A. Zhang, **M.S-W Chen**, "A 12-bit 1.6 GS/s Interleaved SAR ADC with Dual Reference Shifting and Interpolation Achieving 17.8 fJ/conv-step in 65nm CMOS," *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, June 2016.
40. C.R. Ho, **M. S-W Chen**, "A Digital PLL with Feedforward Multi-Tone Spur Cancellation Loop Achieving <-73dBc Fractional Spur and <-110dBc Reference Spur in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2016.
41. S. Su, **M. S-W. Chen**, "A 12b 2GS/s Dual-Rate Hybrid DAC with Pulsed Timing-Error Pre-Distortion and In-Band Noise Cancellation Achieving >74dBc SFDR up to 1GHz in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2016.
42. T.F. Wu, C.R. Ho, **M. S.-W. Chen**, "A Flash-Based Non-Uniform Sampling ADC Enabling Digital Anti-Aliasing Filter in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep 2015.
43. S. Su, T. Tsai, P. Sharma, **M. S.-W. Chen**, "A 12-bit Hybrid DAC with 8GS/s Unrolled Pipeline Delta-Sigma Modulator achieving >75dB SFDR over 500MHz in 65nm CMOS," *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, June 2014.
44. C.R. Ho, **M. S.-W. Chen**, "A Fractional-N DPLL with Adaptive Spur Cancellation and Calibration-Free Injection-Locked TDC in 65nm CMOS," to be presented at *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June, 2014.
45. J.W. Nam, D. Chiong, and **M. S.W. Chen**, "A 95-MS/s 11-bit 1.36-mW Asynchronous SAR ADC with Embedded Passive Gain in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2013

46. P.K. Sharma, and **M. S.W. Chen**, "A 6b 800MS/s 3.62mW Nyquist AC-coupled VCO Based ADC in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2013
47. **M. S.W. Chen**, "Trend of High-Speed SAR ADC towards RF Sampling," *10th International Conference on Sampling Theory & Applications (SampTA)* (Invited), July. 2013.
48. D. Hand, and **M. S.W. Chen**, "A Non-Uniform Sampling ADC Architecture with Embedded Alias-Free Asynchronous Filter," *Global Telecommunications Conference (GLOBECOM)*, Dec. 2012.
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INVITED TALKS/TUTORIALS/WORKSHOPS

1. ITRI, Taiwan, “New Opportunities in Mixed-Signal ICs”, June, 2011.
2. UMC, Taiwan, “New Opportunities in Mixed-Signal ICs”, June, 2011.
3. HRL Laboratories, LLC: “Enhancing A-to-D Conversion Efficiency”. July 2nd, 2012
4. “Analog-to-Digital Interface: A Time Approach” 2013 CMOS Emerging Technologies Research Symposium, Whistler, July 2013.
5. “Path towards High-Speed High-Resolution Data Converters with Diminishing Cost”, Sep. 2013, Broadcom.
6. “Analog-Digital Interface Research, really?” Sep. 2013, Qualcomm-Atheros.
7. “Re-shape Future Mixed-Signal IC Design” Oct. 2013. Qualcomm.
8. “Path towards High-Speed High-Resolution Data Converters with Diminishing Cost”, Nov. 2013, UT Dallas.
9. “Path towards High-Speed High-Resolution Data Converters with Diminishing Cost”, Nov. 2013, Texas Instrument.
10. “Power efficient ADC Topologies towards RF Sampling” 2014 RFIC Tutorial.
11. “Path Towards Direct RF Synthesis: A Hybrid Digital-to-Analog Converter Architecture” 2014 IEEE MWSCAS Conference, Distinguished Speaker Series.
12. “Asynchronous SAR ADC: Past, Present and Beyond” 2014 IEEE MWSCAS Conference Tutorial
13. “Exploring Limits of Mixed-Signal ICs” Sep. 2014, MaxLinear Corp.
14. “Rethinking Analog-Digital Interface Circuit Architectures” Oct. 2014, IC Seminar, Columbia University, NY.
15. “Rethinking Analog-Digital Interface Circuit Architectures” Mar. 2015, IC Seminar, UC Berkeley, CA.
16. “Rethinking Analog-Digital Interface Circuit Architectures” Dec. 2015, IC Seminar, National Taiwan University(NTU)/IEEE Chapter, Taipei, Taiwan.
17. “Rethinking Analog-Digital Interface Circuit Architectures” Feb. 2016, IC Seminar, UT Austin, Texas.
18. “Asynchronous SAR ADC: Past, Present and Beyond”, Feb. 2016, EE department Colloquium, UT Austin/IEEE Chapter.
19. “Rethinking Analog-Digital Interface Circuit Architectures” Feb. 2016, IC Seminar, University of Michigan, Ann Arbor.
20. “Rethinking Analog-Digital Boundary from Circuit to System Level towards Reconfigurability of Everything” Mar. 2016, SystemX Seminar, Stanford

21. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, EE department Colloquium. Carnegie Mellon University (CMU).
22. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, IC Seminar, University of California, Los Angeles (UCLA).
23. "IC Research overview," TSMC, 2017
24. "IC Research overview," Intel Lab, 2017
25. "IC Research overview," InPhi, 2017
26. "Advancing Low-Power High-Speed Analog-to-Digital Converters: An Asynchronous Design Approach", VLSI DAT tutorial, 2017
27. "Generic spur cancellation for digital PLL," Qualcomm 2017
28. "Evolutions of SAR ADC: from High Resolution to High Speed Regime," IEEE CICC 2018 tutorial.
29. "Emerging Opportunities in Analog Mixed-Signal Circuit Design Automation," ACM/IEEE ICCAD 2018 workshop.
30. "Analog-to-Digital Converter Architecture Opportunities in Emerging Wireless Systems," RFIC 2018 workshop
31. "How can hardware designers reclaim the spotlight?" moderator/co-organizer of ISSCC 2019 evening panel.
32. "Fundamentals of Analog-to-digital conversion," 2-day tutorial in Shanghai, China 2019.
33. "Digital Fractional-N Phase Locked Loop Design," tutorial, ISSCC Feb 2020
34. "Digital Fractional-N Phase Locked Loop Design," ISSCCedu Feb 2020
35. "Low Spur PLL architectures," MEAD tutorial in EPFL, 2021 (to appear)
36. "Low Spur PLL architectures and techniques," IEEE CICC 2020
37. "New Opportunities in Nonuniform Sampling," IEEE SSCS Webinar Oct 2020.
38. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IESD Keynote June 2021
39. "ADC Evolution via Architectural Rethinking: from Asynchronous SAR to Non-uniform Sampling ADC," IEEE SSCS Tainan Chapter, Oct 2021
40. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IEEE SSCS Atlanta Chapter, Nov. 2021
41. "Asynchronous SAR ADC: Past, Present and Beyond," IEEE Southern Alberta Chapter, Nov. 2021
42. "Non-Uniform Sampling Data Converters: A Journey to Uncharted Circuits and Systems" IEEE VLSI-DAT April 2022
43. "Asynchronous SAR ADC: Past, Present and Beyond," IEEE Swiss Chapter, May 2022
44. "New Opportunities in Nonuniform Sampling," IEEE Penang Chapter, July 2022
45. "Trend in Digital PLL Design and New Opportunities in Spur Cancellation," IEEE Southern Alberta Chapter, Sep. 2022
46. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IEEE Egypt Chapter Nov. 2022
47. "New Opportunities in Nonuniform Sampling," IEEE Taipei Chapter, Dec. 2022
48. "Trend in Digital PLL Design and New Opportunities in Spur Cancellation," IEEE Tainan Chapter, Dec. 2022

PROFESSIONAL SERVICES

Review Panel:

1. IEEE SSCS James D. Meindl Innovators Award
2. NSF Panelist
3. Samsung Research

Journal article review:

1. IEEE Journal of Solid-State Circuits
2. IEEE Solid-State Circuits Letters (SSC-L)
3. IEEE Transactions on Signal Processing
4. IEEE Transactions on Communications
5. IEEE Transactions on Circuits and Systems I
6. IEEE Transactions on Circuits and Systems II
7. IEEE Transactions on Vehicular Technology
8. IEEE Communications Letters
9. Journal of VLSI Signal Processing Systems

USC Department Services:

1. Munishian Series Committee
2. EFC
3. EE Festival reviewer

Conference TPC:

IEEE European Conference on Solid-State Circuits (ESSCIRC) (2022- present)
IEEE International Solid State Circuits Conference (ISSCC) (2018 - present)
IEEE Symposium on VLSI Circuits (VLSIC) (2017 - 2020)
IEEE Custom Integrated Circuits Conference (CICC) (2015 - 2019)
IEEE GlobalSIP (2014)

Organized/Participated Panel/Forum/Workshops for SSCS:

1. Forum: “Emerging Design Techniques for Data Converters” served as organizer at CICC 2017
2. Panel: “What can/should Circuit Designers do to Ride on the Wave of Machine Learning?” served as co-organizer and moderator at CICC 2018
3. Panel: “How can hardware designers reclaim the spotlight?” served as co-organizer and moderator at ISSCC 2019
4. Panel: “Favorite circuit design and testing mistakes of starting engineers?” served as co-organizer at ISSCC 2021
5. VLSI Symposia Mentoring Event June 2021
6. Panel: “How to choose career path, academia, industry, startups?” served as panelist at CICC 2022 (to appear)
7. Panel: “Open Source Systems, Circuits, and Design: Is It the Future?” served as panelist at CICC 2022 (to appear)

Associate Editor:

SSC-L, TCAS-II

Society Membership:
IEEE Fellow

APPENDIX 2: MATERIALS CONSIDERED IN THE PREPARATION OF THIS DECLARATION

Exhibit No.	Description
1001	U.S. Patent No. 11,012,252 to Lam and Chen (“the ’252 patent”)
1002	Certified Prosecution File History for the ’252 Patent (“Prosecution History”)
1004	U.S. Patent No. 9,882,706 to Lugthart, et al. (“Lugthart”)
1005	U.S. Patent No. 7,445,389 to Aronson (“Aronson”)
1006	U.S. Patent No. 8,516,238 to Cornelius, et al. (“Cornelius”)
1007	Samaan, High-speed Serial Bus Repeater Primer (“Samaan”)
1008	Ars Technica, Why Thunderbolt cables will be expensive until 2013 (Library of Congress Capture)
1009	Intersil, ISL37231 [Datasheet]
1010	U.S. Patent Application Publication No. 2019/0028262 A1 to Kobayashi, et al. (“Kobayashi”)
1011	TE Connectivity, SFP+ High Speed Copper Cable Assemblies
1012	Cisco, Cisco 40GBASE QSFP Modules Data Sheet (Internet Archive Capture)
1013	AppleInsider, Intel details Thunderbolt, says Apple has full year head start (Internet Archive Capture)
1014	macstories, Intel: Apple Transferring Thunderbolt Trademark To Us (Internet Archive Capture)
1015	AnandTech, Intel’s Codename Light Peak Launches as Thunderbolt (Internet Archive Capture)
1016	Ars Technica, The technology inside Apple’s \$50 Thunderbolt cable (Internet Archive Capture)
1017	Gasca, et al., CMOS Continuous-Time Adaptive Equalizers for High-Speed Serial Links
1018	Declaration of June Munford re: Samaan
1019	Excerpts from 10G SFP+ Video
1020	Excerpts from Stauffer, High Speed Serdes Devices and Applications (“Stauffer”)
1021	U.S. Patent No. 7,233,617 to Gorecki (“Gorecki”)
1022	<i>Certain Active Electrical Cables and Components Thereof</i> , ITC Investigation 337-TA-1446, Exhibit 38 to Complaint, Credo’s Infringement Claim Chart Showing Molex’s Infringement of the ’252 Patent

Exhibit No.	Description
1023	<i>Certain Active Electrical Cables and Components Thereof</i> , ITC Investigation 337-TA-1446, Exhibit 41 to Complaint, Credo's Infringement Claim Chart Showing TE Connectivity's Infringement of the '252 Patent
1024	<i>Certain Active Electrical Cables and Components Thereof</i> , ITC Investigation 337-TA-1446, Exhibit 66 to Complaint, Credo's Domestic Industry Claim Chart for the '252 Patent
1025	SFF-8431 Rev 4.1 + Addendum
1026	Texas Instruments Technical Article, How to Reduce Jitter and Improve Signal Integrity in Source and Sink System Designs Supporting HDMI 2.0
1027	Intel, Thunderbolt™ Networking Bridging and Routing Instructional White Paper
1028	Intel, PCI Express Ethernet Networking White Paper
1029	U.S. Patent No. 9,231,846 to Sinha, et al. ("Sinha")
1030	Excerpts from Prosecution File History of CN2019101555359 to Thermo Scientific Co. Ltd. (Chinese counterpart application to the '252 Patent)
1031	U.S. Patent No. 8,787,430 to Rhagavan, et al. ("Raghavan")
1032	Internet Archive Declaration of Mina Ching re SFF-8636 Rev 1.7
1033	Intel, PCI Express Architecture
1034	Internet Archive Capture, The Wayback Machine, Wikipedia, "PCI Express"
1035	Intel Website Search Results

APPENDIX 3: CHALLENGED CLAIMS

[1pre] An active Ethernet cable that comprises:

[1a] electrical conductors connected between a first connector and a second connector,

[1b] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,

[1c] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,

[1d] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, and

[1e] the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as

the outbound data stream, and the clock and data recovery performed on the electrical input signal.

2. The active Ethernet cable of claim 1, wherein the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal.

3. The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters adapt during usage of the Ethernet cable.

4. The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable.

5. The active Ethernet cable of claim 4, wherein the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd.

[6pre] A communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector:

[6a] receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device;

[6b] performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream;

[6c] re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs;

[6d] receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device;

[6e] performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream;

6[f] re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs;

[6g] performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream;

6[h] re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device;

[6i] performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream; and

[6j] re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device,

[6k] wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.

7. The communication method of claim 6, wherein cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said performing clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.

8. The communication method of claim 7, wherein said cable-dependent equalization parameters are adaptively updated.

9. The communication method of claim 7, wherein said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable.

10. The communication method of claim 9, wherein the first inbound data stream has a per-lane symbol rate in excess of 50 GBd.

[11pre] A cable manufacturing method that comprises:

[11a] connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver;

[11b] packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and

[11c] packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device,

[11d] the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams,

configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals.

12. The cable manufacturing method of claim 11, wherein the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals.

13. The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation.

14. The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters.

APPENDIX 4: UNDERSTANDING OF THE LAW

I have applied the following legal principles provided to me by counsel in arriving at the opinions set forth in this report.

Legal Standard for Prior Art

I am not an attorney. I have been informed by attorneys of the relevant legal principles and have applied them to arrive at the opinions set forth in this declaration.

I understand that the petitioner for inter partes review may request the cancelation of one or more claims of a patent based on grounds available under 35 U.S.C. § 102 and 35 U.S.C. § 103 using prior art that consists of patents and printed publications.

Anticipation and Prior Art

I understand that § 102 specifies when a challenged claim is invalid for lacking novelty over the prior art, and that this concept is also known as “anticipation.” I understand that a prior art reference anticipates a challenged claim, and thus renders it invalid by anticipation, if all elements of the challenged claim are disclosed in the prior art reference. I understand the disclosure in the prior art reference can be either explicit or inherent, meaning it is necessarily present or implied. I understand that the prior art reference does not have to use the same words as the challenged claim, but all of the requirements of the claim

must be disclosed so that a person of ordinary skill in the art could make and use the claimed subject-matter.

In addition, I understand that § 102 also defines what is available for use as a prior art reference to a challenged claim.

Under § 102(a)(1), a challenged claim is anticipated if it was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the challenged claimed invention.

Under § 102(a)(2), a challenged claim is anticipated if it was described in an issued patent, or in an application for patent that was published by the USPTO, in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the challenged claimed invention.

I understand that the filing date of a patent is generally the filing date of the application filed in the United States that issued as the patent. However, I understand that a patent may be granted an earlier effective filing date if the patent owner properly claimed priority to an earlier patent application.

I understand that when a challenged claim covers several structures, either generically or as alternatives, the claim is deemed anticipated if any of the structures within the scope of the claim is found in the prior art reference.

I understand that when a challenged claim requires selection of an element from a list of alternatives, the prior art teaches the element if one of the alternatives is taught by the prior art.

Legal Standard for Obviousness

I understand that even if a challenged claim is not anticipated, it is still invalid if the differences between the claimed subject matter and the prior art are such that the claimed subject matter would have been obvious to a person of ordinary skill in the pertinent art at the time the alleged invention.

I understand that obviousness must be determined with respect to the challenged claim as a whole.

I understand that one cannot rely on hindsight in deciding whether a claim is obvious.

I also understand that an obviousness analysis includes the consideration of factors such as (1) the scope and content of the prior art, (2) the differences between the prior art and the challenged claim, (3) the level of ordinary skill in the pertinent art, and (4) “secondary” or “objective” evidence of non-obviousness.

Secondary or objective evidence of non-obviousness includes evidence of: (1) a long felt but unmet need in the prior art that was satisfied by the claimed invention; (2) commercial success or the lack of commercial success of the claimed invention; (3) unexpected results achieved by the claimed invention; (4)

praise of the claimed invention by others skilled in the art; (5) taking of licenses under the patent by others; (6) deliberate copying of the claimed invention; and (7) contemporaneous and independent invention by others. However, I understand that there must be a relationship between any secondary evidence of non-obviousness and the claimed invention.

I understand that a challenged claim can be invalid for obviousness over a combination of prior art references if a reason existed (at the time of the alleged invention) that would have prompted a person of ordinary skill in the art to combine elements of the prior art in the manner required by the challenged claim. I understand that this requirement is also referred to as a “motivation to combine,” “suggestion to combine,” or “reason to combine,” and that there are several rationales that meet this requirement.

I understand that the prior art references themselves may provide a motivation to combine, but other times simple common sense can link two or more prior art references. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may come from market forces.

I understand obviousness to include, for instance, scenarios where known techniques are simply applied to other devices, systems, or processes to improve them in an expected or known way. I also understand that practical and common-

sense considerations should be applied in a proper obviousness analysis. For instance, familiar items may have obvious uses beyond their primary purposes.

I understand that the combination of familiar elements according to known methods is obvious when it yields predictable results. For instance, obviousness bars patentability of a predictable variation of a technique even if the technique originated in another field of endeavor. This is because design incentives and other market forces can prompt variations of it, and predictable variations are not the product of innovation, but rather ordinary skill and common sense.

I understand that a particular combination may be obvious if it was obvious to try the combination. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. This would result in something obvious because the result is the product not of innovation but of ordinary skill and common sense. However, I understand that it may not be obvious to try a combination when it involves unpredictable technologies.

It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, I understand that any need or problem known in the field of

endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

It is my understanding that the Manual of Patent Examining Procedure §2143 sets forth the following as exemplary rationales that support a conclusion of obviousness:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- Choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;

- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

A person of ordinary skill in the art looking to overcome a problem will often use the teachings of multiple publications together like pieces of a puzzle, even though the prior art does not necessarily fit perfectly together. Therefore, I understand that references for obviousness need not fit perfectly together like puzzle pieces. Instead, I understand that obviousness analysis takes into account inferences, creative steps, common sense, and practical logic and applications that a person of ordinary skill in the art would employ under the circumstances.

I understand that a claim can be obvious in light of a single reference, if the elements of the challenged claim that are not explicitly or inherently disclosed in the reference can be supplied by the common sense of one of skill in the art.

I understand that obviousness also bars the patentability of applying known or obvious design choices to the prior art. One cannot patent merely substituting one prior art element for another if the substitution can be made with predictable results. Likewise, combining prior art techniques that are interoperable with respect to one another is generally obvious and not patentable.

In order for a claim to be found invalid based upon a modification or combination of the prior art, there must be reasonable expectation that a person of ordinary skill would have successfully modified or combined the prior art to arrive at the claimed arrangement. This does not mean that it must be certain that a person of ordinary skill would have been successful—the law only requires that the person of ordinary skill in the art would have perceived a reasonable expectation of success in modifying or combining the prior art to arrive at the claimed invention.

In sum, my understanding is that obviousness invalidates claims that merely recite combinations of, or obvious variations of, prior art teachings using understanding and knowledge of one of skill in the art at the time and motivated by the general problem facing the inventor at the time. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of or attempting obvious variations on prior art references in the claimed manner.

Legal Standard for Claim Construction

I understand that before any invalidity analysis can be properly performed, the scope and meaning of the challenged claims must be determined by claim construction.

I understand that a patent may include two types of claims, independent claims and dependent claims. I understand that an independent claim stands alone

and includes only the limitations it recites. I understand that a dependent claim depends from an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to the limitations recited in the claim (or claims) from which it depends.

In comparing the challenged claims to the prior art, I have carefully considered the patent and its file history in light of the understanding of a person of skill at the time of the alleged invention.

I understand that to determine how a person of ordinary skill would have understood a claim term, one should look to sources available at the time of the alleged invention that show what a person of skill in the art would have understood disputed claim language to mean. It is my understanding that this may include what is called “intrinsic” evidence as well as “extrinsic” evidence.

I understand that, in construing a claim term, one should primarily rely on intrinsic patent evidence, which includes the words of the claims themselves, the remainder of the patent specification, and the prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient. I understand that extrinsic evidence may include principles, concepts, terms, and other resources available to those of skill in the art at the time of the invention.

I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else or something more specific. I understand that to determine whether a term has special meaning, the claims, the patent specification, and the prosecution history are particularly important, and may show that the inventor gave a term a particular definition or intentionally disclaimed, disavowed, or surrendered claim scope.

I understand that the claims of a patent define the scope of the rights conferred by the patent. I understand that because the claims point out and distinctly claim the subject matter which the inventors regard as their invention, claim construction analysis must begin with and is focused on the claim language itself. I understand that the context of the term within the claim as well as other claims of the patent can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, how a term is used in one claim can often inform the meaning of the same term in other claims. Differences among claims or claim terms can also be a useful guide in understanding the meaning of particular claim terms.

I understand that a claim term should be construed not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the entire specification. I understand that because the

specification is a primary basis for construing the claims, a correct construction must align with the specification.

I understand that the prosecution history of the patent as well as art incorporated by reference or otherwise cited during the prosecution history are also highly relevant in construing claim terms. For instance, art cited by or incorporated by reference may indicate how the inventor and others of skill in the art at the time of the invention understood certain terms and concepts. Additionally, the prosecution history may show that the inventors disclaimed or disavowed claim scope, or further explained the meaning of a claim term.

With regard to extrinsic evidence, I understand that all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises, can also be considered. For example, technical dictionaries may indicate how one of skill in the art used or understood the claim terms. However, I understand that extrinsic evidence is considered to be less reliable than intrinsic evidence, and for that reason is generally given less weight than intrinsic evidence.

I understand that in general, a term or phrase found in the introductory words or preamble of the claim, should be construed as a limitation if it recites essential structure or steps, or is necessary to give meaning to the claim. For instance, I understand preamble language may limit claim scope: (i) if dependence

on a preamble phrase for antecedent basis indicates a reliance on both the preamble and claim body to define the claimed invention; (ii) if reference to the preamble is necessary to understand limitations or terms in the claim body; or (iii) if the preamble recites additional structure or steps that the specification identifies as important.

On the other hand, I understand that a preamble term or phrase is not limiting where a challenged claim defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention. I understand that to make this determination, one should review the entire patent to gain an understanding of what the inventors claim they invented and intended to encompass in the claims.

I understand that 35 U.S.C. § 112 ¶ 6 created an exception to the general rule of claim construction called a “means plus function” limitation. These types of terms and limitations should be interpreted to cover only the corresponding structure described in the specification, and equivalents thereof. I also understand that a limitation is presumed to be a means plus function limitation if (a) the claim limitation uses the phrase “means for”; (b) the “means for” is modified by functional language; and (c) the phrase “means for” is not modified by sufficient structure for achieving the specified function.

I understand that a structure is considered structurally equivalent to the corresponding structure identified in the specification only if the differences between them are insubstantial. For instance, if the structure performs the same function in substantially the same way to achieve substantially the same result. I further understand that a structural equivalent must have been available at the time of the issuance of the claim.