Exhibit B-11

Invalidity Claim Chart for U.S. Patent No. 11,012,252 (the "'252 Patent")
in view of Obviousness References

As detailed in the cover pleading, and in addition to the reasons set forth in Exs. B-1 through B-10, the claims of the '252 Patent are invalid under 35 U.S.C. § 103 based on the prior art references identified in these invalidity contentions, alone or in combination with the obviousness references cited below. As explained in the cover pleading, a person of ordinary skill in the art as of the claimed priority date of the '252 Patent would have been motivated to combine the prior art identified in these invalidity contentions with the obviousness references cited below.

Defendants reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the invalidity contentions.

Common Management Interface Specification for 8X/16X Pluggable Transceivers Rev 3.0 ("CMIS") was published September 18, 2018. CMIS qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

A 4-32 Gb/s Bidirectional Link With 3-Tap FFE/6-Tap DFE and Collaborative CDR in 22 nm CMOS ("Musah") was published December 2014 in IEEE Journal of Solid-State Circuits, Volume 49, No. 12. Musah qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

A 12.5-Gbps, 7-bit Transmit DAC with 4-Tap LUT-based Equalization in 0.13um CMOS ("Chung") was published September 21, 2008. Chung qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (pre-AIA).

U.S. Patent 10,659,337 to Jamal Riani et al. ("Riani") was filed on August 28, 2018. Riani qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

A 40-Gb/s Quarter Rate SerDes Transmitter and Receiver Chipset in 65 nm CMOS ("Zheng") was published November 2017 in IEEE Journal of Solid-State Circuits, Volume 52, No. 11. Zheng qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

U.S. Patent 10,461,918 issued to Kobayashi et al. ("Kobayashi") was filed on August 31, 2018 and published on October 29, 2019. Kobayashi qualifies as prior art under at least 35 U.S.C. § 102(a)(1) and (2) (AIA).

U.S. Patent Application 2016/0099795 filed by Lusted et al. ("Lusted") was published on April 4, 2016. Lusted qualifies as prior art under at least 35 U.S.C. § 102(a)(1) and (2) (AIA).

U.S. Patent Application 2009/0274170 filed by Yu et al. ("Yu") was published on November 5, 2009. Yu qualifies as prior art under at least 35 U.S.C. § 102(a)(1) and (2)(AIA).

Chinese Patent 106953818 A to Yin ("Yin") was published July 14, 2017. Yin qualifies as prior art under at least 35 U.S.C. § 102(a)(1) and (2)(AIA).

U.S. Patent 8,251,721 to Ikeda et al. was filed on August 23, 2010 and issued August 28, 2012. Ikeda qualifies as prior art under at least 35 U.S.C. § 102(a)(1) and (2) (AIA).

U.S. Patent 10,498,562 to Norimatsu ("Norimatsu") was filed April 8, 2016 and published on December 3, 2019. Norimatsu qualifies as prior art under at least 35 U.S.C. § 102(a)(1) and (2) (AIA).

Texas Instruments DS125DF1610 retimer chip datasheet ("DS125DF1610") was published on March 2017. DS125DF1610 qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

U.S. Patent No. 7,762,727 to Aronson ("Aronson") was filed on October 31, 2008, and was issued on July 27, 2010. Aronson qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

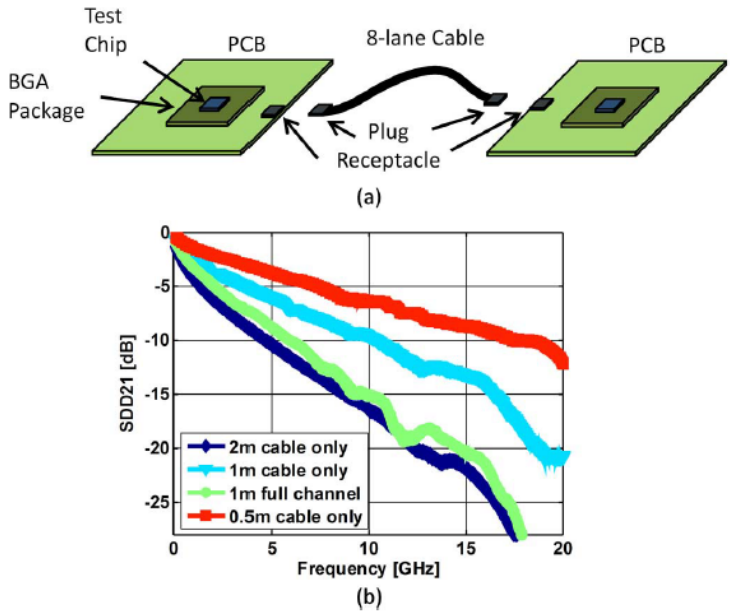
"High-speed Serial Bus Repeater Primer" Rev. 1.2 was published in October 2015 by Samie Samaan et al. ("Samaan"). Samaan qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

A. INDEPENDENT CLAIM 1

Claim 1	Disclosure
1[pre] An active Ethernet cable that comprises:	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: **1.1 Introduction** This specification defines the Common Management Interface Specification (CMIS) for QSFP-DD, OSFP and COBO in order to enable flexible use of modules and cable assemblies (hereafter referred to as modules unless cable assemblies are specifically mentioned) by the user. It shares some similarities with the management interfaces used in other form factors such as QSFP, SFP, and CFP. This specification supports a module with 8 host electrical lanes. Support for modules with more host lanes is possible (in increments of up to 8 lanes) by a bank selection feature (which allows several instances of an adressable page to exist in the paged register map). Due to this new mechanism this specification is not backwards compatible with SFF-8636. Some host ports may support both 4-channel and 8-channel devices; when a 4-channel device is inserted into such a port the appropriate memory map (e.g. SFF-8636) must be used. This case is outside the scope of this document. The host-to-module interactions needed to initialize active modules are presented in two state machines. A module-level state machine defines the initialization of the management interface as well as control of the module-wide power mode. A data path-specific state machine defines the host and module interactions and behaviors needed for power up and initialization of the data path(s) in the module. The CMIS is intended to cover a wide range of possible module functionalities and applications, ranging from cable assemblies to coherent DWDM modules. The CMIS is designed with the intent not to burden the simple cases but to provide a common set of management interactions and a common register map. In some modules, multiplexing of the high speed signals between the host electrical interface and the module media interface may occur in the module. In this specification, all references to lane numbers are based on the electrical connector interface lanes, unless otherwise indicated. In cases where a status or control aspect is applicable only to lanes after multiplexing or demultiplexing has occurred, the status or control is intended to apply to all lanes in the data path, unless otherwise indicated. Symmetry is expected between the Tx and the Rx hardware structure; for example Tx lanes that are multiplexed in the Tx are demultiplexed in the Rx. Each Application selected by the host is applied to the same Tx and Rx host electrical lanes. CMIS, 5-6.

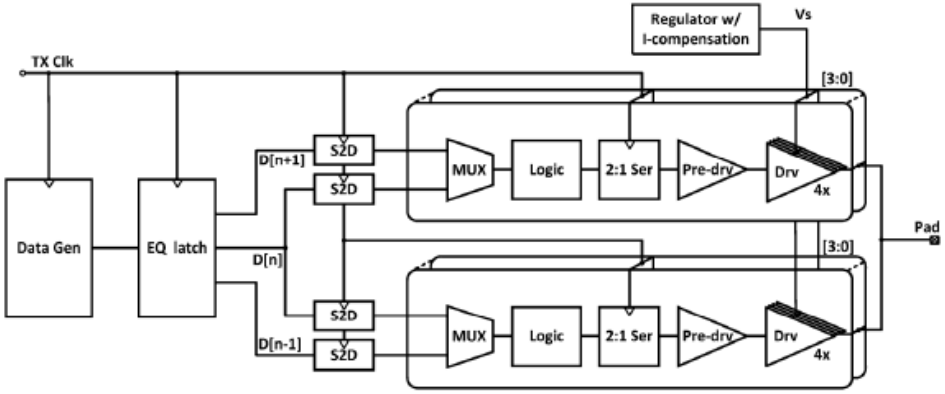
Claim 1	Disclosure
	Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. Table 1 and Table 2 provide a summary of the high-level behaviors and properties of each module state for passive copper cable assembly and active module implementations, respectively. Implementers of passive copper cable assemblies should note that this specification was designed to allow for flat-memory EEPROM implementations for that cable type. Active modules and active cable assemblies shall use the paged memory model. For all module types, refer to sections 1.4.3-1.4.9 for detailed requirements for each state. CMIS, 18. ***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.**

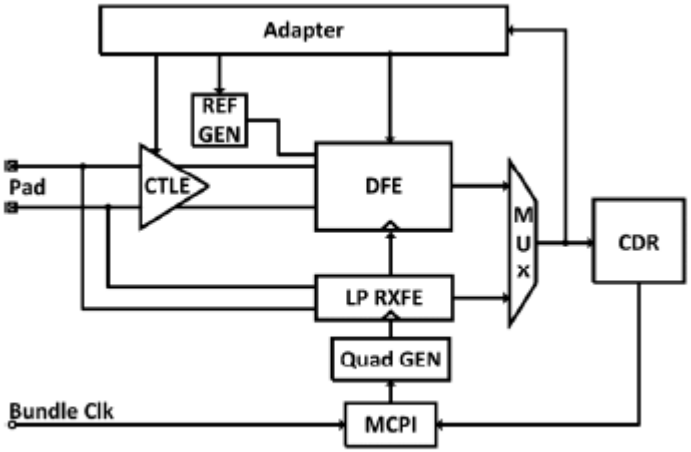
Claim 1	Disclosure
	Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling.

Claim 1	Disclosure
	Musah, 3079-3080.  Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 1	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

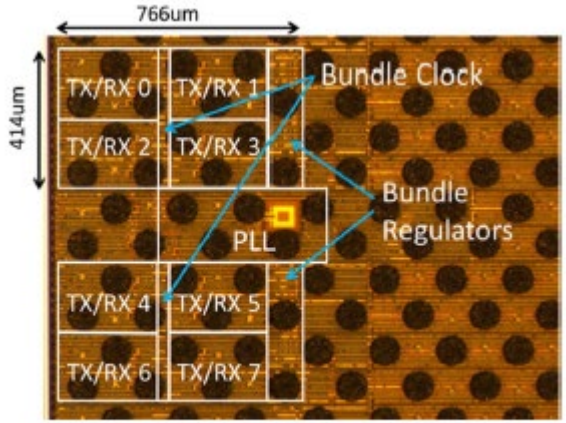
Claim 1	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 1	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

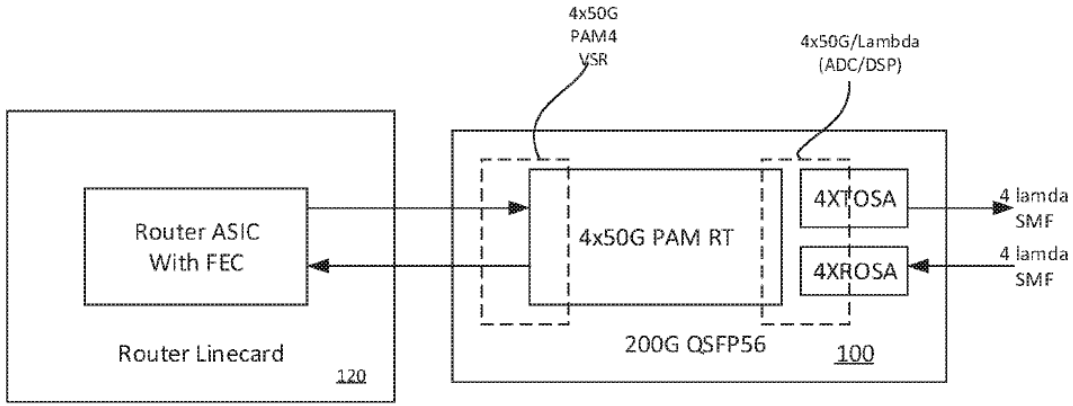
Claim 1	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

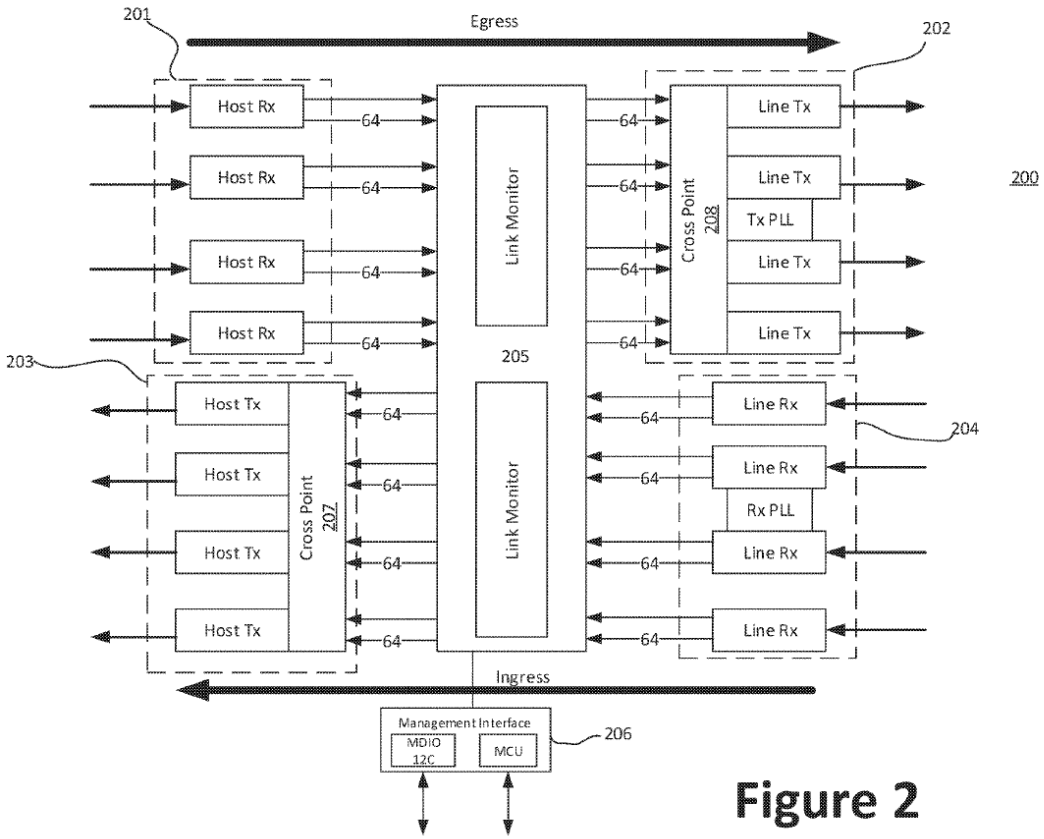
Claim 1	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 1	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 1	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 1	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088.

Claim 1	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 1	Disclosure
	 Riani, Figure 2.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 1	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G

Claim 1	Disclosure
	data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below. Riani, 4:43-5:5. ***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER < 10^{-12} over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 1	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 1	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 1	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 1	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 1	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

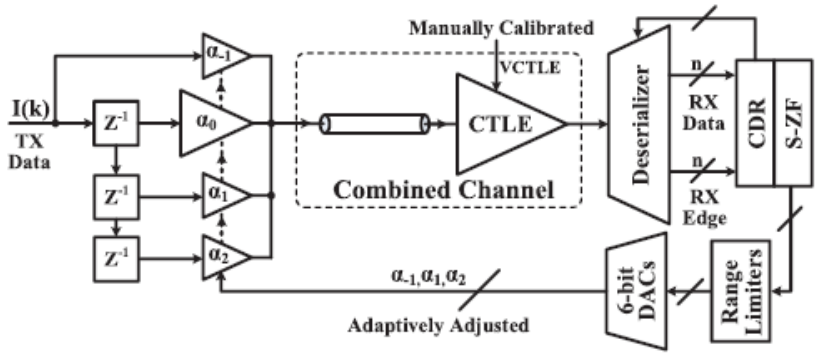
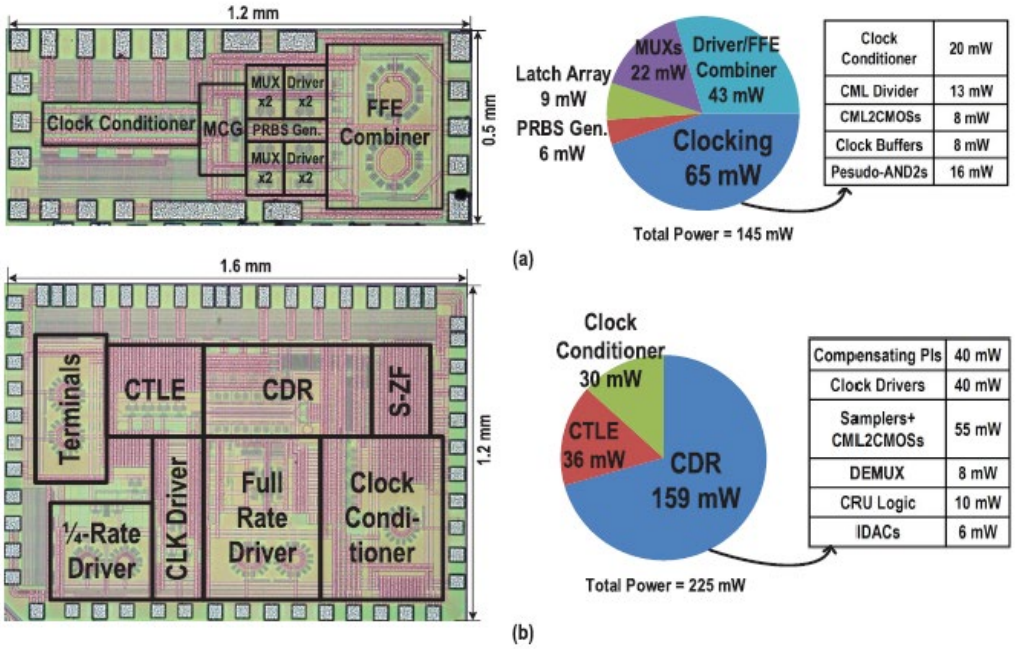


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

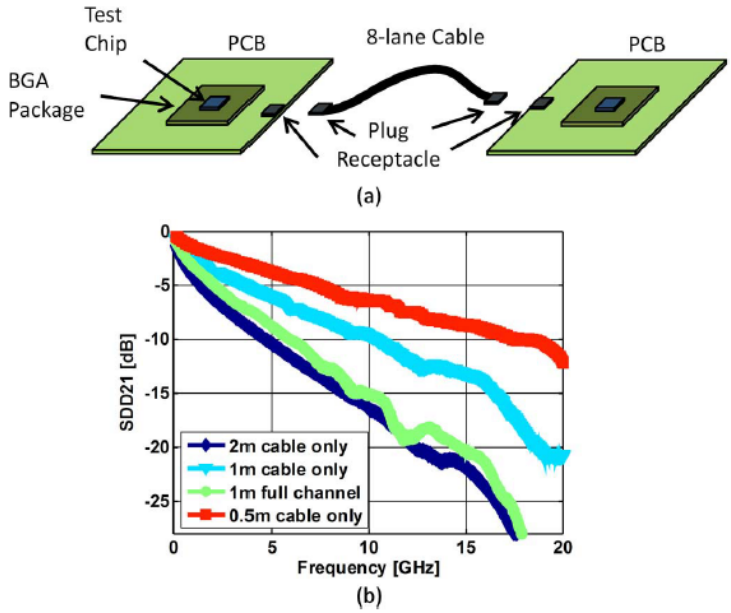
Claim 1	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 1	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 1	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 1, the data transmission system 1 is in accordance with DP1.4, for example, and includes an upstream device 2, a downstream device 4, and an active cable 3 connecting the upstream device 2 and downstream device 4." Kobayashi, 2:41-45.
1[a] electrical conductors connected between a first connector and a second connector,	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

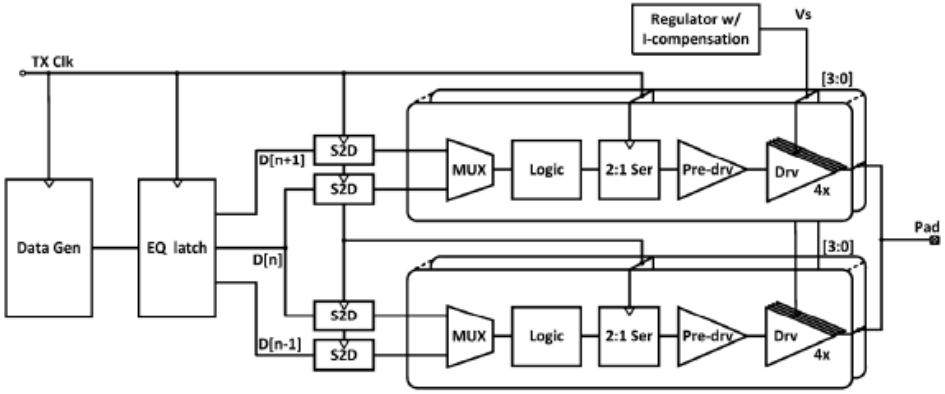
Claim 1	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

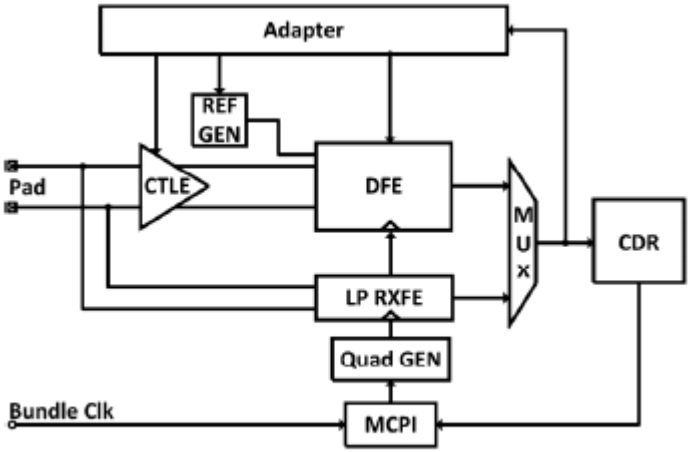
Claim 1	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 1	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 1	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

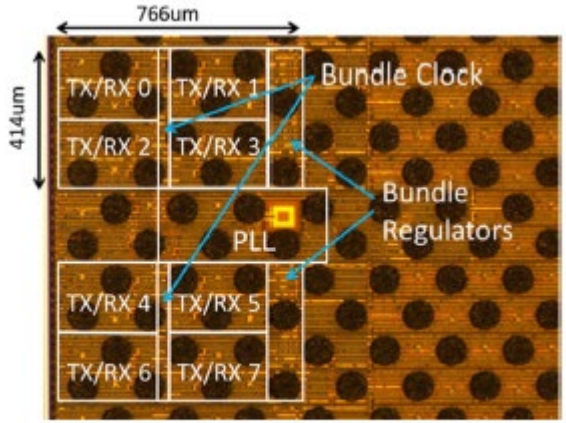
Claim 1	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 1	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 1	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

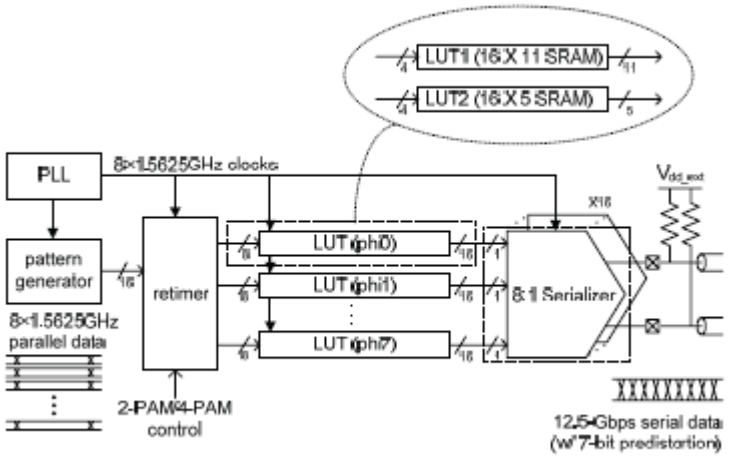
Claim 1	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 1	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 1	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

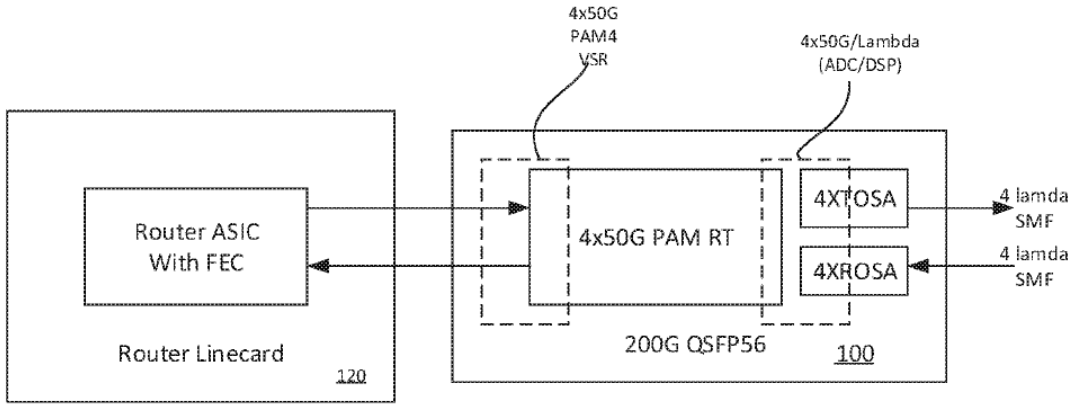
Claim 1	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

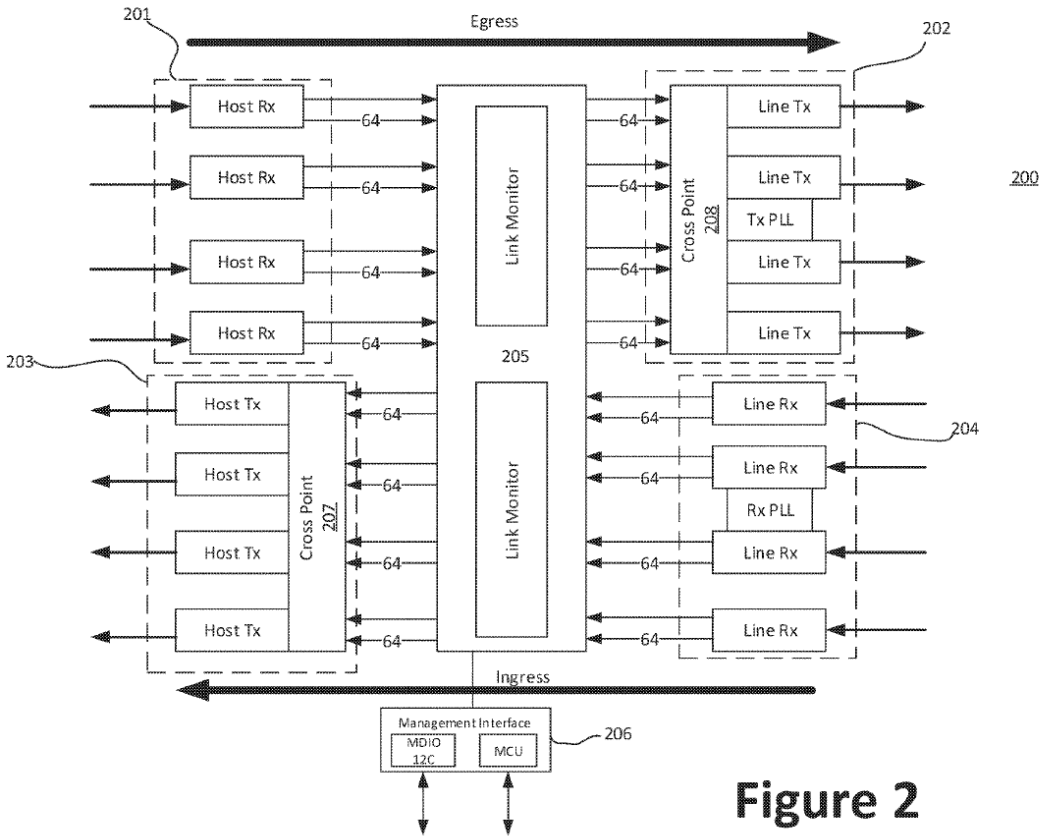
Claim 1	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 1	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 1	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 1	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 1	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 1	Disclosure
	 Riani, Figure 2.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 1	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 1	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 1	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 1	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 1	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

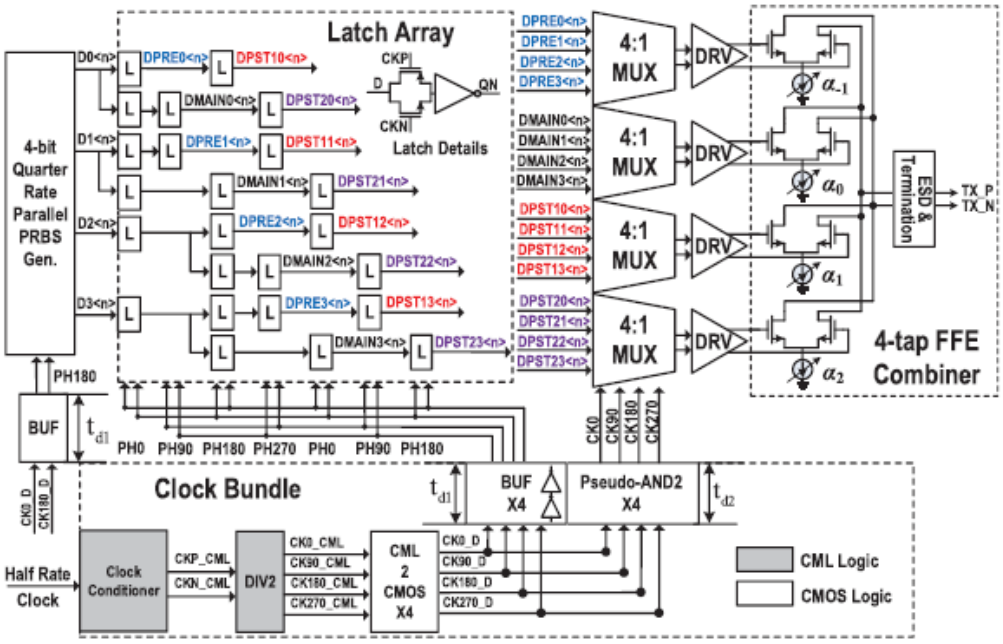
Claim 1	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

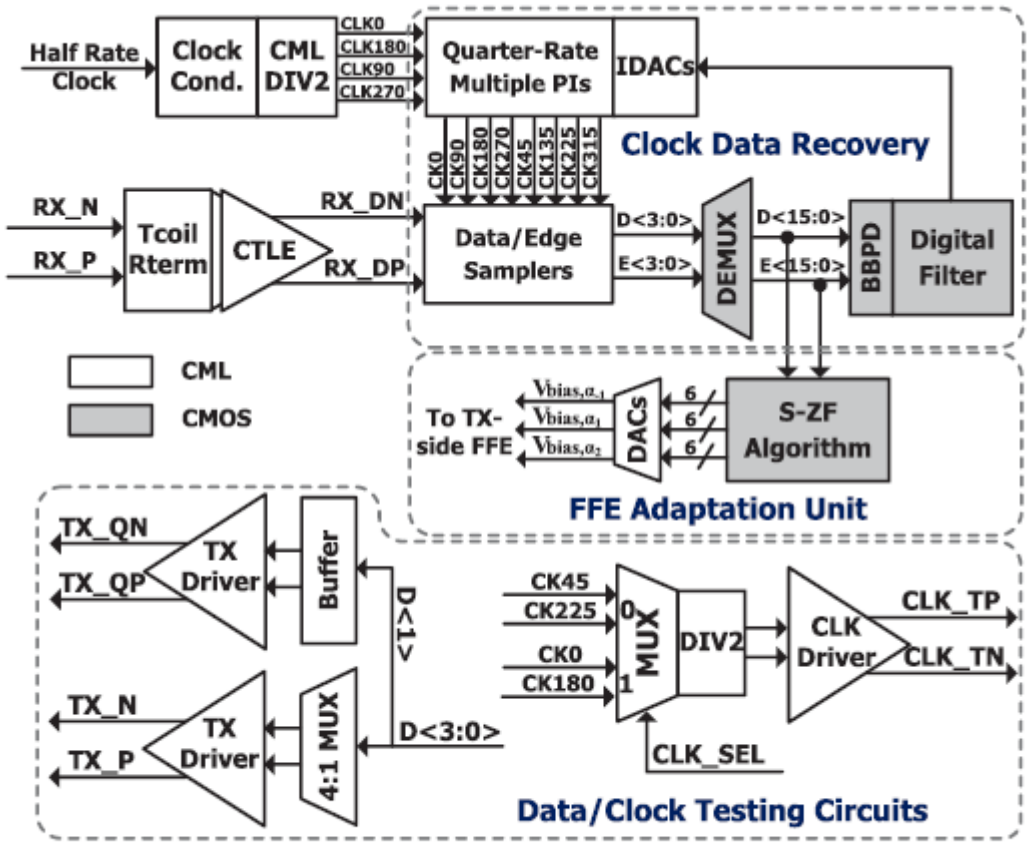
Claim 1	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 1	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 1	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 1	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 1	Disclosure
	 Fig. 1. Block diagram of the TX chip. Zheng, 2964.

Claim 1	Disclosure
	 Fig. 8. Block diagram of the RX chip. Zheng, 2966.

Claim 1	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 1	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 1	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 1	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

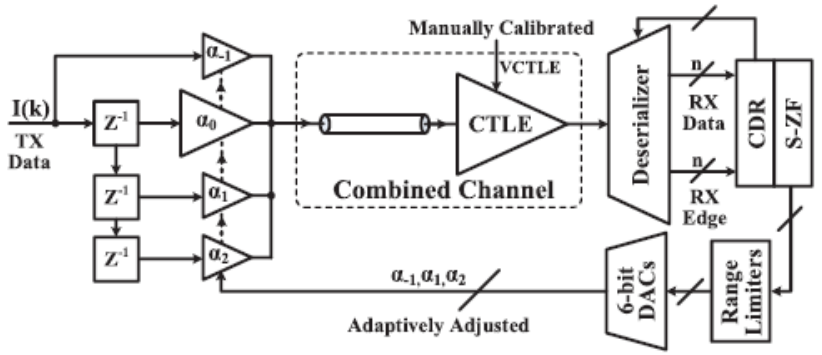
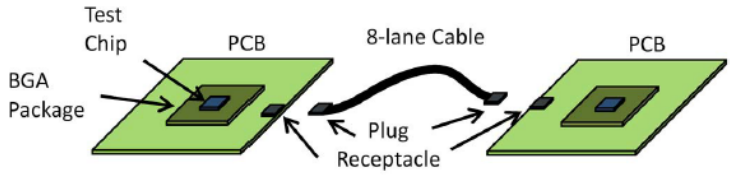
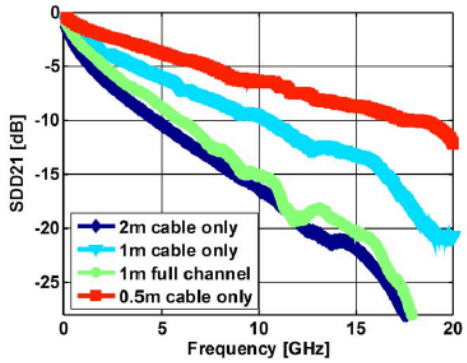


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 1	Disclosure
	Zheng, 2970. This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 1, the data transmission system 1 is in accordance with DP1.4, for example, and includes an upstream device 2, a downstream device 4, and an active cable 3 connecting the upstream device 2 and downstream device 4." Kobayashi, 2:41-45.
1[b] each of the first and second connectors being adapted to fit into an Ethernet port of a	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

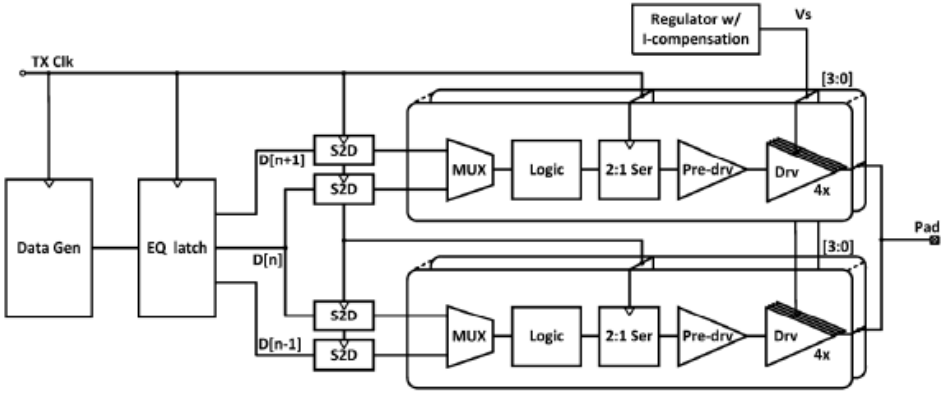
Claim 1	Disclosure
corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm².** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

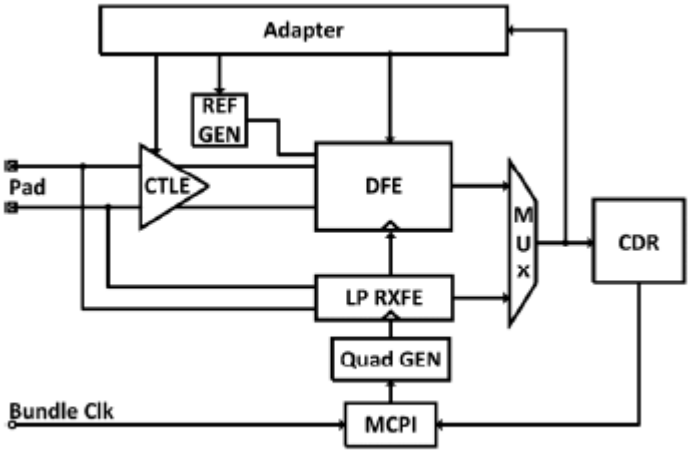
Claim 1	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 1	Disclosure
	 (a)  (b) Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 1	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

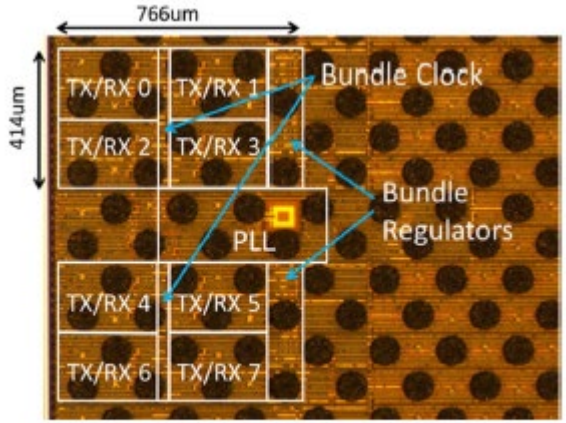
Claim 1	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 1	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 1	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

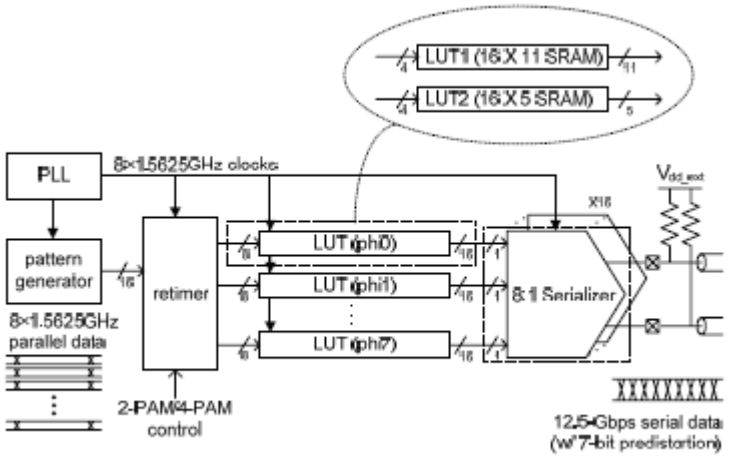
Claim 1	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 1	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 1	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

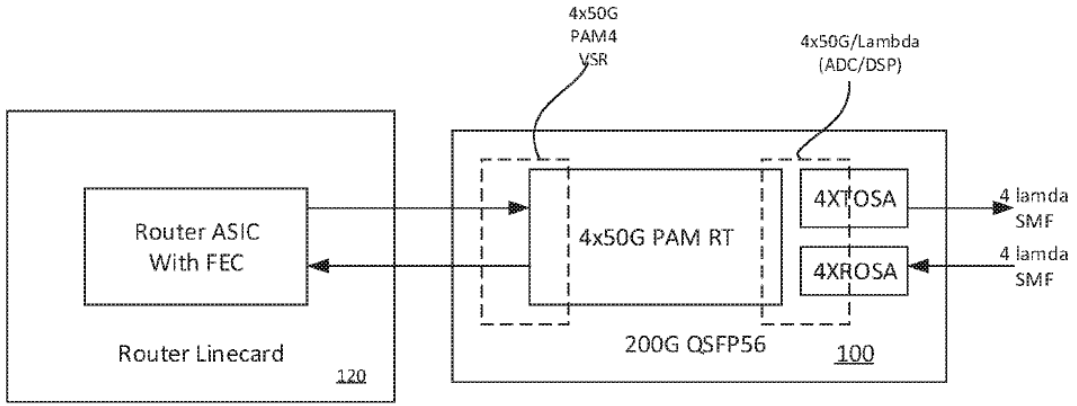
Claim 1	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

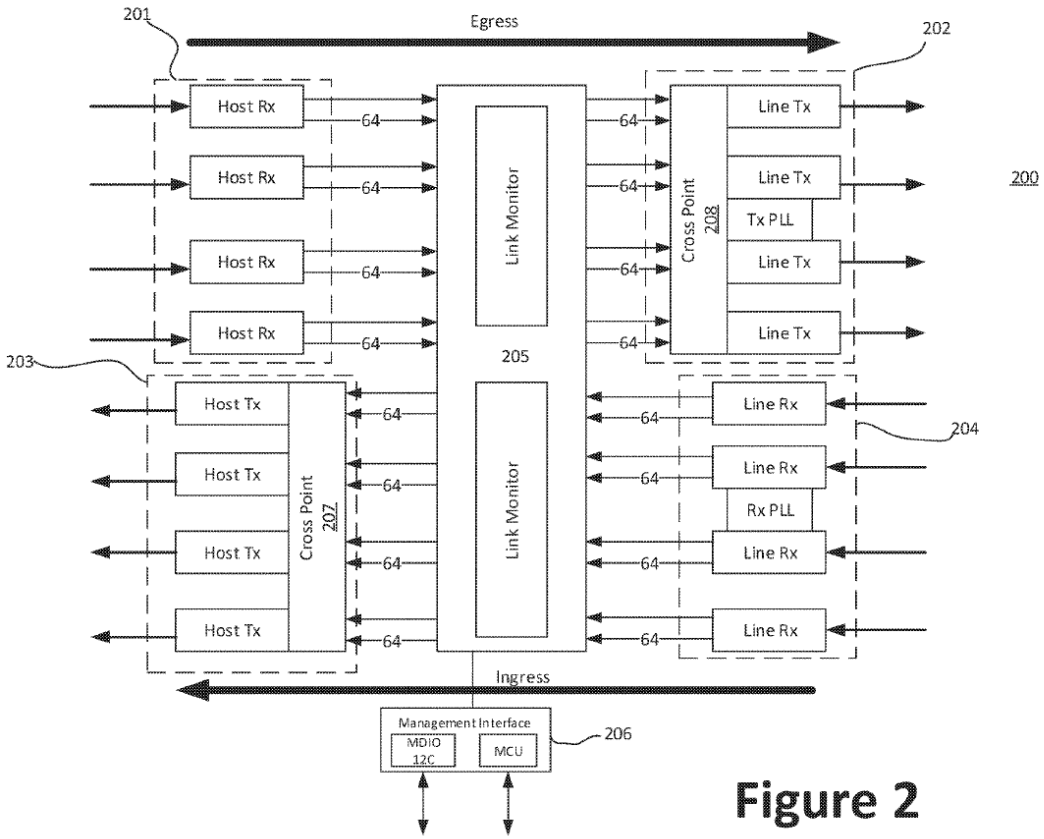
Claim 1	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 1	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 1	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 1	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 1	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 1	Disclosure
	 Riani, Figure 2.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 1	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 1	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 1	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 1	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 1	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 1	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 1	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 1	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector.

Claim 1	Disclosure
	Riani, 11:4-45. It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 1	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 1	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 1	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 1	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 1	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 1	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

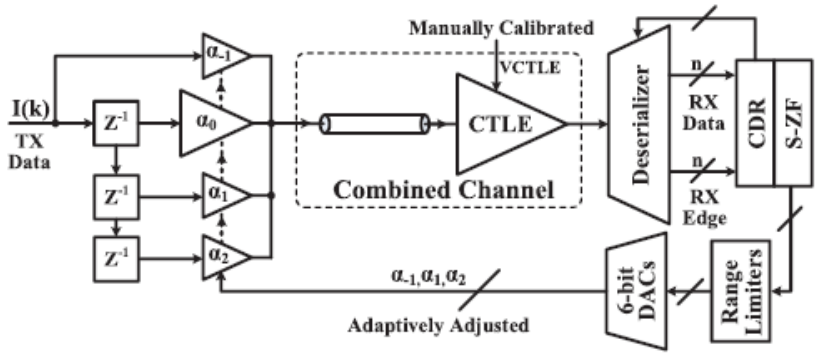
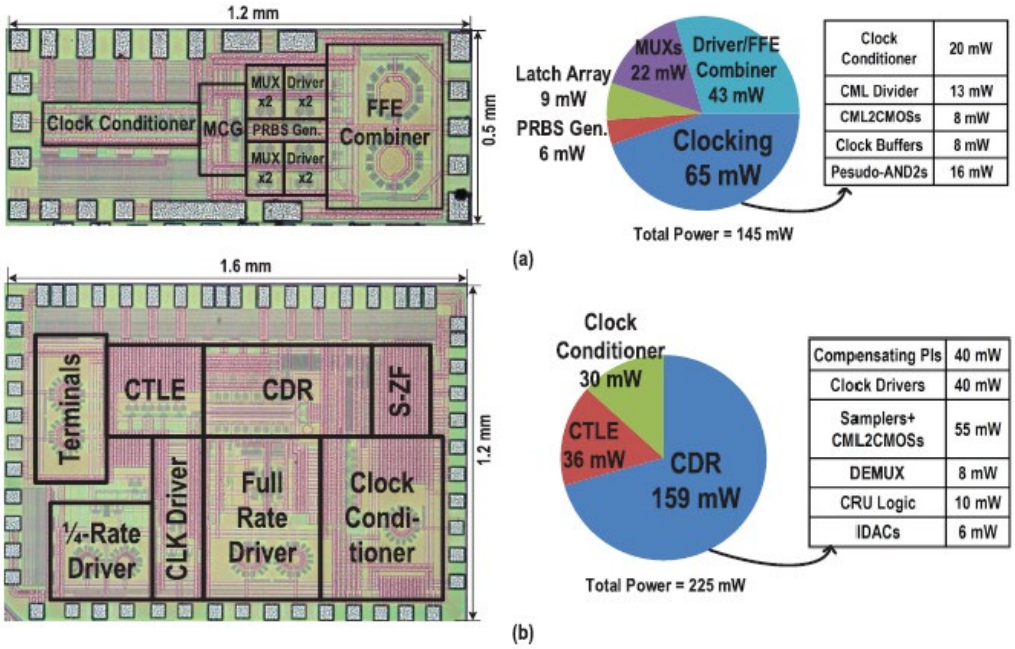


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

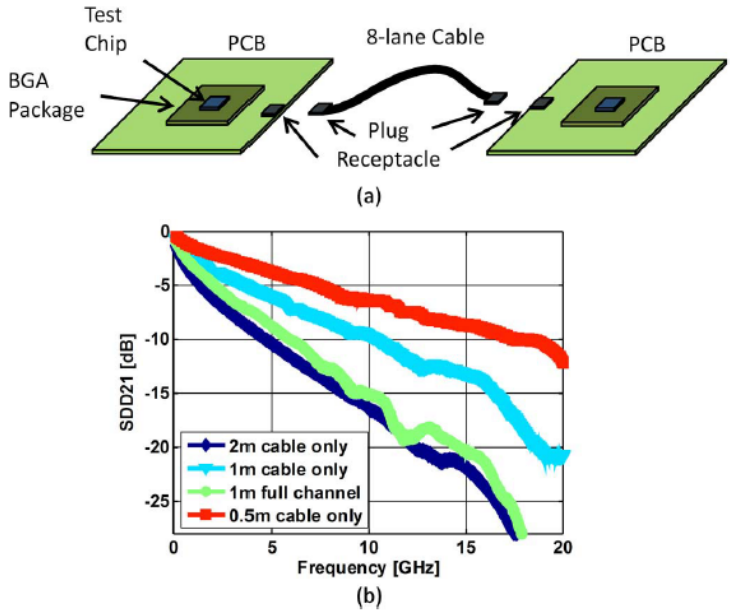
Claim 1	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 1	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 1	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "In the data transmission system 1 having the above configuration, the source 20 in the upstream device 2 generates a serial bit stream which is a video signal, for example. The source 20 transmits the generated serial bit stream from the downstream facing TX 20a to the retimer 21. The retimer 21 receives the serial bit stream transmitted from the downstream facing TX 20a in the upstream facing TX 21a. The retimer 21 performs a waveform shaping on the received serial bit stream and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 21b to the active cable 3." Kobayshi, 2:60-3:4.
1[c] each of the first and second connectors including a respective	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

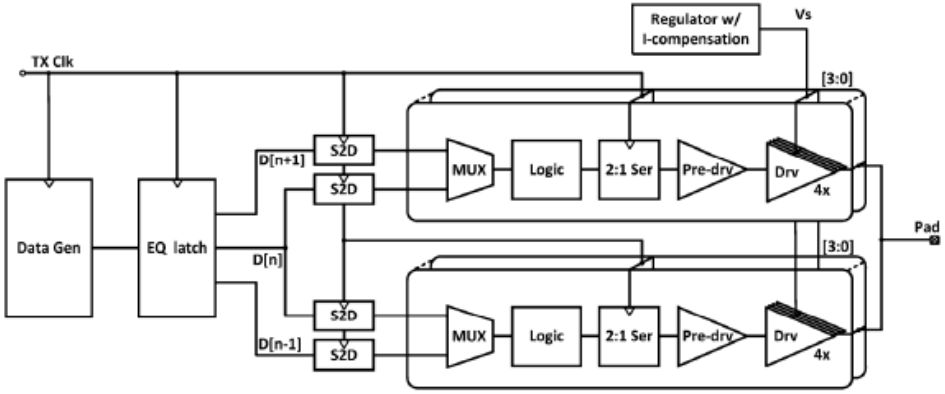
Claim 1	Disclosure
transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

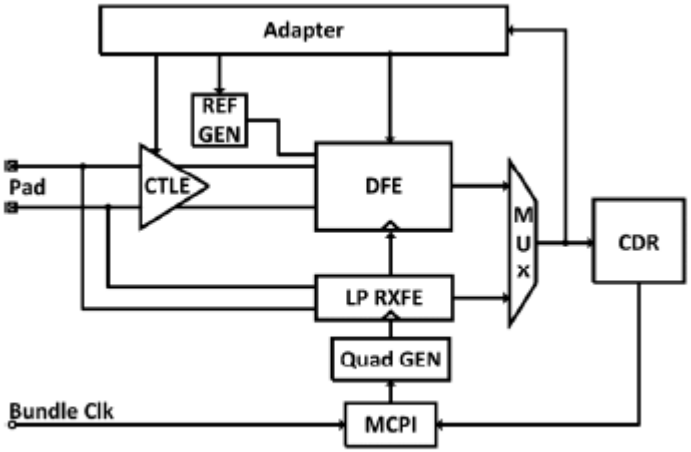
Claim 1	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 1	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 1	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

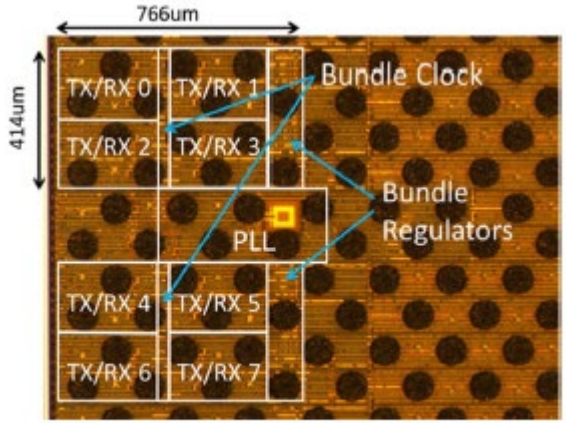
Claim 1	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 1	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 1	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

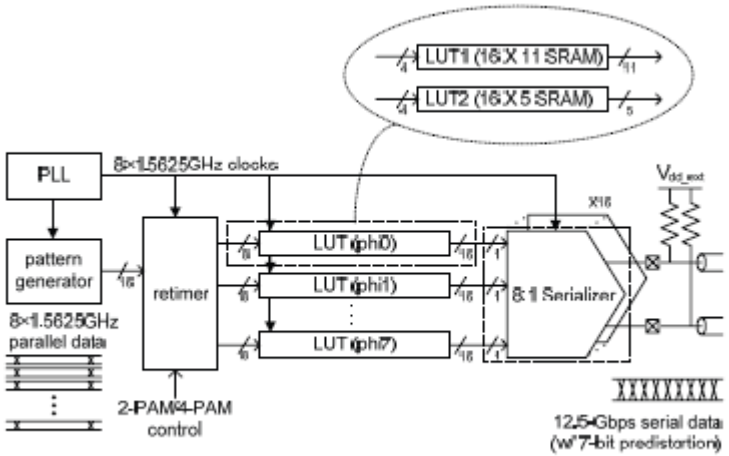
Claim 1	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 1	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 1	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

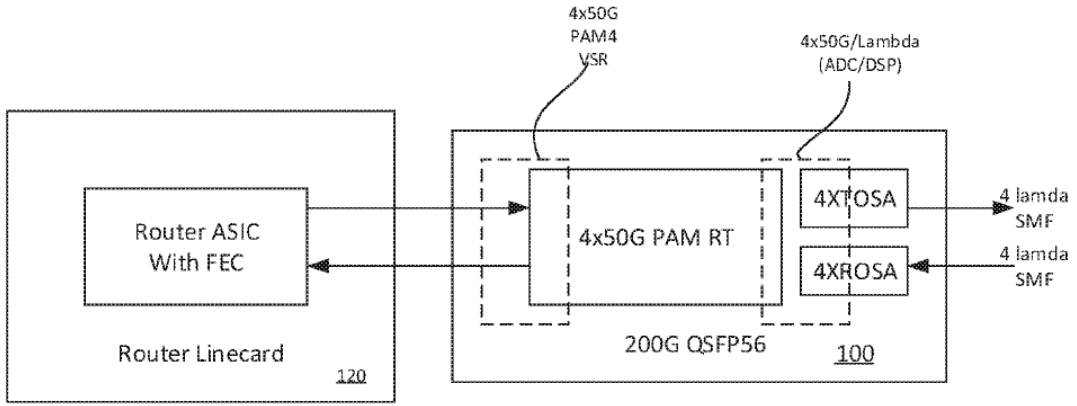
Claim 1	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

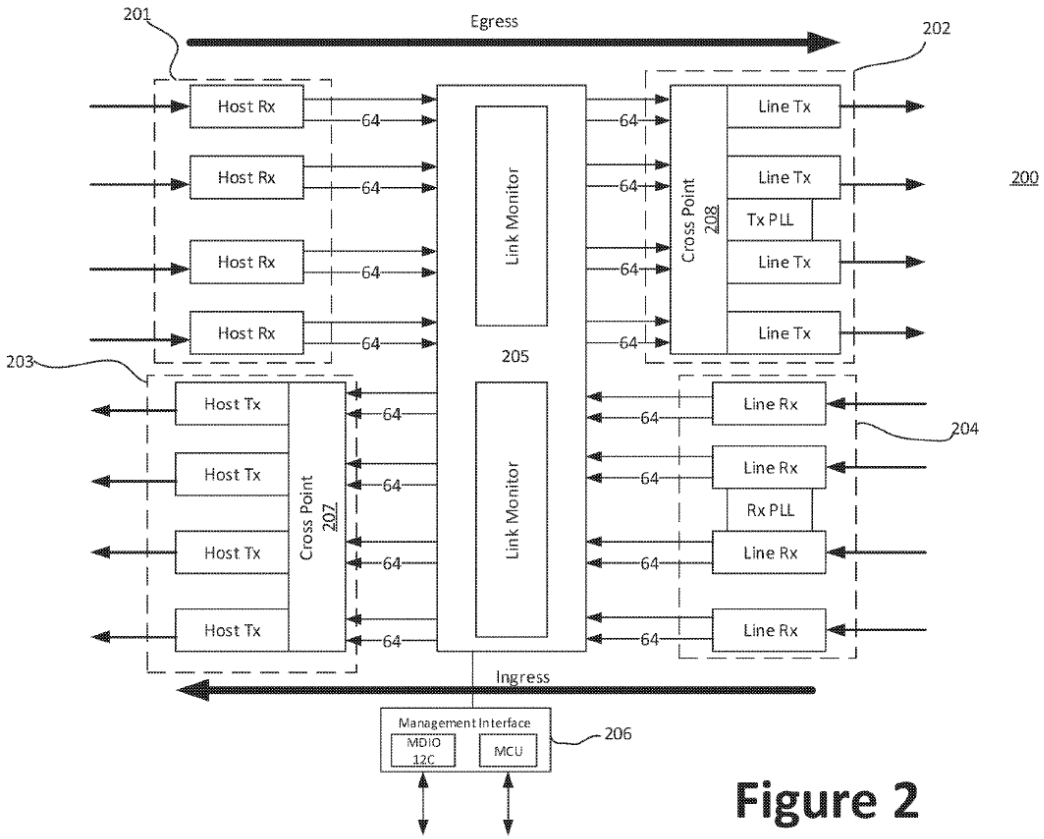
Claim 1	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 1	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 1	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 1	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 1	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 1	Disclosure
	 Riani, Figure 2.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 1	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 1	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 1	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 1	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 1	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 1	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 1	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 1	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 1	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 1	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 1	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 1	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 1	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 1	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 1	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

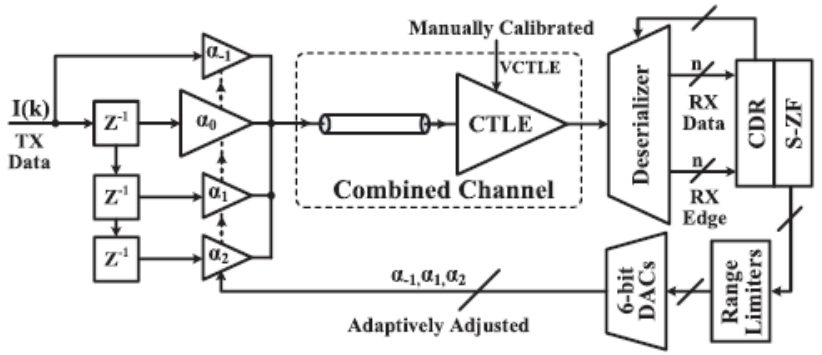
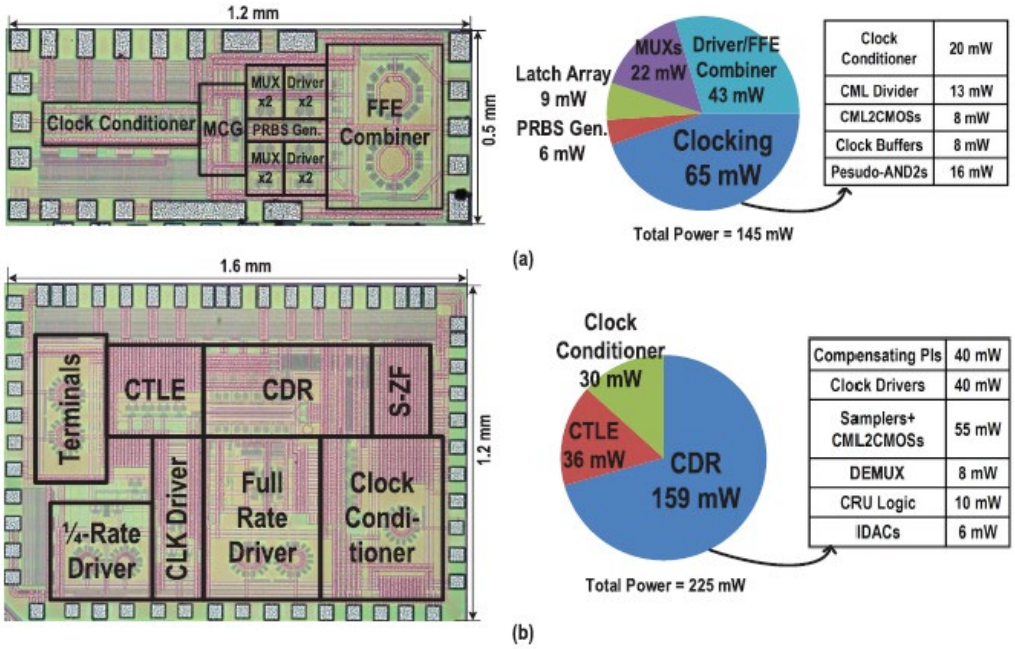


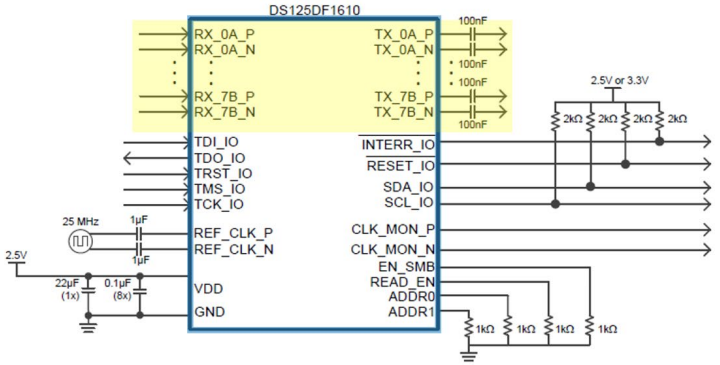
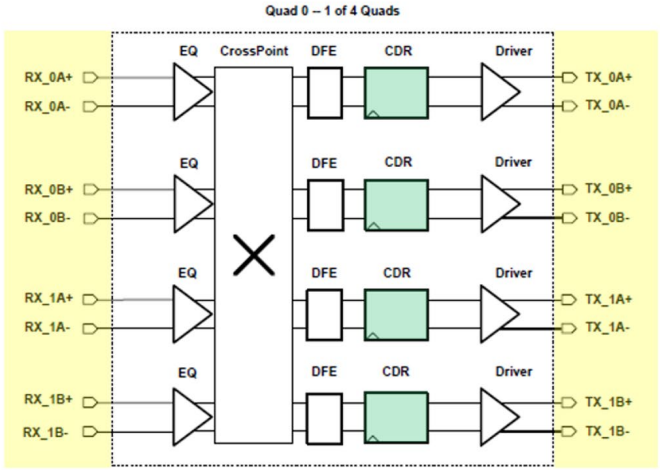
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

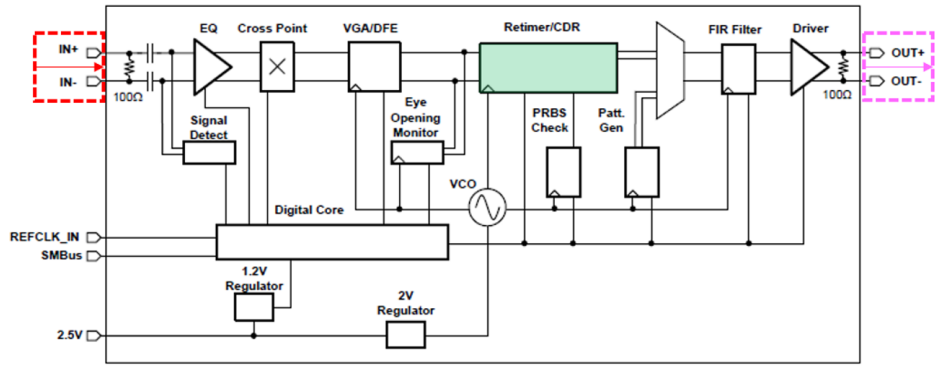
Claim 1	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 1	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 1	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK"

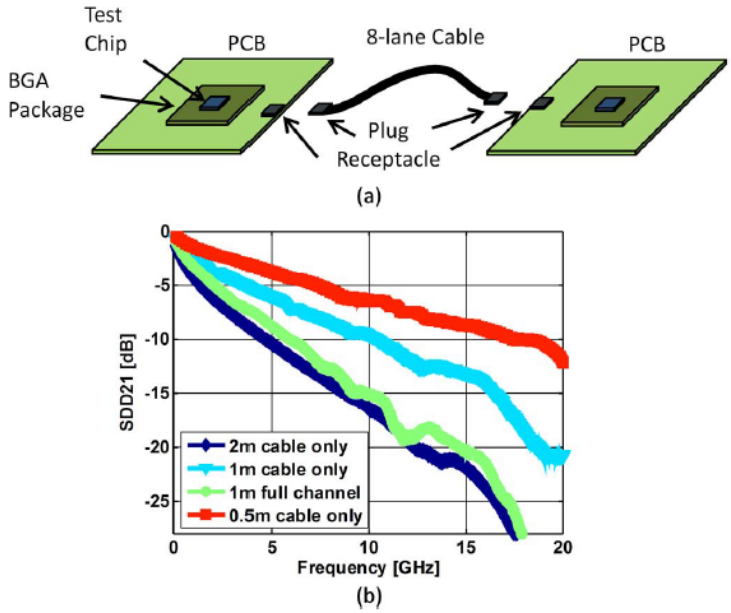
Claim 1	Disclosure
	Kobayashi, 4:4-22. <u>*DS125DF1610 Retimer Publication*</u> The DS125DF1610 circuit is illustrated in the Simplified Schematic and Figure 1 below. The highlighted pins illustrate sixteen channels of data, with each channel having two differential (Positive and Negative) input pins (RX_0A_P/N through RX_7B_P/N) to receive the channel of data and corresponding output pins (TX_0A_P/N through TX_7B_P/N) to transmit the channel of data after processing. *See, e.g.*, DS125DF1610 at §§ 3, 7.2. Thus, DS125DF1610's retimer is a transceiver that, when used in Tang's cable, receives one or more inbound data streams (on RX_0A_P/N through RX_7B_P/N), and transmits one or more transit data streams (via pins TX_0A_P/N through TX_7B_P/N).

Claim 1	Disclosure
	Simplified Schematic   **Figure 1. DS125DF1610 Simplified Cross Point Diagram** Figure 1 above shows four channels and illustrates that DS125DF1610's retimer processes each data channel by, inter alia, performing "clock and data recovery (CDR)." *See id.* at §§ 3, 7.1. A channel's data path is shown in more detail in DS125DF1610 Figure 2 (below), which illustrates the input signal conveying an inbound data stream and the transit signal conveying a transit data stream in Tang's cable

Claim 1	Disclosure
	when DS125DF1610's retimer implements Tang's signal driver 44.  **Figure 2. DS125DF1610 Simplified Data Path Diagram** The Retimer/CDR circuit performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream. *See id*. at § 7.3.6. The '252 Patent specification makes clear that the input signal from the host can be pre-processed before CDR is performed on it. An ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data for output as the transit data stream because after extracting the input signal's timing and using that timing to sample and extract the input signal's data in an analog-to-digital CDR process, the retimer generates a new data stream for equalization by the FIR Filter (a digital-to-analog process) and to be driven for output by the differential driver (which produces an analog signal with configurable output voltage levels) to convey the output data stream (transit data stream when outputting over the cable) as an analog signal over the cable conductors, where the new signal is a "re-modulation" of the data. *See id*. at §§ 7.3.6-7.3.9. .

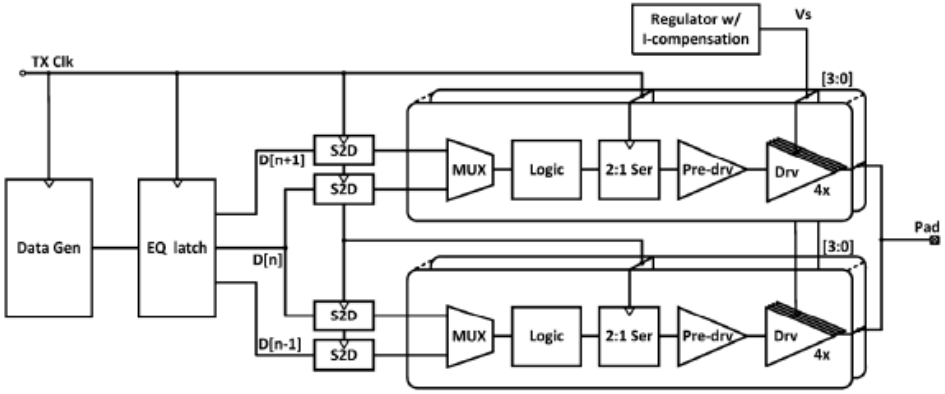
Claim 1	Disclosure
1[d] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and remodulate the transit data stream as the outbound data stream from the cable, and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: ***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm².** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

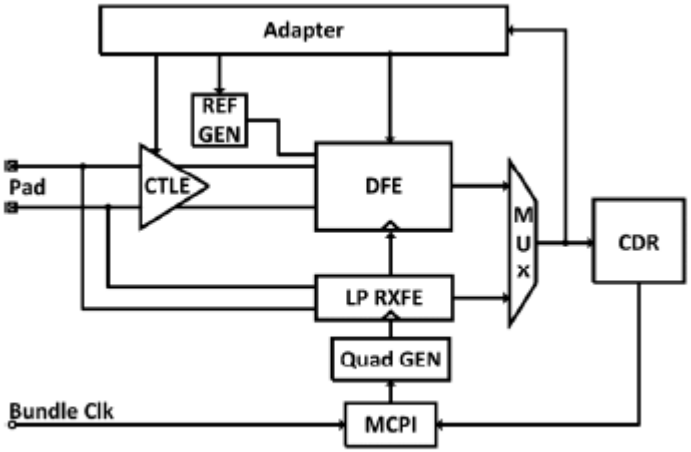
Claim 1	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 1	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 1	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

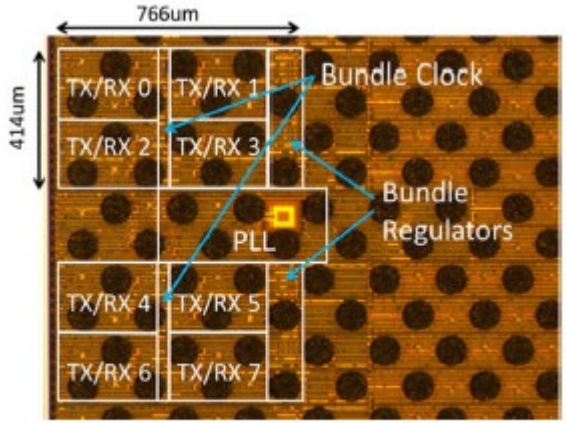
Claim 1	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 1	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 1	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

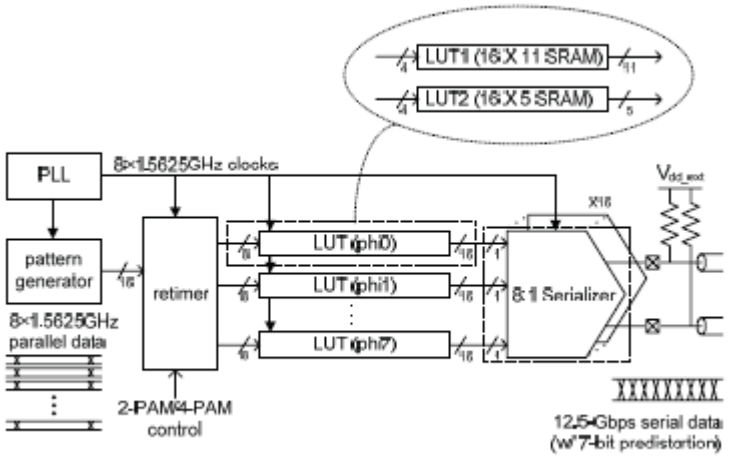
Claim 1	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 1	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 1	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

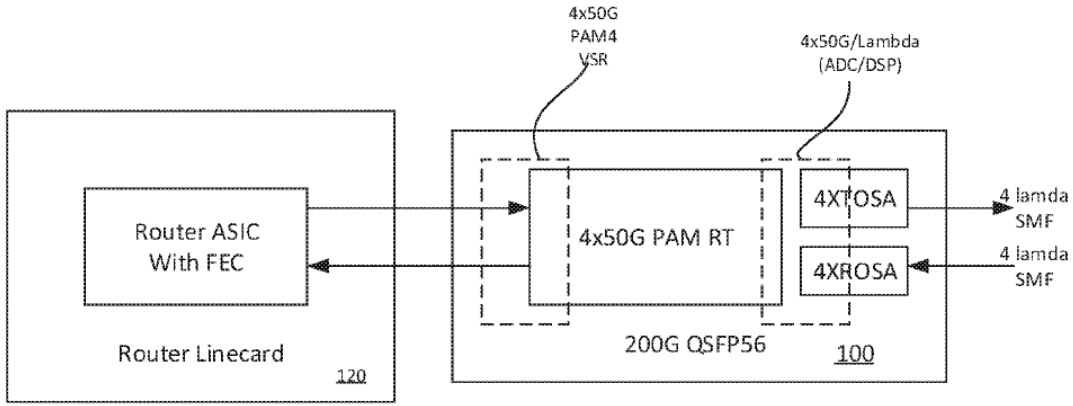
Claim 1	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

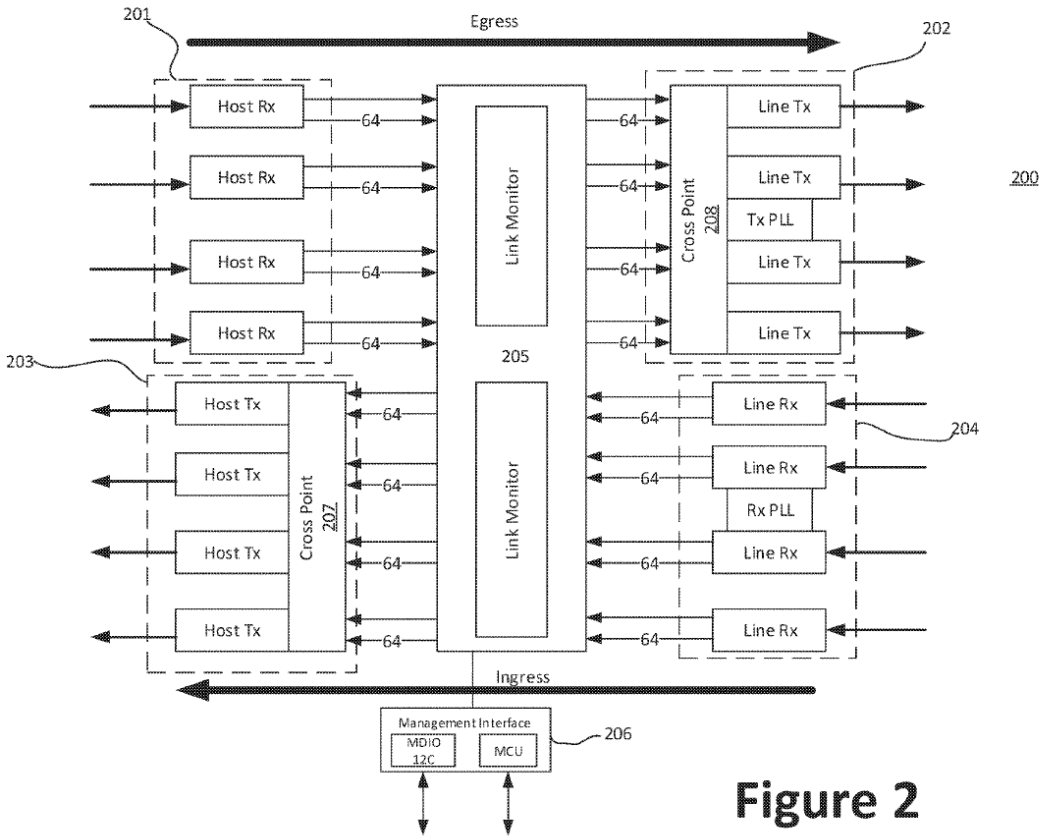
Claim 1	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 1	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 1	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 1	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 1	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 1	Disclosure
	 Riani, Figure 2.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 1	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 1	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 1	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 1	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 1	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 1	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 1	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 1	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 1	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 1	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 1	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 1	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 1	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 1	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 1	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

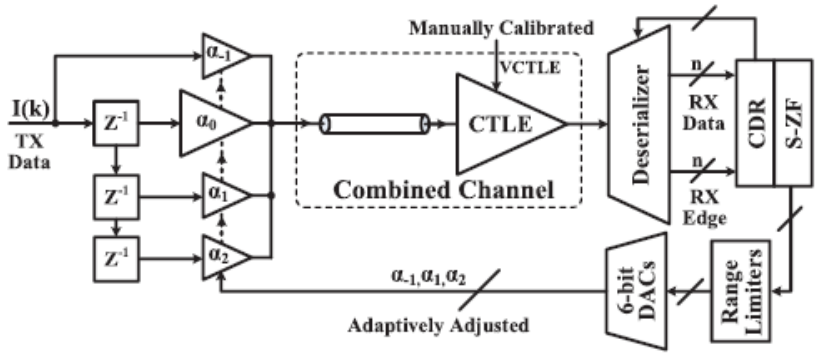
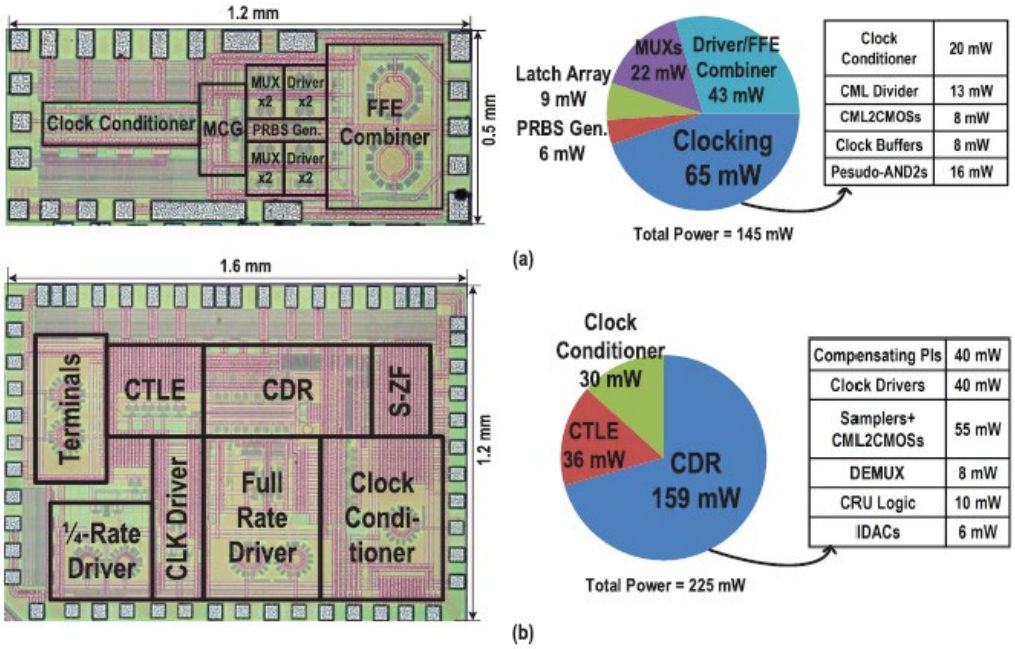
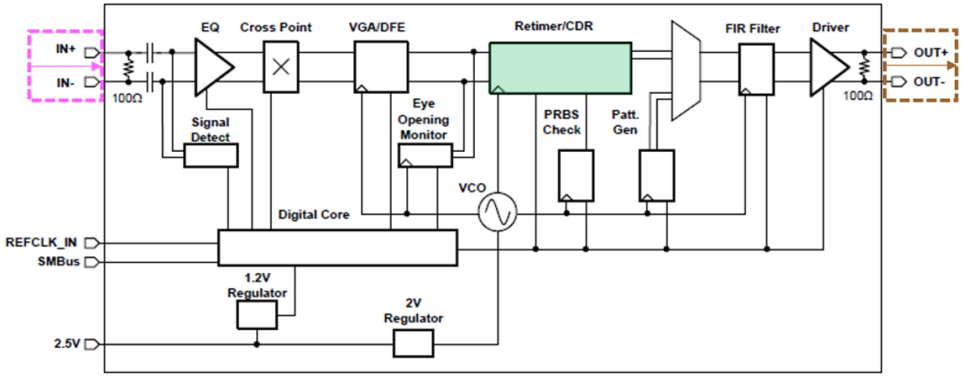


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 1	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 1	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 1	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK"

Claim 1	Disclosure
	Kobayashi, 4:4-22. *DS125DF1610 Retimer Publication* The DS125DF1610 retimer performs CDR for respective transit signals conveying transit data streams received from electrical conductors to generate output signals conveying outbound data streams that exit cable 10 to respective hosts, as shown in DS125DF1610 Fig. 2 below. For similar reasons to those discussed in claim limitation 1[c], an ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data as the outbound data after extracting the input signal's data and generating a newly-timed signal that is a "re-modulation" of the data.  **Figure 2. DS125DF1610 Simplified Data Path Diagram**

Claim 1	Disclosure
	5. The PCIe 3.0 Equalization Adaptation Protocol The PCIe 3.0 Base Specification [10] requires that a compliant Tx be able to produce any of the output equalization (TxEQ) levels shown in Figure 21, whenever requested to do so by the receiving port, during link equalization training. The same specification describes a protocol of TxEQ adaptation, where the host (upstream agent) or the end device (downstream agent) can each request that any of the TxEQ values in Figure 21 be presented to them by the other agent on the link. The intent of adaptation is to allow both agents to adjust the link partner's TxEQ to an optimal value for their receiver, and for the specific channel and operating conditions at hand. Samaan, p. 24.
1[e] the respective transceivers each employing fixed, cable-independent equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1.

Claim 1	Disclosure
	1.4.4 MgmtInit State The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp. CMIS, 22.

Claim 1	Disclosure
	1.5.4 Control Set Overview A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 1	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 1	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 1	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 1	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 1	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 1	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

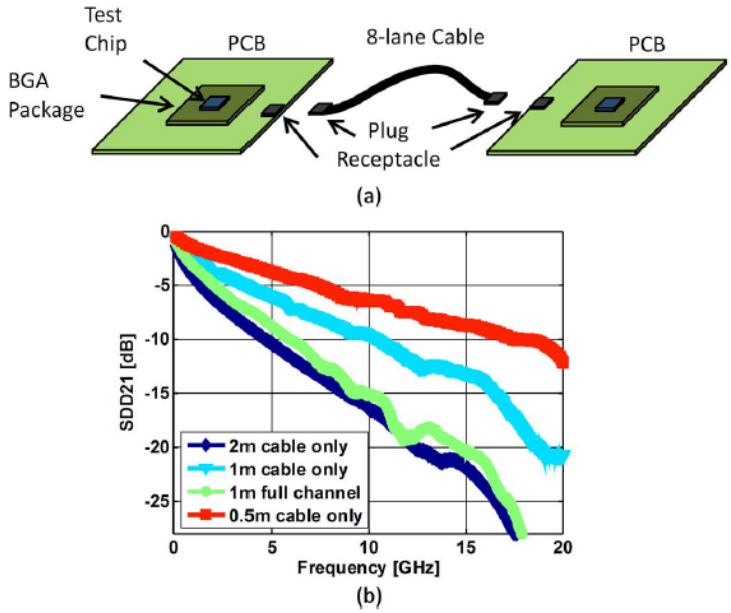
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

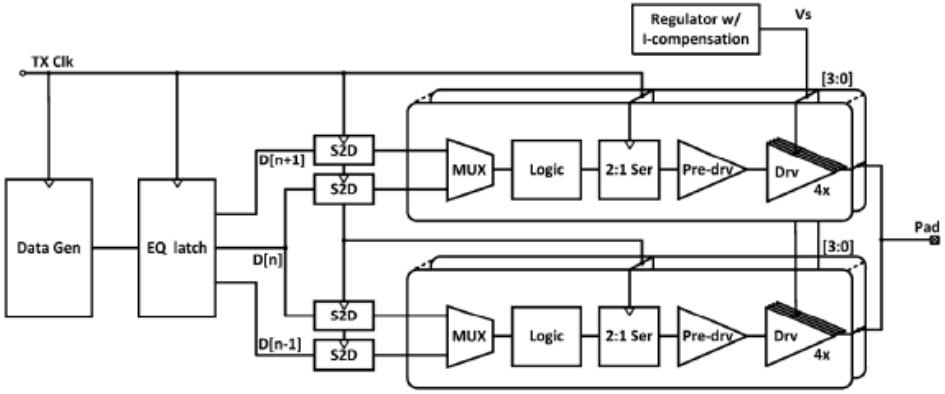
Claim 1	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

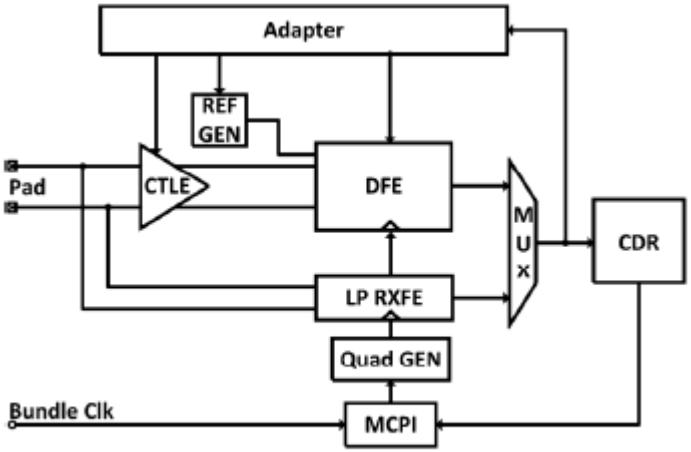
Claim 1	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 1	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 1	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

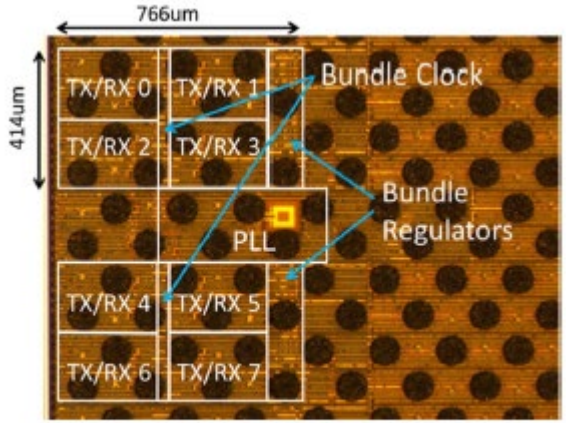
Claim 1	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 1	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 1	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

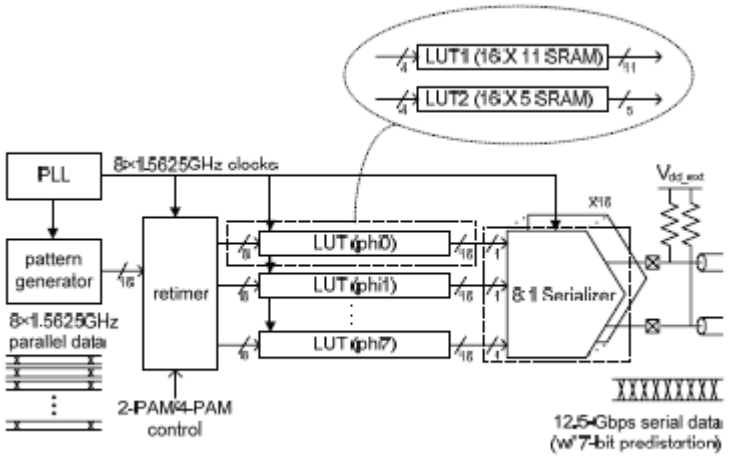
Claim 1	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 1	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 1	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

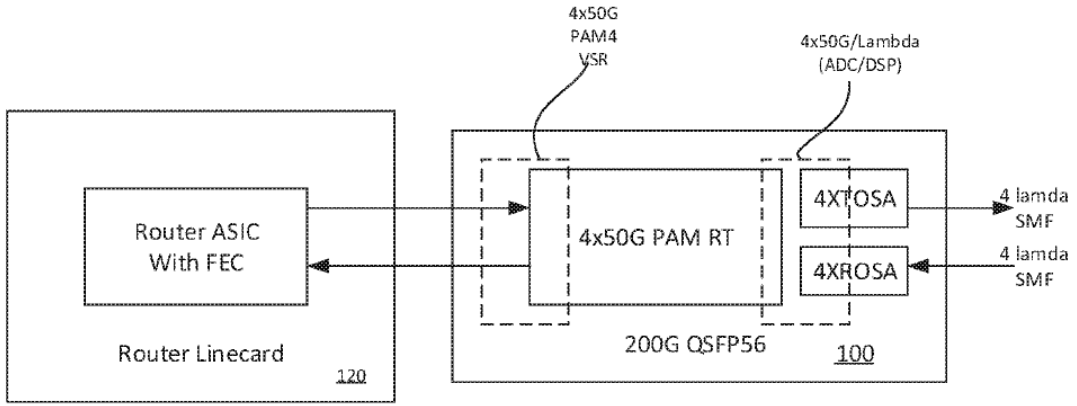
Claim 1	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

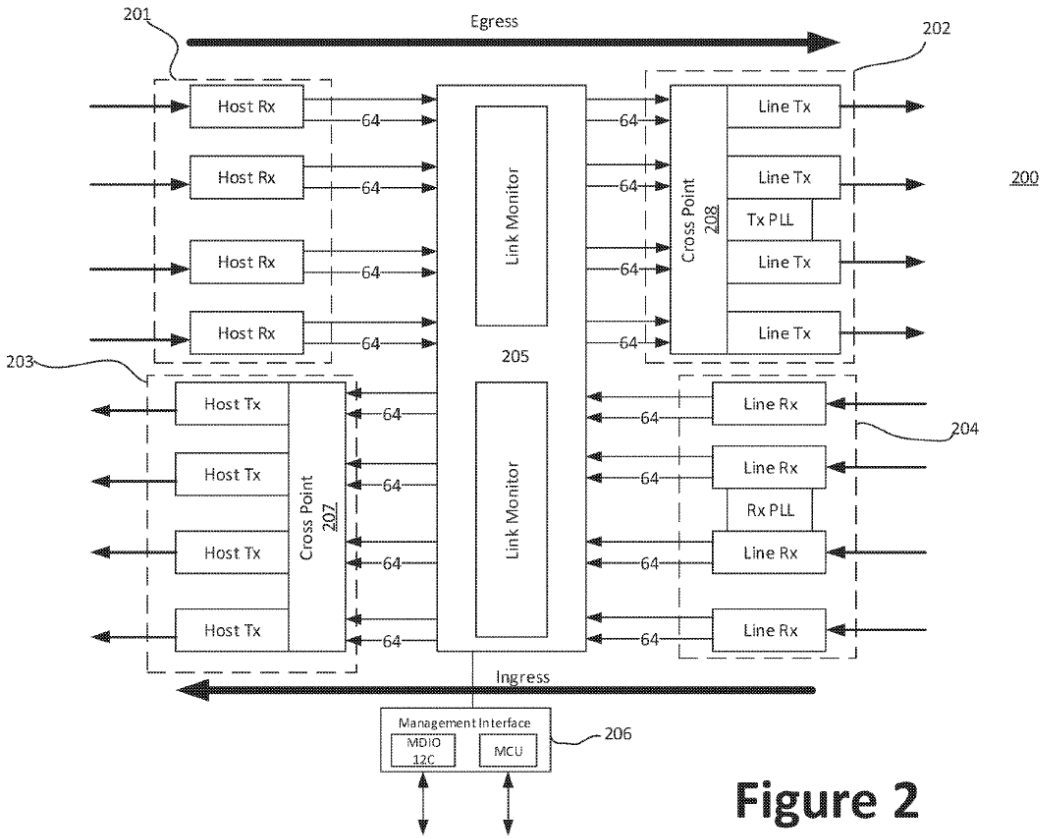
Claim 1	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 1	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 1	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 1	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 1	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 1	Disclosure
	 Riani, Figure 2.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 1	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 1	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 1	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 1	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 1	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 1	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 1	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 1	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 1	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 1	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 1	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 1	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 1	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 1	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 1	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 1	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

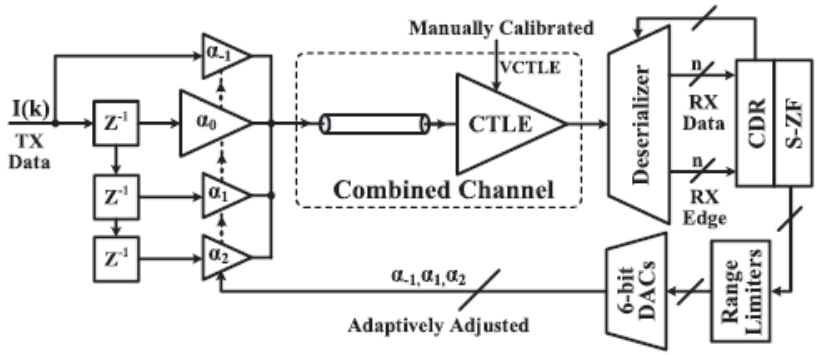
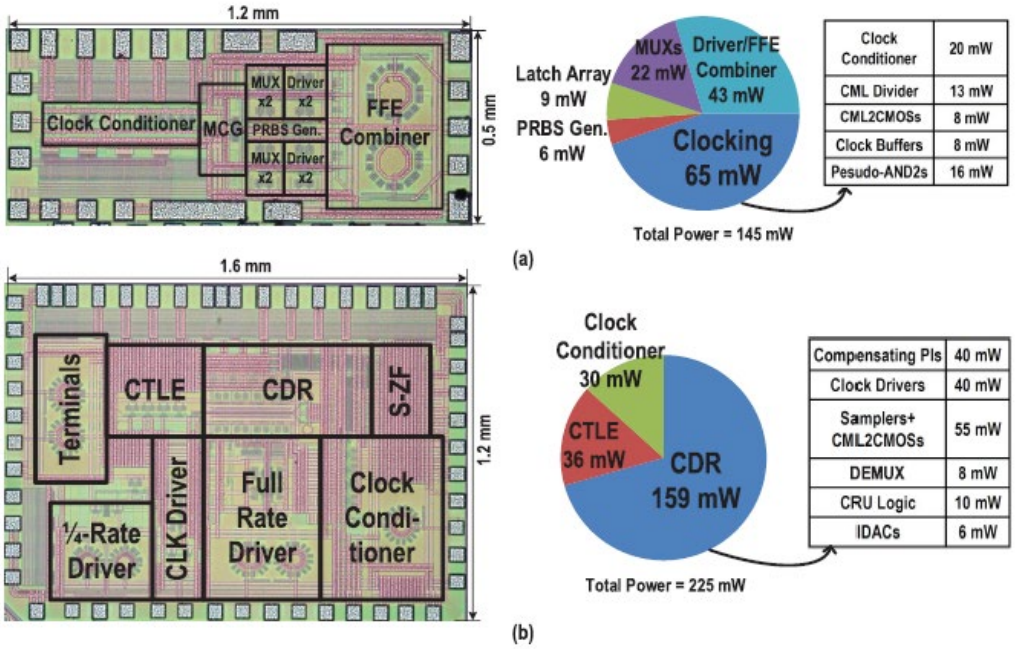


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

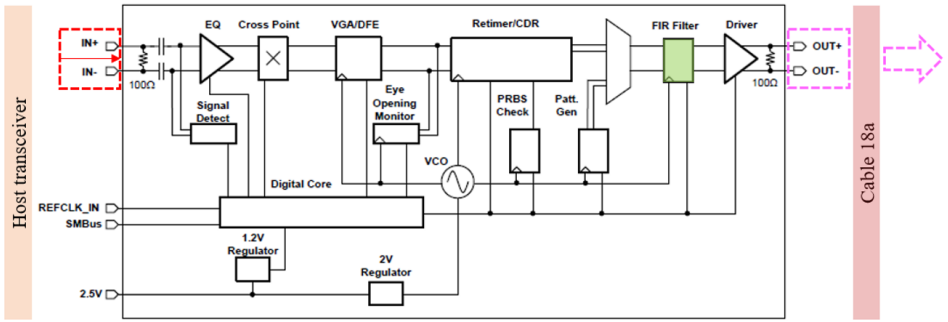
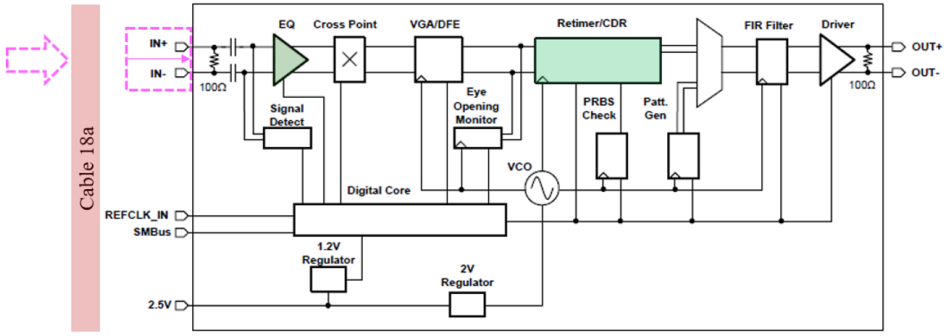
Claim 1	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

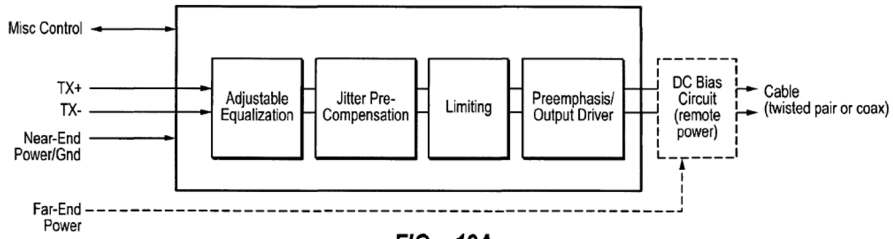
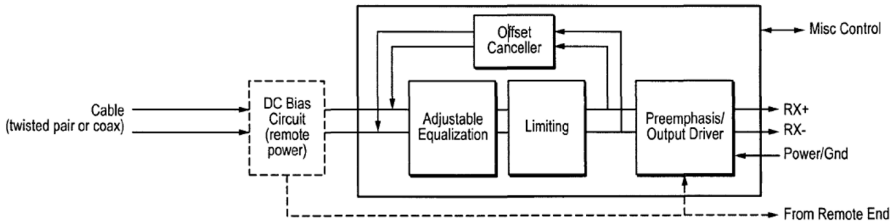
Claim 1	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 1	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The active cable 3 receives the serial bit stream transmitted from the upstream device 2 in the upstream facing RX 30a in one retimer 30. The retimer 30 performs a waveform shaping on the serial bit stream received by the upstream facing RX 30a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 30b to the other retime 31. The retimer 31 receives the serial bit stream transmitted from the retimer 30 in the upstream facing RX 31a. The retimer 31 performs a waveform shaping on the serial bit stream received by the upstream facing RX 31a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 31b to the downstream device 4." Kobayashi, 3:5-19. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX

Claim 1	Disclosure
	serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver." Kobayashi, 4:4-9. "The exchange module 202 is configured to communicate capabilities information with a remote link partner including host loss information, RS-FEC ability information, and RS-FEC request information. The exchange module 202 may transmit local host loss information to the link partner and receive remote host loss information from the link partner. In some embodiments, the exchange module 202 may be included in or otherwise established by the autonegotiation module 104 and thus the capabilities information may be exchanged during execution of an autonegotiation protocol. In some embodiments, the exchange module 202 may be included in or otherwise established by the PMD/PMA module 106 and thus the capabilities information may be exchanged during a startup protocol performed by the PMD/PMA module 106." Lusted, paragraph 23. "The autonegotiation module 104 is configured to auto-negotiate line transmission speed, mode of operation, and other communication parameters with a link partner when the communication lane 102 is brought up. Additionally, in some embodiments the autonegotiation module 104 may be configured to exchange capabilities information with the link partner including host insertion loss information, RS-FEC ability information, and RS-FEC request information. The autonegotiation module 104 may encode the capabilities information, for example, in an autonegotiation base page or in a next page. Although illustrated in FIG. 1 as coupled between the PMD/PMA 106 and the communication lanes 102, in other embodiments the autonegotiation module 104 may be included at different positions in the Ethernet port logic 100. For example, in some embodiments the autonegotiation module 104 may be coupled between the PMD/PMA 106 and the FEC 108." Lusted, paragraph 17. "In view of the above transmission characteristics of twisted-pair, current Ethernet chips are usually equipped with preemphasis technique of a transmitting end and equalization technique of a receiving end to compensate the difference in transmission attenuation of physical layer signals on different frequencies on

Claim 1	Disclosure
	the same medium during Ethernet baseband transmission. Main functions of the preemphasis technique of the transmitting end and the equalization technique of the receiving end include: amplifying signals on different frequencies differently at the transmitting end to compensate different transmission attenuation in the twisted pair; applying the equalization technique to different frequency components in signals received at the receiving end to compensate the attenuation." Yu, paragraph 34. "An embodiment of the present invention provides an equalizer setting apparatus, which uses a filter circuit 101, an analog-to-digital converter 102, a digital memory 103, a digital comparator 104 and a first digital accumulator 105, the filter circuit 101, the analog-to-digital converter 102, the digital memory 103, the digital comparator 104 and the first digital accumulator 105 are connected in sequence, the output end of the equalizer 201 is connected with the input end of the filter circuit 101, the output end of the first digital accumulator 105 is connected with the set value input end of the equalizer 201, the output end of the analog-to-digital converter 102 is connected with the input end of the digital comparator 104, so that the problems that the setting value of the equalizer is accurately set in the prior art, which is time-consuming and labor-consuming are solved, the method has the advantages of achieving accurate setting of the set value of the equalizer in a single time, fast, simple, convenient, accurate and low-cost manner and saving labor force to a certain extent." Yin, paragraph 26 (English translation). *DS125DF1610 Retimer Publication* The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610's FIR filter) and the CDR performed on the electrical input signal (by the DS125DF1610's EQ). DS125DF1610's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See*

Claim 1	Disclosure
	id. at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit signal."  Figure 2. DS125DF1610 Simplified Data Path Diagram  Figure 2. DS125DF1610 Simplified Data Path Diagram *U.S. Patent No. 7,762,727 to Aronson*

Claim 1	Disclosure
	Aronson discloses an active cable for high-speed transmissions between network nodes. See, e.g., Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.  *FIG. 12A*  *FIG. 12B* Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23.

Claim 1	Disclosure
	Aronson discloses the host-side equalization and pre-equalization use fixed cable-independent parameters to address host-side losses. *See, e.g.*, Aronson at 12:10-17, 14:16-23, 15:17-24. "Fixed" parameters reduced complexity and manufacturing costs. See, e.g., U.S. Patent No. 7,239,665 at 1:7-18 (discussing slow convergence with adaptive equalization); U.S. Patent App. Pub. No. 2011/0228821 at [0009]-[0011] (discussing tradeoffs between fixed and adaptive equalization); U.S. Patent No. 6,621,862 at 1:52-55 (large gate count for adaptive equalization can cause "high chip costs"); U.S. Patent App. Pub. No. 2006/0045176 at [0034] ("The adaptive equalizer can be trapped in a failure state (i.e., incorrect state) and not able to recover from the failure state."); U.S. Patent App. Pub. No. 2017/0187463 at [0058] ("[E]qualization techniques… come with different engineering tradeoffs, including trade-offs in power consumption, performance, and/or cost."). **5. The PCIe 3.0 Equalization Adaptation Protocol** The PCIe 3.0 Base Specification [10] requires that a compliant Tx be able to produce any of the output equalization (TxEQ) levels shown in Figure 21, whenever requested to do so by the receiving port, during link equalization training. The same specification describes a protocol of TxEQ adaptation, where the host (upstream agent) or the end device (downstream agent) can each request that any of the TxEQ values in Figure 21 be presented to them by the other agent on the link. The intent of adaptation is to allow both agents to adjust the link partner's TxEQ to an optimal value for their receiver, and for the specific channel and operating conditions at hand. Samaan, p. 24.

B. DEPENDENT CLAIM 2

Claim 2	Disclosure
2[a] The active Ethernet cable of claim 1,wherein the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp.

Claim 2	Disclosure
	CMIS, 22. **1.5.4 Control Set Overview** A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 2	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 2	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 2	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 2	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 2	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 2	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

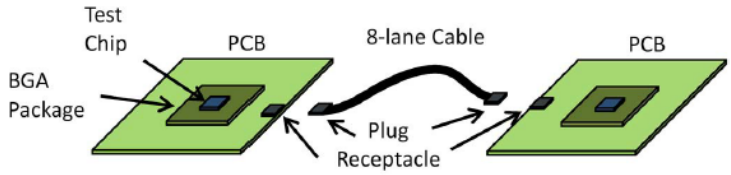
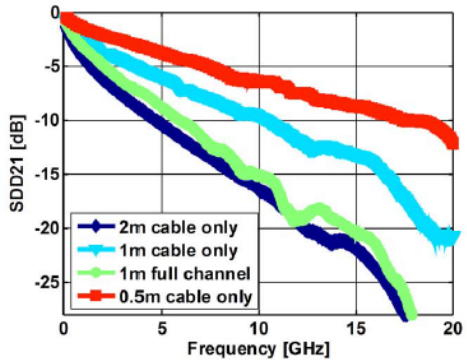
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

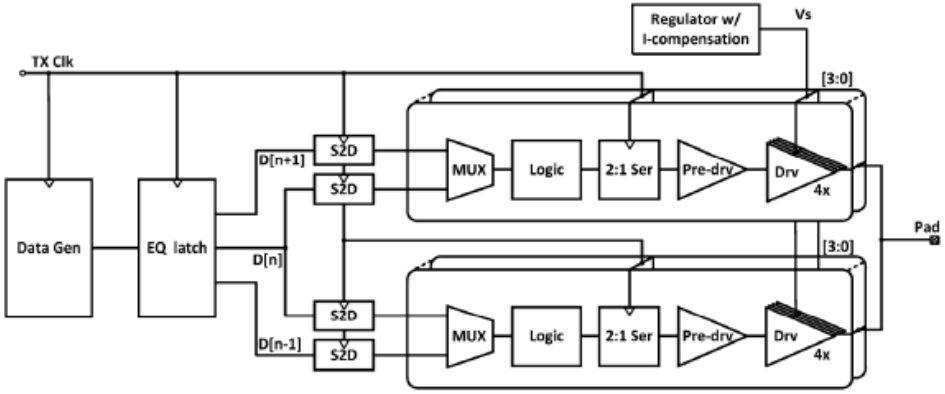
Claim 2	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

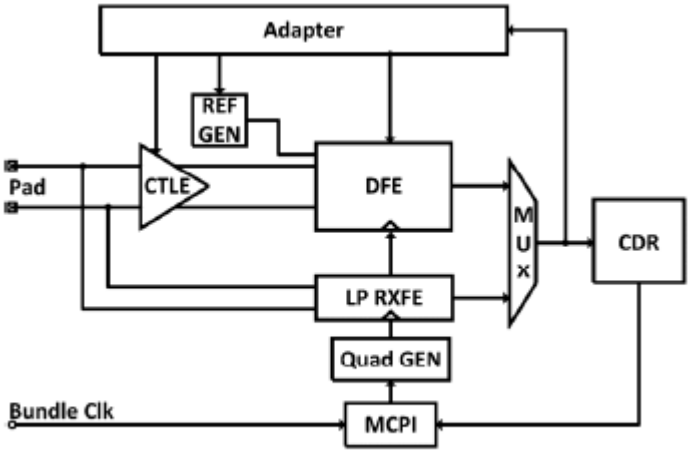
Claim 2	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 2	Disclosure
	 (a)  (b) Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 2	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

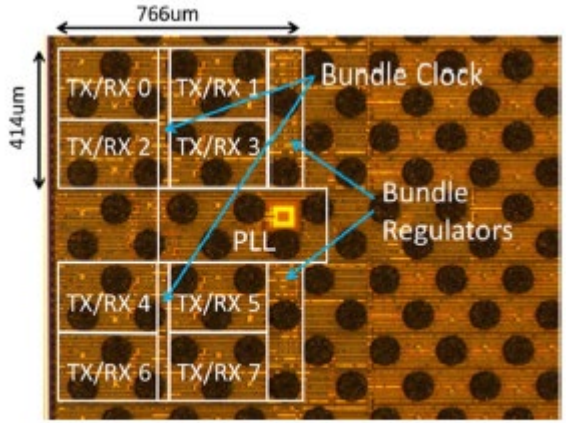
Claim 2	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 2	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 2	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

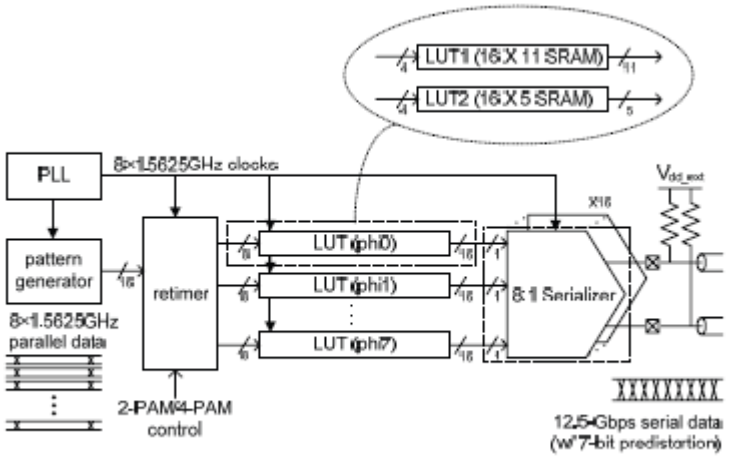
Claim 2	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 2	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 2	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 2	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 2	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 2	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 2	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 2	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 2	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 2	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 2	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 2	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 2	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 2	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 2	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 2	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 2	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 2	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

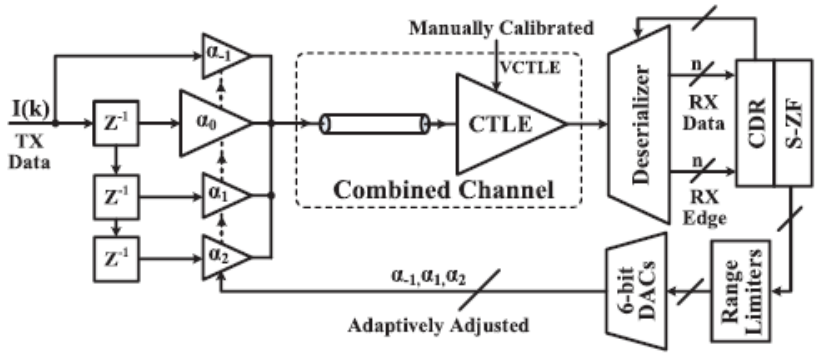
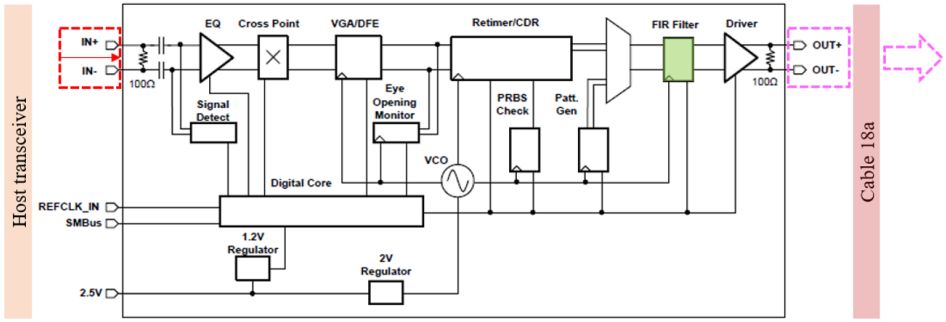


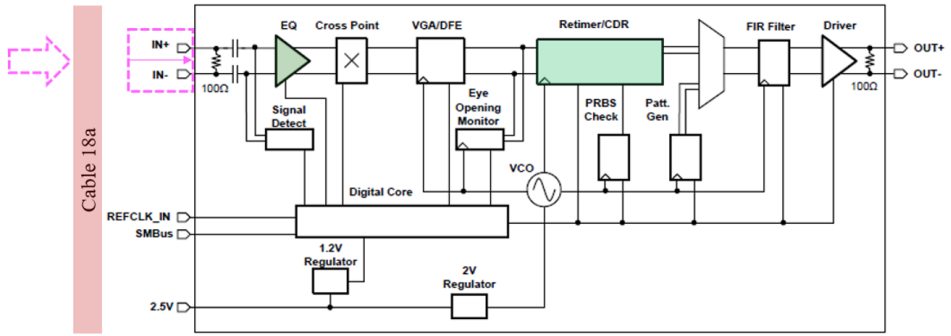
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

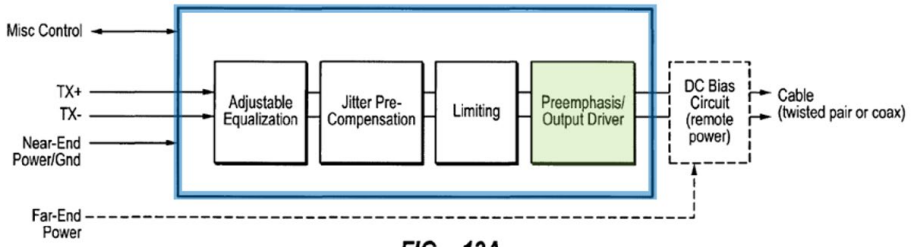
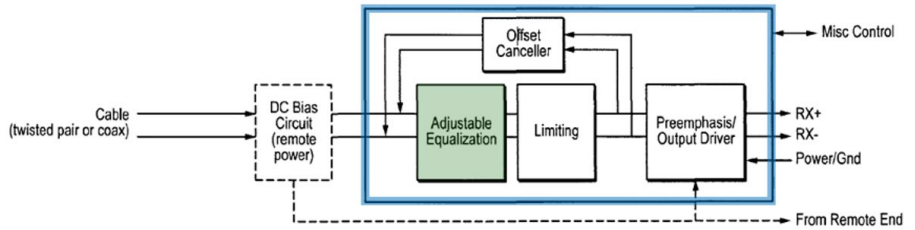
Claim 2	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

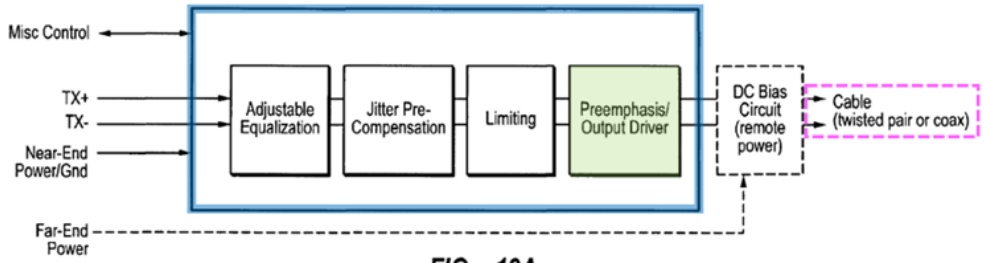
Claim 2	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The link activation module 204 is configured to determine a total insertion loss for the connection with the remote host based on the local host loss, the remote host loss, and cable loss. The link activation module 204 compares the total insertion loss to a FEC limit and to a specification limit. The link activation module 204 may bring up the communication link with the link partner without FEC enabled if the total insertion loss is below the specification limit and below the FEC limit. Additionally, the link activation module 204 may bring up the communication link with the link partner with FEC enabled if the total insertion loss is below the specification limit but not below the FEC limit. Further, the link activation module 204 may not bring up the communication link with the link partner if the total insertion loss is not below the specification limit (e.g., the link activation module 204 may keep the communication link down or bring the communication link down)." Lusted, paragraph 24.

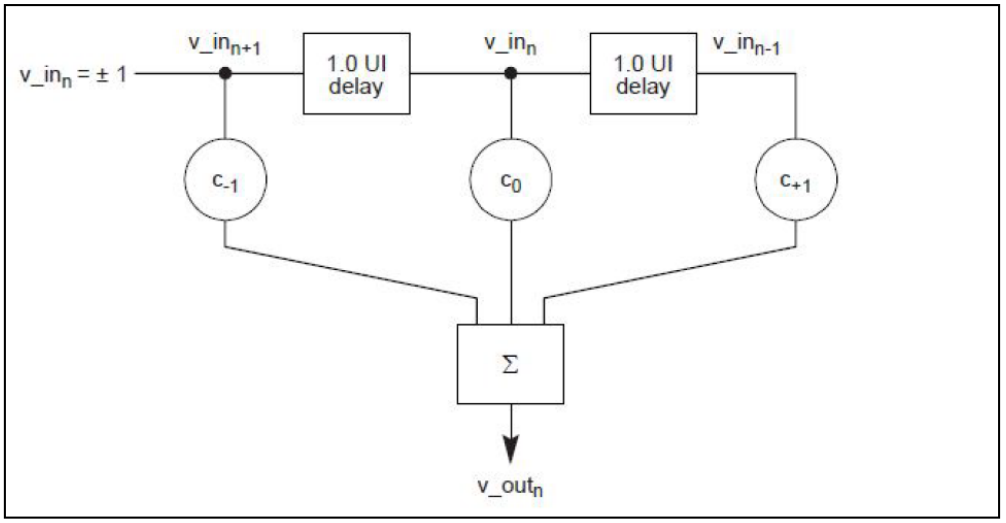
Claim 2	Disclosure
	"The PCS 110 is configured to encode Ethernet frame data received from the MAC 112 into encoded data blocks that may be transmitted by the PMD/PMA 106, and to decode data received from the PMD/PMA 106 into decoded Ethernet frame data that may be processed by the MAC 112. The PCS 110 may encode and distribute the data blocks over one or more logical PCS lanes. The PCS 110 may encode data for transmission over the communication lanes 102 for example, to improve communication efficiency. For example, encoding the data may add timing or synchronization symbols, align the data, add state transitions to the encoded data to improve clock recovery, adjust the DC balance of the data signal, or otherwise prepare the encoded data for serial transmission. The PCS 110 may be capable of encoding or decoding the data using a 64b/66b line code in which 64-bit blocks of data are encoded into 66-bit blocks of encoded data, and vice versa." Lusted, paragraph 20. "The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage." Ikeda, 7:44-55. "FIG. 9 is a block diagram of still another example of a configuration of the second embodiment of the active connector according to the present invention. An active connector 107 illustrated in FIG. 9 differs from the active connector 106 illustrated in FIG. 8 in that the connector base 20 of the active connector 107 further includes a clock recovery circuit (CDR circuit) that recovers the timing of the input signal and reclocks the signal with an optimal timing at each time slot. More specifically, as illustrated in FIG. 9, after an input signal P32 supplied from the coaxial cable transmission line to the external port 30 is supplied to the matching circuit 210, the signal from the matching circuit 210 is supplied to the equalizing circuit 216 and then to a clock recovery circuit 218. Next, the output from the clock recovery circuit 218 is supplied to the buffer circuit 214, and then the output signal P12 is supplied from the buffer circuit 214 through the matching circuit 212 to the internal port 10. The clock recovery circuit 218 is driven by direct-current

Claim 2	Disclosure
	voltage Vcc supplied from an electrical power source (not shown) to a power supply terminal 12." Ikeda, 10:20-38. *DS125DF1610 Retimer Publication* The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610's FIR filter) and the CDR performed on the electrical input signal (by the DS125DF1610's EQ). DS125DF1610's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See id.* at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit signal."  Figure 2. DS125DF1610 Simplified Data Path Diagram

Claim 2	Disclosure
	 **Figure 2. DS125DF1610 Simplified Data Path Diagram** Aronson discloses cable-side equalization and pre-equalization that use cable-dependent parameters to address cable-side losses. *See, e.g.*, Aronson, 14:33-43, 15:1-8. Aronson's transmitter IC's line-side pre-emphasis/output driver overcomes "loss on the cable" using cable-dependent parameters that "match the particular length [and/or] the characteristics of the copper cabling." *See id*. at 14:33-43, Fig. 12A (below). Similarly, Aronson's receiver IC equalizes received line-side signals to "compensat[e] for the cable" losses using cable-dependent parameters based on "cable length and characteristics." *See id*. at 15:1-8, Fig. 12B (below).

Claim 2	Disclosure
	 *FIG. 12A*  *FIG. 12B* Using "cable dependent" parameters for equalization would have been the conventional and obvious way to address losses over the cable. *See, e.g.*, Aronson at 14:33-43 (pre-emphasis/output driver performs pre-equalization to overcome "loss on the cable" using cable-dependent parameters that "match the particular length [and/or] the characteristics of the copper cabling"), Fig. 12A (below).

Claim 2	Disclosure
	 *FIG. 12A*

Claim 2	Disclosure
	 **Figure 22 The PCIe 3.0 Tx Equalization FIR filter representation. (Note: The 10G-KR Filter is similar in definition).** This PCIe 3.0 TxEQ adaptation [10] protocol has 4 phases, defined as follows:- Samaan, p. 25.
2[b] the clock and data recovery performed on the electrical transit signal.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: `Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers.` CMIS, 1.

Claim 2	Disclosure
	1.4.4 MgmtInit State The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp. CMIS, 22.

Claim 2	Disclosure
	1.5.4 Control Set Overview A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 2	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 2	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 2	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 2	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 2	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 2	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

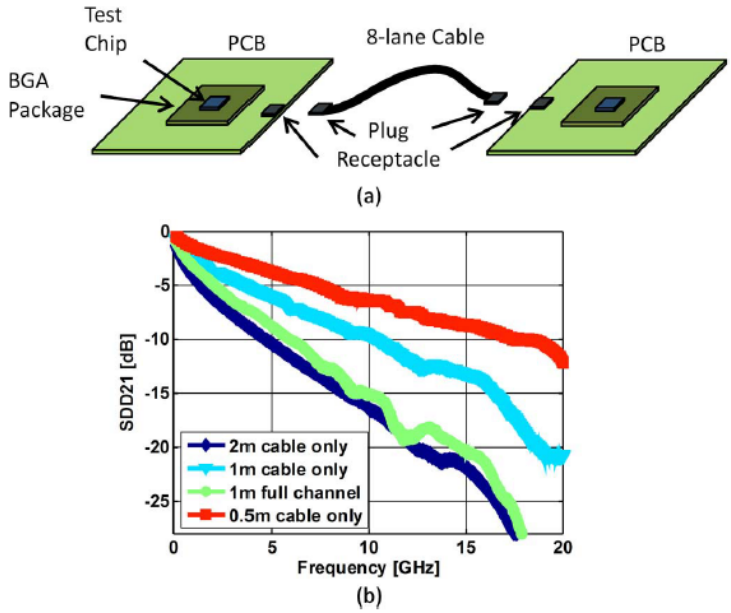
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

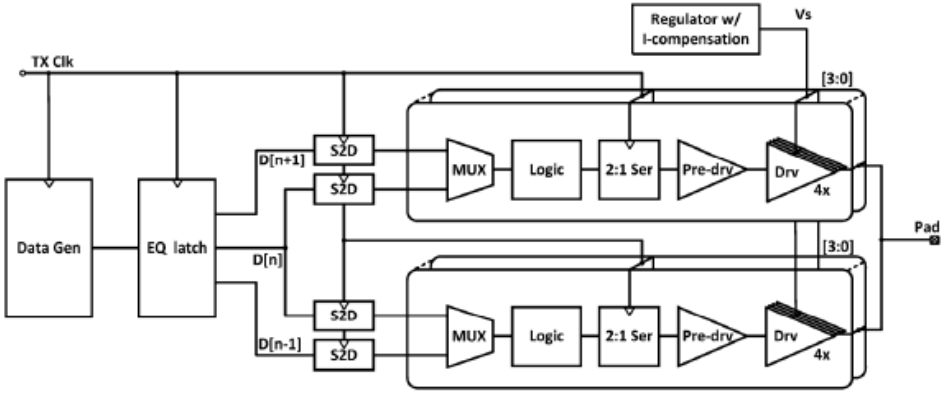
Claim 2	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

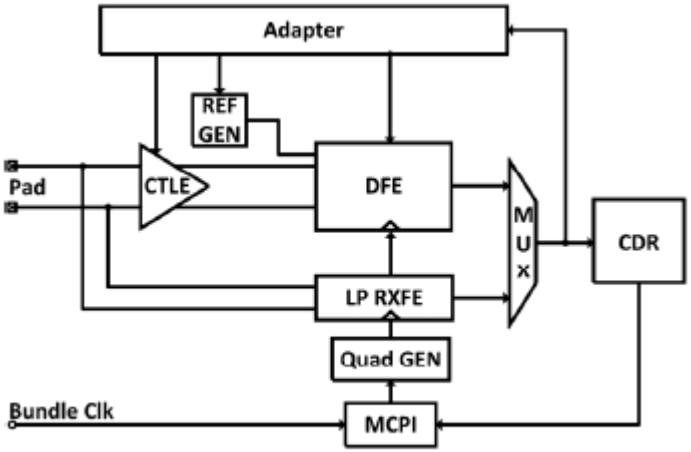
Claim 2	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 2	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 2	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

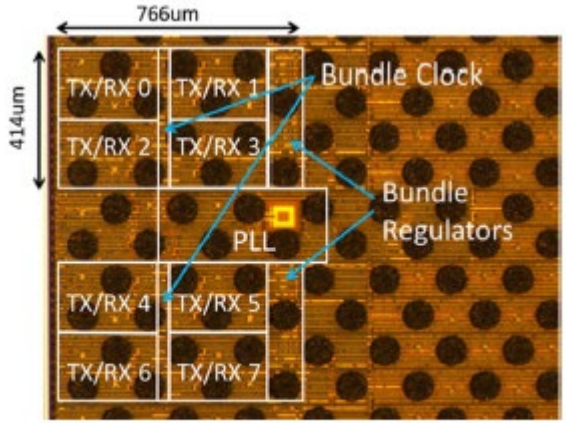
Claim 2	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 2	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 2	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

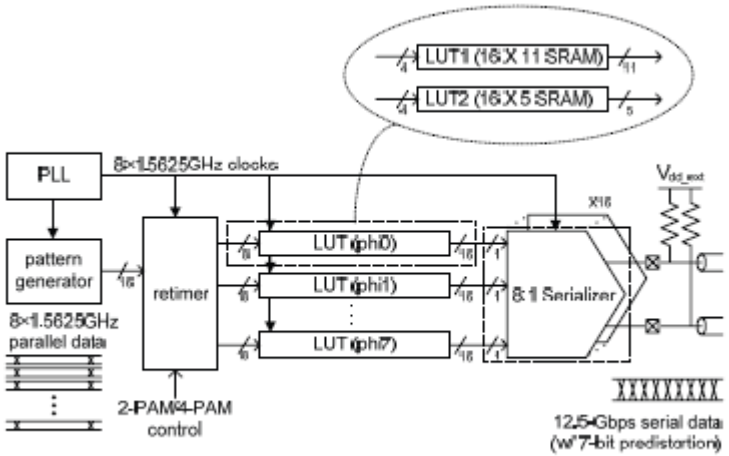
Claim 2	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 2	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 2	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 2	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 2	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 2	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 2	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 2	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 2	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 2	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 2	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 2	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 2	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 2	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 2	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 2	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 2	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 2	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

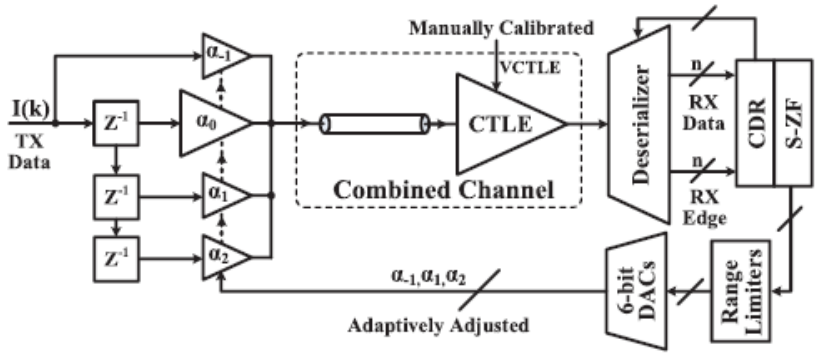
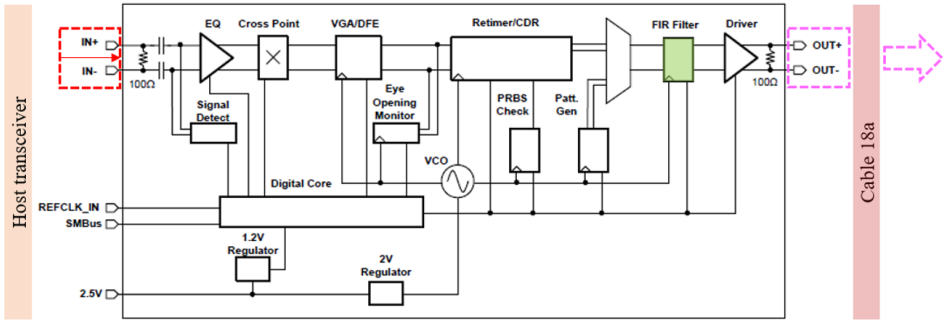
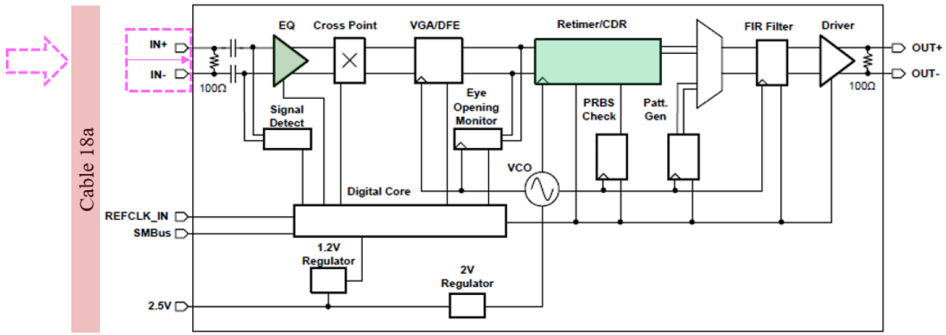


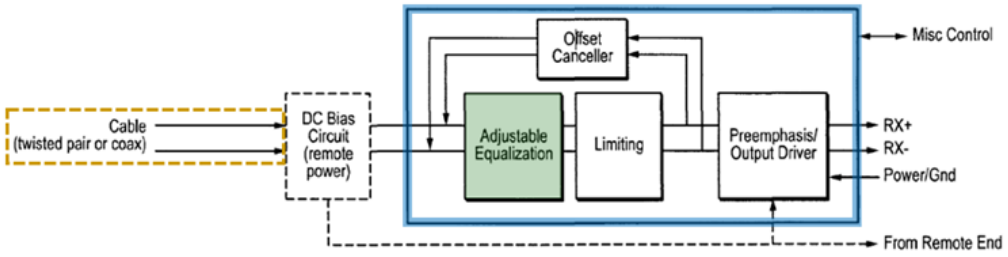
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

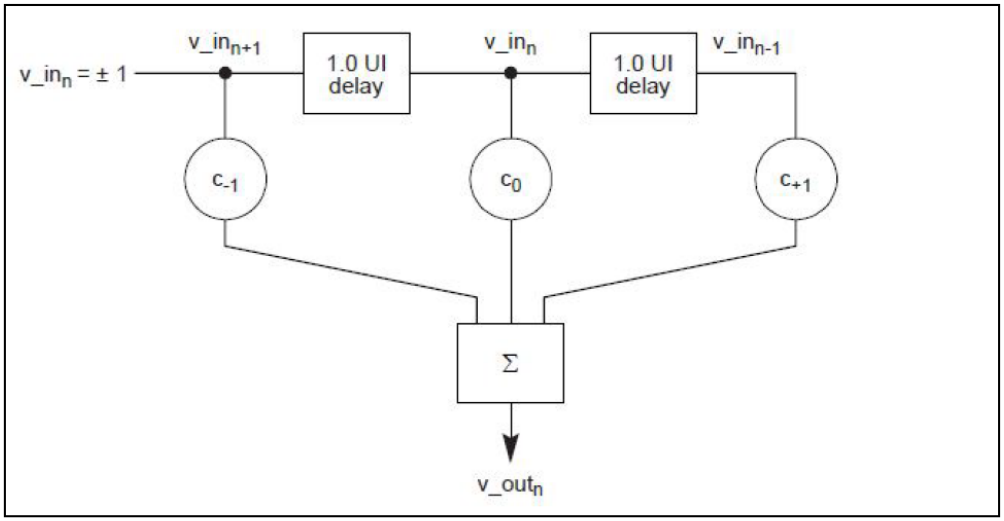
Claim 2	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 2	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The PCS 110 is configured to encode Ethernet frame data received from the MAC 112 into encoded data blocks that may be transmitted by the PMD/PMA 106, and to decode data received from the PMD/PMA 106 into decoded Ethernet frame data that may be processed by the MAC 112. The PCS 110 may encode and distribute the data blocks over one or more logical PCS lanes. The PCS 110 may encode data for transmission over the communication lanes 102 for example, to improve communication efficiency. For example, encoding the data may add timing or synchronization symbols, align the data, add state transitions to the encoded data to improve clock recovery, adjust the DC balance of the data signal, or otherwise prepare the encoded data for serial transmission. The PCS 110 may be capable of encoding or decoding the data using a 64b/66b line code in which 64-bit blocks of data are encoded into 66-bit blocks of encoded data, and vice versa." Lusted, paragraph 20.

Claim 2	Disclosure
	"FIG. 9 is a block diagram of still another example of a configuration of the second embodiment of the active connector according to the present invention. An active connector 107 illustrated in FIG. 9 differs from the active connector 106 illustrated in FIG. 8 in that the connector base 20 of the active connector 107 further includes a clock recovery circuit (CDR circuit) that recovers the timing of the input signal and reclocks the signal with an optimal timing at each time slot. More specifically, as illustrated in FIG. 9, after an input signal P32 supplied from the coaxial cable transmission line to the external port 30 is supplied to the matching circuit 210, the signal from the matching circuit 210 is supplied to the equalizing circuit 216 and then to a clock recovery circuit 218. Next, the output from the clock recovery circuit 218 is supplied to the buffer circuit 214, and then the output signal P12 is supplied from the buffer circuit 214 through the matching circuit 212 to the internal port 10. The clock recovery circuit 218 is driven by direct-current voltage Vcc supplied from an electrical power source (not shown) to a power supply terminal 12." Ikeda, 10:20-38. *DS125DF1610 Retimer Publication* The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610's FIR filter) and the CDR performed on the electrical input signal (by the DS125DF1610's EQ). DS125DF1610's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See id.* at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit signal."

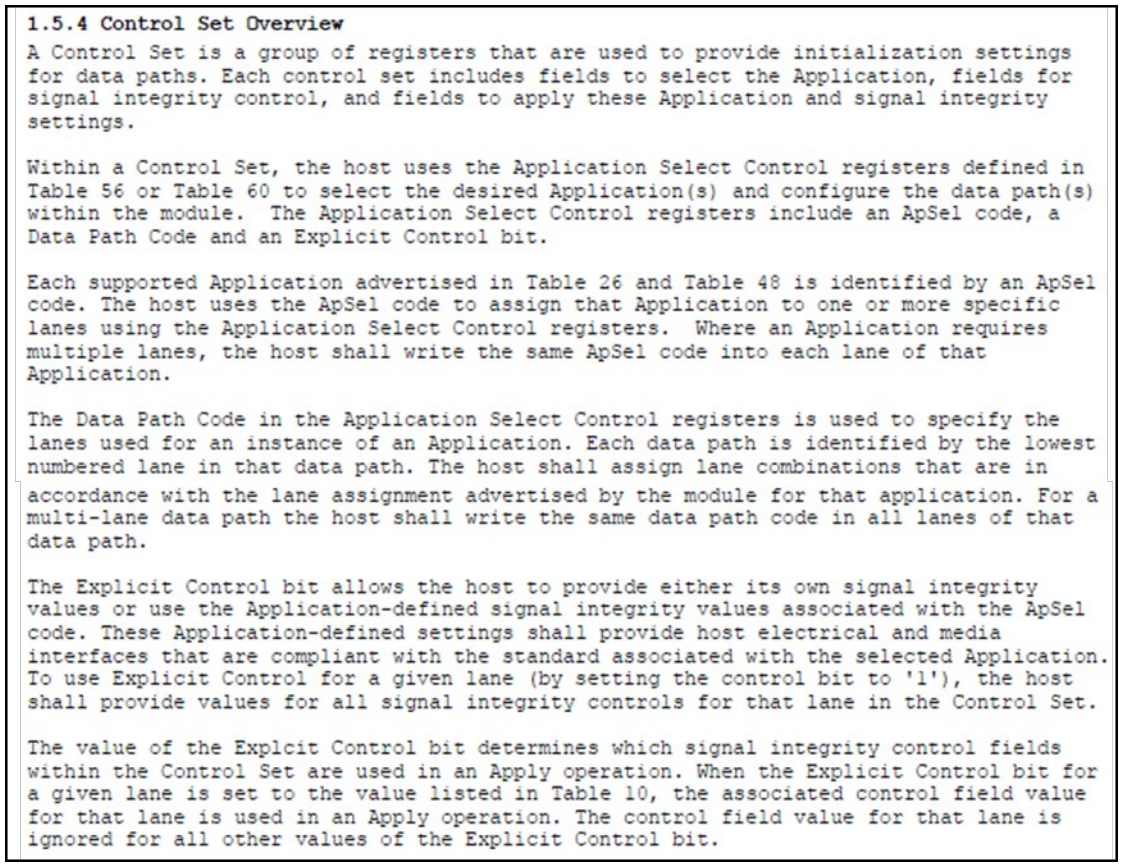
Claim 2	Disclosure
	 Figure 2. DS125DF1610 Simplified Data Path Diagram  Figure 2. DS125DF1610 Simplified Data Path Diagram Using "cable dependent" parameters for equalization would have been the conventional and obvious way to address losses over the cable. Aronson at 15:1-8 (equalization "compensate[s] for the cable" losses using cable dependent parameters based on "cable length and characteristics"), Fig. 12B (below).

Claim 2	Disclosure
	 *FIG. 12B*

Claim 2	Disclosure
	 **Figure 22 The PCIe 3.0 Tx Equalization FIR filter representation. (Note: The 10G-KR Filter is similar in definition).** This PCIe 3.0 TxEQ adaptation [10] protocol has 4 phases, defined as follows:- Samaan, p. 25.

C. DEPENDENT CLAIM 3

Claim 3	Disclosure
3. The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters adapt during usage of the Ethernet cable.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp.

Claim 3	Disclosure
	CMIS, 22.  **1.5.4 Control Set Overview** A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 3	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 3	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 3	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 3	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 3	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 3	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

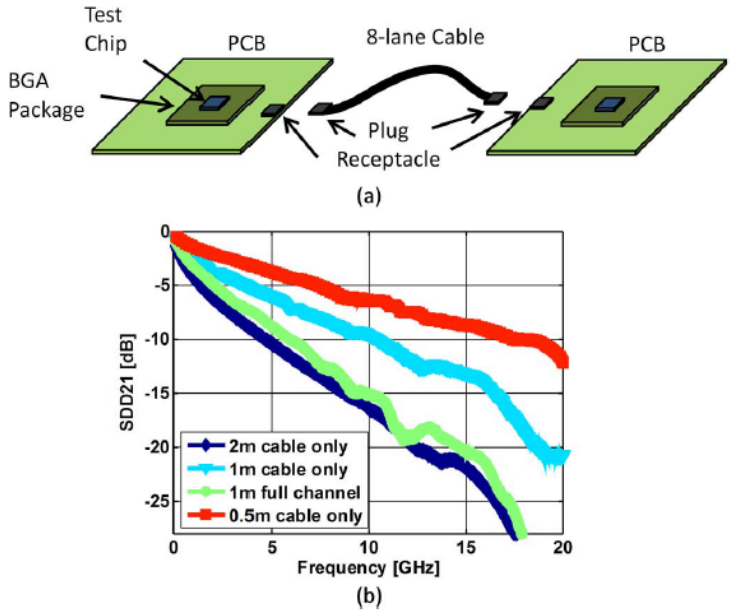
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

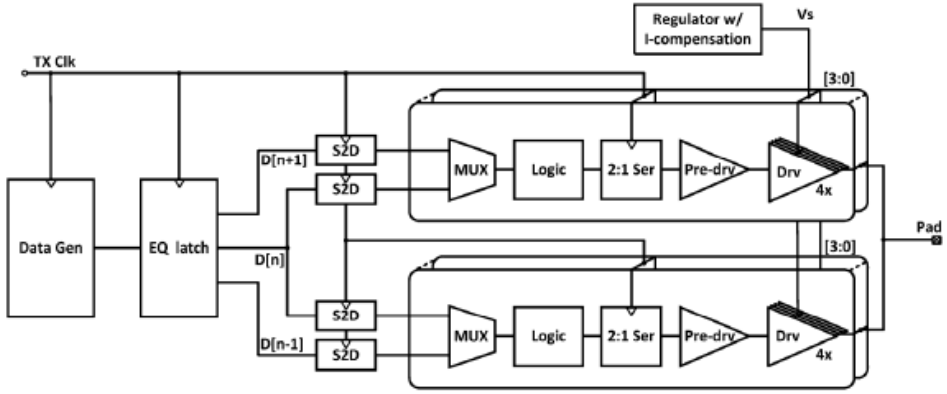
Claim 3	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

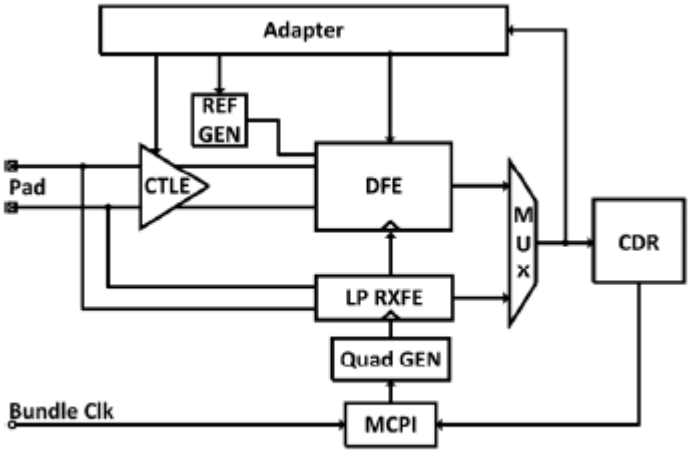
Claim 3	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 3	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 3	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

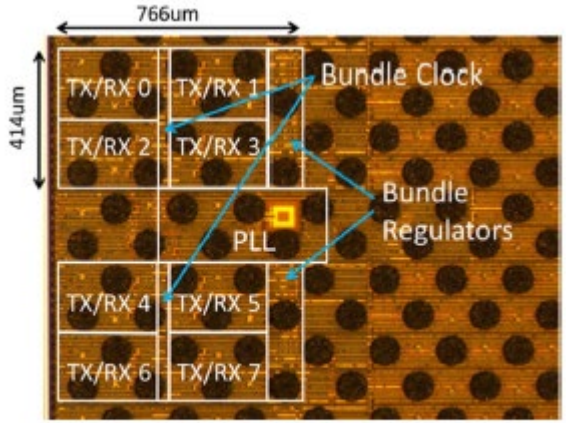
Claim 3	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 3	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 3	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

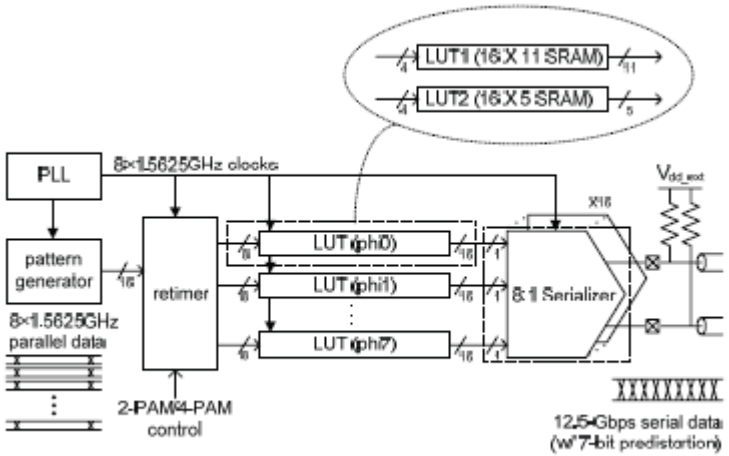
Claim 3	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 3	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 3	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 3	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 3	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 3	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 3	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 3	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 3	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 3	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 3	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 3	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 3	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 3	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 3	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 3	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 3	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 3	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

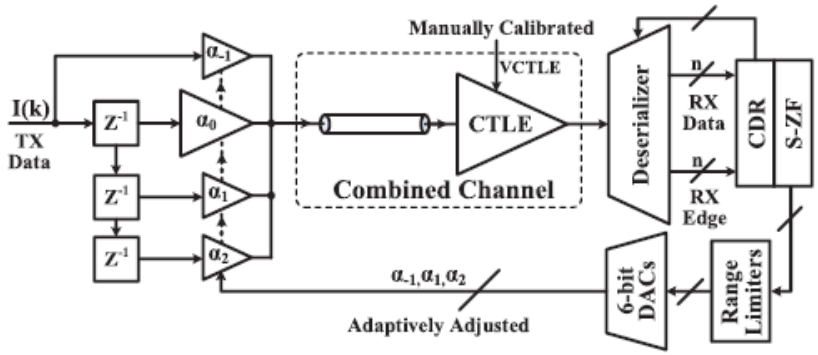
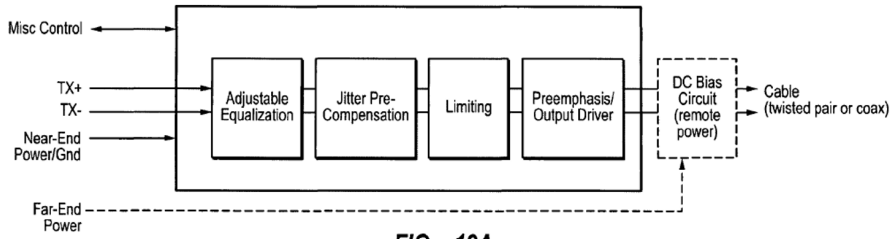
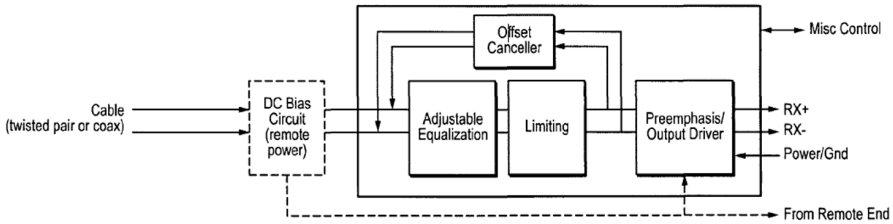
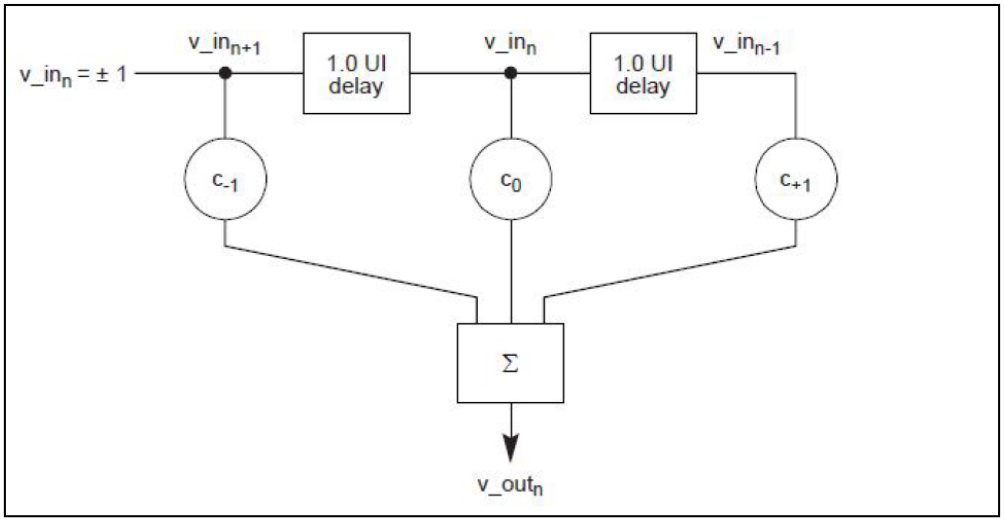


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 3	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 3	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage." Ikeda, 7:44-55. *U.S. Patent No. 7,762,727 to Aronson*

Claim 3	Disclosure
	Aronson discloses an active cable for high-speed transmissions between network nodes. See, e.g., Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.  *FIG. 12A*  *FIG. 12B* Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23. Aronson discloses that cable-dependent equalization parameters used for cable-side equalization and pre-

Claim 3	Disclosure
	equalization, respectively (*see, e.g.*, claim 2), are adapted during usage of the Ethernet cable. *See, e.g.*, Aronson at 15:1-8, Figs. 12A-12B.  **Figure 22 The PCIe 3.0 Tx Equalization FIR filter representation. (Note: The 10G-KR Filter is similar in definition).** This PCIe 3.0 TxEQ adaptation [10] protocol has 4 phases, defined as follows:- Samaan, p. 25.

D. DEPENDENT CLAIM 4

Claim 4	Disclosure
4[a] The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp.

Claim 4	Disclosure
	CMIS, 22. **1.5.4 Control Set Overview** A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 4	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 4	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 4	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 4	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 4	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value / Bit pattern / Output Amplitude 0 / 0000 / 100-400 mV (P-P) 1 / 0001 / 300-600 mV (P-P) 2 / 0010 / 400-800 mV (P-P) 3 / 0011 / 600-1200 mV (P-P) 4-14 / 0100-1110 / Reserved 15 / 1111 / Custom CMIS, 41.

Claim 4	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

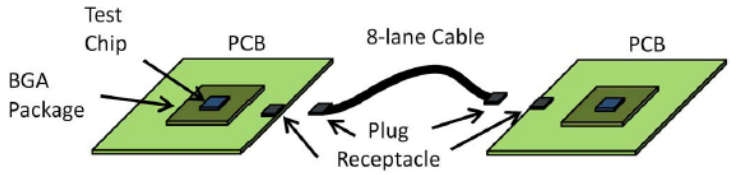
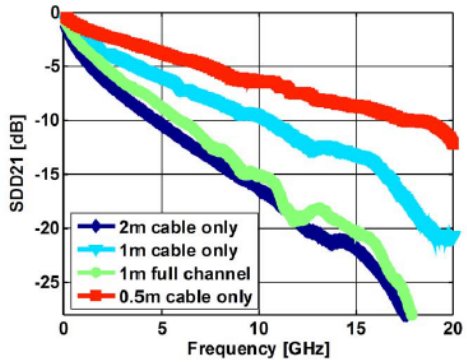
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

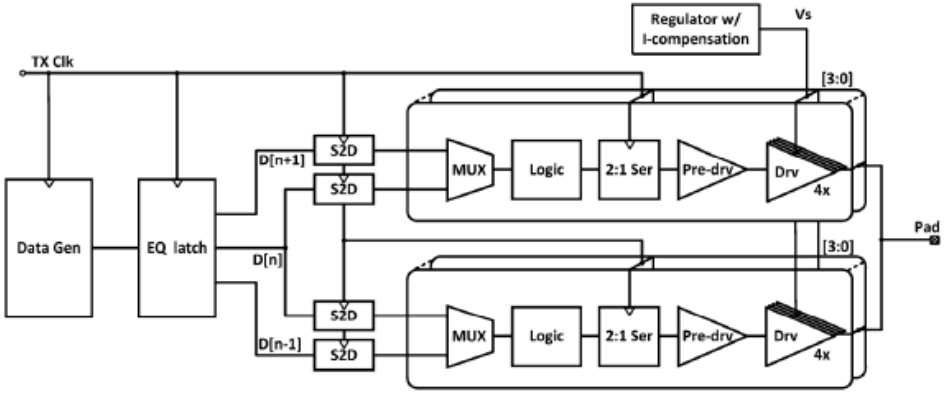
Claim 4	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

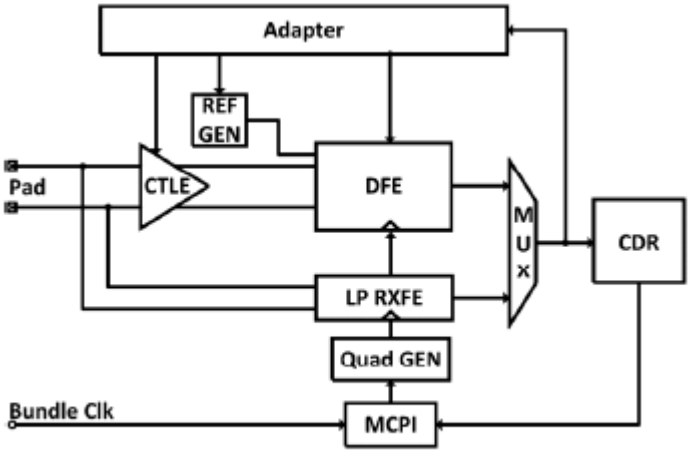
Claim 4	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 4	Disclosure
	 (a)  (b) Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 4	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

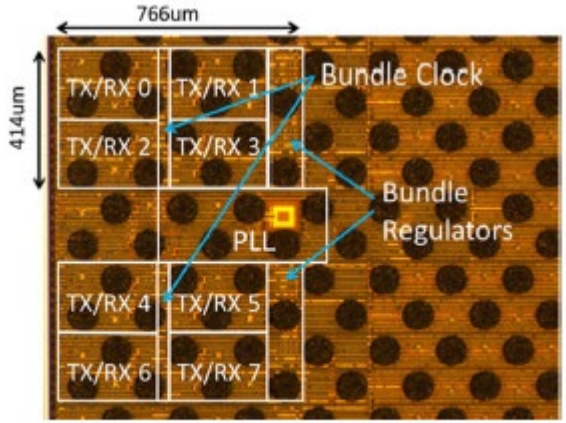
Claim 4	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 4	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 4	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

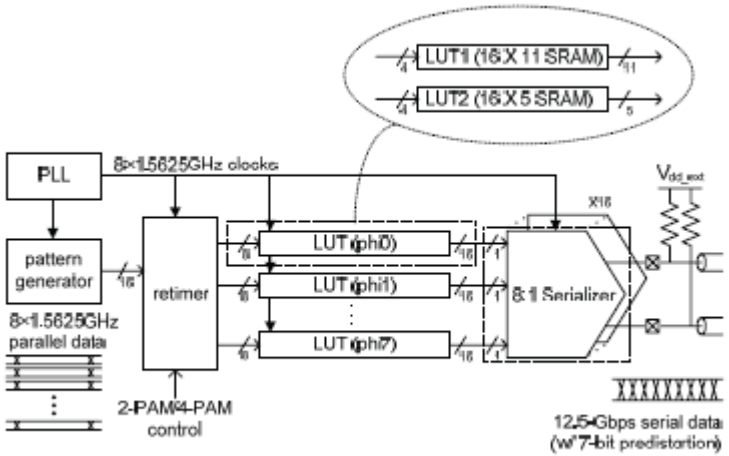
Claim 4	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 4	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 4	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 4	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 4	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 4	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 4	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 4	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 4	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 4	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 4	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 4	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 4	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 4	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 4	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 4	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 4	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 4	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

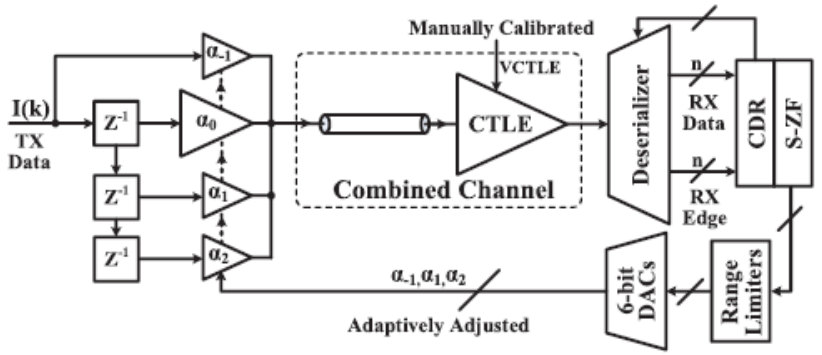
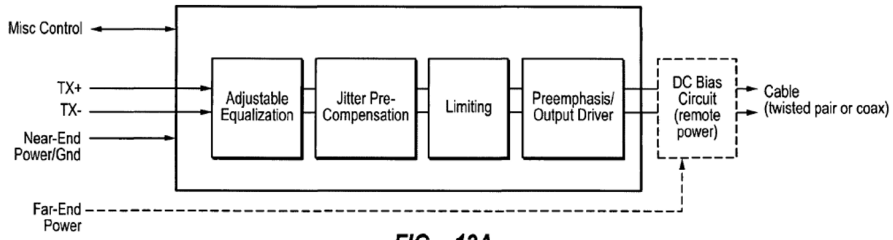
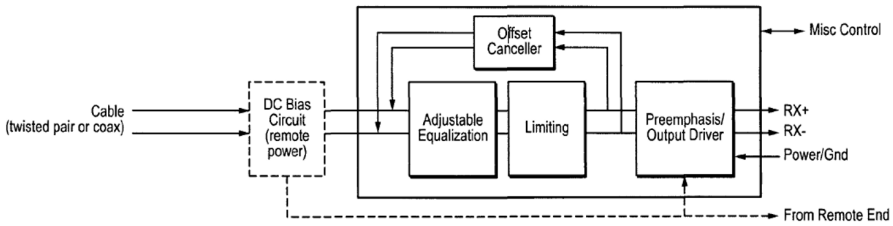


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 4	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 4	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. *U.S. Patent No. 7,762,727 to Aronson* Aronson discloses an active cable for high-speed transmissions between network nodes. See, e.g., Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.

Claim 4	Disclosure
	 *FIG. 12A*  *FIG. 12B* Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23. Aronson discloses that cable-dependent equalization parameters used for cable-side equalization and pre-equalization, respectively (*see, e.g.*, claim 2), are fixed during normal usage of the Ethernet cable. *See, e.g.*, Aronson at 14:35-39, 15:4-8, 15:21-23 (describing factory-set cable-dependent equalization parameters).

Claim 4	Disclosure
4[b] wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp. CMIS, 22.

Claim 4	Disclosure
	1.5.4 Control Set Overview A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 4	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 4	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 4	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 4	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 4	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value / Bit pattern / Output Amplitude 0 / 0000 / 100-400 mV (P-P) 1 / 0001 / 300-600 mV (P-P) 2 / 0010 / 400-800 mV (P-P) 3 / 0011 / 600-1200 mV (P-P) 4-14 / 0100-1110 / Reserved 15 / 1111 / Custom CMIS, 41.

Claim 4	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

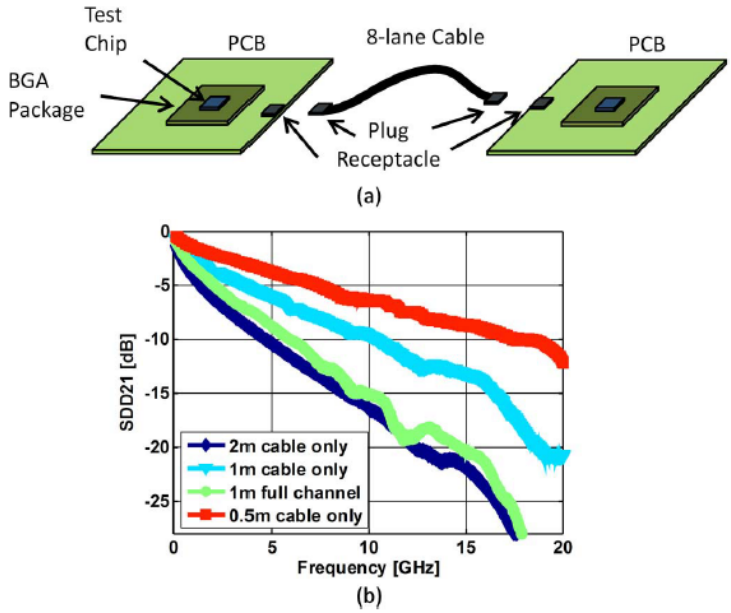
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

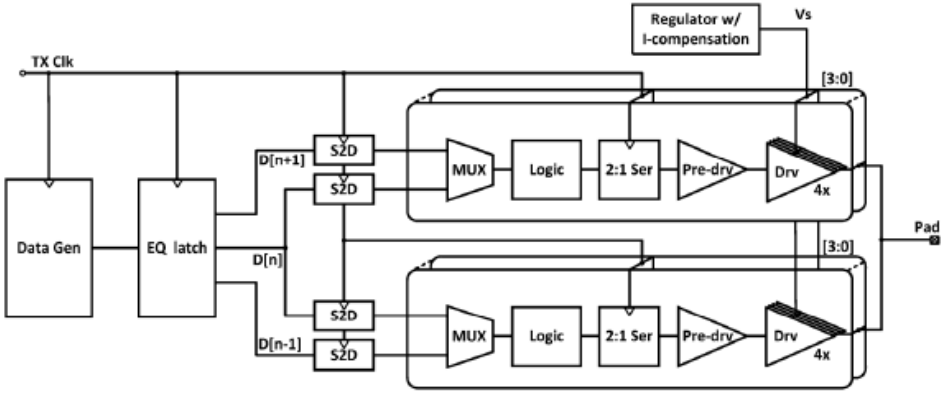
Claim 4	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

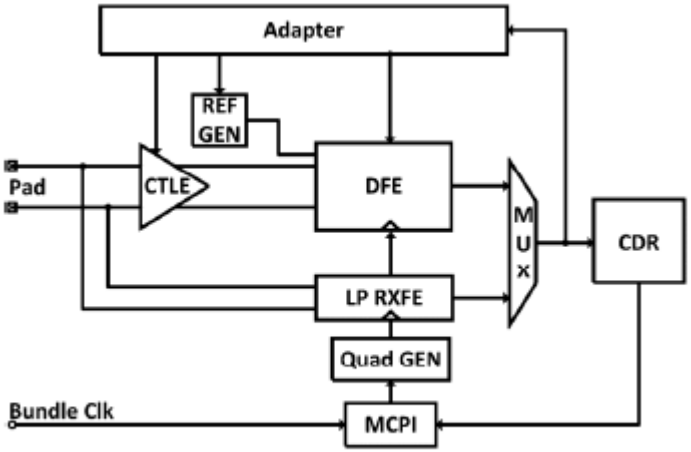
Claim 4	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 4	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 4	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

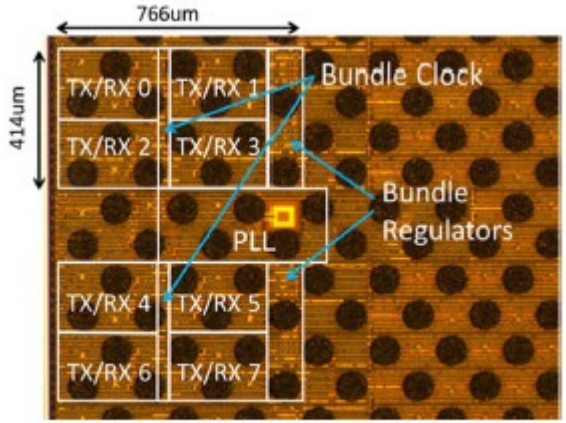
Claim 4	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 4	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 4	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

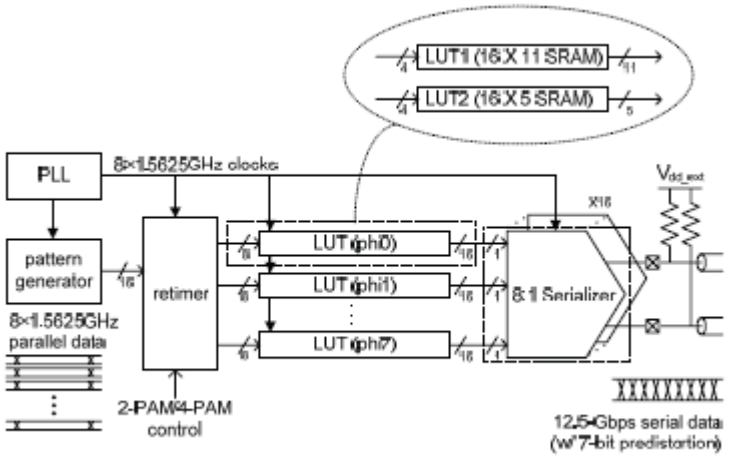
Claim 4	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 4	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 4	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 4	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 4	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 4	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 4	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 4	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 4	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 4	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 4	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 4	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 4	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 4	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 4	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 4	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 4	Disclosure
	III. RECEIVER CHIP *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 4	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

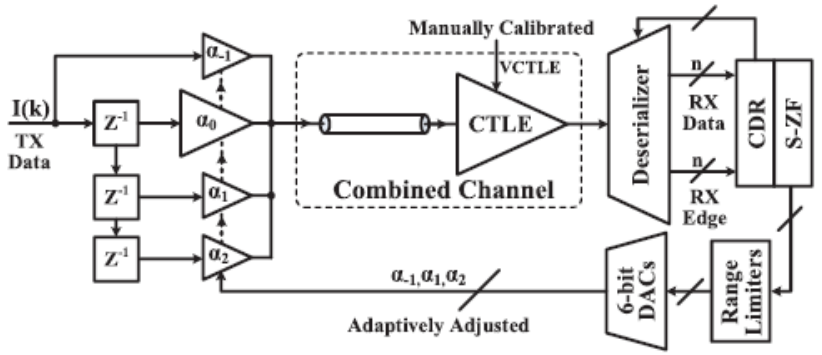
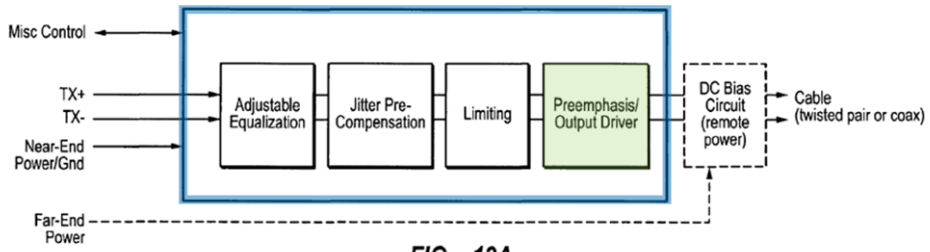
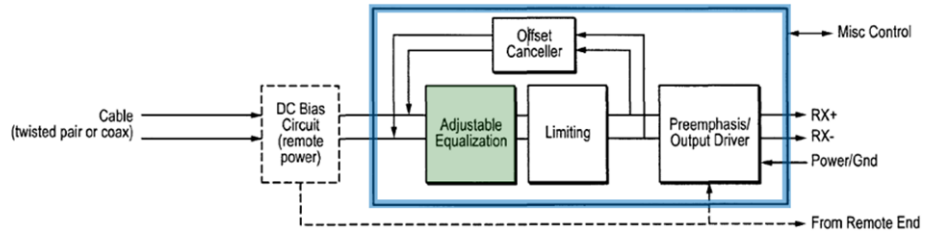


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 4	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 4	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage." Ikeda, 7:44-55.

Claim 4	Disclosure
	U.S. Patent No. 7,762,727 to Aronson One obvious way to implement the equalization coefficients used by a FIR filter and an equalizer is during manufacturing-testing. *See, e.g.*, Aronson at 14:35-39 (Fig. 12A's pre-equalization parameters for transit over the line-side are "adjusted at factory setup"), 15:1-8 (Fig. 12B's equalization may be "fixed" or "adjustable but factory set" "at the time of the cable manufacture").  *FIG. 12A*  *FIG. 12B* Aronson discloses that cable-dependent equalization parameters used for cable-side equalization and pre-equalization, respectively (*see, e.g.*, claim 2), are fixed during normal usage of the Ethernet cable. *See, e.g.*, Aronson at 14:35-39, 15:4-8, 15:21-23 (describing factory-set cable-dependent equalization parameters).

E. DEPENDENT CLAIM 5

Claim 5	Disclosure
5. The active Ethernet cable of claim 4, wherein the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: ***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** ***Index Terms*—Active inductor CTLE, bidirectional link, collaborative CDR, conditional phase detection, decision-feedback equalizer (DFE), phase error decimation, regulated CMOS clocking, source-series terminated (SST) driver.** Musah, 3079.

Claim 5	Disclosure
	II. LINK ARCHITECTURE The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 5	Disclosure
	IV. MEASUREMENTS Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. The measured TX output is shown in Fig. 16 at 32 Gb/s operation over a short channel. Fig. 17 shows the on-die 10^{-10} BER eye at 32 Gb/s over a 0.5 m cable using PRBS10 data on a single lane. Amortizing the PLL and clock distribution power over 4 lanes, the link power consumption is 205 mW at 32 Gb/s. Transceiver power efficiency given for multiple data rates from 4 to 32 Gb/s is shown in Fig. 18. Excluding the PLL power, the transceiver power efficiency ranges from 3.4 to 5.7 pJ/b, while equalizing 24 dB and 16 dB of Nyquist rate channel loss at 16 Gb/s and 32 Gb/s, respectively. Due to circuit BW limitations, the equalized channel loss tolerance is 24 dB up to 27 Gb/s and reduces to 16 dB at the highest data rate. When the HP RX is disabled and the LP RX is enabled, the measured power efficiencies are 1.0 pJ/b at 4 Gb/s, 1.5 pJ/b at 8 Gb/s and 2.2 pJ/b at 12 Gb/s with 4.5 dB, 8 dB and 10 dB of channel loss, respectively. A breakdown of the link power is shown in Table I, with PLL power amortized over 4 lanes. Musah, 3086.

Claim 5	Disclosure

TABLE II
COMPARISON TABLE

	[1]	[2]	[3]	[4]	This Work	
CMOS technology	32nm	32nm	28nm	40nm	22nm	
Supply voltage [V]	1.2/1.05	1.00	1.5/1.05	0.90	0.90	1.07
Data rate [Gb/s]	28	32	28	28	16	32
Channel loss at Nyquist [dB]	35	30	34	20	24	16
TX FFE	4-tap	4-tap	3-tap	3-tap	3-tap	3-tap
RX DFE	15-tap	15-tap	14-tap	N/A	6-tap	6-tap
RX peaking amplifier	2-stage	2-stage	1-stage	1-stage	1-stage	1-stage
TX output swing [$V_{pp\text{-}diff}$]	0.950			0.6	0.515	0.630
TX output jitter [ps_{rms}]	0.45		0.25	0.2		<0.54
RX input sensitivity [mV]	15		15	27		35
Area density [mm^2/Gb/s]	0.0289	0.0219	0.0298	0.0506	0.0049	0.0025
Transceiver power efficiency per lane [pJ/b]	24.8	21	20	6.96	4.6	6.4

Musah, 3087.

V. CONCLUSION

We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane.

Musah, 3088.

Claim 5	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G

Claim 5	Disclosure
	data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below. Riani, 4:43-5:5. ***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 5	Disclosure
	A. Transmitter Chip Measurement The TX output is measured after a channel consisting of a doubled bonding wire, a 4-cm PCB trace, and a 0.5-m connection cable. Fig. 23(a) shows the over-equalized eye-diagram at 5 Gb/s, where the four sub-levels are contributed by the four FFE taps. Fig. 23(b) and (c) gives the output eye-diagrams at 40 Gb/s before and after applying the four-tap FFE. Obviously, the FFE can significantly improve the eye opening. The eye height and eye width are optimized from 140 mV and 0.45 UI to 180 mV and 0.68 UI, respectively. Meanwhile, the thickness of the eyelid is dramatically reduced from around 330 to 140 mV. Fig. 23(d) shows the properly compensated eye-diagram at the maximum operation speed of 50 Gb/s. Its eye height and eye width are 50 mV and 0.38 UI. Clearly, a wide operation range from 5 to 50 Gb/s is achieved, which is mainly attributed to the multi-MUX-based FFE implementation. Fig. 24 further shows the TX output with four separate eyes. It can be seen that the horizontal eye widths for both fixed clock and PRBS patterns are almost identical, thus proving that the four sampling phases are properly aligned. Zheng, 2972-2973. *B. Receiver Chip Measurement* The RX standalone measurement results are presented in this part. Fig. 25(a) shows the eye-diagram of the 40-Gb/s input data generated by an Anritsu MP1812A through combining four 10-Gb/s PRBS7 sequences, where the single-end eye height and eye width are around 360 mV and 0.71 UI. Fig. 25(b) shows the eye-diagram of the 10-Gb/s recovered

Claim 5	Disclosure
	data with a total jitter of 12.73 ps. The eye-diagrams of the recovered clocks (divided by 2) for the edge sampling and data sampling are shown in Fig. 25(c) and (d), which reveal that the introduced LPFs can optimize the total jitter from 11.48 to 7.66 ps. To demonstrate the effect of the LPFs with adaptively adjusting bandwidth, the jitter transfer (JTRAN) and JTOL curves are measured using a Tektronix BSA286C with a CDR block. The input peak-to-peak swing is tuned to 800 mV and the control voltage of the CTLE is manually set to 710 mV. The JTRAN curves in Fig. 26 illustrate that the bandwidth of the data-sampling path depending on the LPFs is 4 MHz, which is much smaller than 18 MHz for the edge-sampling path determined by the loop parameters. The measured JTOL in Fig. 26 indicates that the embedded LPFs result in a significant dip attenuation around the corner frequency and improve the JTOL amplitudes apparently at high jitter frequencies. Meanwhile, the adaptively adjusting bandwidth of the LPFs makes them exhibit little effect on the phase-tracking slew rate at low jitter frequencies. Additionally, the corner frequency of the JTOL is about 20 MHz, which is much larger than the JTRAN bandwidth of 4 MHz. Zheng, 2973-2974.

Claim 5	Disclosure

Transmitter Chip				
	[4]	[16]	[20]	This work
Technology (nm)	65	14	65	65
Supply (V)	1.2	N/A	1.2	1.2
Data Rate (Gb/s)	50-64	16-40	38.8-42	5-50
Area (mm^2)	1.2 × 1.0	0.215 × 0.13	0.9 × 0.7	1.2 × 0.5
TX Equalization	4-tap FFE	4-tap FFE	5-tap FFE	4-tap FFE
1UI-Delay Gen.	LC-Delay	Multi-MUX	CML-Delay	Multi-MUX
MUX Type	4:1	4:1	N/A	4:1
Data Jitter RJ (ps_{rms})	N/A	0.33@28Gb/s 0.51@40Gb/s	N/A	0.23@40Gb/s 0.18@50Gb/s
Data Jitter (ps) TJ (BER=1e-12)	N/A	10.72@28Gb/s 12.89@40Gb/s	15.1@40Gb/s	9.90@40Gb/s 10.58@50Gb/s
Power (mW)	199*	518	135**	145*
Energy Efficiency (pJ/bit)	3.1	12.9	3.4	3.6

*Exclude PLL power consumption, ** Standalone FFE without data serializer.

Zheng, 2974.

"FIG. 5 illustrates an EYE waveform of a signal obtained after passing a 56 Gbps PAM-4 signal through a raised cosine filter with a bandwidth of 22 GHz and a roll-off of 0.5. In FIG. 5, when the signal has a value higher than a determination threshold 501, the signal is determined to be +3, when the signal has a value between the determination threshold 501 and a determination threshold 502, the signal is determined to be +1, when the signal has a value between the determination threshold 502 and a determination threshold 503, the signal is determined to be −1, and when the signal has a value lower than the determination threshold 503, the signal is determined to be −3. Ranges above the determination thresholds 501, 502, and 503 through which the signal does not pass is referred to as the EYE widths. As seen in FIG. 5, the EYE width is defined by the upper EYE width 505 and the lower the EYE width 506, and the EYE widths 505 and 506 are defined by the data transition time, −3→+3 and +3→−3. The EYE width is narrowed by approximately 15 ps even under the condition that the bandwidth is limited by a frequency higher than the

Claim 5	Disclosure
	Nyquist frequency and there is almost no influence of ISI. In this manner, the EYE width of the PAM multilevel signal is narrowed relative to that of the NRZ signal due to data pattern dependence." Norimatsu, 4:27-50.

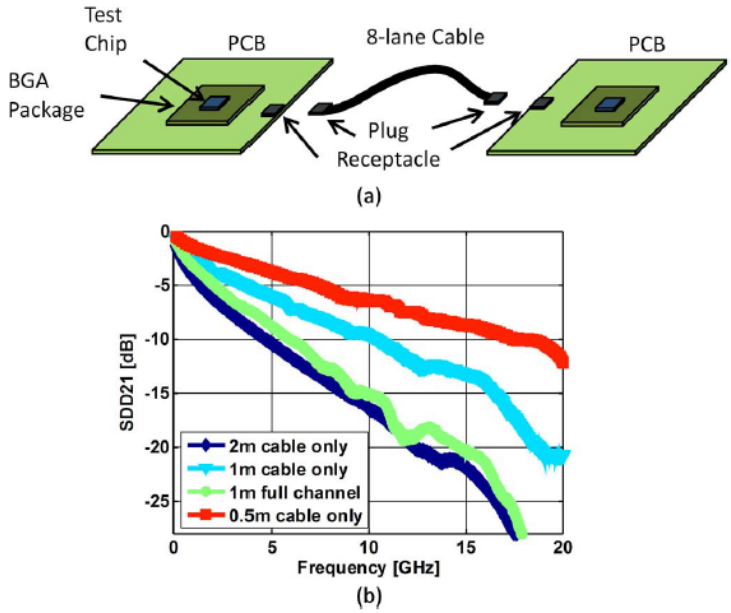
F. INDEPENDENT CLAIM 6

Claim 6	Disclosure
6[pre] A communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: **1.1 Introduction** This specification defines the Common Management Interface Specification (CMIS) for QSFP-DD, OSFP and COBO in order to enable flexible use of modules and cable assemblies (hereafter referred to as modules unless cable assemblies are specifically mentioned) by the user. It shares some similarities with the management interfaces used in other form factors such as QSFP, SFP, and CFP. This specification supports a module with 8 host electrical lanes. Support for modules with more host lanes is possible (in increments of up to 8 lanes) by a bank selection feature (which allows several instances of an adressable page to exist in the paged register map). Due to this new mechanism this specification is not backwards compatible with SFF-8636. Some host ports may support both 4-channel and 8-channel devices; when a 4-channel device is inserted into such a port the appropriate memory map (e.g. SFF-8636) must be used. This case is outside the scope of this document. The host-to-module interactions needed to initialize active modules are presented in two state machines. A module-level state machine defines the initialization of the management interface as well as control of the module-wide power mode. A data path-specific state machine defines the host and module interactions and behaviors needed for power up and initialization of the data path(s) in the module. The CMIS is intended to cover a wide range of possible module functionalities and applications, ranging from cable assemblies to coherent DWDM modules. The CMIS is designed with the intent not to burden the simple cases but to provide a common set of management interactions and a common register map. In some modules, multiplexing of the high speed signals between the host electrical interface and the module media interface may occur in the module. In this specification, all references to lane numbers are based on the electrical connector interface lanes, unless otherwise indicated. In cases where a status or control aspect is applicable only to lanes after multiplexing or demultiplexing has occurred, the status or control is intended to apply to all lanes in the data path, unless otherwise indicated. Symmetry is expected between the Tx and the Rx hardware structure; for example Tx lanes that are multiplexed in the Tx are demultiplexed in the Rx. Each Application selected by the host is applied to the same Tx and Rx host electrical lanes. CMIS, 5-6.

Claim 6	Disclosure
	Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. Table 1 and Table 2 provide a summary of the high-level behaviors and properties of each module state for passive copper cable assembly and active module implementations, respectively. Implementers of passive copper cable assemblies should note that this specification was designed to allow for flat-memory EEPROM implementations for that cable type. Active modules and active cable assemblies shall use the paged memory model. For all module types, refer to sections 1.4.3-1.4.9 for detailed requirements for each state. CMIS, 18.

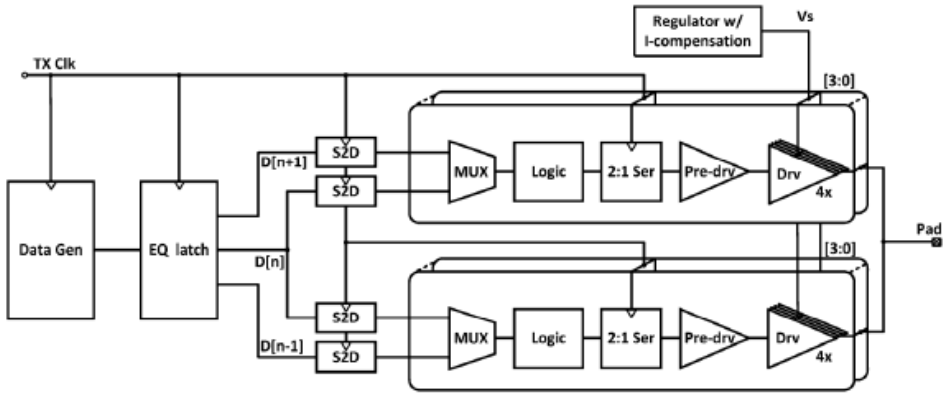
Claim 6	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

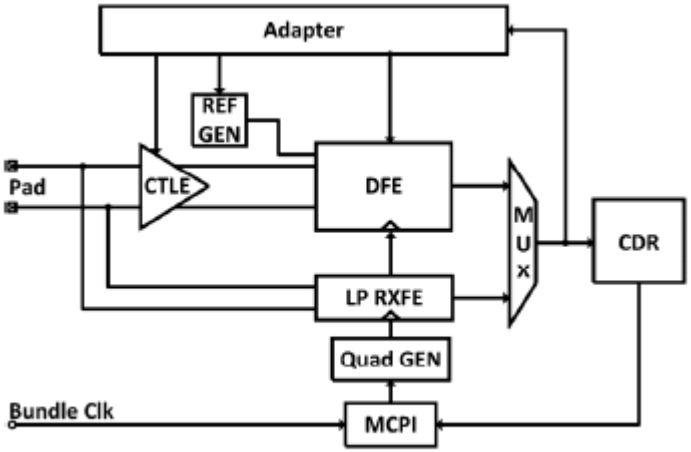
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

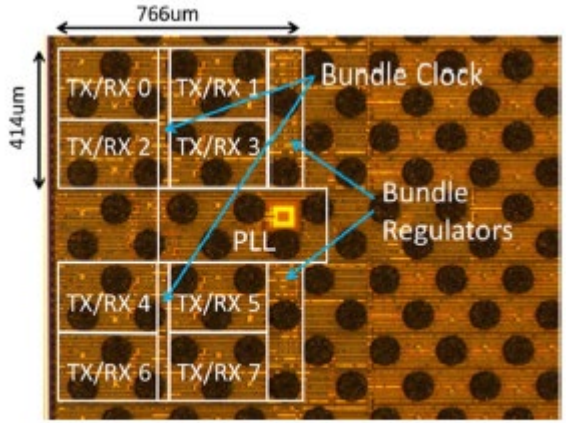
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

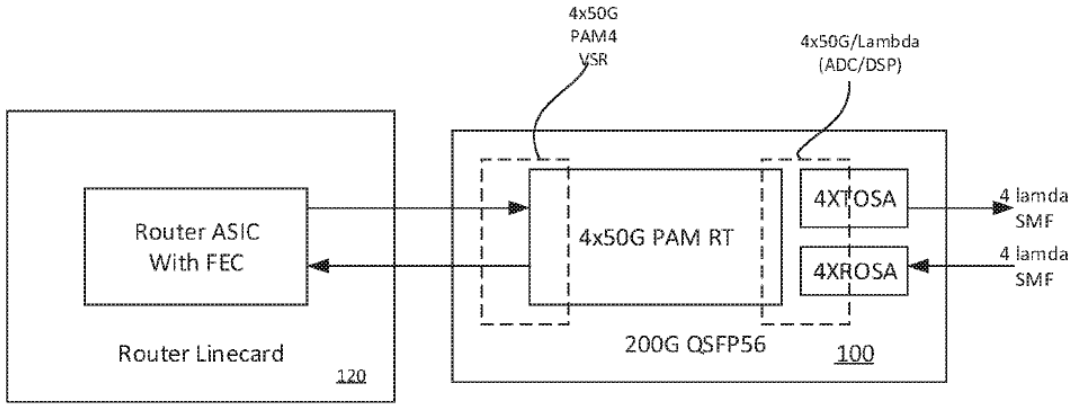
Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

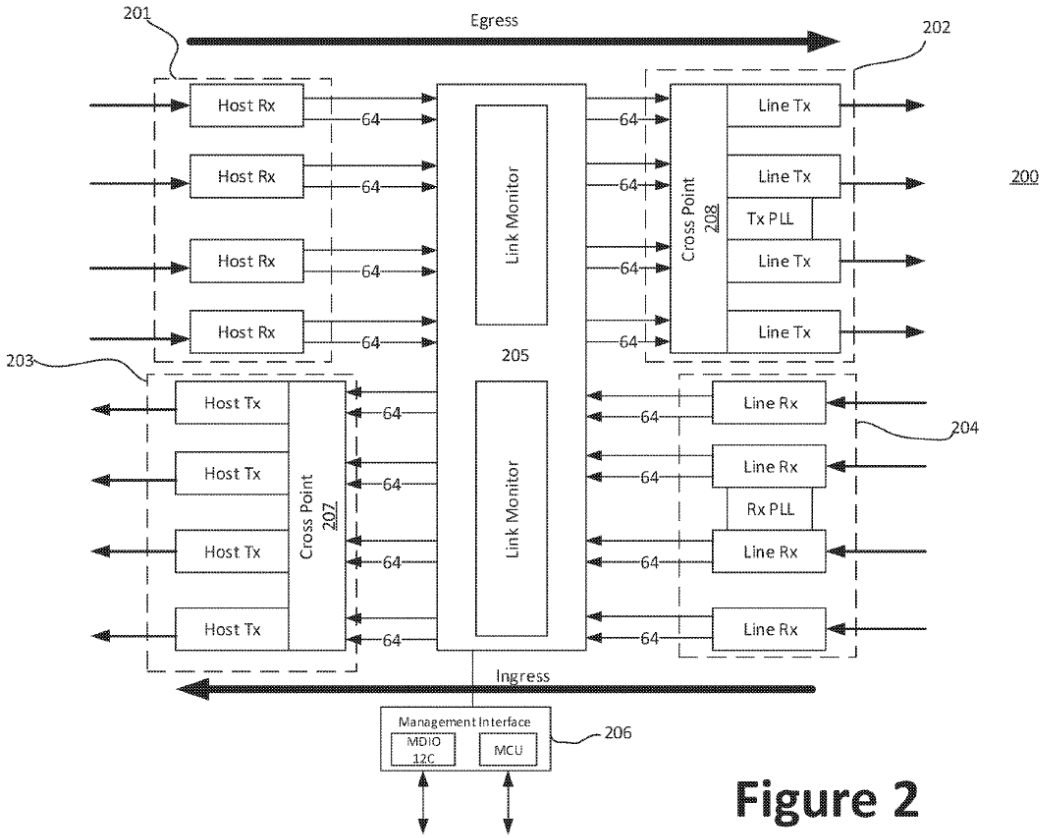
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free $(BER < 10^{-12})$ transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 **Figure 2** Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. ***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	THE exponential growth of cloud computing, social networking, and multimedia sharing has led to an explosive bandwidth demand on data communication in both telecommunication equipment and inter/intra data center [1], [2]. To accommodate to this requirement, the data rate of the wireline serializer/deserializer (SerDes) transceiver has been continuously increased [3]–[5]. Currently, 25–28 Gb/s serial links approved by InfiniBand EDR, 32GFC, and CEI-28G have stepped into the period of industrial deployment [1], [3], [6]. The 38–64 Gb/s transceivers, which will play a key role in the next-generation data rate supported by Ethernet 400GbE, InfiniBand HDR, and CEI-56G, have attracted increasing attentions in the industry and the academia [2], [4], [5], [7]–[11]. The main challenges in designing such high-speed transceivers originate from the ever decreased unit interval (UI) period, which not only poses high bandwidth requests on the blocks located at the critical path, but also makes the link timing budget extremely tight. Moreover, advanced processes cannot completely solve these problems, since the parasitic capacitances/resistances at the high-speed outputs usually do not scale well with the technology due to the bonding and/or electro-static discharge (ESD) protection requirements. Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

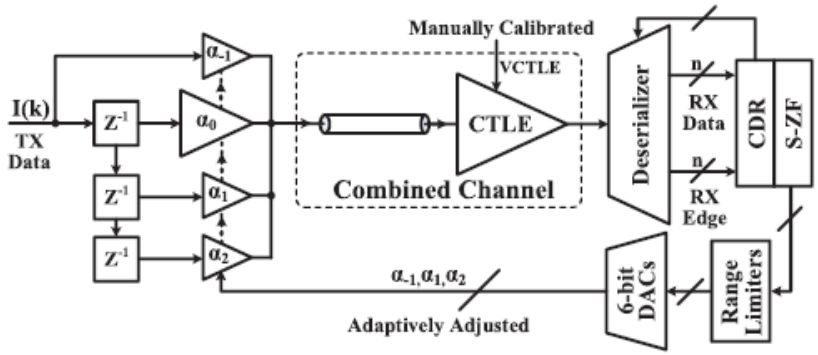
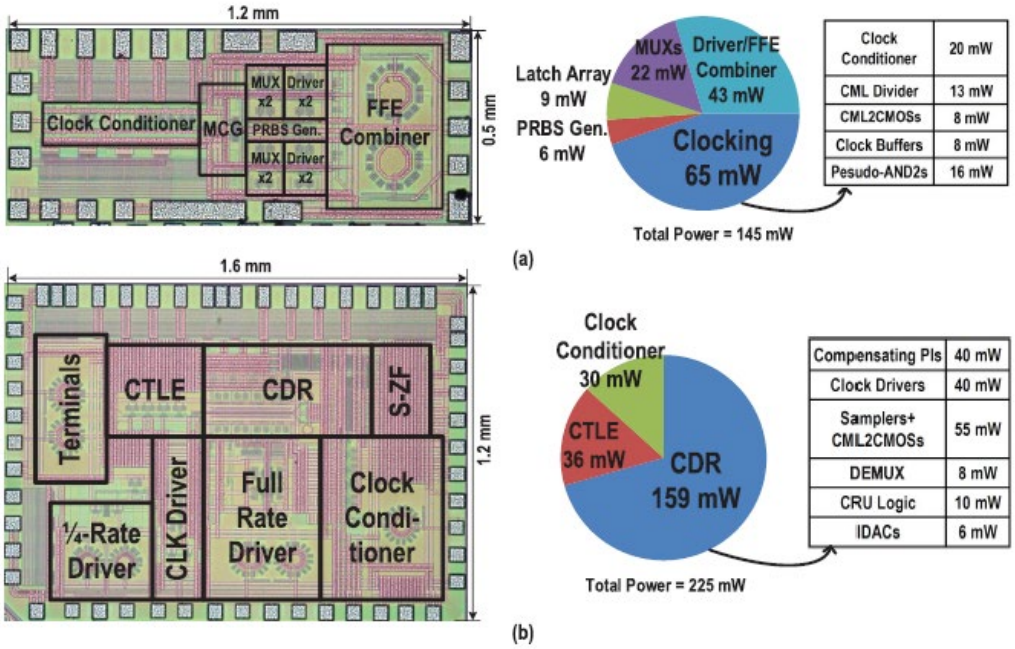


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

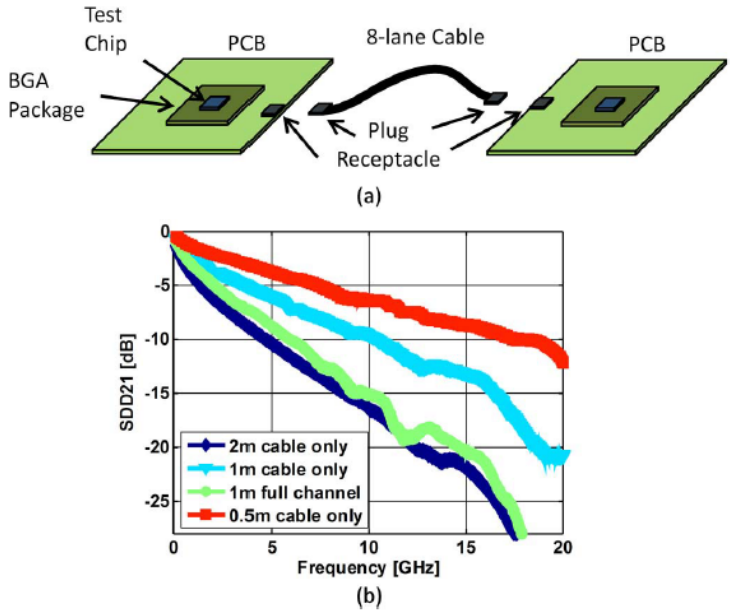
Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 1, the data transmission system 1 is in accordance with DP1.4, for example, and includes an upstream device 2, a downstream device 4, and an active cable 3 connecting the upstream device 2 and downstream device 4." Kobayashi, 2:41-45.
6[a] receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device;	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

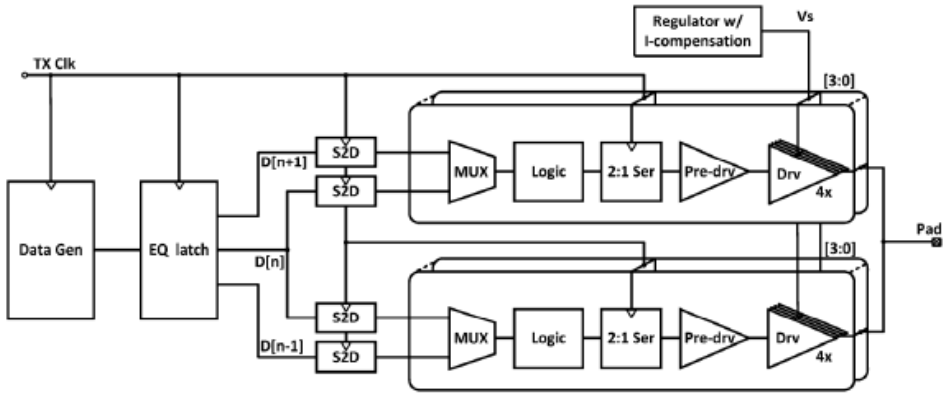
Claim 6	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

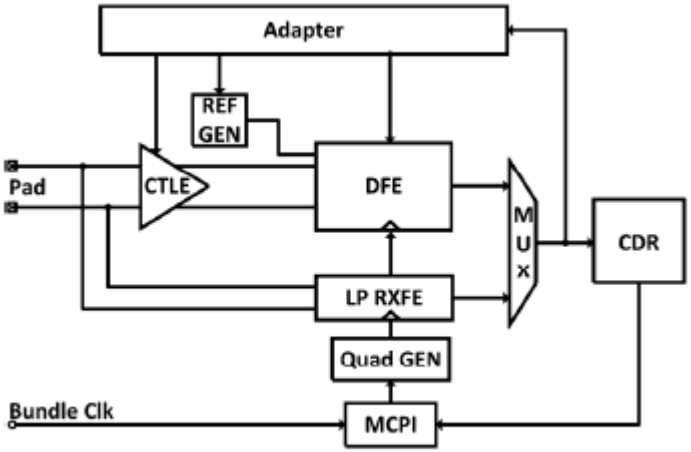
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

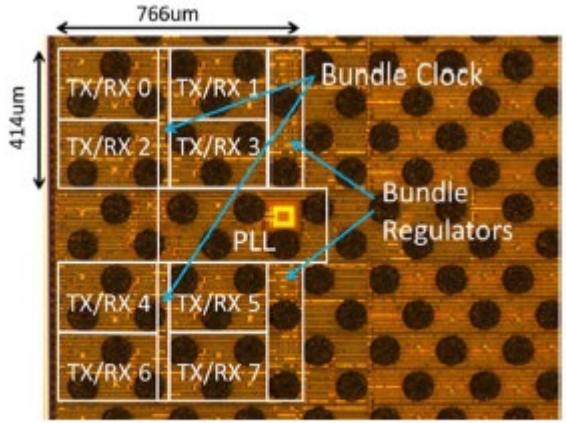
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

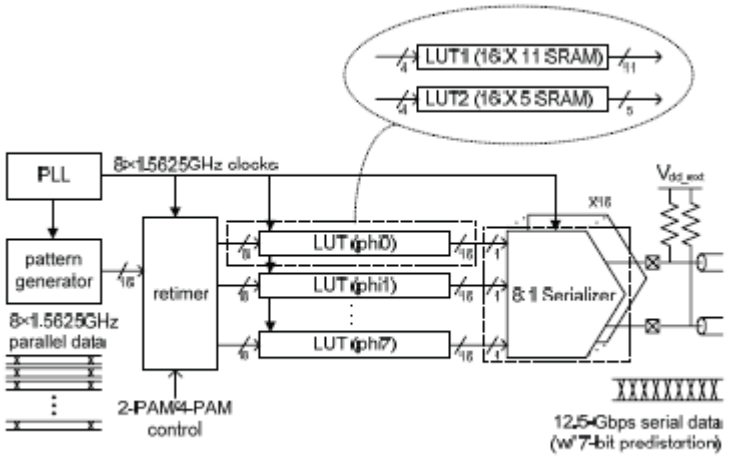
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

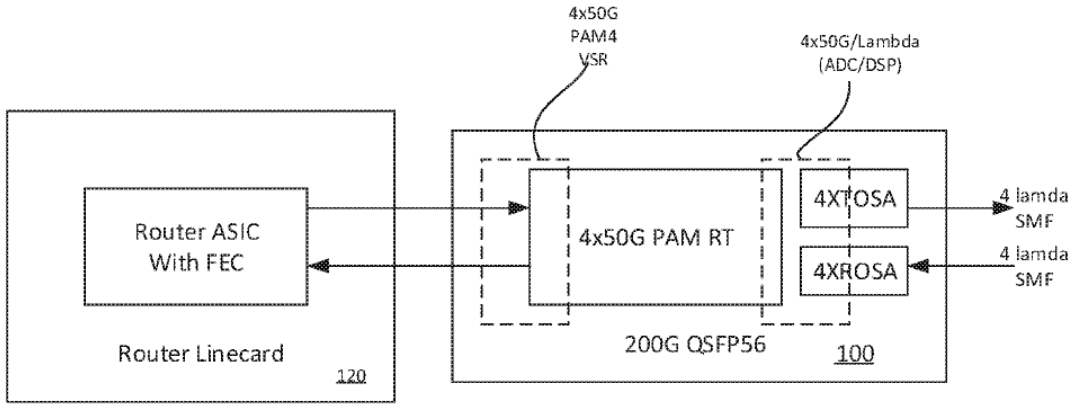
Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

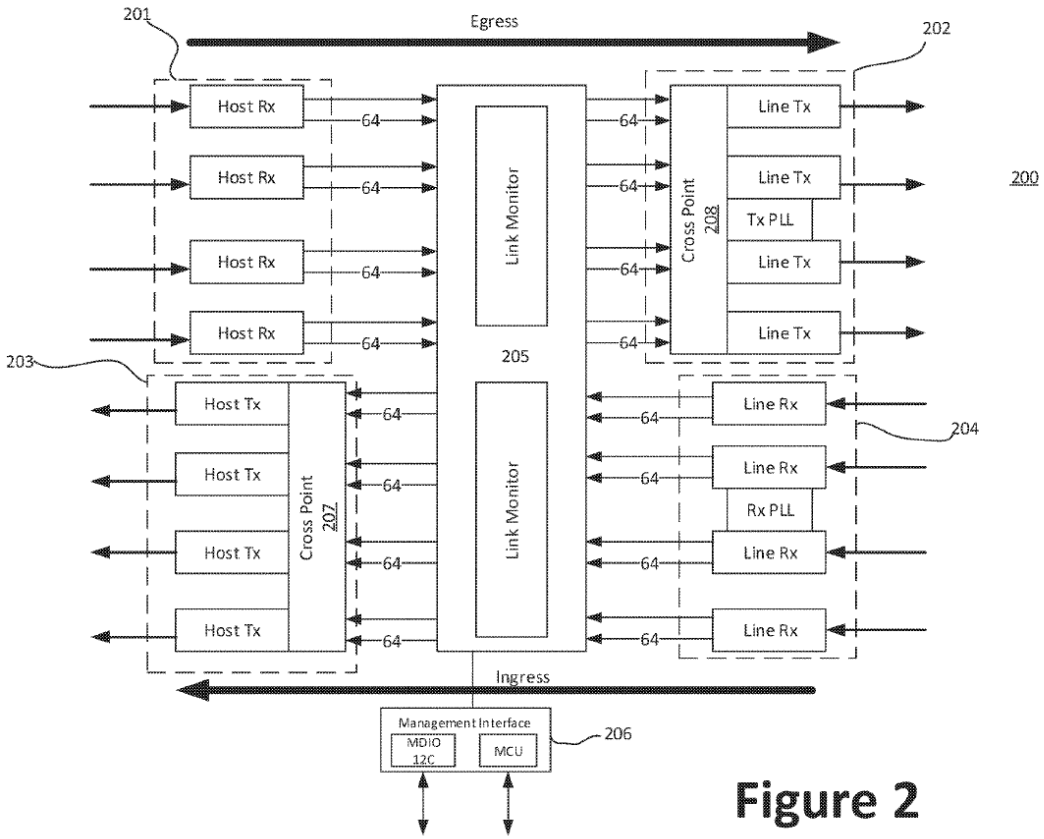
Claim 6	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 6	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 6	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 6	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 **Figure 2** Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 6	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 6	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 6	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 6	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 6	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 6	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 6	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 6	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

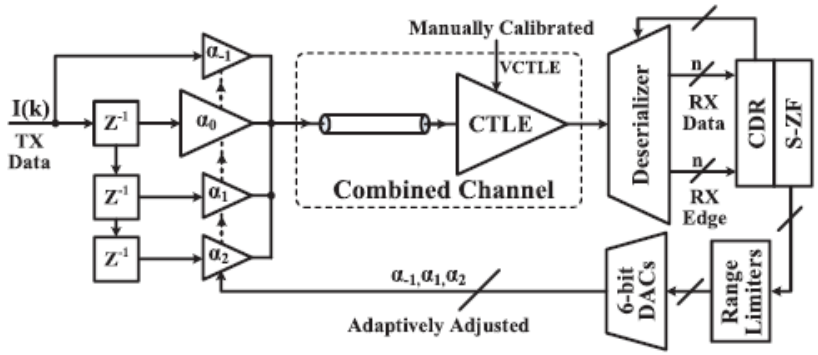
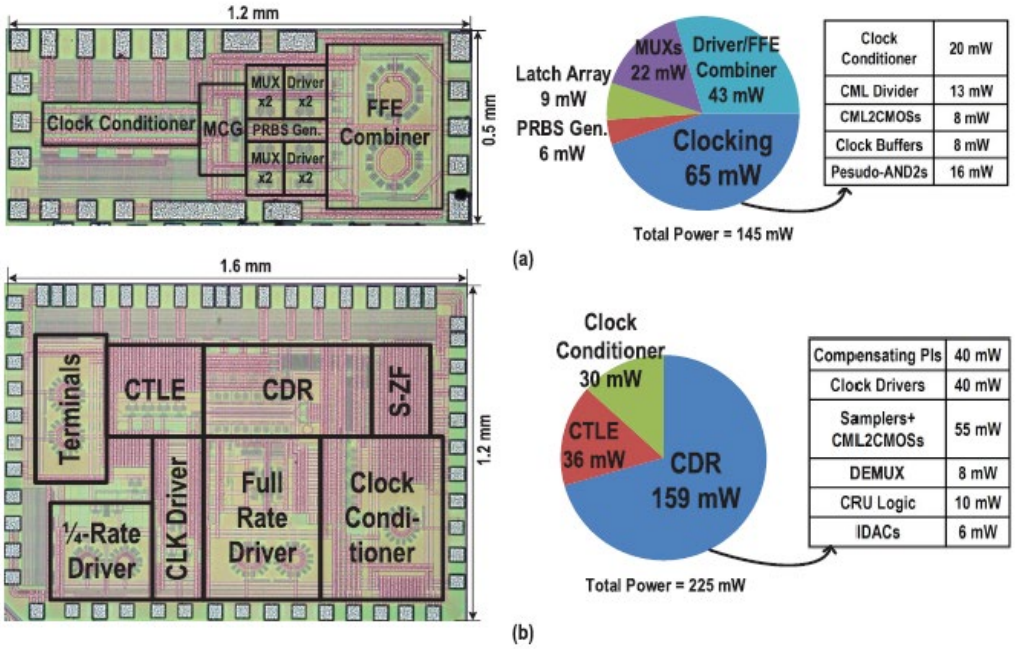


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

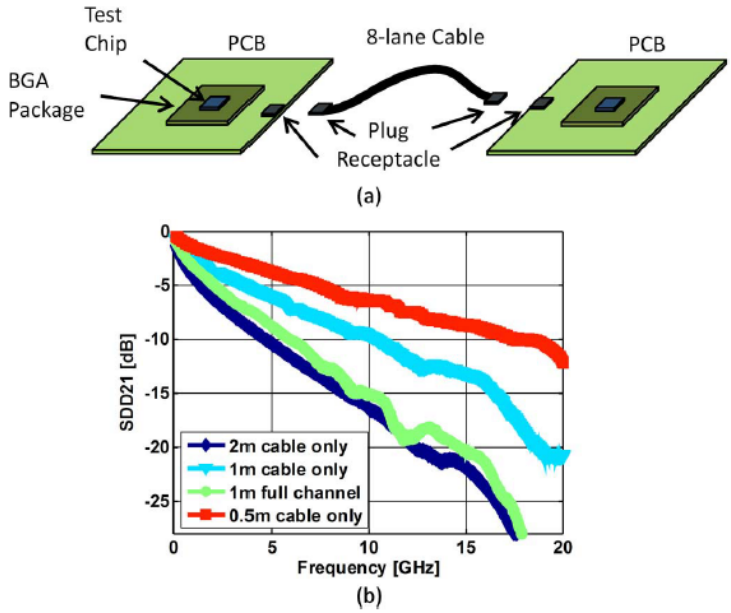
Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "In the data transmission system 1 having the above configuration, the source 20 in the upstream device 2 generates a serial bit stream which is a video signal, for example. The source 20 transmits the generated serial bit stream from the downstream facing TX 20a to the retimer 21. The retimer 21 receives the serial bit stream transmitted from the downstream facing TX 20a in the upstream facing TX 21a. The retimer 21 performs a waveform shaping on the received serial bit stream and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 21b to the active cable 3." Kobayashi, 2:60-3:4.
6[b] performing clock and data recovery on the	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following

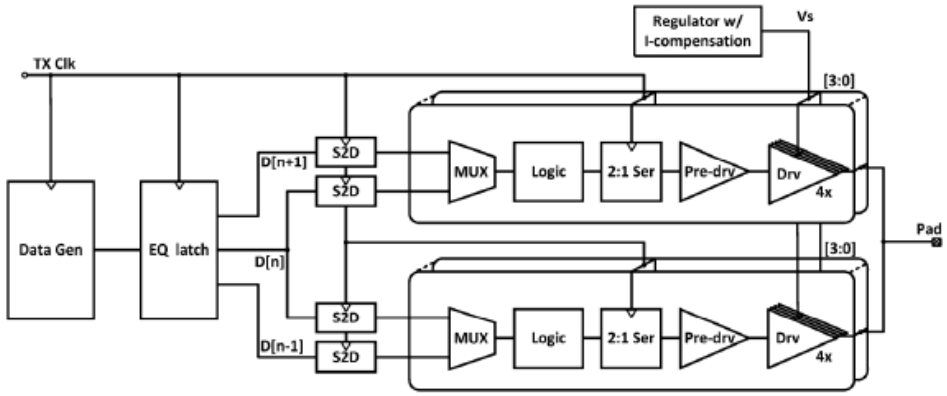
Claim 6	Disclosure
first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream;	exemplary citations: ***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

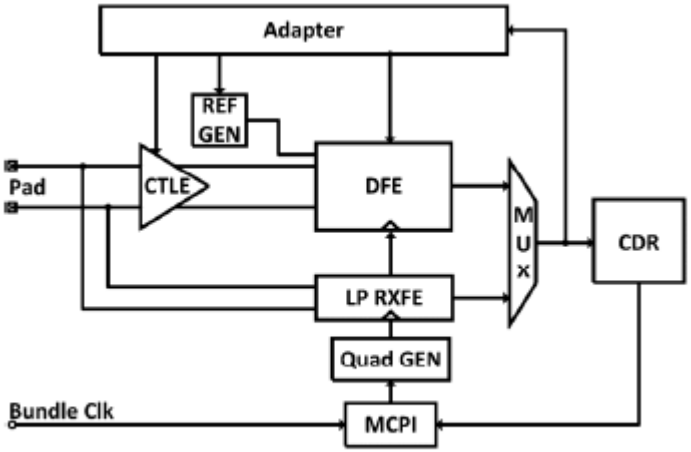
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

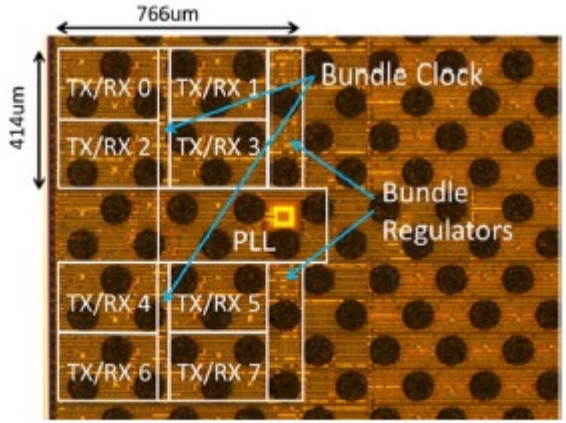
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

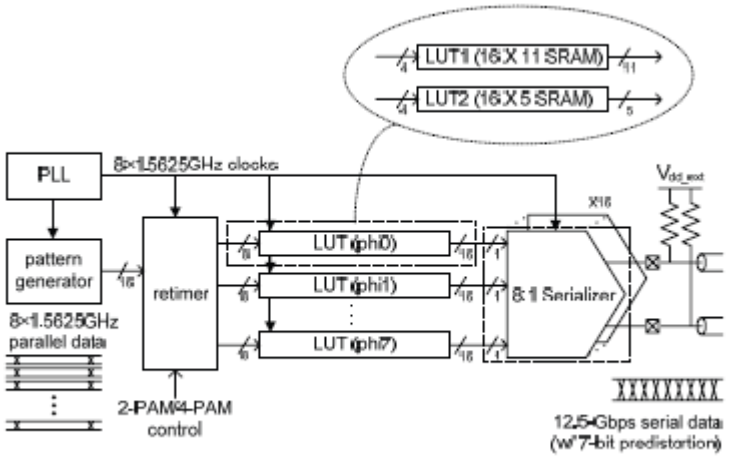
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

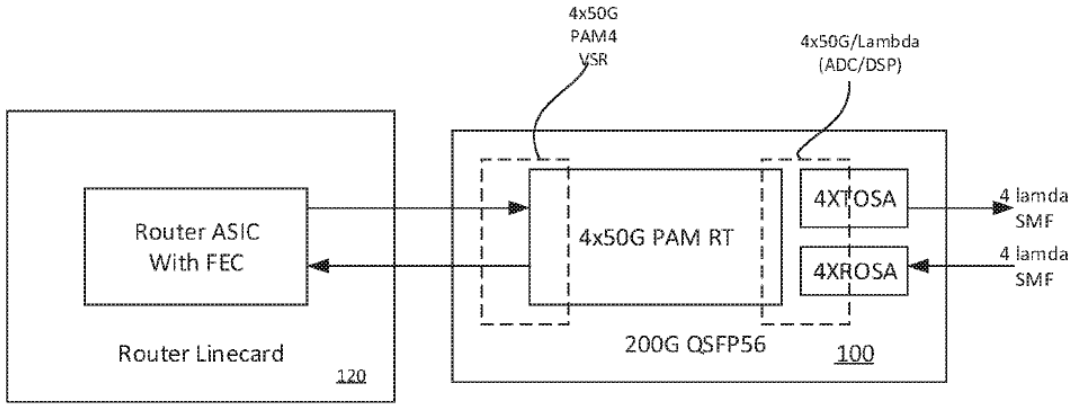
Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

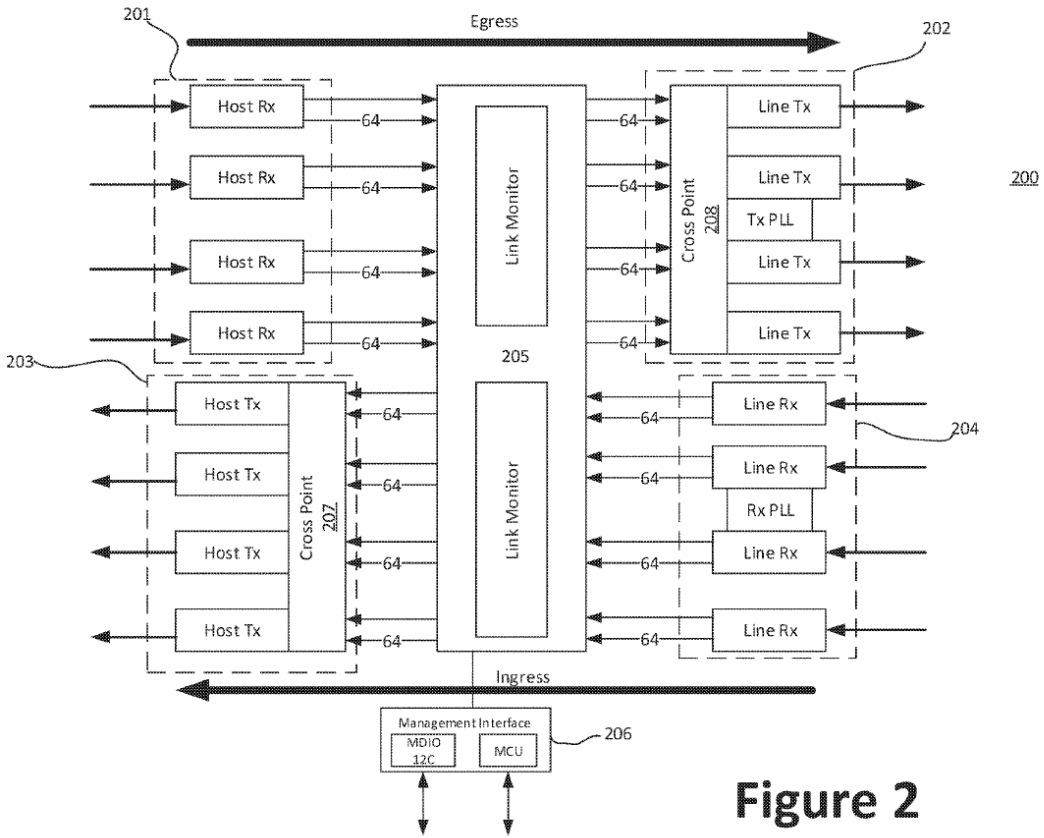
Claim 6	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 6	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 6	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 6	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 **Figure 2** Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 6	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 6	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 6	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 6	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 6	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 6	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 6	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 6	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

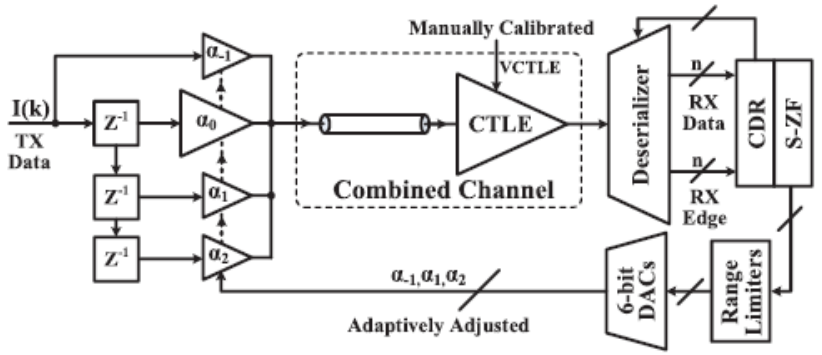
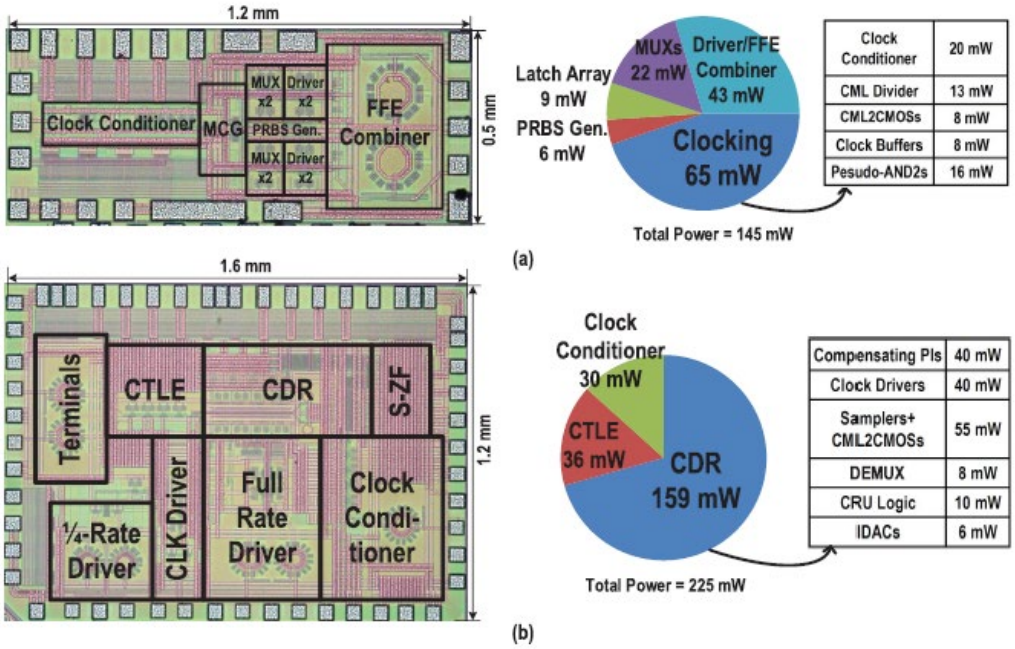


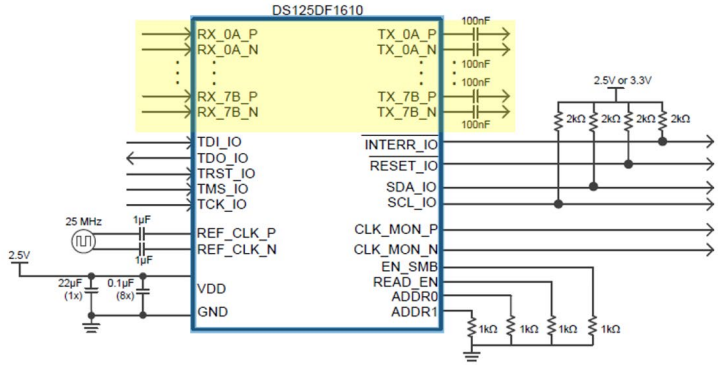
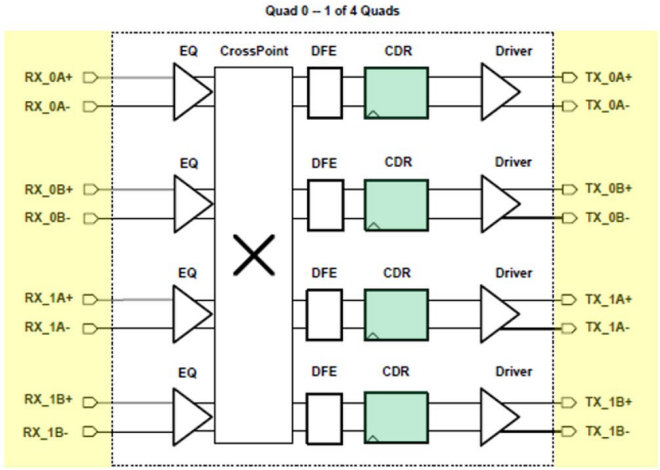
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

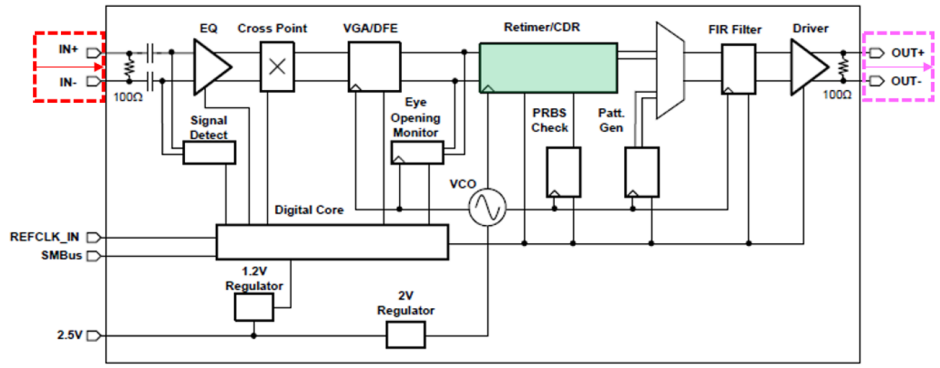
Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local

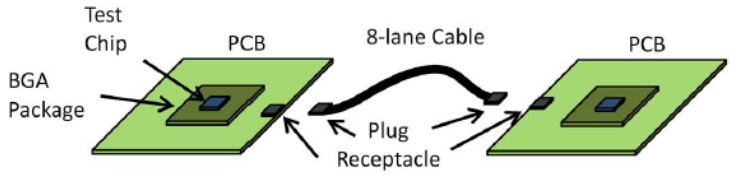
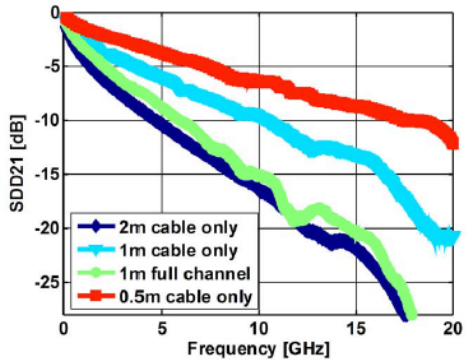
Claim 6	Disclosure
	timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK" Kobayashi, 4:4-22. *DS125DF1610 Retimer Publication* The DS125DF1610 circuit is illustrated in the Simplified Schematic and Figure 1 below. The highlighted pins illustrate sixteen channels of data, with each channel having two differential (Positive and Negative) input pins (RX_0A_P/N through RX_7B_P/N) to receive the channel of data and corresponding output pins (TX_0A_P/N through TX_7B_P/N) to transmit the channel of data after processing. *See, e.g.*, DS125DF1610 at §§ 3, 7.2. Thus, DS125DF1610's retimer is a transceiver that, when used in Tang's cable, receives one or more inbound data streams (on RX_0A_P/N through RX_7B_P/N), and transmits one or more transit data streams (via pins TX_0A_P/N through TX_7B_P/N).

Claim 6	Disclosure
	Simplified Schematic   **Figure 1. DS125DF1610 Simplified Cross Point Diagram** Figure 1 above shows four channels and illustrates that DS125DF1610's retimer processes each data channel by, inter alia, performing "clock and data recovery (CDR)." *See id.* at §§ 3, 7.1. A channel's data path is shown in more detail in DS125DF1610 Figure 2 (below), which illustrates the input signal conveying an inbound data stream and the transit signal conveying a transit data stream in Tang's cable

Claim 6	Disclosure
	when DS125DF1610's retimer implements Tang's signal driver 44.  **Figure 2. DS125DF1610 Simplified Data Path Diagram** The Retimer/CDR circuit performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream. *See id*. at § 7.3.6. The '252 Patent specification makes clear that the input signal from the host can be pre-processed before CDR is performed on it. An ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data for output as the transit data stream because after extracting the input signal's timing and using that timing to sample and extract the input signal's data in an analog-to-digital CDR process, the retimer generates a new data stream for equalization by the FIR Filter (a digital-to-analog process) and to be driven for output by the differential driver (which produces an analog signal with configurable output voltage levels) to convey the output data stream (transit data stream when outputting over the cable) as an analog signal over the cable conductors, where the new signal is a "re-modulation" of the data. *See id*. at §§ 7.3.6-7.3.9.
6[c] re-modulating the first inbound data stream as a first transit data stream conveyed by a	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

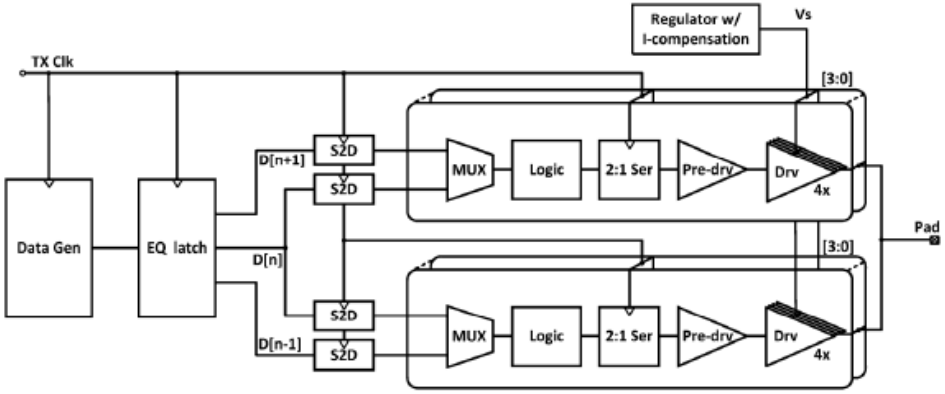
Claim 6	Disclosure
first electrical transit signal over a first of the conductor pairs;	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

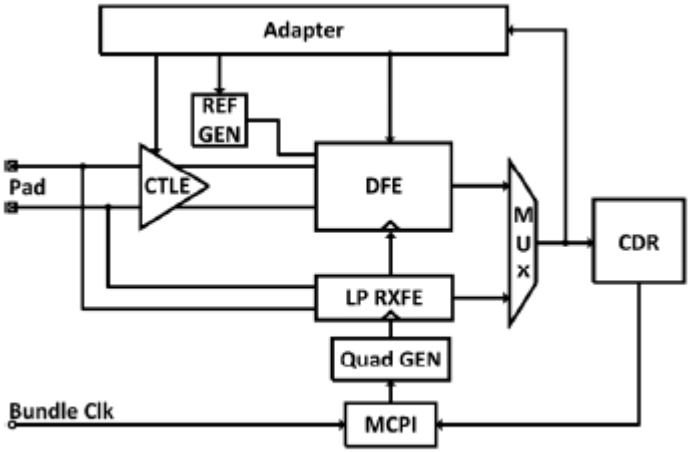
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 (a)  (b) Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

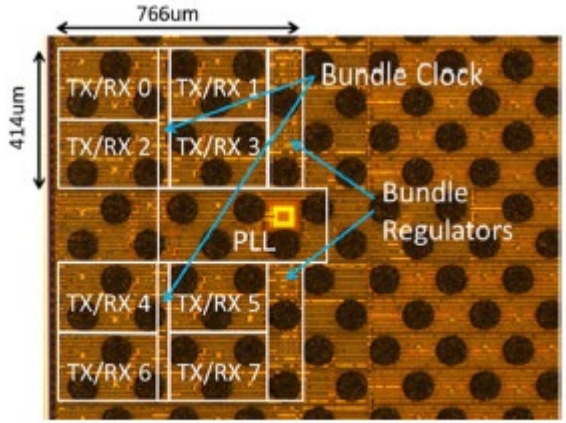
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

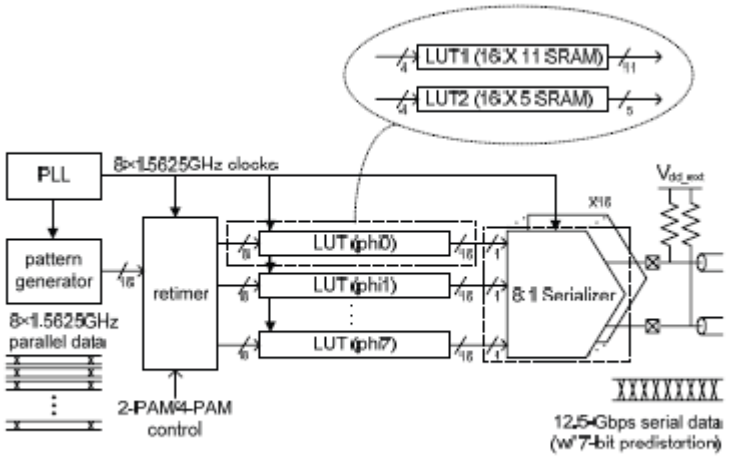
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

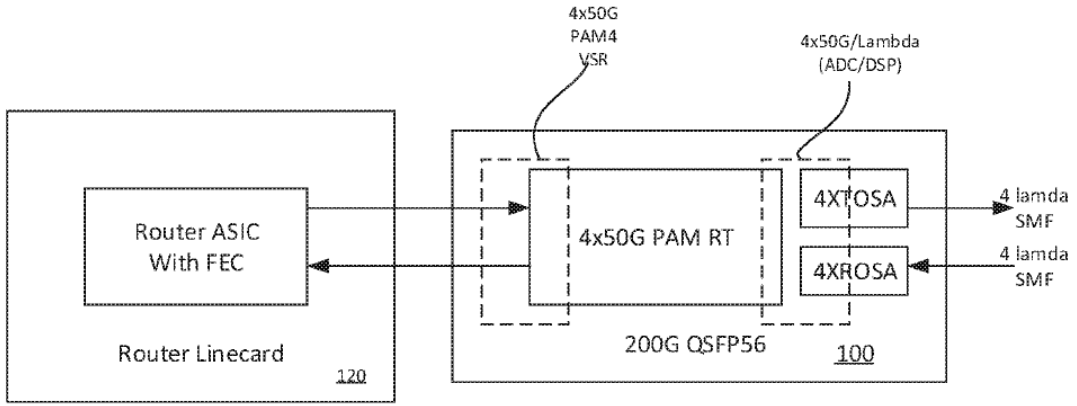
Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13µm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

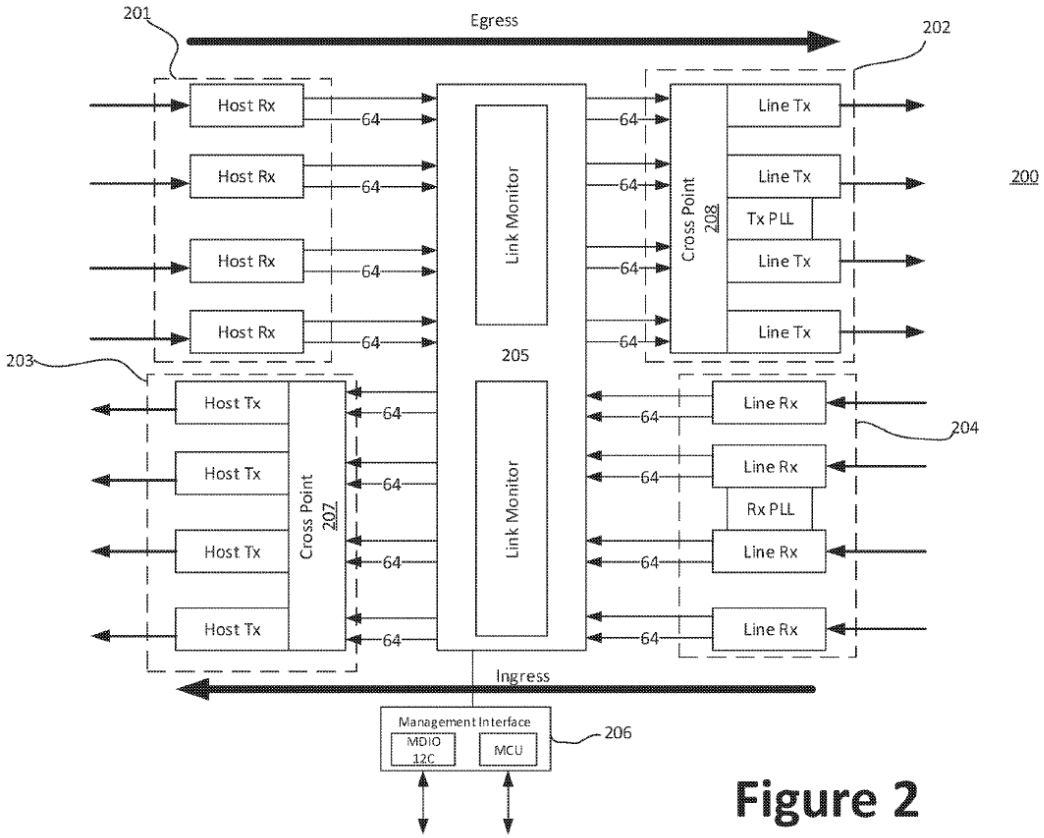
Claim 6	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 6	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 6	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 6	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 6	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 6	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 6	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 6	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 6	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 6	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 6	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 6	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

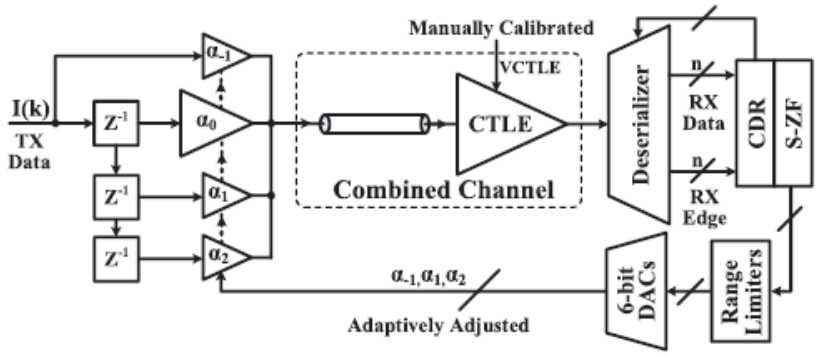
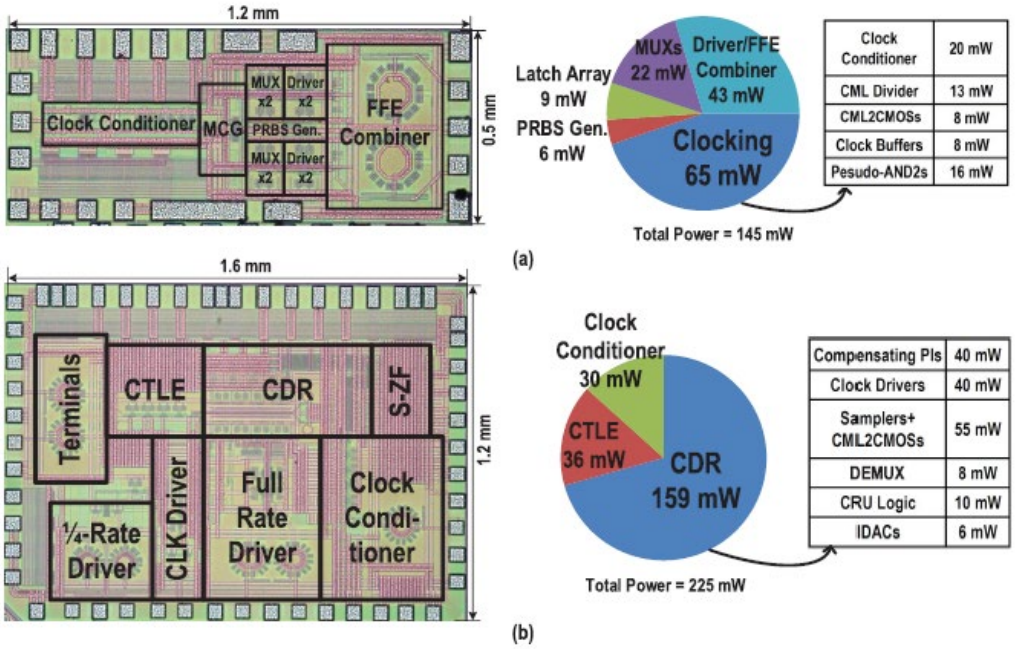


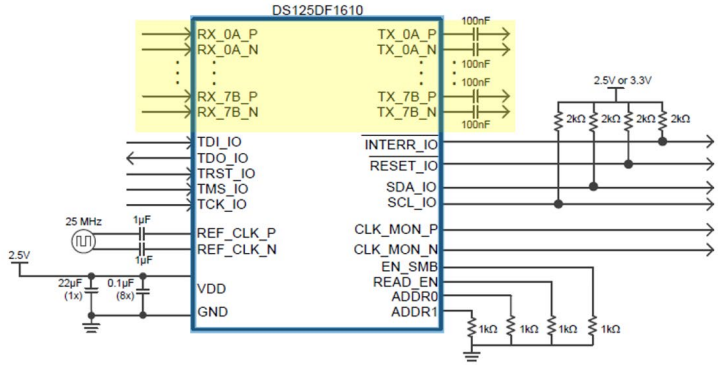
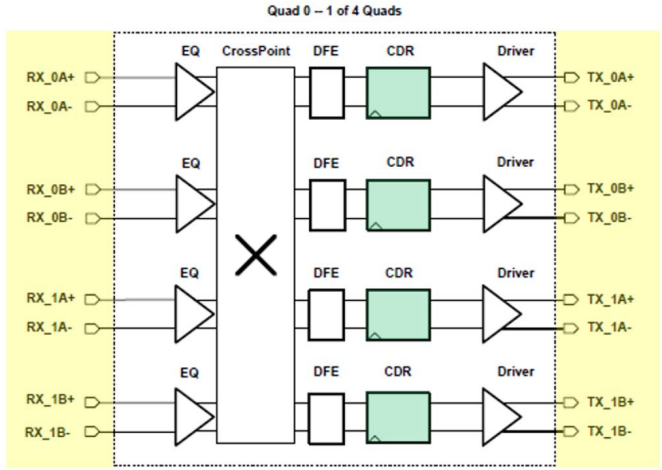
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

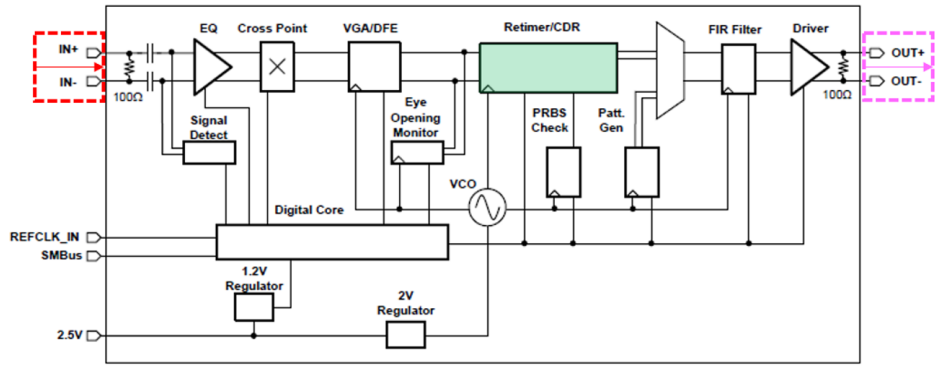
Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local

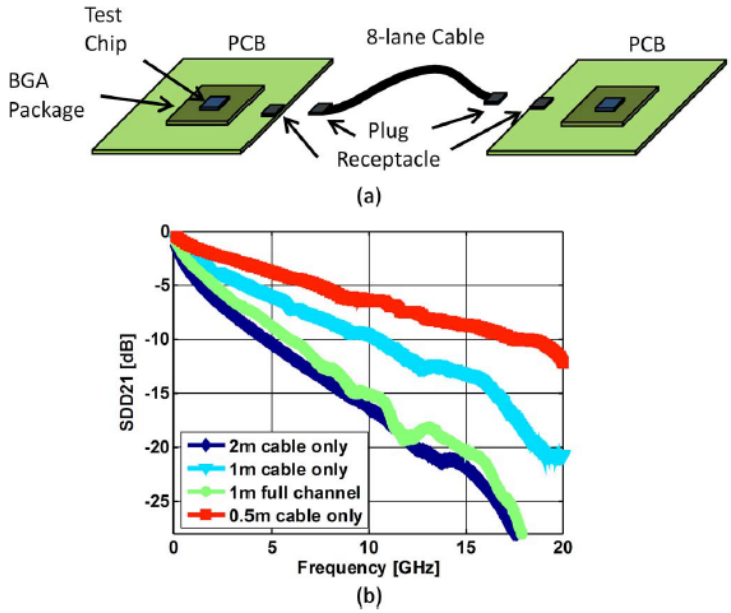
Claim 6	Disclosure
	timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK" Kobayashi, 4:4-22. *DS125DF1610 Retimer Publication* The DS125DF1610 circuit is illustrated in the Simplified Schematic and Figure 1 below. The highlighted pins illustrate sixteen channels of data, with each channel having two differential (Positive and Negative) input pins (RX_0A_P/N through RX_7B_P/N) to receive the channel of data and corresponding output pins (TX_0A_P/N through TX_7B_P/N) to transmit the channel of data after processing. *See, e.g.*, DS125DF1610 at §§ 3, 7.2. Thus, DS125DF1610's retimer is a transceiver that, when used in Tang's cable, receives one or more inbound data streams (on RX_0A_P/N through RX_7B_P/N), and transmits one or more transit data streams (via pins TX_0A_P/N through TX_7B_P/N).

Claim 6	Disclosure
	Simplified Schematic   **Figure 1. DS125DF1610 Simplified Cross Point Diagram** Figure 1 above shows four channels and illustrates that DS125DF1610's retimer processes each data channel by, inter alia, performing "clock and data recovery (CDR)." *See id.* at §§ 3, 7.1. A channel's data path is shown in more detail in DS125DF1610 Figure 2 (below), which illustrates the input signal conveying an inbound data stream and the transit signal conveying a transit data stream in Tang's cable

Claim 6	Disclosure
	when DS125DF1610's retimer implements Tang's signal driver 44.  **Figure 2. DS125DF1610 Simplified Data Path Diagram** The Retimer/CDR circuit performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream. *See id*. at § 7.3.6. The '252 Patent specification makes clear that the input signal from the host can be pre-processed before CDR is performed on it. An ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data for output as the transit data stream because after extracting the input signal's timing and using that timing to sample and extract the input signal's data in an analog-to-digital CDR process, the retimer generates a new data stream for equalization by the FIR Filter (a digital-to-analog process) and to be driven for output by the differential driver (which produces an analog signal with configurable output voltage levels) to convey the output data stream (transit data stream when outputting over the cable) as an analog signal over the cable conductors, where the new signal is a "re-modulation" of the data. *See id*. at §§ 7.3.6-7.3.9s.
6[d] receiving with the second connector a second electrical input	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

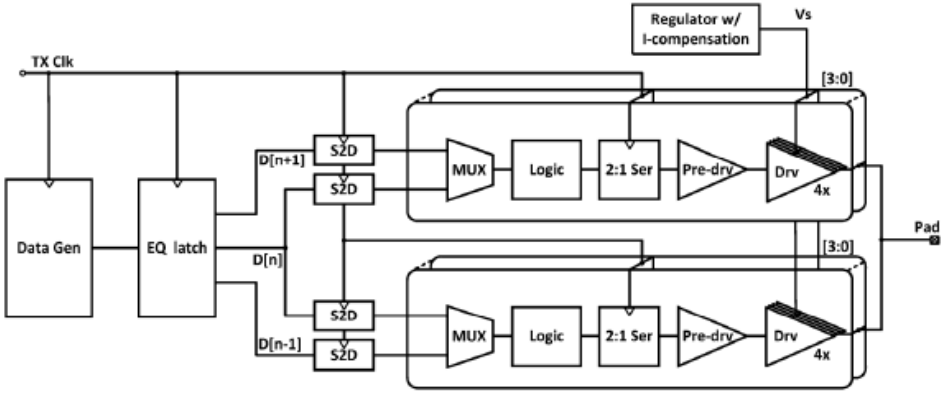
Claim 6	Disclosure
signal conveying a second inbound data stream from a second host device;	*Abstract*—**This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

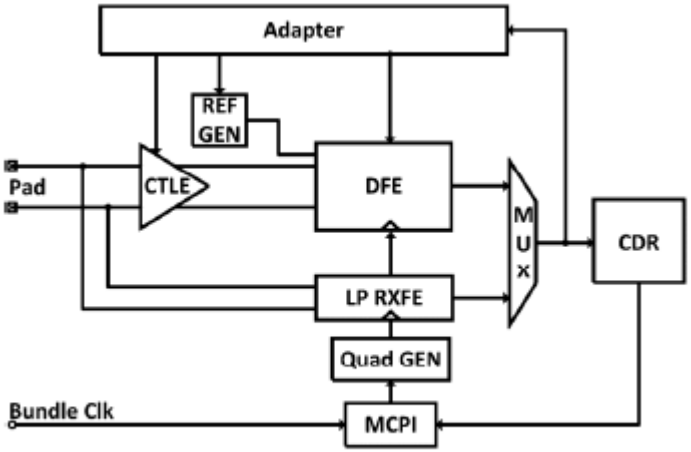
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

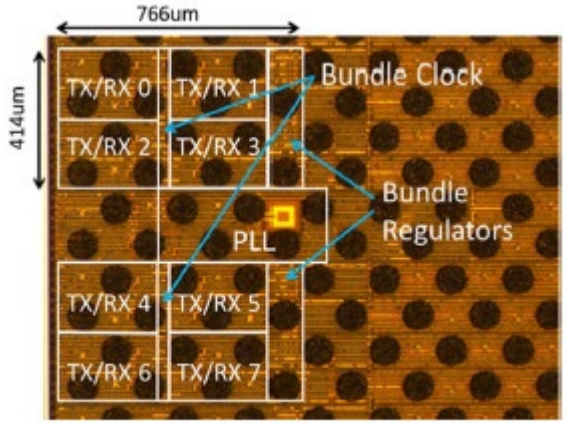
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

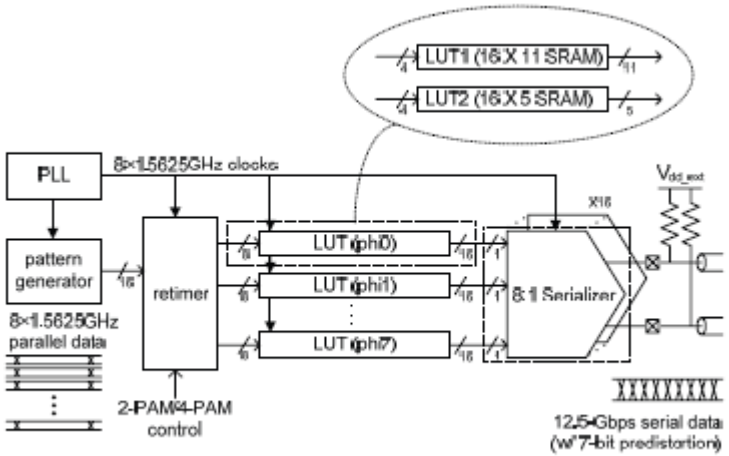
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

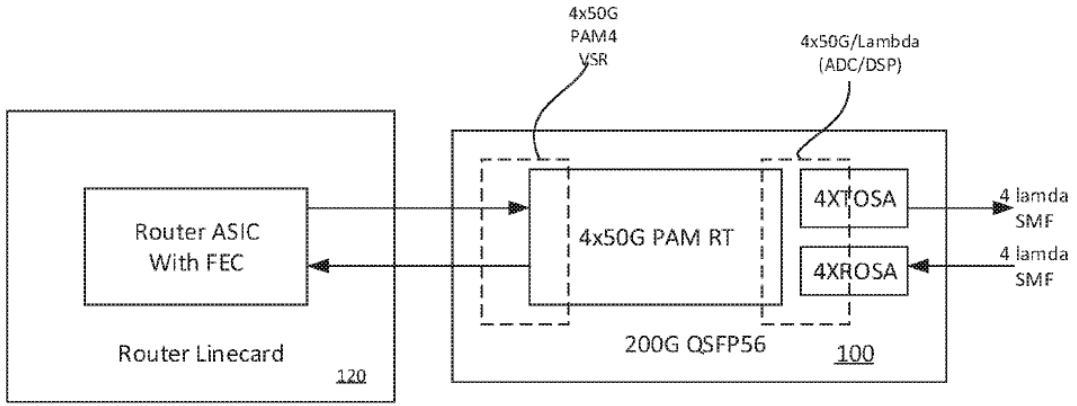
Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

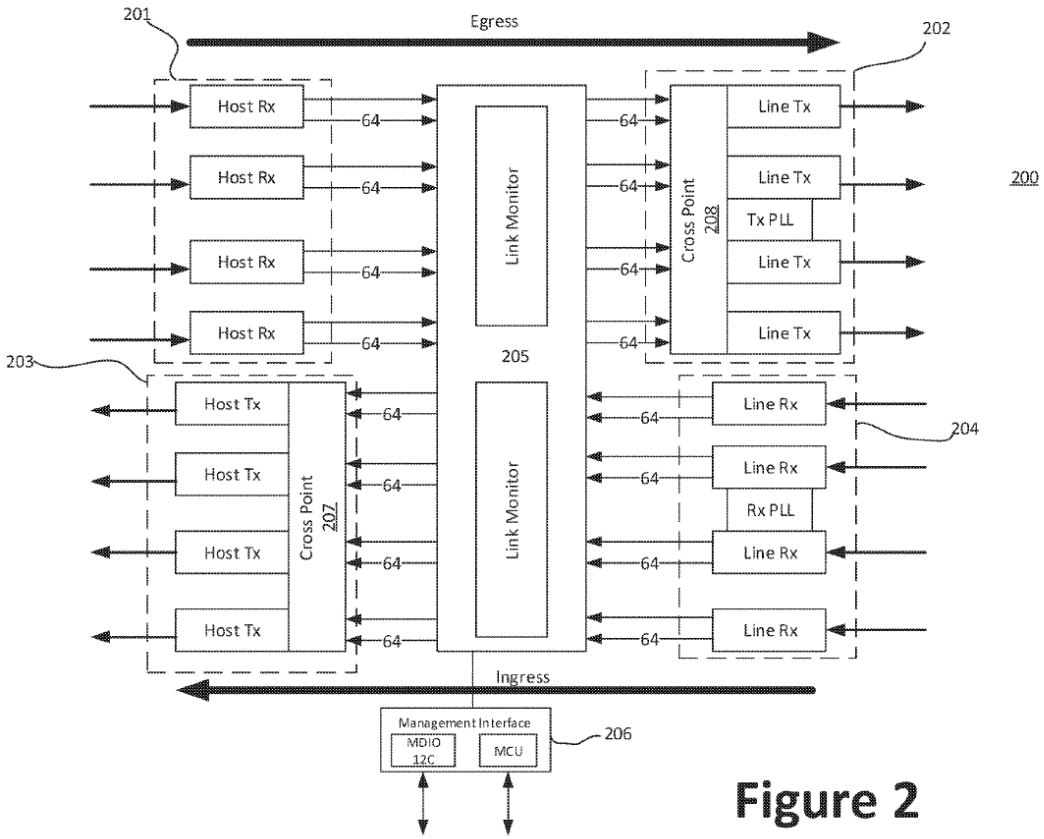
Claim 6	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 6	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 6	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 6	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 6	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 6	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 6	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 6	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 6	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 6	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 6	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 6	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

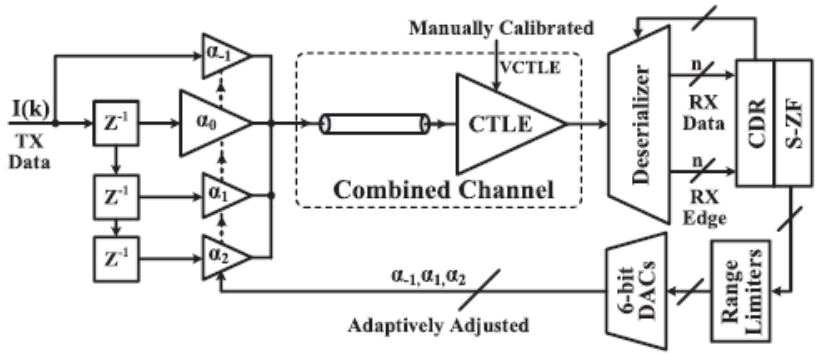
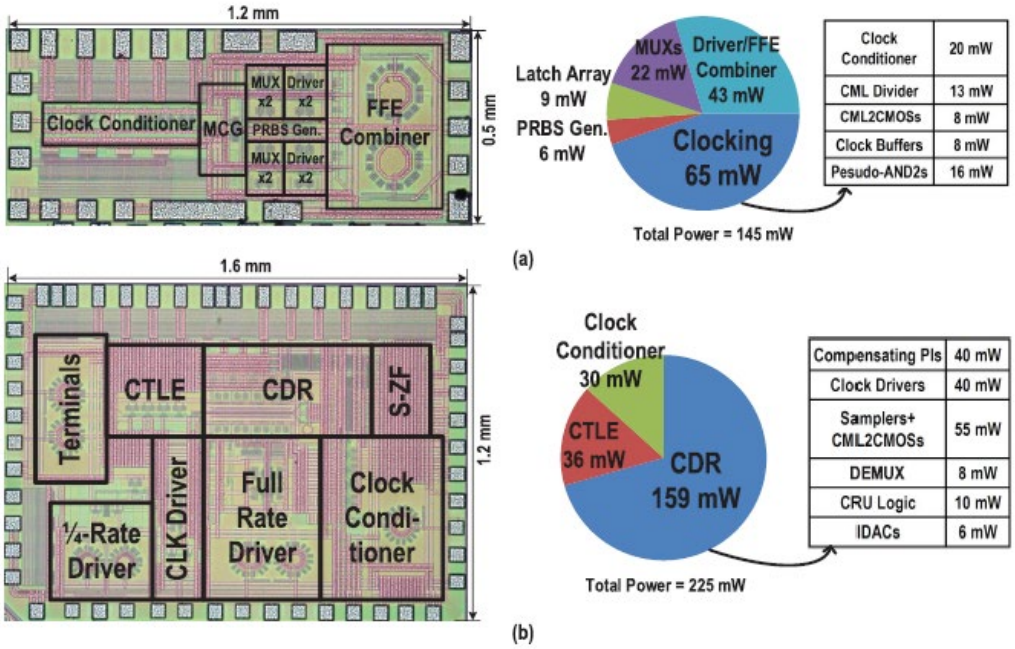


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

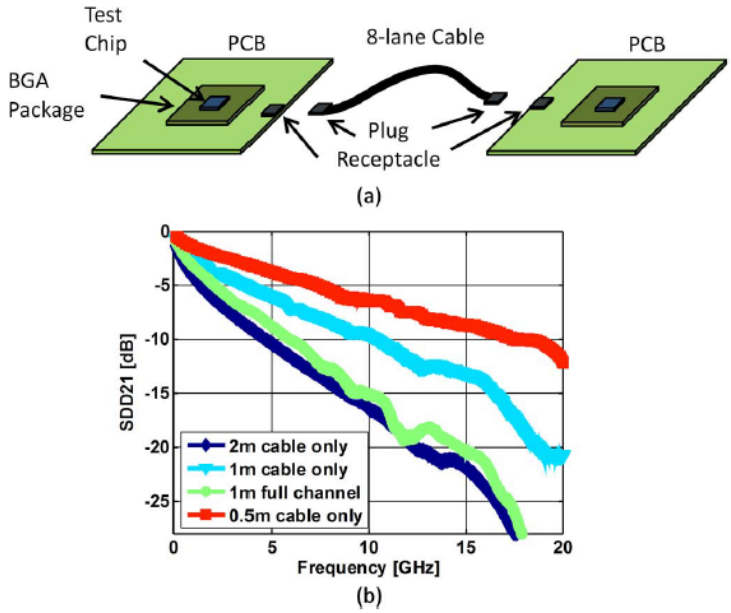
Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The downstream device 4 receives the serial bit stream transmitted from the active cable 3 in the upstream facing RX 40a in the retimer 40. The retimer 40 performs a waveform shaping on the serial bit stream received by the upstream facing RX 40a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 40b to a sink 41. The sink 41 displays a video, for example, based on the received serial bit data." Kobayashi, 3:20-28.
6[e] performing clock and data recovery on the second electrical input signal with a second transceiver in the second	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

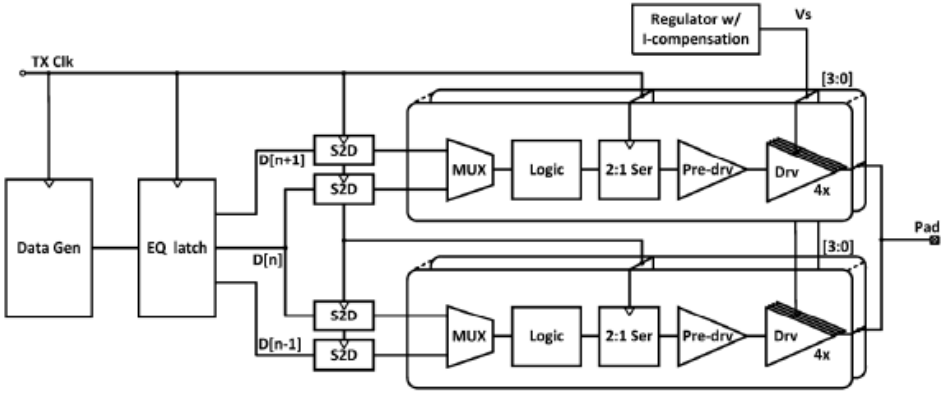
Claim 6	Disclosure
connector to extract the second inbound data stream;	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

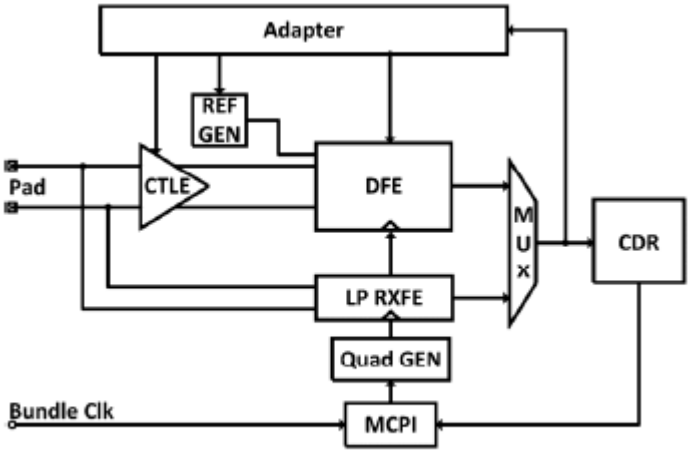
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

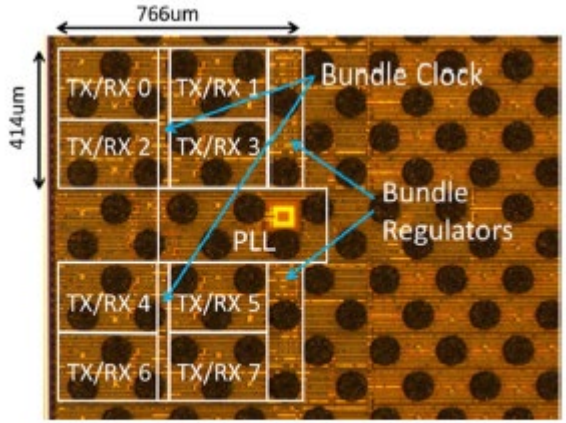
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

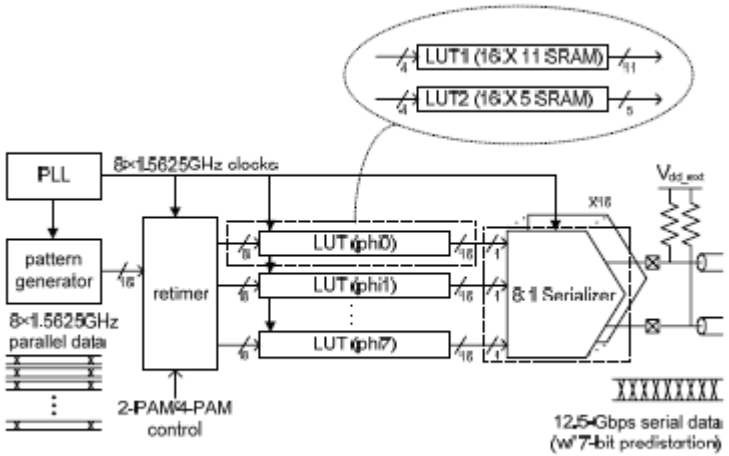
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

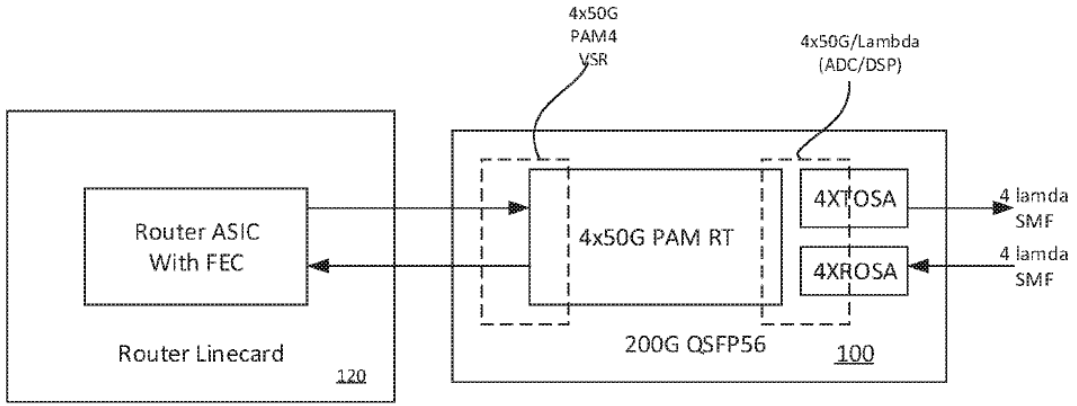
Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

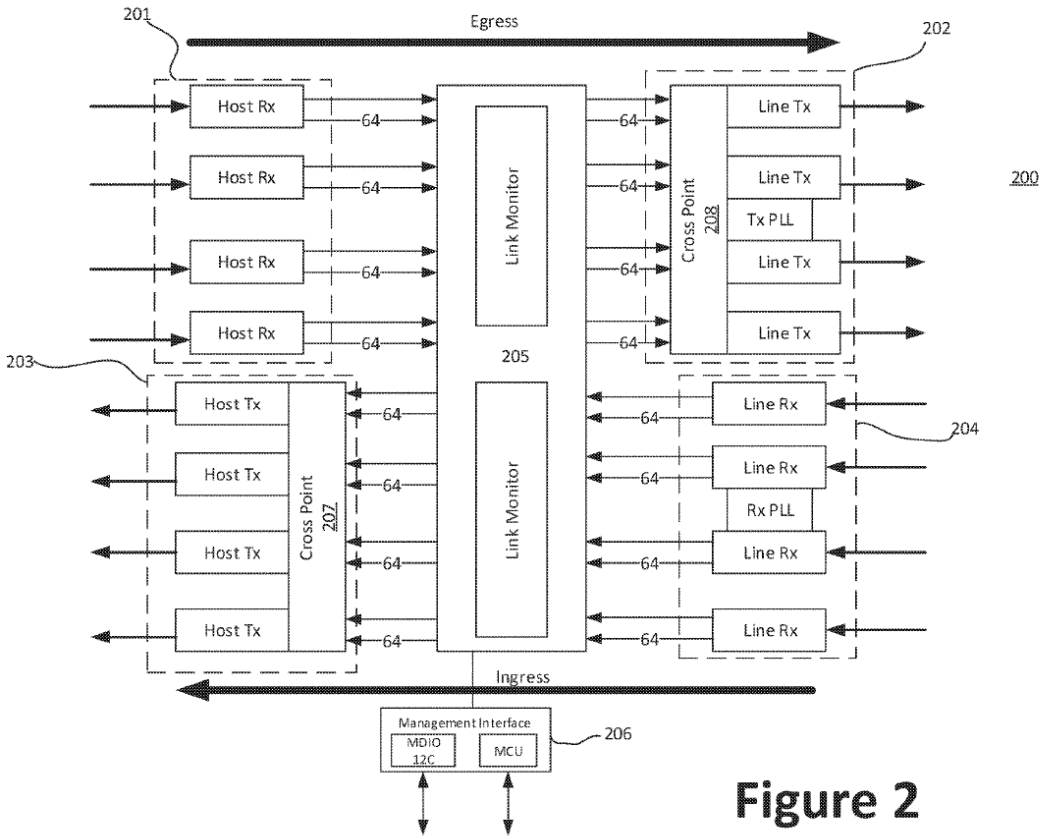
Claim 6	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 6	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 6	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 6	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 6	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 6	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 6	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 6	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 6	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 6	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 6	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 6	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

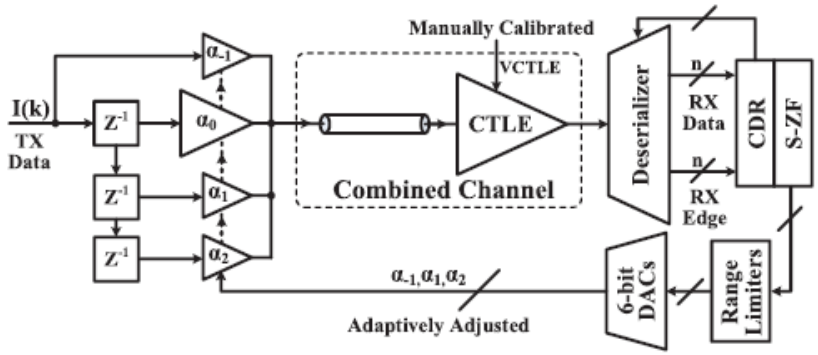
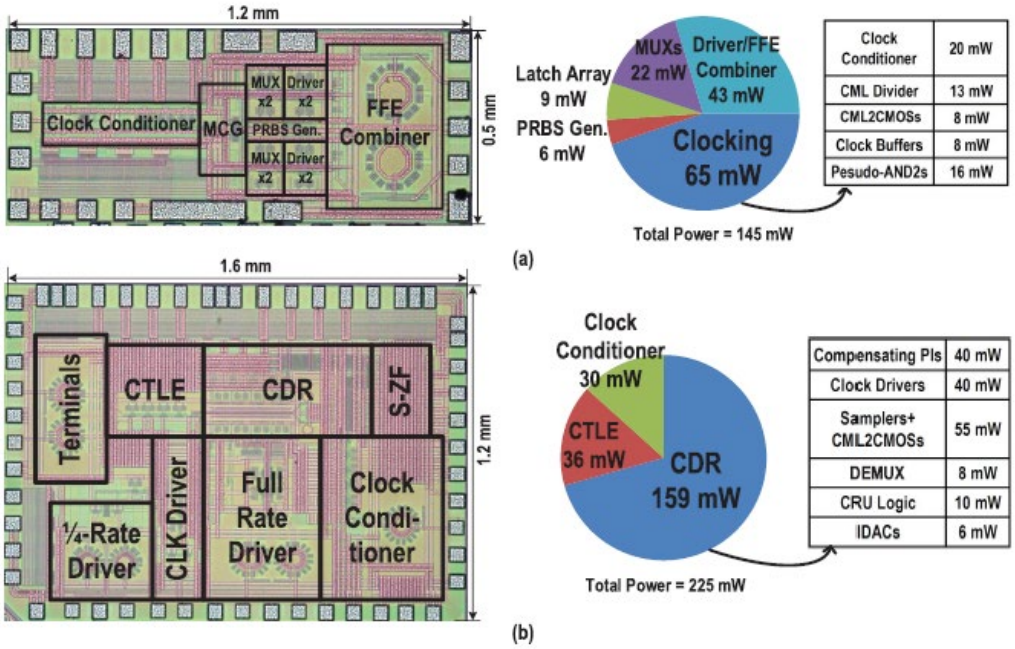


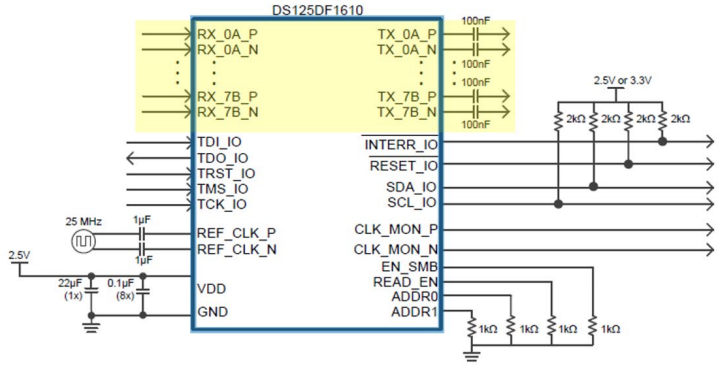
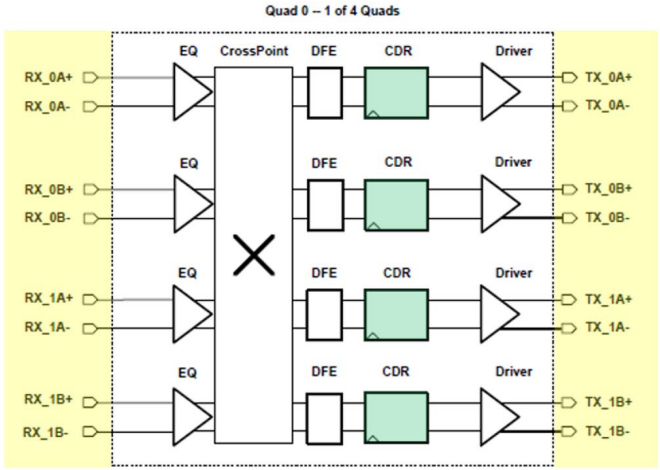
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

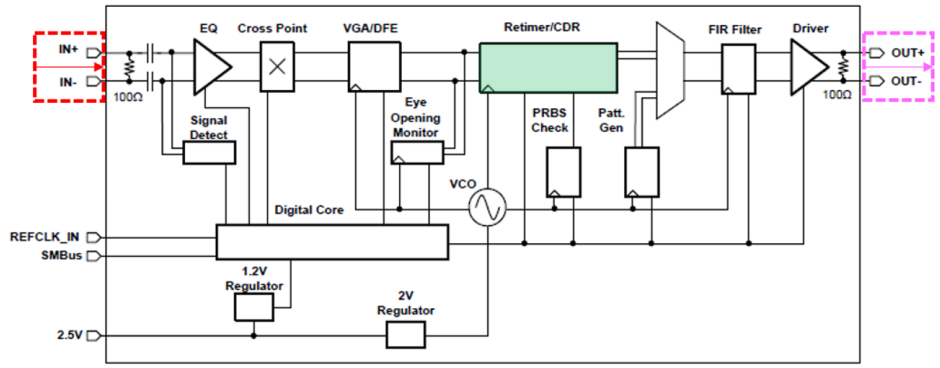
Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK"

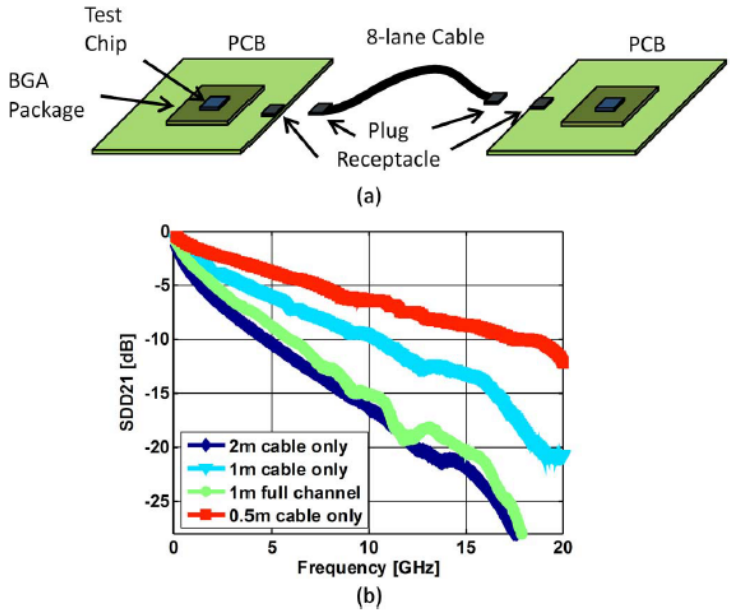
Claim 6	Disclosure
	Kobayashi, 4:4-22. <u>*DS125DF1610 Retimer Publication*</u> The DS125DF1610 circuit is illustrated in the Simplified Schematic and Figure 1 below. The highlighted pins illustrate sixteen channels of data, with each channel having two differential (Positive and Negative) input pins (RX_0A_P/N through RX_7B_P/N) to receive the channel of data and corresponding output pins (TX_0A_P/N through TX_7B_P/N) to transmit the channel of data after processing. *See, e.g.*, DS125DF1610 at §§ 3, 7.2. Thus, DS125DF1610's retimer is a transceiver that, when used in Tang's cable, receives one or more inbound data streams (on RX_0A_P/N through RX_7B_P/N), and transmits one or more transit data streams (via pins TX_0A_P/N through TX_7B_P/N).

Claim 6	Disclosure
	Simplified Schematic   **Figure 1. DS125DF1610 Simplified Cross Point Diagram** Figure 1 above shows four channels and illustrates that DS125DF1610's retimer processes each data channel by, inter alia, performing "clock and data recovery (CDR)." *See id.* at §§ 3, 7.1. A channel's data path is shown in more detail in DS125DF1610 Figure 2 (below), which illustrates the input signal conveying an inbound data stream and the transit signal conveying a transit data stream in Tang's cable

Claim 6	Disclosure
	when DS125DF1610's retimer implements Tang's signal driver 44.  **Figure 2. DS125DF1610 Simplified Data Path Diagram** The Retimer/CDR circuit performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream. *See id*. at § 7.3.6. The '252 Patent specification makes clear that the input signal from the host can be pre-processed before CDR is performed on it. An ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data for output as the transit data stream because after extracting the input signal's timing and using that timing to sample and extract the input signal's data in an analog-to-digital CDR process, the retimer generates a new data stream for equalization by the FIR Filter (a digital-to-analog process) and to be driven for output by the differential driver (which produces an analog signal with configurable output voltage levels) to convey the output data stream (transit data stream when outputting over the cable) as an analog signal over the cable conductors, where the new signal is a "re-modulation" of the data. *See id*. at §§ 7.3.6-7.3.9.
6[f] re-modulating the second inbound data stream as a second transit	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

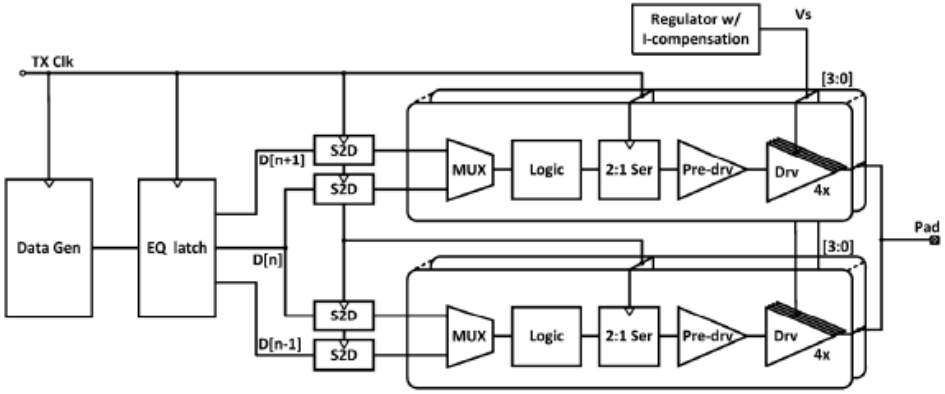
Claim 6	Disclosure
data stream conveyed by a second electrical transit signal over a second of the conductor pairs;	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

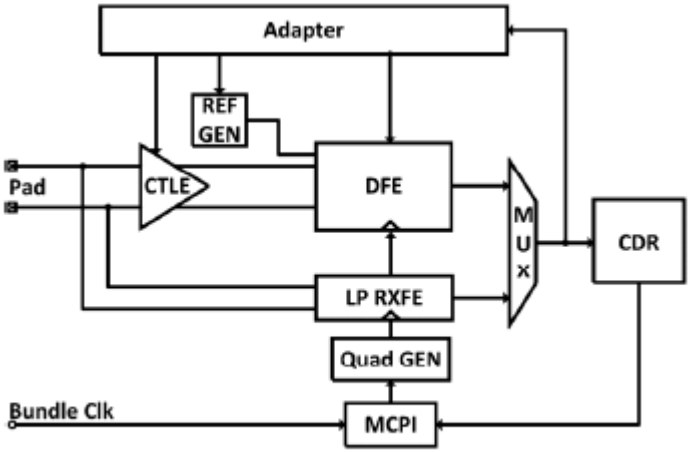
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

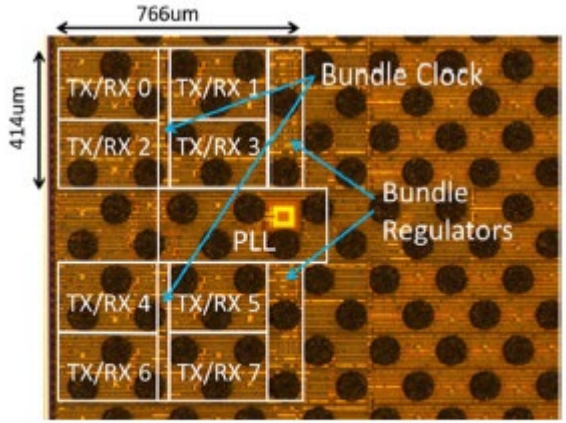
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

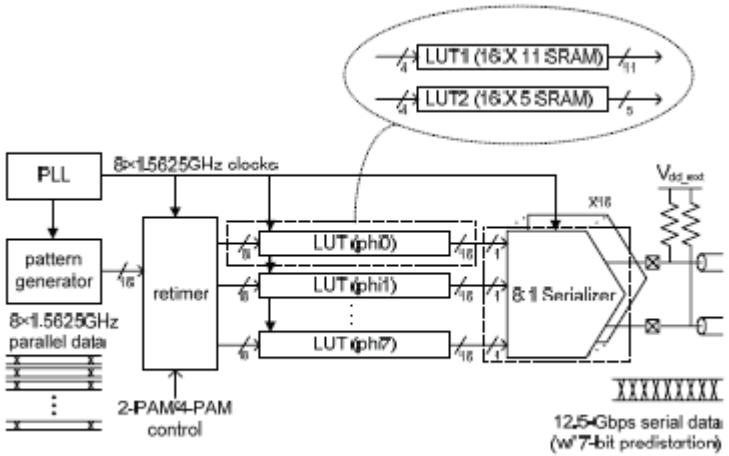
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

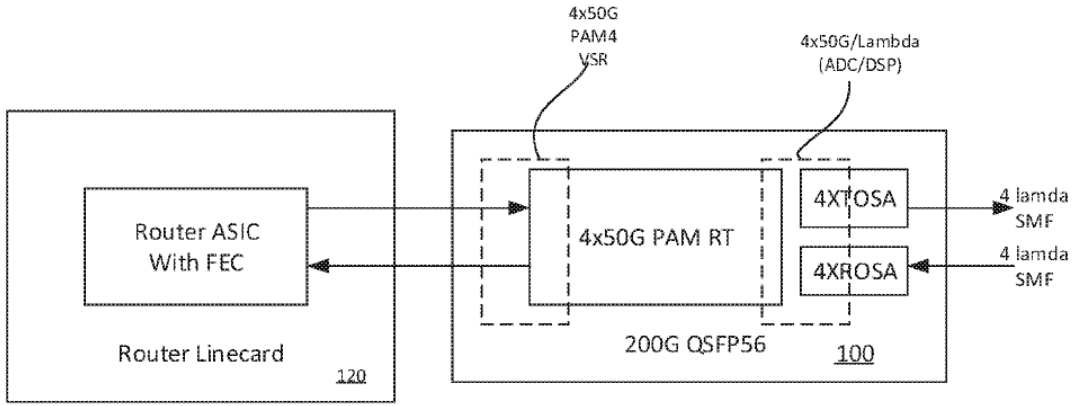
Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

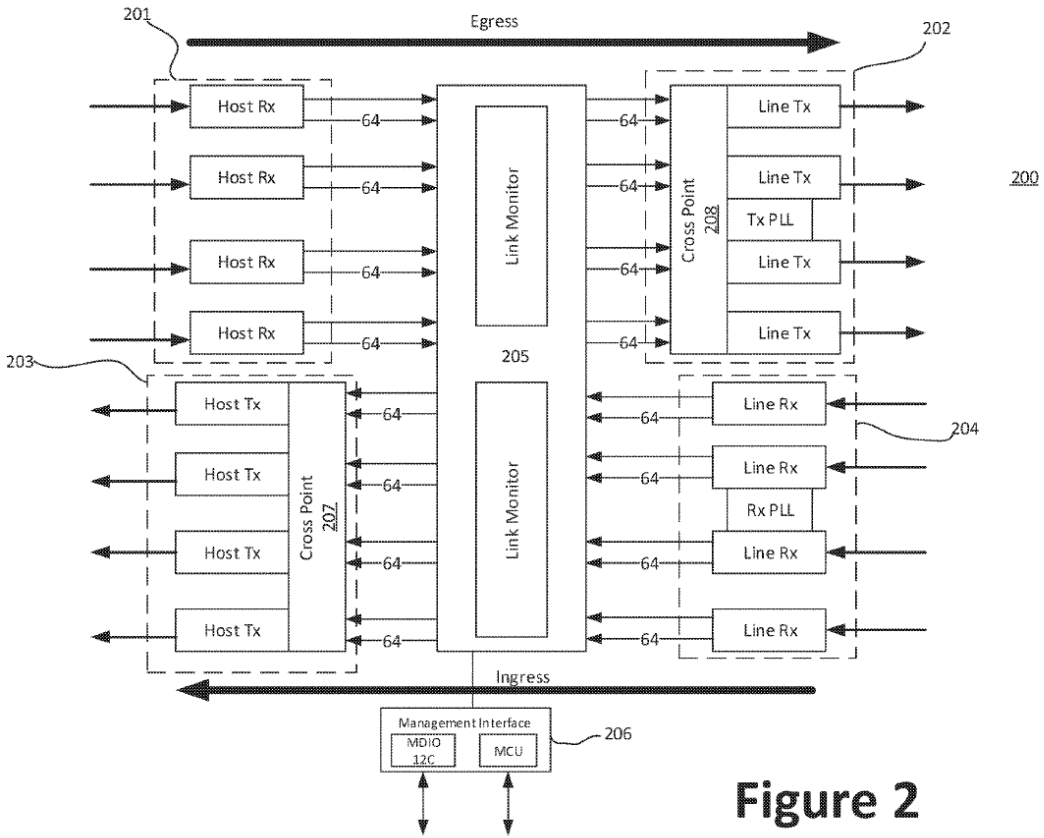
Claim 6	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 6	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 6	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 6	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 **Figure 2** Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 6	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 6	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 6	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 6	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 6	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 6	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 6	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 6	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

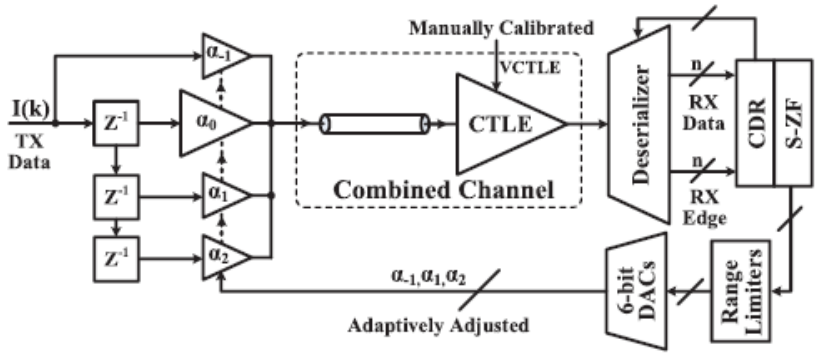
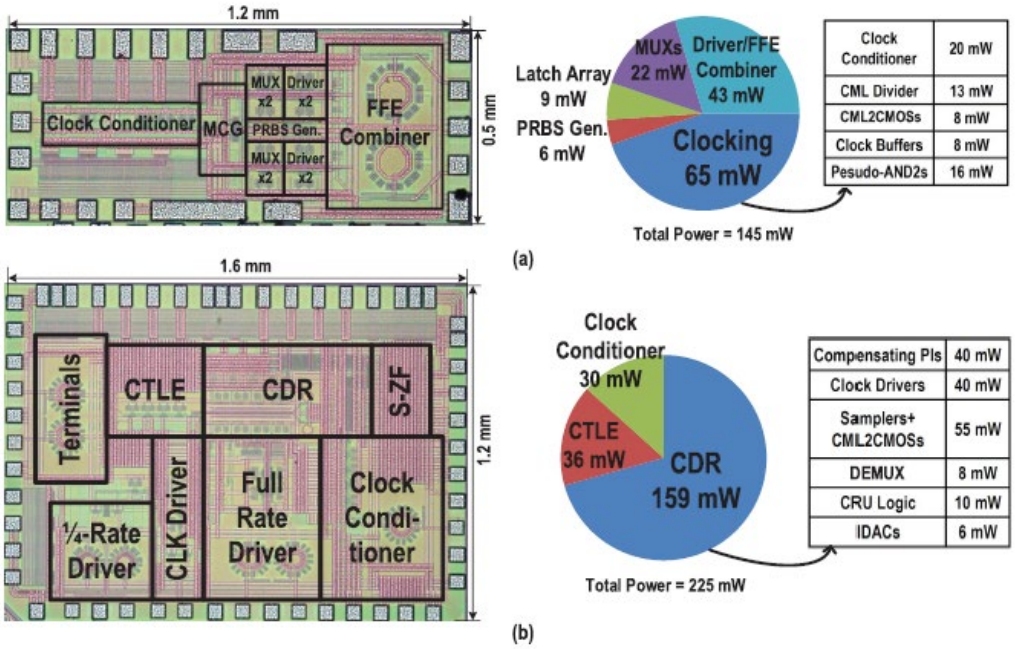


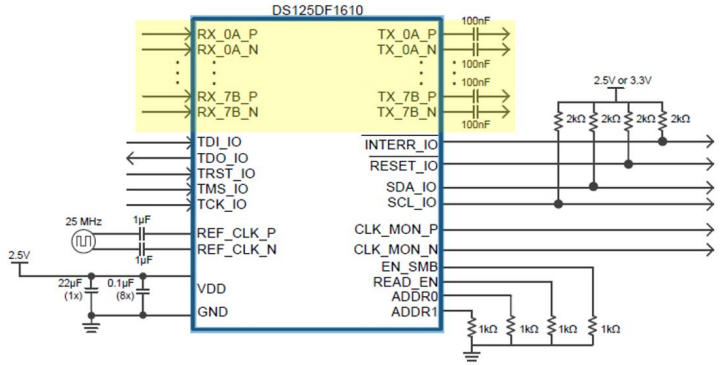
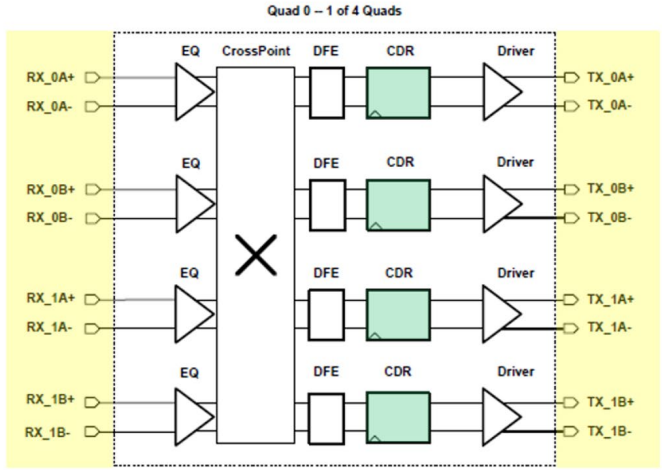
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

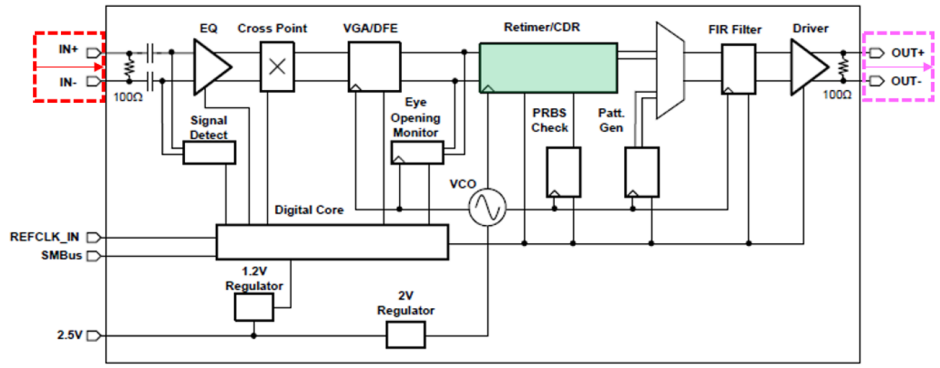
Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK"

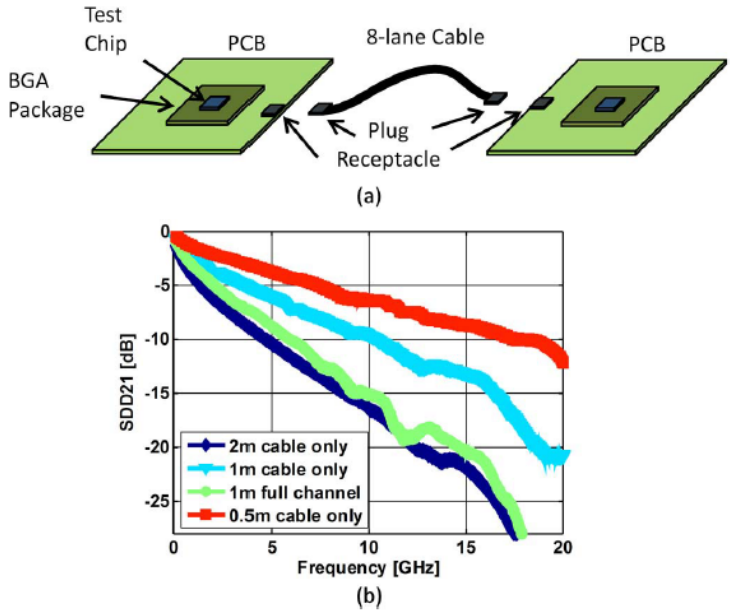
Claim 6	Disclosure
	Kobayashi, 4:4-22. <u>*DS125DF1610 Retimer Publication*</u> The DS125DF1610 circuit is illustrated in the Simplified Schematic and Figure 1 below. The highlighted pins illustrate sixteen channels of data, with each channel having two differential (Positive and Negative) input pins (RX_0A_P/N through RX_7B_P/N) to receive the channel of data and corresponding output pins (TX_0A_P/N through TX_7B_P/N) to transmit the channel of data after processing. *See, e.g.*, DS125DF1610 at §§ 3, 7.2. Thus, DS125DF1610's retimer is a transceiver that, when used in Tang's cable, receives one or more inbound data streams (on RX_0A_P/N through RX_7B_P/N), and transmits one or more transit data streams (via pins TX_0A_P/N through TX_7B_P/N).

Claim 6	Disclosure
	Simplified Schematic   **Figure 1. DS125DF1610 Simplified Cross Point Diagram** Figure 1 above shows four channels and illustrates that DS125DF1610's retimer processes each data channel by, inter alia, performing "clock and data recovery (CDR)." *See id.* at §§ 3, 7.1. A channel's data path is shown in more detail in DS125DF1610 Figure 2 (below), which illustrates the input signal conveying an inbound data stream and the transit signal conveying a transit data stream in Tang's cable

Claim 6	Disclosure
	when DS125DF1610's retimer implements Tang's signal driver 44.  **Figure 2. DS125DF1610 Simplified Data Path Diagram** The Retimer/CDR circuit performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream. *See id*. at § 7.3.6. The '252 Patent specification makes clear that the input signal from the host can be pre-processed before CDR is performed on it. An ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data for output as the transit data stream because after extracting the input signal's timing and using that timing to sample and extract the input signal's data in an analog-to-digital CDR process, the retimer generates a new data stream for equalization by the FIR Filter (a digital-to-analog process) and to be driven for output by the differential driver (which produces an analog signal with configurable output voltage levels) to convey the output data stream (transit data stream when outputting over the cable) as an analog signal over the cable conductors, where the new signal is a "re-modulation" of the data. *See id*. at §§ 7.3.6-7.3.9.
6[g] performing clock and data recovery on the first electrical transit	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

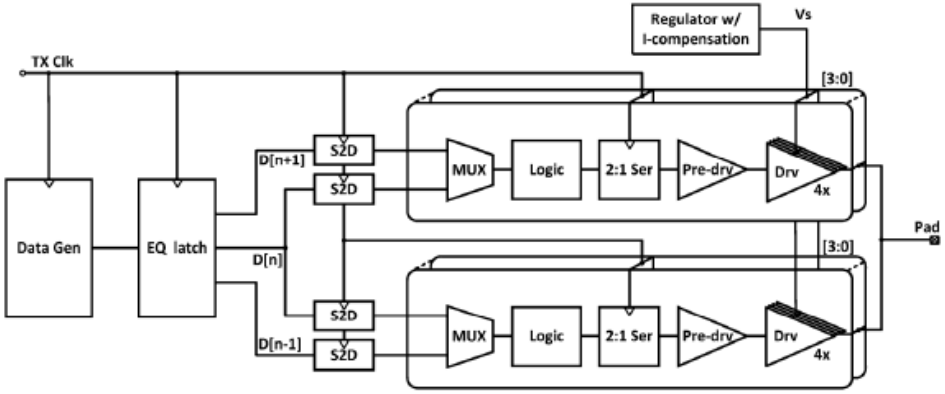
Claim 6	Disclosure
signal with the second transceiver to extract the first transit data stream;	*Abstract*—**This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

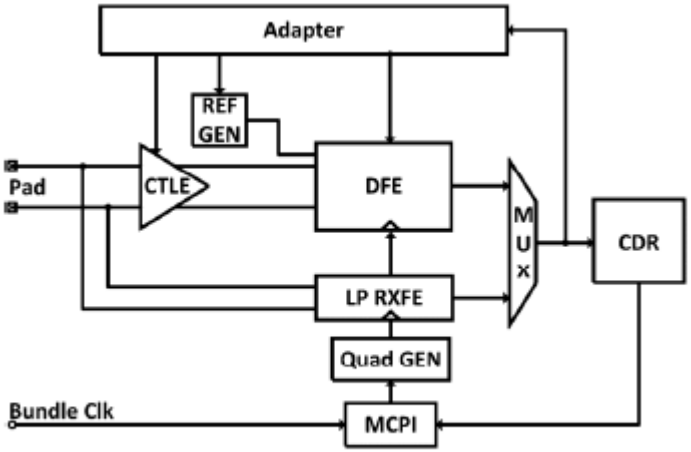
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

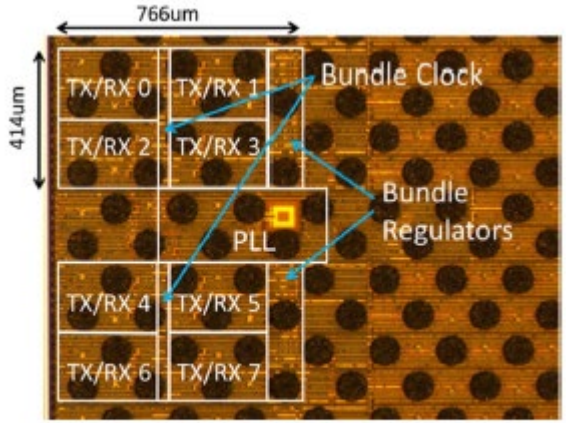
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

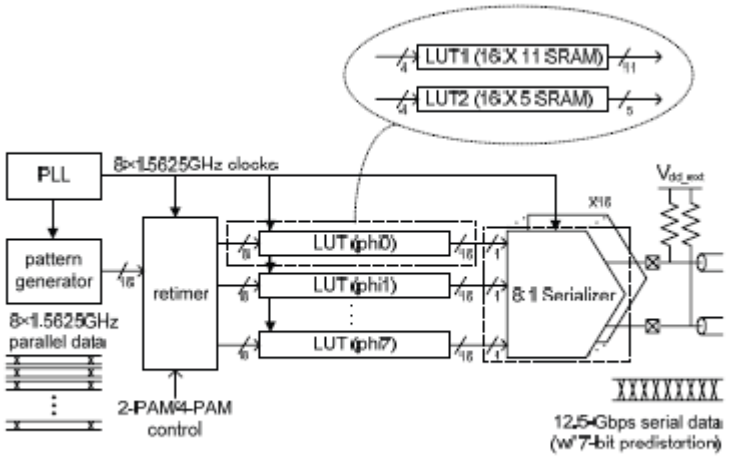
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

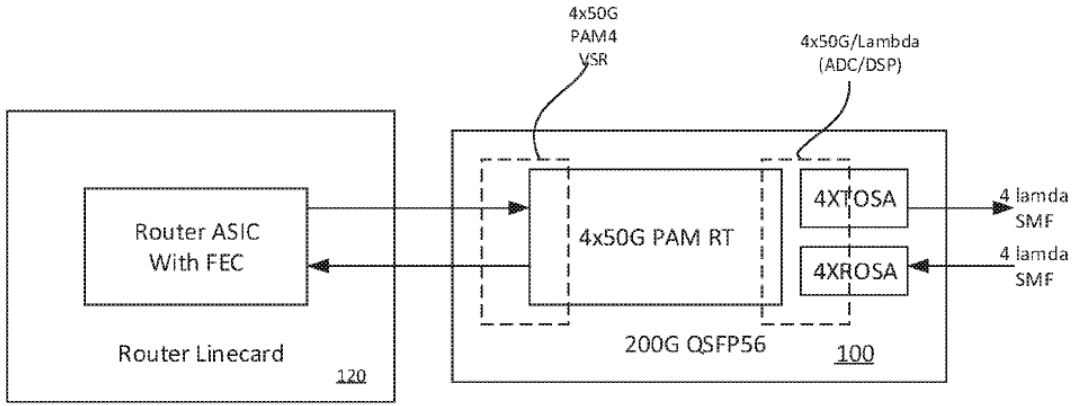
Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

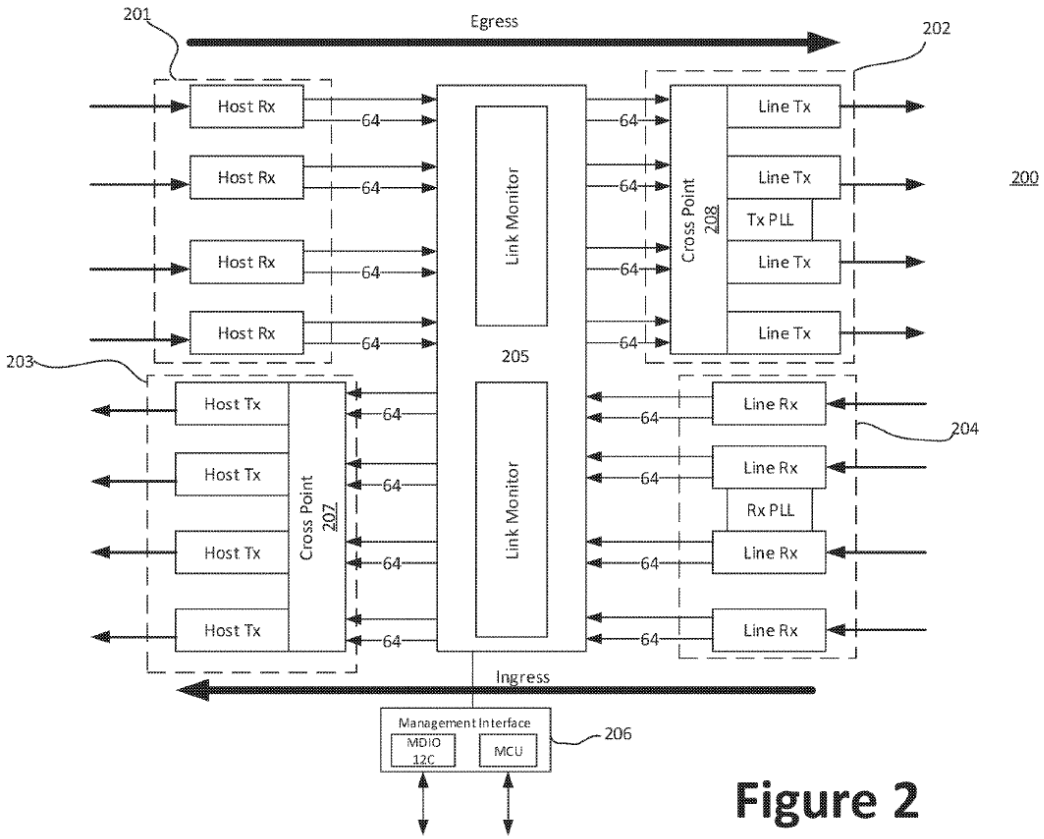
Claim 6	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 6	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 6	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 6	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 6	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 6	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 6	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 6	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 6	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 6	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 6	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 6	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

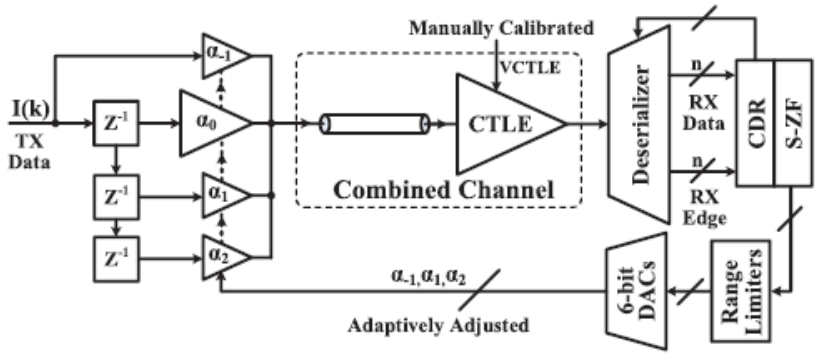
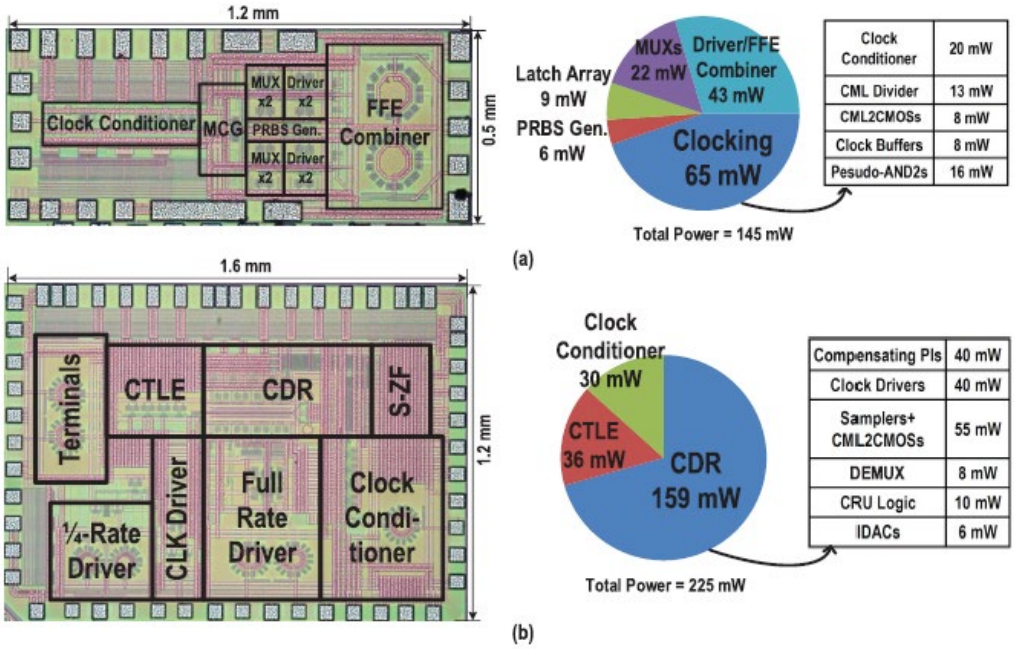
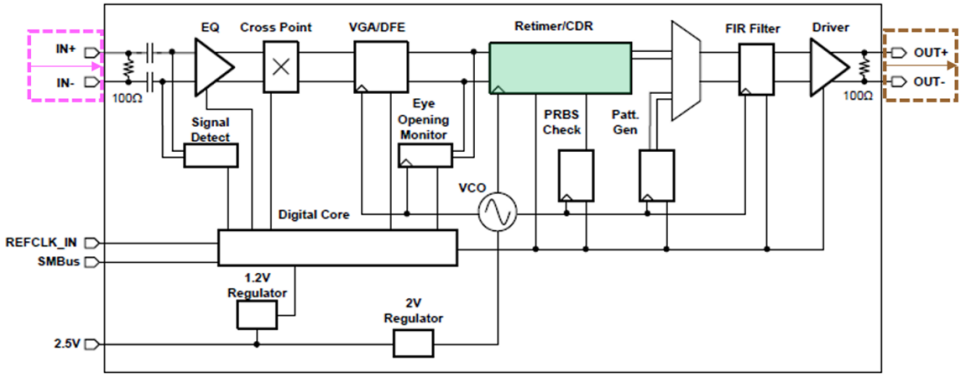


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

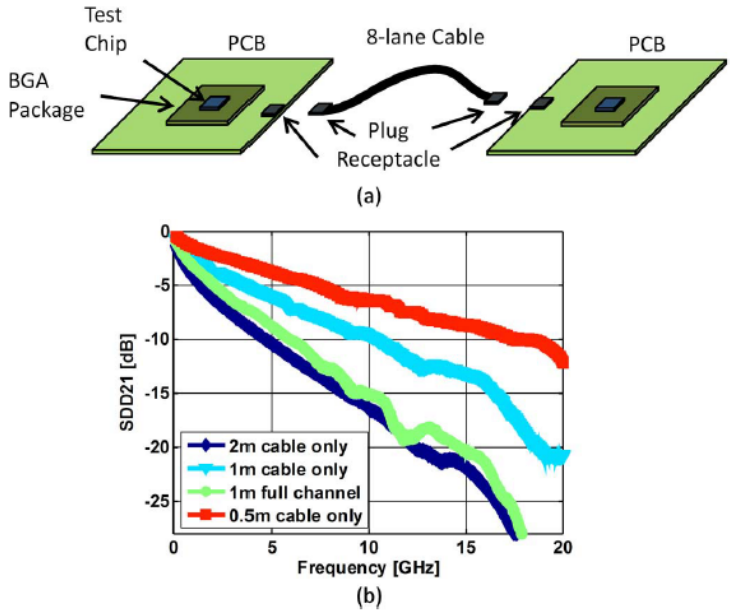
Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK"

Claim 6	Disclosure
	Kobayashi, 4:4-22. *DS125DF1610 Retimer Publication* The DS125DF1610 retimer performs CDR for respective transit signals conveying transit data streams received from electrical conductors to generate output signals conveying outbound data streams that exit cable 10 to respective hosts, as shown in DS125DF1610 Fig. 2 below. For similar reasons to those discussed in claim limitation 1[c], an ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data as the outbound data after extracting the input signal's data and generating a newly-timed signal that is a "re-modulation" of the data.  **Figure 2. DS125DF1610 Simplified Data Path Diagram**
6[h] re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

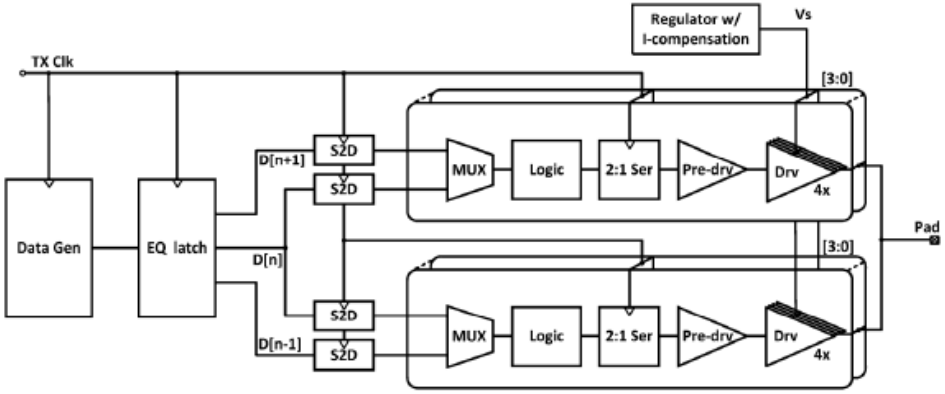
Claim 6	Disclosure
device;	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

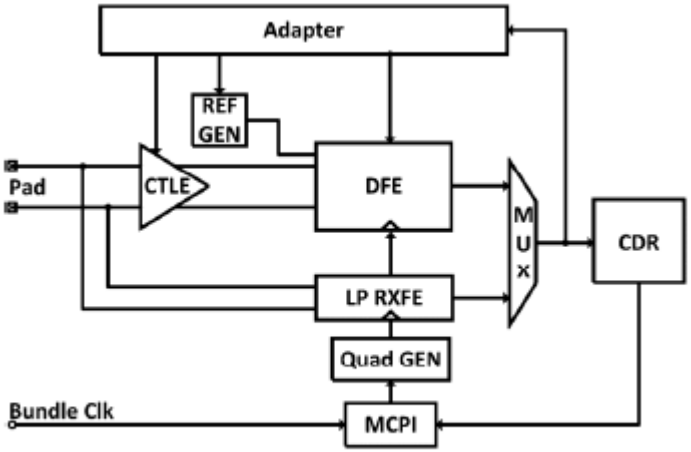
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

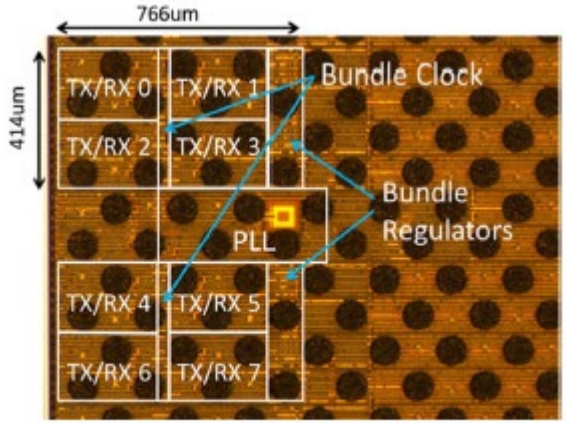
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

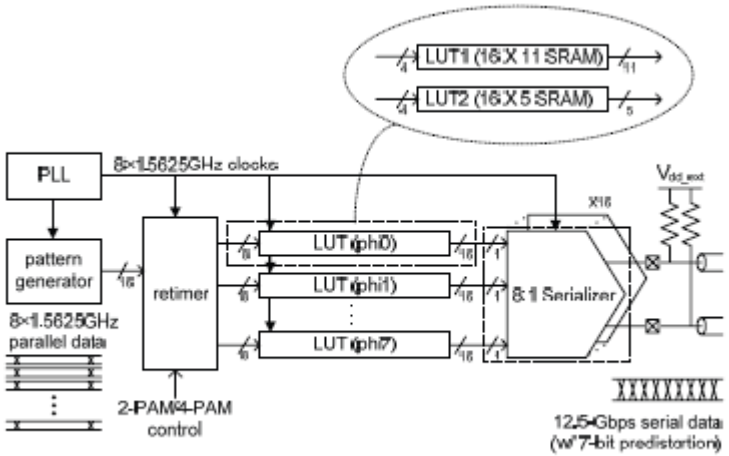
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

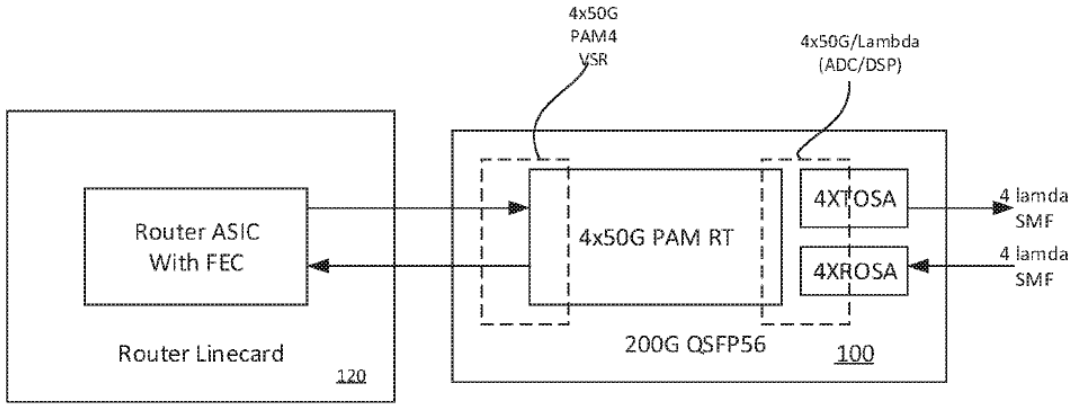
Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

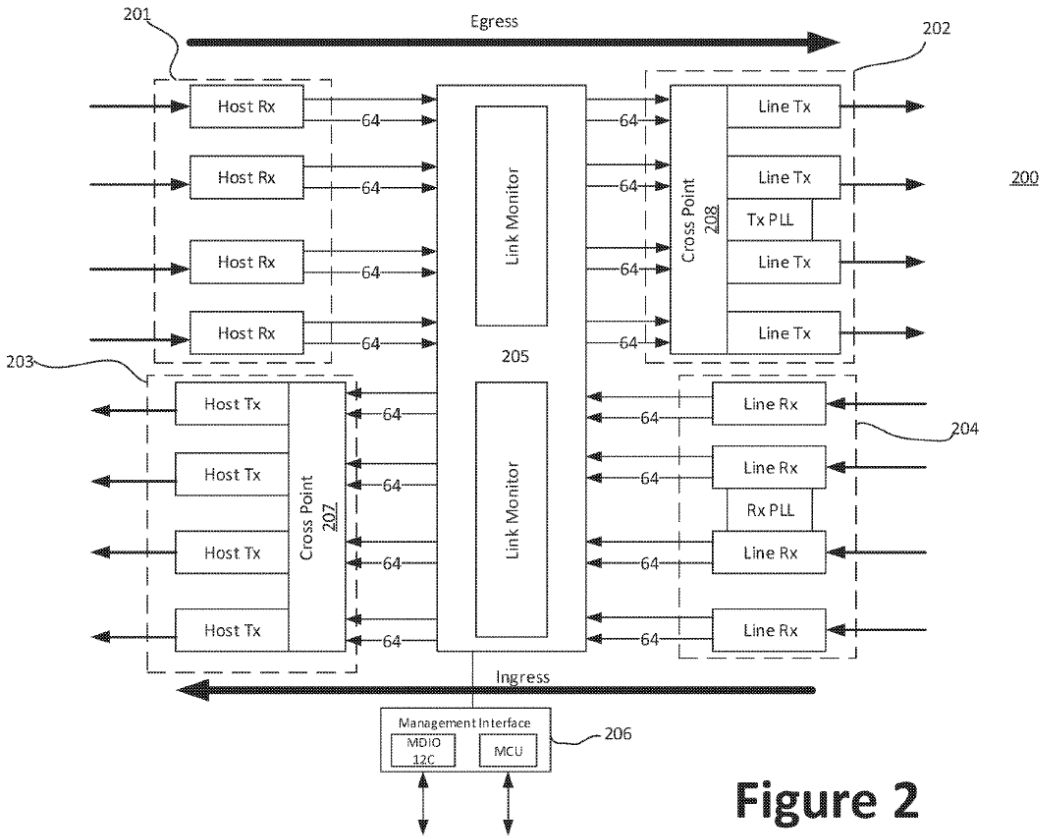
Claim 6	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 6	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 6	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 6	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 **Figure 2** Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 6	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 6	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 6	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 6	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 6	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 6	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 6	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 6	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

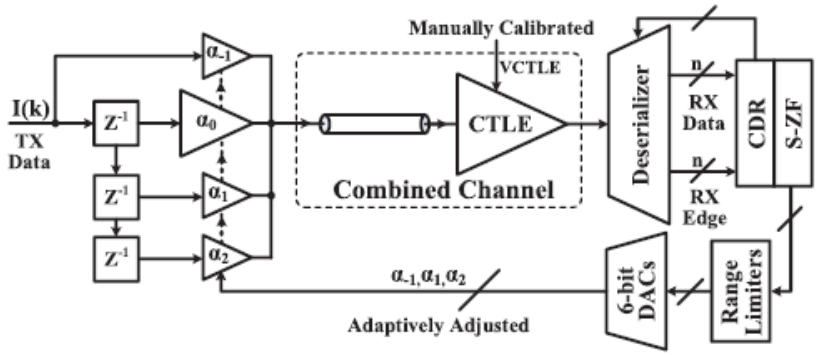
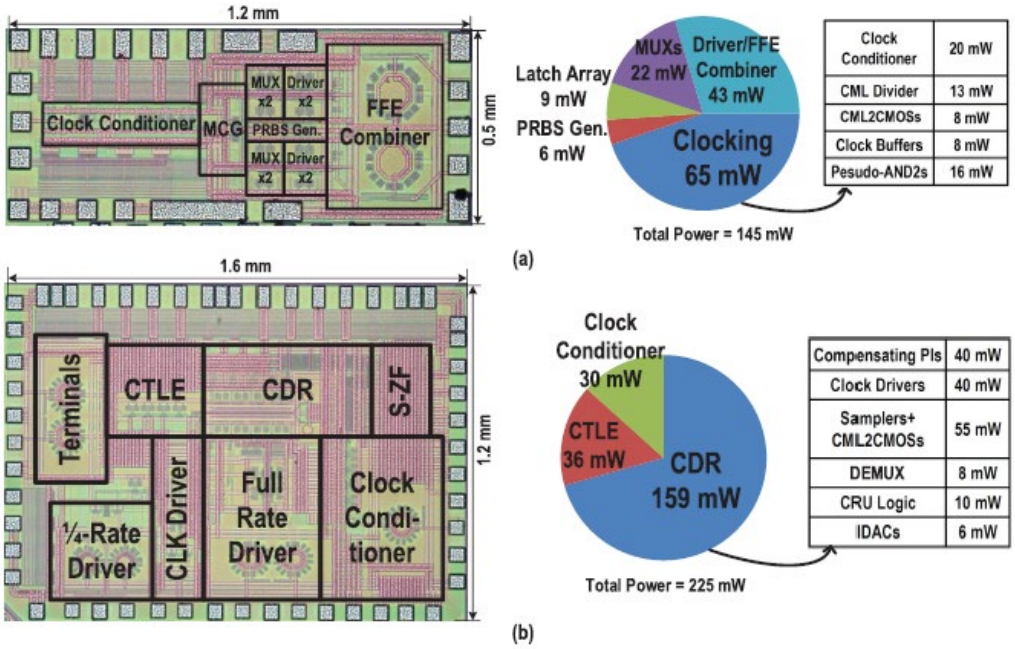
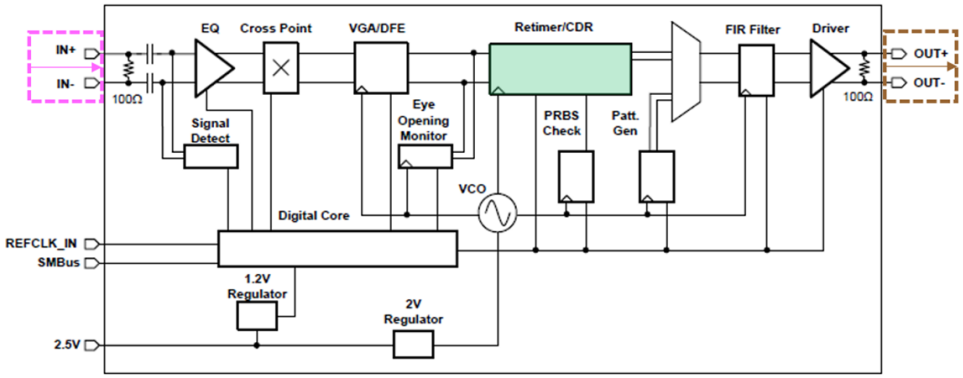


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

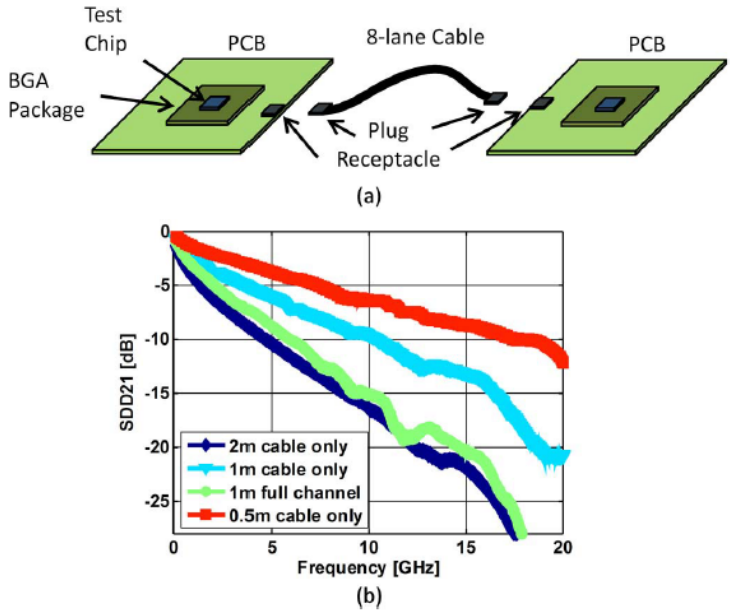
Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK"

Claim 6	Disclosure
	Kobayashi, 4:4-22. <u>*DS125DF1610 Retimer Publication*</u> The DS125DF1610 retimer performs CDR for respective transit signals conveying transit data streams received from electrical conductors to generate output signals conveying outbound data streams that exit cable 10 to respective hosts, as shown in DS125DF1610 Fig. 2 below. For similar reasons to those discussed in claim limitation 1[c], an ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data as the outbound data after extracting the input signal's data and generating a newly-timed signal that is a "re-modulation" of the data.  **Figure 2. DS125DF1610 Simplified Data Path Diagram**
6[i] performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

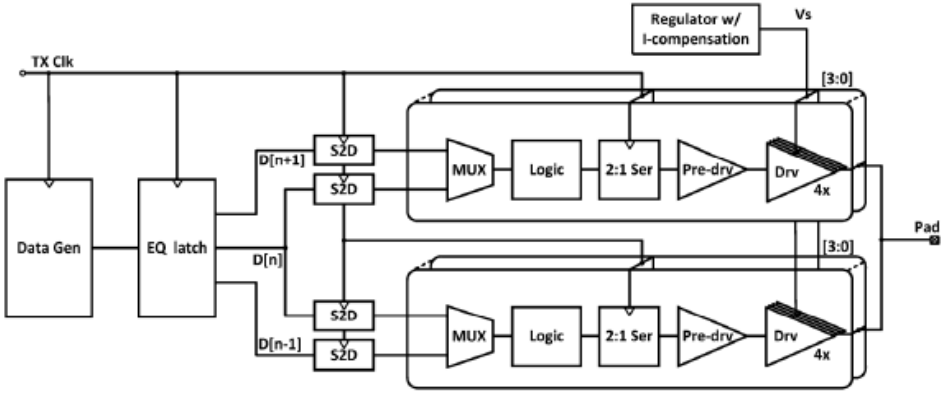
Claim 6	Disclosure
second transit data stream; and	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm².** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

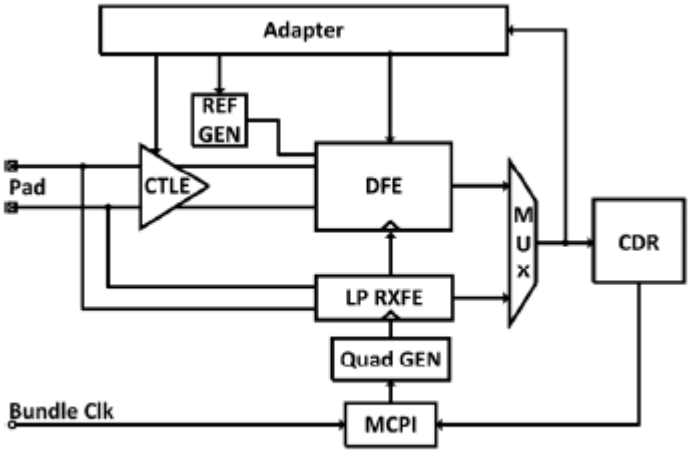
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

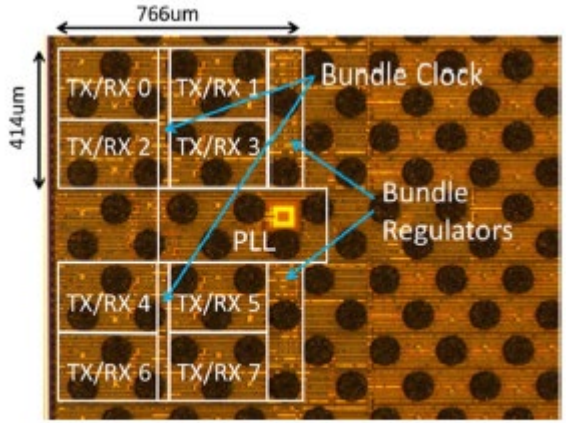
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

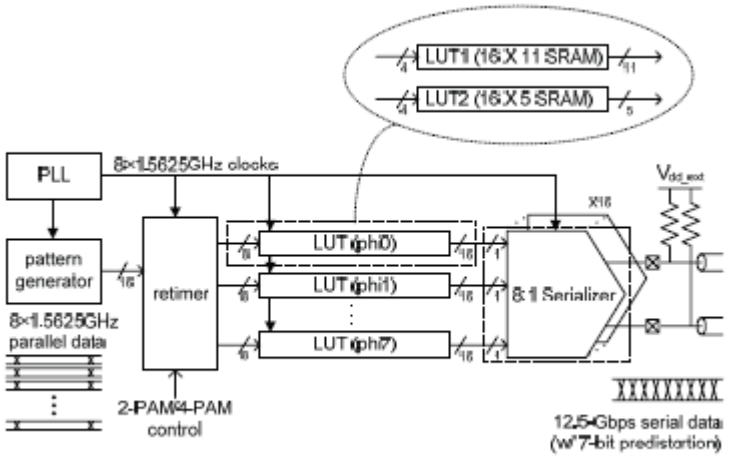
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

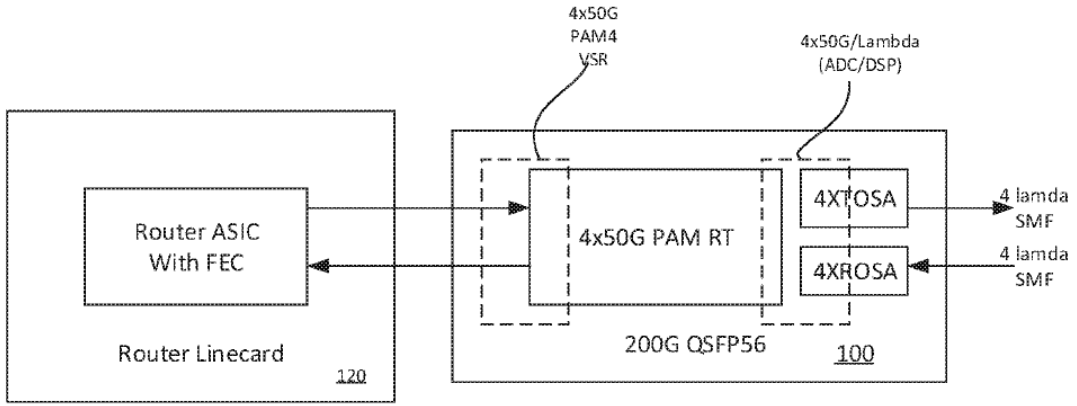
Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

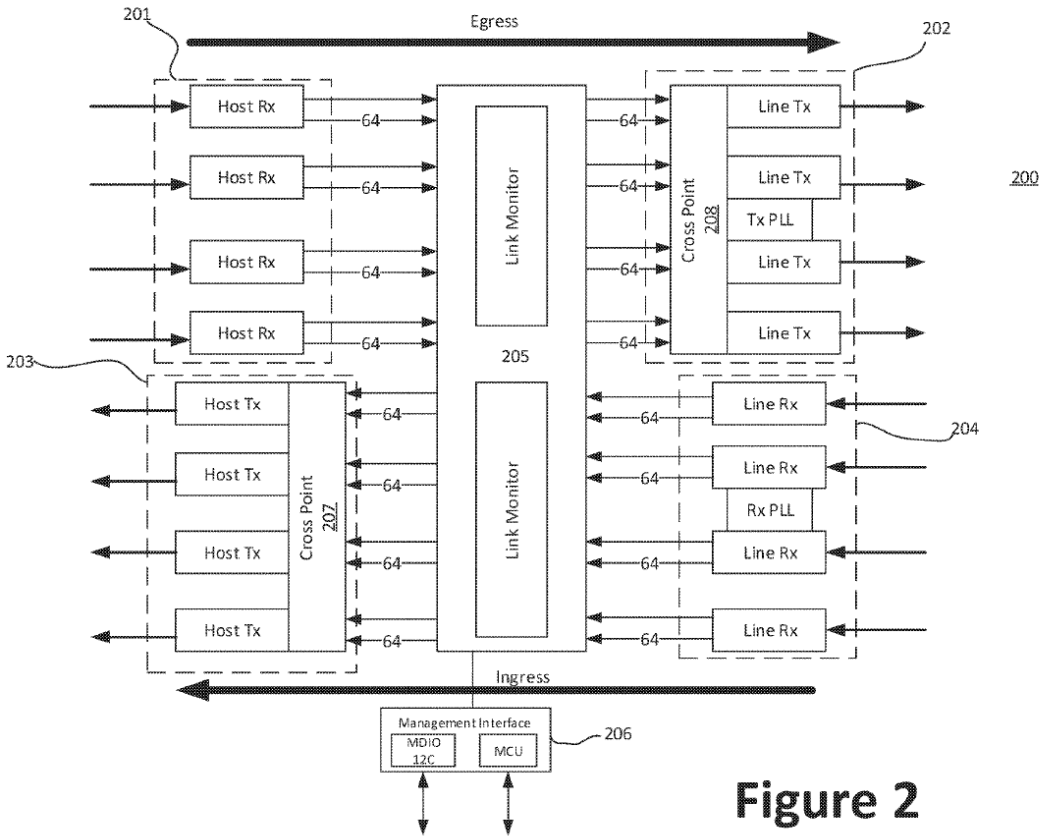
Claim 6	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 6	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 6	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 6	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 **Figure 2** Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 6	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 6	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 6	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 6	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 6	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 6	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 6	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 6	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

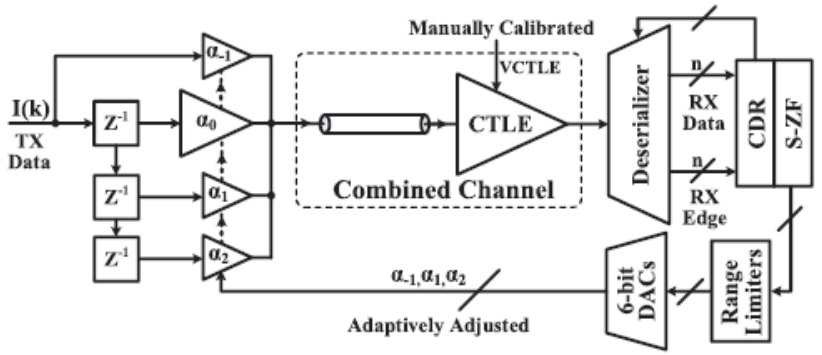
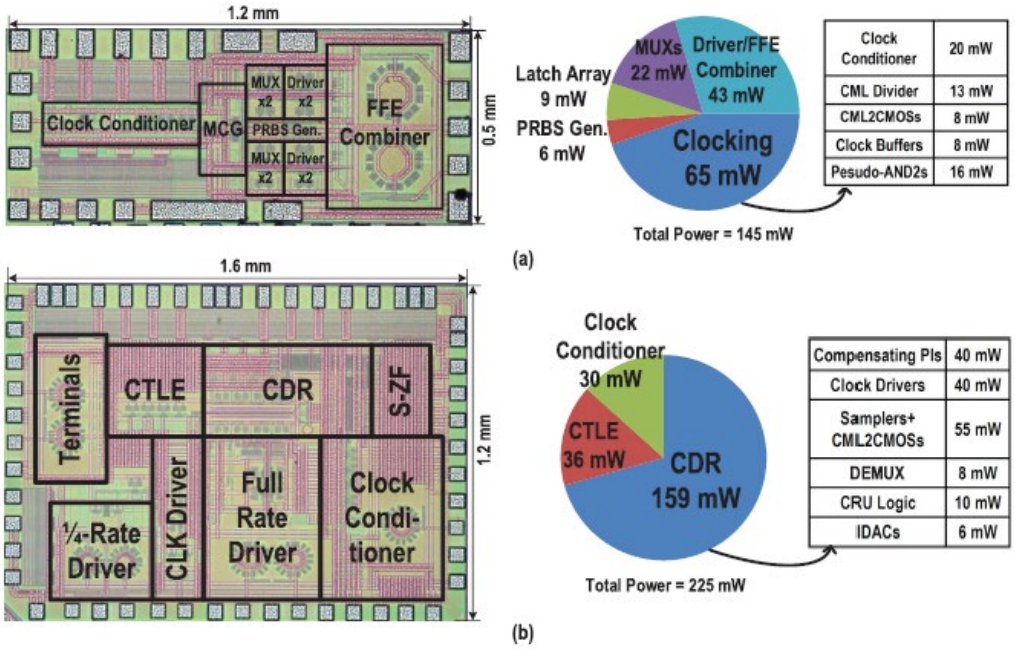
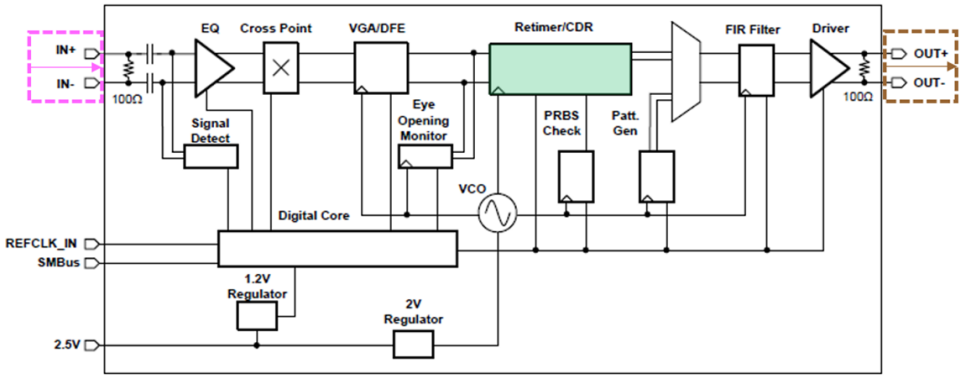


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

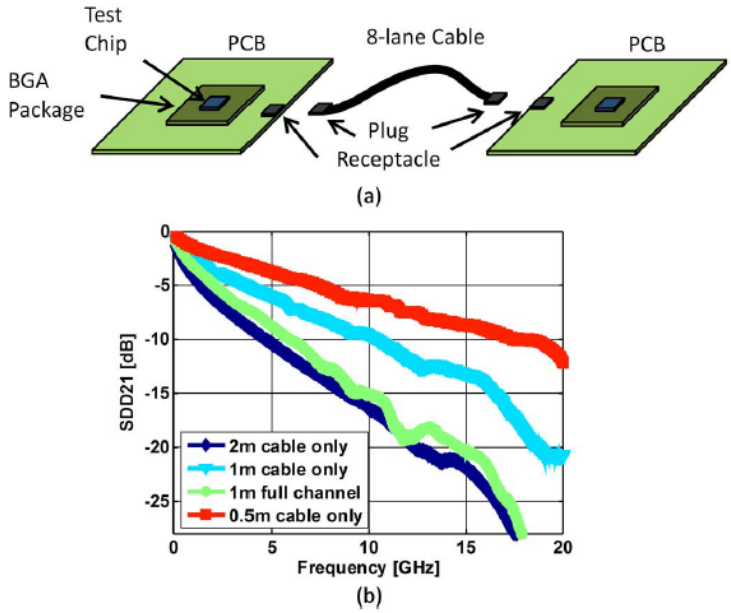
Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK"

Claim 6	Disclosure
	Kobayashi, 4:4-22. <u>*DS125DF1610 Retimer Publication*</u> The DS125DF1610 retimer performs CDR for respective transit signals conveying transit data streams received from electrical conductors to generate output signals conveying outbound data streams that exit cable 10 to respective hosts, as shown in DS125DF1610 Fig. 2 below. For similar reasons to those discussed in claim limitation 1[c], an ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data as the outbound data after extracting the input signal's data and generating a newly-timed signal that is a "re-modulation" of the data.  **Figure 2. DS125DF1610 Simplified Data Path Diagram**
6[j] re-modulating the second transit data stream as a first outbound data stream conveyed by a first	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

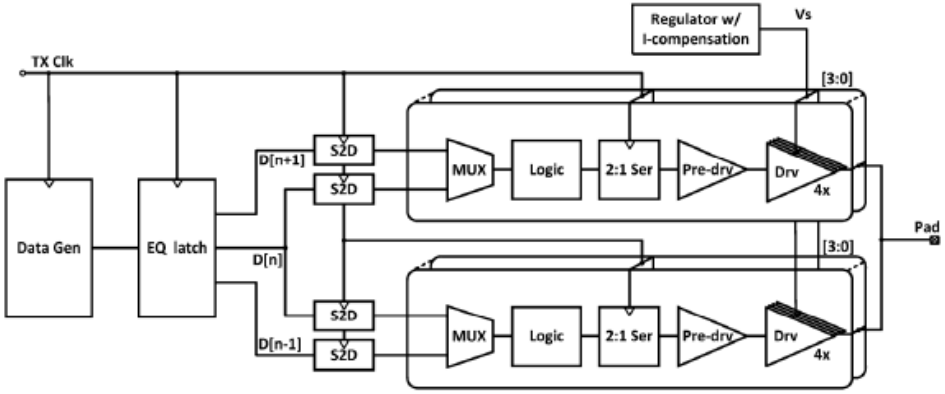
Claim 6	Disclosure
electrical output signal to the first host device,	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

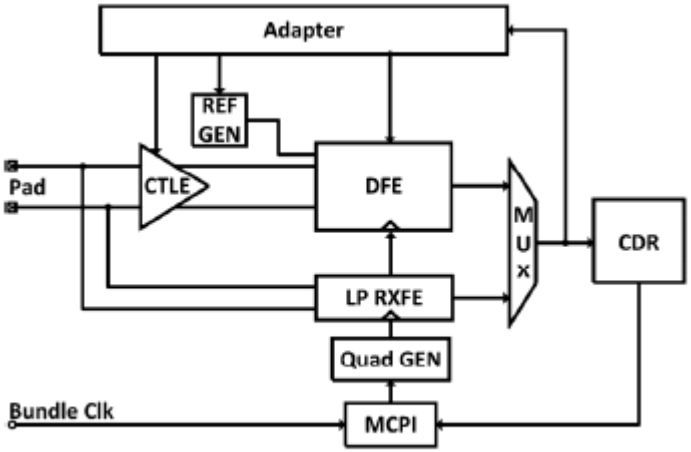
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

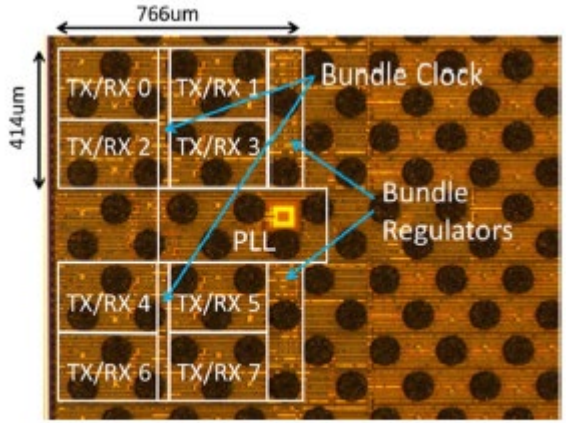
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

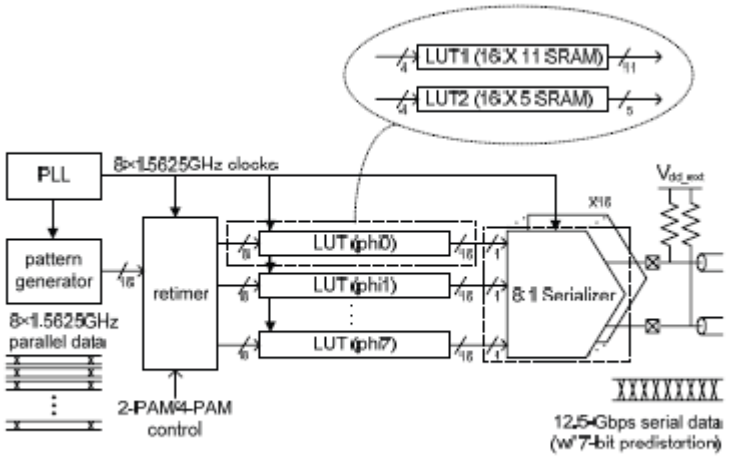
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

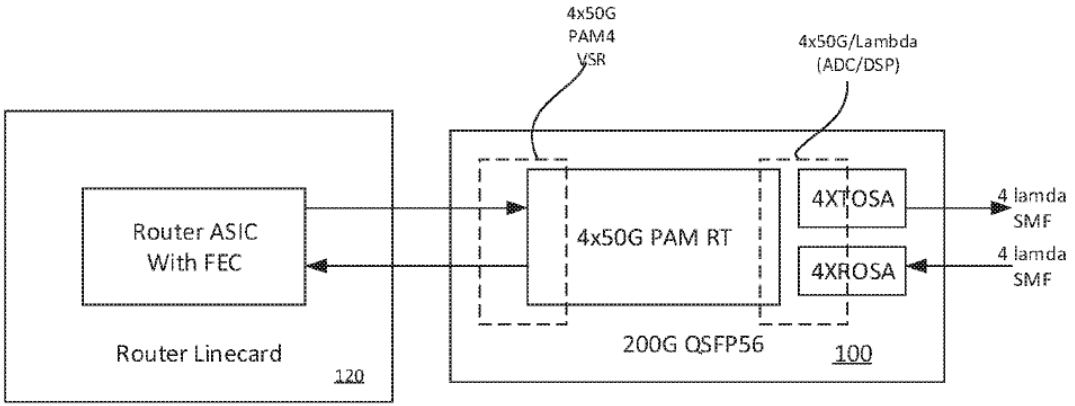
Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

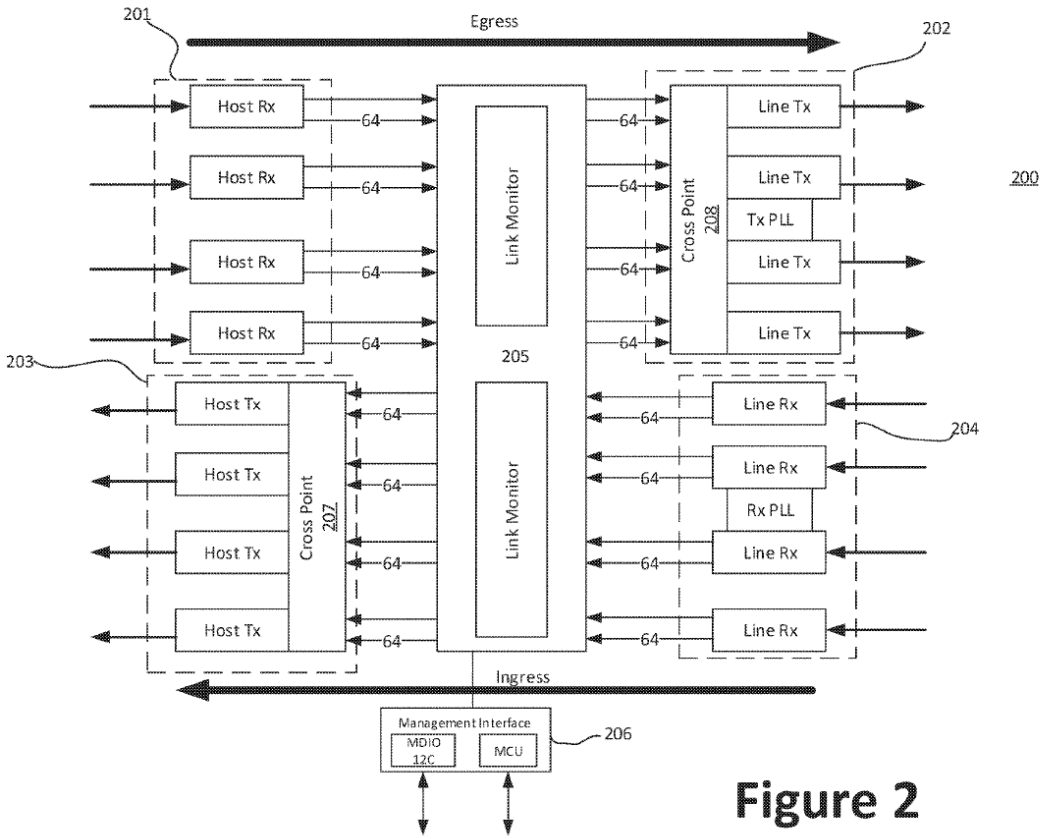
Claim 6	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 6	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 6	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 6	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 6	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 6	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 6	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 6	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 6	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 6	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 6	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 6	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

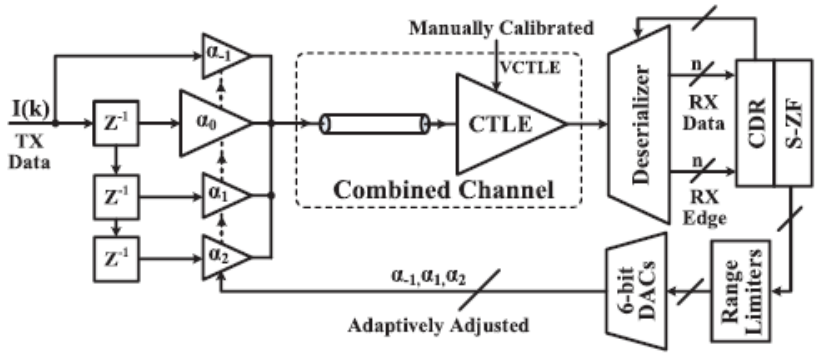
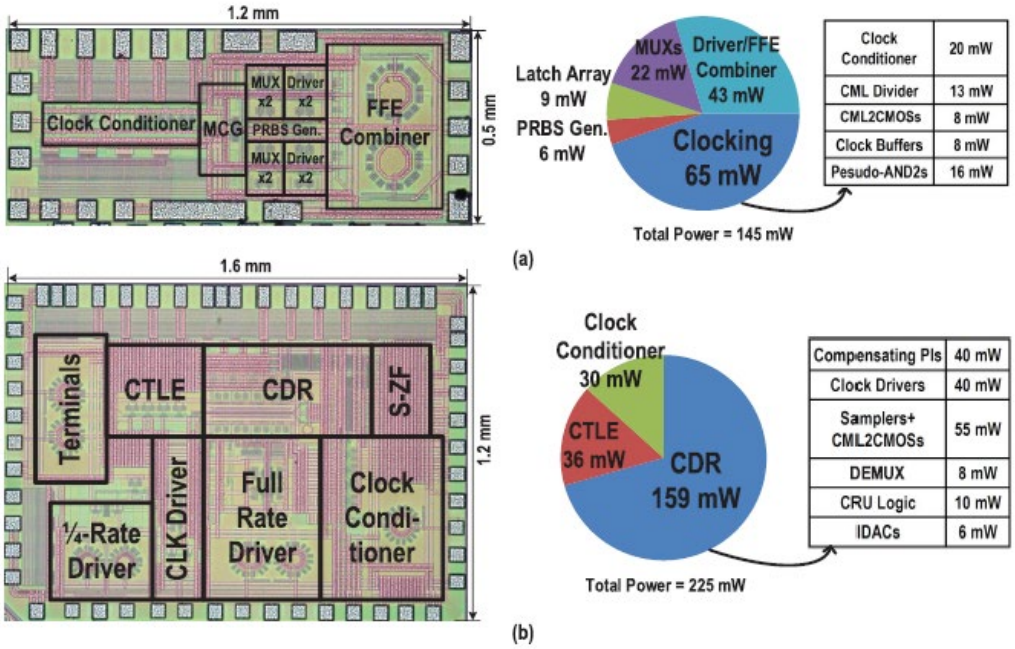
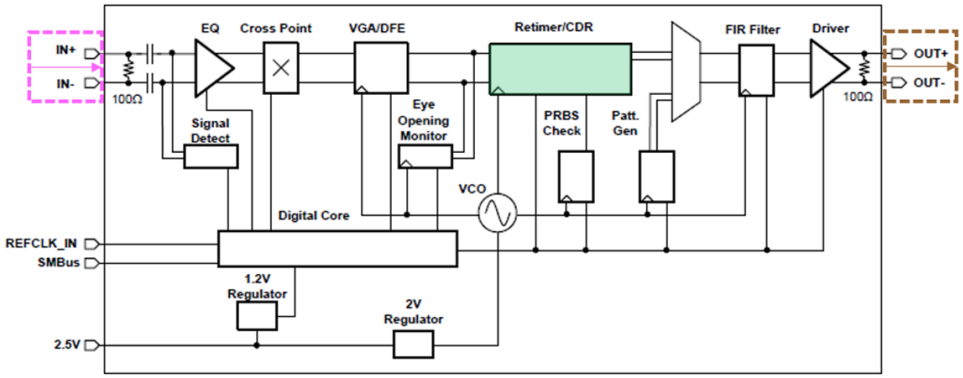


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK"

Claim 6	Disclosure
	Kobayashi, 4:4-22. <u>*DS125DF1610 Retimer Publication*</u> The DS125DF1610 retimer performs CDR for respective transit signals conveying transit data streams received from electrical conductors to generate output signals conveying outbound data streams that exit cable 10 to respective hosts, as shown in DS125DF1610 Fig. 2 below. For similar reasons to those discussed in claim limitation 1[c], an ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data as the outbound data after extracting the input signal's data and generating a newly-timed signal that is a "re-modulation" of the data.  **Figure 2. DS125DF1610 Simplified Data Path Diagram**
6[k] wherein said re-modulating the first transit data stream, said remodulating the second transit data stream, said	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

Claim 6	Disclosure
performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.	Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp. CMIS, 22.

Claim 6	Disclosure
	1.5.4 Control Set Overview A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 6	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 6	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 6	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 6	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 6	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 6	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

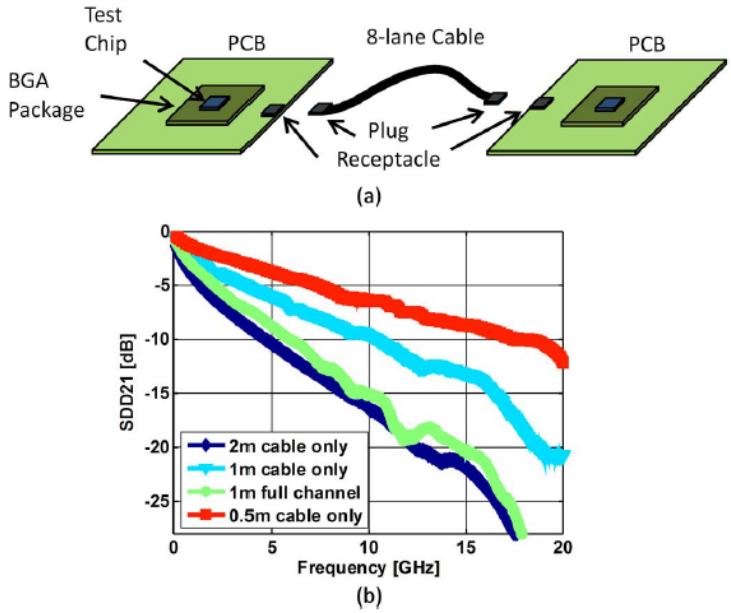
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

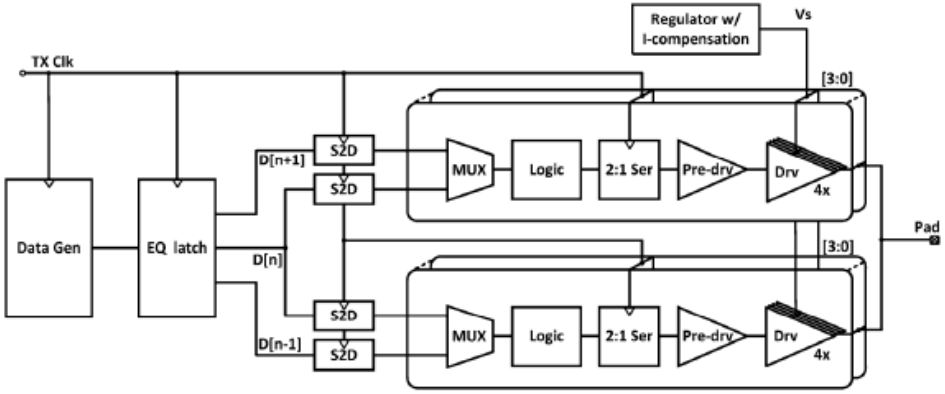
Claim 6	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

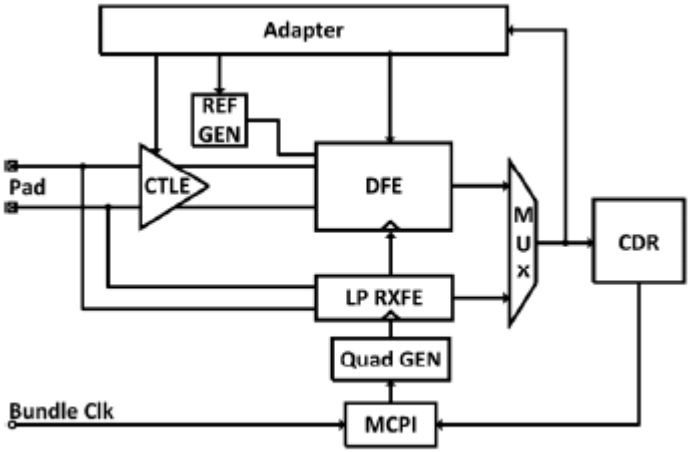
Claim 6	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 6	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 6	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

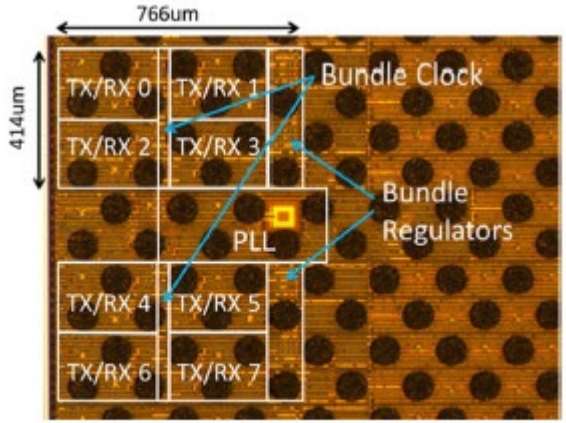
Claim 6	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 6	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 6	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

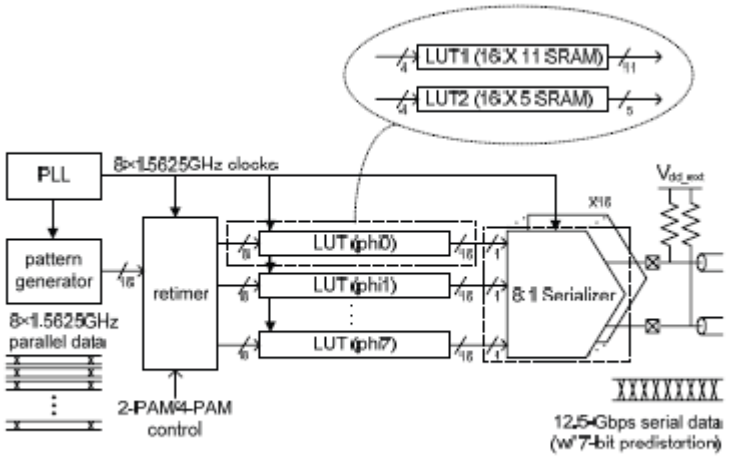
Claim 6	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 6	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 6	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

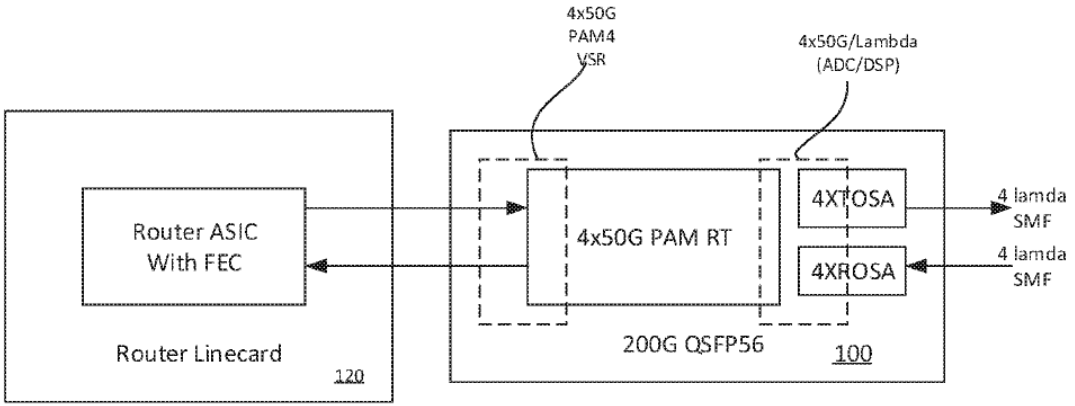
Claim 6	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

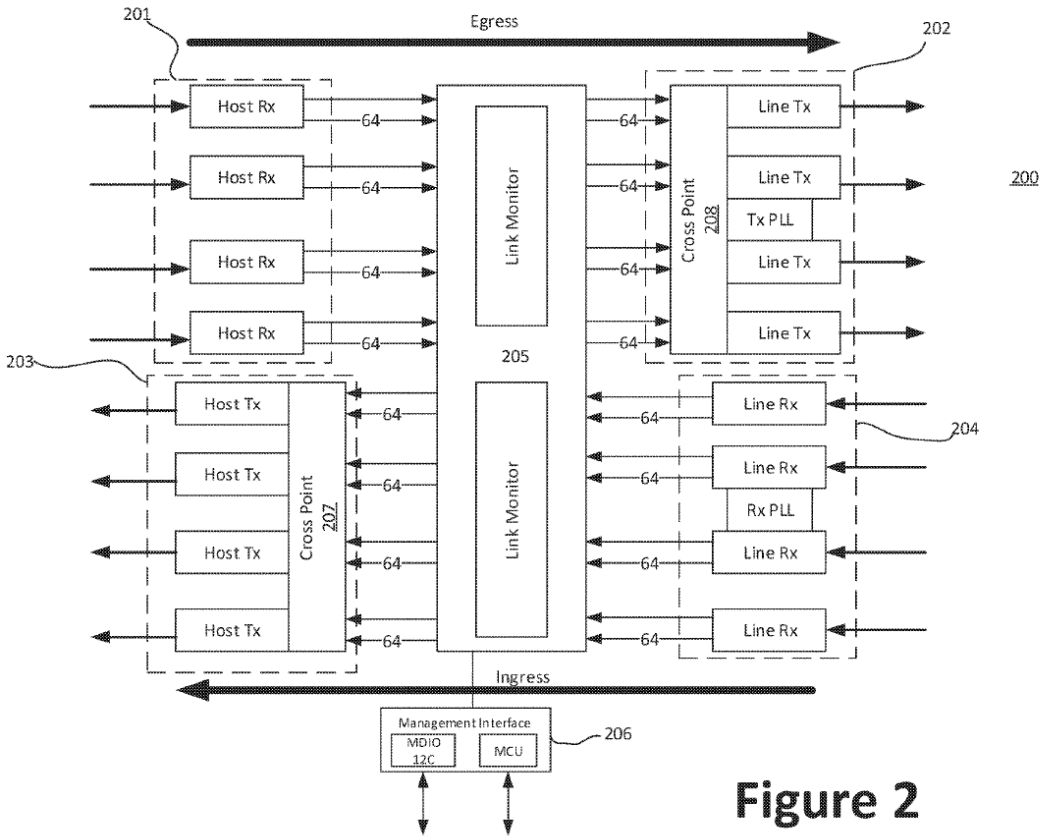
Claim 6	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 6	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 6	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 6	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 6	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 6	Disclosure
	 Riani, Figure 2.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 6	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 6	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 6	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 6	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 6	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 6	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 6	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 6	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 6	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 6	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 6	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 6	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 6	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 6	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 6	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 6	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

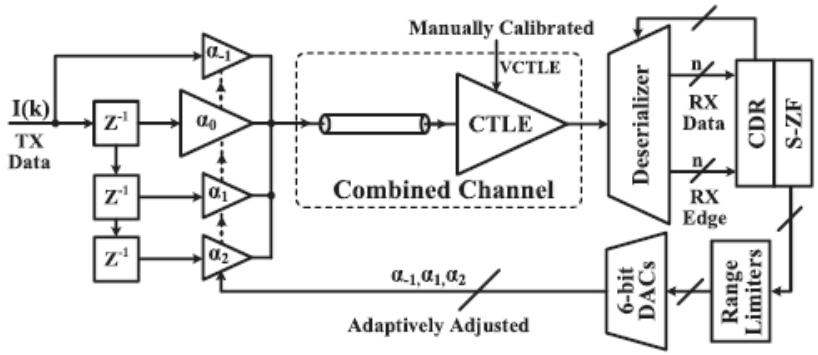
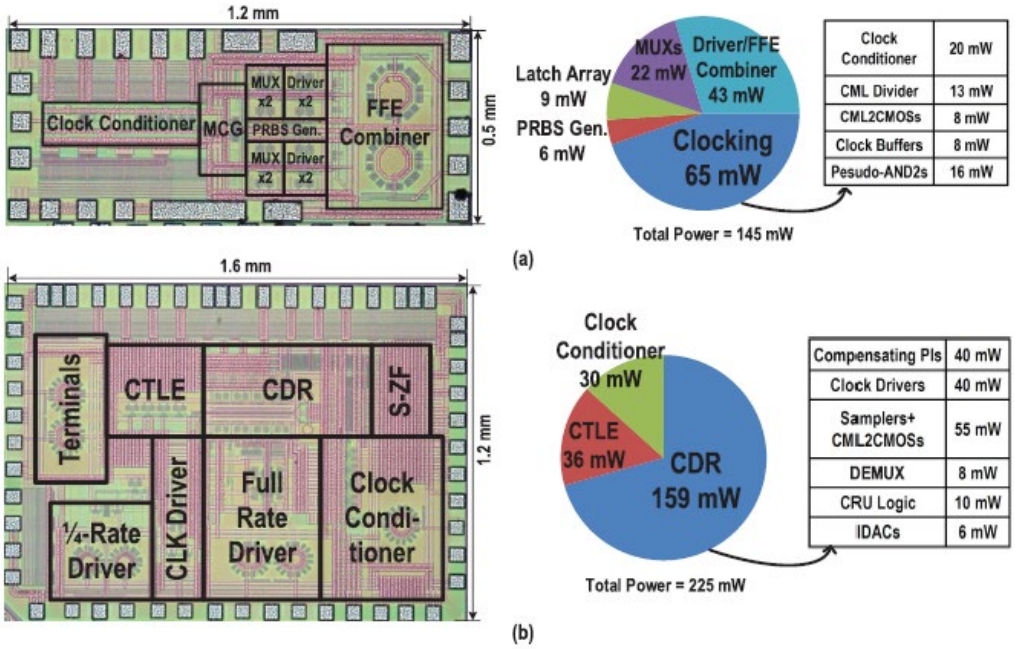


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

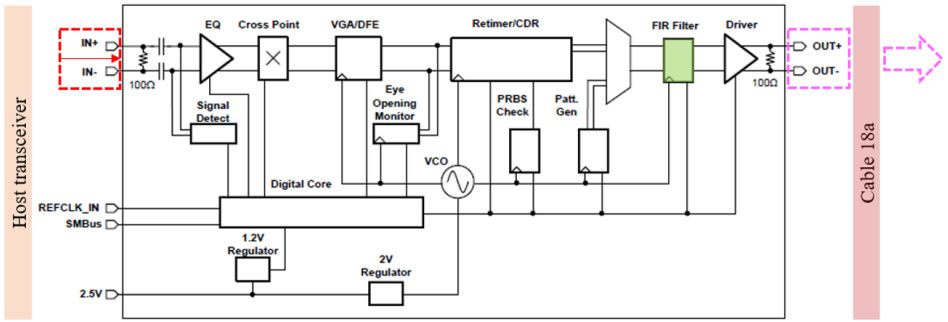
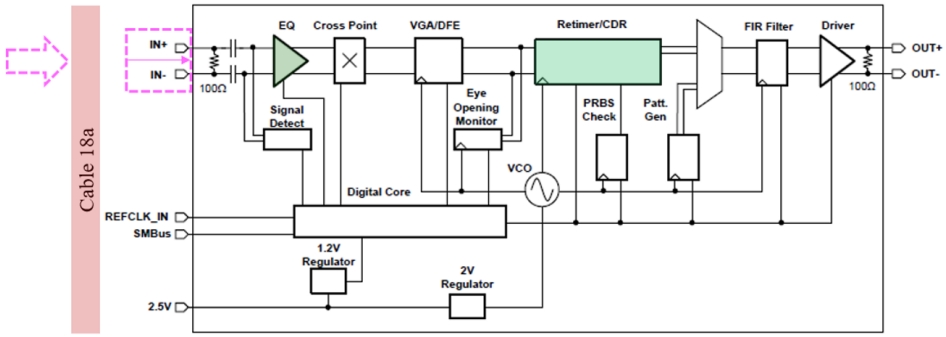
Claim 6	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

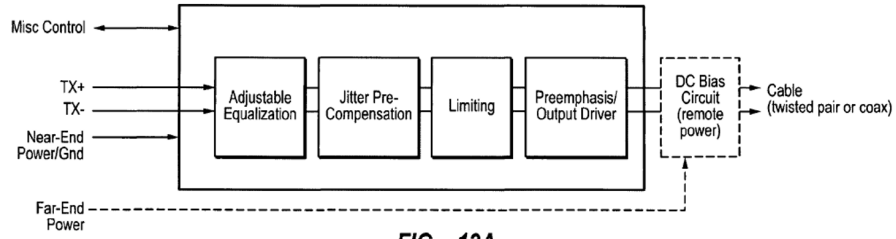
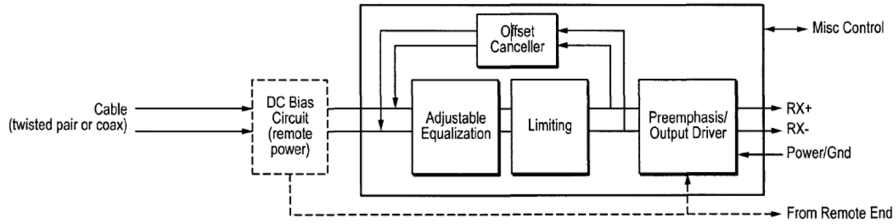
Claim 6	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 6	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The active cable 3 receives the serial bit stream transmitted from the upstream device 2 in the upstream facing RX 30a in one retimer 30. The retimer 30 performs a waveform shaping on the serial bit stream received by the upstream facing RX 30a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 30b to the other retime 31. The retimer 31 receives the serial bit stream transmitted from the retimer 30 in the upstream facing RX 31a. The retimer 31 performs a waveform shaping on the serial bit stream received by the upstream facing RX 31a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 31b to the downstream device 4." See column 3, lines 5-19. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing

Claim 6	Disclosure
	TX 52 includes a serializer and a driver." Kobayashi, 4:4-9. "The exchange module 202 is configured to communicate capabilities information with a remote link partner including host loss information, RS-FEC ability information, and RS-FEC request information. The exchange module 202 may transmit local host loss information to the link partner and receive remote host loss information from the link partner. In some embodiments, the exchange module 202 may be included in or otherwise established by the autonegotiation module 104 and thus the capabilities information may be exchanged during execution of an autonegotiation protocol. In some embodiments, the exchange module 202 may be included in or otherwise established by the PMD/PMA module 106 and thus the capabilities information may be exchanged during a startup protocol performed by the PMD/PMA module 106." Lusted, paragraph 23. "The autonegotiation module 104 is configured to auto-negotiate line transmission speed, mode of operation, and other communication parameters with a link partner when the communication lane 102 is brought up. Additionally, in some embodiments the autonegotiation module 104 may be configured to exchange capabilities information with the link partner including host insertion loss information, RS-FEC ability information, and RS-FEC request information. The autonegotiation module 104 may encode the capabilities information, for example, in an autonegotiation base page or in a next page. Although illustrated in FIG. 1 as coupled between the PMD/PMA 106 and the communication lanes 102, in other embodiments the autonegotiation module 104 may be included at different positions in the Ethernet port logic 100. For example, in some embodiments the autonegotiation module 104 may be coupled between the PMD/PMA 106 and the FEC 108." Lusted, paragraph 17. "In view of the above transmission characteristics of twisted-pair, current Ethernet chips are usually equipped with preemphasis technique of a transmitting end and equalization technique of a receiving end to compensate the difference in transmission attenuation of physical layer signals on different frequencies on the same medium during Ethernet baseband transmission. Main functions of the preemphasis technique of the transmitting end and the equalization technique of the receiving end include: amplifying signals on different frequencies differently at the transmitting end to compensate different transmission attenuation in

Claim 6	Disclosure
	the twisted pair; applying the equalization technique to different frequency components in signals received at the receiving end to compensate the attenuation." Yu, paragraph 34. "An embodiment of the present invention provides an equalizer setting apparatus, which uses a filter circuit 101, an analog-to-digital converter 102, a digital memory 103, a digital comparator 104 and a first digital accumulator 105, the filter circuit 101, the analog-to-digital converter 102, the digital memory 103, the digital comparator 104 and the first digital accumulator 105 are connected in sequence, the output end of the equalizer 201 is connected with the input end of the filter circuit 101, the output end of the first digital accumulator 105 is connected with the set value input end of the equalizer 201, the output end of the analog-to-digital converter 102 is connected with the input end of the digital comparator 104, so that the problems that the setting value of the equalizer is accurately set in the prior art, which is time-consuming and labor-consuming are solved, the method has the advantages of achieving accurate setting of the set value of the equalizer in a single time, fast, simple, convenient, accurate and low-cost manner and saving labor force to a certain extent." Yin, paragraph 26 (English translation). <u>*DS125DF1610 Retimer Publication*</u> The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610's FIR filter) and the CDR performed on the electrical input signal (by the DS125DF1610's EQ). DS125DF1610's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See id.* at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit

Claim 6	Disclosure
	signal.”  Figure 2. DS125DF1610 Simplified Data Path Diagram  Figure 2. DS125DF1610 Simplified Data Path Diagram *U.S. Patent No. 7,762,727 to Aronson* Aronson discloses an active cable for high-speed transmissions between network nodes. See, e.g., Aronson at Abstract, 1:12-21. While Aronson’s title recites an optical cable, Aronson also discloses copper twisted-

Claim 6	Disclosure
	pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.  *FIG. 12A*  *FIG. 12B* Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23. Aronson discloses the host-side equalization and pre-equalization use fixed cable-independent parameters to address host-side losses. *See, e.g.*, Aronson at 12:10-17, 14:16-23, 15:17-24. "Fixed" parameters reduced complexity and manufacturing costs. See, e.g., U.S. Patent No. 7,239,665 at 1:7-18 (discussing slow

Claim 6	Disclosure
	convergence with adaptive equalization); U.S. Patent App. Pub. No. 2011/0228821 at [0009]-[0011] (discussing tradeoffs between fixed and adaptive equalization); U.S. Patent No. 6,621,862 at 1:52-55 (large gate count for adaptive equalization can cause "high chip costs"); U.S. Patent App. Pub. No. 2006/0045176 at [0034] ("The adaptive equalizer can be trapped in a failure state (i.e., incorrect state) and not able to recover from the failure state."); U.S. Patent App. Pub. No. 2017/0187463 at [0058] ("[E]qualization techniques… come with different engineering tradeoffs, including trade-offs in power consumption, performance, and/or cost."). **5. The PCIe 3.0 Equalization Adaptation Protocol** The PCIe 3.0 Base Specification [10] requires that a compliant Tx be able to produce any of the output equalization (TxEQ) levels shown in Figure 21, whenever requested to do so by the receiving port, during link equalization training. The same specification describes a protocol of TxEQ adaptation, where the host (upstream agent) or the end device (downstream agent) can each request that any of the TxEQ values in Figure 21 be presented to them by the other agent on the link. The intent of adaptation is to allow both agents to adjust the link partner's TxEQ to an optimal value for their receiver, and for the specific channel and operating conditions at hand. Samaan, p. 24.

G. DEPENDENT CLAIM 7

Claim 7	Disclosure
7[a] The communication method of claim 6, wherein cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream,	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp.

Claim 7	Disclosure
	CMIS, 22. **1.5.4 Control Set Overview** A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 7	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 7	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 7	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 7	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 7	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 7	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

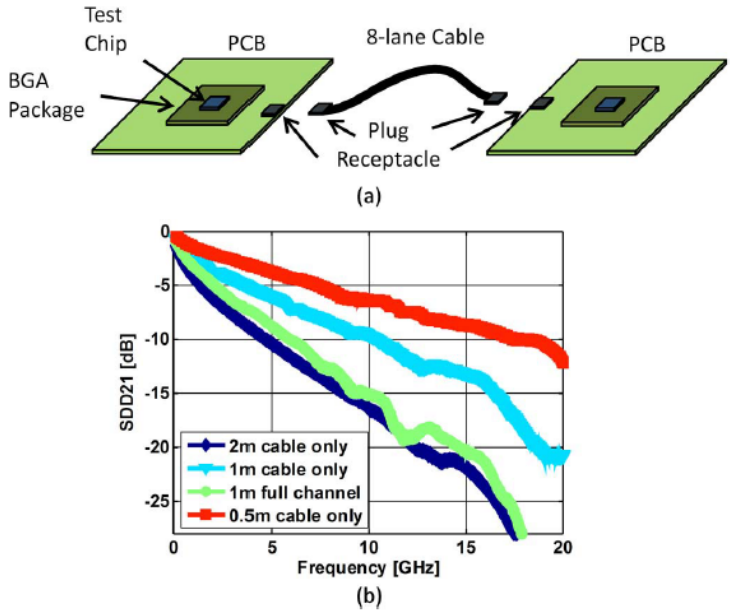
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

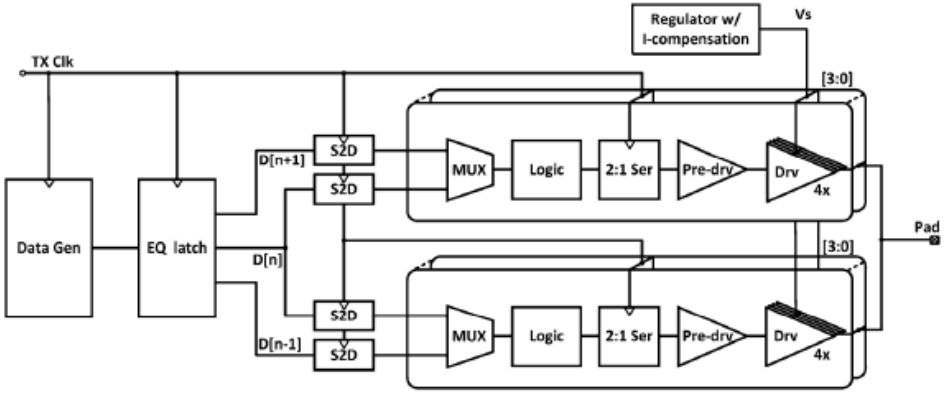
Claim 7	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

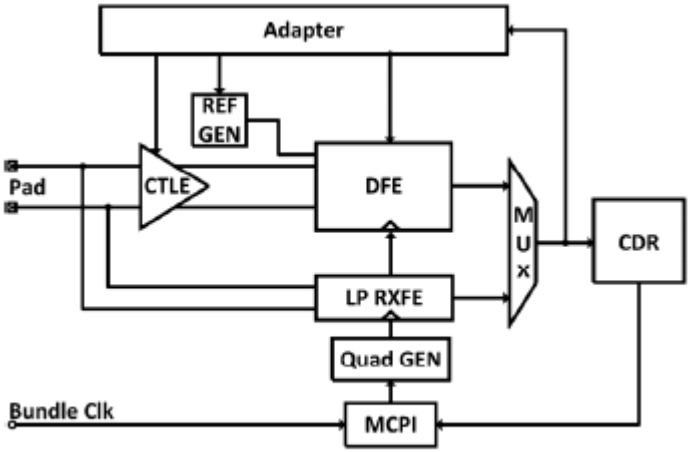
Claim 7	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 7	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 7	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

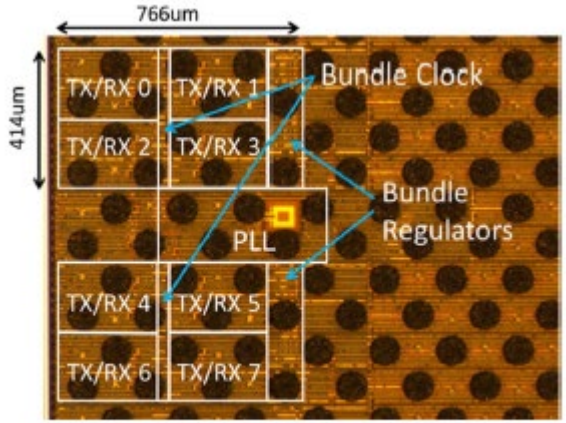
Claim 7	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 7	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 7	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

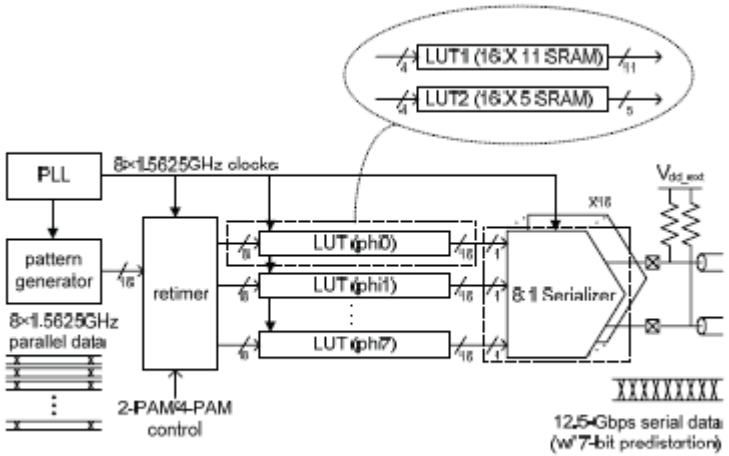
Claim 7	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 7	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 7	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 7	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 7	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 7	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 7	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 7	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 7	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 7	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 7	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 7	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 7	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 7	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 7	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 7	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 7	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 7	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

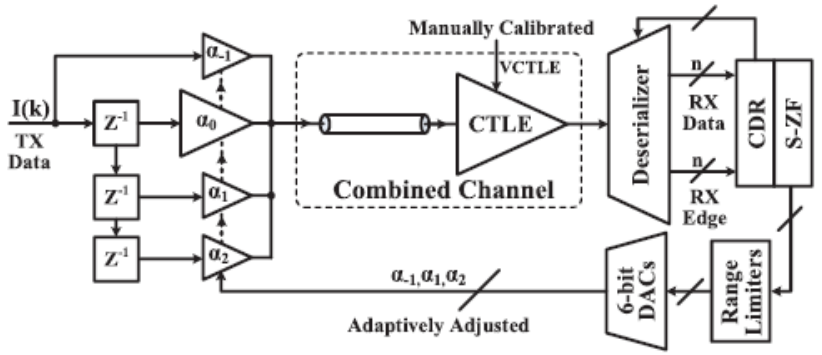


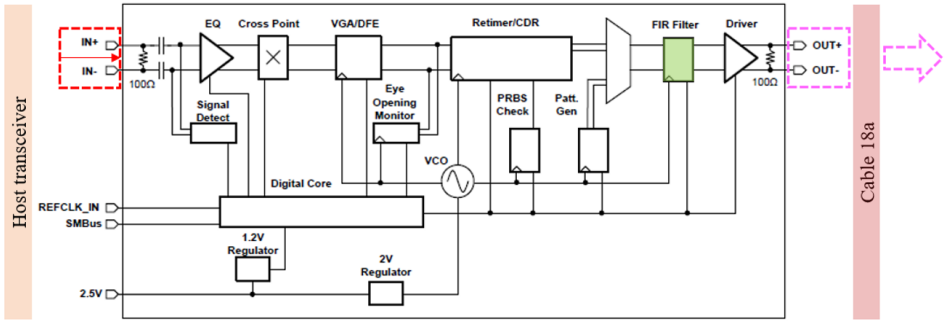
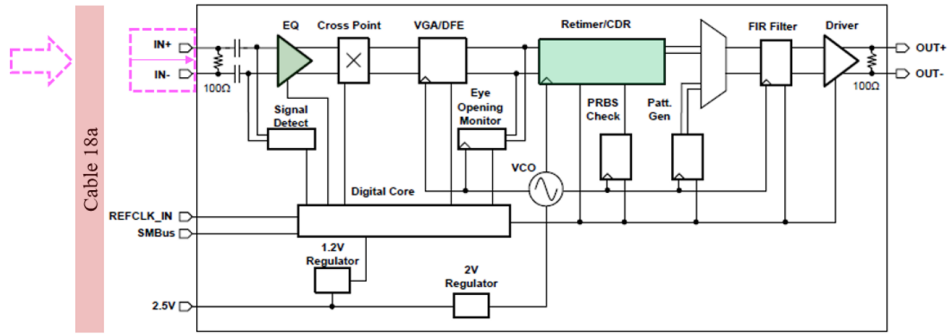
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

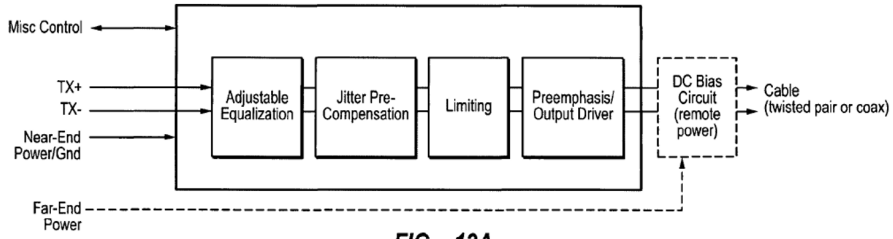
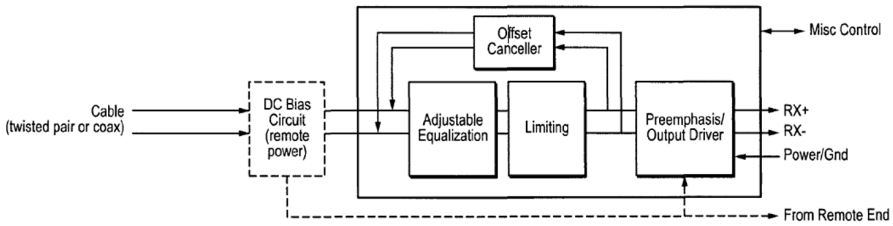
Claim 7	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

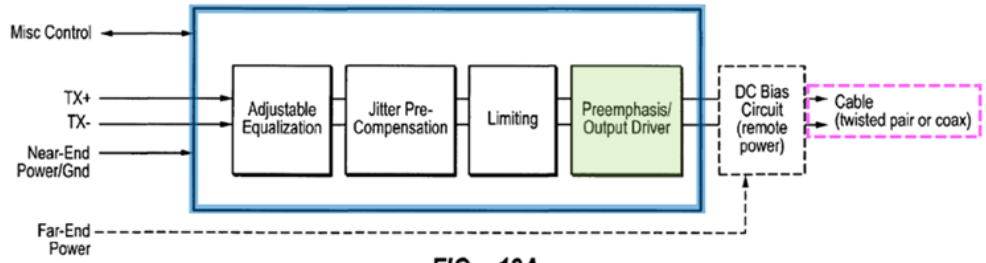
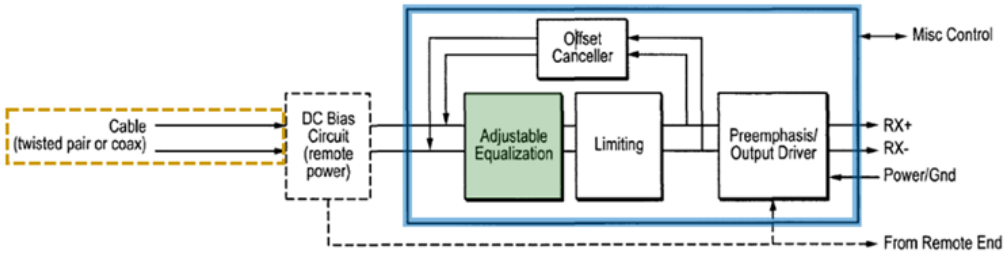
Claim 7	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The link activation module 204 is configured to determine a total insertion loss for the connection with the remote host based on the local host loss, the remote host loss, and cable loss. The link activation module 204 compares the total insertion loss to a FEC limit and to a specification limit. The link activation module 204 may bring up the communication link with the link partner without FEC enabled if the total insertion loss is below the specification limit and below the FEC limit. Additionally, the link activation module 204 may bring up the communication link with the link partner with FEC enabled if the total insertion loss is below the specification limit but not below the FEC limit. Further, the link activation module 204 may not bring up the communication link with the link partner if the total insertion loss is not below the specification limit (e.g., the link activation module 204 may keep the communication link down or bring the communication link down)." Lusted, paragraph 24.

Claim 7	Disclosure
	"The PCS 110 is configured to encode Ethernet frame data received from the MAC 112 into encoded data blocks that may be transmitted by the PMD/PMA 106, and to decode data received from the PMD/PMA 106 into decoded Ethernet frame data that may be processed by the MAC 112. The PCS 110 may encode and distribute the data blocks over one or more logical PCS lanes. The PCS 110 may encode data for transmission over the communication lanes 102 for example, to improve communication efficiency. For example, encoding the data may add timing or synchronization symbols, align the data, add state transitions to the encoded data to improve clock recovery, adjust the DC balance of the data signal, or otherwise prepare the encoded data for serial transmission. The PCS 110 may be capable of encoding or decoding the data using a 64b/66b line code in which 64-bit blocks of data are encoded into 66-bit blocks of encoded data, and vice versa." Lusted, paragraph 20. "The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage." Ikeda, 7:44-55. "FIG. 9 is a block diagram of still another example of a configuration of the second embodiment of the active connector according to the present invention. An active connector 107 illustrated in FIG. 9 differs from the active connector 106 illustrated in FIG. 8 in that the connector base 20 of the active connector 107 further includes a clock recovery circuit (CDR circuit) that recovers the timing of the input signal and reclocks the signal with an optimal timing at each time slot. More specifically, as illustrated in FIG. 9, after an input signal P32 supplied from the coaxial cable transmission line to the external port 30 is supplied to the matching circuit 210, the signal from the matching circuit 210 is supplied to the equalizing circuit 216 and then to a clock recovery circuit 218. Next, the output from the clock recovery circuit 218 is supplied to

Claim 7	Disclosure
	the buffer circuit 214, and then the output signal P12 is supplied from the buffer circuit 214 through the matching circuit 212 to the internal port 10. The clock recovery circuit 218 is driven by direct-current voltage Vcc supplied from an electrical power source (not shown) to a power supply terminal 12." Ikeda, 10:20-38. <u>*DS125DF1610 Retimer Publication*</u> The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610's FIR filter) and the CDR performed on the electrical input signal (by the DS125DF1610's EQ). DS125DF1610's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See id.* at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit signal."

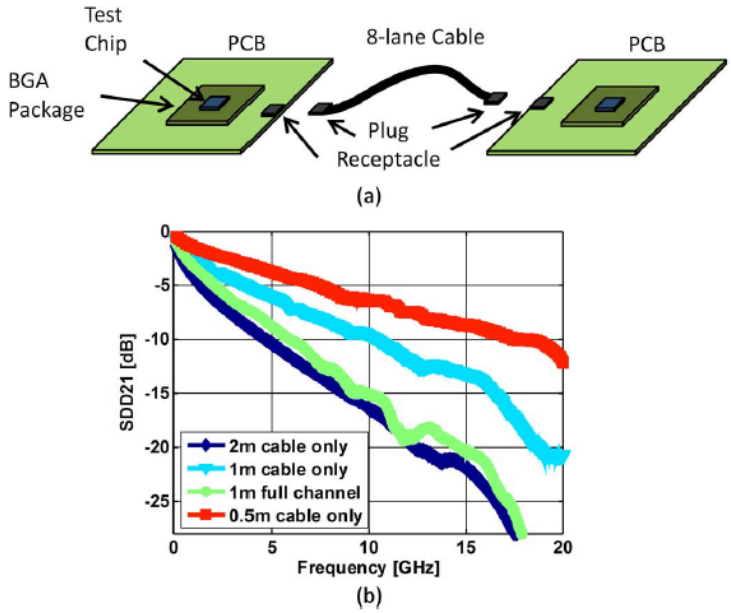
Claim 7	Disclosure
	 Figure 2. DS125DF1610 Simplified Data Path Diagram  Figure 2. DS125DF1610 Simplified Data Path Diagram *U.S. Patent No. 7,762,727 to Aronson* Aronson discloses an active cable for high-speed transmissions between network nodes. See, e.g., Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.

Claim 7	Disclosure
	 *FIG. 12A*  *FIG. 12B* Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23. Using "cable dependent" parameters for equalization would have been the conventional and obvious way to address losses over the cable. *See, e.g.*, Aronson at 14:33-43 (pre-emphasis/output driver performs pre-equalization to overcome "loss on the cable" using cable-dependent parameters that "match the particular length [and/or] the characteristics of the copper cabling"), Fig. 12A (below).

Claim 7	Disclosure
	 FIG. 12A Using "cable dependent" parameters for equalization would have been the conventional and obvious way to address losses over the cable. Aronson at 15:1-8 (equalization "compensate[s] for the cable" losses using cable dependent parameters based on "cable length and characteristics"), Fig. 12B (below).  FIG. 12B
7[b] re-modulating the second inbound data stream,	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

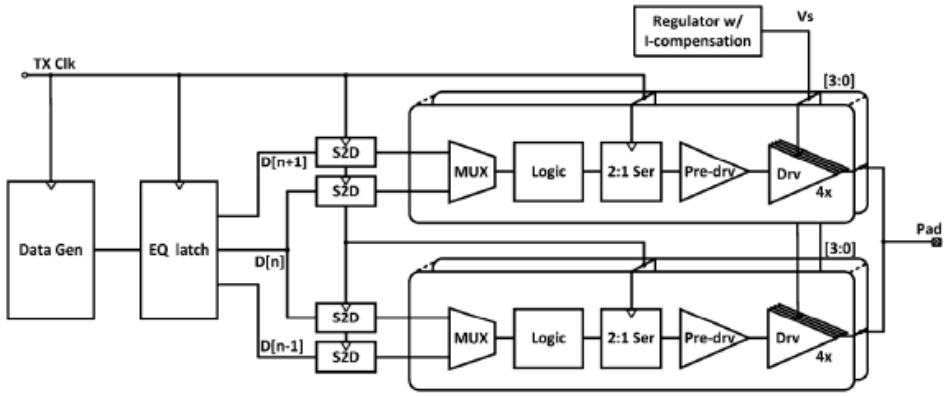
Claim 7	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

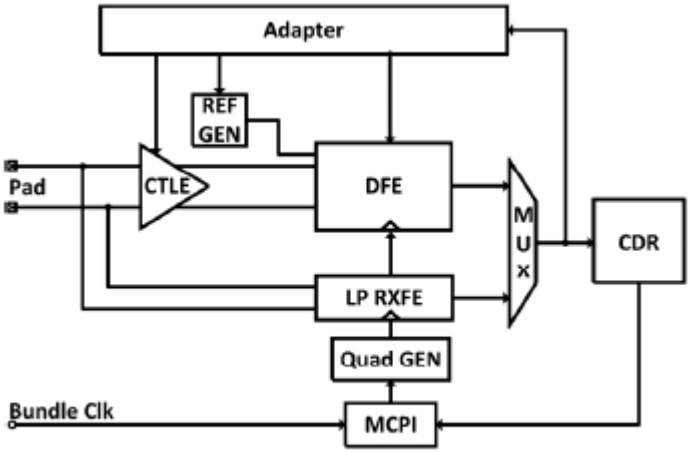
Claim 7	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 7	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 7	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

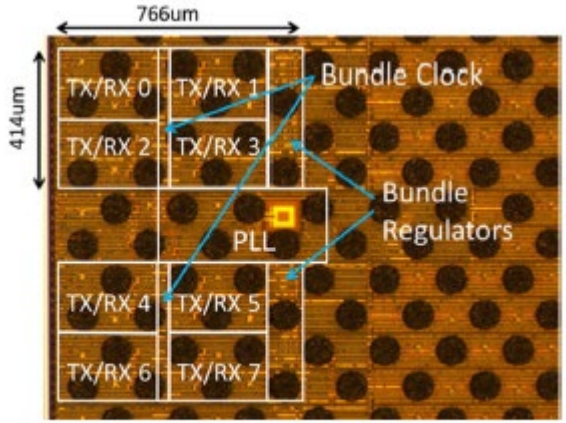
Claim 7	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 7	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 7	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

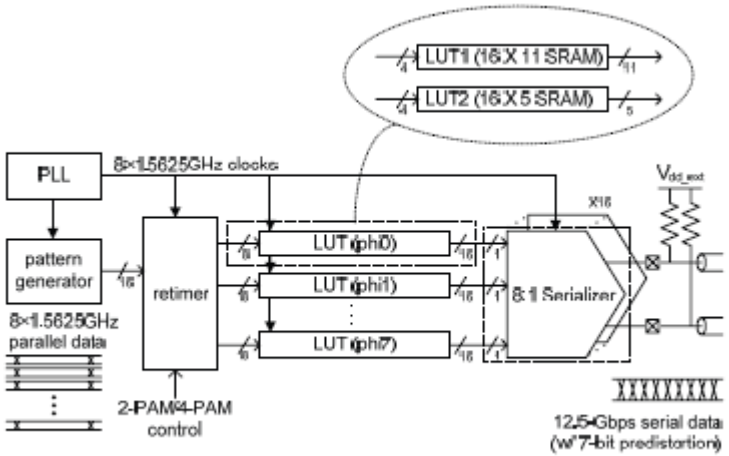
Claim 7	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 7	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 7	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 7	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 7	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 7	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 7	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 7	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 7	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 7	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 7	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 7	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 7	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 7	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 7	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 7	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 7	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 7	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

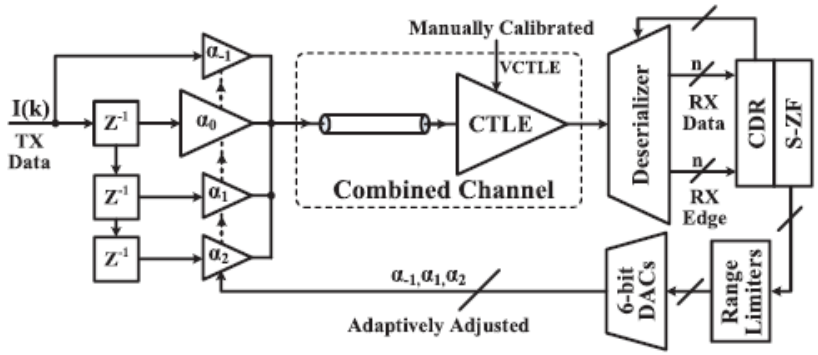
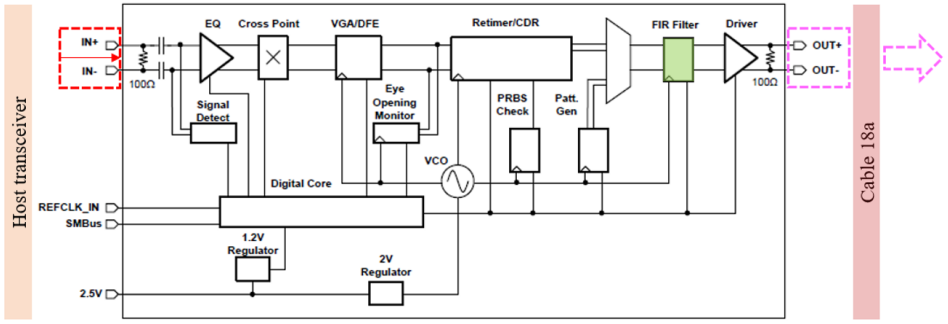
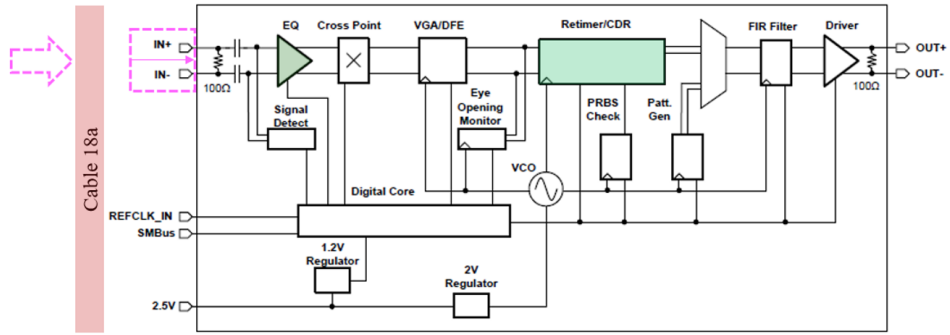


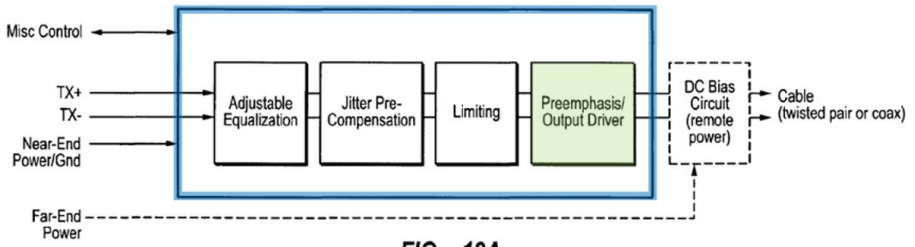
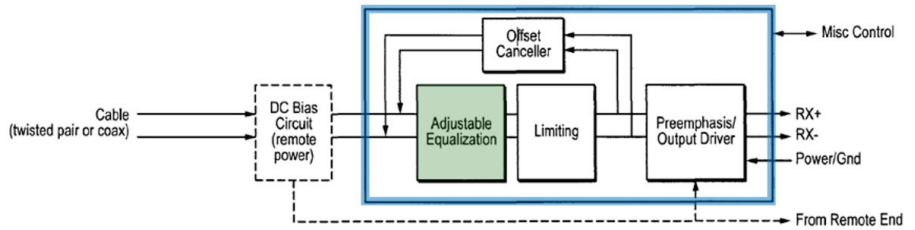
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 7	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 7	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The PCS 110 is configured to encode Ethernet frame data received from the MAC 112 into encoded data blocks that may be transmitted by the PMD/PMA 106, and to decode data received from the PMD/PMA 106 into decoded Ethernet frame data that may be processed by the MAC 112. The PCS 110 may encode and distribute the data blocks over one or more logical PCS lanes. The PCS 110 may encode data for transmission over the communication lanes 102 for example, to improve communication efficiency. For example, encoding the data may add timing or synchronization symbols, align the data, add state transitions to the encoded data to improve clock recovery, adjust the DC balance of the data signal, or otherwise prepare the encoded data for serial transmission. The PCS 110 may be capable of encoding or decoding the data using a 64b/66b line code in which 64-bit blocks of data are encoded into 66-bit blocks of encoded data, and vice versa." Lusted, paragraph 20.

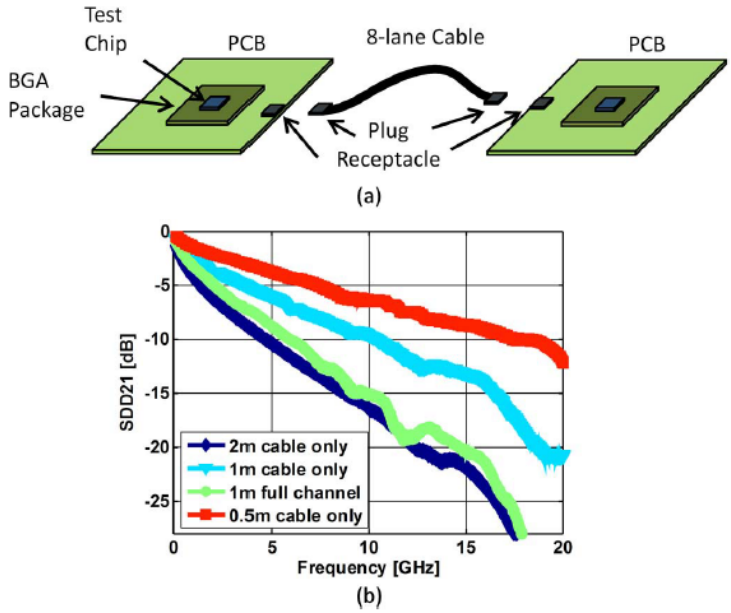
Claim 7	Disclosure
	"FIG. 9 is a block diagram of still another example of a configuration of the second embodiment of the active connector according to the present invention. An active connector 107 illustrated in FIG. 9 differs from the active connector 106 illustrated in FIG. 8 in that the connector base 20 of the active connector 107 further includes a clock recovery circuit (CDR circuit) that recovers the timing of the input signal and reclocks the signal with an optimal timing at each time slot. More specifically, as illustrated in FIG. 9, after an input signal P32 supplied from the coaxial cable transmission line to the external port 30 is supplied to the matching circuit 210, the signal from the matching circuit 210 is supplied to the equalizing circuit 216 and then to a clock recovery circuit 218. Next, the output from the clock recovery circuit 218 is supplied to the buffer circuit 214, and then the output signal P12 is supplied from the buffer circuit 214 through the matching circuit 212 to the internal port 10. The clock recovery circuit 218 is driven by direct-current voltage Vcc supplied from an electrical power source (not shown) to a power supply terminal 12." Ikeda, 10:20-38. *DS125DF1610 Retimer Publication* The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610's FIR filter) and the CDR performed on the electrical input signal (by the DS125DF1610's EQ). DS125DF1610's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See id.* at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit signal."

Claim 7	Disclosure
	 Figure 2. DS125DF1610 Simplified Data Path Diagram  Figure 2. DS125DF1610 Simplified Data Path Diagram <u>*U.S. Patent No. 7,762,727 to Aronson*</u> Aronson discloses cable-side equalization and pre-equalization that use cable-dependent parameters to address cable-side losses. *See, e.g.*, Aronson, 14:33-43, 15:1-8. Aronson's transmitter IC's line-side pre-emphasis/output driver overcomes "loss on the cable" using cable-dependent parameters that "match the particular length [and/or] the characteristics of the copper cabling." *See id*. at 14:33-43, Fig. 12A (below). Similarly, Aronson's receiver IC equalizes received line-side signals to "compensat[e] for the cable" losses using cable-dependent parameters based on "cable length and characteristics." *See id*. at 15:1-8, Fig. 12B

Claim 7	Disclosure
	(below).  *FIG. 12A*  *FIG. 12B*
7[c] said performing clock and data recovery on the first electrical transit signal, and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

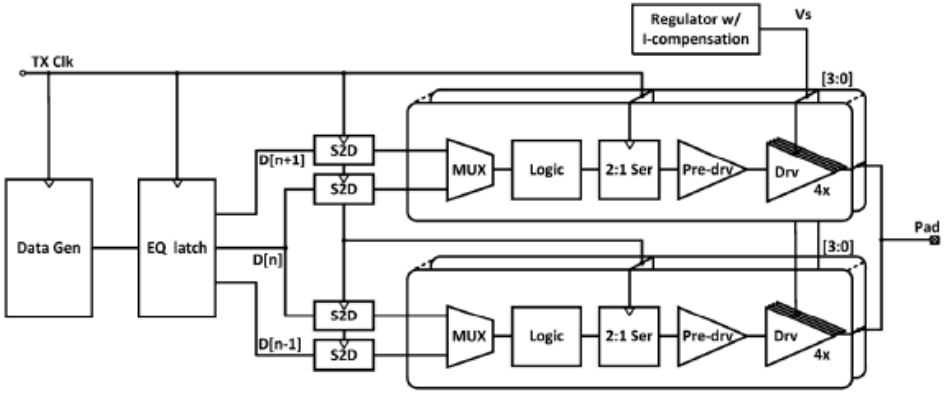
Claim 7	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

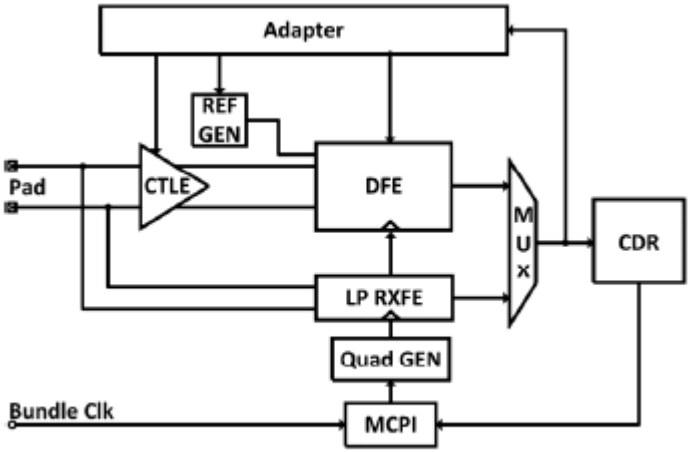
Claim 7	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 7	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 7	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

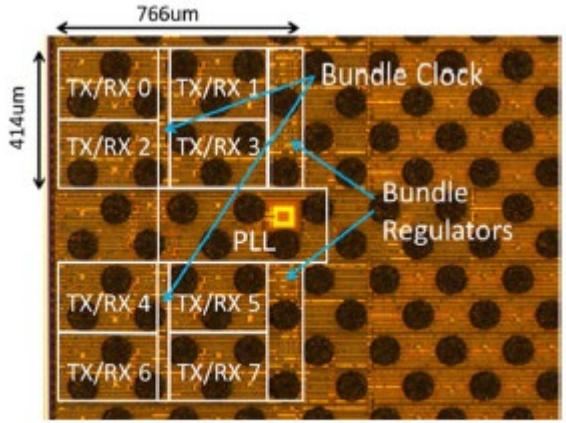
Claim 7	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 7	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 7	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

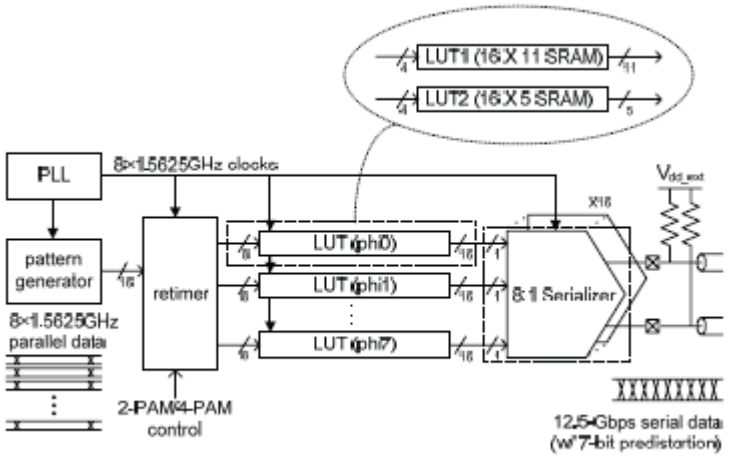
Claim 7	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 7	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 7	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 7	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 7	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 7	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 7	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 7	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 7	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 7	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 7	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 7	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 7	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 7	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 7	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 7	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 7	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 7	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

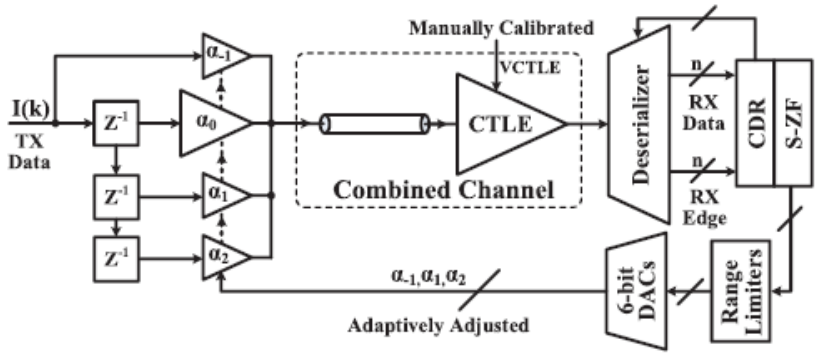
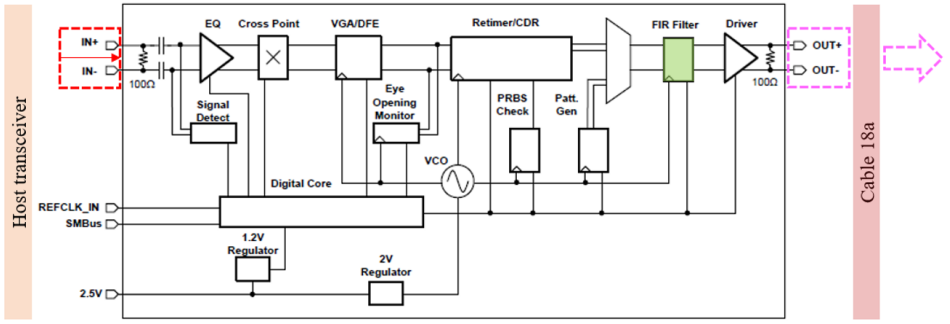
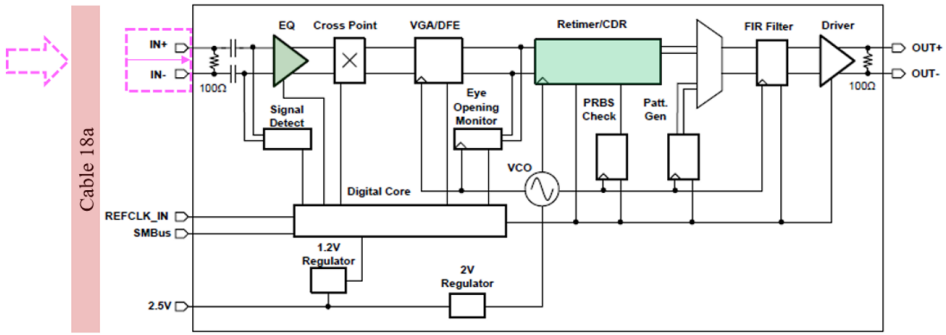


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 7	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

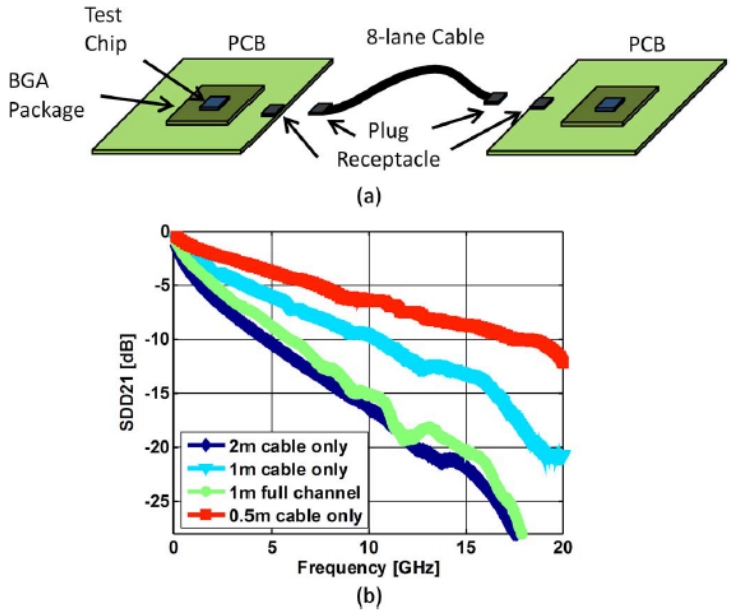
Claim 7	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The PCS 110 is configured to encode Ethernet frame data received from the MAC 112 into encoded data blocks that may be transmitted by the PMD/PMA 106, and to decode data received from the PMD/PMA 106 into decoded Ethernet frame data that may be processed by the MAC 112. The PCS 110 may encode and distribute the data blocks over one or more logical PCS lanes. The PCS 110 may encode data for transmission over the communication lanes 102 for example, to improve communication efficiency. For example, encoding the data may add timing or synchronization symbols, align the data, add state transitions to the encoded data to improve clock recovery, adjust the DC balance of the data signal, or otherwise prepare the encoded data for serial transmission. The PCS 110 may be capable of encoding or decoding the data using a 64b/66b line code in which 64-bit blocks of data are encoded into 66-bit blocks of encoded data, and vice versa." Lusted, paragraph 20.

Claim 7	Disclosure
	"FIG. 9 is a block diagram of still another example of a configuration of the second embodiment of the active connector according to the present invention. An active connector 107 illustrated in FIG. 9 differs from the active connector 106 illustrated in FIG. 8 in that the connector base 20 of the active connector 107 further includes a clock recovery circuit (CDR circuit) that recovers the timing of the input signal and reclocks the signal with an optimal timing at each time slot. More specifically, as illustrated in FIG. 9, after an input signal P32 supplied from the coaxial cable transmission line to the external port 30 is supplied to the matching circuit 210, the signal from the matching circuit 210 is supplied to the equalizing circuit 216 and then to a clock recovery circuit 218. Next, the output from the clock recovery circuit 218 is supplied to the buffer circuit 214, and then the output signal P12 is supplied from the buffer circuit 214 through the matching circuit 212 to the internal port 10. The clock recovery circuit 218 is driven by direct-current voltage Vcc supplied from an electrical power source (not shown) to a power supply terminal 12." Ikeda, 10:20-38. *DS125DF1610 Retimer Publication* The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610's FIR filter) and the CDR performed on the electrical input signal (by the DS125DF1610's EQ). DS125DF1610's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See id.* at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit signal."

Claim 7	Disclosure
	 Figure 2. DS125DF1610 Simplified Data Path Diagram  Figure 2. DS125DF1610 Simplified Data Path Diagram
7[d] said performing clock and data recovery on the second electrical input signal,	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

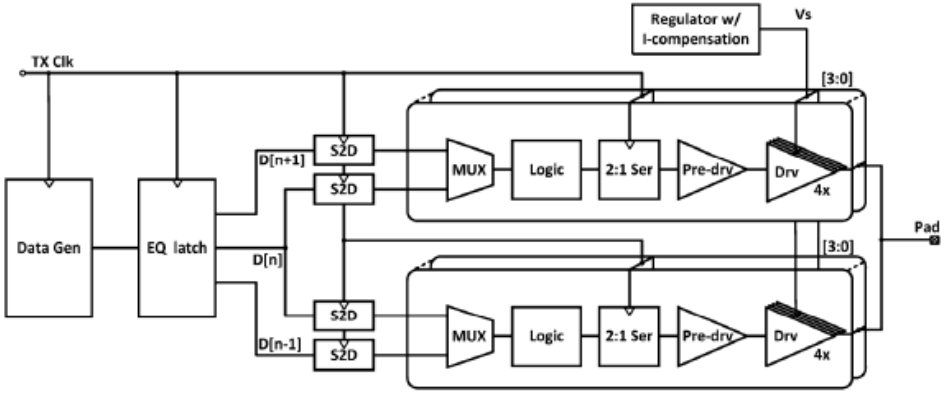
Claim 7	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

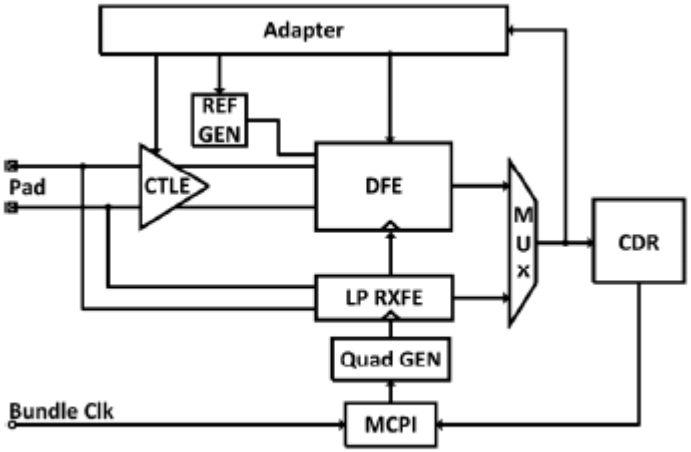
Claim 7	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 7	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 7	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

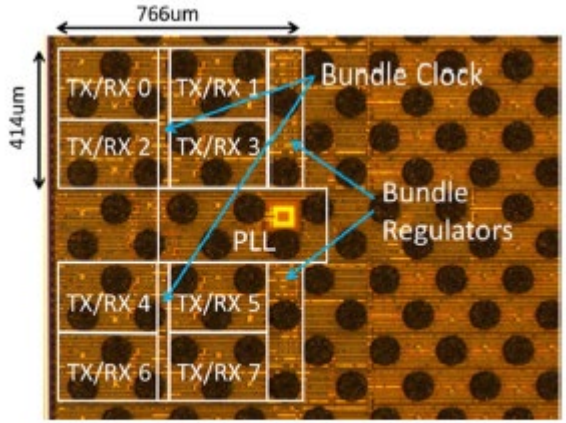
Claim 7	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 7	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 7	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

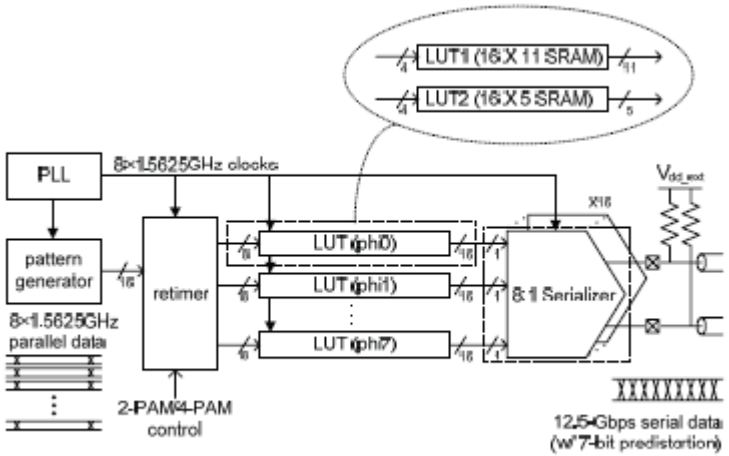
Claim 7	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 7	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 7	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 7	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 7	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 7	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 7	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 7	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 7	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 7	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 7	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 7	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 7	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 7	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 7	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 7	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 7	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 7	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

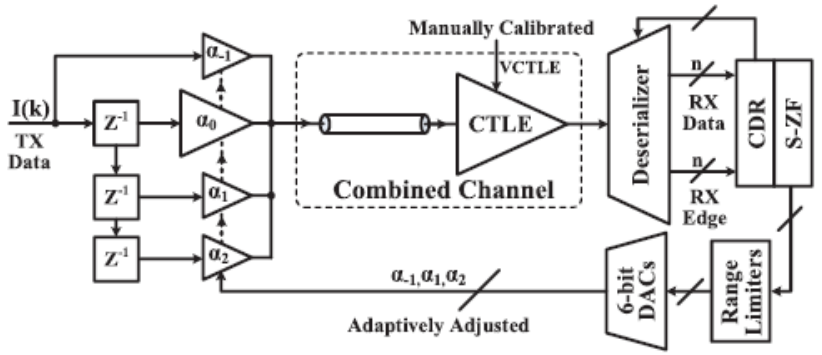
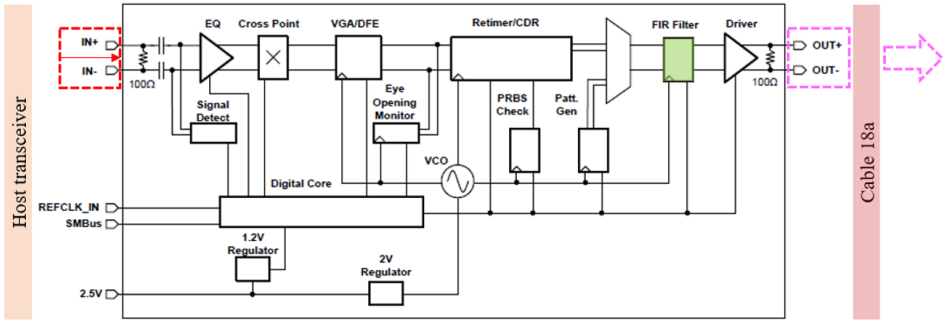
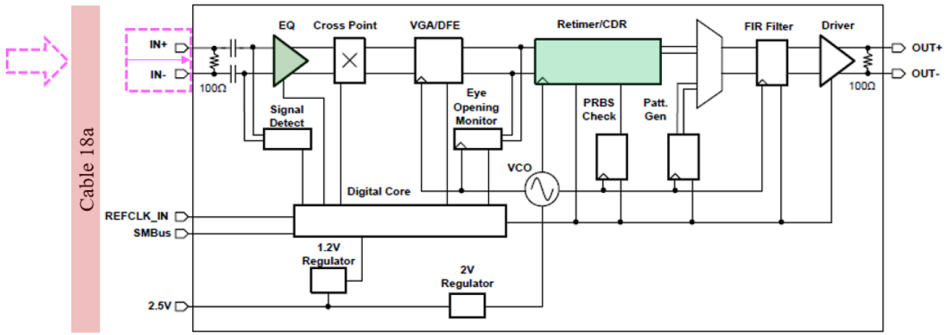


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 7	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 7	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The PCS 110 is configured to encode Ethernet frame data received from the MAC 112 into encoded data blocks that may be transmitted by the PMD/PMA 106, and to decode data received from the PMD/PMA 106 into decoded Ethernet frame data that may be processed by the MAC 112. The PCS 110 may encode and distribute the data blocks over one or more logical PCS lanes. The PCS 110 may encode data for transmission over the communication lanes 102 for example, to improve communication efficiency. For example, encoding the data may add timing or synchronization symbols, align the data, add state transitions to the encoded data to improve clock recovery, adjust the DC balance of the data signal, or otherwise prepare the encoded data for serial transmission. The PCS 110 may be capable of encoding or decoding the data using a 64b/66b line code in which 64-bit blocks of data are encoded into 66-bit blocks of encoded data, and vice versa." Lusted, paragraph 20.

Claim 7	Disclosure
	"FIG. 9 is a block diagram of still another example of a configuration of the second embodiment of the active connector according to the present invention. An active connector 107 illustrated in FIG. 9 differs from the active connector 106 illustrated in FIG. 8 in that the connector base 20 of the active connector 107 further includes a clock recovery circuit (CDR circuit) that recovers the timing of the input signal and reclocks the signal with an optimal timing at each time slot. More specifically, as illustrated in FIG. 9, after an input signal P32 supplied from the coaxial cable transmission line to the external port 30 is supplied to the matching circuit 210, the signal from the matching circuit 210 is supplied to the equalizing circuit 216 and then to a clock recovery circuit 218. Next, the output from the clock recovery circuit 218 is supplied to the buffer circuit 214, and then the output signal P12 is supplied from the buffer circuit 214 through the matching circuit 212 to the internal port 10. The clock recovery circuit 218 is driven by direct-current voltage Vcc supplied from an electrical power source (not shown) to a power supply terminal 12." Ikeda, 10:20-38. *DS125DF1610 Retimer Publication* The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610's FIR filter) and the CDR performed on the electrical input signal (by the DS125DF1610's EQ). DS125DF1610's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See id.* at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit signal."

Claim 7	Disclosure
	 Figure 2. DS125DF1610 Simplified Data Path Diagram  Figure 2. DS125DF1610 Simplified Data Path Diagram
7[e] each employ fixed, cable-independent, equalization parameters.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

Claim 7	Disclosure
	Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp. CMIS, 22.

Claim 7	Disclosure
	1.5.4 Control Set Overview A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 7	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 7	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 7	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 7	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 7	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 7	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

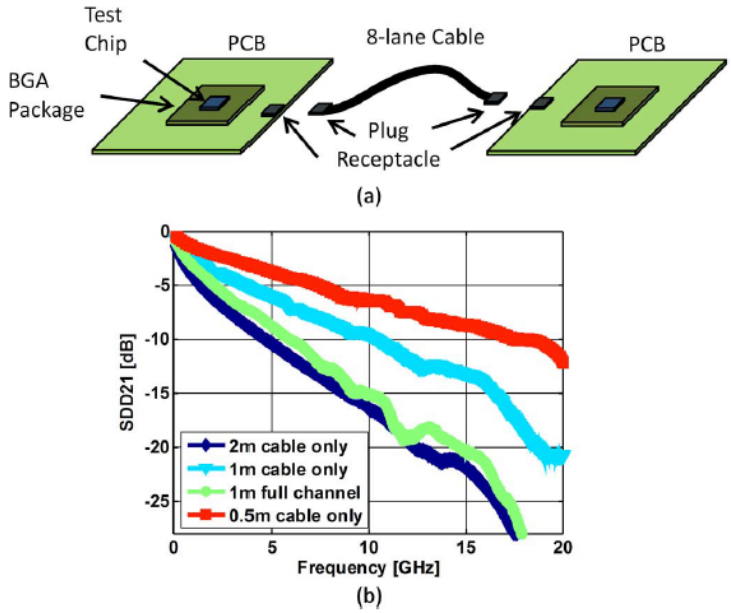
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

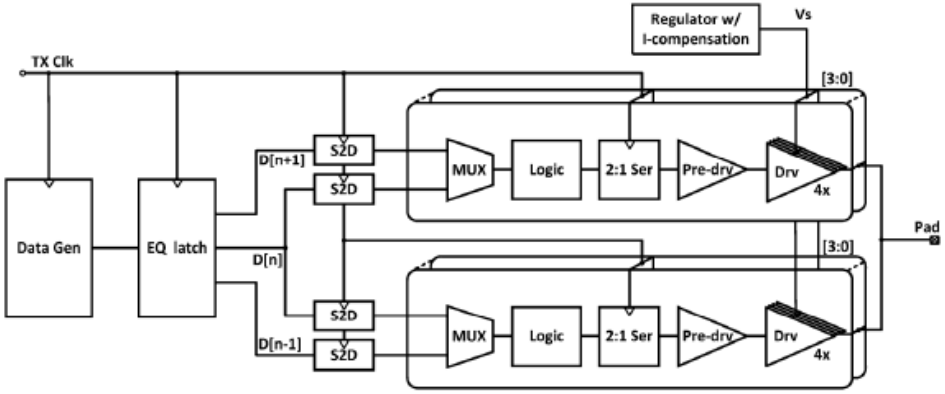
Claim 7	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

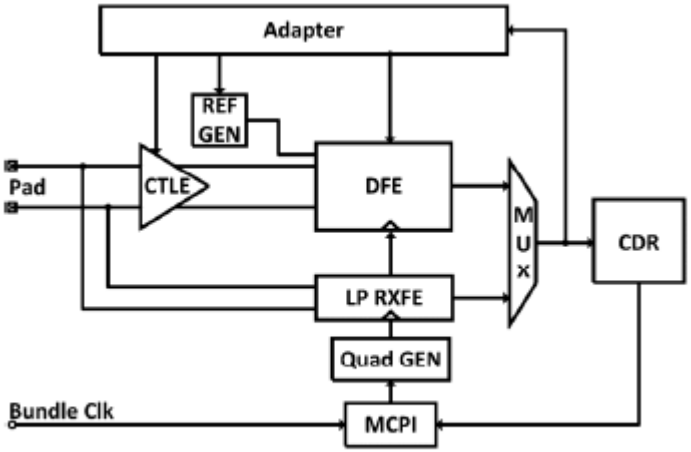
Claim 7	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 7	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 7	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

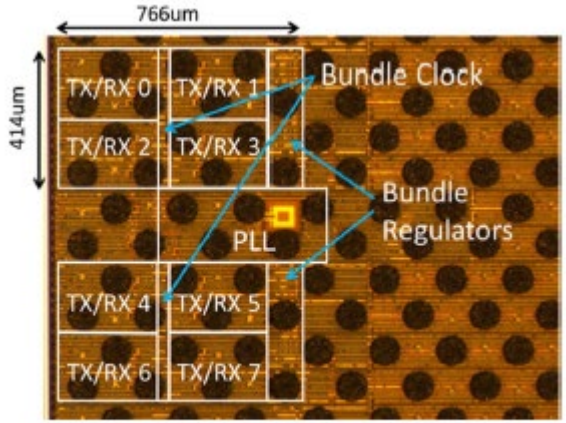
Claim 7	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 7	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 7	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

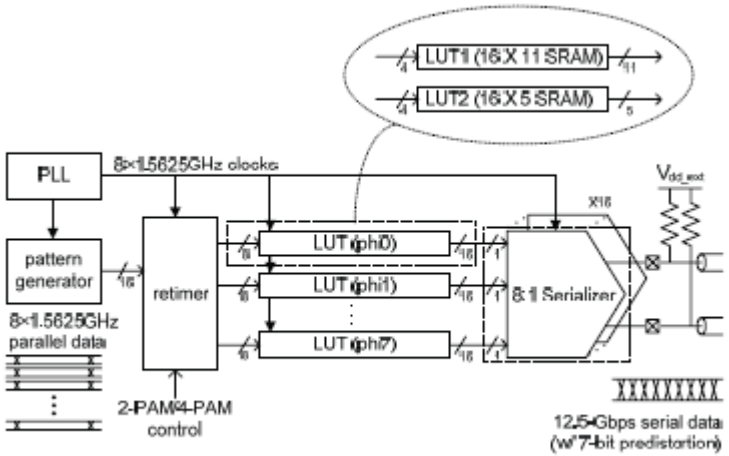
Claim 7	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 7	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 7	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 7	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 7	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 7	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 7	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 7	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 7	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 7	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 7	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 7	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 7	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 7	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 7	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 7	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 7	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 7	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

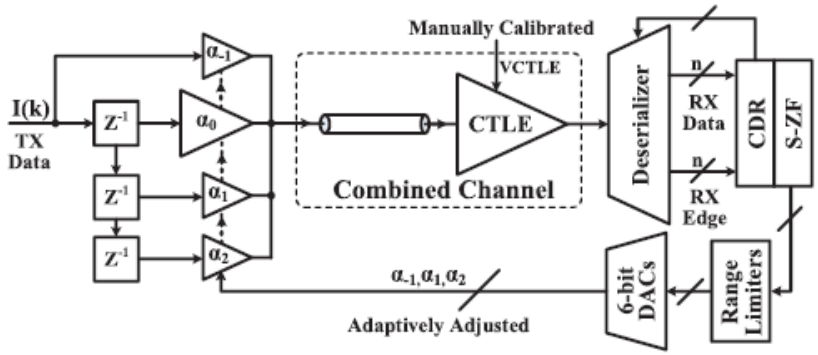
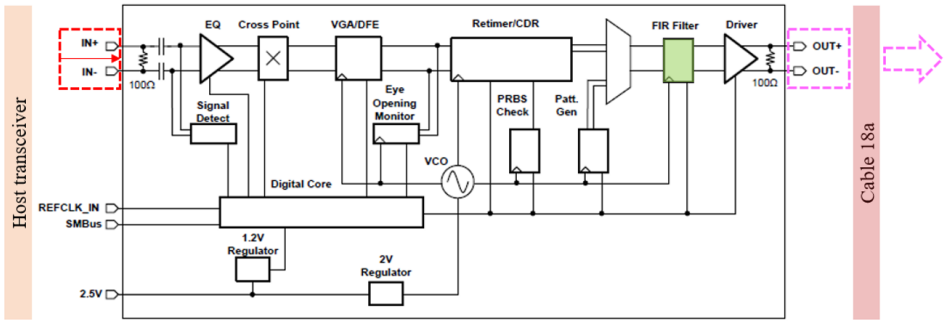
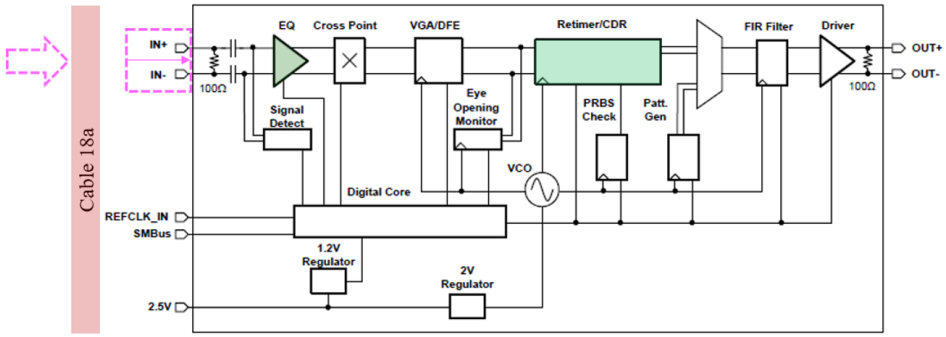


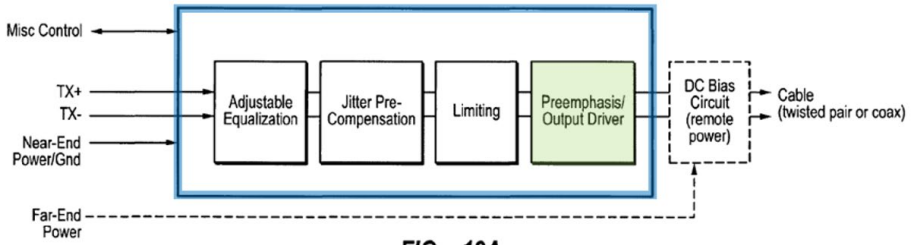
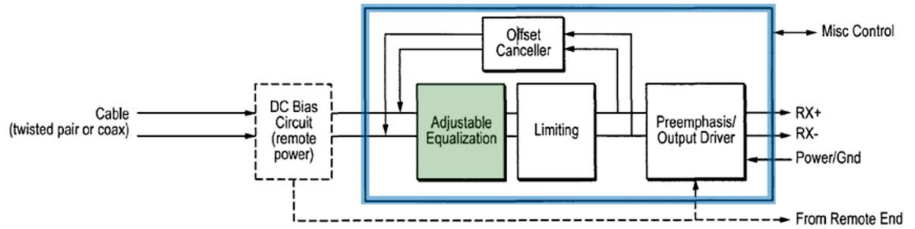
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

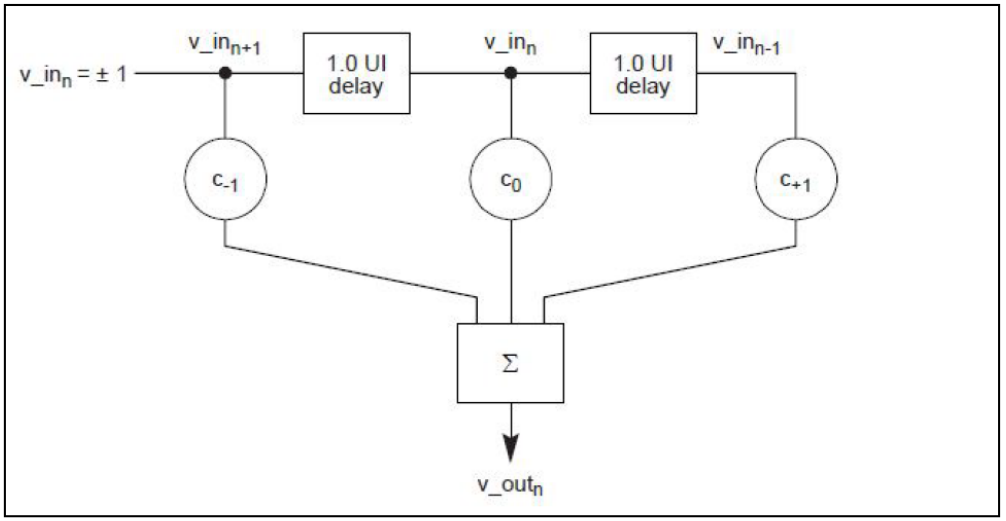
Claim 7	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 7	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The PCS 110 is configured to encode Ethernet frame data received from the MAC 112 into encoded data blocks that may be transmitted by the PMD/PMA 106, and to decode data received from the PMD/PMA 106 into decoded Ethernet frame data that may be processed by the MAC 112. The PCS 110 may encode and distribute the data blocks over one or more logical PCS lanes. The PCS 110 may encode data for transmission over the communication lanes 102 for example, to improve communication efficiency. For example, encoding the data may add timing or synchronization symbols, align the data, add state transitions to the encoded data to improve clock recovery, adjust the DC balance of the data signal, or otherwise prepare the encoded data for serial transmission. The PCS 110 may be capable of encoding or decoding the data using a 64b/66b line code in which 64-bit blocks of data are encoded into 66-bit blocks of encoded data, and vice versa." Lusted, paragraph 20.

Claim 7	Disclosure
	"FIG. 9 is a block diagram of still another example of a configuration of the second embodiment of the active connector according to the present invention. An active connector 107 illustrated in FIG. 9 differs from the active connector 106 illustrated in FIG. 8 in that the connector base 20 of the active connector 107 further includes a clock recovery circuit (CDR circuit) that recovers the timing of the input signal and reclocks the signal with an optimal timing at each time slot. More specifically, as illustrated in FIG. 9, after an input signal P32 supplied from the coaxial cable transmission line to the external port 30 is supplied to the matching circuit 210, the signal from the matching circuit 210 is supplied to the equalizing circuit 216 and then to a clock recovery circuit 218. Next, the output from the clock recovery circuit 218 is supplied to the buffer circuit 214, and then the output signal P12 is supplied from the buffer circuit 214 through the matching circuit 212 to the internal port 10. The clock recovery circuit 218 is driven by direct-current voltage Vcc supplied from an electrical power source (not shown) to a power supply terminal 12." Ikeda, 10:20-38. *DS125DF1610 Retimer Publication* The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610's FIR filter) and the CDR performed on the electrical input signal (by the DS125DF1610's EQ). DS125DF1610's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See id.* at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit

Claim 7	Disclosure
	signal."  Figure 2. DS125DF1610 Simplified Data Path Diagram  Figure 2. DS125DF1610 Simplified Data Path Diagram *U.S. Patent No. 7,762,727 to Aronson* Aronson discloses cable-side equalization and pre-equalization that use cable-dependent parameters to address cable-side losses. *See, e.g.*, Aronson, 14:33-43, 15:1-8. Aronson's transmitter IC's line-side pre-emphasis/output driver overcomes "loss on the cable" using cable-dependent parameters that "match the particular length [and/or] the characteristics of the copper cabling." *See id.* at 14:33-43, Fig. 12A (below).

Claim 7	Disclosure
	Similarly, Aronson's receiver IC equalizes received line-side signals to "compensat[e] for the cable" losses using cable-dependent parameters based on "cable length and characteristics." *See id*. at 15:1-8, Fig. 12B (below).  *FIG. 12A*  *FIG. 12B*

Claim 7	Disclosure
	 **Figure 22 The PCIe 3.0 Tx Equalization FIR filter representation. (Note: The 10G-KR Filter is similar in definition).** This PCIe 3.0 TxEQ adaptation [10] protocol has 4 phases, defined as follows:- Samaan, p. 25.

H. DEPENDENT CLAIM 8

Claim 8	Disclosure
8. The communication method of claim 7, wherein said cable-dependent equalization parameters are adaptively updated.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp.

Claim 8	Disclosure
	CMIS, 22. **1.5.4 Control Set Overview** A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 8	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 8	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 8	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 8	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 8	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 8	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

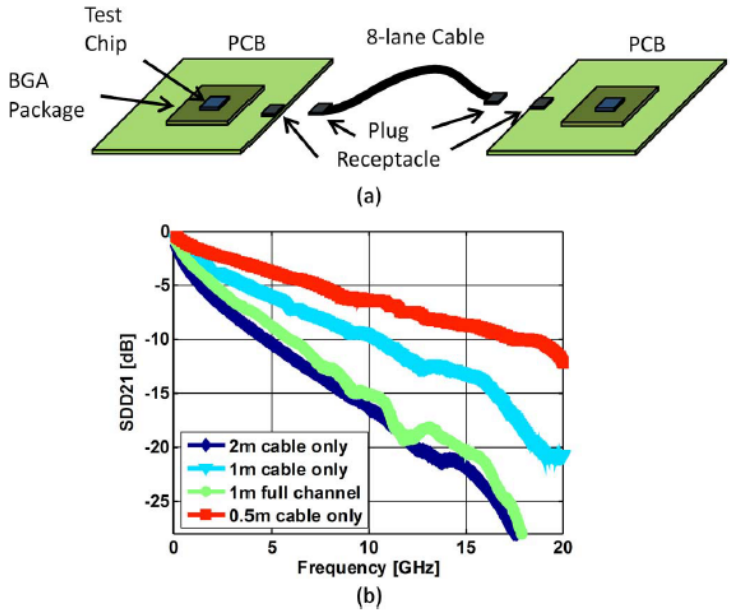
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

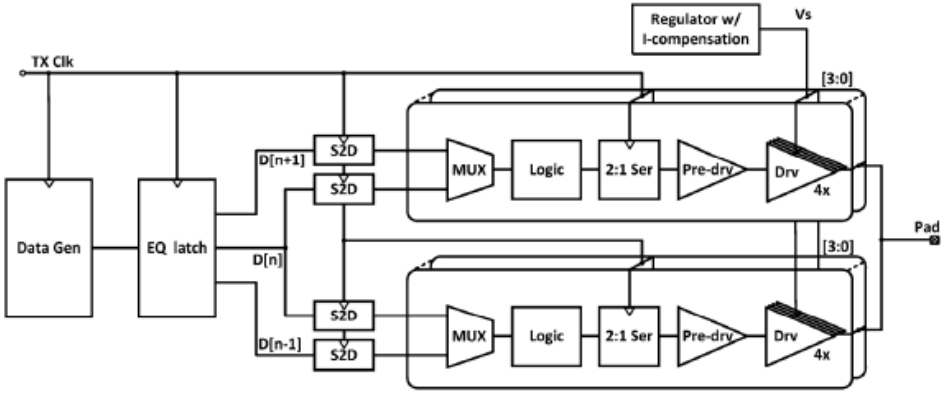
Claim 8	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

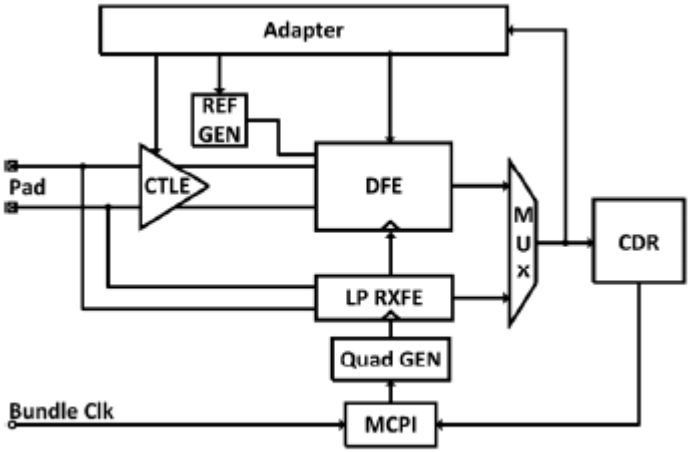
Claim 8	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 8	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 8	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

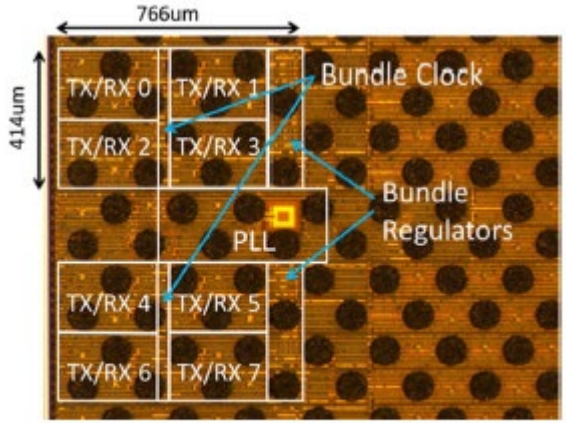
Claim 8	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 8	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 8	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

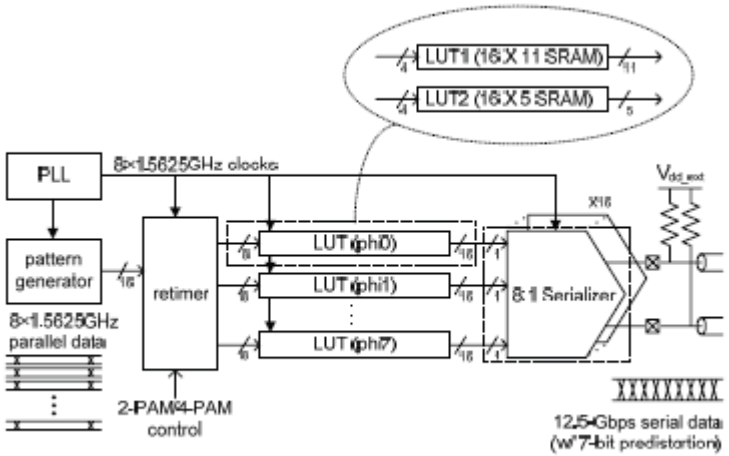
Claim 8	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 8	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 8	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 8	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 8	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 8	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 8	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 8	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 8	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 8	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 8	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 8	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 8	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 8	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 8	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 8	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 8	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 8	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

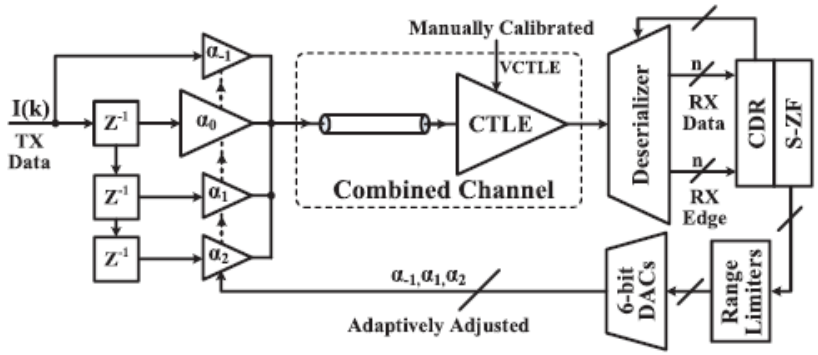
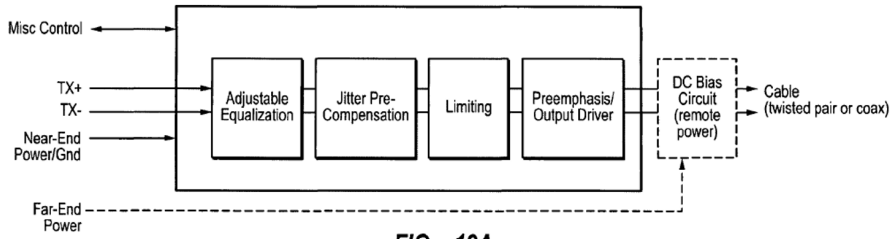
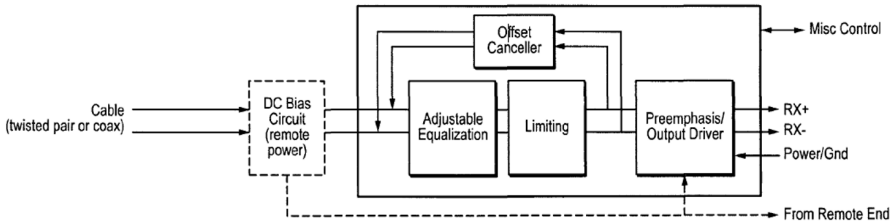
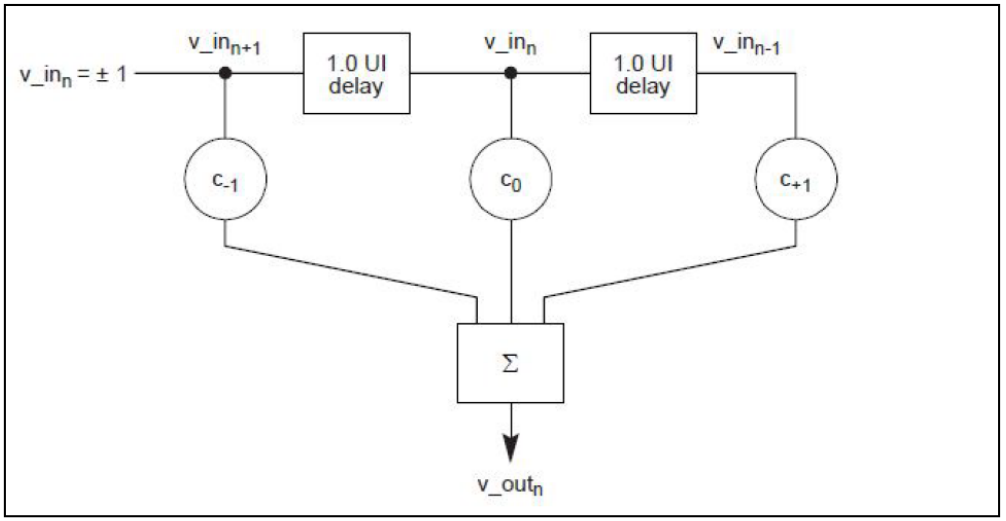


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 8	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 8	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage." Ikeda, 7:44-55. *U.S. Patent No. 7,762,727 to Aronson*

Claim 8	Disclosure
	Aronson discloses an active cable for high-speed transmissions between network nodes. See, e.g., Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.  *FIG. 12A*  *FIG. 12B* Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23.

Claim 8	Disclosure
	 **Figure 22 The PCIe 3.0 Tx Equalization FIR filter representation. (Note: The 10G-KR Filter is similar in definition).** This PCIe 3.0 TxEQ adaptation [10] protocol has 4 phases, defined as follows:- Samaan, p. 25.

I. DEPENDENT CLAIM 9

Claim 9	Disclosure
9[a] The communication method of claim 7, wherein said cable-dependent equalization parameters are fixed during normal usage, and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp.

Claim 9	Disclosure
	CMIS, 22. **1.5.4 Control Set Overview** A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 9	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 9	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 9	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 9	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 9	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 9	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

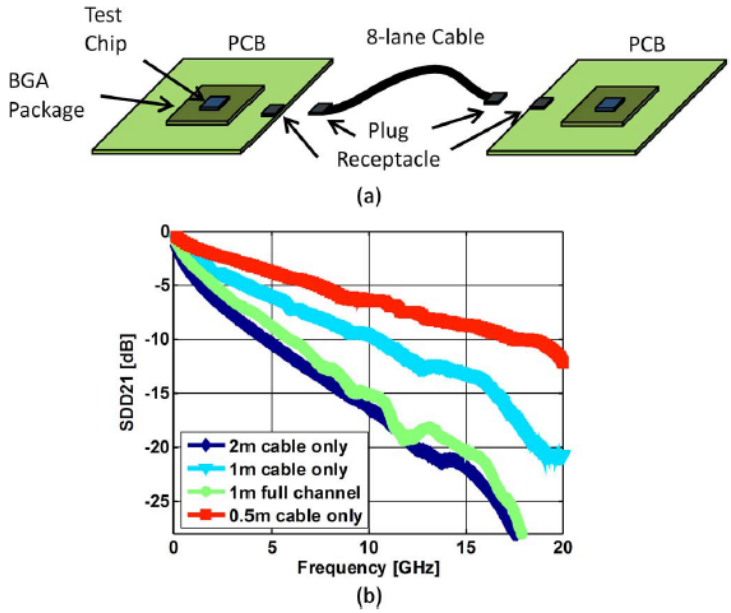
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

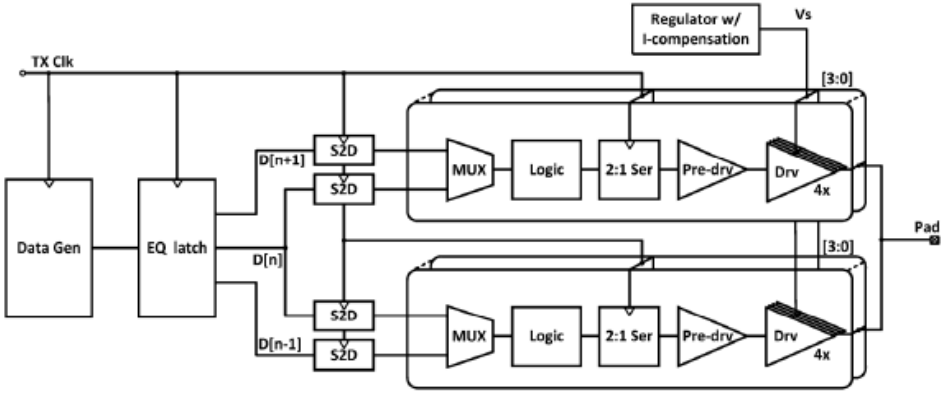
Claim 9	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

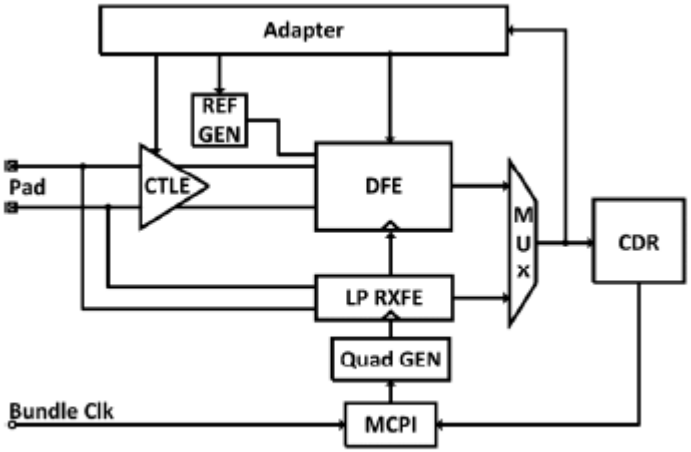
Claim 9	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 9	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 9	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

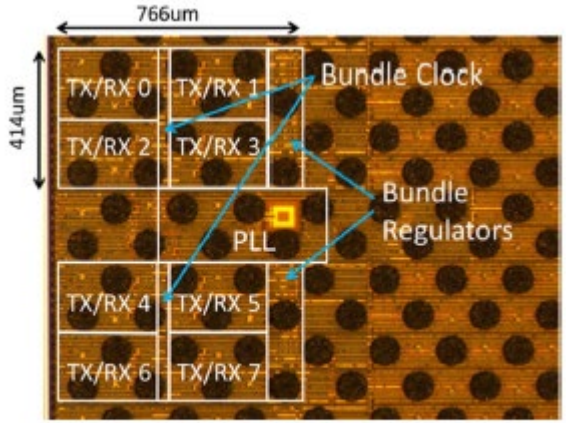
Claim 9	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 9	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 9	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

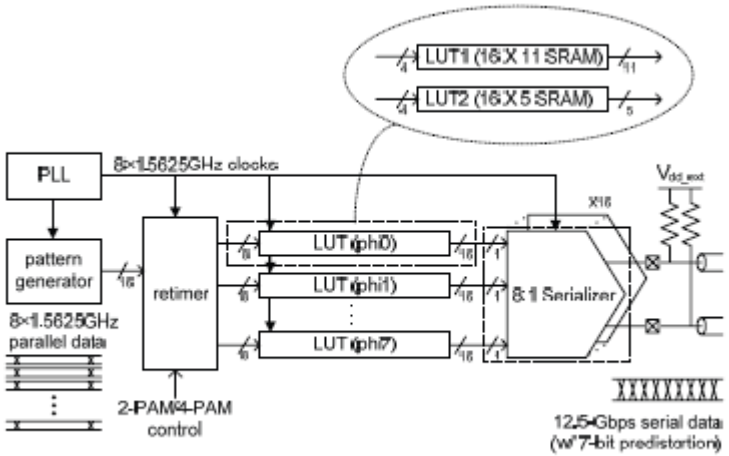
Claim 9	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 9	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 9	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 9	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 9	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 9	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 9	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 9	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 9	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 9	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 9	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 9	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 9	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 9	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 9	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 9	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 9	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 9	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

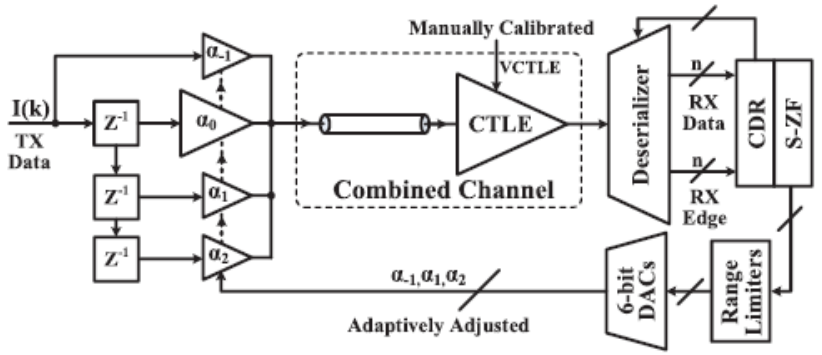
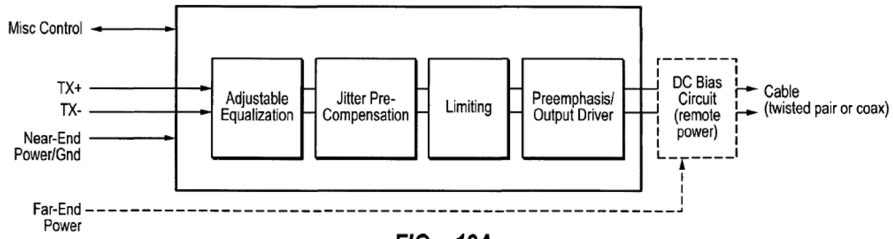
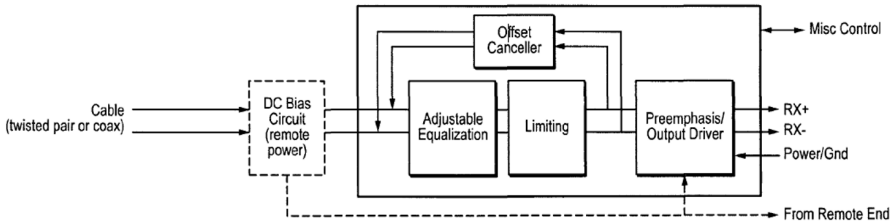


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 9	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 9	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage." Ikeda, 7:44-55. *U.S. Patent No. 7,762,727 to Aronson*

Claim 9	Disclosure
	Aronson discloses an active cable for high-speed transmissions between network nodes. See, e.g., Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.  *FIG. 12A*  *FIG. 12B* Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23.

Claim 9	Disclosure
9[b] wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp.

Claim 9	Disclosure
	CMIS, 22. **1.5.4 Control Set Overview** A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 9	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 9	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 9	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 9	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 9	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 9	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

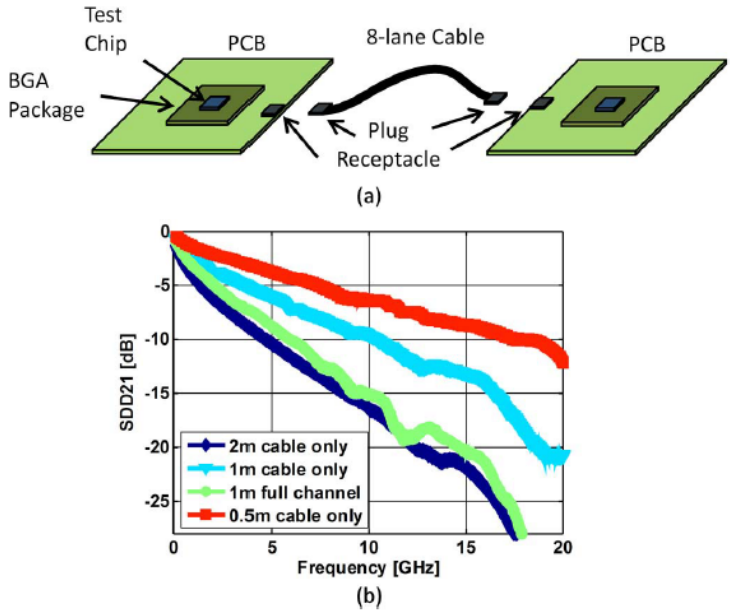
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

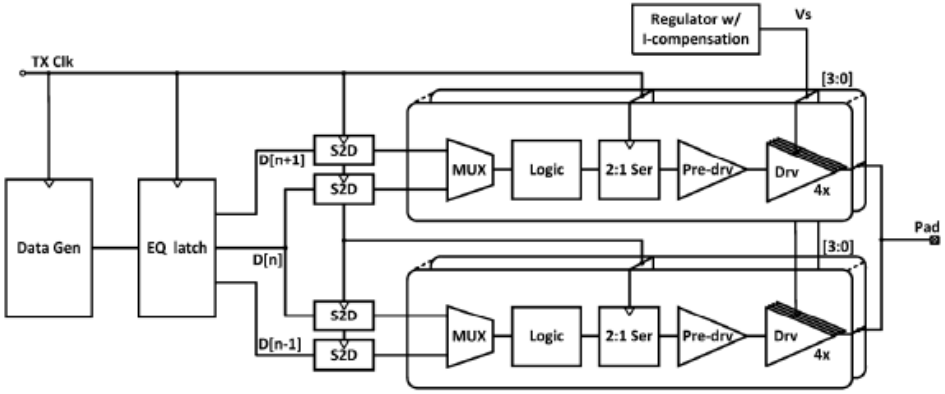
Claim 9	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

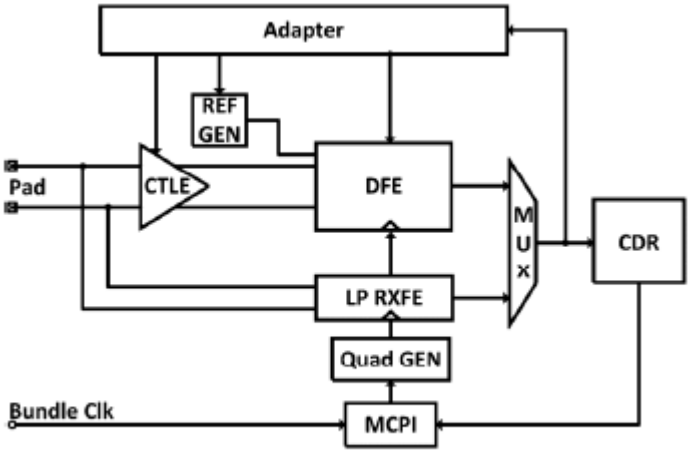
Claim 9	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 9	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 9	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

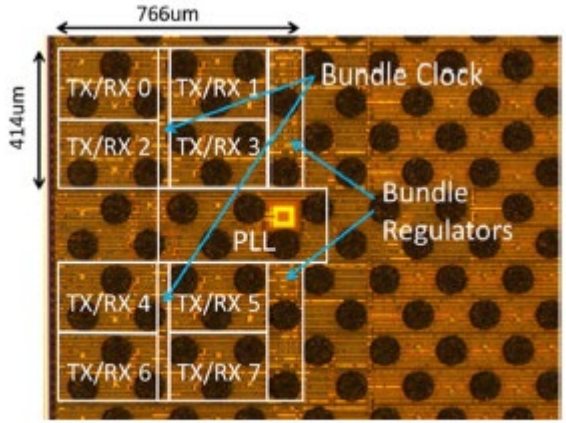
Claim 9	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 9	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 9	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

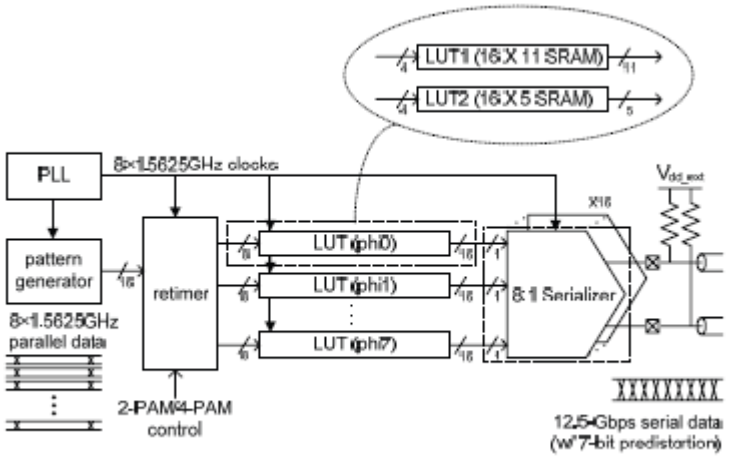
Claim 9	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 9	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 9	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 9	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 9	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 9	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 9	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 9	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 9	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 9	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 9	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 9	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 9	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 9	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 9	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 9	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 9	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 9	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

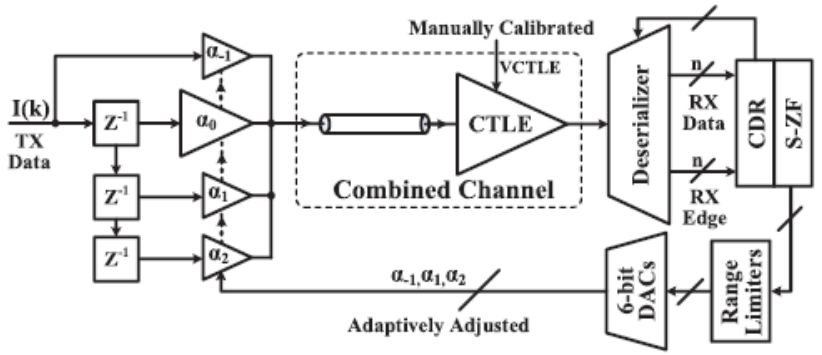
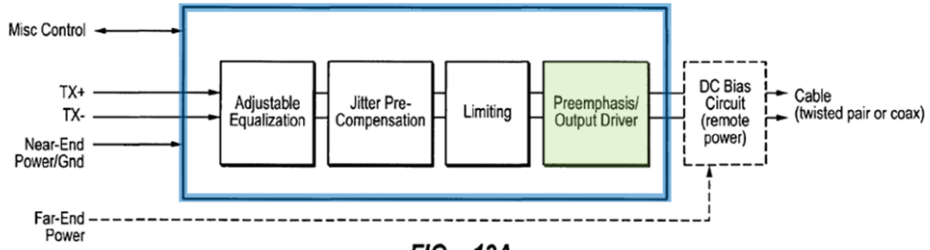
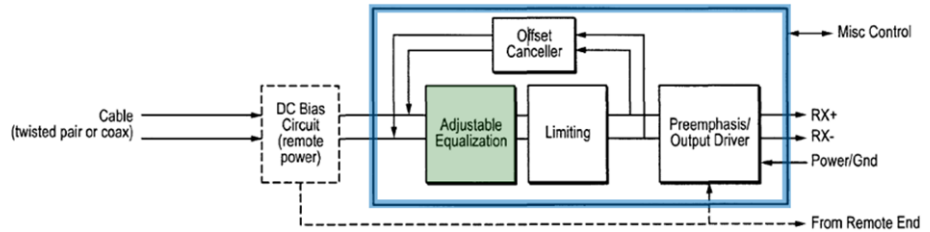


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 9	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 9	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage." Ikeda, 7:44-55.

Claim 9	Disclosure
	U.S. Patent No. 7,762,727 to Aronson One obvious way to implement the equalization coefficients used by a FIR filter and an equalizer is during manufacturing-testing. *See, e.g.*, Aronson at 14:35-39 (Fig. 12A's pre-equalization parameters for transit over the line-side are "adjusted at factory setup"), 15:1-23 (Fig. 12B's equalization may be "fixed" or "adjustable but factory set" "at the time of the cable manufacture").  *FIG. 12A*  *FIG. 12B*

J. DEPENDENT CLAIM 10

Claim 10	Disclosure
10. The communication method of claim 9, wherein the first inbound data stream has a per-lane symbol rate in excess of 50 GBd.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: ***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** ***Index Terms*—Active inductor CTLE, bidirectional link, collaborative CDR, conditional phase detection, decision-feedback equalizer (DFE), phase error decimation, regulated CMOS clocking, source-series terminated (SST) driver.** Musah, 3079.

Claim 10	Disclosure
	II. LINK ARCHITECTURE The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 10	Disclosure
	IV. MEASUREMENTS Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. The measured TX output is shown in Fig. 16 at 32 Gb/s operation over a short channel. Fig. 17 shows the on-die 10^{-10} BER eye at 32 Gb/s over a 0.5 m cable using PRBS10 data on a single lane. Amortizing the PLL and clock distribution power over 4 lanes, the link power consumption is 205 mW at 32 Gb/s. Transceiver power efficiency given for multiple data rates from 4 to 32 Gb/s is shown in Fig. 18. Excluding the PLL power, the transceiver power efficiency ranges from 3.4 to 5.7 pJ/b, while equalizing 24 dB and 16 dB of Nyquist rate channel loss at 16 Gb/s and 32 Gb/s, respectively. Due to circuit BW limitations, the equalized channel loss tolerance is 24 dB up to 27 Gb/s and reduces to 16 dB at the highest data rate. When the HP RX is disabled and the LP RX is enabled, the measured power efficiencies are 1.0 pJ/b at 4 Gb/s, 1.5 pJ/b at 8 Gb/s and 2.2 pJ/b at 12 Gb/s with 4.5 dB, 8 dB and 10 dB of channel loss, respectively. A breakdown of the link power is shown in Table I, with PLL power amortized over 4 lanes. Musah, 3086.

Claim 10	Disclosure

TABLE II
COMPARISON TABLE

	[1]	[2]	[3]	[4]	This Work	
CMOS technology	32nm	32nm	28nm	40nm	22nm	
Supply voltage [V]	1.2/1.05	1.00	1.5/1.05	0.90	0.90	1.07
Data rate [Gb/s]	28	32	28	28	16	32
Channel loss at Nyquist [dB]	35	30	34	20	24	16
TX FFE	4-tap	4-tap	3-tap	3-tap	3-tap	3-tap
RX DFE	15-tap	15-tap	14-tap	N/A	6-tap	6-tap
RX peaking amplifier	2-stage	2-stage	1-stage	1-stage	1-stage	1-stage
TX output swing [$V_{pp\text{-}diff}$]	0.950			0.6	0.515	0.630
TX output jitter [ps_{rms}]	0.45		0.25	0.2		<0.54
RX input sensitivity [mV]	15		15	27		35
Area density [mm^2/Gb/s]	0.0289	0.0219	0.0298	0.0506	0.0049	0.0025
Transceiver power efficiency per lane [pJ/b]	24.8	21	20	6.96	4.6	6.4

Musah, 3087.

V. CONCLUSION

We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane.

Musah, 3088.

Claim 10	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 10	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 10	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 10	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 10	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 10	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 10	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER < 10^{-12} over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963. *A. Transmitter Chip Measurement* The TX output is measured after a channel consisting of a doubled bonding wire, a 4-cm PCB trace, and a 0.5-m

Claim 10	Disclosure
	connection cable. Fig. 23(a) shows the over-equalized eye-diagram at 5 Gb/s, where the four sub-levels are contributed by the four FFE taps. Fig. 23(b) and (c) gives the output eye-diagrams at 40 Gb/s before and after applying the four-tap FFE. Obviously, the FFE can significantly improve the eye opening. The eye height and eye width are optimized from 140 mV and 0.45 UI to 180 mV and 0.68 UI, respectively. Meanwhile, the thickness of the eyelid is dramatically reduced from around 330 to 140 mV. Fig. 23(d) shows the properly compensated eye-diagram at the maximum operation speed of 50 Gb/s. Its eye height and eye width are 50 mV and 0.38 UI. Clearly, a wide operation range from 5 to 50 Gb/s is achieved, which is mainly attributed to the multi-MUX-based FFE implementation. Fig. 24 further shows the TX output with four separate eyes. It can be seen that the horizontal eye widths for both fixed clock and PRBS patterns are almost identical, thus proving that the four sampling phases are properly aligned. Zheng, 2972-2973. *B. Receiver Chip Measurement* The RX standalone measurement results are presented in this part. Fig. 25(a) shows the eye-diagram of the 40-Gb/s input data generated by an Anritsu MP1812A through combining four 10-Gb/s PRBS7 sequences, where the single-end eye height and eye width are around 360 mV and 0.71 UI. Fig. 25(b) shows the eye-diagram of the 10-Gb/s recovered

Claim 10	Disclosure
	data with a total jitter of 12.73 ps. The eye-diagrams of the recovered clocks (divided by 2) for the edge sampling and data sampling are shown in Fig. 25(c) and (d), which reveal that the introduced LPFs can optimize the total jitter from 11.48 to 7.66 ps. To demonstrate the effect of the LPFs with adaptively adjusting bandwidth, the jitter transfer (JTRAN) and JTOL curves are measured using a Tektronix BSA286C with a CDR block. The input peak-to-peak swing is tuned to 800 mV and the control voltage of the CTLE is manually set to 710 mV. The JTRAN curves in Fig. 26 illustrate that the bandwidth of the data-sampling path depending on the LPFs is 4 MHz, which is much smaller than 18 MHz for the edge-sampling path determined by the loop parameters. The measured JTOL in Fig. 26 indicates that the embedded LPFs result in a significant dip attenuation around the corner frequency and improve the JTOL amplitudes apparently at high jitter frequencies. Meanwhile, the adaptively adjusting bandwidth of the LPFs makes them exhibit little effect on the phase-tracking slew rate at low jitter frequencies. Additionally, the corner frequency of the JTOL is about 20 MHz, which is much larger than the JTRAN bandwidth of 4 MHz. Zheng, 2973-2974.

Claim 10	Disclosure

Transmitter Chip				
	[4]	[16]	[20]	This work
Technology (nm)	65	14	65	65
Supply (V)	1.2	N/A	1.2	1.2
Data Rate (Gb/s)	50-64	16-40	38.8-42	5-50
Area (mm^2)	1.2 × 1.0	0.215 × 0.13	0.9 × 0.7	1.2 × 0.5
TX Equalization	4-tap FFE	4-tap FFE	5-tap FFE	4-tap FFE
1UI-Delay Gen.	LC-Delay	Multi-MUX	CML-Delay	Multi-MUX
MUX Type	4:1	4:1	N/A	4:1
Data Jitter RJ (ps_{rms})	N/A	0.33@28Gb/s 0.51@40Gb/s	N/A	0.23@40Gb/s 0.18@50Gb/s
Data Jitter (ps) TJ (BER=1e-12)	N/A	10.72@28Gb/s 12.89@40Gb/s	15.1@40Gb/s	9.90@40Gb/s 10.58@50Gb/s
Power (mW)	199*	518	135**	145*
Energy Efficiency (pJ/bit)	3.1	12.9	3.4	3.6

*Exclude PLL power consumption, ** Standalone FFE without data serializer.

Zheng, 2974.

"FIG. 5 illustrates an EYE waveform of a signal obtained after passing a 56 Gbps PAM-4 signal through a raised cosine filter with a bandwidth of 22 GHz and a roll-off of 0.5. In FIG. 5, when the signal has a value higher than a determination threshold 501, the signal is determined to be +3, when the signal has a value between the determination threshold 501 and a determination threshold 502, the signal is determined to be +1, when the signal has a value between the determination threshold 502 and a determination threshold 503, the signal is determined to be −1, and when the signal has a value lower than the determination threshold 503, the signal is determined to be −3. Ranges above the determination thresholds 501, 502, and 503 through which the signal does not pass is referred to as the EYE widths. As seen in FIG. 5, the EYE width is defined by the upper EYE width 505 and the lower the EYE width 506, and the EYE widths 505 and 506 are defined by the data transition time, −3→+3 and +3→−3. The EYE width is narrowed by approximately 15 ps even under the condition that the bandwidth is limited by a frequency higher than the

Claim 10	Disclosure
	Nyquist frequency and there is almost no influence of ISI. In this manner, the EYE width of the PAM multilevel signal is narrowed relative to that of the NRZ signal due to data pattern dependence." Norimatsu, 4: 27-50.

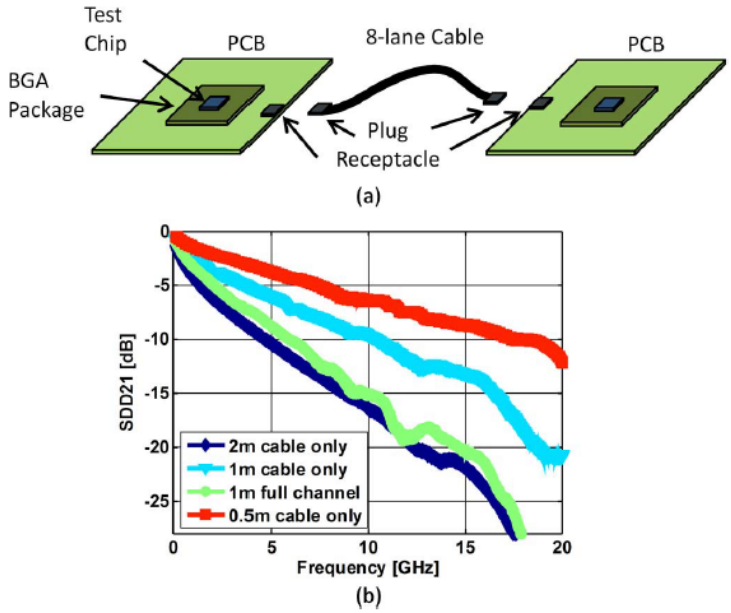
K. INDEPENDENT CLAIM 11

Claim 11	Disclosure
11[pre] A cable manufacturing method that comprises:	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: **1.1 Introduction** This specification defines the Common Management Interface Specification (CMIS) for QSFP-DD, OSFP and COBO in order to enable flexible use of modules and cable assemblies (hereafter referred to as modules unless cable assemblies are specifically mentioned) by the user. It shares some similarities with the management interfaces used in other form factors such as QSFP, SFP, and CFP. This specification supports a module with 8 host electrical lanes. Support for modules with more host lanes is possible (in increments of up to 8 lanes) by a bank selection feature (which allows several instances of an adressable page to exist in the paged register map). Due to this new mechanism this specification is not backwards compatible with SFF-8636. Some host ports may support both 4-channel and 8-channel devices; when a 4-channel device is inserted into such a port the appropriate memory map (e.g. SFF-8636) must be used. This case is outside the scope of this document. The host-to-module interactions needed to initialize active modules are presented in two state machines. A module-level state machine defines the initialization of the management interface as well as control of the module-wide power mode. A data path-specific state machine defines the host and module interactions and behaviors needed for power up and initialization of the data path(s) in the module. The CMIS is intended to cover a wide range of possible module functionalities and applications, ranging from cable assemblies to coherent DWDM modules. The CMIS is designed with the intent not to burden the simple cases but to provide a common set of management interactions and a common register map. In some modules, multiplexing of the high speed signals between the host electrical interface and the module media interface may occur in the module. In this specification, all references to lane numbers are based on the electrical connector interface lanes, unless otherwise indicated. In cases where a status or control aspect is applicable only to lanes after multiplexing or demultiplexing has occurred, the status or control is intended to apply to all lanes in the data path, unless otherwise indicated. Symmetry is expected between the Tx and the Rx hardware structure; for example Tx lanes that are multiplexed in the Tx are demultiplexed in the Rx. Each Application selected by the host is applied to the same Tx and Rx host electrical lanes. CMIS, 5-6.

Claim 11	Disclosure
	Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. Table 1 and Table 2 provide a summary of the high-level behaviors and properties of each module state for passive copper cable assembly and active module implementations, respectively. Implementers of passive copper cable assemblies should note that this specification was designed to allow for flat-memory EEPROM implementations for that cable type. Active modules and active cable assemblies shall use the paged memory model. For all module types, refer to sections 1.4.3-1.4.9 for detailed requirements for each state. CMIS, 18.

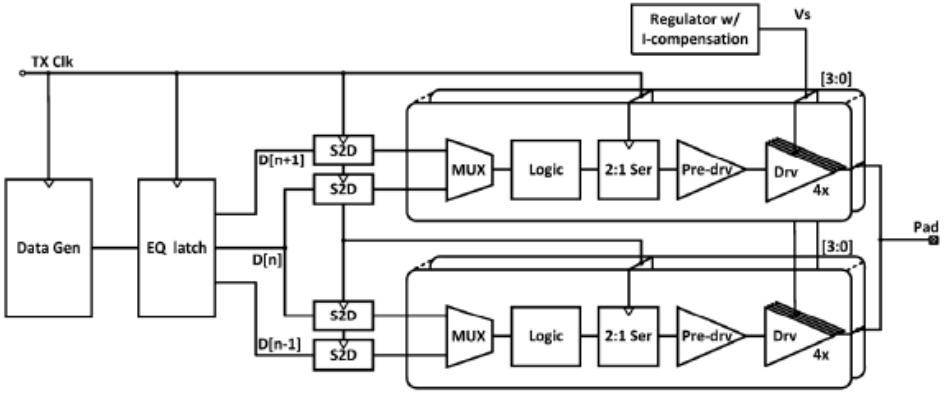
Claim 11	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

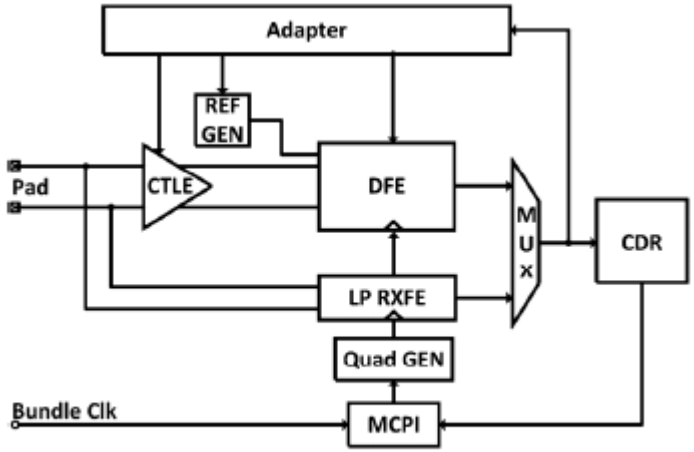
Claim 11	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 11	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 11	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

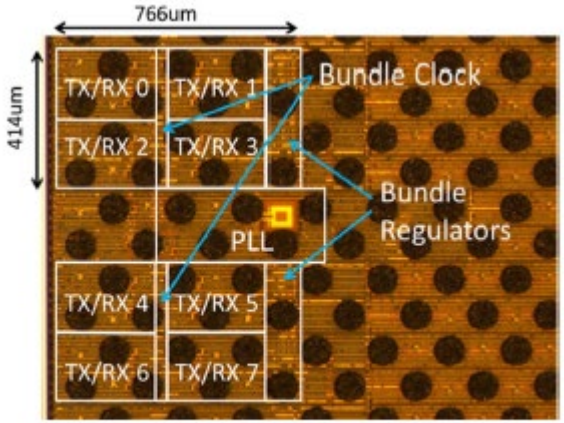
Claim 11	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 11	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

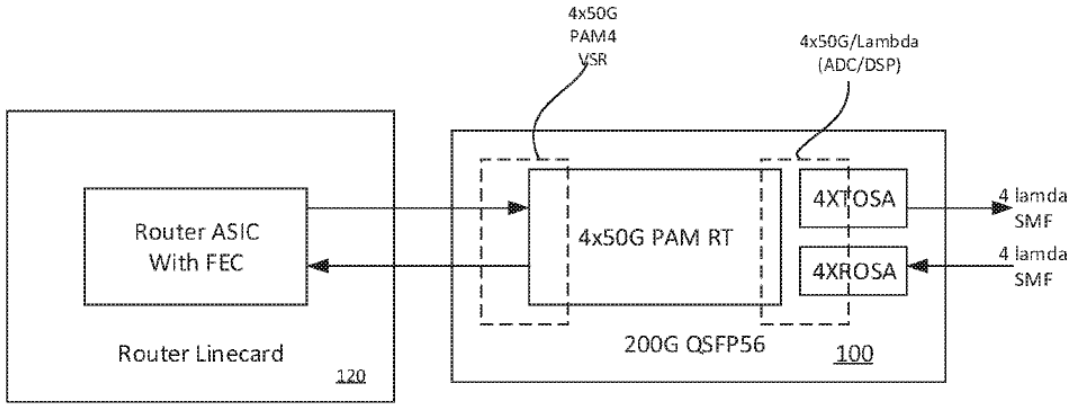
Claim 11	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

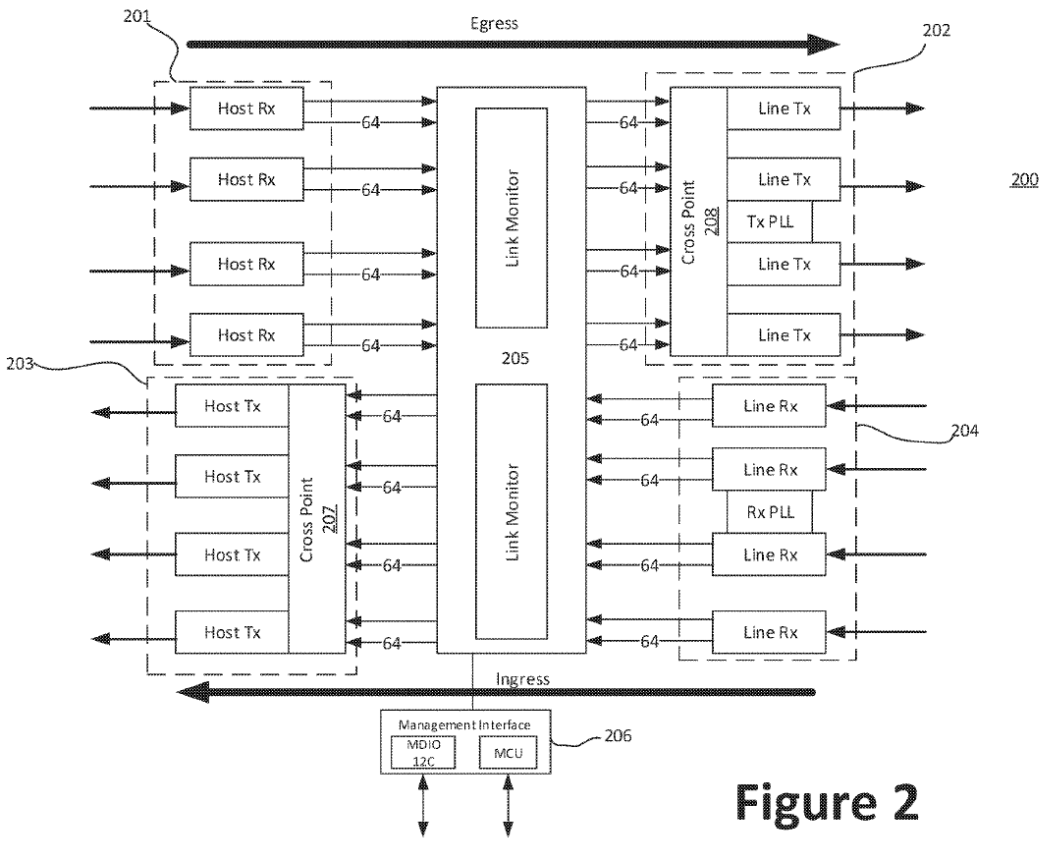
Claim 11	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 11	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 11	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 11	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free $(BER < 10^{-12})$ transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088.

Claim 11	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 11	Disclosure
	 Riani, Figure 2.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 11	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 11	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 11	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 11	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 11	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 11	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 11	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 11	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 11	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 11	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 11	Disclosure
	THE exponential growth of cloud computing, social networking, and multimedia sharing has led to an explosive bandwidth demand on data communication in both telecommunication equipment and inter/intra data center [1], [2]. To accommodate to this requirement, the data rate of the wireline serializer/deserializer (SerDes) transceiver has been continuously increased [3]–[5]. Currently, 25–28 Gb/s serial links approved by InfiniBand EDR, 32GFC, and CEI-28G have stepped into the period of industrial deployment [1], [3], [6]. The 38–64 Gb/s transceivers, which will play a key role in the next-generation data rate supported by Ethernet 400GbE, InfiniBand HDR, and CEI-56G, have attracted increasing attentions in the industry and the academia [2], [4], [5], [7]–[11]. The main challenges in designing such high-speed transceivers originate from the ever decreased unit interval (UI) period, which not only poses high bandwidth requests on the blocks located at the critical path, but also makes the link timing budget extremely tight. Moreover, advanced processes cannot completely solve these problems, since the parasitic capacitances/resistances at the high-speed outputs usually do not scale well with the technology due to the bonding and/or electro-static discharge (ESD) protection requirements. Zheng, 2963.

Claim 11	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 11	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 11	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 11	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 11	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

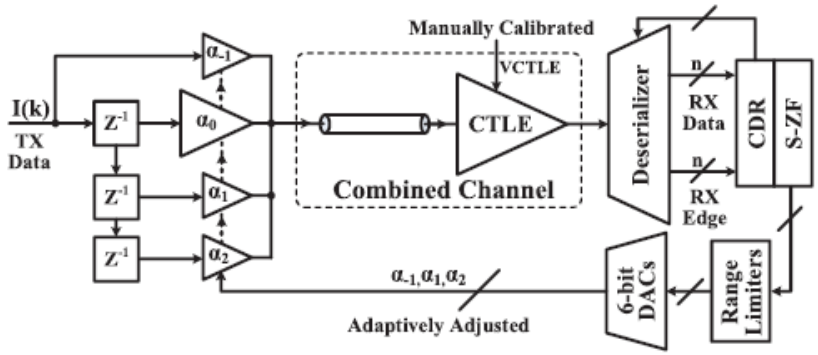


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 11	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 11	Disclosure

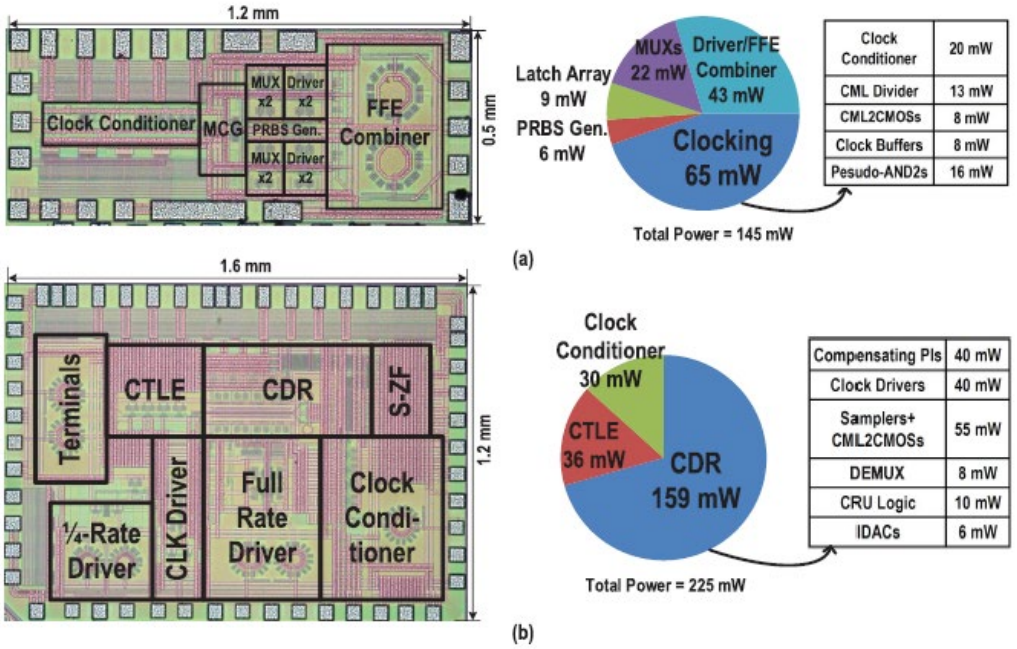


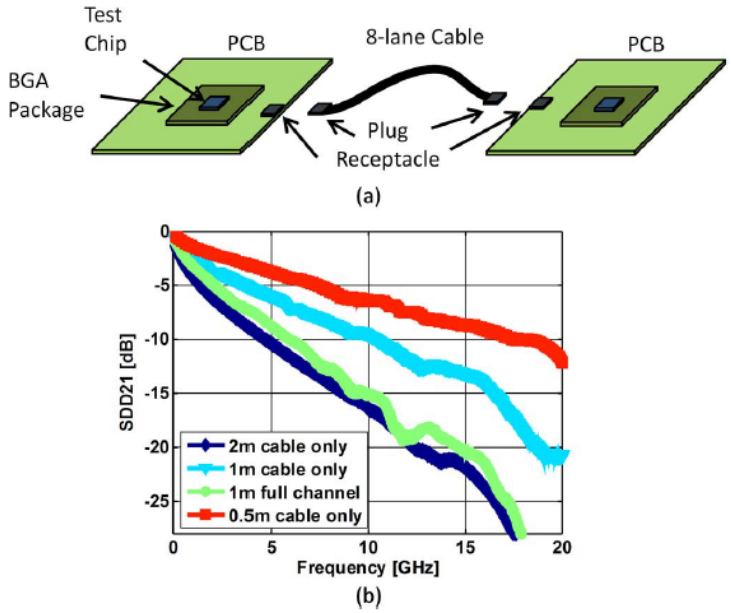
Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip.

Zheng, 2973.

Claim 11	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 1, the data transmission system 1 is in accordance with DP1.4, for example, and includes an upstream device 2, a downstream device 4, and an active cable 3 connecting the upstream device 2 and downstream device 4." Kobayashi, 2:41-45. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream

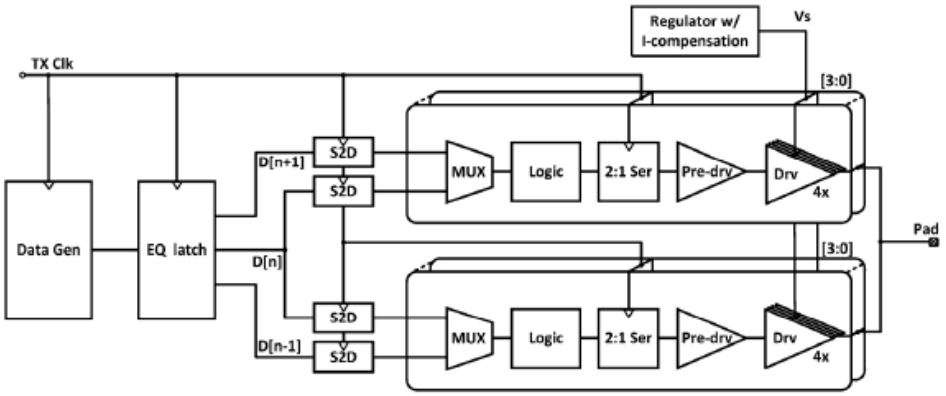
Claim 11	Disclosure
	transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK" Kobayashi, 4:4-22.
11[a] connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver;	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: ***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.**

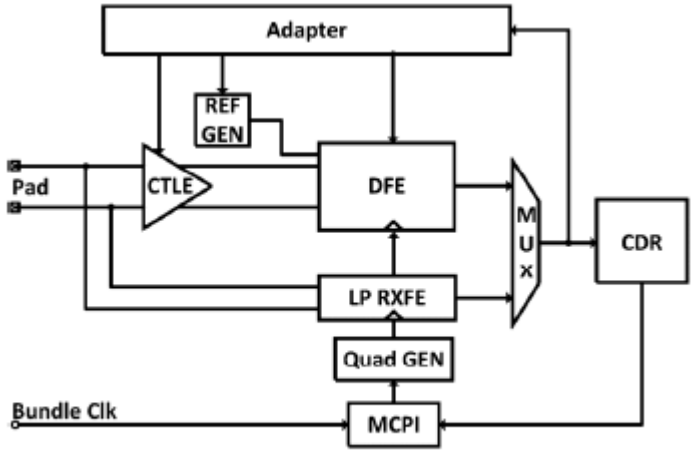
Claim 11	Disclosure
	Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 11	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 11	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

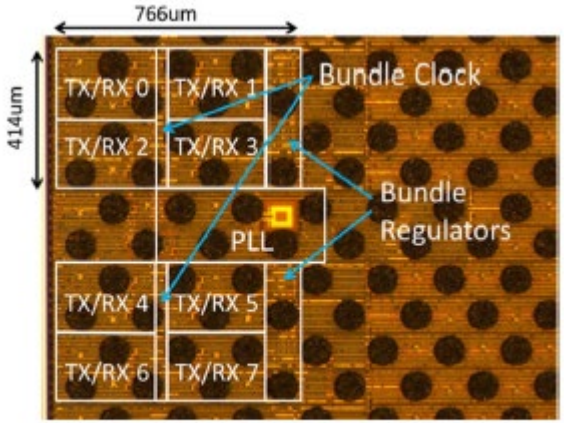
Claim 11	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 11	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 11	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

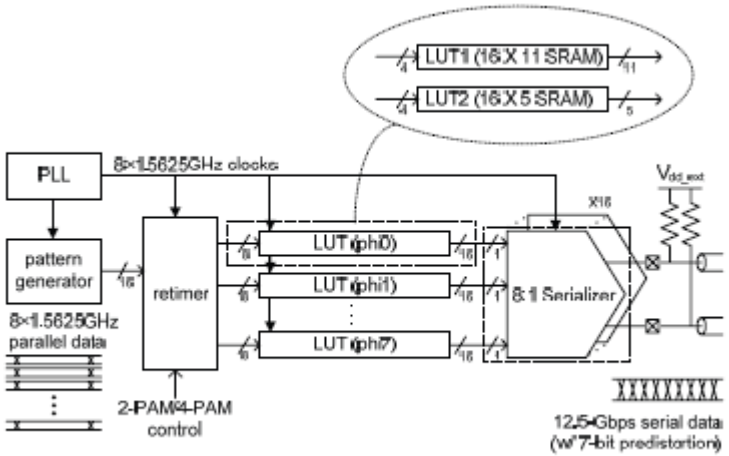
Claim 11	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 11	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 11	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

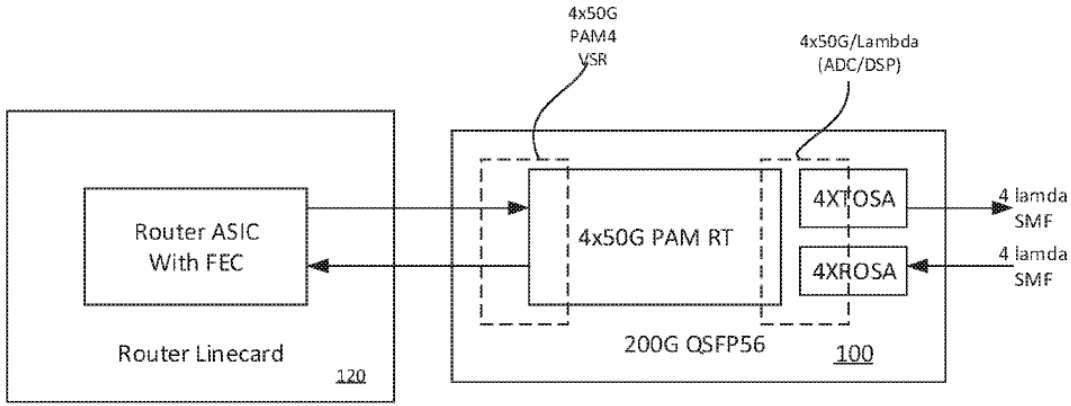
Claim 11	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13µm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

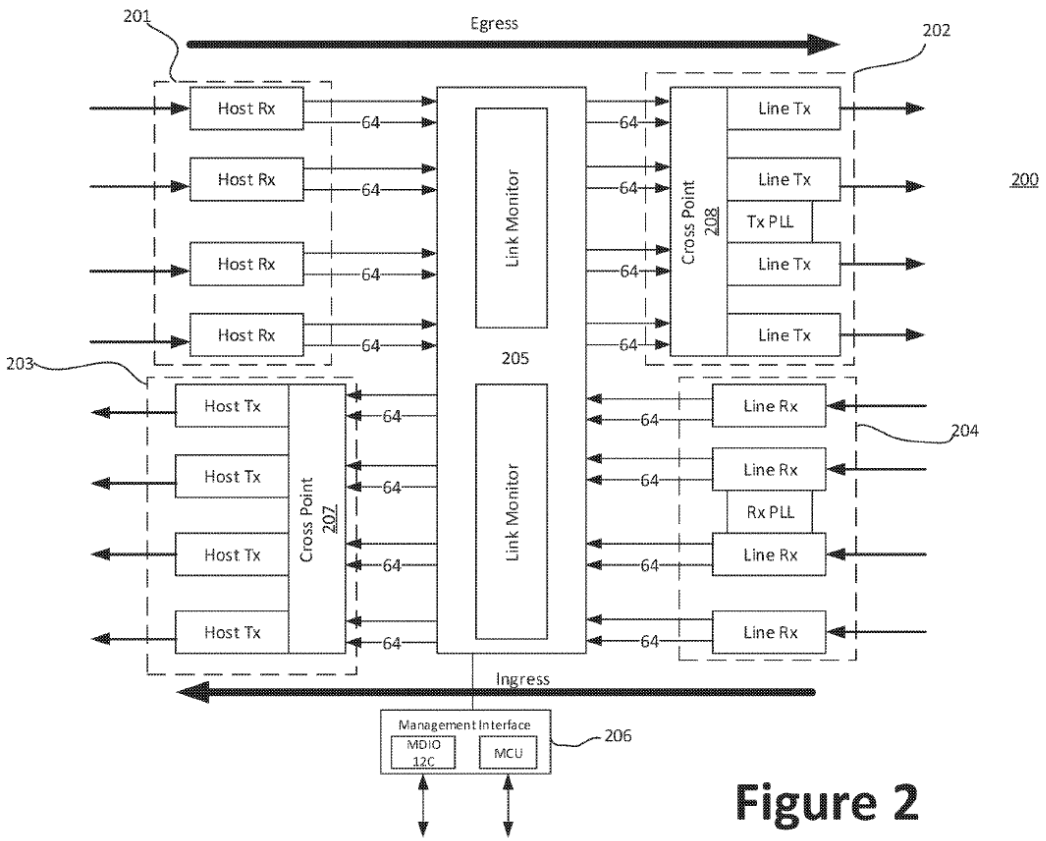
Claim 11	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 11	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 11	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 11	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 11	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 11	Disclosure
	 Riani, Figure 2.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 11	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 11	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 11	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 11	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 11	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 11	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 11	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 11	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 11	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 11	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 11	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 11	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 11	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 11	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 11	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

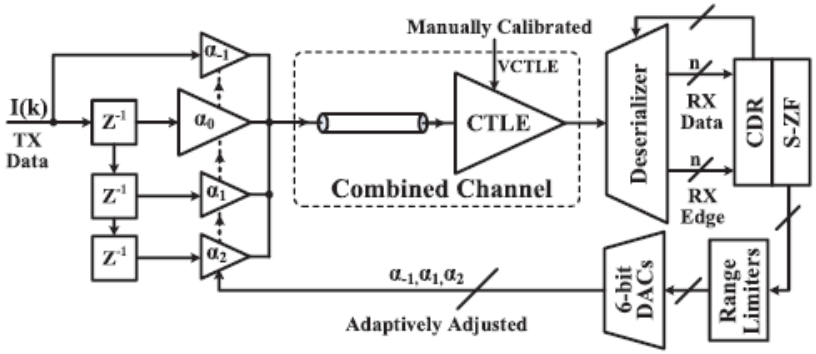
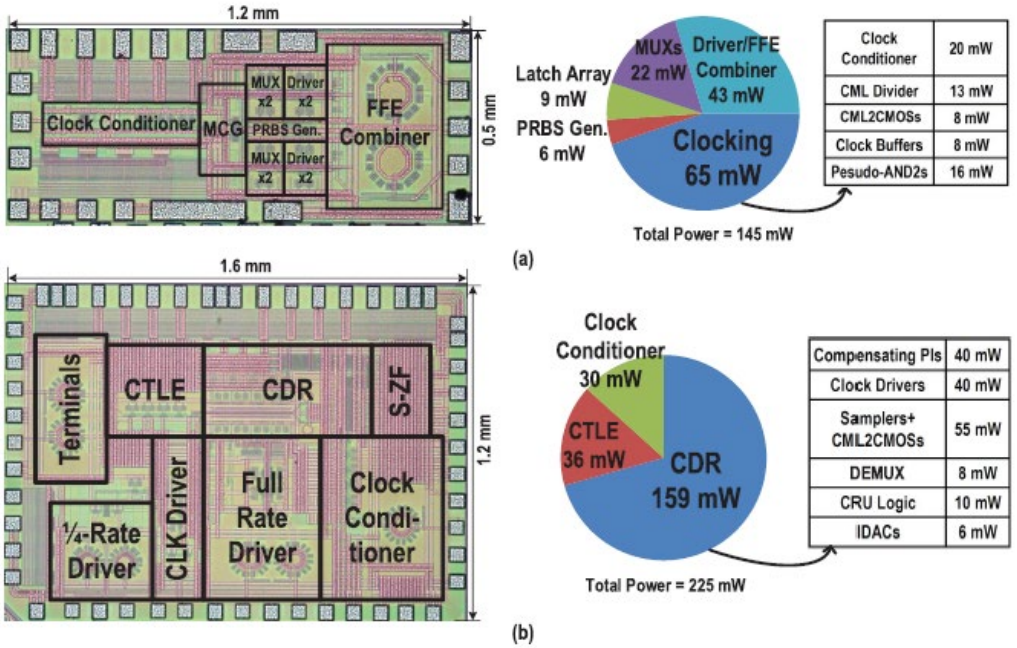


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

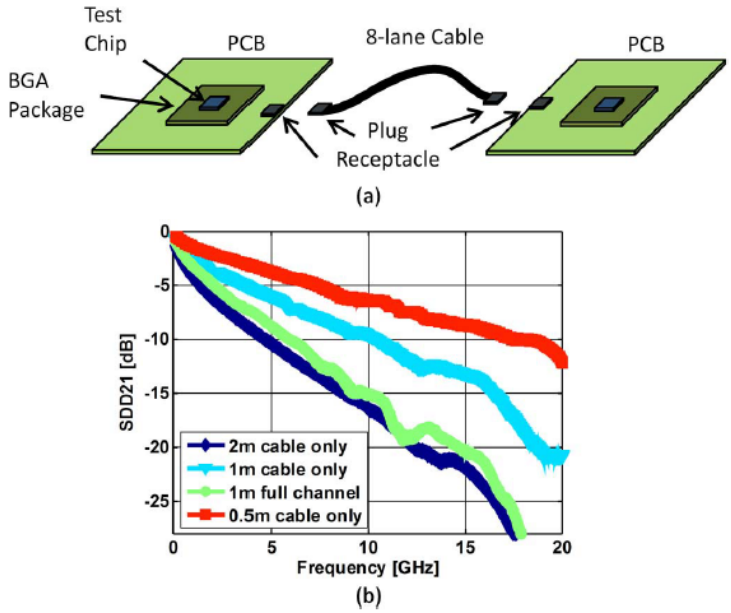
Claim 11	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 11	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 11	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 1, the data transmission system 1 is in accordance with DP1.4, for example, and includes an upstream device 2, a downstream device 4, and an active cable 3 connecting the upstream device 2 and downstream device 4." Kobayashi, 2:41-45. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream

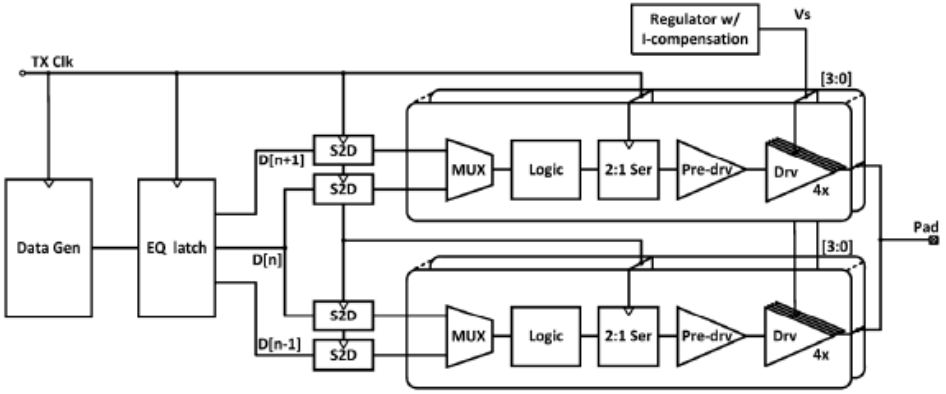
Claim 11	Disclosure
	transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK" Kobayashi, 4:4-22.
11[b] packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: ***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.**

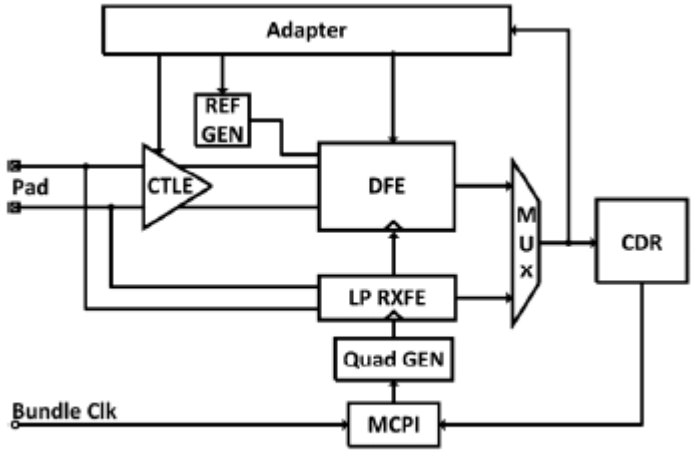
Claim 11	Disclosure
	Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 11	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 11	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

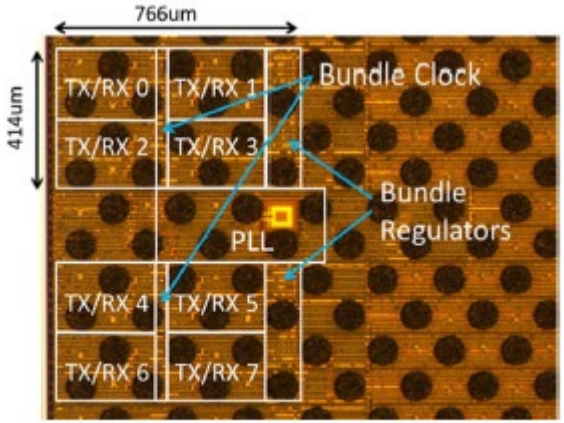
Claim 11	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 11	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 11	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

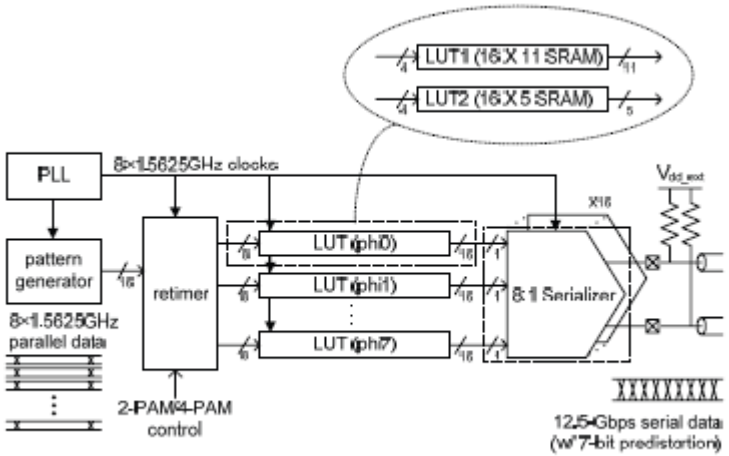
Claim 11	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 11	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 11	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

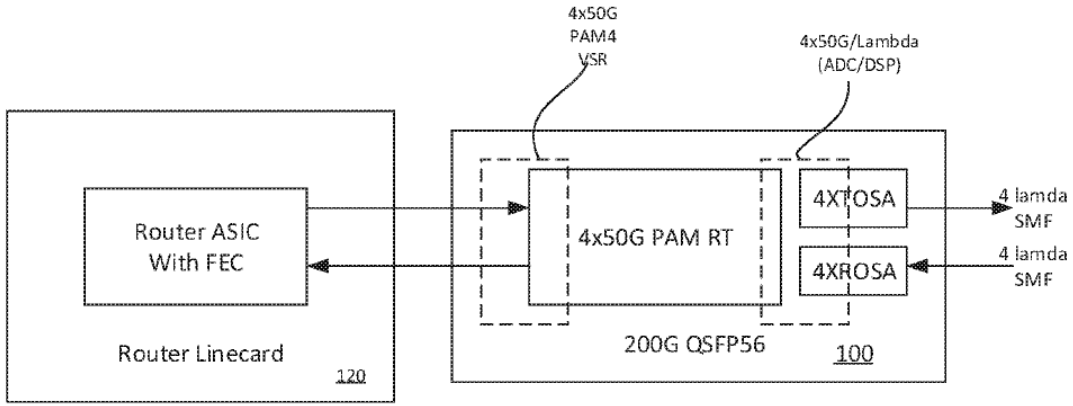
Claim 11	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13µm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

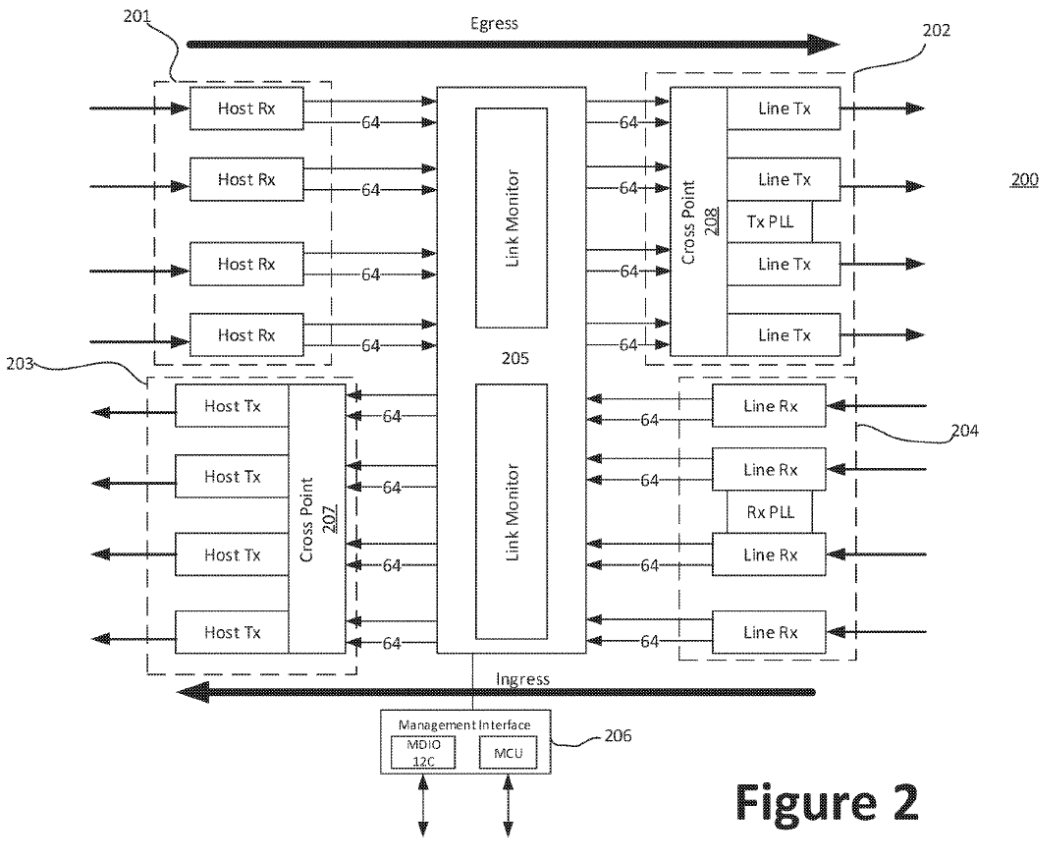
Claim 11	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 11	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 11	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 11	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 11	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 11	Disclosure
	 Riani, Figure 2.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 11	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 11	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 11	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 11	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 11	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 11	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 11	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 11	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 11	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 11	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 11	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 11	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 11	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 11	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 11	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

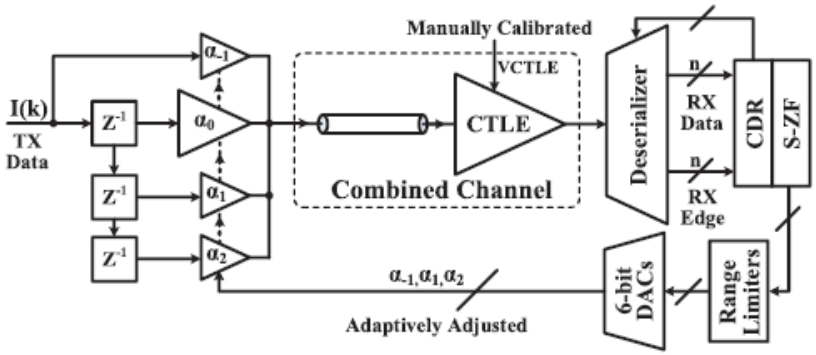


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 11	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 11	Disclosure

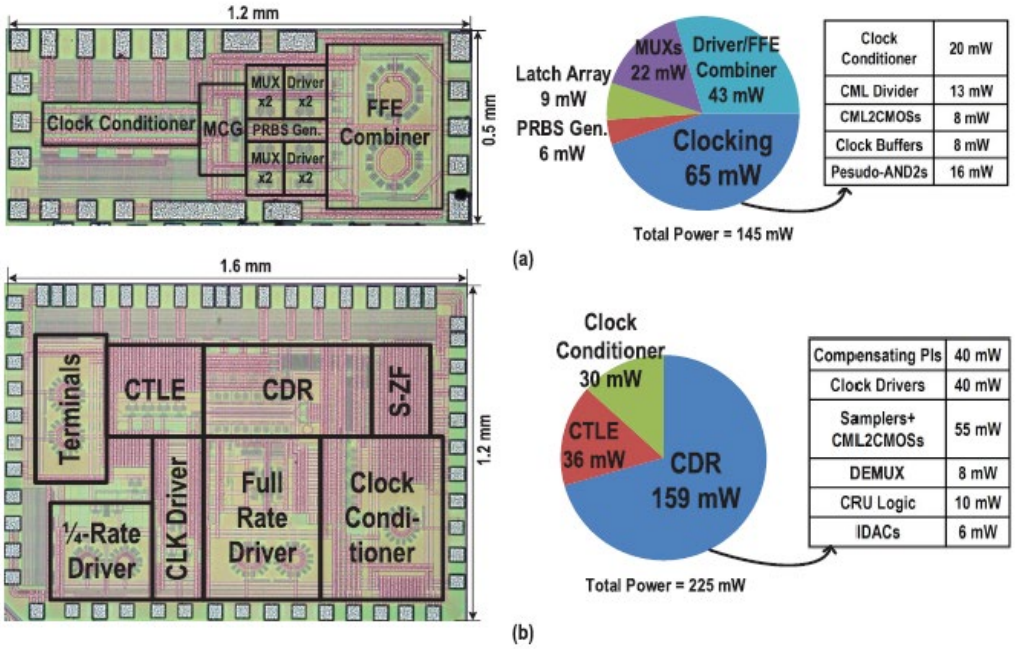


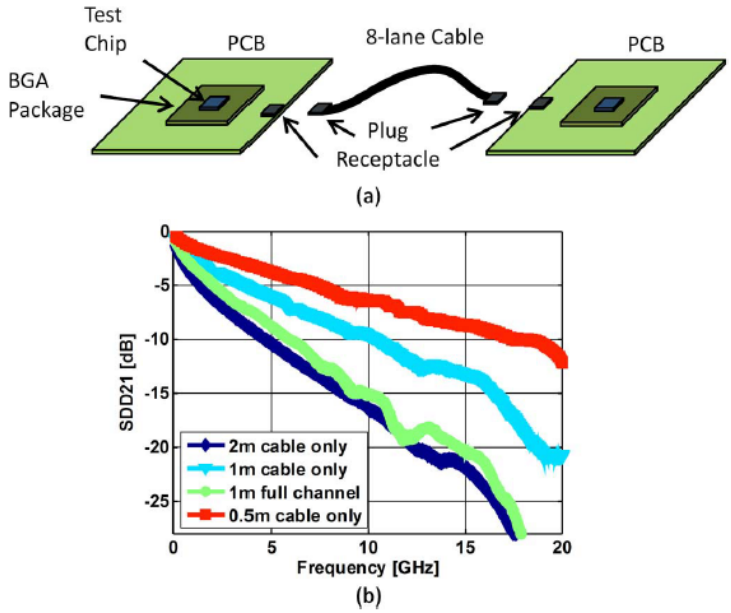
Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip.

Zheng, 2973.

Claim 11	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the

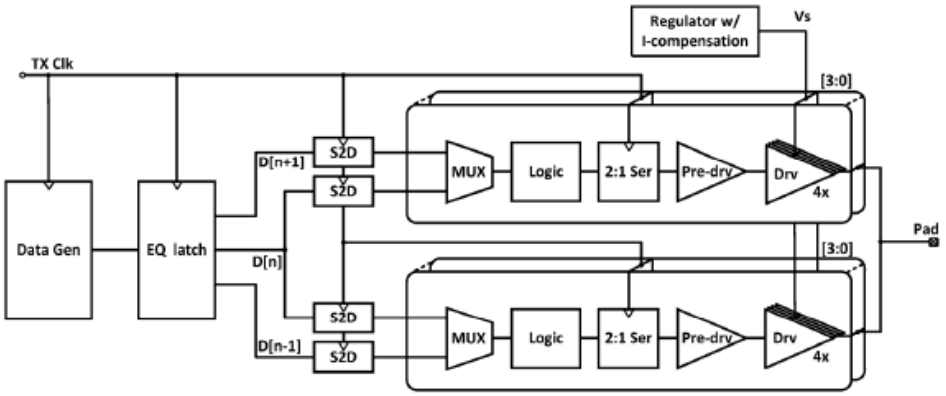
Claim 11	Disclosure
	IN_LT_SEQ_MARK" Kobayashi, 4:4-22.
11[c] packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device,	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: ***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

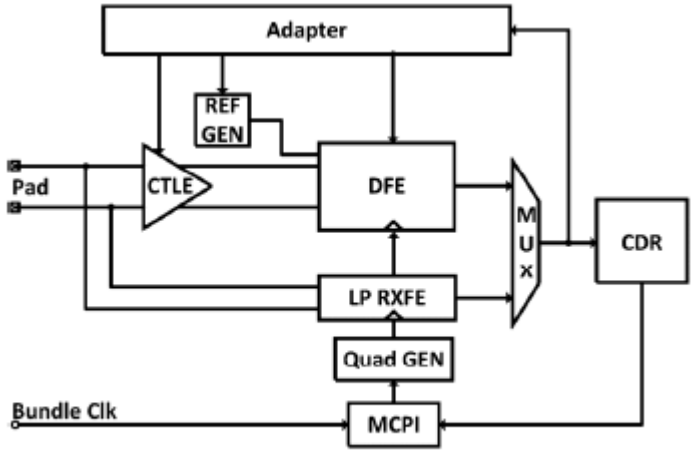
Claim 11	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 11	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 11	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

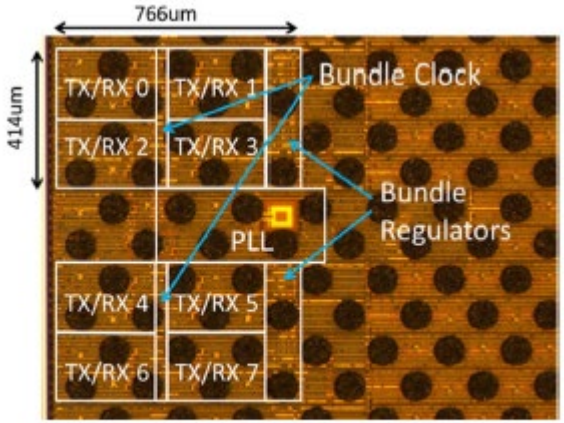
Claim 11	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 11	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 11	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

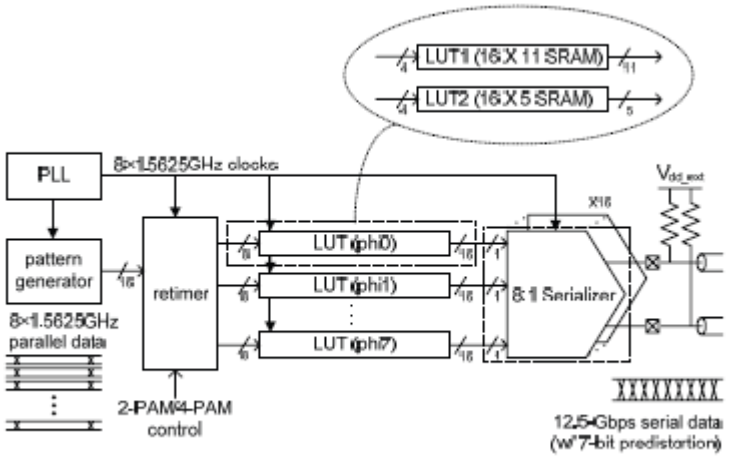
Claim 11	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 11	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 11	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

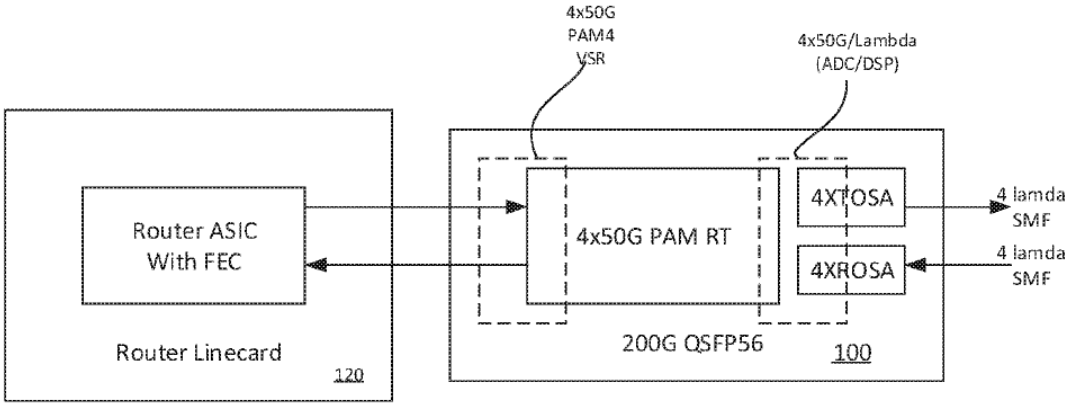
Claim 11	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13µm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

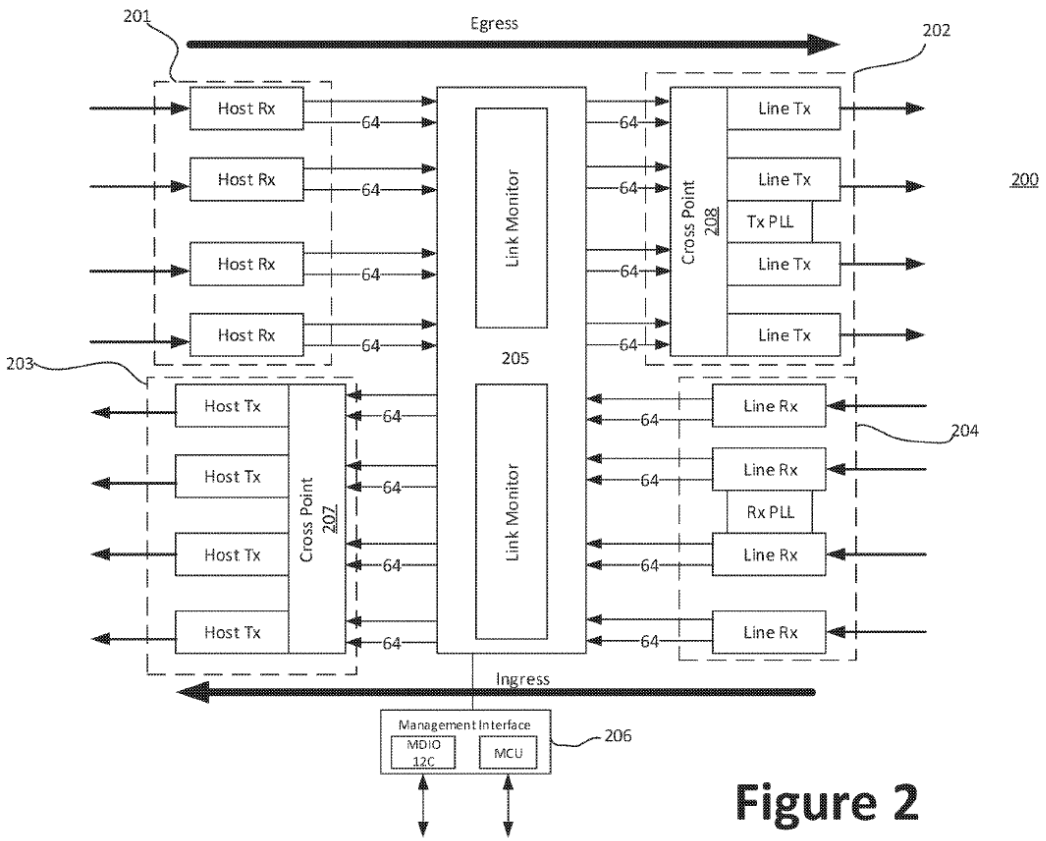
Claim 11	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 11	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 11	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 11	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 11	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 11	Disclosure
	 Riani, Figure 2.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 11	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 11	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 11	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 11	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 11	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 11	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 11	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 11	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 11	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 11	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 11	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 11	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 11	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 11	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 11	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

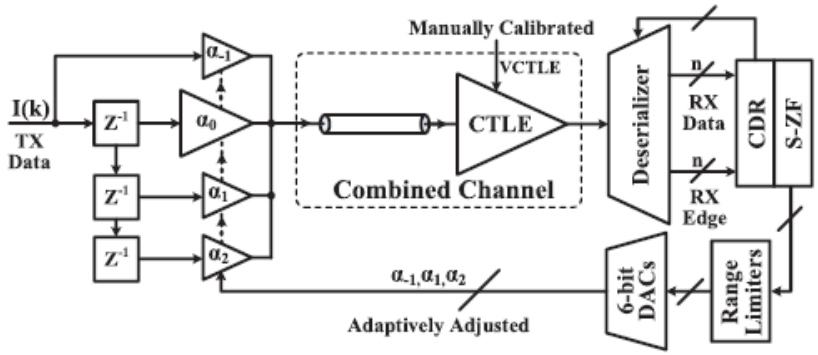


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 11	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 11	Disclosure

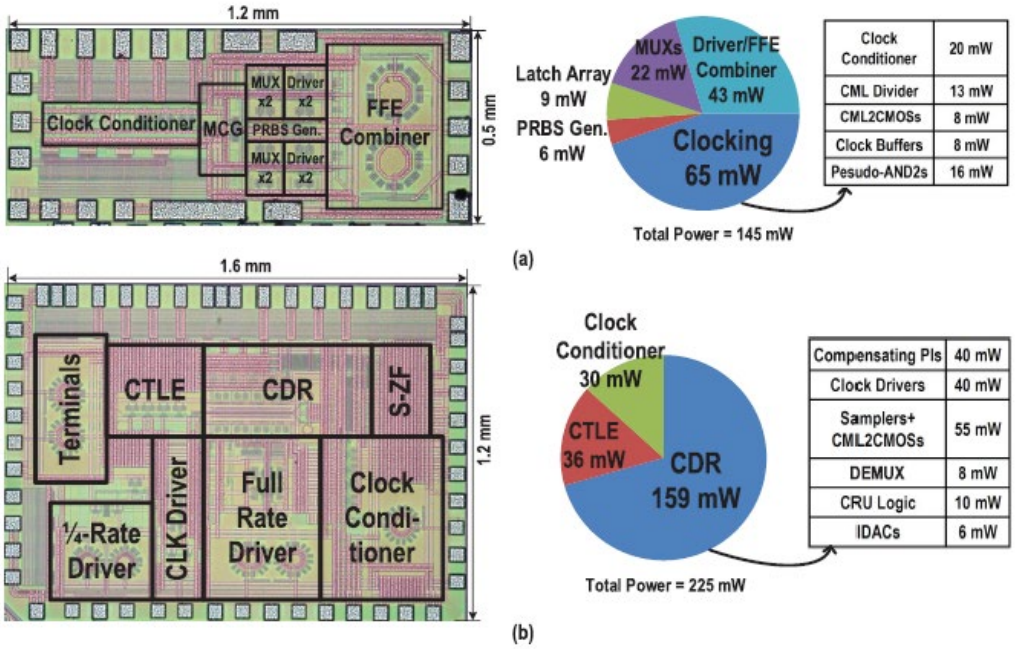


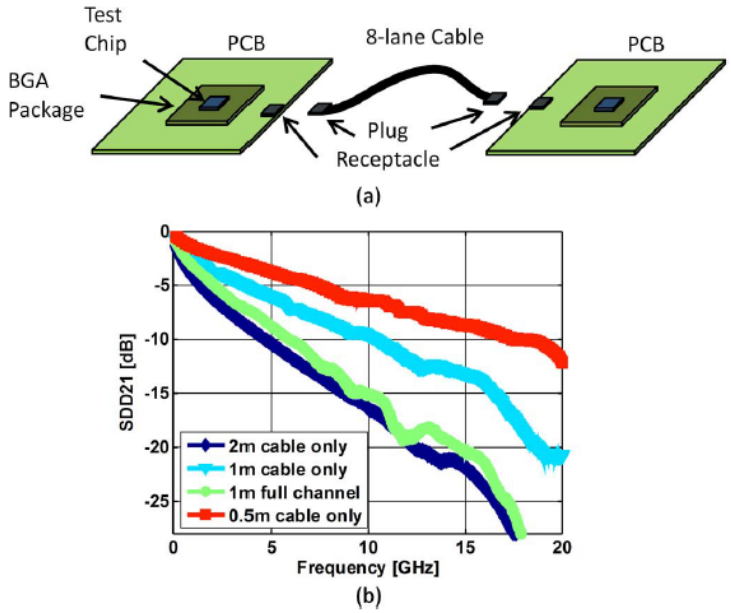
Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip.

Zheng, 2973.

Claim 11	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The downstream device 4 receives the serial bit stream transmitted from the active cable 3 in the upstream facing RX 40a in the retimer 40. The retimer 40 performs a waveform shaping on the serial bit stream received by the upstream facing RX 40a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 40b to a sink 41. The sink 41 displays a video, for example, based on the received serial bit data." Kobayashi, 3:20-28.
11[d] the first and second transceivers being configured to perform clock and data recovery on the first and second	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations:

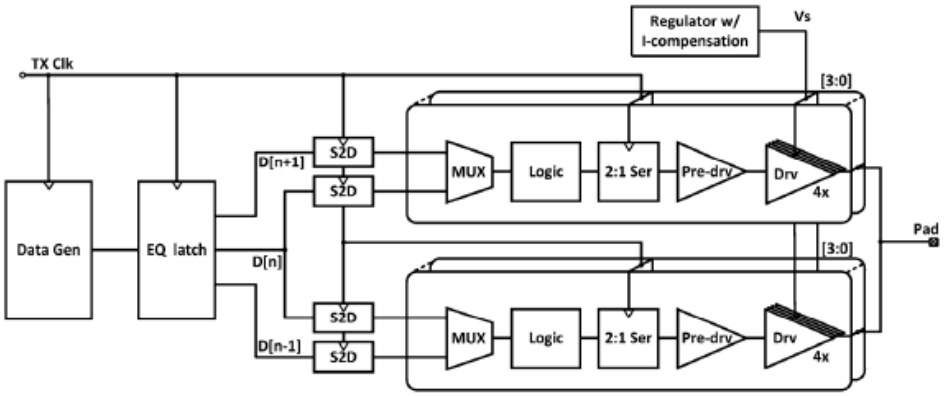
Claim 11	Disclosure
electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams,	*Abstract*—**This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

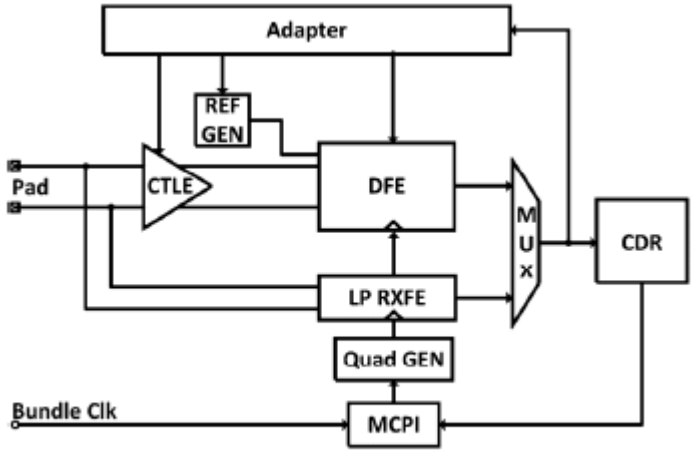
Claim 11	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 11	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 11	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

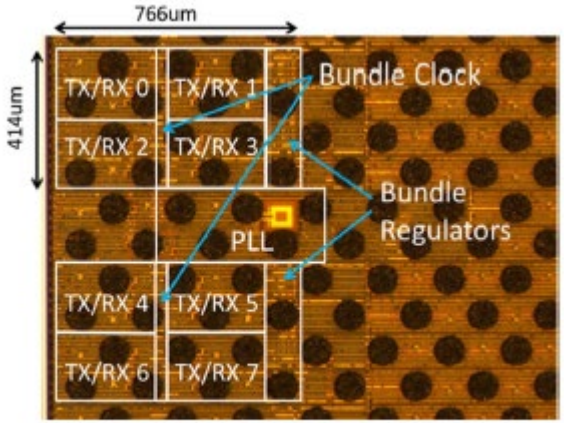
Claim 11	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 11	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 11	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

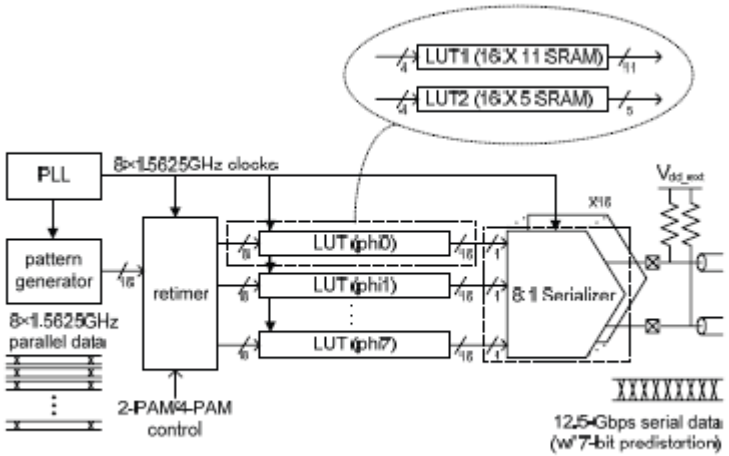
Claim 11	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 11	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 11	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

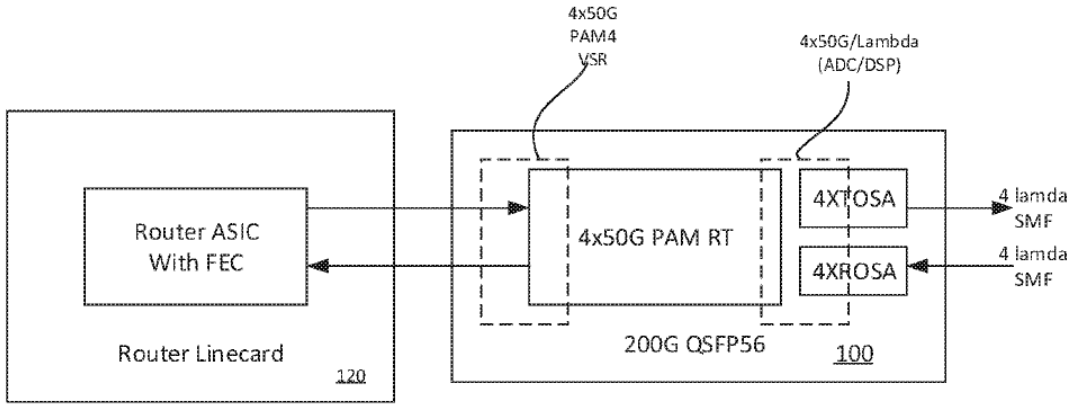
Claim 11	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13µm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

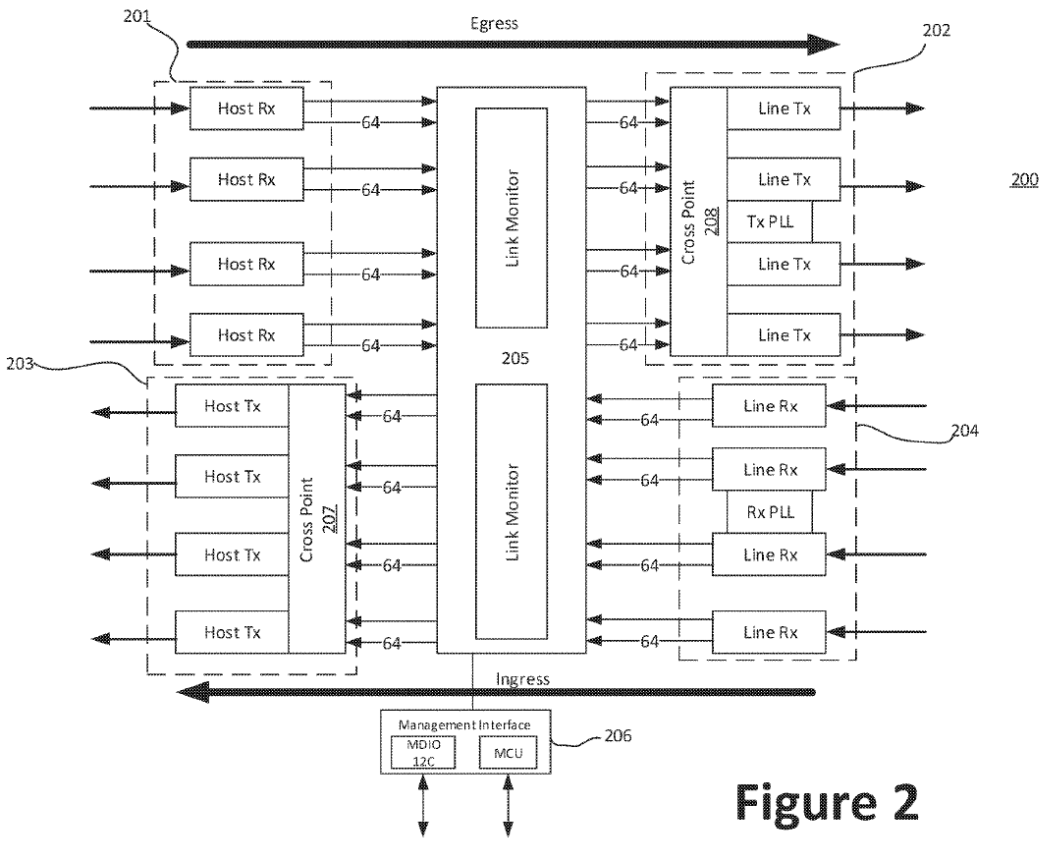
Claim 11	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 11	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 11	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 11	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 11	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 11	Disclosure
	 Figure 2 Riani, Figure 2.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 11	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 11	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 11	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 11	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 11	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 11	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 11	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 11	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 11	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 11	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 11	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 11	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 11	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 11	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 11	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

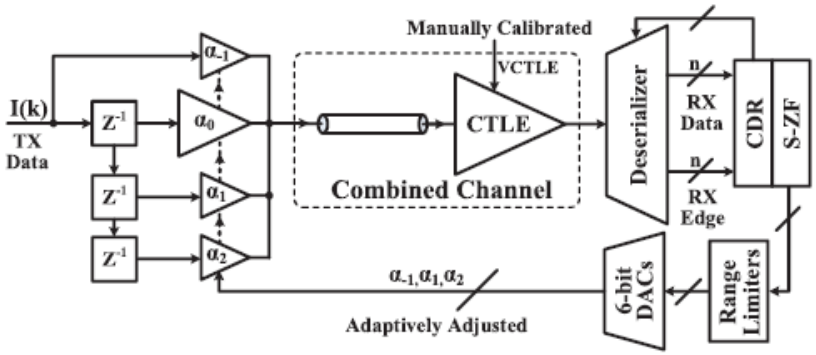
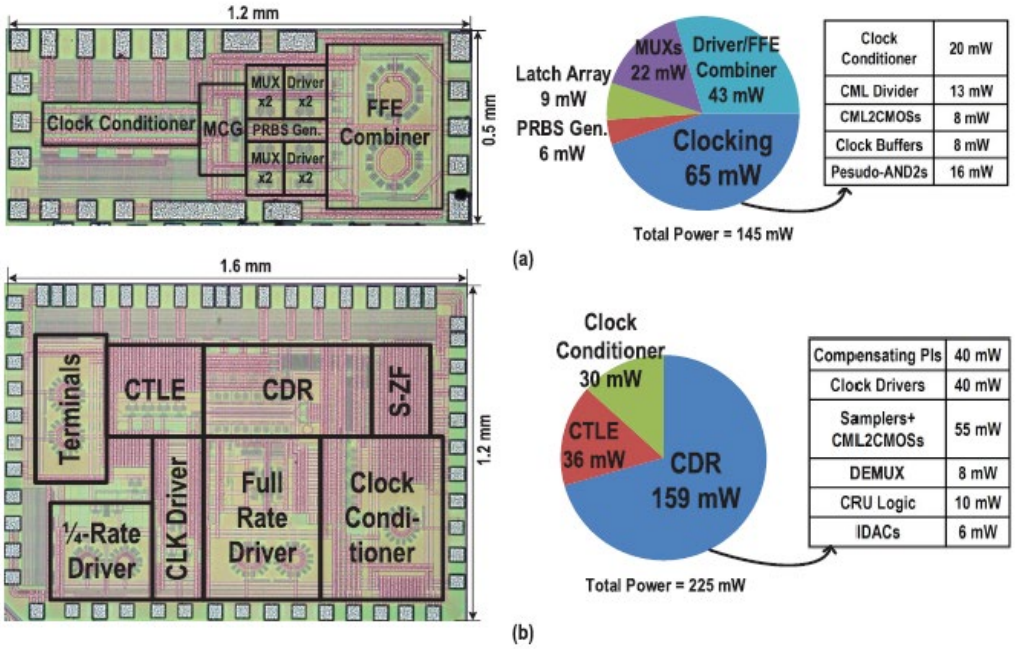


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

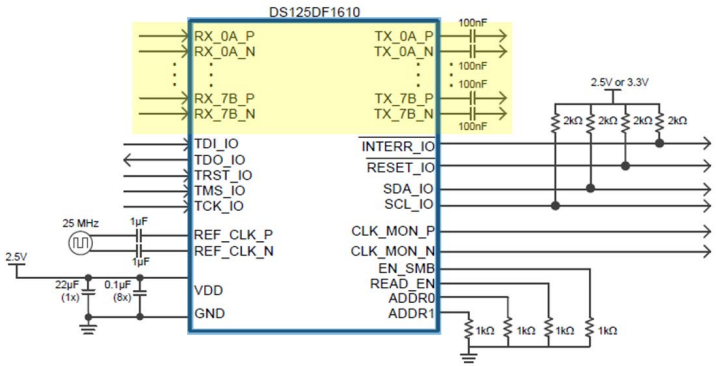
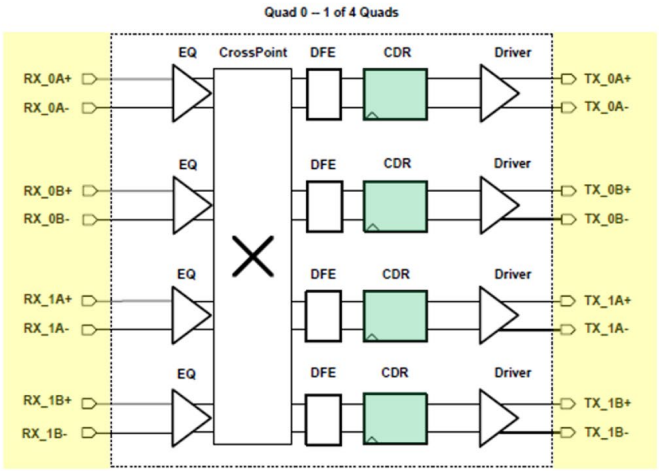
Claim 11	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

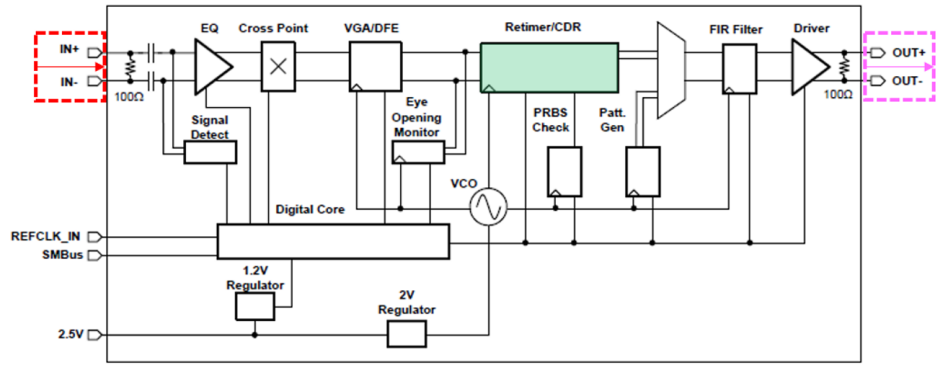
Claim 11	Disclosure
	 Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip. Zheng, 2973.

Claim 11	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The active cable 3 receives the serial bit stream transmitted from the upstream device 2 in the upstream facing RX 30a in one retimer 30. The retimer 30 performs a waveform shaping on the serial bit stream received by the upstream facing RX 30a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 30b to the other retime 31. The retimer 31 receives the serial bit stream transmitted from the retimer 30 in the upstream facing RX 31a. The retimer 31 performs a waveform shaping on the serial bit stream received by the upstream facing RX 31a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 31b to the downstream device 4." Kobayashi, 3:5-19. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a

Claim 11	Disclosure
	TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver." Kobayashi, 4:4-9. "The exchange module 202 is configured to communicate capabilities information with a remote link partner including host loss information, RS-FEC ability information, and RS-FEC request information. The exchange module 202 may transmit local host loss information to the link partner and receive remote host loss information from the link partner. In some embodiments, the exchange module 202 may be included in or otherwise established by the autonegotiation module 104 and thus the capabilities information may be exchanged during execution of an autonegotiation protocol. In some embodiments, the exchange module 202 may be included in or otherwise established by the PMD/PMA module 106 and thus the capabilities information may be exchanged during a startup protocol performed by the PMD/PMA module 106." Lusted, paragraph 23. "The autonegotiation module 104 is configured to auto-negotiate line transmission speed, mode of operation, and other communication parameters with a link partner when the communication lane 102 is brought up. Additionally, in some embodiments the autonegotiation module 104 may be configured to exchange capabilities information with the link partner including host insertion loss information, RS-FEC ability information, and RS-FEC request information. The autonegotiation module 104 may encode the capabilities information, for example, in an autonegotiation base page or in a next page. Although illustrated in FIG. 1 as coupled between the PMD/PMA 106 and the communication lanes 102, in other embodiments the autonegotiation module 104 may be included at different positions in the Ethernet port logic 100. For example, in some embodiments the autonegotiation module 104 may be coupled between the PMD/PMA 106 and the FEC 108." Lusted, paragraph 17. "In view of the above transmission characteristics of twisted-pair, current Ethernet chips are usually equipped with preemphasis technique of a transmitting end and equalization technique of a receiving end

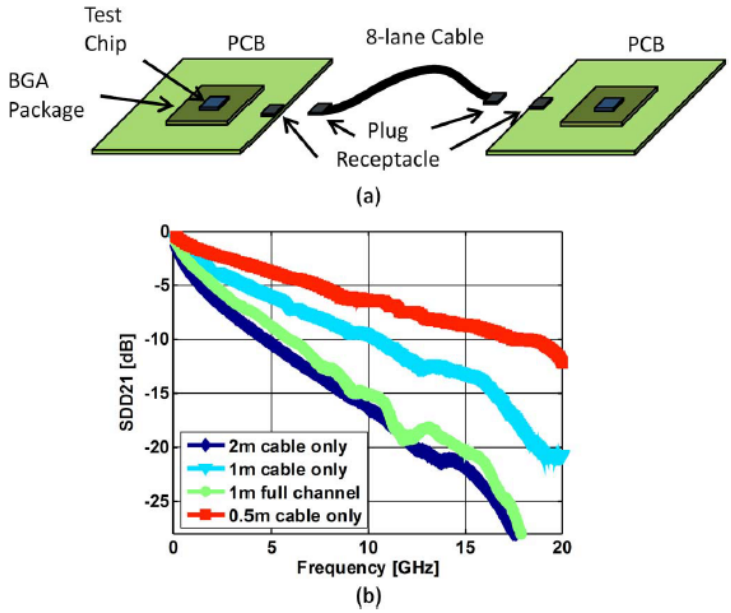
Claim 11	Disclosure
	to compensate the difference in transmission attenuation of physical layer signals on different frequencies on the same medium during Ethernet baseband transmission. Main functions of the preemphasis technique of the transmitting end and the equalization technique of the receiving end include: amplifying signals on different frequencies differently at the transmitting end to compensate different transmission attenuation in the twisted pair; applying the equalization technique to different frequency components in signals received at the receiving end to compensate the attenuation." Yu, paragraph 34. "An embodiment of the present invention provides an equalizer setting apparatus, which uses a filter circuit 101, an analog-to-digital converter 102, a digital memory 103, a digital comparator 104 and a first digital accumulator 105, the filter circuit 101, the analog-to-digital converter 102, the digital memory 103, the digital comparator 104 and the first digital accumulator 105 are connected in sequence, the output end of the equalizer 201 is connected with the input end of the filter circuit 101, the output end of the first digital accumulator 105 is connected with the set value input end of the equalizer 201, the output end of the analog-to-digital converter 102 is connected with the input end of the digital comparator 104, so that the problems that the setting value of the equalizer is accurately set in the prior art, which is time-consuming and labor-consuming are solved, the method has the advantages of achieving accurate setting of the set value of the equalizer in a single time, fast, simple, convenient, accurate and low-cost manner and saving labor force to a certain extent." Yin, paragraph 26 (English translation). *DS125DF1610 Retimer Publication* The DS125DF1610 circuit is illustrated in the Simplified Schematic and Figure 1 below. The highlighted pins illustrate sixteen channels of data, with each channel having two differential (Positive and Negative) input pins (RX_0A_P/N through RX_7B_P/N) to receive the channel of data and corresponding output pins (TX_0A_P/N through TX_7B_P/N) to transmit the channel of data after processing. *See, e.g.*, DS125DF1610 at §§ 3, 7.2. Thus, DS125DF1610's retimer is a transceiver that, when used in Tang's

Claim 11	Disclosure
	cable, receives one or more inbound data streams (on RX_0A_P/N through RX_7B_P/N), and transmits one or more transit data streams (via pins TX_0A_P/N through TX_7B_P/N). **Simplified Schematic**   **Figure 1. DS125DF1610 Simplified Cross Point Diagram** Figure 1 above shows four channels and illustrates that DS125DF1610's retimer processes each data

Claim 11	Disclosure
	channel by, inter alia, performing "clock and data recovery (CDR)." *See id*. at §§ 3, 7.1. A channel's data path is shown in more detail in DS125DF1610 Figure 2 (below), which illustrates the input signal conveying an inbound data stream and the transit signal conveying a transit data stream in Tang's cable when DS125DF1610's retimer implements Tang's signal driver 44.  **Figure 2. DS125DF1610 Simplified Data Path Diagram** The Retimer/CDR circuit performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream. *See id*. at § 7.3.6. The '252 Patent specification makes clear that the input signal from the host can be pre-processed before CDR is performed on it. An ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data for output as the transit data stream because after extracting the input signal's timing and using that timing to sample and extract the input signal's data in an analog-to-digital CDR process, the retimer generates a new data stream for equalization by the FIR Filter (a digital-to-analog process) and to be driven for output by the differential driver (which produces an analog signal with configurable output voltage levels) to convey the output data stream (transit data stream when outputting over the cable) as an analog signal over the cable conductors, where the new signal is a "re-modulation" of the data. *See id*. at §§ 7.3.6-7.3.9.

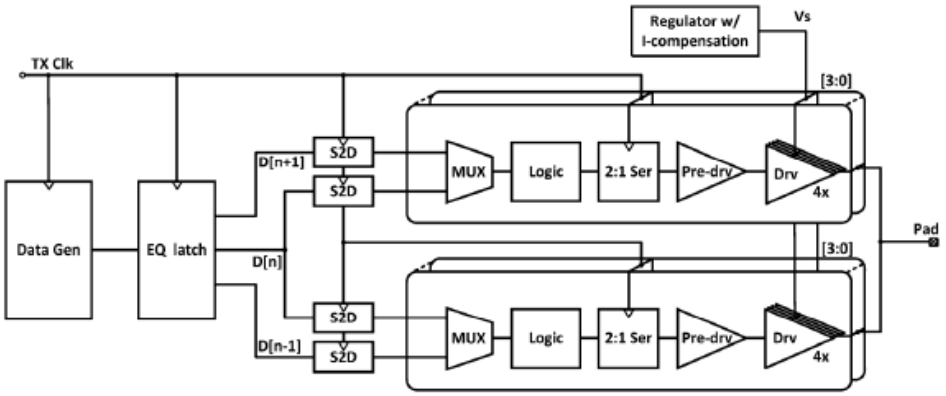
Claim 11	Disclosure
11[e] configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: ***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

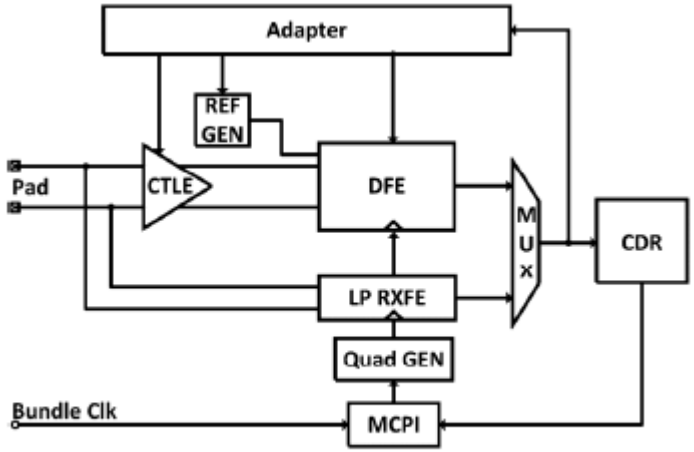
Claim 11	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 11	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 11	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

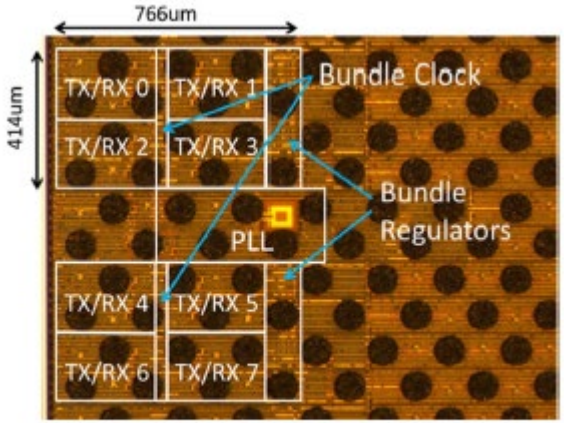
Claim 11	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 11	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 11	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

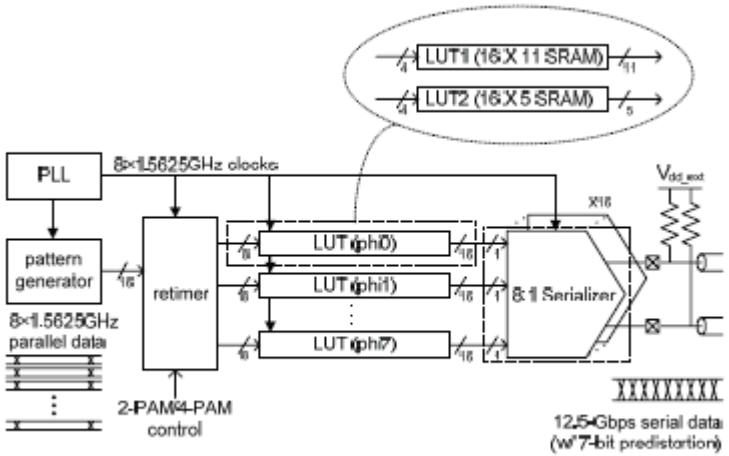
Claim 11	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 11	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 11	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

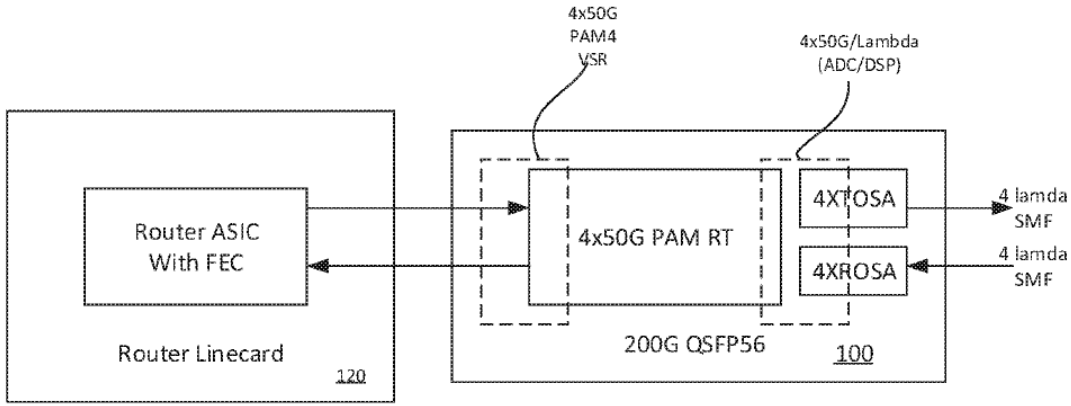
Claim 11	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13µm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

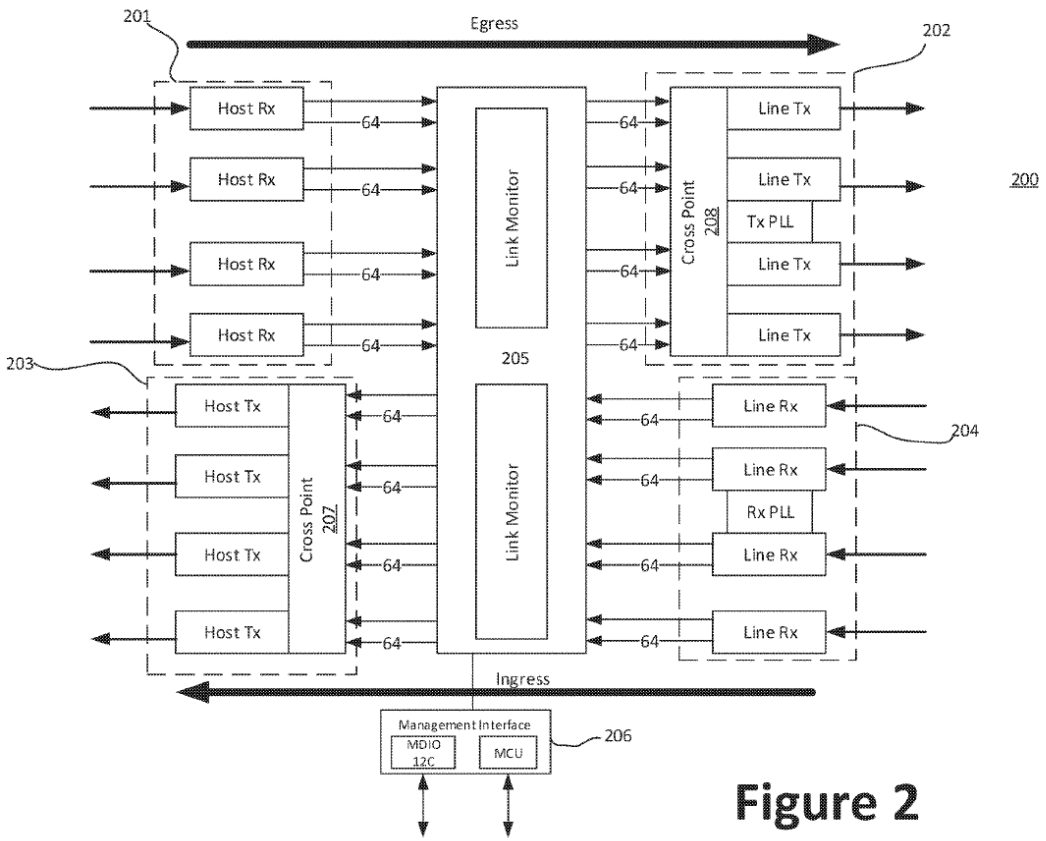
Claim 11	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 11	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 11	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 11	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 11	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 11	Disclosure
	 Riani, Figure 2.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 11	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 11	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 11	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 11	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 11	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 11	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 11	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 11	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 11	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 11	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 11	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 11	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 11	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 11	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 11	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

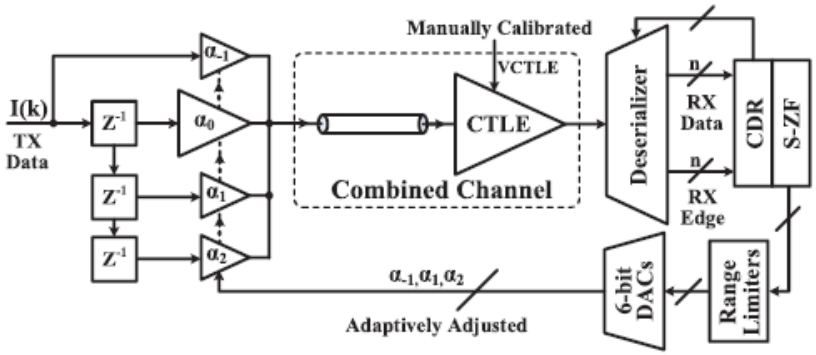


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 11	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 11	Disclosure

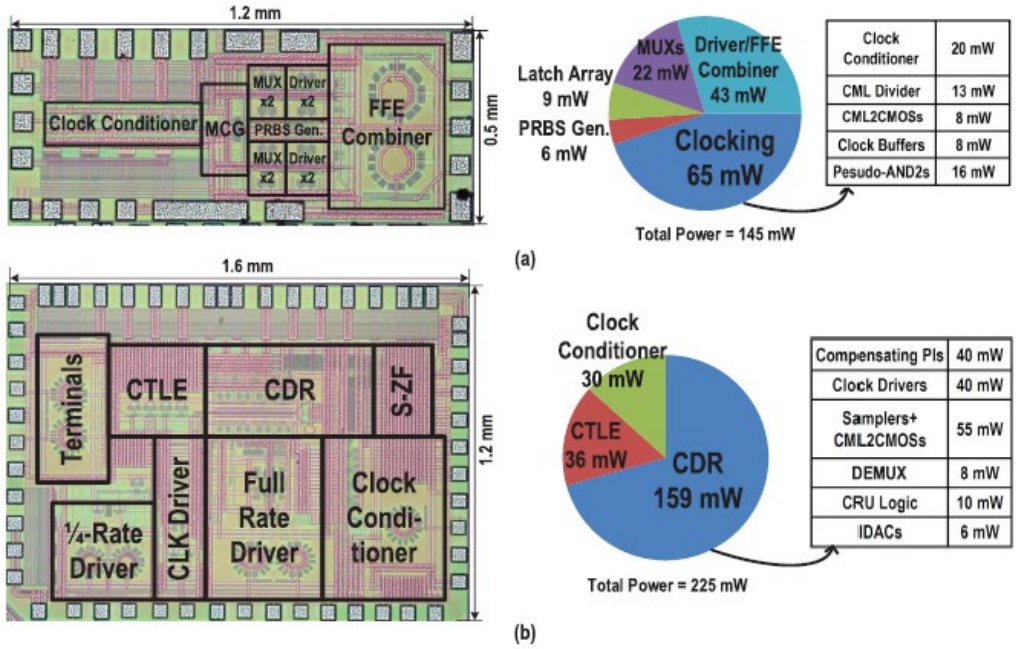


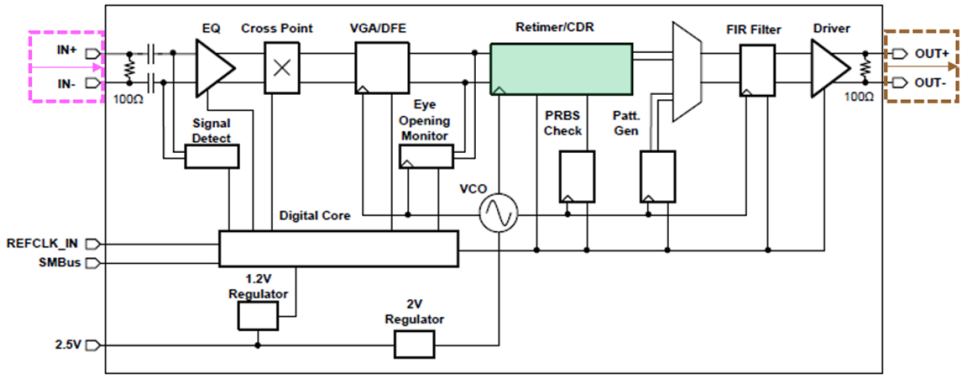
Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip.

Zheng, 2973.

Claim 11	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The active cable 3 receives the serial bit stream transmitted from the upstream device 2 in the upstream facing RX 30a in one retimer 30. The retimer 30 performs a waveform shaping on the serial bit stream received by the upstream facing RX 30a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 30b to the other retime 31. The retimer 31 receives the serial bit stream transmitted from the retimer 30 in the upstream facing RX 31a. The retimer 31 performs a waveform shaping on the serial bit stream received by the upstream facing RX 31a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 31b to the downstream device 4." Kobayashi, 3:5-19. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a

Claim 11	Disclosure
	TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver." Kobayashi, 4:4-9. "The exchange module 202 is configured to communicate capabilities information with a remote link partner including host loss information, RS-FEC ability information, and RS-FEC request information. The exchange module 202 may transmit local host loss information to the link partner and receive remote host loss information from the link partner. In some embodiments, the exchange module 202 may be included in or otherwise established by the autonegotiation module 104 and thus the capabilities information may be exchanged during execution of an autonegotiation protocol. In some embodiments, the exchange module 202 may be included in or otherwise established by the PMD/PMA module 106 and thus the capabilities information may be exchanged during a startup protocol performed by the PMD/PMA module 106." Lusted, paragraph 23. "The autonegotiation module 104 is configured to auto-negotiate line transmission speed, mode of operation, and other communication parameters with a link partner when the communication lane 102 is brought up. Additionally, in some embodiments the autonegotiation module 104 may be configured to exchange capabilities information with the link partner including host insertion loss information, RS-FEC ability information, and RS-FEC request information. The autonegotiation module 104 may encode the capabilities information, for example, in an autonegotiation base page or in a next page. Although illustrated in FIG. 1 as coupled between the PMD/PMA 106 and the communication lanes 102, in other embodiments the autonegotiation module 104 may be included at different positions in the Ethernet port logic 100. For example, in some embodiments the autonegotiation module 104 may be coupled between the PMD/PMA 106 and the FEC 108." Lusted, paragraph 17. "In view of the above transmission characteristics of twisted-pair, current Ethernet chips are usually equipped with preemphasis technique of a transmitting end and equalization technique of a receiving end

Claim 11	Disclosure
	to compensate the difference in transmission attenuation of physical layer signals on different frequencies on the same medium during Ethernet baseband transmission. Main functions of the preemphasis technique of the transmitting end and the equalization technique of the receiving end include: amplifying signals on different frequencies differently at the transmitting end to compensate different transmission attenuation in the twisted pair; applying the equalization technique to different frequency components in signals received at the receiving end to compensate the attenuation." Yu, paragraph 34. "An embodiment of the present invention provides an equalizer setting apparatus, which uses a filter circuit 101, an analog-to-digital converter 102, a digital memory 103, a digital comparator 104 and a first digital accumulator 105, the filter circuit 101, the analog-to-digital converter 102, the digital memory 103, the digital comparator 104 and the first digital accumulator 105 are connected in sequence, the output end of the equalizer 201 is connected with the input end of the filter circuit 101, the output end of the first digital accumulator 105 is connected with the set value input end of the equalizer 201, the output end of the analog-to-digital converter 102 is connected with the input end of the digital comparator 104, so that the problems that the setting value of the equalizer is accurately set in the prior art, which is time-consuming and labor-consuming are solved, the method has the advantages of achieving accurate setting of the set value of the equalizer in a single time, fast, simple, convenient, accurate and low-cost manner and saving labor force to a certain extent." Yin, paragraph 26 (English translation). *DS125DF1610 Retimer Publication* The DS125DF1610 retimer performs CDR for respective transit signals conveying transit data streams received from electrical conductors to generate output signals conveying outbound data streams that exit cable 10 to respective hosts, as shown in DS125DF1610 Fig. 2 below. For similar reasons to those discussed in claim limitation 1[c], an ordinarily skilled artisan understood that DS125DF1610's retimer remodulates the data as the outbound data after extracting the input signal's data and generating a newly-

Claim 11	Disclosure
	timed signal that is a "re-modulation" of the data.  **Figure 2. DS125DF1610 Simplified Data Path Diagram**
11[f] each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: `Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers.` CMIS, 1.

Claim 11	Disclosure
	1.4.4 MgmtInit State The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp. CMIS, 22.

Claim 11	Disclosure
	1.5.4 Control Set Overview A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 11	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 11	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 11	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 11	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))

The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 11	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value / Bit pattern / Output Amplitude 0 / 0000 / 100-400 mV (P-P) 1 / 0001 / 300-600 mV (P-P) 2 / 0010 / 400-800 mV (P-P) 3 / 0011 / 600-1200 mV (P-P) 4-14 / 0100-1110 / Reserved 15 / 1111 / Custom CMIS, 41.

Claim 11	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

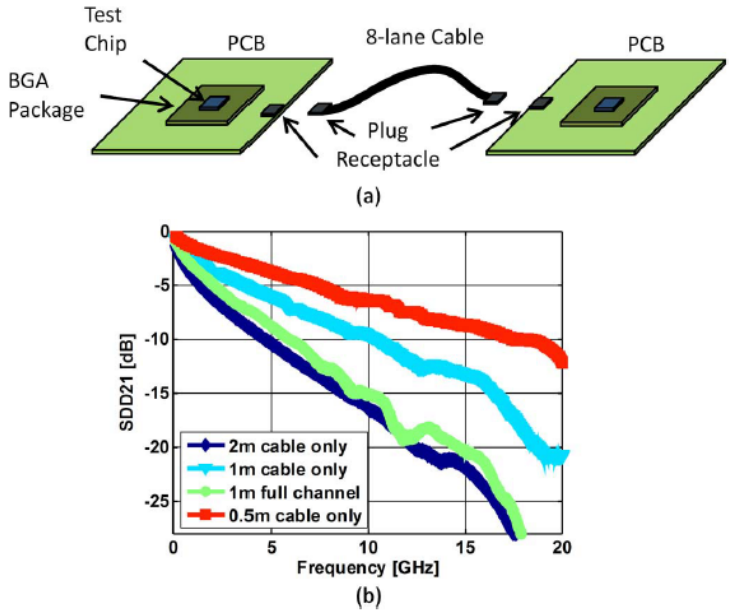
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

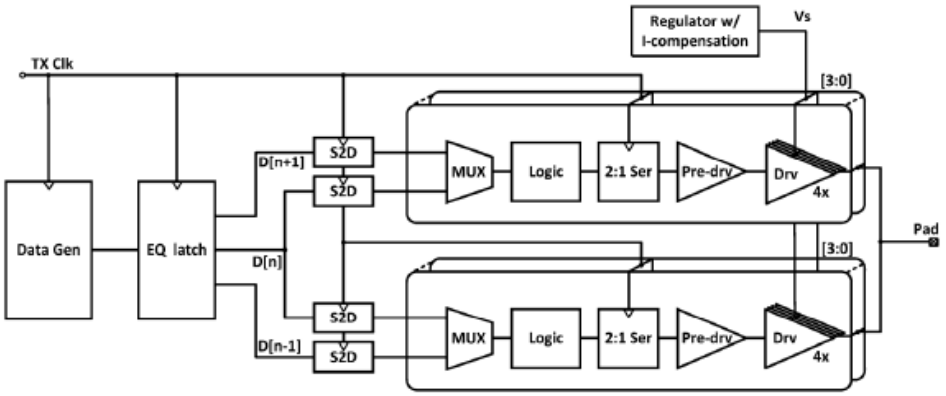
Claim 11	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

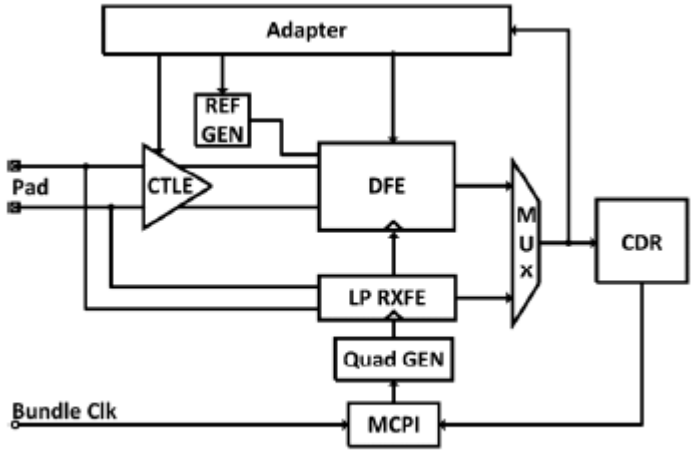
Claim 11	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 11	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 11	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

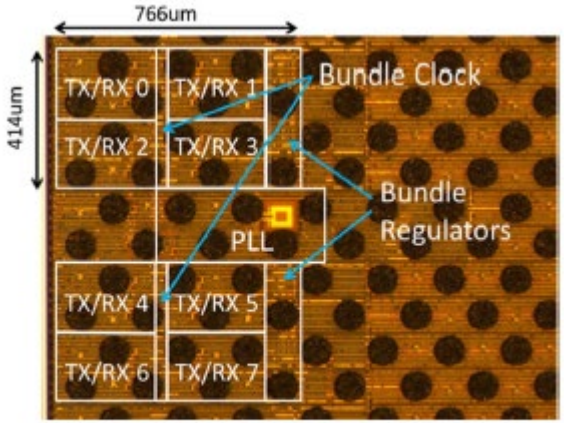
Claim 11	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 11	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 11	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

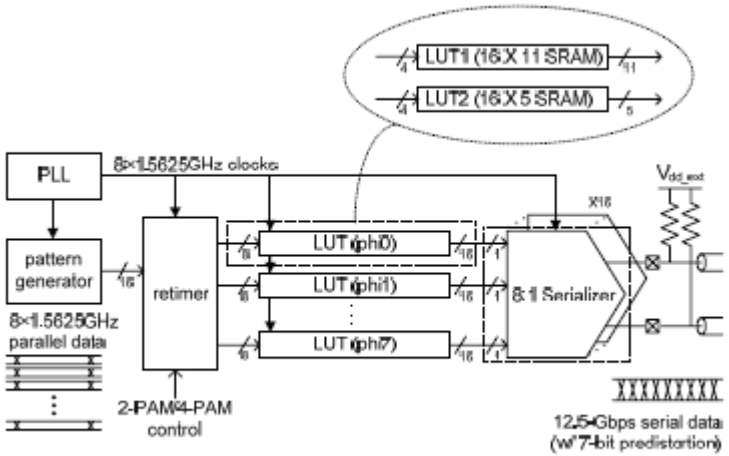
Claim 11	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 11	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 11	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

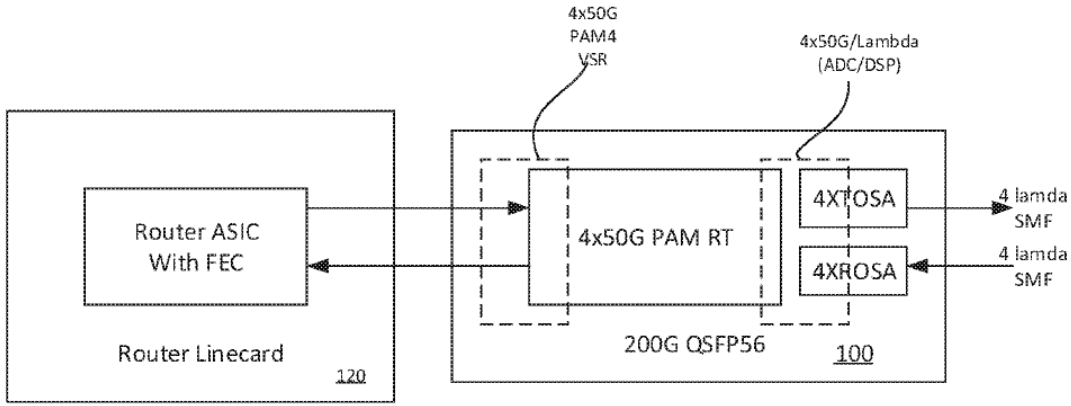
Claim 11	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13µm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

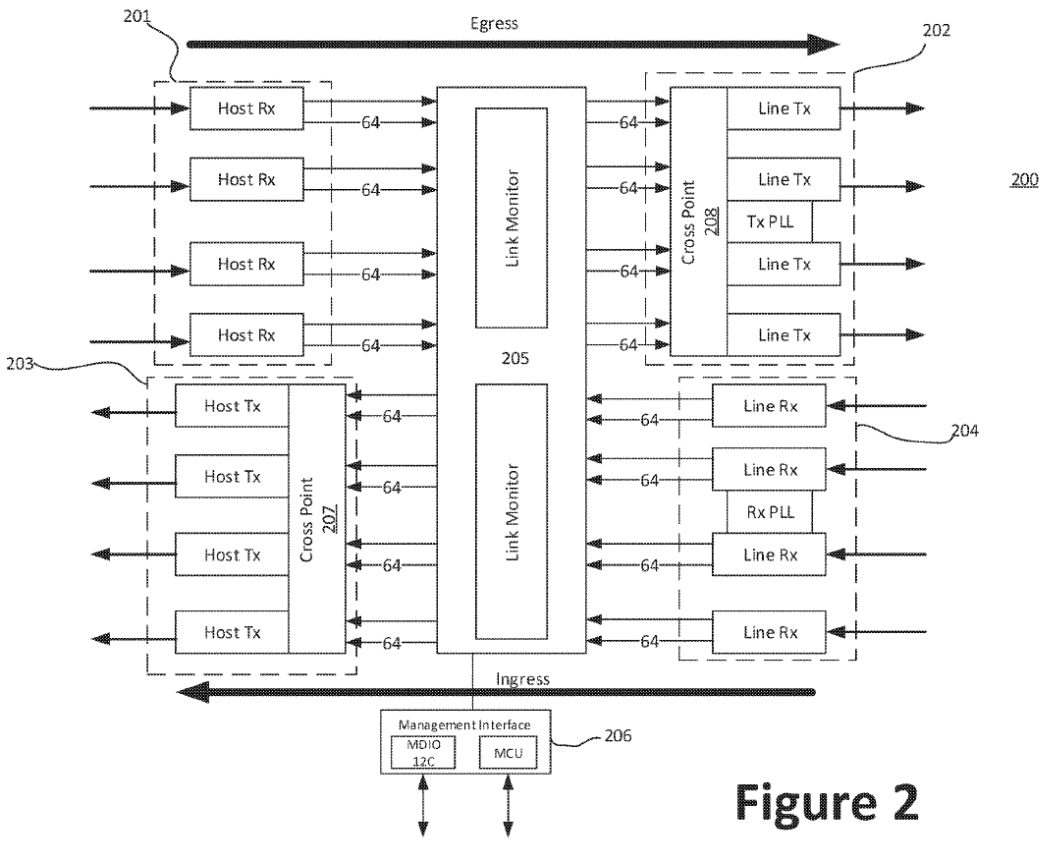
Claim 11	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 11	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 11	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 11	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 11	Disclosure
	 **Figure 1** Riani, Figure 1.

Claim 11	Disclosure
	 **Figure 2** Riani, Figure 2.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host system and a line system. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 1:45-52. It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, the re-timer module allows flexible implementation of high-speed communication network systems. For example, various fast communication protocols such as PAM-4 communication techniques is supported for optical communication networks. Re-timer modules according to embodiments of the present invention can be readily adopted into data centers and provide performance improvement and cost reduction. Riani, 3:3-13.

Claim 11	Disclosure
	The present invention is directed to data communication systems and techniques thereof. More specifically, embodiments of the present invention provide a retimer module that includes plurality of communication lanes for interfacing with a host and a line. The retimer module includes a link monitor and cross point sections. The retimer also includes a management interface module. There are other embodiments as well. Riani, 3:60-67.

Claim 11	Disclosure
	FIG. **1** is a simplified diagram illustrating a communication module **100** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Among other features, the communication module can be readily deployed at data centers that require 100 Gb/s or 200 Gb/s Ethernet. For data center applications, it is desirable to have optical modules that support 200 Gb/s and comply to the QSFP56 form factor, with lower cost and lower power compared to existing modules. To reduce the cost of the modules, efforts have been made to reduce the number of optical components by decreasing the number of wavelengths used to transmit data at 200 Gb/s, which requires advanced modulation techniques. Pulse amplitude modulation (PAM) is emerging as a preferred modulation technique for such application. For example, the "IN015050-CC02" module is a four-port duplex re-timer for PAM-4 signals between the line and host interfaces. The exemplary communication module illustrated in FIG. **1** is an application diagram of a QSFP56 module using the IN015050-CC02. The communication module **100** includes a transmitter interface (e.g., "4XTOSA") for transmitting four 50G data lanes and a receiver interface (e.g., "4XROSA") for receiving four 50G data lanes. Various DSP processes are performed for transmitted and received data. Communication module **100** interfaces with router line card **120** using four 50G PAM4 communication lanes. More detailed descriptions are provided below.

Claim 11	Disclosure
	Riani, 4:43-5:5. FIG. **2** is a simplified diagram illustrating a re-timer module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown in FIG. **2**, retimer module **200** includes host Rx section **201** and host Tx section **203** that interface with a host system (not shown). As respective names and arrows imply, host Rx section **201** receives data from the host system, and the host Tx section **203** transmits data to the host system. Retimer module **200** also includes line Tx section **202** and line Rx section **204**. For data transmitted from host system to line, a data path (i.e., egress data path) is formed by host Rx section **201** and line Tx section **202**, with link monitor section **205** in the middle. Riani, 5:6-20.

Claim 11	Disclosure
	It is to be appreciated that the retimer module **200** can be configured to operate in various modes and can support a wide variety of standards. For example, the following data rates (e.g., from 10.3 Gbps to 28.125 Gbps) are supported: 20.625 GBaud, 25.78125 GBaud, and 26.5625 GBaud PAM-4 10.3125 Gbit/s, 25.78125 Gbit/s or 26.5625 Gbit/s NRZ data 28.125 Gbps NRZ or 28.125 GBaud PAM-4 data The operation of retimer module **200** is in large part controlled by management interface **206**, which is coupled to link monitor **205**. As explained above, link monitor **205** is positioned between the host side sections (**201** and **203**) and line side sections (**202** and **204**), and it is configured to monitor the data traffic going through retimer module **200** to ensure proper operation. In various embodiments, link monitor **205** is configured to provide diagnostic functions and analyzes a specific type of diagnostic data. Management interface **206** comprises a management data input/output (MIDIO) interface and a microcontroller unit (MCU) as shown. In a specific implementation, retimer module **200** has 0.75, 1V and 1.95V (1.6V in non-EML mode) power supply rails. Riani, 5:57-6:12.

Claim 11	Disclosure
	In various embodiments, retimer module **200** works in conjunction with a storage unit, which may be implemented with an EEPROM device that is connected through an SPI interface. The EEPROM device stores the startup and DSP sequencing codes that are to be read by retimer module **200** at startup. This enables power up of the device independent from the power up of the entire module. It is to be appreciated that the initiation sequence automatically enables all the internal design blocks to their proper operating states. For example, many registers associated with the internal blocks do not have to be written externally through the MDIO/I2C interface. Riani, 6:25-36. Re-timer modules, as illustrated in FIG. **2**, include line side and host side. The line side includes line receivers. For example, the receiver module **204** in FIG. **2** includes four line side receivers. For example, four ADC/DSP-based line side receivers each operates at 28 Gbaud/s data rate. Each of the line receivers includes one or more equalizers. For example, an equalizer can be implemented as a combination of digital FFE and DFE. Line receivers may additionally incorporate automatic gain control loop to load the receiver ADC appropriately. Line receivers may also support eye monitor function on the receiver and slicer threshold adjust for each PAM4 level. Riani, 6:63-7:7.

Claim 11	Disclosure
	FIG. **3** is a simplified diagram illustrating a line receiver module according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The line receiver module **300** is implemented as a part of retimer module **200**, and it is configured on the line side for receiving optical signals. Receiver module **300** includes four receivers (shown as stacked receiver slices) for supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL is configured to serve four lanes. As an example, the high-speed analog front end (AFE) section of the data path consists of four lanes that each handles up to 56 Gbps of PAM-4 data. In various implementations, the AFE section comprises equalizer and variable gain amplifier (VGA), which are not shown in FIG. **3**. In a specific embodiment, the VGA is AC-coupled to the line signal via external capacitors and has about 50 ohms of internal resistance. The AFE includes a continuous time linear equalizer (CTLE) that is designed to provide high performance boost. For example, the auto gain control and CTLE functions can be configured to be auto-adaptive. An on-chip low dropout regulator is used to provide a regulated voltage to function blocks of the AFE. Riani, 7:15-39.

Claim 11	Disclosure
	FIG. **4** is a simplified diagram illustrating a line side transmitter module **400** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **400** is implemented as a component (e.g., section **202**) of retimer **200** illustrated in FIG. **2**. The transmitter module **400** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). A common PLL provides services all four lanes. The data path receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. In various embodiments, transmitter module **400** operates in quad-lambda mode at 28.125 GBd, transmitting data streams with PAM-4 modulation (56.25 Gb/s). Data are transmitted as optical signals. For example, the AFE block of transmitter module **400** includes an externally modulated laser for optical data transmission, and a single transmit PLL is shared among the four transmit lanes. For example, the four transmit lanes are shown in FIG. **4** as four slices. In addition to data transmission (i.e., from host Rx to line Tx), transmitter module **400** also operates in shallow line loopback mode (e.g., operating at PAM-4 to PAM-4). Riani, 8:37-60.

Claim 11	Disclosure
	The PAM-4 encoding/Gray coding block follows the error injection block. For example, at this block, Gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swapping, and/or other coding processes may be performed. Next, Tx DSP block performs various DSP processes on the encoded data. At the AFE block, data are converted to optical signal for transmission. If the transmitter module **400** is operating in a testing mode, test patterns from the test pattern memory block (instead of actual data) are transmitted. Riani, 9:38-47.

Claim 11	Disclosure
	FIG. **6** is a simplified block diagram illustrating a transmitter at the host side transmitter module **600** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, transmitter module **600** is implemented as a component (e.g., section **203**) of retimer **200** illustrated in FIG. **2**. The transmitter module **600** includes a quad lane transmitter supporting data streams of up to 28.125 GBd with PAM-4 modulation (56.25 Gb/s). Four PLLs service the 8 transmit lanes allowing for 4 independent output frequencies. The data path receives up to 8 lanes of NRZ data or 4 lanes of PAM-4 data from the core and prepares them for transmission. The cross point **601** supports the receive data streams to be transmitted on any of host transmit lanes. The received data are first processed by the FIFO buffer as shown. In various embodiments, the AM framer supports 25GE, 50GE, 100GE, 200GE and 400GE protocols. The AM framer provides protocol lock status. Data are encoded for transmission using PAM-4 communication protocol. For example, PAM-4 encoding block provides processes for polarity inversion, PAM-4 encoding, and PAM-4 MSB/LSB swap. The transmitter module **600** further provides squelch control. The pattern generator block generates test patterns for each communication. The pattern generator logic supports PRSB58/31/23/16/15/13/11/9/7, PRBS13Q, SSPRQ, and/or other formats. For example, PRBS can be generated independently on PAM-4 MSBs and LSBs. In a specific embodiment, 2×63 bit programmable-repeatable fixed patterns are used. Square wave, JP03A, JP03B, transmitter linearity test patterns, and CID jitter tolerance pattern can be used as well. The test pattern memory can be configured in a binary mode, which provides up to 32,768 bits for four transmitter lanes, and each transmitter can have a unique pattern with identical lengths. The test pattern memory can operate in linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. The host side transmitter module **600** may additionally include features such as error injection and continuous identical symbol detector. Riani, 11:4-45.

Claim 11	Disclosure
	It is to be appreciated that embodiments of the present invention implemented in various ways. For example, re-timers according to embodiments of the present invention operate in low power and are compatible with PAM communication protocols. In various implementations, re-timer form factors are suitable for QSFP56 200G modules. Certain re-timers implement PAM-4 electrical outputs and includes an integrated EML driver. Re-timers can support both 56.25 Gb/s data streams with PAM-4 modulation and 28.125 Gb/s data streams with NRZ modulation. Lane-based diagnostic link monitor can be implemented to analyze receive error statistics and estimate BER. Riani, 12:19-30.

Claim 11	Disclosure
	***Abstract*—This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.** ***Index Terms*—4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.** Zheng, 2963.

Claim 11	Disclosure
	To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feed-forward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper. Zheng, 2964.

Claim 11	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 11	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 11	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 11	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

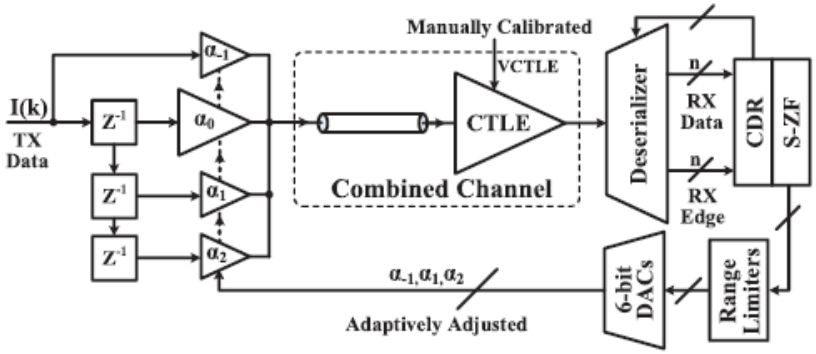


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 11	Disclosure
	Zheng, 2970. The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micrographs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits). Zheng, 2972.

Claim 11	Disclosure

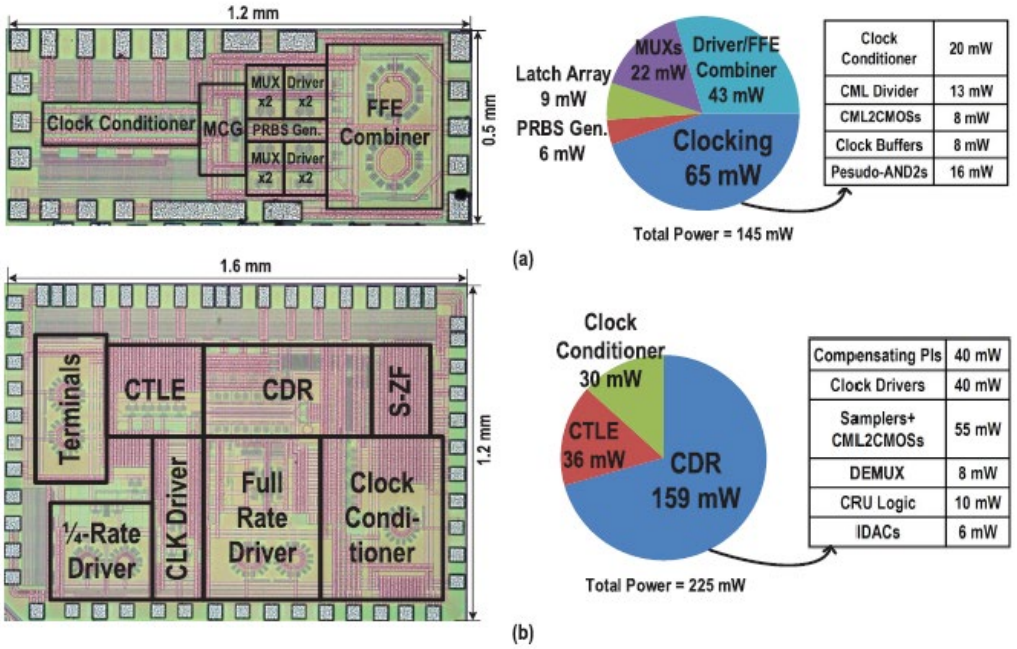


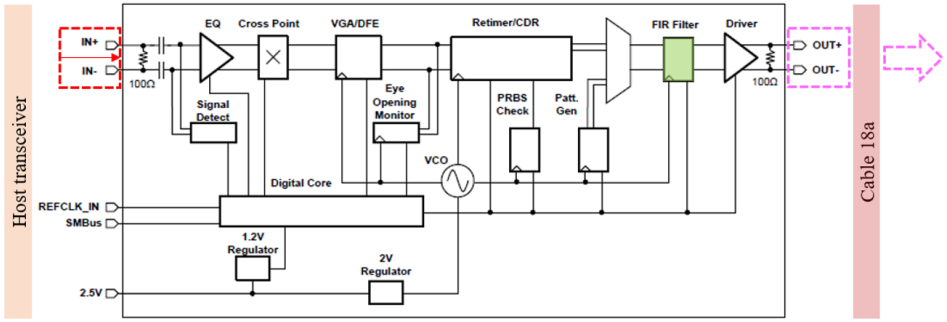
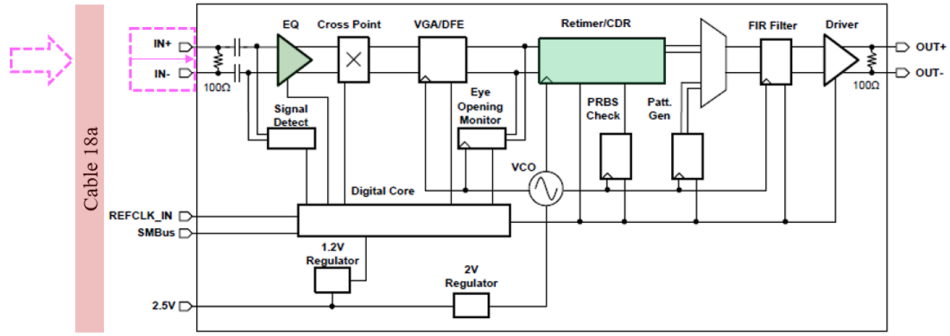
Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip.

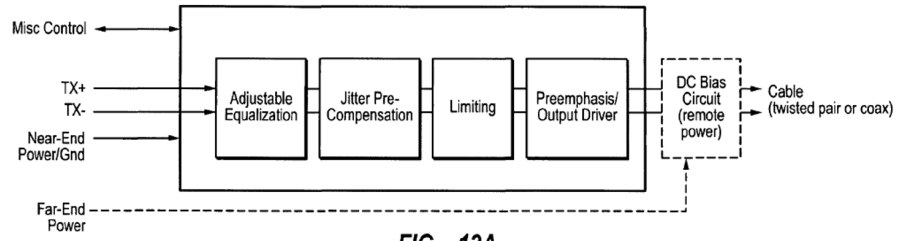
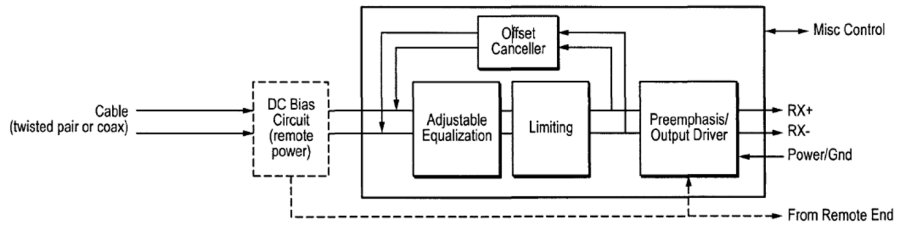
Zheng, 2973.

Claim 11	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The active cable 3 receives the serial bit stream transmitted from the upstream device 2 in the upstream facing RX 30a in one retimer 30. The retimer 30 performs a waveform shaping on the serial bit stream received by the upstream facing RX 30a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 30b to the other retime 31. The retimer 31 receives the serial bit stream transmitted from the retimer 30 in the upstream facing RX 31a. The retimer 31 performs a waveform shaping on the serial bit stream received by the upstream facing RX 31a and retimes the serial bit stream after being waveform-shaped and transmits the serial bit stream from the downstream facing TX 31b to the downstream device 4." Kobayashi, 3:5-19. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a

Claim 11	Disclosure
	TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver." Kobayashi, 4:4-9. "The exchange module 202 is configured to communicate capabilities information with a remote link partner including host loss information, RS-FEC ability information, and RS-FEC request information. The exchange module 202 may transmit local host loss information to the link partner and receive remote host loss information from the link partner. In some embodiments, the exchange module 202 may be included in or otherwise established by the autonegotiation module 104 and thus the capabilities information may be exchanged during execution of an autonegotiation protocol. In some embodiments, the exchange module 202 may be included in or otherwise established by the PMD/PMA module 106 and thus the capabilities information may be exchanged during a startup protocol performed by the PMD/PMA module 106." Lusted, paragraph 23. "The autonegotiation module 104 is configured to auto-negotiate line transmission speed, mode of operation, and other communication parameters with a link partner when the communication lane 102 is brought up. Additionally, in some embodiments the autonegotiation module 104 may be configured to exchange capabilities information with the link partner including host insertion loss information, RS-FEC ability information, and RS-FEC request information. The autonegotiation module 104 may encode the capabilities information, for example, in an autonegotiation base page or in a next page. Although illustrated in FIG. 1 as coupled between the PMD/PMA 106 and the communication lanes 102, in other embodiments the autonegotiation module 104 may be included at different positions in the Ethernet port logic 100. For example, in some embodiments the autonegotiation module 104 may be coupled between the PMD/PMA 106 and the FEC 108." Lusted, paragraph 17. "In view of the above transmission characteristics of twisted-pair, current Ethernet chips are usually equipped with preemphasis technique of a transmitting end and equalization technique of a receiving end

Claim 11	Disclosure
	to compensate the difference in transmission attenuation of physical layer signals on different frequencies on the same medium during Ethernet baseband transmission. Main functions of the preemphasis technique of the transmitting end and the equalization technique of the receiving end include: amplifying signals on different frequencies differently at the transmitting end to compensate different transmission attenuation in the twisted pair; applying the equalization technique to different frequency components in signals received at the receiving end to compensate the attenuation." Yu, paragraph 34. "An embodiment of the present invention provides an equalizer setting apparatus, which uses a filter circuit 101, an analog-to-digital converter 102, a digital memory 103, a digital comparator 104 and a first digital accumulator 105, the filter circuit 101, the analog-to-digital converter 102, the digital memory 103, the digital comparator 104 and the first digital accumulator 105 are connected in sequence, the output end of the equalizer 201 is connected with the input end of the filter circuit 101, the output end of the first digital accumulator 105 is connected with the set value input end of the equalizer 201, the output end of the analog-to-digital converter 102 is connected with the input end of the digital comparator 104, so that the problems that the setting value of the equalizer is accurately set in the prior art, which is time-consuming and labor-consuming are solved, the method has the advantages of achieving accurate setting of the set value of the equalizer in a single time, fast, simple, convenient, accurate and low-cost manner and saving labor force to a certain extent." Yin, paragraph 26 (English translation). *DS125DF1610 Retimer Publication* The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610's FIR filter) and the CDR performed on the electrical input signal (by the DS125DF1610's EQ). DS125DF1610's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top) and the other showing the retimer processing the transit signal

Claim 11	Disclosure
	received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See id.* at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit signal."  Figure 2. DS125DF1610 Simplified Data Path Diagram  Figure 2. DS125DF1610 Simplified Data Path Diagram

Claim 11	Disclosure
	U.S. Patent No. 7,762,727 to Aronson Aronson discloses an active cable for high-speed transmissions between network nodes. See, e.g., Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.  *FIG. 12A*  *FIG. 12B* Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side]

Claim 11	Disclosure
	PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23. Aronson discloses the host-side equalization and pre-equalization use fixed cable-independent parameters to address host-side losses. *See, e.g.*, Aronson at 12:10-17, 14:16-23, 15:17-24. "Fixed" parameters reduced complexity and manufacturing costs. See, e.g., U.S. Patent No. 7,239,665 at 1:7-18 (discussing slow convergence with adaptive equalization); U.S. Patent App. Pub. No. 2011/0228821 at [0009]-[0011] (discussing tradeoffs between fixed and adaptive equalization); U.S. Patent No. 6,621,862 at 1:52-55 (large gate count for adaptive equalization can cause "high chip costs"); U.S. Patent App. Pub. No. 2006/0045176 at [0034] ("The adaptive equalizer can be trapped in a failure state (i.e., incorrect state) and not able to recover from the failure state."); U.S. Patent App. Pub. No. 2017/0187463 at [0058] ("[E]qualization techniques… come with different engineering tradeoffs, including trade-offs in power consumption, performance, and/or cost."). **5. The PCIe 3.0 Equalization Adaptation Protocol** The PCIe 3.0 Base Specification [10] requires that a compliant Tx be able to produce any of the output equalization (TxEQ) levels shown in Figure 21, whenever requested to do so by the receiving port, during link equalization training. The same specification describes a protocol of TxEQ adaptation, where the host (upstream agent) or the end device (downstream agent) can each request that any of the TxEQ values in Figure 21 be presented to them by the other agent on the link. The intent of adaptation is to allow both agents to adjust the link partner's TxEQ to an optimal value for their receiver, and for the specific channel and operating conditions at hand. Samaan, p. 24.

L. DEPENDENT CLAIM 12

Claim 12	Disclosure
12[a] The cable manufacturing method of claim 11, wherein the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp.

Claim 12	Disclosure
	CMIS, 22. **1.5.4 Control Set Overview** A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 12	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 12	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 12	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 12	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 12	Disclosure

The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows:

Table 14- Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000	100-400 mV (P-P)
1	0001	300-600 mV (P-P)
2	0010	400-800 mV (P-P)
3	0011	600-1200 mV (P-P)
4-14	0100-1110	Reserved
15	1111	Custom

CMIS, 41.

Claim 12	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

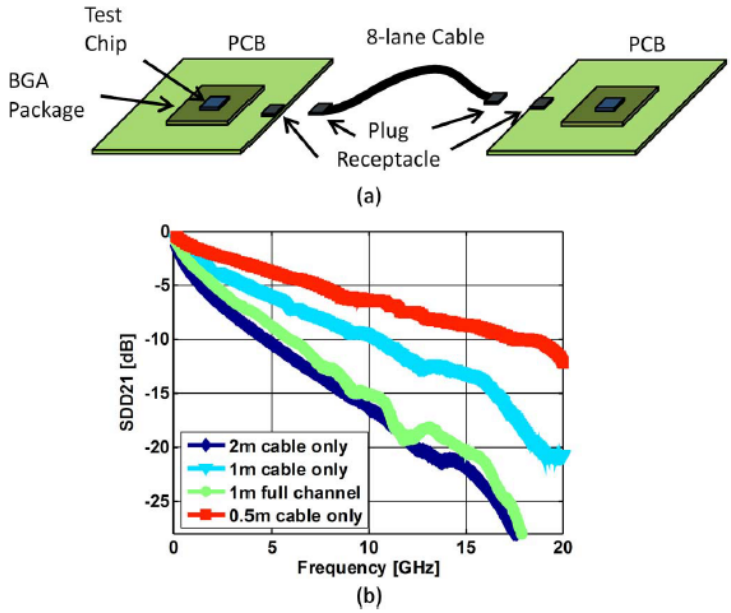
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

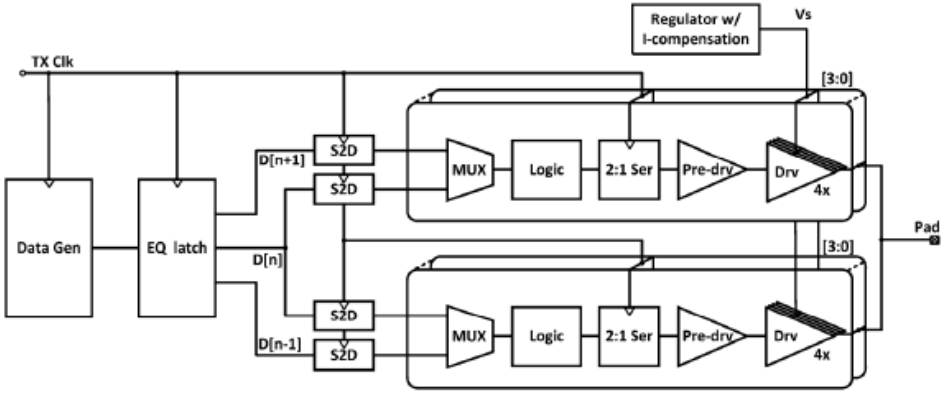
Claim 12	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

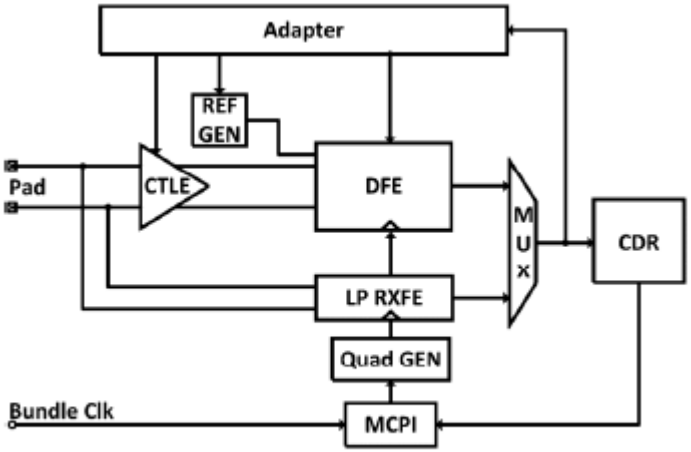
Claim 12	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 12	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 12	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

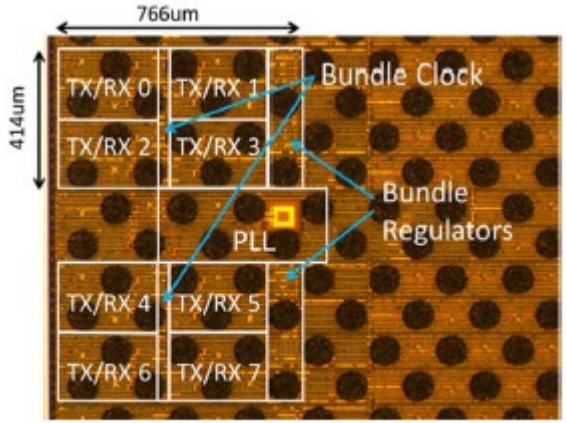
Claim 12	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 12	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 12	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

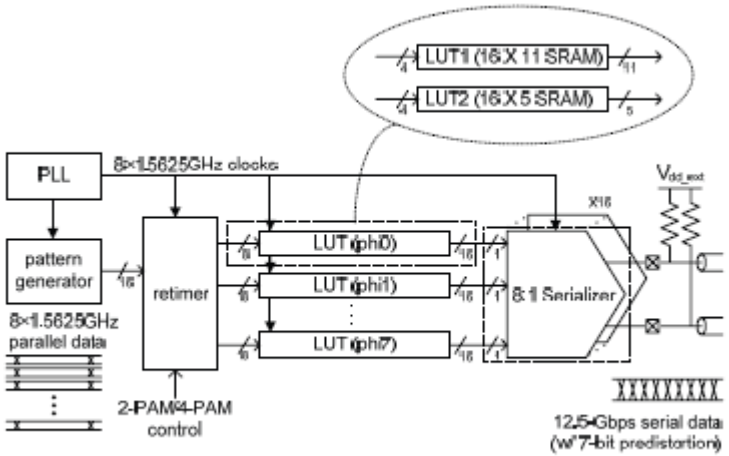
Claim 12	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 12	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 12	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 12	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 12	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 12	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 12	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 12	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 12	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 12	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 12	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 12	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 12	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 12	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 12	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 12	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 12	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 12	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

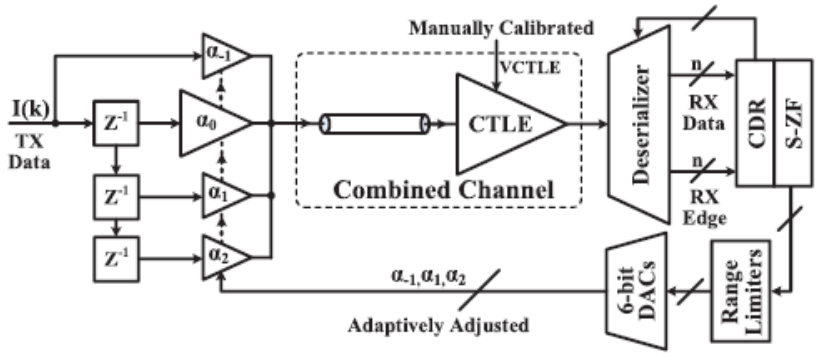
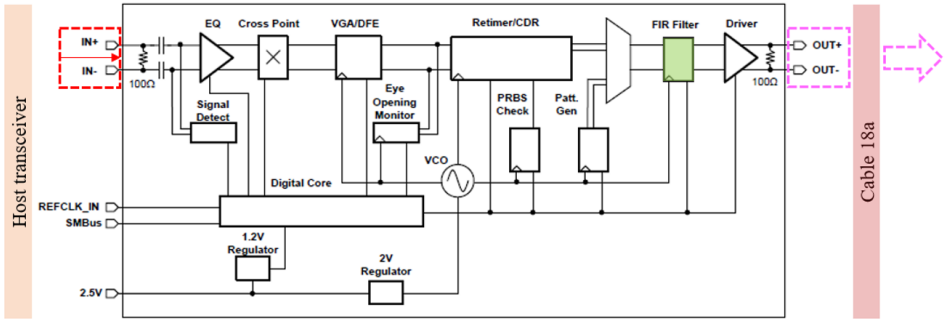
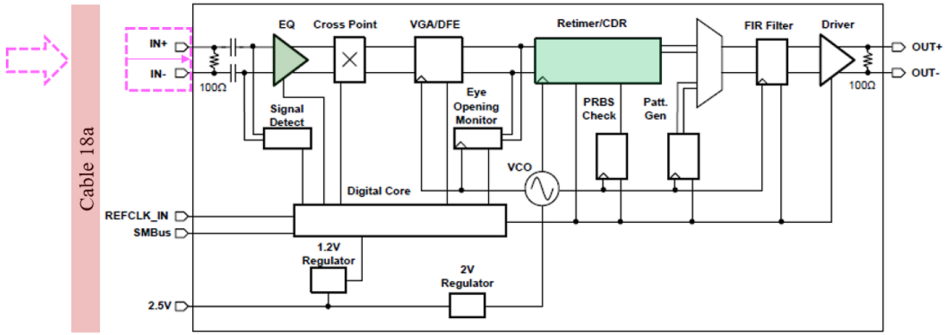


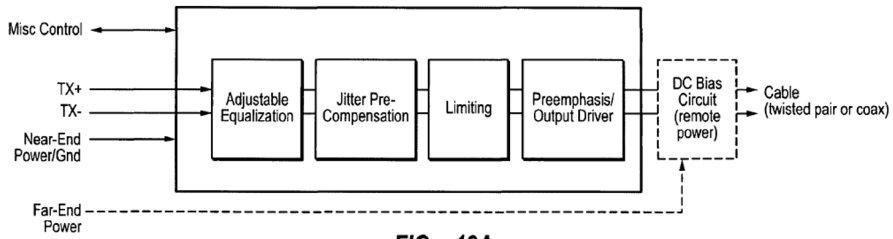
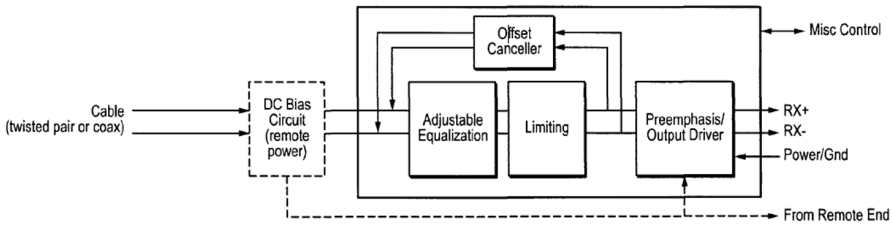
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

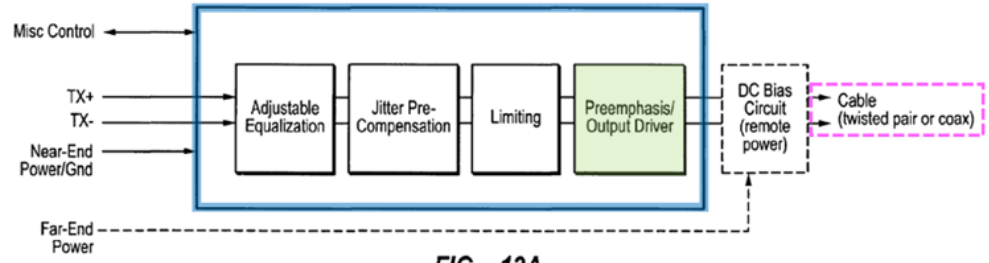
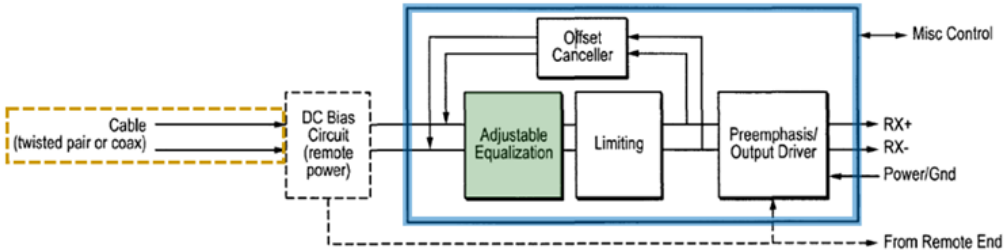
Claim 12	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 12	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50 itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK"

Claim 12	Disclosure
	Kobayashi, 4:4-22. **“**The link activation module 204 is configured to determine a total insertion loss for the connection with the remote host based on the local host loss, the remote host loss, and cable loss. The link activation module 204 compares the total insertion loss to a FEC limit and to a specification limit. The link activation module 204 may bring up the communication link with the link partner without FEC enabled if the total insertion loss is below the specification limit and below the FEC limit. Additionally, the link activation module 204 may bring up the communication link with the link partner with FEC enabled if the total insertion loss is below the specification limit but not below the FEC limit. Further, the link activation module 204 may not bring up the communication link with the link partner if the total insertion loss is not below the specification limit (e.g., the link activation module 204 may keep the communication link down or bring the communication link down).” Lusted, paragraph 24. “The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage.” Ikeda, 7:44-55. <u>*DS125DF1610 Retimer Publication*</u> The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610’s FIR filter) and the CDR performed on the electrical input signal (by the DS125DF1610’s EQ). DS125DF1610’s Figure 2 is annotated twice below – once to show the retimer processing the transit signal

Claim 12	Disclosure
	for transmission over the cable (top) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See id.* at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit signal."  Figure 2. DS125DF1610 Simplified Data Path Diagram  Figure 2. DS125DF1610 Simplified Data Path Diagram

Claim 12	Disclosure
	U.S. Patent No. 7,762,727 to Aronson Aronson discloses an active cable for high-speed transmissions between network nodes. See, e.g., Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.  *FIG. 12A*  *FIG. 12B* Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it

Claim 12	Disclosure
	receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23. Using "cable dependent" parameters for equalization would have been the conventional and obvious way to address losses over the cable. *See, e.g.*, Aronson at 14:33-43 (pre-emphasis/output driver performs pre-equalization to overcome "loss on the cable" using cable-dependent parameters that "match the particular length [and/or] the characteristics of the copper cabling"), Fig. 12A (below).  *FIG. 12A* Using "cable dependent" parameters for equalization would have been the conventional and obvious way to address losses over the cable. Aronson at 15:1-8 (equalization "compensate[s] for the cable" losses using cable dependent parameters based on "cable length and characteristics"), Fig. 12B (below).  *FIG. 12B*

Claim 12	Disclosure
12[b] for clock and data recovery on the second and first electrical transit signals.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1.

Claim 12	Disclosure
	1.4.4 MgmtInit State The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp. CMIS, 22.

Claim 12	Disclosure
	1.5.4 Control Set Overview A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 12	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 12	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 12	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 12	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 12	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 12	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

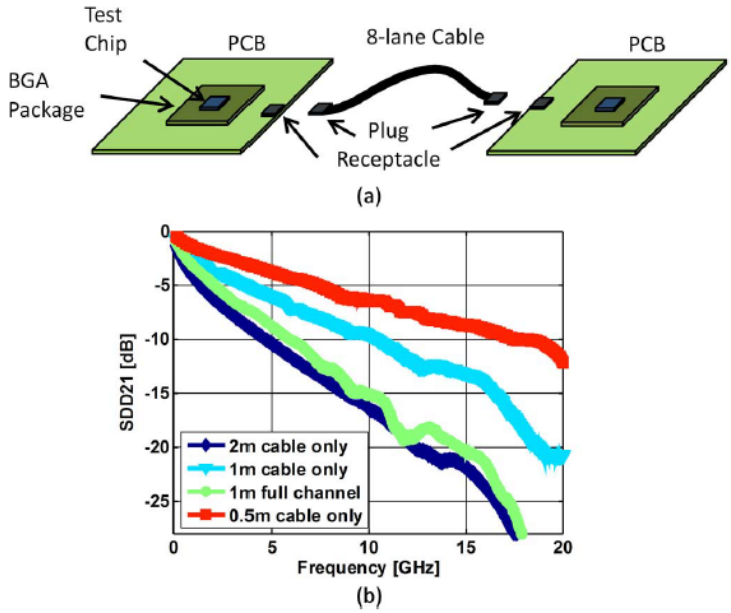
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

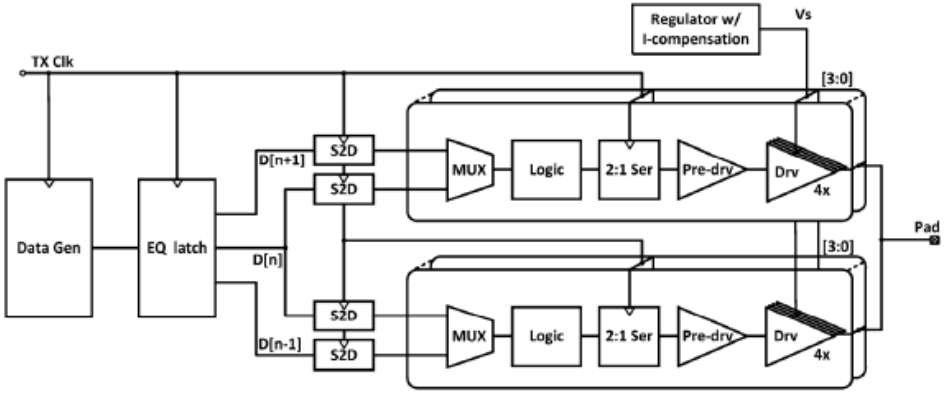
Claim 12	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

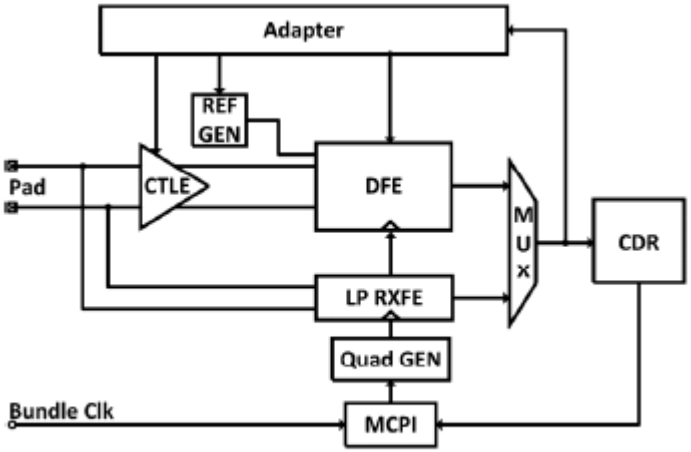
Claim 12	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 12	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 12	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

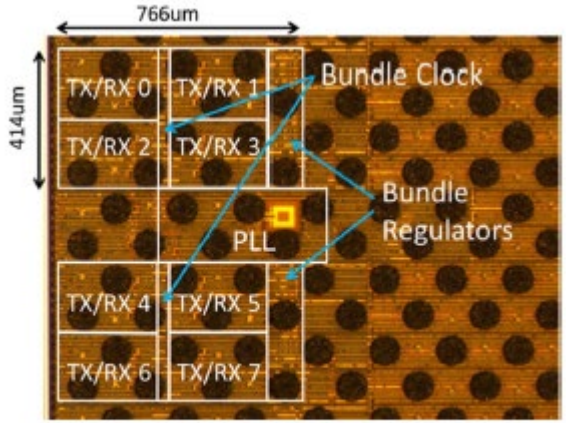
Claim 12	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 12	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 12	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

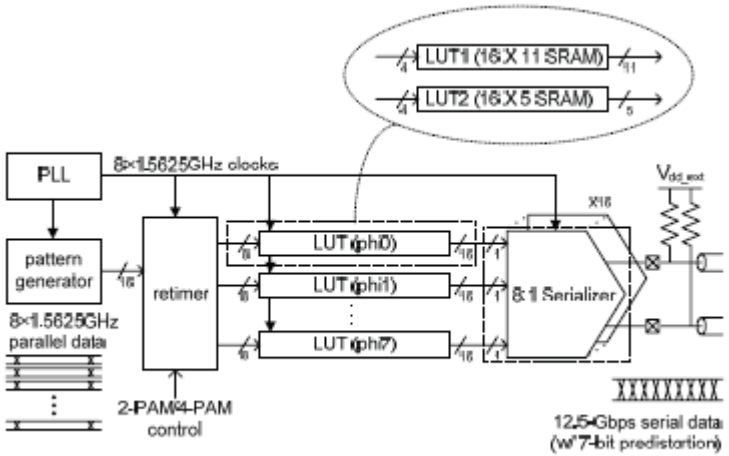
Claim 12	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 12	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 12	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 12	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 12	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 12	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 12	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 12	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 12	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 12	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 12	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 12	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 12	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 12	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 12	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 12	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 12	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 12	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

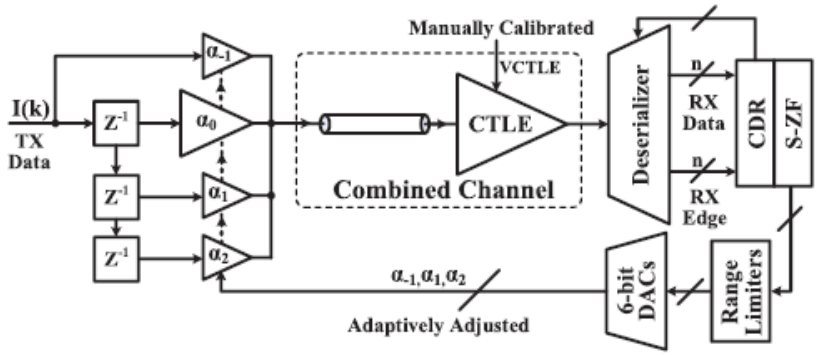
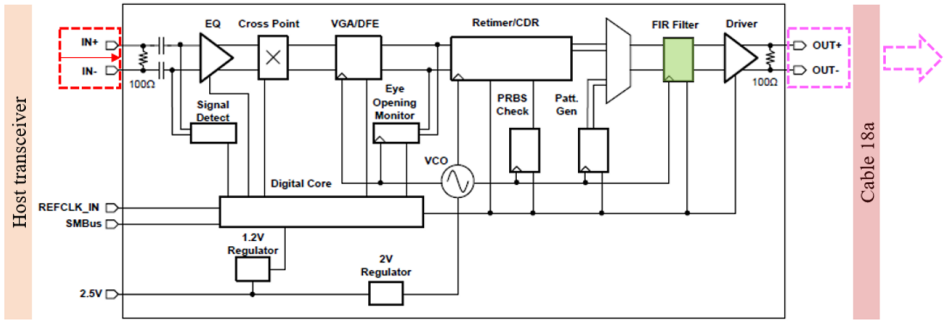


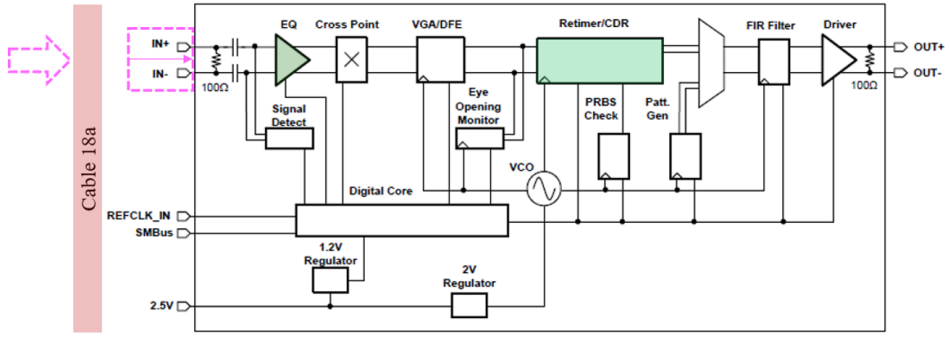
Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

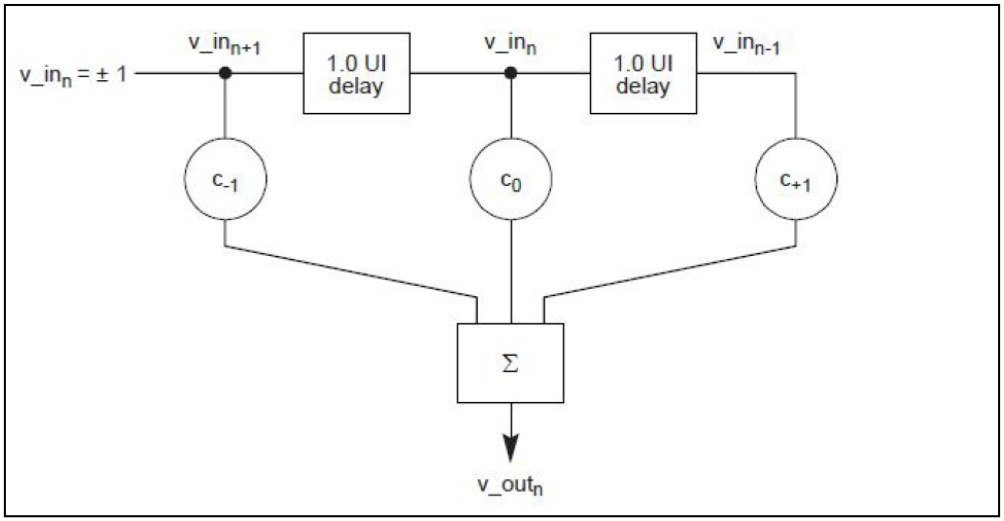
Claim 12	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 12	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "As shown in FIG. 2, the retimer 50 includes an upstream facing RX 51, a downstream facing TX 52, a TX serial bit rate generator 53, a FIFO 54, a link training sequence pattern generator 55, and a selection circuit 56. The upstream facing RX 51 includes an equalizer, a CDR, and a de-serializer. The downstream facing TX 52 includes a serializer and a driver. The upstream facing RX 51 generates a parallel word (10 bits, for example), a recovered parallel clock, and an incoming link training sequence marker (IN_LT_SEQ_MARK) based on the serial bit stream transmitted from the upstream TX and outputs them. The TX serial bit rate generator 53 generates a serial bit clock and a parallel word clock based on a local timing reference 60 (a type of reference clock) generated in the retimer 50 and outputs them. The TX serial bit rate generator 53 also generates a training sequence marker (SELF_LT_SEQ_MARK) of the retimer 50

Claim 12	Disclosure
	itself and outputs it. The SELF_LT_SEQ_MARK is synchronized with the IN_LT_SEQ_MARK" Kobayashi, 4:4-22. **"**The link activation module 204 is configured to determine a total insertion loss for the connection with the remote host based on the local host loss, the remote host loss, and cable loss. The link activation module 204 compares the total insertion loss to a FEC limit and to a specification limit. The link activation module 204 may bring up the communication link with the link partner without FEC enabled if the total insertion loss is below the specification limit and below the FEC limit. Additionally, the link activation module 204 may bring up the communication link with the link partner with FEC enabled if the total insertion loss is below the specification limit but not below the FEC limit. Further, the link activation module 204 may not bring up the communication link with the link partner if the total insertion loss is not below the specification limit (e.g., the link activation module 204 may keep the communication link down or bring the communication link down)." Lusted, paragraph 24. "The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage." Ikeda, 7:44-55. *DS125DF1610 Retimer Publication* The transceivers of the DS125DF1610 each employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data stream for transit (by the DS125DF1610's FIR filter) and the

Claim 12	Disclosure
	CDR performed on the electrical input signal (by the DS125DF1610's EQ). DS125DF1610's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. *See, e.g.*, DS125DF1610 at §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. *See id.* at DS125DF1610, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "employing … equalization parameters for … the remodulation of the inbound data stream for transit, and the [CDR] performed on the electrical transit signal."  **Figure 2. DS125DF1610 Simplified Data Path Diagram**

Claim 12	Disclosure
	 Figure 2. DS125DF1610 Simplified Data Path Diagram

Claim 12	Disclosure
	 **Figure 22 The PCIe 3.0 Tx Equalization FIR filter representation. (Note: The 10G-KR Filter is similar in definition).** This PCIe 3.0 TxEQ adaptation [10] protocol has 4 phases, defined as follows:- Samaan, p. 25.

M. DEPENDENT CLAIM 13

Claim 13	Disclosure
13. The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp.

Claim 13	Disclosure
	CMIS, 22. **1.5.4 Control Set Overview** A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 13	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 13	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 13	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 13	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 13	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 13	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

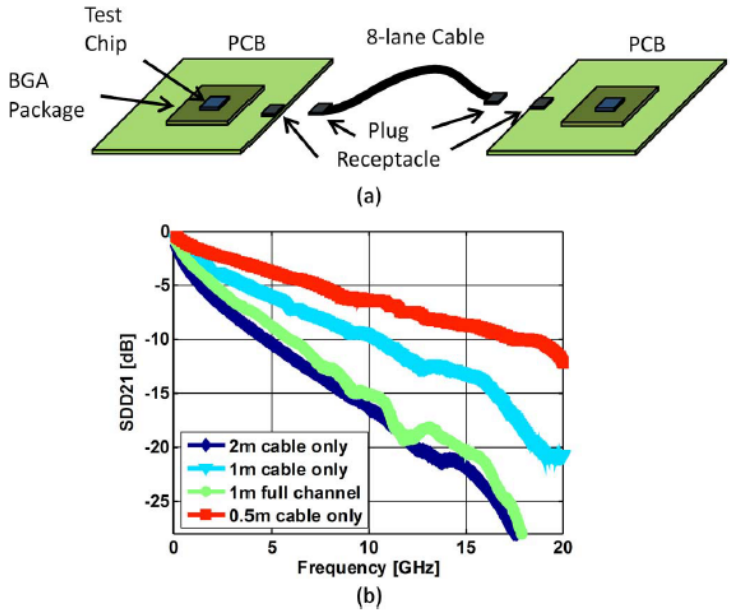
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

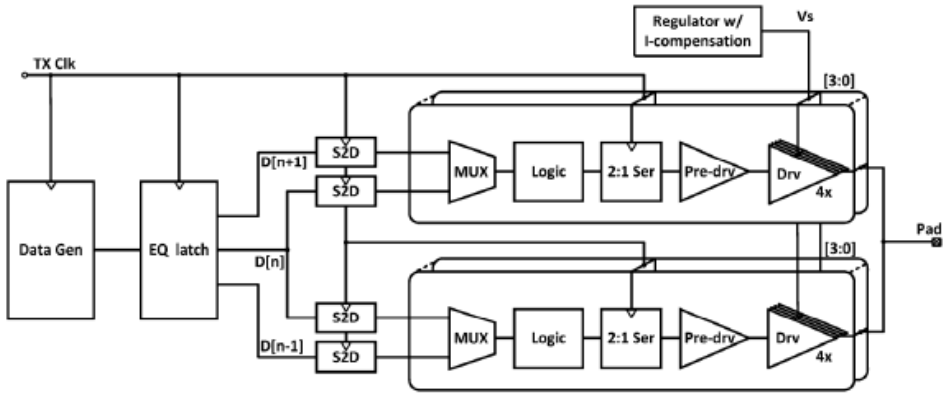
Claim 13	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

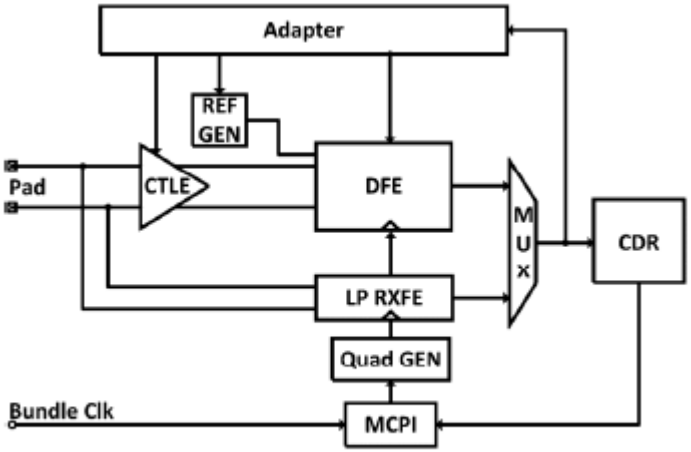
Claim 13	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 13	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 13	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

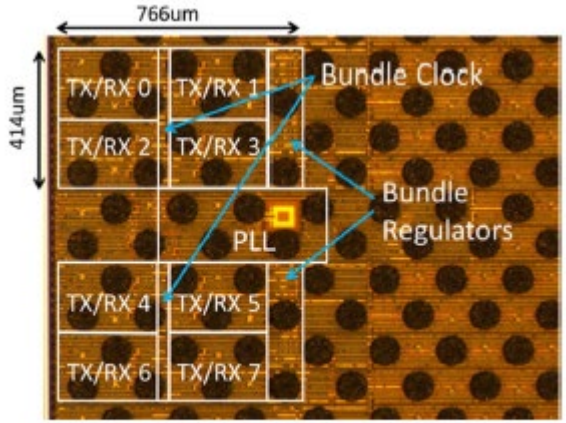
Claim 13	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 13	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 13	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

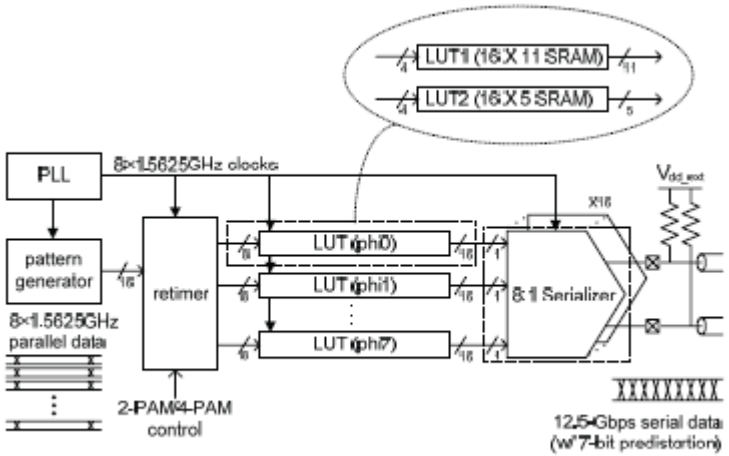
Claim 13	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 13	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 13	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 13	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 13	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 13	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 13	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 13	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 13	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 13	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 13	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 13	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 13	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 13	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 13	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 13	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 13	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 13	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

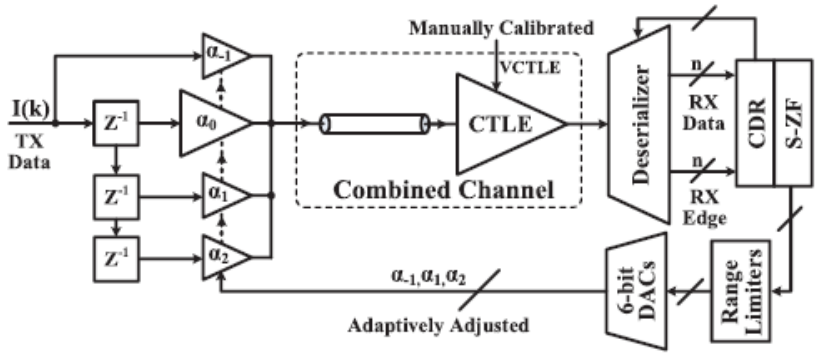
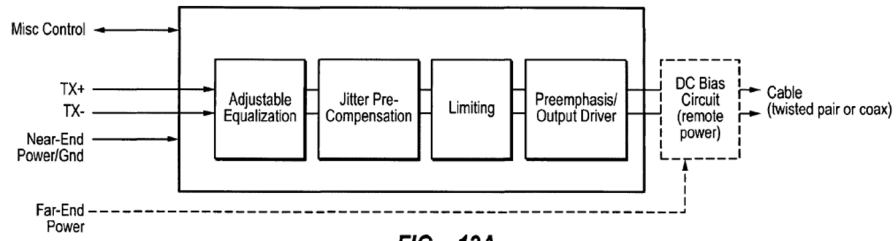
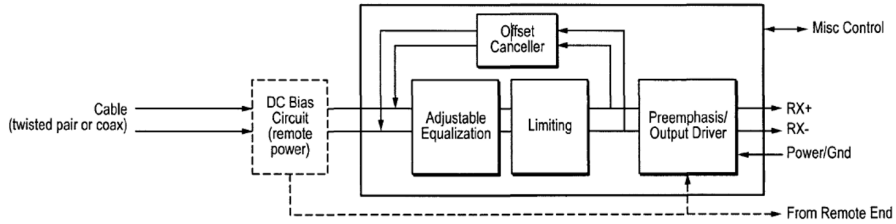
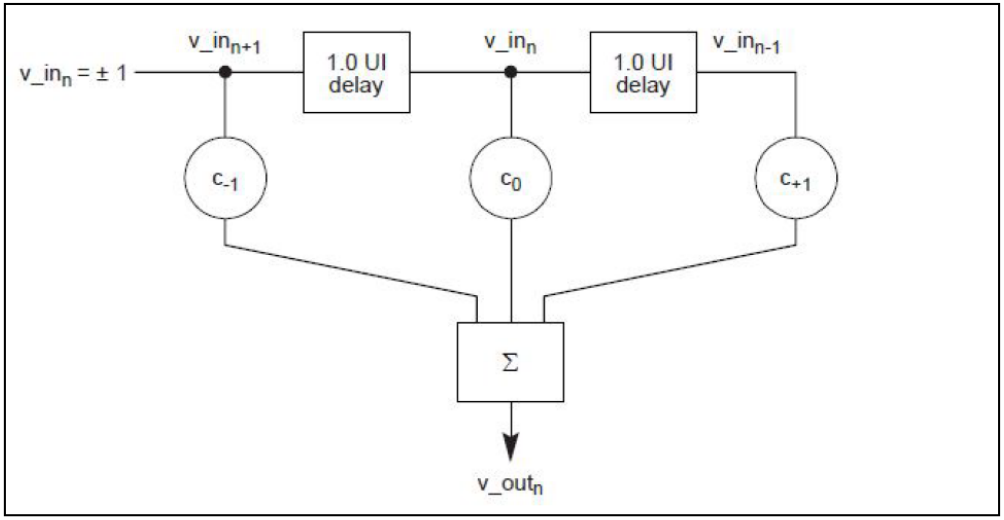


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 13	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 13	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage." Ikeda, 7:44-55.

Claim 13	Disclosure
	U.S. Patent No. 7,762,727 to Aronson Aronson discloses an active cable for high-speed transmissions between network nodes. See, e.g., Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.  *FIG. 12A*  *FIG. 12B* Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23.

Claim 13	Disclosure
	 **Figure 22 The PCIe 3.0 Tx Equalization FIR filter representation. (Note: The 10G-KR Filter is similar in definition).** This PCIe 3.0 TxEQ adaptation [10] protocol has 4 phases, defined as follows:- Samaan, p. 25.

N. DEPENDENT CLAIM 14

Claim 14	Disclosure
14[a] The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1. **1.4.4 MgmtInit State** The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp.

Claim 14	Disclosure
	CMIS, 22. **1.5.4 Control Set Overview** A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 14	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 14	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 14	Disclosure
	1.7 Module Memory Map This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module. CMIS, 44. **1.5.5 Signal Integrity Control Field Background** The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated. The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11). Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable Control / Tx Adaptive Input Eq Enable value to use this control Tx Input Eq Adaptation Freeze: 1 Tx Input Eq Adaptation Store: 1 Tx Adaptive Input Eq Recall: 1 Tx Input Eq control: 0 The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module. CMIS, 40.

Claim 14	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 14	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value / Bit pattern / Output Amplitude 0 / 0000 / 100-400 mV (P-P) 1 / 0001 / 300-600 mV (P-P) 2 / 0010 / 400-800 mV (P-P) 3 / 0011 / 600-1200 mV (P-P) 4-14 / 0100-1110 / Reserved 15 / 1111 / Custom CMIS, 41.

Claim 14	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

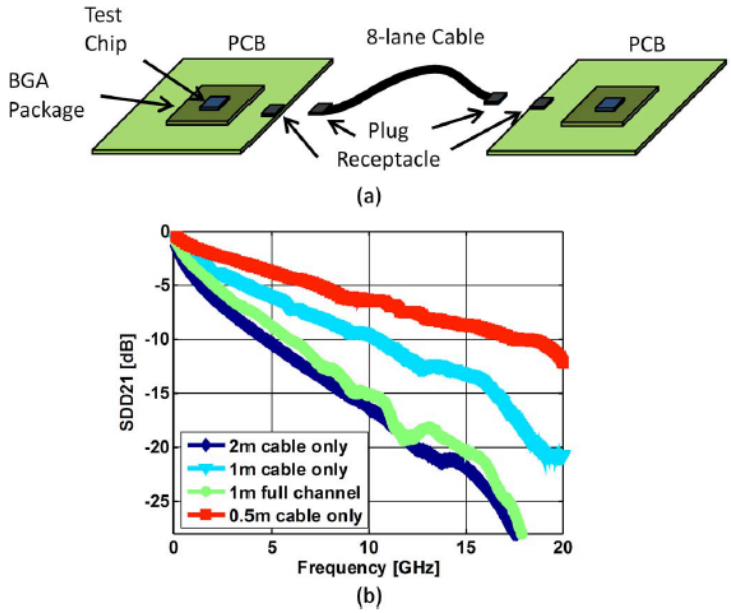
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

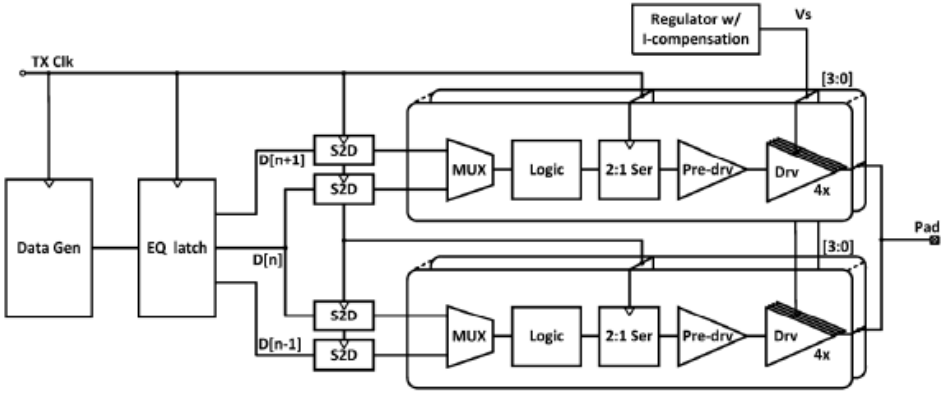
Claim 14	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

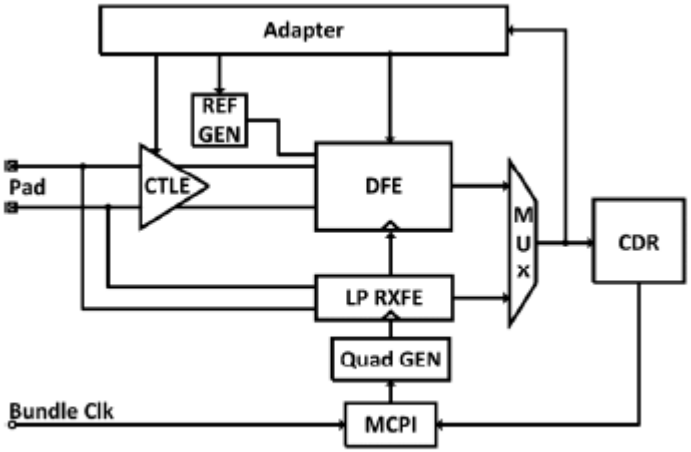
Claim 14	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 14	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 14	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

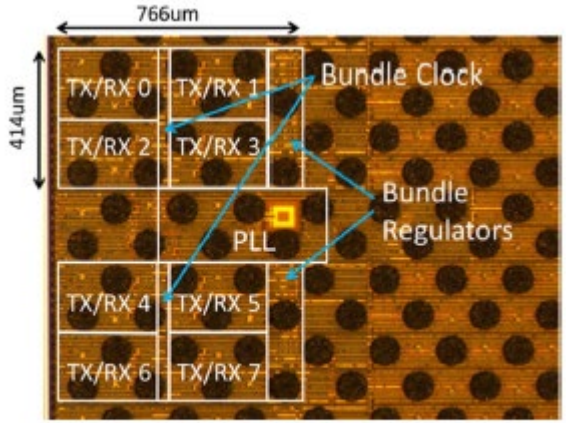
Claim 14	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 14	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 14	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

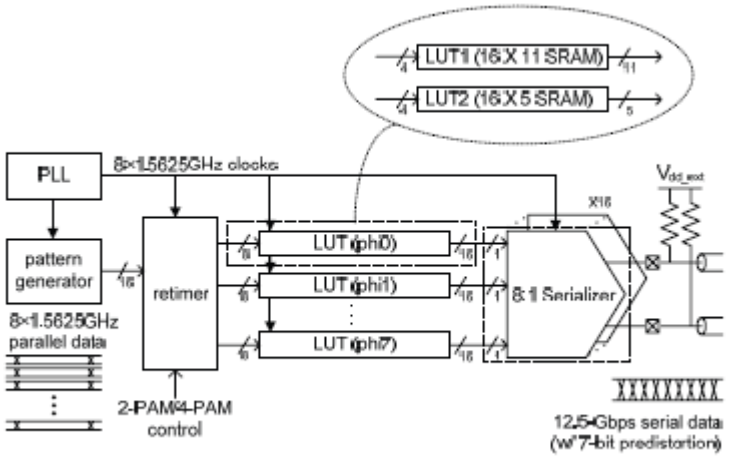
Claim 14	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 14	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 14	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 14	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 14	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 14	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 14	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 14	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 14	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 14	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 14	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 14	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 14	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 14	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 14	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 14	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 14	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 14	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

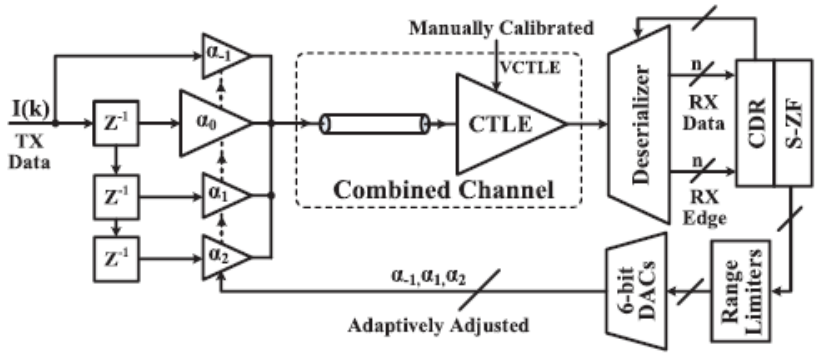
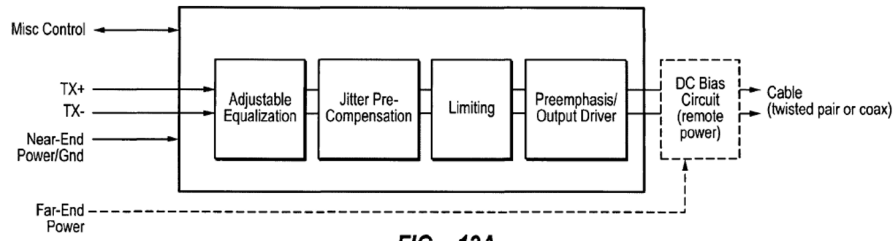
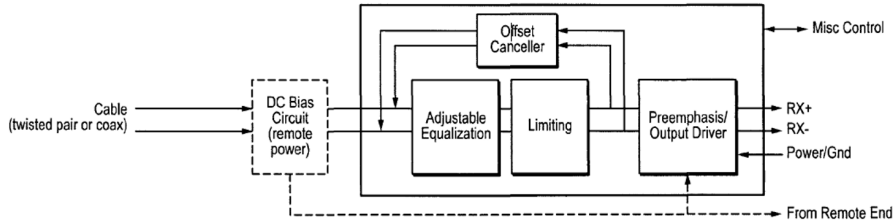


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 14	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 14	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage." Ikeda, 7:44-55.

Claim 14	Disclosure
	U.S. Patent No. 7,762,727 to Aronson Aronson discloses an active cable for high-speed transmissions between network nodes. See, e.g., Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.  *FIG. 12A*  *FIG. 12B* Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23.

Claim 14	Disclosure
14[b] wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: Abstract: This document defines the Common Management Interface Specification (CMIS) for pluggable modules such as QSFP Double Density (QSFP-DD), OSFP and COBO. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers. CMIS, 1.

Claim 14	Disclosure
	1.4.4 MgmtInit State The MgmtInit state is a module control state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both active modules and passive copper cable assemblies. During this state, the module shall configure the memory map and initialize the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For active modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state. Interrupt flag conformance in the MgmtInit state is defined in Section 1.6.1. All disallowed interrupt flags shall not be set during MgmtInit. Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. In Hardware Init mode, power-up defaults may include DataPathPwrUp bits. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface. Upon completion of MgmtInit, the next state depends on the Init mode of the module. If the module is booting in Software Init mode, the next state is ModuleLowPwr. If the module is booting in Hardware Init mode, the next state is ModulePwrUp. CMIS, 22.

Claim 14	Disclosure
	1.5.4 Control Set Overview A Control Set is a group of registers that are used to provide initialization settings for data paths. Each control set includes fields to select the Application, fields for signal integrity control, and fields to apply these Application and signal integrity settings. Within a Control Set, the host uses the Application Select Control registers defined in Table 56 or Table 60 to select the desired Application(s) and configure the data path(s) within the module. The Application Select Control registers include an ApSel code, a Data Path Code and an Explicit Control bit. Each supported Application advertised in Table 26 and Table 48 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The Data Path Code in the Application Select Control registers is used to specify the lanes used for an instance of an Application. Each data path is identified by the lowest numbered lane in that data path. The host shall assign lane combinations that are in accordance with the lane assignment advertised by the module for that application. For a multi-lane data path the host shall write the same data path code in all lanes of that data path. The Explicit Control bit allows the host to provide either its own signal integrity values or use the Application-defined signal integrity values associated with the ApSel code. These Application-defined settings shall provide host electrical and media interfaces that are compliant with the standard associated with the selected Application. To use Explicit Control for a given lane (by setting the control bit to '1'), the host shall provide values for all signal integrity controls for that lane in the Control Set. The value of the Explcit Control bit determines which signal integrity control fields within the Control Set are used in an Apply operation. When the Explicit Control bit for a given lane is set to the value listed in Table 10, the associated control field value for that lane is used in an Apply operation. The control field value for that lane is ignored for all other values of the Explicit Control bit. CMIS, 37-38.

Claim 14	Disclosure

Table 10- Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

CMIS, 38.

1.5.4.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy those settings from the Staged Control Set registers into the Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests power up of a data path, the module shall use the settings in the Active Control Set for data path initialization. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings at power on or exit from reset.

CMIS, 38.

Claim 14	Disclosure
	1.5.5.1 Tx Input Eq Adaptation Store/Recall Methodology Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time. Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 46. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification. The Tx Input Eq Adaptation Store control field is located in Table 54. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while a data path is powered and occurs when requested. The Tx Input Eq Adaptation Recall control field is located in Table 57 for Staged Set 0 and Table 61 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set. The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes. CMIS, 41-42.

Claim 14	Disclosure

1.7 Module Memory Map

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

CMIS, 44.

1.5.5 Signal Integrity Control Field Background

The signal integrity control fields provide an opportunity for the host to specify signal integrity settings to the module. For each control, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 11 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control (see Table 11).

Table 11- Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 12. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 46 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 42 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

CMIS, 40.

Claim 14	Disclosure

Table 12- Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13-15		Custom

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 46 to determine if the module supports Rx Output Emphasis Control. Refer to Table 42 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 13- Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000	No Equalization	No Equalization
1	0001	1 dB	0.5 dB
2	0010	2 dB	1.0 dB
3	0011	3 dB	1.5 dB
4	0100	4 dB	2.0 dB
5	0101	5 dB	2.5 dB
6	0110	6 dB	3.0 dB
7	0111	7 dB	3.5 dB
8-10	1000-1010	Reserved	Reserved
11-15	1011-1111	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-(C(-1)/(C(-1)+C(0)+C(1))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-(C(1)/(C(-1)+C(0)+C(1))

CMIS, 40-41.

Claim 14	Disclosure
	The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 46 to determine if the module supports Rx Output Amplitude Control and Table 42 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows: **Table 14- Rx Output Amplitude Codes** Code Value | Bit pattern | Output Amplitude 0 | 0000 | 100-400 mV (P-P) 1 | 0001 | 300-600 mV (P-P) 2 | 0010 | 400-800 mV (P-P) 3 | 0011 | 600-1200 mV (P-P) 4-14 | 0100-1110 | Reserved 15 | 1111 | Custom CMIS, 41.

Claim 14	Disclosure

1.7.4.10 Implemented Signal Integrity Controls

Table 46 describes the implemented signal integrity controls.

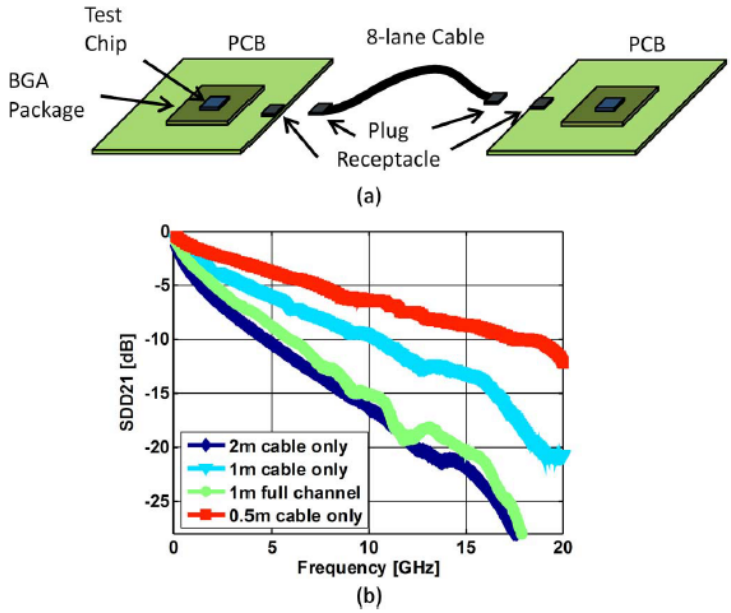
Table 46- Implemented Signal Integrity Controls (Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Pg 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

CMIS, 71.

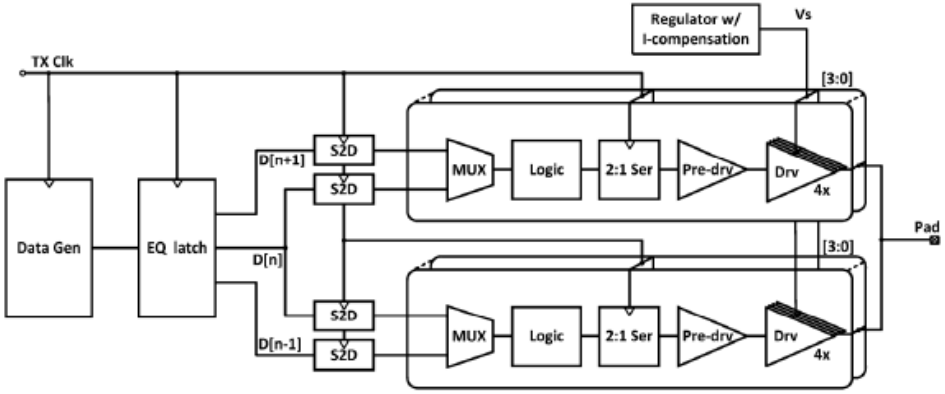
Claim 14	Disclosure
	***Abstract*—This paper details the design of an 8-lane bidirectional link for both within-the-box and external communications in 22 nm CMOS technology. A low profile connector with a high density cable assembly ensure a data rate of up to 32 Gb/s per lane while maintaining channel loss below 25 dB. Channel equalization is performed by a combination of a 3-tap feed-forward equalizer (FFE), single-stage continuous-time linear equalizer (CTLE) and a 6-tap decision-feedback equalizer (DFE). Collaborative timing recovery is used to enable lane characterization without degrading jitter performance. Phase error decimation, with a conditional phase detection scheme, is used to reduce the DFE complexity by 50%. Power consumption over a wide range of data rates from 4 to 32 Gb/s is reduced by using regulated CMOS clocking with lane bundling, low swing transmitter with a source-series terminated (SST) driver and a highly reconfigurable receiver with an active inductor CTLE. At a lane data rate of 32 Gb/s, over a 0.5 m cable with 16 dB of loss, a transceiver lane consumes 205 mW from a 1.07 V supply. The power scales down to 26 mW from a 0.72 V supply at 8 Gb/s, when transmitting over a channel with 8 dB loss. The active silicon area per lane is 0.079 mm^2.** Musah, Abstract. The link architecture block diagram is shown in Fig. 2, which includes 8 bidirectional transceiver lanes [5]. The bidirectional

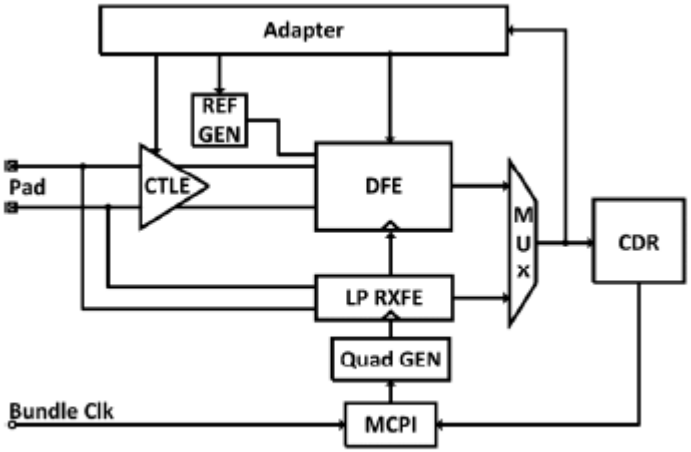
Claim 14	Disclosure
	lanes support asymmetric BW operation through the use of unequal transmit and receive rates or by configuring the lanes to transmit or receive. Link data rate scalability is achieved with minimal power overhead by operating in dual modes and by having multiple configurations for clocking, transmitter (TX) and receiver (RX) circuits depending on data rate. Each lane consists of a TX with a low-swing voltage-mode driver and low power pre-emphasis, a data-rate scalable RX front-end (RXFE) with a continuous-time linear equalizer (CTLE) and decision-feedback equalizer (DFE), embedded clock and data recovery (CDR), lane clocking and adaptation and calibration logic. The link is targeted to applications whose data rate requirements may span from 4 to 32 Gb/s per lane. Supply voltage scaling, assuming a switching regulator, is employed to ensure that the link power decreases at least linearly with data rate [6]. However, even with supply voltage scaling, a link design solely optimized for performance may exhibit sublinear power scaling with data rate, as circuit blocks with static power consumption degrade power efficiency at lower rates. To overcome the challenge of power optimization across different data rates, a multi-mode design approach was adopted, transforming the lane from high performance mode (HP) to low power mode (LP). The HP and LP modes span 8–32 Gb/s and 4–12 Gb/s, respectively. Supply voltage scaling, power gating, bias control and transmit swing control are used to ensure optimal power-performance scaling. Musah, 3079-3080.

Claim 14	Disclosure
	 Fig. 1. (a) Interconnect topology. (b) Channel frequency response. Musah, 3080.

Claim 14	Disclosure
	The CDR block diagram in Fig. 5 shows the bundle timing recovery loop. Similar to the approach introduced in [7], the collaborative CDR combines phase error information from the 4 lanes in a bundle to synthesize the recovered clock. However, instead of using full phase information from each lane to pursue wider jitter tracking BW, the per-lane phase contribution is decreased to one-fourth to reduce the receiver complexity. Moreover, unlike [8], this CDR scheme enables full eye margining characterization of one lane within the bundle while still transmitting data. When the collaborative CDR is enabled, the lane CDR is configured to track low-frequency inter-lane skew. Musah, 3081.

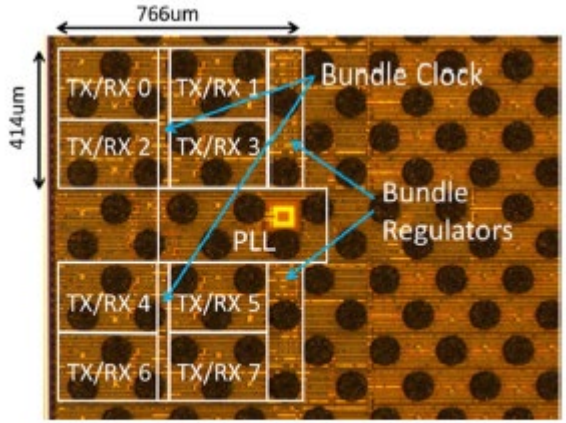
Claim 14	Disclosure
	With differential RX termination, an unequalized voltage-mode driver output stage dissipates about a quarter of the current-mode driver output stage power [12]. The differential equalization technique [13] is utilized to improve the voltage-mode driver power efficiency when equalization is enabled. To support the bidirectional operation of the link, the voltage-mode driver performs two functions: (a) a data driver and termination in the TX mode; (b) a common-mode voltage generator and RX termination in the RX mode. The block diagram for the TX is shown in Fig. 6. An on-chip PRBS data generator (Data Gen) drives the equalization delay chain to produce the delayed versions of the signals needed for equalization. The reconfigurable 1 to 3-tap differential equalization is realized with 2 banks of 16-leg drivers, bringing the total to 32 legs. Based on the equalization MUX (EQ MUX) selection, the driver legs in the first bank are split between the primary-cursor and the post-cursor signal, while those in the other bank are split between the primary-cursor and the pre-cursor signal. Musah, 3082.

Claim 14	Disclosure
	 Fig. 6. Half-rate transmitter architecture. Musah, 3082. The RX block diagram is shown in Fig. 7. The RXFE is configured to operate in HP and LP modes. The CDR, MCPI and quadrature generator are shared in both modes. A half-rate front-end with 2× oversampling phase detection is used to recover the clock and data in the LP mode. This results in a 4-way interleaved receiver, with each interleaved slice realized as a

Claim 14	Disclosure
	simple comparator that contains a track-and-hold, sense amplifier and RS latch. Offset correction is included in the input of the sense amplifier. Since the LP RX is employed only at data rates below 12 Gb/s, the TX FFE is sufficient to mitigate channel induced inter-symbol interference (ISI). The HP RXFE is designed to equalize approximately 18 dB of the 24 dB channel loss target and includes a first-order CTLE with auto-gain control (AGC) and a 6-tap quarter-rate DFE. The DFE uses Mueller-Muller baud-rate phase detection [15] to avoid having an auxiliary equalized path for error detection as in [1]. A 6b resistor string DAC generates the reference voltage levels needed for the phase detection. A background adaptation unit monitors and controls the DFE coefficients and gain parameters. Musah, 3082.  Fig. 7. Multi-mode RX.

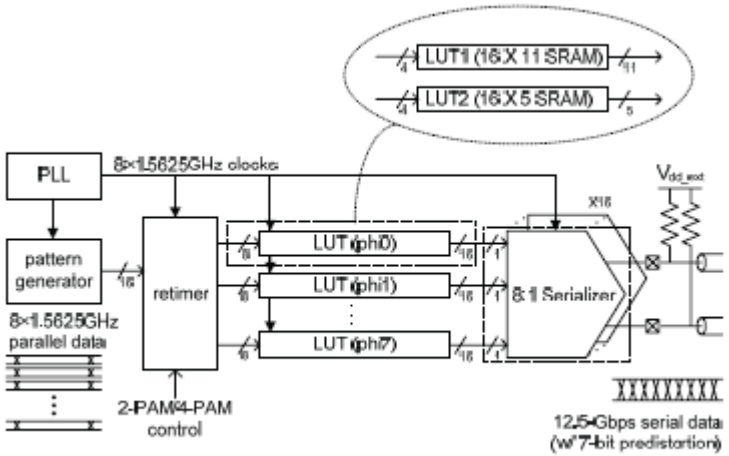
Claim 14	Disclosure
	Musah, 3082. Each comparator has a 9b segmented DAC (3b coarse, 6b fine) with programmable range and resolution to cancel the comparator offset and to provide the speculative tap value. The remaining five DFE taps are directly fed back into the summer. All DFE coefficients have a 6b control, with varying ranges, to ensure accurate ISI cancellation over various channel lengths and supply voltages. On-die logic controls foreground and background adaptation of CTLE, CML summer and sense amplifier offset voltages. Foreground calibration requires interruption of data transmission/reception while background calibration happens with the link fully operational. The logic also performs continuous AGC, DFE tap weight adaptation and reference voltage adaptation in the background using a sign-sign least mean squares (SSLMS) algorithm. To reduce design and area overhead of the RX adaptation, a unified adaptation macro unit (AMU) is configured to adapt or calibrate all RX parameters. The AMU block diagram is shown in Fig. 10. The RXFE output signals are first pre-processed to generate data, error and error valid signals. Correlation of data and error signal are used to adapt the DFE tap coefficients. If data mask is enabled, only the error signals are sent to the up/down counter enabling offset cancellation, AGC and reference voltage adaptation. De-asserting the enable signal freezes the AMU outputs allowing normal operation for foreground calibrated parameters like summer offsets. Musah, 3084.

Claim 14	Disclosure
	The CTLE drives 4 slices of the reconfigurable DFE. Fig. 13 shows a simplified schematic of one DFE slice. The quadrature sampling clocks for the interleaved track and hold circuit ensure that only two DFE slices load the CTLE at any instance, thereby reducing the CTLE power needed to achieve the target BW. A CML summer following the track and hold sums the DFE currents from the non-speculative taps. To facilitate data-rate scalability of the DFE, the CML summer has to operate across a wide frequency range. Thus, the summer NMOS load is biased to be in triode and is coupled to the tail current to minimize the sensitivity of the output common-mode voltage to the summer bias. This biasing technique reduces the summer current at lower data rates to save power, while not sacrificing the sense amplifier performance. The voltage offset of the CML summer is cancelled with a digitally controlled offset current sourced into its output. The CML summer is followed by the speculative DFE tap latches and MUX. The three parallel latches can be configured for baud-rate phase detection and to receive data with or without tap speculation. To support the various latch configurations, there are three input differential pairs with inputs from the CML summer, the voltage reference generator and the coarse speculative tap coefficient. The speculative DFE tap is applied in a coarse-fine approach using a 3b device DAC (coarse) and a 6b current DAC (fine). This configuration enables wide voltage ranges that can realize equalization and comparator offset cancellation concurrently. The MUX provides additional amplification and speculative tap selection. When the speculative tap is disabled, the MUX is bypassed. Musah, 3085.

Claim 14	Disclosure
	Two 4-lane bidirectional transceivers, shown in Fig. 15, were fabricated in a 22 nm CMOS process. A 4-lane transceiver occupies 0.317 mm^2. In addition to the cables listed in Section I, a combination of cables and FR-4 PCB traces were employed to realize different channel losses to characterize the link performance at lower data rates. Musah, 3086.  Fig. 15. 22 nm CMOS test chip micrograph. Musah, 3086.

Claim 14	Disclosure
	We have described a scalable bidirectional serial link that targets a variety of applications with data rate requirements within the range of 4 to 32 Gb/s. Supply voltage and TX output swing scaling, regulated CMOS clocking and clock bundling were employed to maintain the per lane power efficiencies between 1 and 5.7 pJ/b. The area of the 8-lane transceiver is 0.634 mm^2. With a TX voltage swing of 630 $mV_{pp-diff}$ and lane CDR enabled, the 4-lane link demonstrated error-free ($BER < 10^{-12}$) transmission over a 0.5 m cable with PRBS10 data at 32 Gb/s per lane. Musah, 3088. ***Abstract*—This paper presents a 12.5-Gbps transmitter that uses a lookup table (LUT)-based equalizer to compensate for within-die imperfections. An equalization technique with 2x sampling is proposed to accommodate timing offsets in the multiphase clocks used for 8:1 serialization. LUT code remapping is also demonstrated to compensate for mismatch effects that introduce nonlinearity in the transmit DAC. Experimental results of a 7-bit resolution transmitter with 4-tap equalization, implemented in 0.13μm CMOS, show the LUT-based equalizer can significantly improve the signal integrity of an otherwise closed eye for data transmitted at 12.5-Gbps.** Chung, Abstract.

Claim 14	Disclosure
	This paper demonstrates a 12.5-Gbps transmit DAC with 7-bit resolution and 4-tap equalization using look-up tables (LUT). The LUT-based equalizer supports both linear and nonlinear forms of equalization and also offers flexibility to easily reprogram equalization tap settings [4,5]. In addition to compensating for channel losses, the proposed equalizer can be used to mitigate various mismatch effects. The transmitter employs an 8-way interleaved structure using 8 multiphase clocks to alleviate on-die speed limitations. Unfortunately, these clock phases are susceptible to variations that lead to inter-symbol timing mismatch and cause eye closure. While phase adjusters can be employed to reduce phase mismatch [6,7], we can leverage the flexibility of the existing transmit equalizer to improve signal integrity by treating the mismatch effects as inter-symbol interference (ISI). Other within-die mismatch effects, such as DAC current mismatch and nonlinearity, and deviations in pulse peak positions, are also addressed by remapping LUT codes. While this paper relies on an external sampling scope and offline analysis, an on-chip sampling scope can be used to measure transmitter characteristics and drive an internal self-calibration engine [8]. Chung, 563.

Claim 14	Disclosure
	 Fig. 1. Overall transmitter block diagram Chung, Figure 1.

Claim 14	Disclosure
	Fig. 1 presents the block diagram of an 8-way interleaved transmitter architecture. It uses a ring-oscillator-based phase-locked loop (PLL) to generate 8 evenly-spaced 1.5625-GHz clock phases for 8:1 serialization. The retimer block samples and rearranges parallel data from a pseudo-random pattern generator (or input data memory) to generate the addresses for 8 parallel sets of LUTs, each running off of a different clock phase. The LUT uses a set of data (current, next, and two previous bits) as addresses that correspond to 4-tap mappings of transmit equalizer outputs. The parallel implementation was originally chosen to accommodate speed limitations of the automatically-generated memories, but the interleaved structure confers the benefit of supporting individual equalizer settings for each serializer path to compensate for phase mismatch effects. As shown in the inset of Fig.1, one LUT set comprises two 16-word SRAMs, instead of one 256-word SRAM, to further overcome speed limitations and to reduce power and area overheads. LUT1 uses a set of current and previous bits as an address to generate a portion of the transmitter output that consists of the main-cursor and first post-cursor components for two adjacent bits in each symbol output. The 11-bit code out of each LUT1 ultimately maps to one of 128 possible output levels (7-bit resolution) with 4-bit binary coding and thermometer coding for the remaining

Claim 14	Disclosure
	higher-order bits. LUT2 uses a set of next and second previous bits as an address that maps to the pre-cursor and second-post cursor compensation components of the transmitter output. Since the pre-cursor and second post-cursor components typically exhibit smaller amplitudes in transmit-side equalization, the LUT2 output requires fewer bits (5-bit binary). Each LUT generates data for 1 out of 8 interleaved symbols combined together via an 8:1 serializer. The 11- and 5-bit codes out of each LUT are connected to 16 parallel serializers. Chung, 563-564. While the LUT-based equalizer can also compensate for channel loss, the focus of this section is on the compensation of within-die variations—improving the worst-case eye by compensating for phase mismatch and DAC current mismatch. Uneven spacing of the multiphase clocks is the dominant cause of signal integrity degradation, creating the worst-case eye. While this issue can also be addressed with phase adjusters [6,7], we investigate how the proposed LUT-based equalizer can also alone compensate for the clock phase mismatch effects. Chung, 565.

Claim 14	Disclosure
	The digital signal processing (DSP) module of receiver module **300** includes a line R×D macro, which is a part of the data path. The DSP module provides many functionalities. Depending on the implementation, the DSP module may include an FFE block, a PAM-4 slicer, a PAM4-DFE, a PAM-4 reflection canceler, a PAM-4 level dependent equalizer, a PAM-4 1+D de-precoder, and/or a soft FEC decoder. Riani, 7:47-54. As an example, the FEC block may be implemented with an 6/10-tap FFE. The assumption is that the interface is 32-unit intervals (UI) interleaved. The 6/10-tap FFE, with gain and DC offset compensation, provides the equalization needed. The 10-taps are fully adaptive. The PAM-4 slicer block compares the FFE output data with thresholds (e.g., {Tn, Tm, Tp}), and produces the PAM-4 decisions. For example, thresholds {Tn, Tm, Tp} are adaptive and can be used to compensate for the level-dependent noise nature of optical channels. The PAM-4 decision feedback equalizer (DFE) is configured to provide nonlinear adaptive feedback on the inner levels in the data path. The line receiver module **300** may also include a PAM-4 reflection canceller to reduce

Claim 14	Disclosure
	group-delay effects. The line receiver module **300** may additionally include a PAM-4 level dependent equalizer, which provides equalization for the two inner levels of the PAM-4 eyes. The PAM-4 1+D de-precoder block is configured to operate in DFE mode. In the DFE mode, to overcome DFE Error propagation, a 1/(1+D) pre-coder is employed on the transmit driver and on the receiver end. The final DFE decisions pass through the (1+D) filter to cancel the effect of pre-coder. The line receiver module **300** may also include a soft FEC that work with parity check code, which inserts parity information every 20 FEC symbols. It is to be appreciated that the soft FEC can provide a 1.5 dB gain with 5% overhead. In various implementations, SFEC supports in 200GE mode where the host data is KP4 FEC encoded. For example, the use of SFEC is described in patent application Ser. No. 15/691,023, filed Aug. 30, 2017, which is incorporated by reference herein. Riani, 7:55-8:17.

Claim 14	Disclosure
	The host receivers are implemented with various features. For example, an OIF 56G-VSR compliant interfaces is implemented with adaptive CTLE/AGC that is able to equalize 10 dB channels loss plus up to 4 dB total package loss. Decision feedback equalizer (DFE) may be included for trace reflection cancellation. Independent CDRs can be configured in each lane with full-rate LC VCO. Similarly, independent power down control is provided for each lane. Host receivers may also include support for reference-less operation. Additional features include SNR monitor, adaptive equalizer convergence monitor, and loss of signal (LOS) detector with programmable thresholds, PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and PAM-4 MSB/LSB swap. Host receivers may also have diagnostic features, such as PRBS13Q, PRBS58/31/23/16/15/13/11/9/7 checkers, PRBS auto-polarity detection, and continuous identical symbol detection. Riani, 9:48-64.

Claim 14	Disclosure
	FIG. **5** is a simplified block diagram illustrating a host side receiver module **500** according to embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. For example, host side receiver module **500** implements section **201** in FIG. **2**. Receiver module **500** may operate in different modes with an aggregate bandwidth of 200 Gbps. For example, receiver module **500** supports eight lanes of NRZ data or four lanes of PAM-4 data. As shown in FIG. **5**, the receiver lanes are capable of receiving data streams at 28.125 Gbps in NRZ mode or 28.125 GBd in PAM-4 mode. For example, data received from the eight data lanes are transmitted through eight parallel data transmission lanes. The AFE **501** receives optical signal through optical communication channels. The AFE **501** is configured to handle various types of data format, such as 56 Gbps of PAM-4 data. In various embodiments, AFE **501** supports adaptive CTLE/AGC for equalizing 10 dB loss channels and up to 4 dB total package loss.

Claim 14	Disclosure
	The AFE block **501** may also include a decision feedback equalizer covering h3 to h12 used to equalize reflections. The AFE block **501** may also include independent a clock data recovery (CDR) module with full rate inductive/capacitive (LC) voltage controlled oscillator (VCO). Each of the eight data lanes may have its own independent power down control. The AFE block **501** may additionally support reference-less operation (receiver is capable of coarse tuning and frequency locking its VCO to incoming data without an external pilot tone). The AFE block **501** may also include a signal-to-noise ratio (SNR) monitor and/or an adaptive equalizer convergence monitor. Additionally, the AFE block **501** may also include a loss of signal detector with programmable threshold (e.g., 50 mV to 100 mV). It is to be appreciated that the functionalities of AFE block **501** may be provided by the analog support block **502**. Riani, 10:6-41.

Claim 14	Disclosure
	Data streams, once processed by the AFE block **501**, are transmitted through data path **504**. In various embodiments, data path block **504** provides PAM-4 inverse gray coding, polarity inversion, PAM-4 decoding, and/or PAM-4 MSB/ LSB swapping. DSP block **503**, as shown, is coupled to AFE block **501**, data path block **504**, and CID detector block **505**. For example, DSP block **503** is capable of processing 32 UI of data and error samples per clock cycle. In various implementations, DSP block **503** provides six shared plus ten DFE LMS engines and two shared search engines. The DSP block **503** may additionally provide calibration and adaption (e.g., by determining operating parameters) for LFEQ, CTLE, AGC gain, sample offsets, thresholds, phases, and DFE. The DSP block **503** may also include eye monitor with 256 steps over 2 unit-intervals and 512 voltage steps. To perform signal processing, the DSP block **503** may be implemented with capture buffer for 32 unit-intervals of aligned data, error, and eye monitor samples and qualifiers. Riani, 10:42-60.

Claim 14	Disclosure
	II. TRANSMITTER CHIP *A. Overall Architecture* Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data D0⟨n⟩, D1⟨n⟩, D2⟨n⟩, and D3⟨n⟩ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed

Claim 14	Disclosure
	to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively. The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques. Zheng, 2964.

Claim 14	Disclosure
	III. Receiver Chip *A. Overall Architecture* The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV. Zheng, 2968.

Claim 14	Disclosure

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

Zheng, 2970.

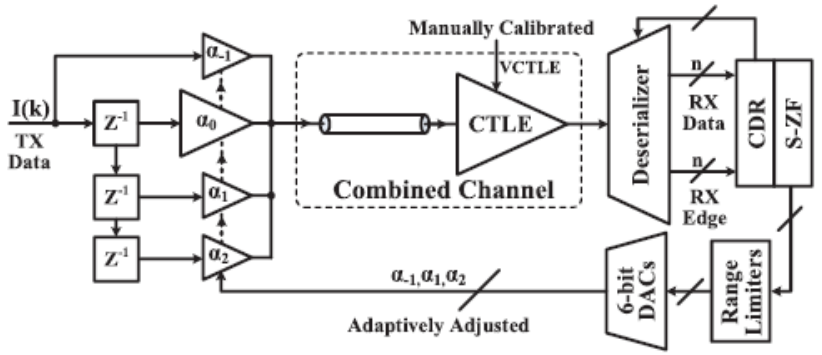
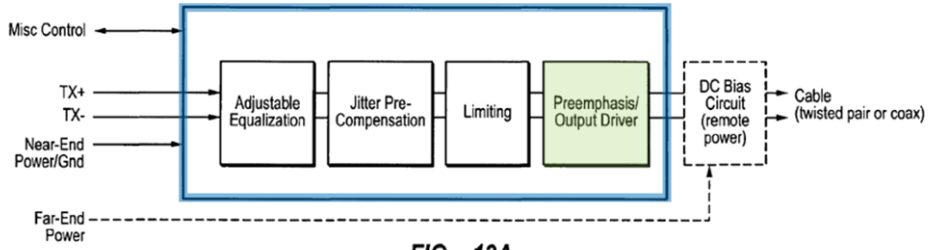
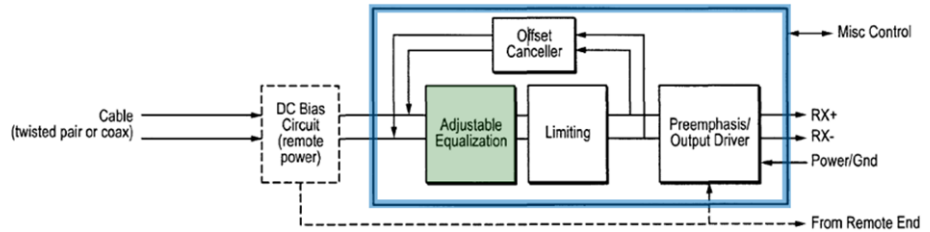


Fig. 17. Implemented equalization scheme with the proposed S-ZF algorithm.

Claim 14	Disclosure
	Zheng, 2970. *D. Implementation of the Edge-Data Correlation-Based S-ZF* Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation $\mathrm{ResCor}_l(n)$, which denotes $\mathrm{sign}[e(n)] \cdot D(n-l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20 further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n+1) = 0]$, $\mathrm{ResCor}_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n+1) = 1]$, $\mathrm{ResCor}_l(n)$ is assigned $+1$ or -1 when the polarities of $D(n-l)$ and $E(n)$ are identical $[D(n-l) \oplus E(n) = 0]$ or opposite $[D(n-l) \oplus E(n) = 1]$. Zheng, 2972.

Claim 14	Disclosure
	This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights. Zheng, 2976. "The filter circuit 206 may be designed to have various characteristics as required. For example, assuming attenuation of the high frequency region in the coaxial cable transmission line beforehand, the filter circuit 206 can have a characteristic that strengthens high frequency range components (transmission signal pre-equalization treatment). On the other hand, the filter circuit 206 can also have another characteristic that suppresses excessive high frequency components to suppress unintentional emission. By providing a filter circuit with these types of characteristics in the connector base 20, a desired output signal P31 spectrum can be obtained according to the usage." Ikeda, 7:44-55.

Claim 14	Disclosure
	U.S. Patent No. 7,762,727 to Aronson One obvious way to implement the equalization coefficients used by a FIR filter and an equalizer is during manufacturing-testing. *See, e.g.*, Aronson at 14:35-39 (Fig. 12A's pre-equalization parameters for transit over the line-side are "adjusted at factory setup"), 15:1-8 (Fig. 12B's equalization may be "fixed" or "adjustable but factory set" "at the time of the cable manufacture").  *FIG. 12A*  *FIG. 12B*