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(54) SYSTEM AND METHOD FOR PROVIDING SLICER LEVEL ADAPTION

(76) Inventors: **James Gorecki**, Hillsboro, OR (US); **David A. Martin**, Portland, OR (US); **Yaohua Yang**, West Linn, OR (US)

Correspondence Address:
Neil A. Steinberg
Steinberg & Whitt, LLP
Suite 514
2672 Bayshore Parkway
Mountain View, CA 94043 (US)

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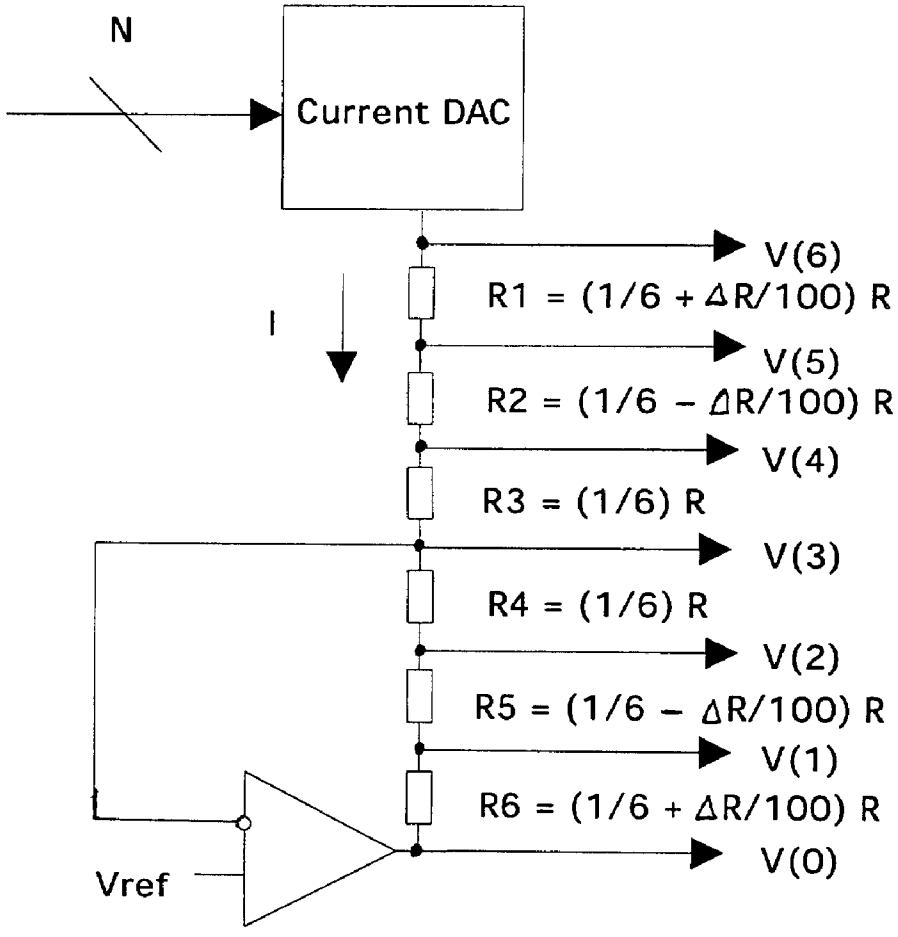
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(57) **ABSTRACT**

The present invention relates in general to a method, apparatus, and article of manufacture for providing high-speed digital communications through a communications channel. In one aspect, the present invention employs an automatic slicer level adaption to enhance the performance of a high speed communications system.



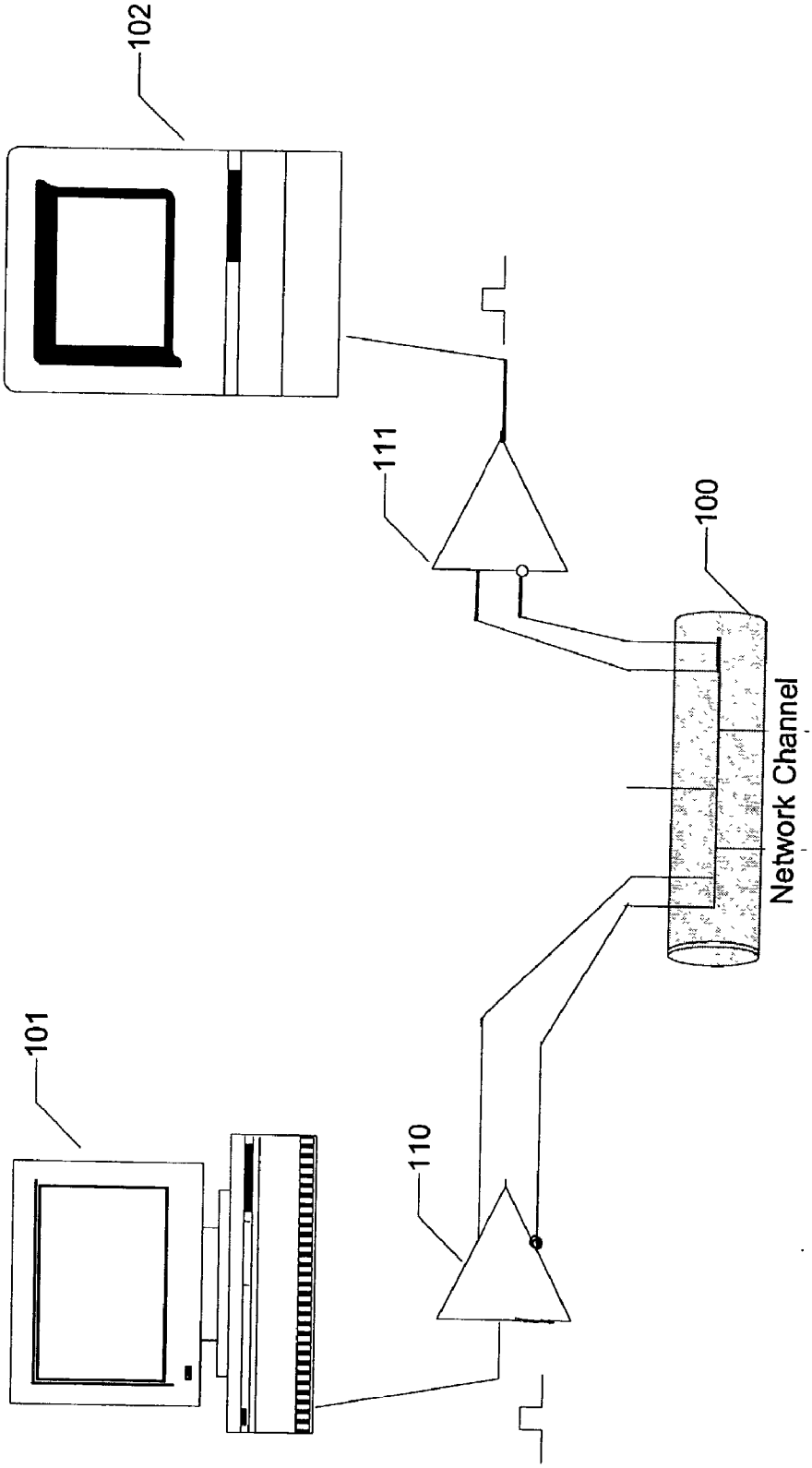


FIGURE 1

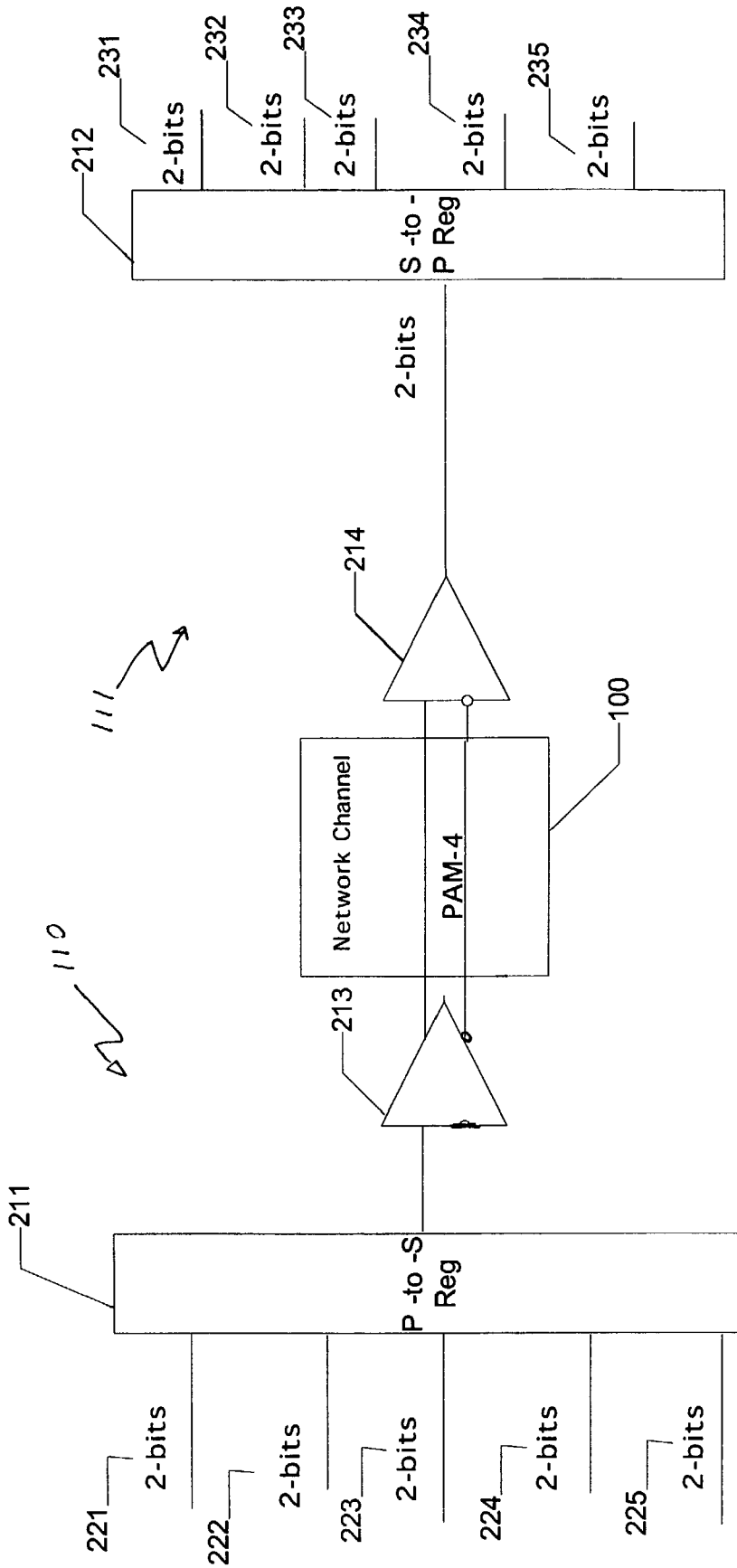
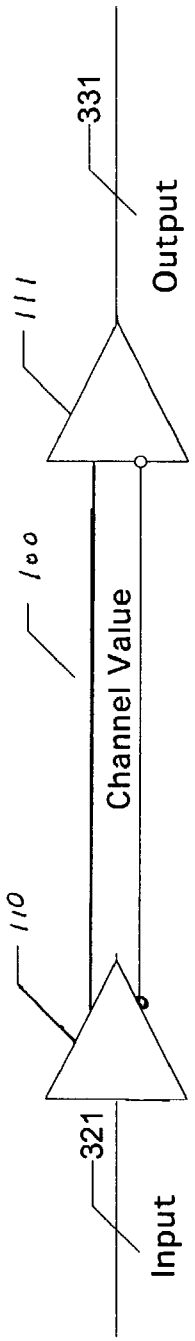

231
232
233
234
235
212
2-bits
2-bits
2-bits
2-bits
2-bits
S -to - P Reg
2-bits
214
111
100
Network Channel
PAM-4
110
213
211
P -to -S Reg
221
222
223
224
225
2-bits
2-bits
2-bits
2-bits
2-bits

FIGURE 2



Signal Level	Bit Xmit
+ 3	01
+ 1	00
- 1	11
- 3	10

FIGURE 3

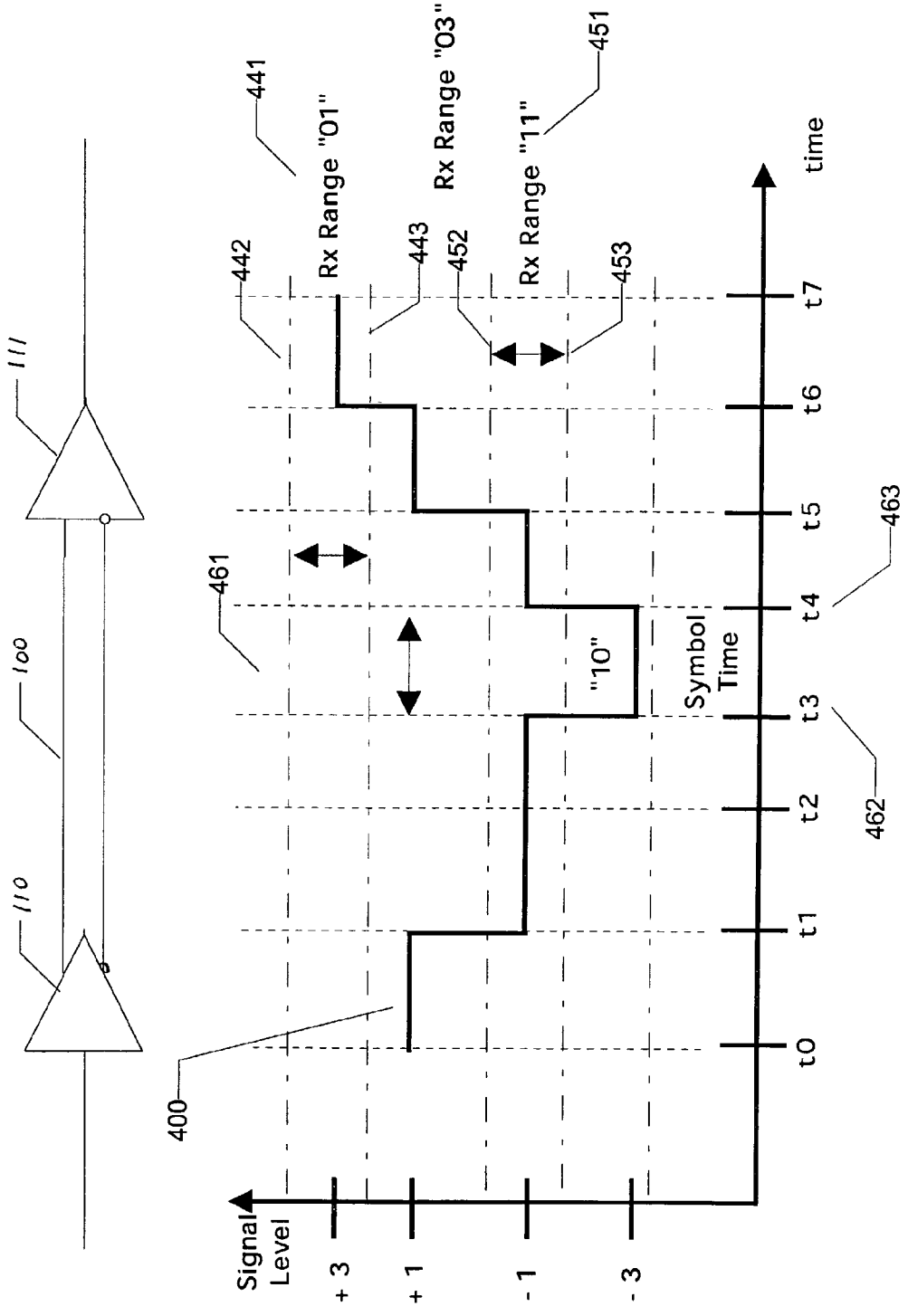

111
100
110
400
441
Rx Range "01"
442
443
Rx Range "03"
451
452
Rx Range "11"
453
461
"10"
Symbol Time
463
462
time
t0
t1
t2
t3
t4
t5
t6
t7
Signal Level
+ 3
+ 1
- 1
- 3

FIGURE 4

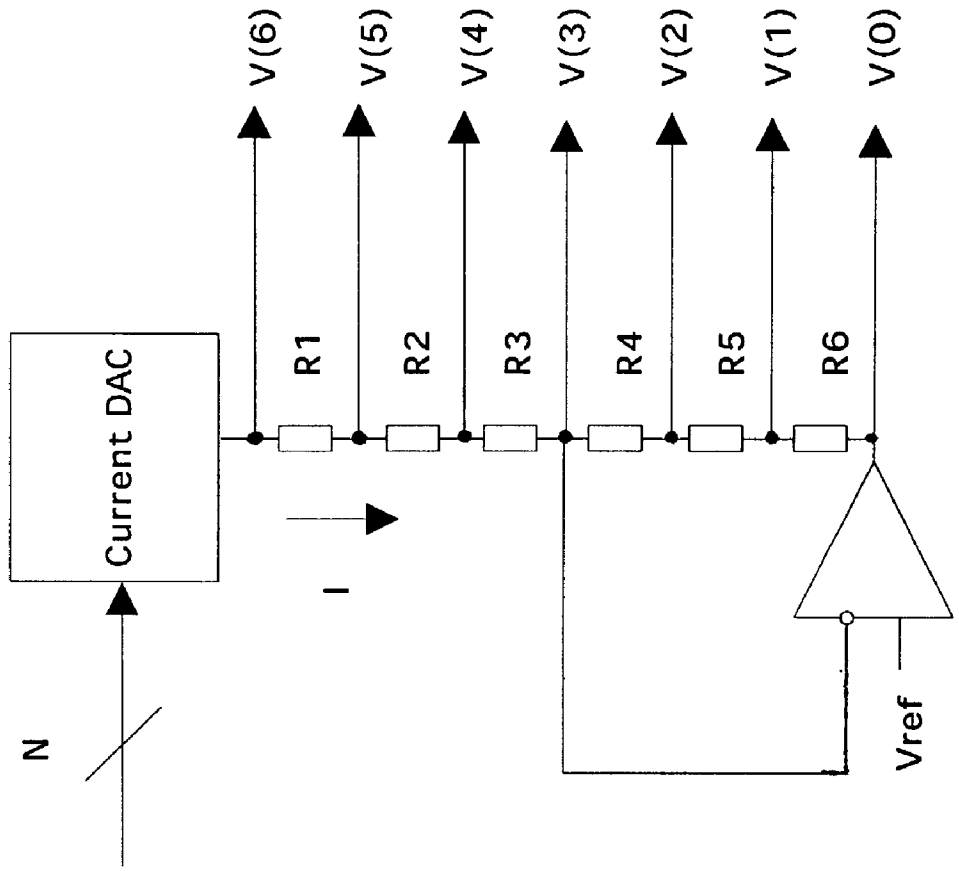


FIGURE 5

FIGURE 6B

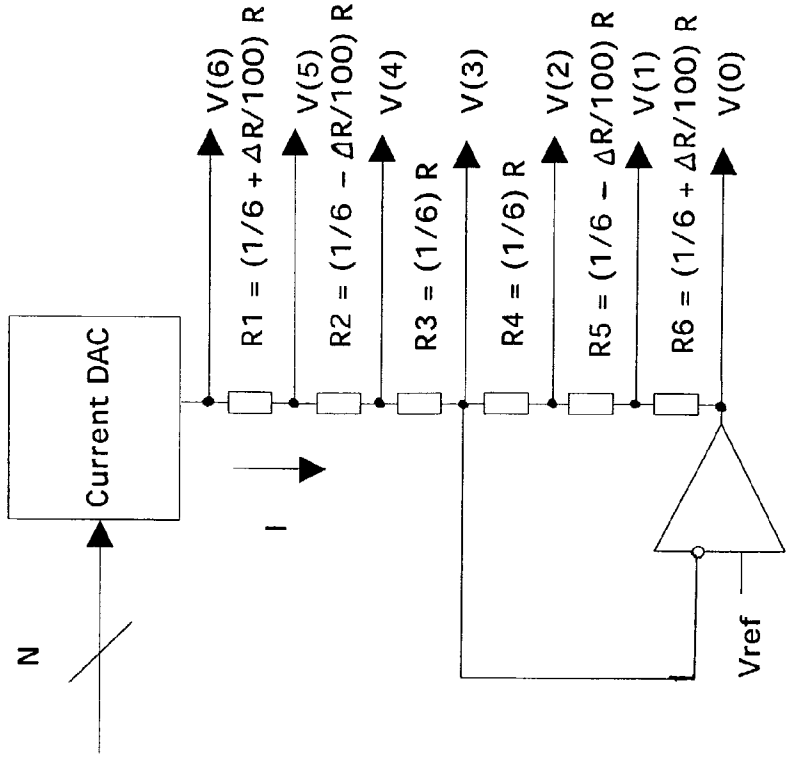
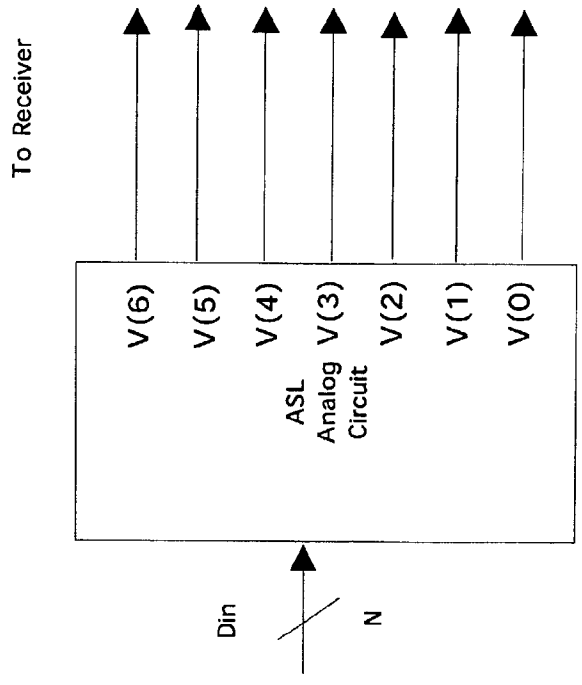


FIGURE 6A



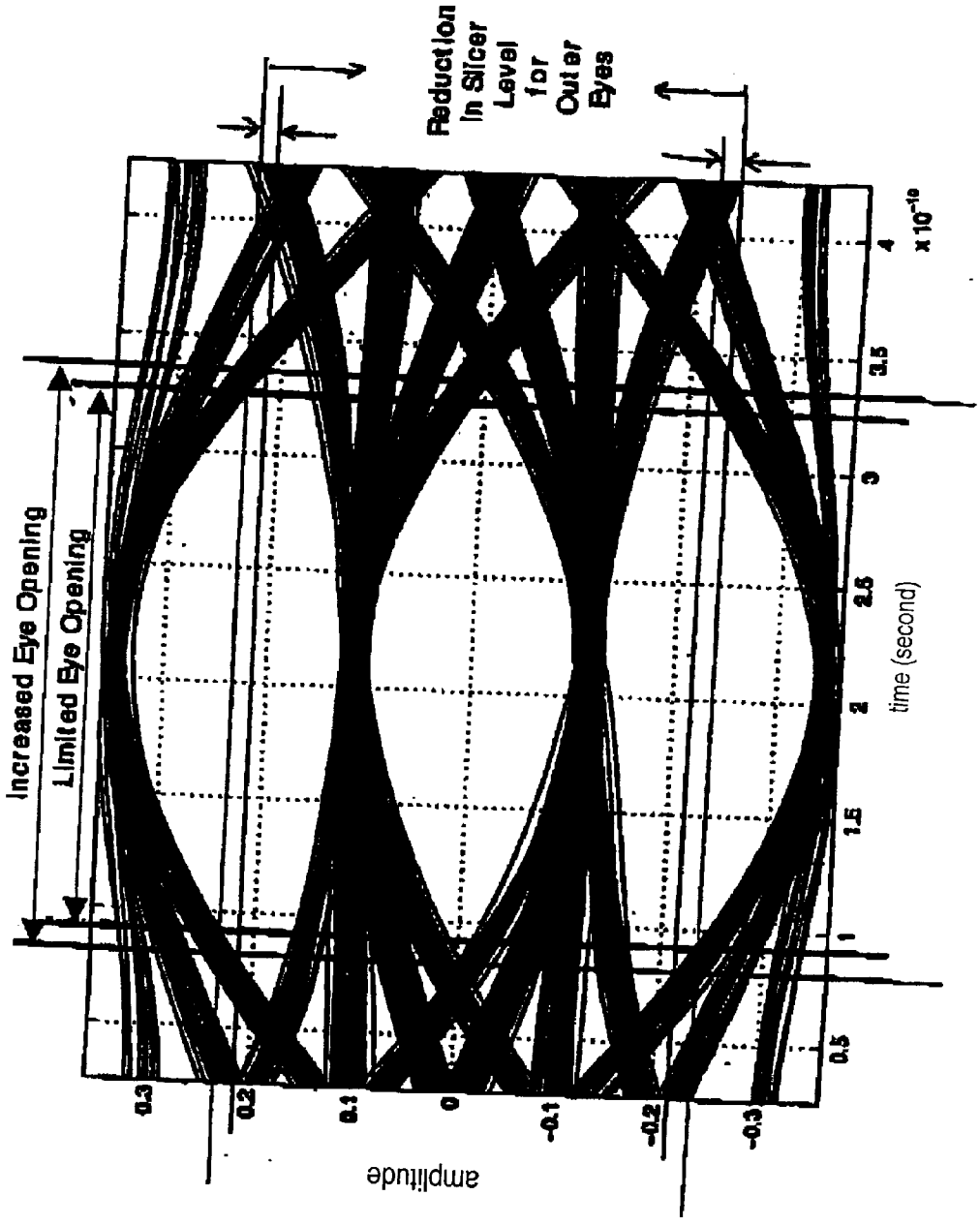

Reduction In Slicer Level for Outer Eyes
Increased Eye Opening
Limited Eye Opening
amplitude
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
0.5
1
1.5
2
2.5
3
3.5
4
x 10^-10
time (second)

FIGURE 7

SYSTEM AND METHOD FOR PROVIDING SLICER LEVEL ADAPTION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application Serial No. 60/313,455, entitled "Automatic Slicer Level Adaption", filed Aug. 20, 2001, and U.S. Provisional Application Serial No. 60/313,214, entitled "Transceiver Apparatus and Method", filed Aug. 17, 2001. The contents of these provisional applications are incorporated, in their entirety, by reference herein.

[0002] This application is related to U.S. Provisional Patent Application Serial No. 60/313,454, entitled "Transceiver System for High Speed Digital Signaling", filed Aug. 20, 2001 (Docket No. 13764.1-US-P1); U.S. Provisional Patent Application Serial No. 60/313,456, entitled "Variable Rate Sub-Channel Using Block Code RDS", filed Aug. 20, 2001 (Docket No. 13764.3-US-P1); U.S. Provisional Patent Application Serial No. 60/313,478, entitled "Variable Delay FIR Equalizer for Serial Baseband Communications", filed Aug. 20, 2001 (Docket No. 13764.4-US-P1); U.S. Provisional Patent Application Serial No. 60/313,477, entitled "Crosstalk Management for High-Speed Signaling Links", filed Aug. 20, 2001 (Docket No. 13764.5-US-P1); and U.S. Provisional Patent Application Serial No. 60/313,476, entitled "Method and Apparatus for Encoding and Decoding Digital Communications Data", filed Aug. 20, 2001 (Docket No. 13764.6-US-P1). The aforementioned applications are hereby incorporated by reference herein.

[0003] This application is also related to non-provisional patent applications that claim priority to one or more of the above-referenced provisional patent applications. These non-provisional patent applications are entitled "System and Method for High Speed Digital Signaling", filed Aug. 16, 2002 (Docket No. 209.001-US); "System and Method for Embedding a Sub-Channel in a Block Coded Data Stream", filed Aug. 16, 2002 (Docket No. 209.003-US); "System and Method for Providing Variable Delay FIR Equalizer for Serial Baseband Communications", filed Aug. 16, 2002 (Docket No. 209.004-US); "System and Method for Providing Crosstalk Management for High-Speed Signaling Links", filed Aug. 16, 2002 (Docket No. 209.005-US); and "Method and Apparatus for Encoding and Decoding Digital Communications Data", filed Aug. 16, 2002 (Docket No. 209.006US). The aforementioned non-provisional patent applications are hereby incorporated by reference, in their entirety, herein.

BACKGROUND OF THE INVENTION

[0004] This application relates in general to a method, apparatus, and article of manufacture for providing high-speed digital communications through a communications channel, and more particularly to a method, apparatus, and article of manufacture for providing slicer level adaption for a high-speed digital communications system.

[0005] Digital communications systems are continuously increasing the transfer rate at which data is transmitted between devices through a communications channel, for example, a backplane. One technique for increasing the data transfer rate is to encode the data prior to transmission. In this regard, there are a number of techniques for encoding data. Many of these techniques utilize different numbers of signals and modulation of symbols in order to increase the data transfer rate. One such method of modulating symbols is to use a multi-level pulse amplitude modulation (PAM-n) scheme that encodes a plurality of bits of data into or onto a single signal in which the symbols are represented as a set of signal levels between minimum and maximum signal levels.

[0006] In order to properly decode the received signal to thereby recover the digital representation of the data bits being transmitted, signal levels need to be set between the minimum and maximum signal levels that allow the transmitted symbol to be decoded properly. These are typically referred to as slicer levels.

[0007] In conventional systems, the slicer levels are an equal distance between adjacent signal levels. These levels are typically set during system design. As such, each signal level has an equal weight and is fixed. This slicer level scheme, however, may not provide a sufficient result from the perspective of a bit error rate of the system performance.

[0008] Accordingly, there exists a need to increase the performance of channel communications by, for example, providing a system and technique that includes an improved slicer level adjustment mechanism and technique.

SUMMARY OF THE INVENTION

[0009] The present invention relates in general to a method, apparatus, and article of manufacture for providing high-speed digital communications through a communications channel. In one aspect, the present invention employs an automatic slicer level adaption to enhance the performance of the system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] In the course of the detailed description to follow, reference will be made to the attached drawings. These drawings show different aspects of the present invention and, where appropriate, reference numerals illustrating like structures, components and/or elements in different figures are labeled similarly. It is understood that various combinations of the structures, components and/or elements other than those specifically illustrated are contemplated and within the scope of the present invention.

[0011] **FIG. 1** illustrates an exemplary communications channel between two digital processing devices according to one embodiment of the present invention;

[0012] **FIG. 2** illustrates an exemplary communications channel according to one embodiment of the present invention;

[0013] **FIG. 3** illustrates a portion of a communications channel implementing PAM-4 symbol encoding according to one embodiment of the present invention;

[0014] **FIG. 4** illustrates an idealized time-varying communications signal for a portion of a communications channel according to one embodiment of the present invention;

[0015] **FIG. 5** illustrates an embodiment of a voltage reference generation circuit, used by or implemented in a receiver, according to one embodiment of the present invention;

[0016] **FIGS. 6A and 6B** illustrate an embodiment of a reference generation circuit according to another aspect of the present invention; and

[0017] **FIG. 7** illustrates a signal receiver "eye" obtained using a reference generation according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0018] In the following detailed description of exemplary embodiments of the invention, reference is made to the accompanied drawings, which form a part hereof, and which is shown by way of illustration. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and other changes may be made, without departing from the scope of the present invention. The following description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

[0019] Throughout the specification and claims, the following terms take the meanings explicitly associated herein, unless the context clearly dictates otherwise. The term "connected" means a direct connection between the items connected, without any intermediate devices. The term "coupled" means either a direct connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, or data signal. The term "module" means a circuit (whether integrated or otherwise), a group of such circuits, a processor(s), a processor(s) implementing software, or a combination of a circuit (whether integrated or otherwise), a group of such circuits, a processor(s) and/or a processor(s) implementing software.

[0020] **FIG. 1** illustrates an exemplary communications channel between two digital processing devices according to one embodiment of the present invention. Digital processing devices **101** and **102**, such as personal computers, communicate with each other by transmitting digital signals through communications channel **100**. In one embodiment, a digital representation of the data to be transmitted is encoded and transformed into an electronic signal capable of passing through communications channel **100**. The electronic signal is transmitted by transmitter **110** to receiver **111**. The received signal, which may be distorted relative to the signal transmitted into channel **100**, is processed and decoded (by the receiver **111**) to reconstruct a digital representation of the information sent by the transmitting or sending device (i.e., the transmitter **110**).

[0021] The communications channel **100** may be, for example, constructed using one or more cables, wires, traces or the like, or may be part of a backplane, or may be a wireless communications medium through which the signal passes from transmitter **110** to receiver **111**. One skilled in the art will recognize that any such communications media, when used in conjunction with a corresponding transmitter/receiver pair appropriate for a particular medium, may be used to construct a communications channel in accordance with the present invention. For example, other channels that may be implemented in the present invention include electronic, optical or wireless. Indeed, all types of channels of communication (i.e., communication channels), whether now known or later developed, are intended to be within the scope of the present invention.

[0022] **FIG. 2** illustrates an exemplary communications channel according to one embodiment of the present invention. The communications channel **100** enables or facilitates transmission of information between associated pairs of transmitters and receivers, for example, transmitter **110** and receiver **111**. In one embodiment, transmitter **110** and receiver **111** employ a four level pulse amplitude modulated (PAM-4) communications technique to send two bits of data through channel **100**. That is, the transmitter/receiver pair is used to send two bits of data for each symbol transmitted through channel **100**. A ten bit word is loaded into parallel-to-serial register **211** with the output of the register being a two bit pair that is transmitted through the channel **100**. Once received, the sequence of two bit codes are loaded into serial-to-parallel register **212** to reconstruct or decode the ten bit word.

[0023] With reference to **FIG. 3**, in one aspect of the present invention, the PAM-4 communications technique transmits one of four signal values from transmitter **110** to a receiver **111**. The signal value represents a single communications symbol. The four signal values are used to encode the four possible combinations of values for two bits of digital data.

[0024] In operation, the data is sent through channel **100** by sending a sequence of symbols wherein each symbol is representative of two bits of data. The sequence of symbols is received by receiver **111**, separated into two bit groups that are reconstructed as output data **331** to allow the digital representation of input data (into the channel) to be extracted as output data (from the channel).

[0025] The communications system typically includes many sets of unidirectional transmitter and receiver pairs connected to communications channel **100**. These pairs simultaneously transmit data across channel **100** in both directions. Thus, from a system level perspective, there are many transmitter/receiver pairs in simultaneous operation, for example, eight or nine transmitter/receiver pairs communicating across a communications channel.

[0026] It should be noted that other communications mechanisms that use different encoding tables, other than four levels, may also be used. For example, PAM-5, PAM-8, PAM-16, CAP, wavelet modulation and other encoding rates such as 16B9Q or 9B5Q may be implemented in the present invention. The techniques described herein are in fact applicable to any and all modulation schemes, whether now known or later developed, including but not limited to PAM-4 encoding described herein.

[0027] **FIG. 4** illustrates an idealized time-varying communications signal for a single line from a communications channel. As data passes from transmitter **110** to receiver **111**, an idealized representation of the signal **400** is seen in or on channel **100**. Two bits of data are sent during each symbol time period **461**, which is defined to be a time period between a starting **462** and an ending **463** time for a symbol. The ending time **463** for a symbol is typically also the starting time for the next symbol. During a symbol time **461**, a particular channel value is observable in the channel **421**.

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[0028] The transmitter **110** sends one of four signal values, i.e. +3, +1, −1 or −3, during each symbol time **461**. The receiver **111** measures or observes the voltage during each symbol time period **461** to determine which of the four signal levels was sent by the transmitter **110**. For example, at time **461**, receiver **411** detects a symbol by detecting the voltage.

[0029] The receiver **411** determines or detects a particular symbol was transmitted when a voltage is detected between a particular maximum signal level and minimum signal level. These signal levels are typically centered around or on the particular symbol signal level. For example, if a bit pattern "01" is transmitted, a +3 signal voltage **441** is expected to be received. The receiver is expected to observe a signal level between a maximum value **442** and a minimum value **443** if the "01" bit pattern is to be recovered. Similar maximum value **452** and minimum value **453** are seen for a −1 signal level used for a bit pattern of "11".

[0030] It should be noted that the idealized time-varying waveform **400** does not illustrate the presence of any noise seen at the receiver. Additionally, the time-varying waveform shows instantaneous changes from one symbol voltage to a second symbol voltage at the start and end of a symbol time period **461**. As symbol communication rates increase, both noise and the rise and fall times for the symbols may become significant factors that limit the rate at which data may be communicated.

[0031] **FIG. 5** illustrates one embodiment of a reference generation circuit. The reference generation circuit of **FIG. 5** may be implemented in a receiver to recover the transmitted information. The reference generation circuit of this embodiment may be employed to set the slicing levels for the receiver front end, for example, a receiver implemented in a system employing a PAM-4 signaling technique.

[0032] With continued reference to **FIG. 5, a** set of resistors, R1-R6, are employed to obtain desired voltages between a maximum and minimum voltage level. In one embodiment, the circuit generates seven reference levels (V(0)-V(6)) for a seven level slicer. These voltages are "mapped" or correlated to the voltage levels in **FIG. 3**. For example, V(6) may be mapped to +3 (i.e., the maximum voltage level), V(5) to +2, V(4) to +1, V(3) to 0 (i.e., center or mid voltage level), V(2) to −1, V(1) to −2 and V(0) to −3 (i.e., the maximum voltage level).

[0033] Thus, in operation, levels V(5), V(3), and V(1) are used by the slicer to determine the value of a symbol. For example, if the signal that is sampled is greater than V(5)=2, the slicer determines that the sliced value was a +3. However, if the signal sample is greater than V(3)=0 and less than V(5)=2, then the slicer determines that the sliced value was a +1. Further, if the sliced sample is greater than V(1)=−2 and less than V(3)=0, then the slicer determines that the sliced value was a −1. Finally, if the sliced sample is less than V(1)=−2, then the slicer determines that the sliced value was a −3.

[0034] The other reference levels (i.e., V(0), V(2), V(4), V(6)) are set to additional slicing levels at the desired symbol values. These slicing levels are used to determine whether a given symbol is greater than or less than its desired value. For example, if a sliced value is greater than V(5) and greater than V(6), then the sliced value is determined to be a +3 and have a positive error (it was greater than the nominal signal level). If a sliced value is greater than V(5) and less than V(6) then the sliced value is determined to be a +3 and have a negative error (it was less than the nominal signal level).

[0035] This information may be employed in the adaptive equalization techniques described in the related applications. In addition, this information may be used to adjust the adaptive slicing levels as described below. Also, by changing the various resistor values R1-R6, other voltage V(0)-V(6) levels may be obtained. It should be noted that the operational amplifier maintains the common mode of the references, V(3), at Vref.

[0036] It should be further noted that more or less levels and other mappings or correlation relationships may be implemented. For example, the present invention may be implemented in any PAM system, including, for example, PAM-5, PAM-8 and PAM-16. Indeed, as mentioned above, the present invention may be implemented in CAP and wavelet modulation, among others.

[0037] **FIGS. 6A and 6B** illustrate a reference generation circuit according to another embodiment of the present invention. The reference generation circuit of this embodiment may be particularly well suited to slice PAM-4 signals. This module may be implemented as part of the automatic slicer level (ASL) module. The ASL module is used to automatically adjust the analog voltage reference levels of a slicer. The inputs to the ASL module are measurements (digital values) from the slicer. The outputs of the ASL module are the analog reference voltages for the slicer.

[0038] In operation, a digital section of the ASL module accepts signals sampled by the receiver. These samples indicate the sign of the recovered data (sign[d(n)]) as measured from slicing levels set by reference voltages (V(1), V(3) and V(5)) and the sign of the error relative to the ideal symbol value (sign[e(n)]) as measured from slicing levels set by reference voltages (V(0), V(2), V(4) and V(6)). This information may be used to measure whether the slicing levels are optimally or properly set. For example, optimal or proper slicing levels may be set to have the levels for V(0), V(2), V(4) and V(6) set at the average values of the corresponding input four data signal levels.

[0039] In one embodiment, the measurement of where the slicing levels are located, positioned or selected with respect to the input signal levels is accomplished by multiplying sign[d(n)]×sign[e(n)] and summing these products over a sequence of many periods (for example, over a sequence of 64, 128, or 255 periods), where each period consists of a number of symbols (for example, five symbols). During this initialization, adjustment or calibration process, if this sum is positive, then the incoming signal level is larger than the slicing levels, and the reference voltages (V(0)-V(6)) should be increased. However, if the sum is negative, then the incoming signal level is smaller than the slicing levels, and the reference voltages (V(0)-V(6)) should be decreased.

[0040] In one preferred embodiment, the sign of the resulting sum is used to control a 10-bit up/down counter in the digital portion of the ASL as indicated below. With reference to **FIG. 6A**, with N=10, the 10-bit up/down counter forms the input, Din, for the ASL analog circuit that generates analog voltage reference levels. The 10-bit up/down counter

varies the peak to peak range of the analog voltage reference levels over a range designed to span at least 250 mV to 500 mV across all process corners. Each digital step in the up/down counter corresponding to a 244 μV change in the peak-to-peak analog reference voltage range. This is represented in the following equation with μ_{asl}=244 μV.

$\mu_{asl} \times sgn[\Sigma sgn(e(n)) \cdot sgn(d(n))]$, for n=1 to N, where $N \cong 64$, 128, or 255.

[0041] It should be noted that other embodiments may be implemented to sum the value or some other mapping techniques of the summed values may be employed. In a preferred embodiment, each change to the digital control word is followed by a waiting period to allow the analog part of the ASL circuit time to settle to its new value before repeating the summation procedure. This adjustment or calibration process is called "ASL Adaption".

[0042] In a preferred embodiment, the adjustment or calibration process (i.e., the ASL Adaption process) runs continually and, as such, the ASL is always tracking or adapting to input signal amplitude(s). However, the ASL Adaption process may also be performed periodically or intermittently to, for example, reduce power consumption.

[0043] Moreover, the ASL Adaption process may be performed at or on a request of the user or a higher layer system function. In this regard, the process of adapting the ASL to, for example, input signal amplitude(s) may be enable or disabled based on a number of considerations, for example, power consumption.

[0044] The ASL Adaption process may also be performed at startup during an initial adjustment or calibration process. This process may be part of a system initialization sequence. Once the initial adjustment or calibration process is complete, the ASL Adaption process is disabled entirely or until the system detects a change in the operating environment (for example, a change in the temperature and/or supply voltage) or operating characteristics (for example, BER and/or operating conditions of the adaptive equalizer) of, for example, the transceivers and/or the communications channel. Thereafter, the initial adjustment or calibration process may be performed again, or may be performed periodically or intermittently, or not at all.

[0045] In one preferred embodiment, the digital section of the ASL module is responsive to two control signals. The first control signal controls the adaption process. When it is asserted, the ASL Adaption operates as described above. When the signal is not asserted, the ASL holds, suspends or maintains its up/down counter at the current value, which in turn holds or maintains the analog voltage reference levels.

[0046] The second control signal, when asserted, resets the ASL up/down counter to a default or predetermined value. In a preferred embodiment, the default or predetermined value of 749 (out of 1024) corresponds to a peak-to-peak analog reference voltage of approximately 450 mV. The second control signal has precedence over the first control signal in the preferred embodiment.

[0047] In one embodiment, the difference between the top and bottom references voltage levels of the ASL is a linear function of the digital input word, i.e., V(6)−V(0)=$_{\mu asl}$*Din+minimum_level, where μasl is a scale factor. Thus, if Din is 0, then V(6)−V(0)=minimum_level. If Din is all ones, then V(6)−V(0)=(2^N−1)μ_{asl}+minimum_level. Other embodiments could use different scalings of the digital word, including but not limited to logarithmic, square law, and exponential.

[0048] With reference to **FIG. 5**, in one embodiment, the reference voltage generation portion of the ASL module includes the characteristics of: V(6)−V(0)=l*6*(R/6)=lR. The current labeled "l" is the current output of a DAC whose digital input is Din, the output of the up/down counter. By varying Din, the current output of the DAC (i.e., "l") is varied, and thus the range V(6)-V(0) is varied. The operational amplifier at the bottom of the resistor string keeps the center reference at a desired common mode.

[0049] With reference to **FIG. 6**B, in another embodiment of the present invention the ASL module is configured such that level 5 and level 1 are shifted towards the center level (i.e., center or mid voltage level), level 3 in this embodiment, by ΔR %. One advantage of this arrangement is that shifting the slicer levels may improve the Bit Error Rate ("BER") of the transceiver in, for example, environments with relatively large levels of phase noise and timing jitter. In this embodiment, the ΔR % offset may be accomplished by changing the resistor values, as illustrated in **FIG. 6B**. The offset may also be implemented in other ways, for example, by reducing the resistance introduced by R3 and R4.

[0050] In another embodiment, the shift of level 1 and level 5 towards the center level is not uniform. In this regard, under certain conditions and/or in certain environments, the performance of the system may be enhanced by shifting level 1 and level 5 (towards the center level) by differing amounts. For example, level 5 may be shifted more towards the center level than the shift of level 1. Thus, a system having the capability of adjusting level 1 and level 5 differently (with or without feedback of the impact on the other levels) may accommodate situations in which the coding produces asymmetry in the "eye" openings from the perspective of the signal received and/or recovered by the receiver.

[0051] This embodiment may be implemented by changing the resistor values of R1, R2, R5 and R6 differently so that one level (i.e., reference voltage) is adjusted more than another. In this way, the ΔR % is not equal.

[0052] It should be noted that levels other than levels 1 and 5 may be shifted in a manner to enhance the performance of the system. In this regard, level 3 (i.e., center voltage level) may be adjusted by changing Vref. This type of configuration may also improve system performance in certain environments and/or under certain conditions.

[0053] It should be further noted that in the configuration described immediately above, the adjustment of R3 and R4 need not be equal. By adjusting R3 and R4 differently, levels 2 and 4 can be set to different adjustments relative to level 3. In this way, the slicer levels may be adjusted to address, for example, asymmetric "eye" openings (when "eye" openings are considered from the view point of the receiver).

[0054] In another embodiment, one or more levels are selectively shifted in a manner to enhance the performance of the system. For example, level 1 is shifted or adjusted by changing one or more of the resistor values R1 to R6 while the other levels are not adjusted. That is, in this example,

levels 3 and 5 are unchanged while level 1 is adjusted. In another example, level 5 is shifted or adjusted and levels 1 and 3 are unchanged.

[0055] The location, positioning and determination of the slicing levels may be calculated using any of the techniques described above. Moreover, there are many other techniques for determining the slicing levels of the ASL. Thus, all techniques for determining these levels, whether now known or later developed, are intended to be within the scope of the present invention.

[0056] By shifting or adjusting one or more levels, the system has the capability of implementing many level shifting permutations in order to enhance the performance of the system for a given condition or environment. In this regard, other combinations of level shifts are possible, for example, levels 1 and 2 and/or levels 4 and 5 may be shifted. This also may be accomplished by selectively changing the resistance values of R1 to R6. In this way, the slicer levels may be adjusted to accommodate, for example, the encoding and transmission techniques that produce the asymmetric "eye" openings.

[0057] The amount or percentage of the shift of the aforementioned embodiments is also selectable or programmable. In one embodiment, a 2% or less shift may optimally enhance the performance of the system from the perspective of the BER. However, other values are also possible. In one embodiment, the amount to percentage of shift may range between 0% and 10% depending upon the needs or performance characteristics of the system for a given environment. In another embodiment, the percentage shift may be 0% to 5%. In other embodiments, the slicing levels for each level may vary between 0% and 15% to accommodate significant asymmetric disparities in the "eye" openings as observed at the receiver.

[0058] In another embodiment, the amount or percentage of the shift may also be predetermined and the levels of the slicer or the resistance of R1 to R6 may be preset or preprogrammed. In this way, the slicer adaption process provides the preprogrammed values into the ASL module, for example, during the initialization process. These values may also be "hardwired" permanently, semi-permanently or temporarily (i.e., until re-programmed) by way of a ROM, PROM, EPROM, EEPROM or the like (e.g., configuring the state of a certain pin or pins on the package).

[0059] In this embodiment, the "hardwired" values may be fixed to the values stored in, for example a ROM or EEPROM. However such values may also be fine tuned to enhance the system performance. In this regard, after (or during) the performance of an initialization or re-initialization process, the system may implement fine adjustments to the predetermined percentage of the shift to the levels or fine adjustments to the voltage levels of the slicer or the resistance of R1 to R6. The fine adjustments to the location, positioning and determination of the slicing levels may be accomplished using any of the techniques described above. Indeed, all techniques for determining these levels, whether now known or later developed, are intended to be within the scope of the present invention.

[0060] Using the above-mentioned embodiments, performance for the communications channel, as measured by the BER, may be improved. Moreover, the system may be more robust.

[0061] An "eye" diagram that is produced using one aspect of the present invention is illustrated in **FIG. 7**. In the "eye" diagram of **FIG. 7**, the upper and lower eye openings are wider than the center opening. The upper and lower openings are shaped somewhat like a banana (i.e., the upper opening is more curved on the top than it is on the bottom).

[0062] In contrast, if the slicer levels were centered vertically in each eye opening, as typical in conventional systems, the horizontal opening in the top and bottom eyes would be limited by the curve of the outermost traces. In fact, the horizontal opening of the upper and lower eyes would be less than the center eye.

[0063] Since the bit error rate performance is typically related to both the horizontal and vertical eye openings, the overall performance may be less than optimum or desired. In this regard, reducing the slicer levels for the outer two eyes by implementing $\Delta R \approx 2$ (i.e., a 2% change±0.2%) causes the horizontal opening to be increased, which may improve the overall BER performance.

[0064] It should be noted that the symbol coding used in generating the "eye" diagram of **FIG. 7** is described in U.S. Provisional Patent Application entitled "Method and Apparatus for Encoding and Decoding Digital Communications Data", filed Aug. 20, 2001 (Docket No. 13764.6-US-P1) and non-provisional patent application entitled "Method and Apparatus for Encoding and Decoding Digital Communications Data", filed Aug. 16, 2002 (Docket No. 209.005-US). As mentioned above, these applications are incorporated by reference herein in their entirety.

[0065] **FIG. 1** illustrates an example of a suitable operating environment in which the invention may be implemented. The operating environment is only one example of a suitable operating environment and is not intended to suggest any limitation as to the scope of use or functionality of the invention. Other well known computing systems, environments, and/or configurations that may be suitable for use with the invention include, but are not limited to, network equipment, backplanes, communications equipment, personal computers, server computers, hand-held or laptop devices, multiprocessor systems, microprocessor-based systems, programmable consumer electronics, network PCs, minicomputers, mainframe computers, distributed computing environments and data communication equipment that include any of the above systems or devices, and the like.

[0066] While the above embodiments of the present invention describe automatic slicer level adaption, one skilled in the art will recognize that the use of particular signal levels, particular modulation and/or encoding techniques, and particular resistor ratios are merely example embodiments of the present invention. It is to be understood that other embodiments may be utilized and operational changes may be made without departing from the scope of the present invention as recited in the attached claims.

[0067] As such, the foregoing description of the exemplary embodiments of the invention has been presented for the purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise circuitry or forms disclosed. Many modifications and variations, whether now known or later developed, are possible. It is intended that the scope of the invention be limited not with this detailed description, but rather by the claims appended hereto.

What is claimed is:

1. A reference generator circuit for a receiver module coupled to a digital communications channel, the reference generator circuit comprising:

a reference voltage generation module to generate an adjustable reference voltage within the receiver module;

an error measurement module, coupled to the reference voltage generation module, to determine an error signal value between a measured received signal and a desired signal; and

wherein the reference voltage generation module uses the error signal to control the magnitude of the adjustable reference voltage.

2. The reference generator circuit according to claim 1, wherein a range of voltage values corresponding to a received symbol are decoded as a particular symbol using a maximum reference voltage and minimum reference voltage; and

the maximum reference voltage and minimum reference voltage are adjusted using error statistics collected within the error measurement module using the incoming data stream.

3. The reference generator circuit according to claim 2, wherein adaption of the maximum reference voltage and minimum reference voltage is performed during an initialization process.

4. The reference generator circuit according to claim 2, wherein the statistics within the error measurement module are collected using the equation:

$\mu_{asl} \times \text{sgn}[\Sigma \text{sgn}(e(n)) \cdot \text{sgn}(d(n))]$, for $n=1$ to N where $N \geqq 64$, or 128, or 255.

5. The reference generator circuit according to claim 2, wherein adaption of the maximum reference voltage and minimum reference voltage is performed continuously, periodically, or intermittently.

6. The reference generator circuit according to claim 5, wherein the adaption of the maximum reference voltage and minimum reference voltage is selectively enabled or disabled.

7. The reference generator circuit according to claim 5, wherein the maximum reference voltage and minimum reference voltage reference magnitude are externally set to a predetermined value.

8. A reference generator circuit according to claim 5, where the spacing between reference levels is non-uniform.

9. The reference generator circuit according to claim 8, wherein a performance criteria for setting the non-uniformity between the range of voltage values is a measure of a bit-error rate (BER) for the receiver module.

10. The reference generator circuit according to claim 1, wherein the spacing between reference levels is non-uniform.

11. The reference generator according to claim 10, wherein the nonuniformity is asymmetric.

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