Exhibit C-12

Invalidity Claim Chart for U.S. Patent No. 11,032,111 (the "'111 Patent")
in view of Obviousness References

As detailed in the cover pleading, and in addition to the reasons set forth in C-01 – C-11, the claims of the '111 Patent are invalid under 35 U.S.C. § 103 based on the prior art references identified in these invalidity contentions, alone or in combination with the obviousness references cited below. As explained in the cover pleading, a person of ordinary skill in the art as of the claimed priority date of the '111 Patent would have been motivated to combine the prior art identified in these invalidity contentions with the obviousness references cited below.

Defendants reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the invalidity contentions.

U.S. Patent 11,095,271 to Kang et al. ("Kang") was filed on December 19, 2018, published December 12, 2019, and claims priority to Korean Patent Application 10-2018-0067061 filed on June 11, 2018. Kang qualifies as prior art under at least 35 U.S.C. § 102(a)(2) (AIA).

InfiniBandTM Architecture Specification Volume 2 Release 1.4 ("Infiniband") published November 16, 2016. InfiniBand qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

U.S. Patent 8,516,238 to Cornelius et al. ("Cornelius") was filed on June 30, 2011, published January 5, 2012, and claims priority to U.S. Provisional Application No. 61/360,436 filed on June 30, 2010, U.S. Provisional Application No. 61/360,432 filed on June 30, 2010, and U.S. Provisional Application No. 61/446,027 filed on February 23, 2011. Cornelius qualifies as prior art under at least 35 U.S.C. §§ 102(a)(1) and 102(a)(2) (AIA).

U.S. Patent Application 2003/0058959 to Rafie et al. ("Rafie"), published March 27, 2003. Rafie qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

U.S. Patent Application 2005/0232336 to Balakrishnan et al ("Balakrishnan"), published October 20, 2005. Balakrishnan qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

U.S. Patent 9,768,985 to Ciacci et al. ("Ciacci") was filed on January 1, 2016 and published on September 19, 2017. Ciacci qualifies as prior art under at least 35 U.S.C. §§ 102(a)(1) and 102(a)(2) (AIA).

WIPO Patent 13155160 to Fox ("Fox") was filed on April 10, 2013 and published October 17, 2013. Fox qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

U.S. Patent Publication No. 2014/0281067 ("Das Sharma") was filed on March 15, 2013, and published on September 18, 2014. Das Sharma qualifies as prior art under at least 35 U.S.C. § 102(a)(1)(AIA).

United States Patent No. 7,239,665 ("Mezer") was filed on November 24, 2003, and published on May 26, 2005. Mezer qualifies as prior art under at least 35 U.S.C. § 102(a)(1)(AIA).

PCI Express Base Specification Revision 3.1a ("PCIe 3.1a") was published on November 7, 2015. PCIe 3.1a qualifies as prior art under at least 35 U.S.C. § 102(a)(1)(AIA).

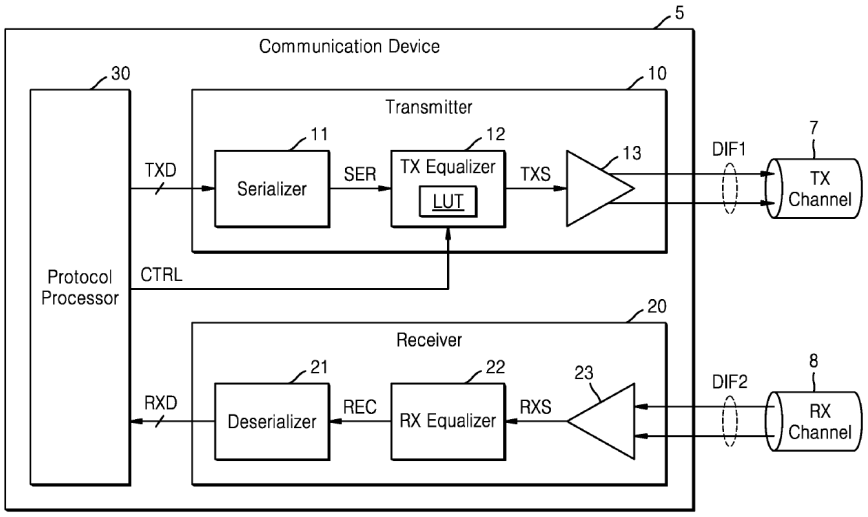
Texas Instruments – DS125DF410 Low-Power Multi-Rate Quad Channel Retimer ("TI DS125DF410") was published in February 2018. TI DS125DF410 qualifies as prior art under at least 35 U.S.C. § 102(a) (AIA).

Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer ("TI DS110DF111") was published in June 2015. TI DS110DF111 qualifies as prior art under at least 35 U.S.C. § 102(a) (AIA).

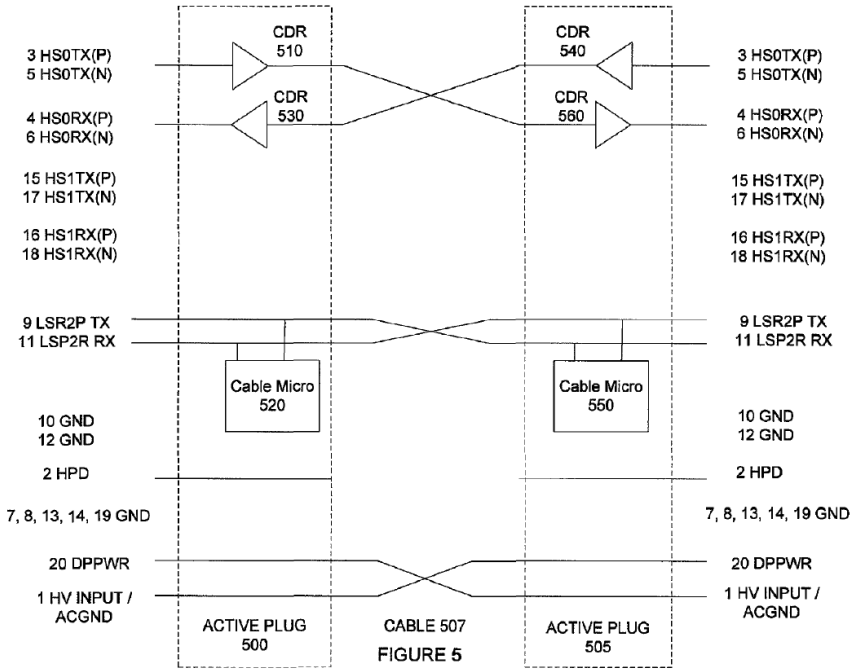
A. INDEPENDENT CLAIM 1

Claim 1	Disclosure
1[pre] A SerDes communications method that comprises, in a transceiver:	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "The disclosure relates to an equalizer, and more particularly, to an equalizer including a lookup table and a transmitter including the equalizer. In serial communication, an interconnection between a transmitter and a receiver, i.e., a channel, may distort signals. In order to compensate for distortion of signals generated in the channel, the transmitter and/or the receiver may include an equalizer. For example, the equalizer included in the transmitter may include a Finite Impulse Response (FIR) filter that provides an inverse transfer function of the transfer function of the channel. An equalizer including a high complexity filter may be necessary in order to precisely compensate for signal distortion while performing fast signal filtering for high speed serial communication. Further, in order to reduce power consumption and heat generation, an equalizer capable of reducing power consumption may be necessary." Kang, 1:13-30 "FIG. 1 is a block diagram illustrating a communication device **5** according to an exemplary embodiment of the disclosure. As shown in FIG. 1, the communication device **5** is capable of serial communication

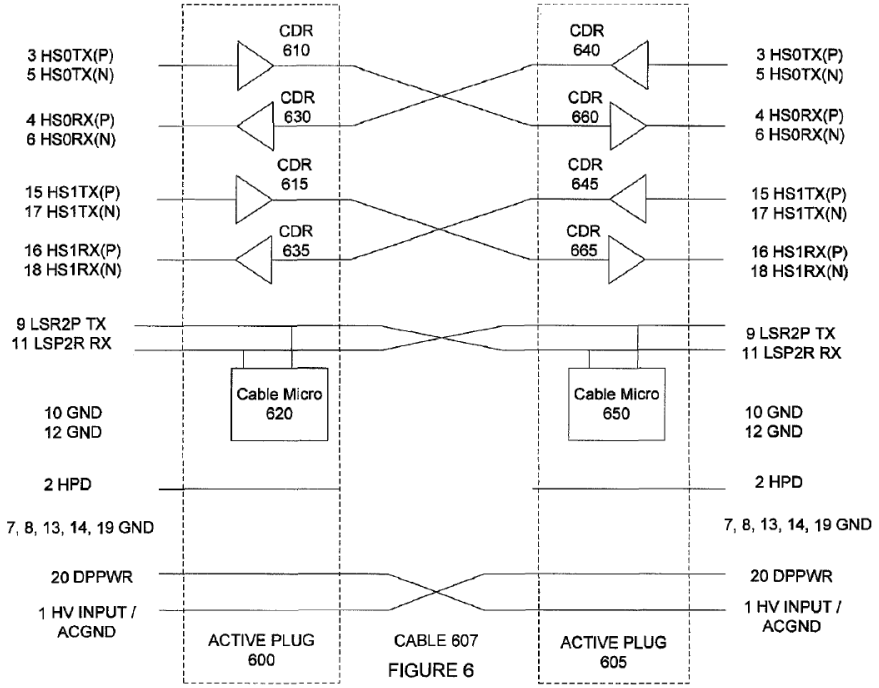
Claim 1	Disclosure
	with a counterpart communication device via a TX channel **7** and an RX channel **8**. Although FIG. 1 illustrates that the communication device **5** communicates with the counterpart communication device through a full duplex communication scheme, i.e., two channels (the TX and RX channels **7** and **8**), according to some embodiments, the communication device **5** may communicate with the counterpart communication device through a half duplex communication scheme, i.e., one channel. The TX channel **7** or the RX channel **8** may refer to interconnection between the communication device **5** and the counterpart communication device, and serial data signals DIF**1** and DIF**2** may transfer through the TX channel **7** and the RX channel **8**, respectively. For example, the TX channel **7** or the RX channel **8** may include at least one of a conductive line of an integrated circuit, a pattern of a printed circuit board (PCB), a connector, and a cable. The serial data signals DIF**1** and DIF**2**, which respectively pass through the TX channel **7** and the RX channel **8**, may be differential signals as shown in FIG. 1 in some embodiments, or may be single signals unlike what is illustrated in FIG. 1. The communication device **5** may refer to any device in serial communication with the counterpart communication device via the TX channel **7** and the RX channel **8**. In some embodiments, the communication device **5** may be a die included in a semiconductor package and may be in serial communication with a counterpart communication device included in the same semiconductor package. In some embodiments, the communication device **5** may be a semiconductor package mounted on a PCB and may be in serial communication with the counterpart communication device mounted on the same PCB or mounted on another PCB. In some embodiments, the communication device **5** may be a system (e.g., a storage, a computing system, etc.) including at least one semiconductor package and a PCB and may be in serial communication with other systems. As shown in FIG. 1, the communication device **5** may include a transmitter **10**, a receiver **20**, and a protocol processor **30**. In some embodiments, the transmitter **10** and the receiver **20** may be implemented as one block as a transceiver. The transmitter **10**, the receiver **20**, and the protocol processor **30** may provide a physical layer of communication and may be collectively referred to as a SerDes (serializer/deserializer) for serial communication." Kang, 3:17-65.

Claim 1	Disclosure
	FIG. 1  Kang, FIG. 1 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**. Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**.

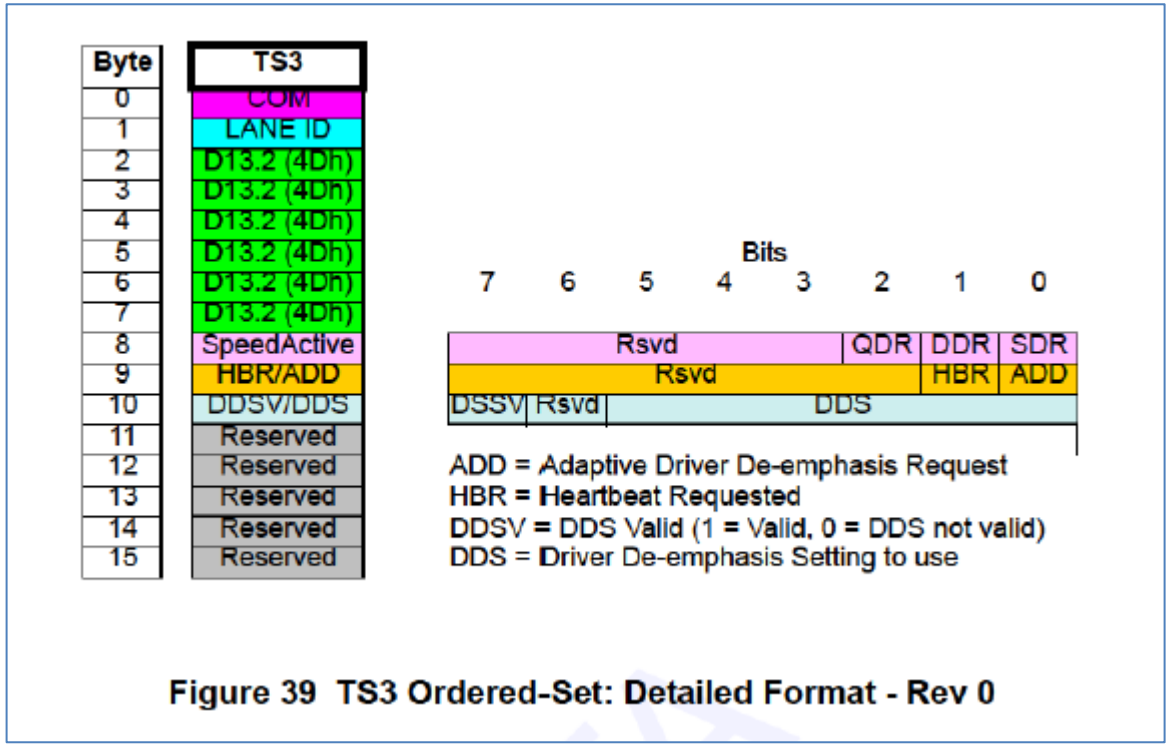
Claim 1	Disclosure
	The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables. In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used.

Claim 1	Disclosure
	In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5 "FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock

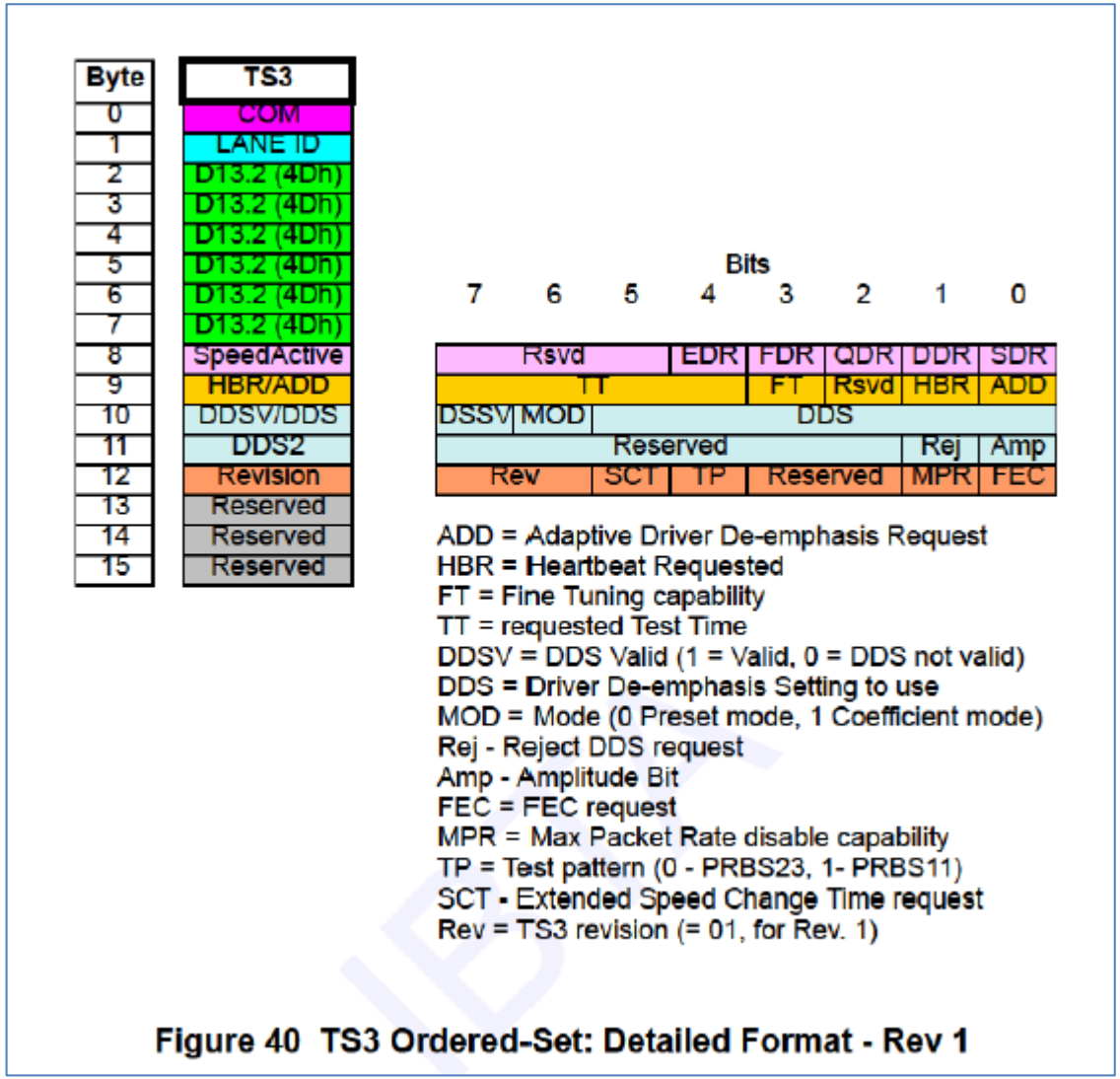
Claim 1	Disclosure
	and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 1	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 1	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 1	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 1	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

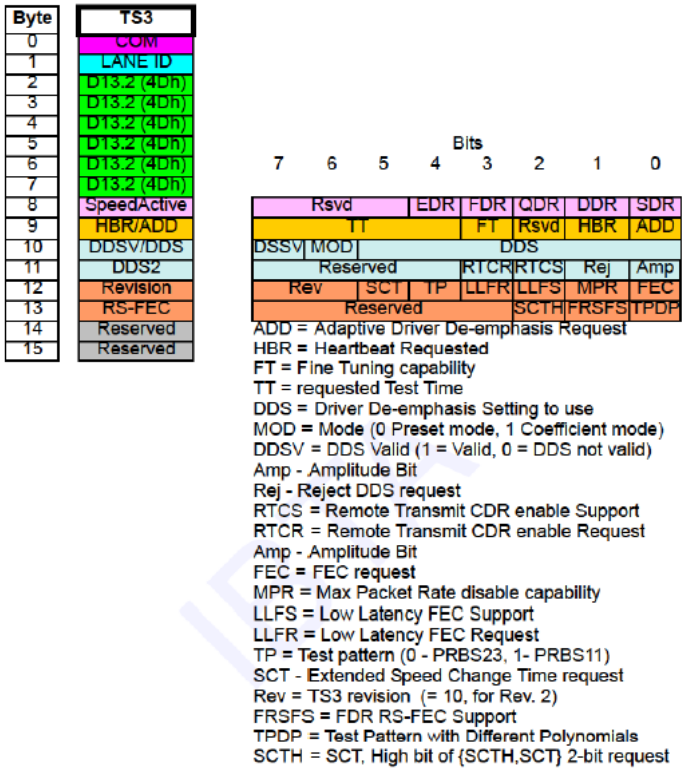
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 1	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 1	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 1	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 1	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 1	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 1	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 1	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 1	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

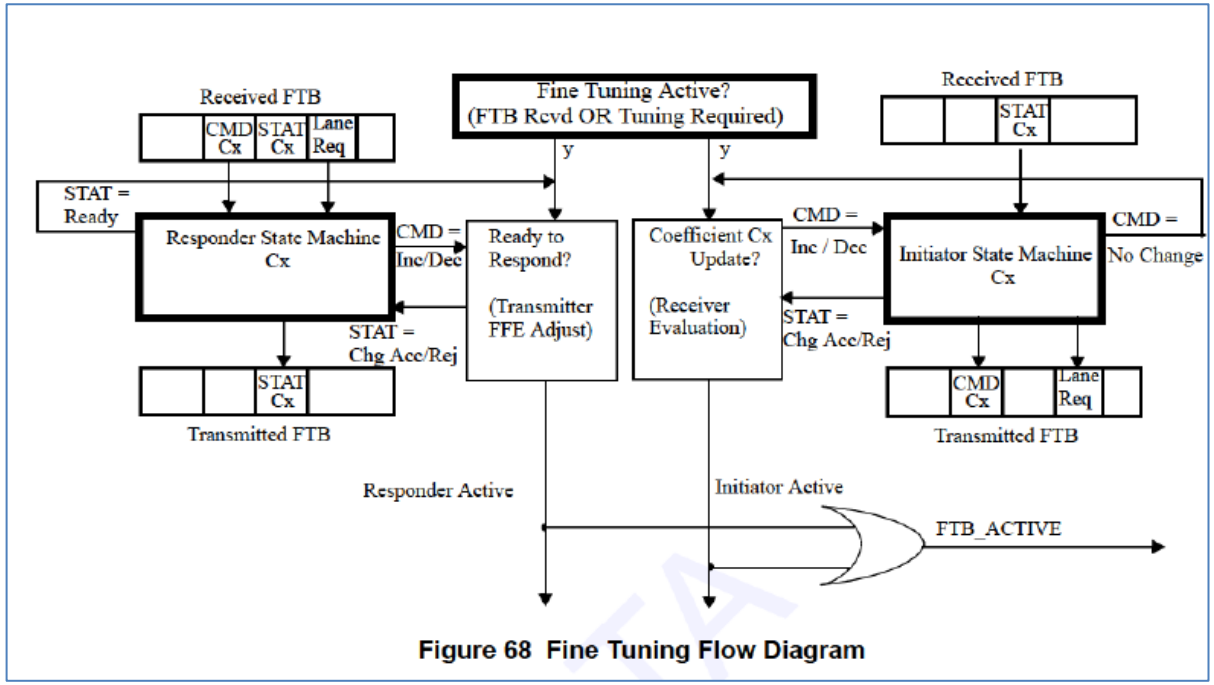
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 1	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 1	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 1	Disclosure

8.5 QSFP+ MEMORY MAP

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 1	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 1	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 1	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

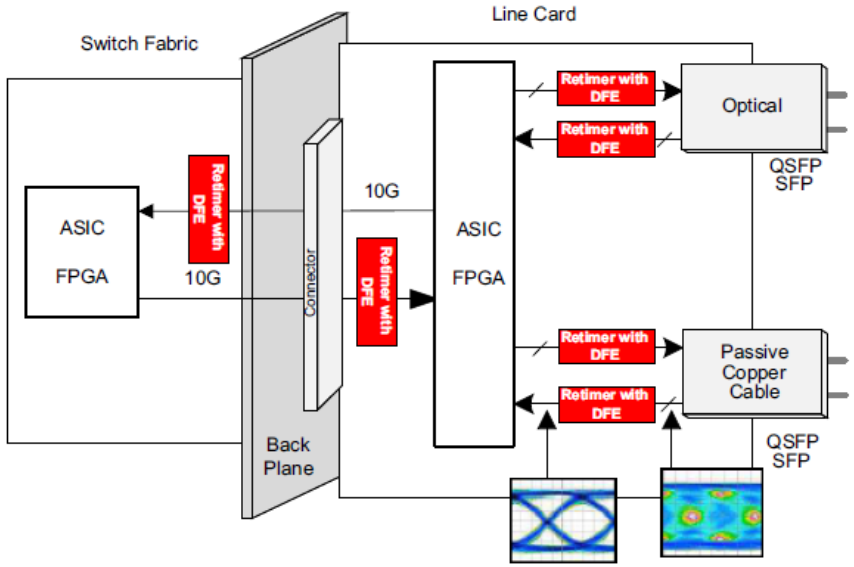
"To provide a high-performance radio link for high-speed systems employing spectrally-efficient modulation schemes, a reliable and robust transmitter radio link is required. Present embodiments of the current invention perform signal processing techniques to enhance the system performance and robustness of the transmitter portion of the transceiver."

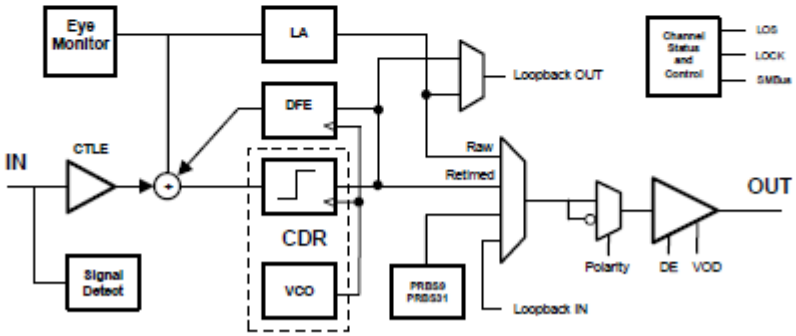
Rafie,¶ 47

"Various embodiments are directed toward a communication device that includes a transceiver circuit that is configured to communicate by generating an RF carrier signal of around 13.56 MHz as consistent with various RFID technologies, such as ISO/IEC standard 14443."

Claim 1	Disclosure
	Ciacci, 3:63–67. **1 Features** • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 1	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 1	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 1	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 1	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 1	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

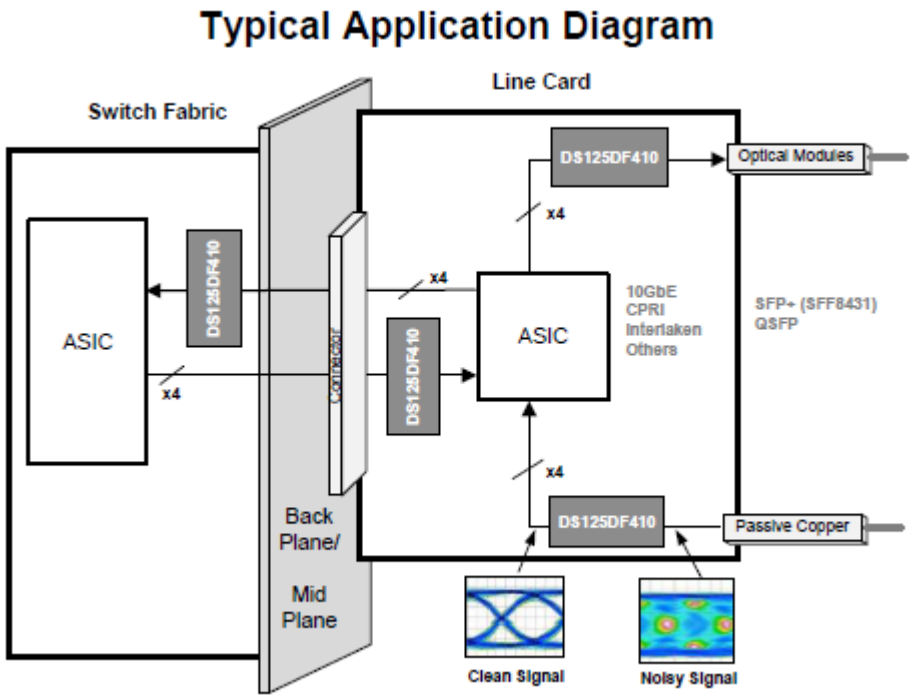
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

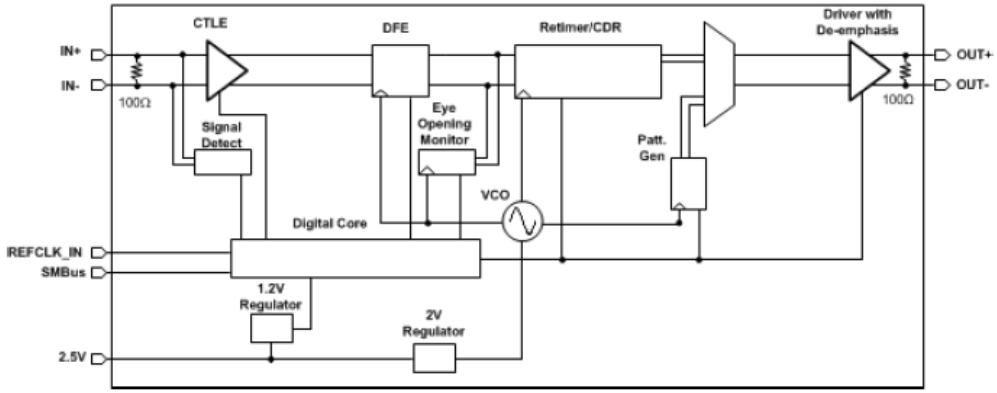
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 1	Disclosure
	 TI DS125DF410, 1.

Claim 1	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 1	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 1	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 1	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 1	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 1	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

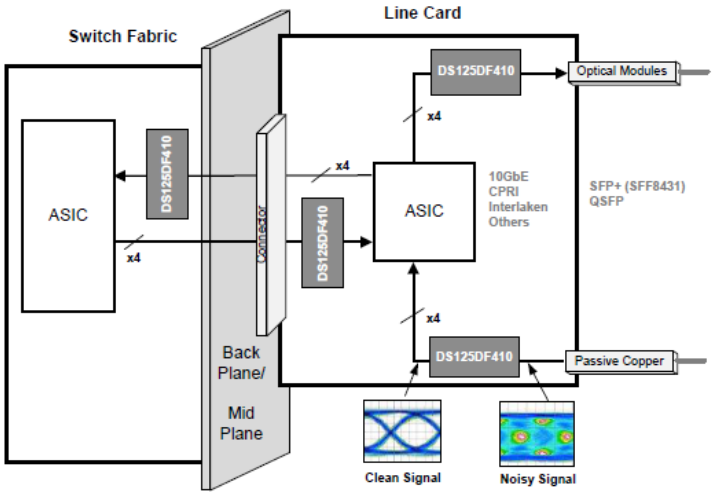
TI DS125DF410, 41.

Claim 1	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 1	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 1	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 1	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Claim 1	Disclosure
1[a] selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

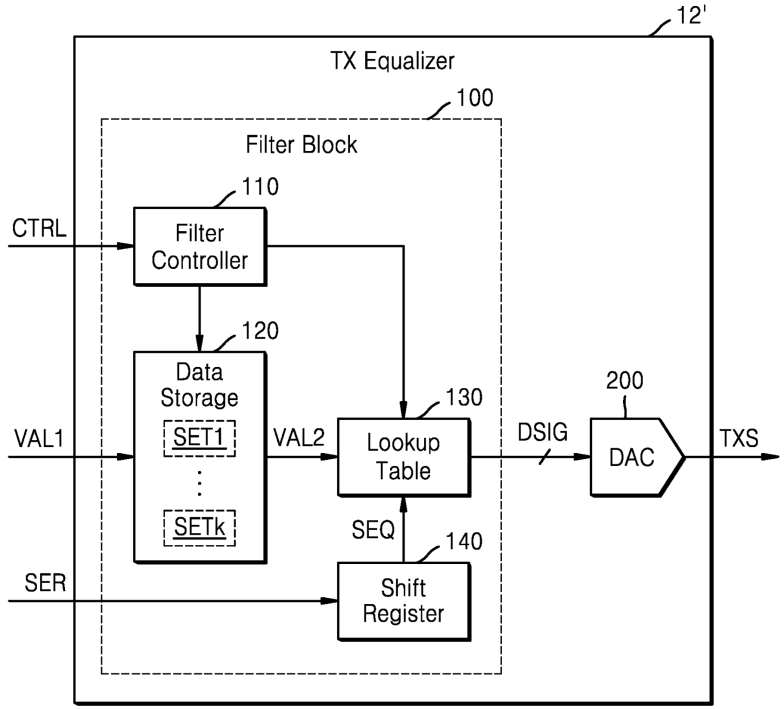
Claim 1	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal

Claim 1	Disclosure
	TXS, which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

Claim 1	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 1	Disclosure

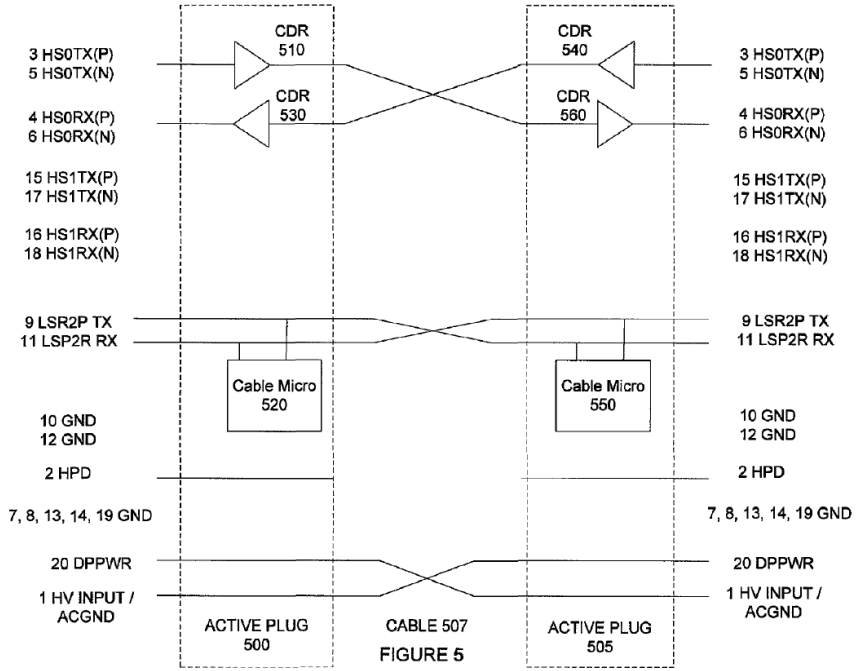
FIG. 3



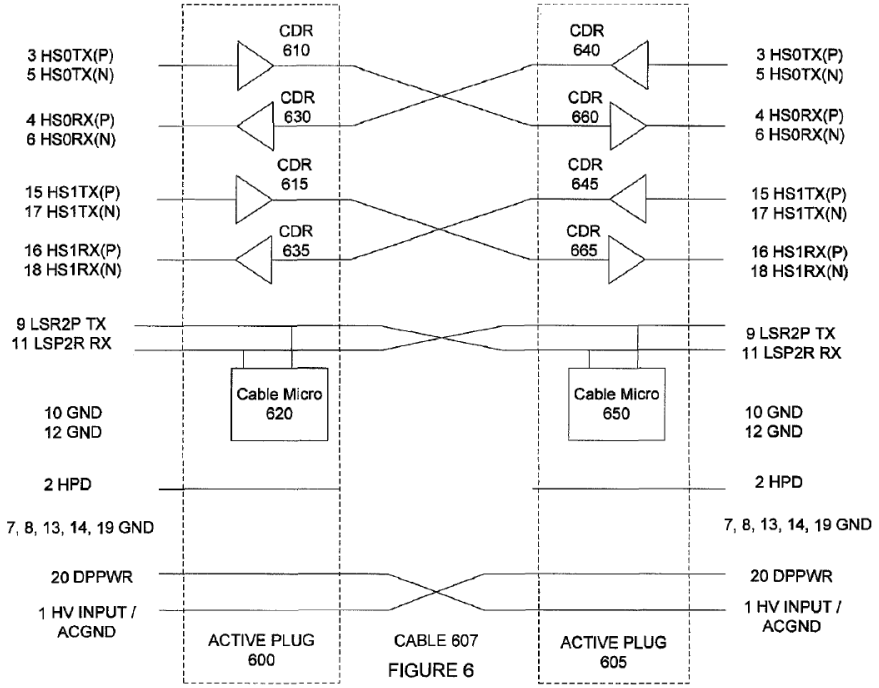
Kang, FIG. 3

"FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

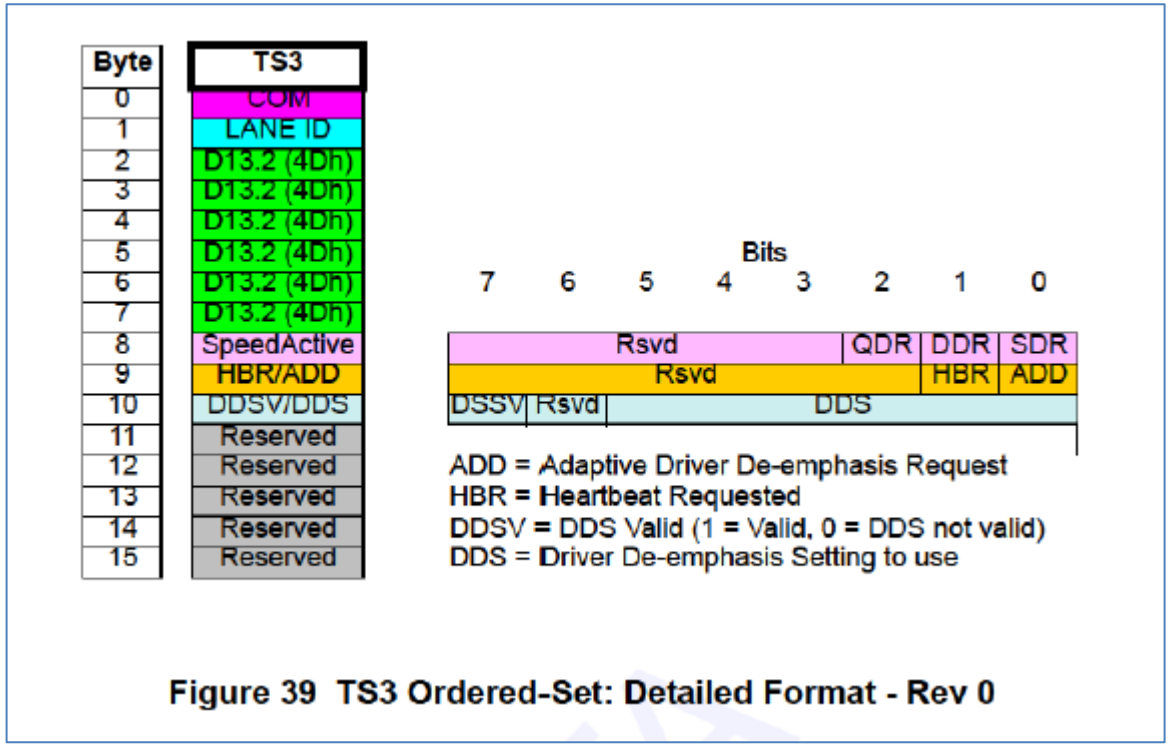
Claim 1	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 1	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

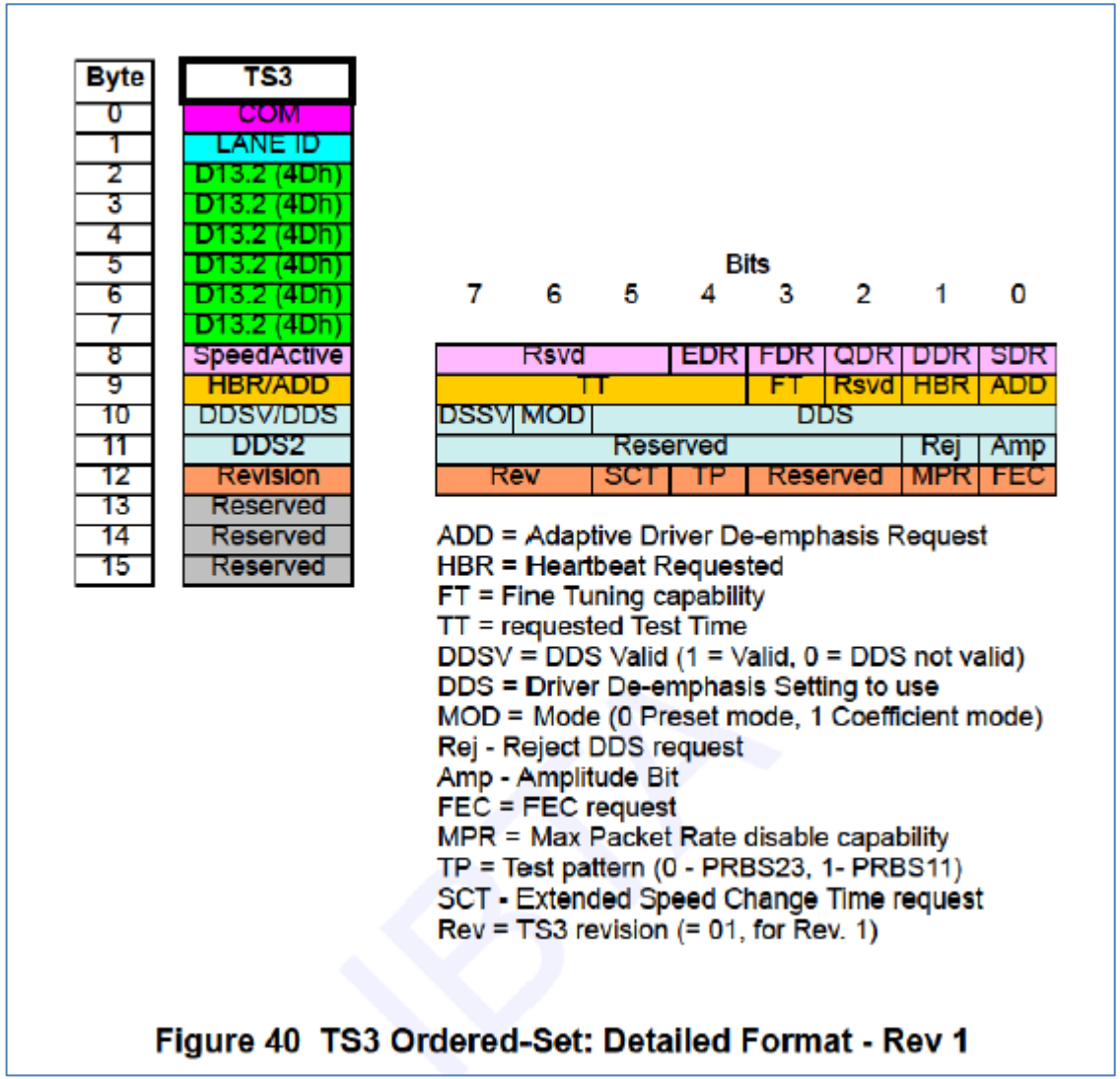
Claim 1	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 1	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 1	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 1	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 1	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

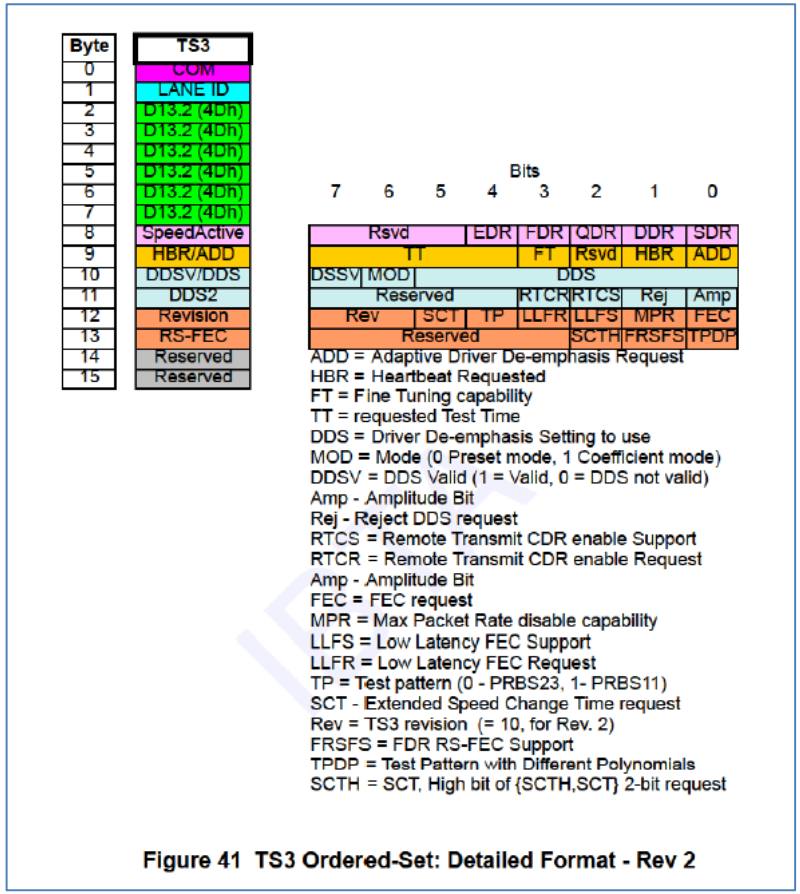
Bits	7	6	5	4	3	2	1	0
	Rsvd			EDR	FDR	QDR	DDR	SDR
	TT				FT	Rsvd	HBR	ADD
	DSSV	MOD	DDS					
	Reserved						Rej	Amp
	Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 1	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 1	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 1	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 1	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 1	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 1	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 1	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 1	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

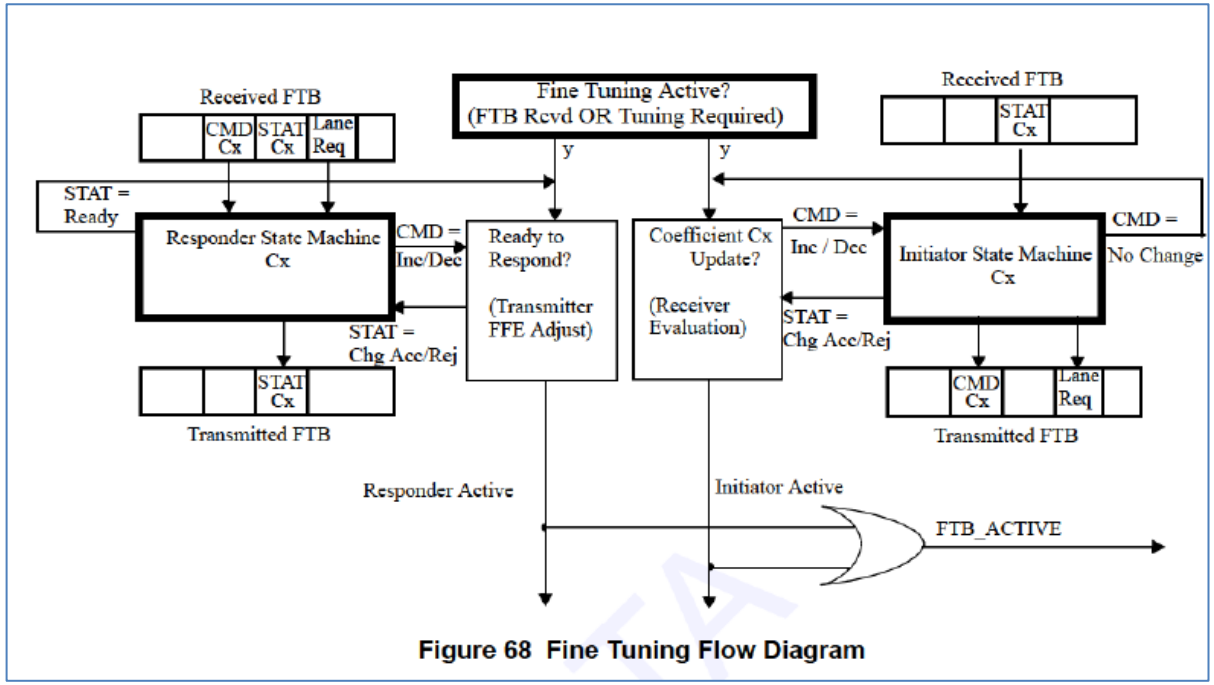
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 1	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 1	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 1	Disclosure

8.5 QSFP+ MEMORY MAP

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 1	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 1	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 1	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"The overall pre-equalizer **800** can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."

Rafie, paragraph 82.

"Digital pre-equalizer (PEQ) circuit **204** can be configured to introduce a distortion to the input signal to compensate for channel impairment. At power-on little or no information may be known about the channel. Accordingly, the digital PEQ circuit **204** can be initially configured with no distortion. In some

Claim 1	Disclosure
	embodiments, the digital PEQ circuit **204** can be initially configured with a distortion that is based upon a corresponding set of coefficients." Ciacci, 5:40-47. "Once frequency response of front-end components has been characterized, this information can be stored in the digital base band on a configuration register (CFR), and thereby used to specify gain coefficients of the digital pre-equalizer." Balakrishnan, paragraph 27. *U.S. Patent Publication No. 2014/0281067 ("Das Sharma")* It was well-known that equalization can be performed on the transmitter side (i.e., pre-equalization) and/or on the receiver side and it was a design choice where to perform equalization. *See, e.g.*, Das Sharma at [0085]. An ordinarily skilled artisan would use pre-equalization in a cable to ensure good cable performance irrespective of the host device with which the cable is used. *See, e.g.*, OIF-CEI-04.0, § 16.2.2 ("16.2.2 Transmitter equalizer function: Both host and module Tx FIRs are likely to be required to meet … eye requirements … for high loss channels."). A transceiver's pre-emphasis coefficients can be adjusted during a training phase. *See, e.g.*, Das Sharma at [0066], [0075]). A set of coefficients adjusted during the training phase are applied to FIR filters in the transceiver. *See id. at* [0079] (FIR filter uses adjusted coefficients). The "set of default coefficients located within registers" in the pluggable module transceiver. *See id*. at [0078], [0106]. The '111 Patent says that each channel model is provided based on assumptions of known or predicted link characteristics and that each channel model stores "default coefficient values" provided by the "the manufacturer of the pluggable module." *See, e.g.*, '111 Patent at 12:1-4, 12:54-13:8. That is precisely

Claim 1	Disclosure
	what the different sets of default coefficients for different channel types are. *See, e.g.*, Das Sharma at [0078] (describing default coefficients "provided by manufacturer"). The set of default coefficients that correspond to a channel having the parameters detected during the basic channel test, or the best performing set of coefficients, is *selected* and requested "from the configuration registers." *See, e.g.*, Das Sharma at [0155], Fig. 15. *United States Patent No. 7,239,665 ("Mezer")* Mezer discloses that equalization can be performed on the transmitter side (i.e., pre-equalization) and/or on the receiver side, and it was a design choice where to perform equalization. *See, e.g.*, Mezer at 5:41-55. Pre-equalization in the cable ensures good cable performance irrespective of the host device with which the cable is used. *See, e.g.*, OIF-CEI-04.0, § 16.2.2 ("16.2.2 Transmitter equalizer function: Both host and module Tx FIRs are likely to be required to meet… eye requirements… for high loss channels."). Mezer discloses that "various types of channels may be tested in advance to determine suitable [pre-equalizer] characteristics therefor, and when it is determined to which one of the channel types the computer system is coupled, the suitable [pre-equalizer] characteristic for that type of channel may be selected." *See, e.g.*, Mezer, 6:53-57; *see also id*. at 3:33-4:42 (describing the process for pre-computing the sets of coefficients), 4:24-26 (teaching "selecting one of the pre-computed equalizer characteristics" (i.e., sets of coefficients) "stored in the storage unit"), and 4:32-39 (describing a "lookup table" used "to select one of the pre-computed equalizer characteristics stored in the storage unit"). *PCIe 3.1a* The equalization procedure consists of up to four Phases, as described below. When operating at the 8.0 GT/s data rate, the Phase information is transmitted using the Equalization Control (EC) field in the TS1 Ordered Sets. Phase 0: The Downstream Port communicates the Transmitter preset values and the Receiver preset hints for each Lane to the Upstream Port using 8b/10b encoding. These values are communicated using the EQ TS2 Ordered Sets (defined in Section 4.2.4.1) in Recovery.RcvrCfg, when a data rate change to 8.0 GT/s has been negotiated, prior to transitioning to 8.0 GT/s data

Claim 1	Disclosure
	rate. These preset values are derived from the Upstream Port Transmitter Preset and Upstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. After the data rate change to 8.0 GT/s, the Upstream Port transmits TS1 Ordered Sets with the preset values it received. The preset values must be within the operable range defined in Section 4.3.3.5.2 if reduced swing will be used by the Transmitter. Phase 1: Both components make the Link operational enough at 8.0 GT/s data rate to be able to exchange TS1 Ordered Sets to complete remaining phases for the fine-tuning their Transmitter/Receiver pairs. It is expected that the Link will operate at a BER of less than 10^{-4} before the component is ready to move on to the next Phase. The Downstream Port initiates Phase 1 by transmitting TS1 Ordered Sets with EC=01b (indicating Phase 1) to the Upstream Port using the preset values in the Downstream Port Transmitter Preset and, optionally, the Downstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. The Upstream Port, after adjusting its Receiver, if necessary, to ensure that it can progress with the equalization process, receives these TS1 Ordered Sets and transitions to Phase 1 (where it transmits TS1 Ordered Sets with EC=01b). The Downstream Port ensures that it can reliably receive the bit stream from the Upstream Port to continue through the rest of the Phases when it receives TS1 Ordered Sets from the Upstream Port with EC=01b before it moves on to Phase 2. Phase 2: In this Phase the Upstream Port adjusts the Transmitter setting of the Downstream Port along with its own Receiver setting, independently, on each Lane, to ensure it receives the bit stream compliant with the requirements in Section 4.3 (e.g., all operational Downstream Lanes have a BER is less than 10^{-12}). The Downstream Port initiates the move to Phase 2 by transmitting TS1 Ordered Sets with EC=10b to the Upstream Port. The Downstream Port advertises the Transmitter coefficients and the preset it is using per the rules below in Phase 1 for preset only and in Phase 2 for preset and coefficients. The Upstream Port receives these Ordered Sets and may request different coefficient or preset settings and continue to evaluate each setting until it arrives at the best setting for operating the Downstream Lanes. After the Upstream Port has completed this Phase, it moves the Link to Phase 3 by transmitting TS1 Ordered Sets with EC=11b to the Downstream Port. Phase 3: In this Phase the Downstream Port adjusts the Transmitter setting of the Upstream Port along with its own Receiver setting, independently, on each Lane, using a handshake and evaluation process similar to Phase 2 with the exception that EC=11b. The Downstream Port signals the end of Phase 3 (and the equalization procedure) by transmitting TS1 Ordered Sets with EC=00b. PCIe 3.1a at 240-241.

Claim 1	Disclosure

4.3.3.5.2. Tx Equalization Presets

An 8.0 GT/s transmitter must support a specified number of presets, where the preset values are defined in terms of voltage ratios as illustrated in Figure 4-42. Presets are defined in terms of two ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GTs/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. Figure 4-42 is shown as an example of TxEQ and is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of 8.0 GT/s signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms, as shown later in this section.

The presets defined in Table 4-16 and Table 4-17 are numbered to match the designations in Section 4.2.3.1. Note, however, that in Section 4.2.3.1 the coefficients are defined as integers (using upper case "C"), while in the electrical section they are defined as floating point (using lower case "c").

PCIe 3.1a at 355.

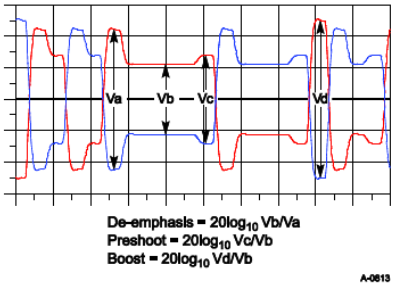
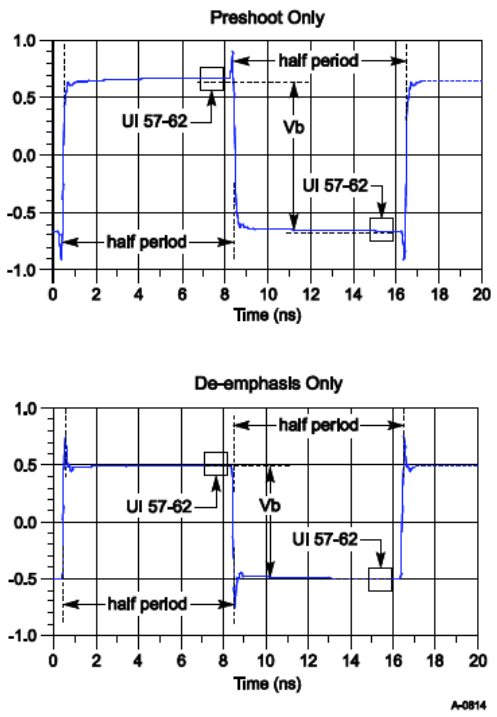


Figure 4-42: Definition of Tx Voltage Levels and Equalization Ratios

Figure 4-43 illustrates the waveforms that will be observed when measuring presets when using the 64-ones/64-zeroes sequence that is part of the compliance pattern. Depending on whether the preset implements de-emphasis, preshoot, or both the corresponding waveshape will differ. The two cases illustrated below show preshoot and de-emphasis, as can be observed by noting whether the boost occurs before or after each edge transition. For the case where both de-emphasis and preshoot are present, boost occurs both before and after each edge transition. Note that in all cases, however, the voltage of interest occurs during the flat portion (Vb) of the waveform, where it can be accurately measured independent of high frequency effects.

PCIe 3.1a at 356.

Claim 1	Disclosure
	 Figure 4-43: Waveform Measurement Points for Pre-shoot and De-emphasis PCIe 3.1a at 357.

Claim 1	Disclosure

Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

Notes:

1. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The allowable P10 boost range is defined by the coefficient space lying between the Min and Max Reduced Swing Limits as shown by the two diagonal lines in the example of Figure 4-45. This approach permits both full and reduced swing transmitters to use P10 for testing to their respective boost limits.

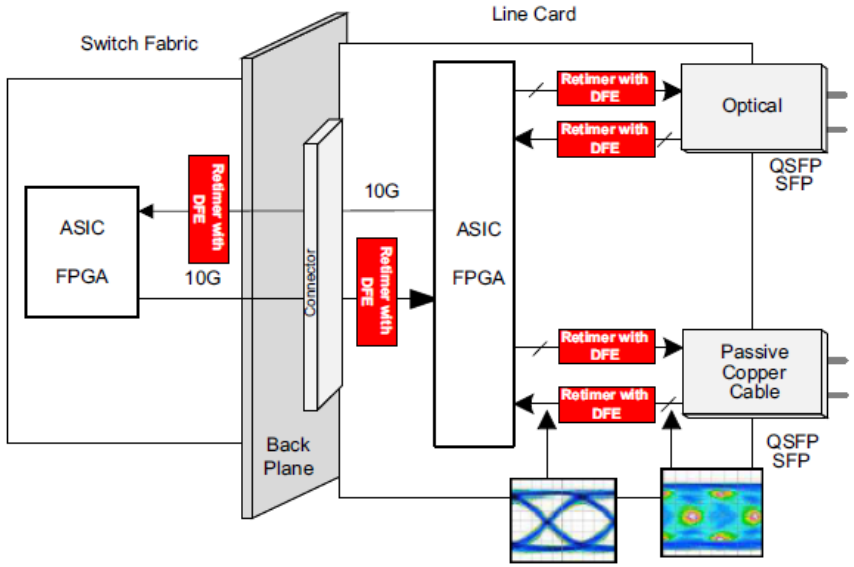
With the exception of P4 (for which both pre-shoot and de-emphasis are 0.0 dB) it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are 1 UI wide and therefore subject to attenuation by the package and the breakout channel. Instead the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval. Table 4-17 lists the preset values required to measure each of the Va and Vc values from which the preshoot or de-emphasis values may be derived.

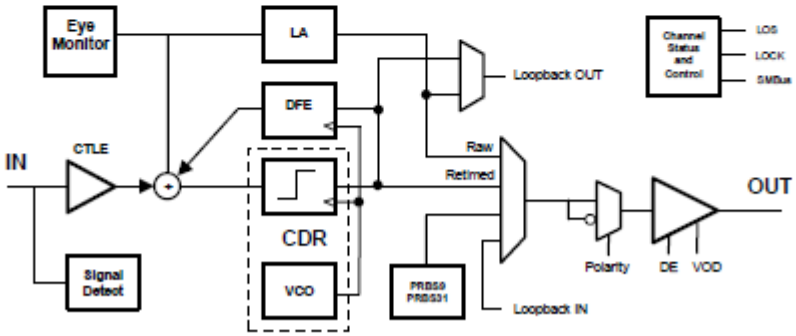
PCIe 3.1a at 358.

Claim 1	Disclosure
	Table 4-17: Preset Measurement Cross Reference Table **Preset Number** | **De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))** | **Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))** P4 | N/A | N/A P1 | P1/P4 | N/A P0 | P0/P4 | N/A P9 | N/A | P4/P9 P8 | P8/P6 | P3/P8 P7 | P7/P5 | P2/P7 P5 | N/A | P4/P5 P6 | N/A | P4/P6 P3 | P3/P4 | N/A P2 | P2/P4 | N/A P10 | P10/P4 | N/A PCIe 3.1a at 359.

Claim 1	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 1	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 1	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 1	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

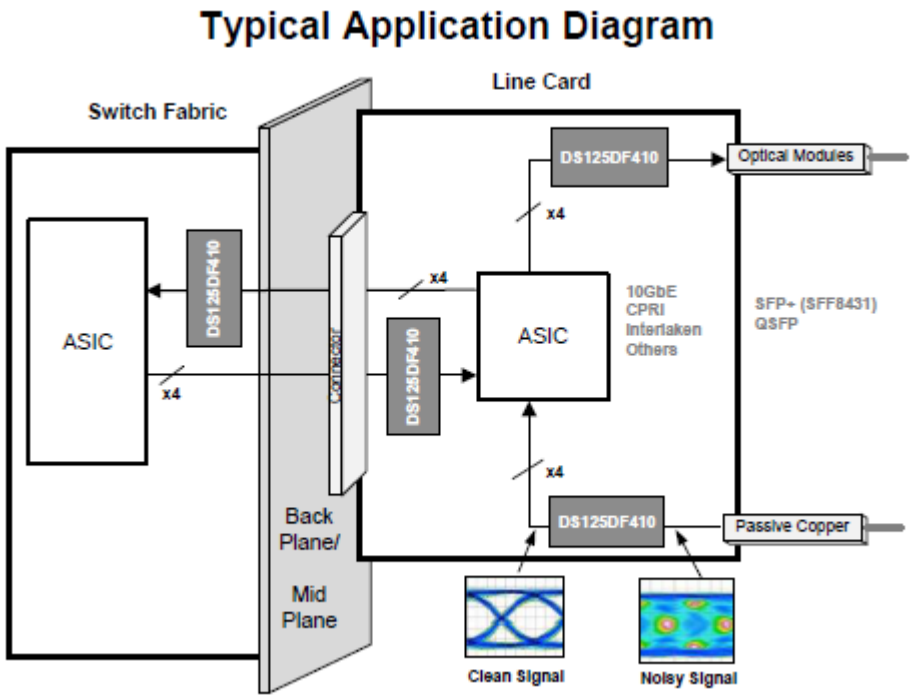
Claim 1	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 1	Disclosure
	7.5.1.26 Setting the Output De-Emphasis Setting *Register 0x15, bits 2:0 and bit 6* Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

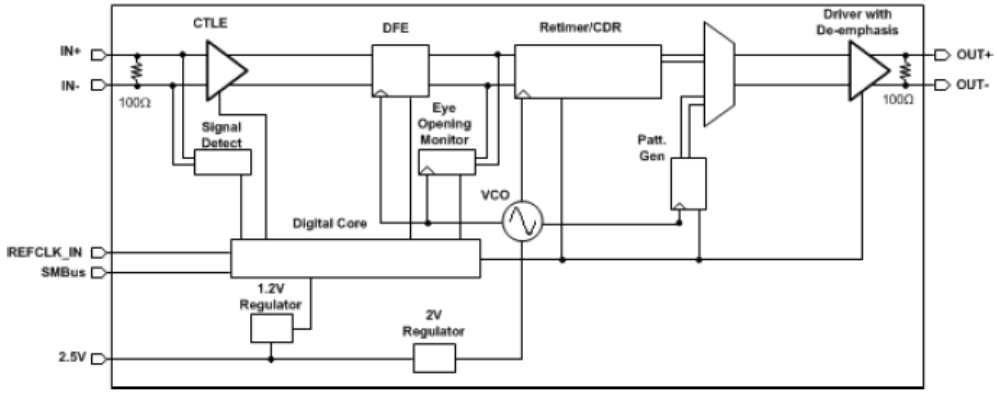
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 1	Disclosure
	 TI DS125DF410, 1.

Claim 1	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 1	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 1	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 1	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 1	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 1	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

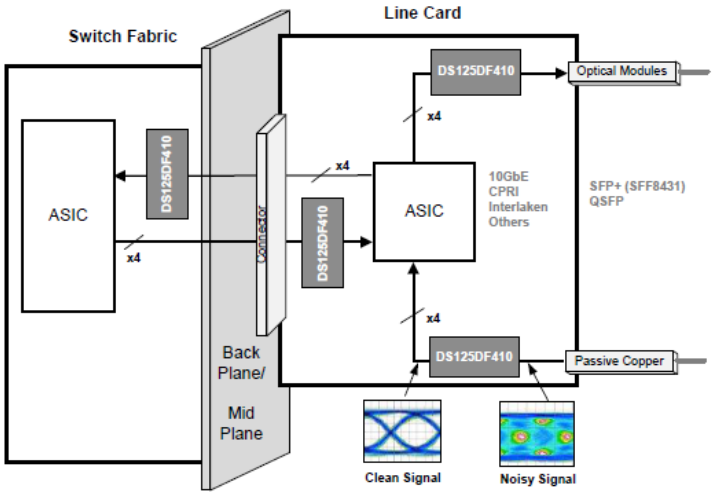
TI DS125DF410, 41.

Claim 1	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

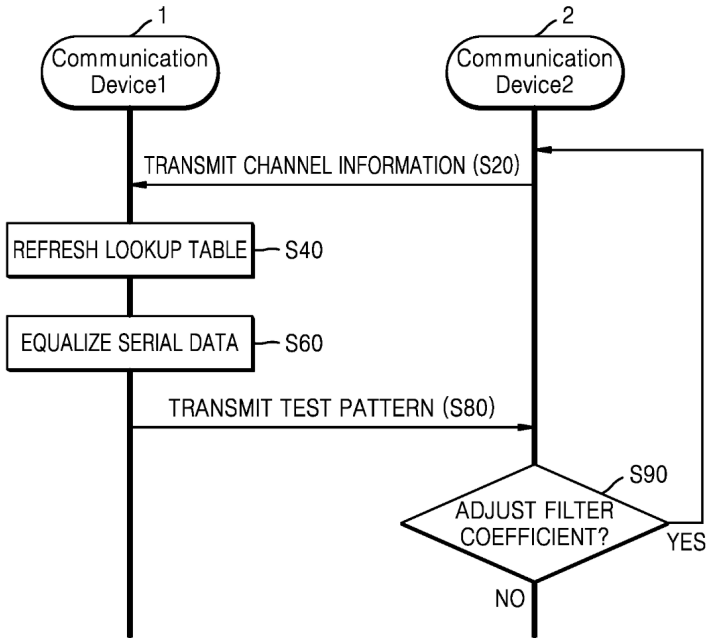
Claim 1	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 1	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

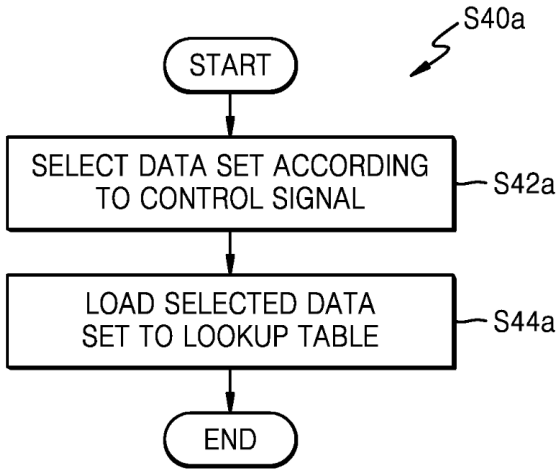
Claim 1	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

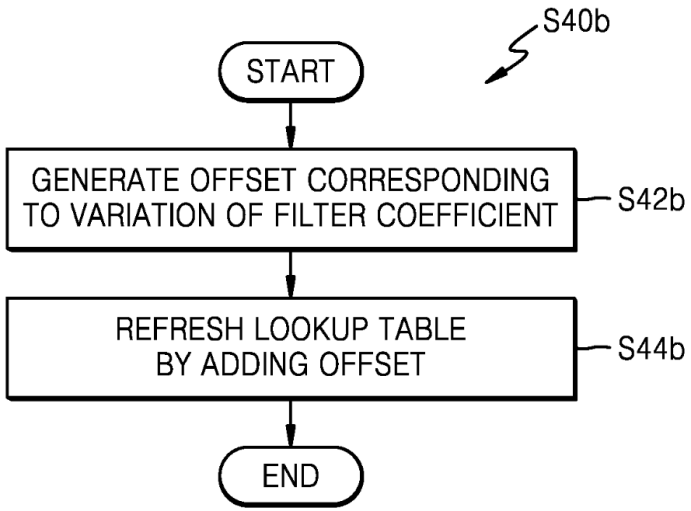
Claim 1	Disclosure
1[b] updating the initial pre-equalizer coefficient values during a training phase; and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "FIG. 10 is a diagram illustrating an equalization method over time according to an exemplary embodiment of the disclosure. For example, the equalization method of FIG. 10 may be performed by the first communication device 1 including the TX equalizer 12 of FIG. 1 and the second communication device 2 communicating with the first communication device 1. The filter coefficients for equalization may be determined according to the equalization method illustrated in FIG. 10, and the method for determining the filter coefficients may be referred to as training of filter coefficients. It is assumed below that the first communication device 1 of FIG. 10 includes the components of the communication device 5 of FIG. 1, and FIG. 10 will be described with reference to FIG. 1. Referring to FIG. 10, in operation S20, the second communication device 2 may transmit channel information. For example, the second communication device 2 may first transmit, to the first communication device 1, channel information including information indicating one of the plurality of data sets, as described above with reference to FIG. 3. In operation S40, the first communication device 1 may refresh the lookup table LUT. For example, the protocol processor 30 of the first communication device 1 may extract information indicating a data set

Claim 1	Disclosure
	from the channel information received in operation S20 and may transmit the control signal CTRL including the extracted information to the TX equalizer 12. TX equalizer 12 may refresh the lookup table LUT based on the control signal CTRL. The lookup table LUT may include values of the digital signal DSIG corresponding to possible values of the symbol sequence extracted from the serial data SER. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information indicating a data set will be described with reference to FIG. 11. In operation S60, the first communication device 1 may equalize the serial data SER. For example, in the TX equalizer 12 of the first communication device 1, the lookup table LUT may output a digital signal (e.g., DSIG in FIG. 3) corresponding to the symbol sequence of the serial data SER, and the DAC 200 included in the TX equalizer 12 may convert the digital signal into an analog signal. Accordingly, an adder and a multiplier for multiplication and addition between the symbol sequence and the filter coefficient sequence for implementing the FIR filter 9 of FIG. 2 may be omitted. The example of operation S60 will be described with reference to FIG. 14. In operation S80, the first communication device 1 may transmit a test pattern. For example, the test pattern may include a pattern previously shared by the first communication device 1 and the second communication device 2, and the second communication device 2 may receive the test pattern through a channel (e.g., 7 of FIG. 1). In operation S90, the second communication device 2 may determine whether to adjust the filter coefficient. For example, the second communication device 2 may evaluate the test pattern received from the first communication device 1 and determine whether to adjust at least one of the coefficients of the FIR filter used for equalization of the first communication device 1 according to the evaluation result. As illustrated in FIG. 10, when it is determined not to adjust at least one of the filter coefficients, the training of the filter coefficients may be terminated and the first communication device 1 may transmit the signal, which is equalized according to the current filter coefficients, to the second communication device 2. On the other hand, when it is determined to adjust at least one of the filter coefficients, operation S20 may be performed. Unlike the initially performed operation S20, in operation S20, which is performed after operation S90, the second communication device 2 may transmit channel information, which includes information on the variation of the filter coefficients, to the first communication device 1. Thereafter, unlike the initially performed operation S40, in operation S40, the first communication device 1 may refresh the lookup table

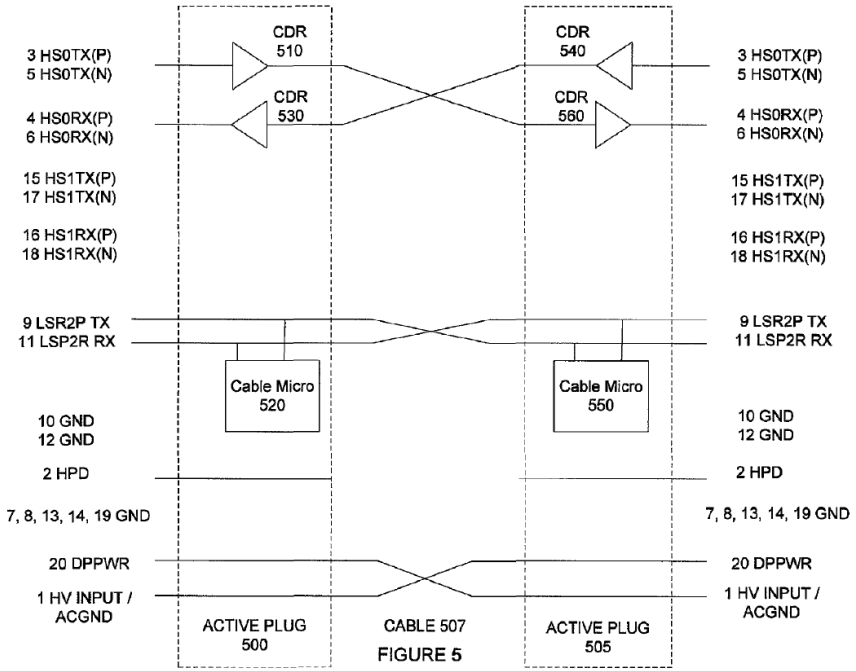
Claim 1	Disclosure
	LUT based on the information on the variation of the filter coefficients. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information on the variation of the filter coefficients will be described with reference to FIG. 12." Kang, 11:62-13:6 FIG. 10  Kang, FIG. 10 "Referring to FIG. 11, operation S**40** *a* may include operations S**42** *a* and S**44** *a*. In operation S**42** *a*, an operation of selecting a data set according to the control signal CTRL may be performed. For example, the controller **110** of FIG. 3 may receive a control signal CTRL including information indicating one of k

Claim 1	Disclosure
	filter coefficient sequences and may control the data storage **120** to output one of first to k-th data sets SET**1** to SETk, which are stored in the data storage **120**, according to the control signal CTRL. In operation S**44** *a*, an operation of loading the selected data set into the lookup table **130** may be performed. For example, the controller **110** may control the data storage **120** and the lookup table **130** to store the second value VAL**2** outputted from the data storage **120** in the lookup table **130**. Referring to FIG. 12, operation S**40** *b* may include operations S**42** *b* and S**44** *b*. In operation S**42** *b*, an operation of generating an offset OFF corresponding to the variation of the filter coefficients may be performed. For example, the offset generator **150** of FIG. 6 may generate an offset OFF, based on the variation signal VAR and the index IDX provided from the controller **110′**. The variation signal VAR may indicate at least one of up, down, hold, and reset of the filter coefficient and may include a variation amount of the filter coefficient. An example of generating the offset OFF when the variation signal VAR indicates the reset of the filter coefficient will be described later with reference to FIG. 13. In operation S**44** *b*, an operation of refreshing the lookup table **130′** may be performed by adding the offset OFF. In some embodiments, the offset generator **150** may generate a positive offset OFF or a negative offset OFF, and thus the calculator **160** may perform an addition. In some embodiments, the offset generator **150** may generate the positive offset OFF, and thus the calculator **160** may perform addition or subtraction according to the control of the controller **110′**. The lookup table **130′** may be refreshed by storing the output value of the calculator **160**, that is, the third value VAL**3**, in the lookup table **130′**." Kang, 13:18-54

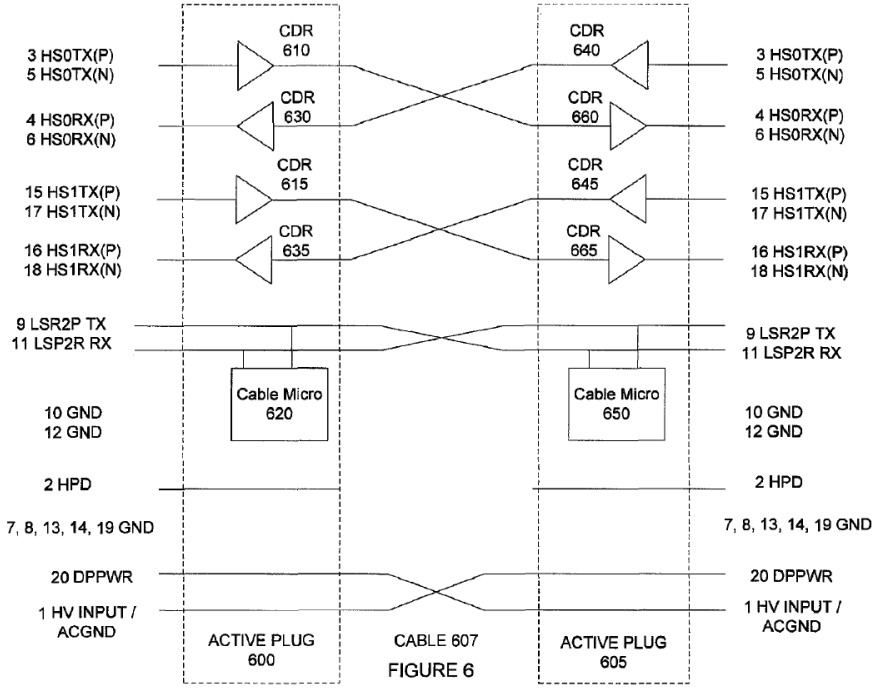
Claim 1	Disclosure
	FIG. 11  Kang, FIG. 11

Claim 1	Disclosure
	FIG. 12  Kang, FIG. 12 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**. Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**.

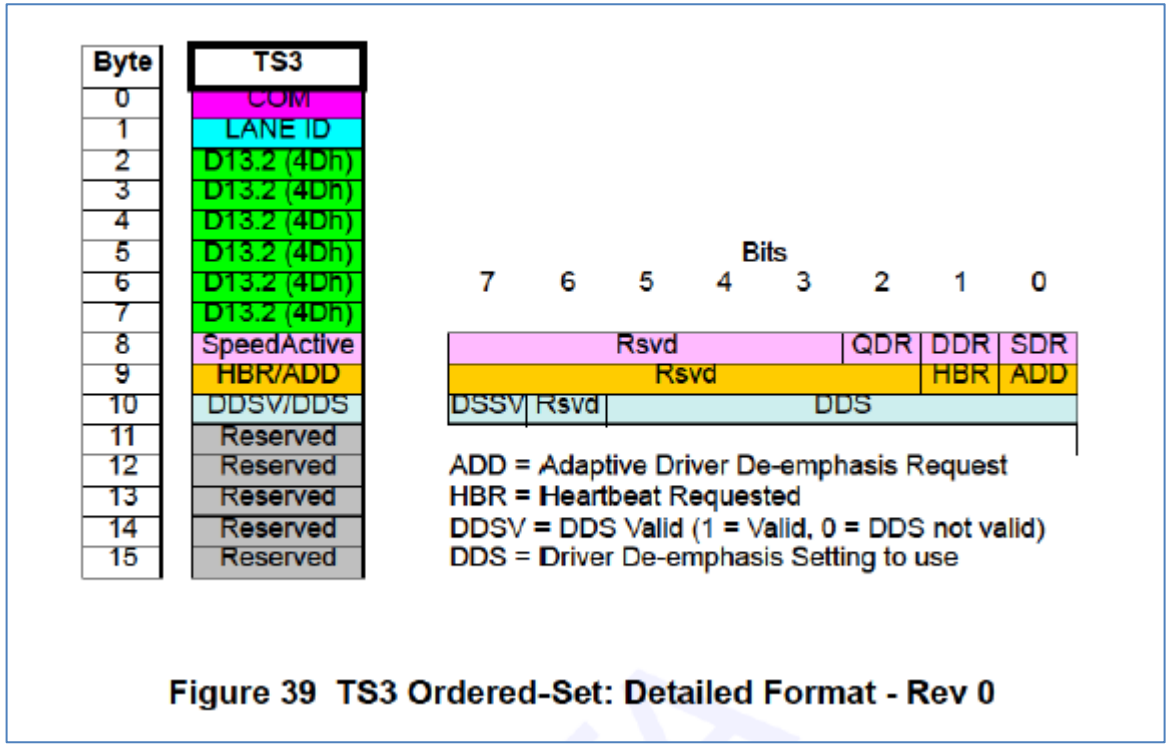
Claim 1	Disclosure
	The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables. In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used.

Claim 1	Disclosure
	In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5 "FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock

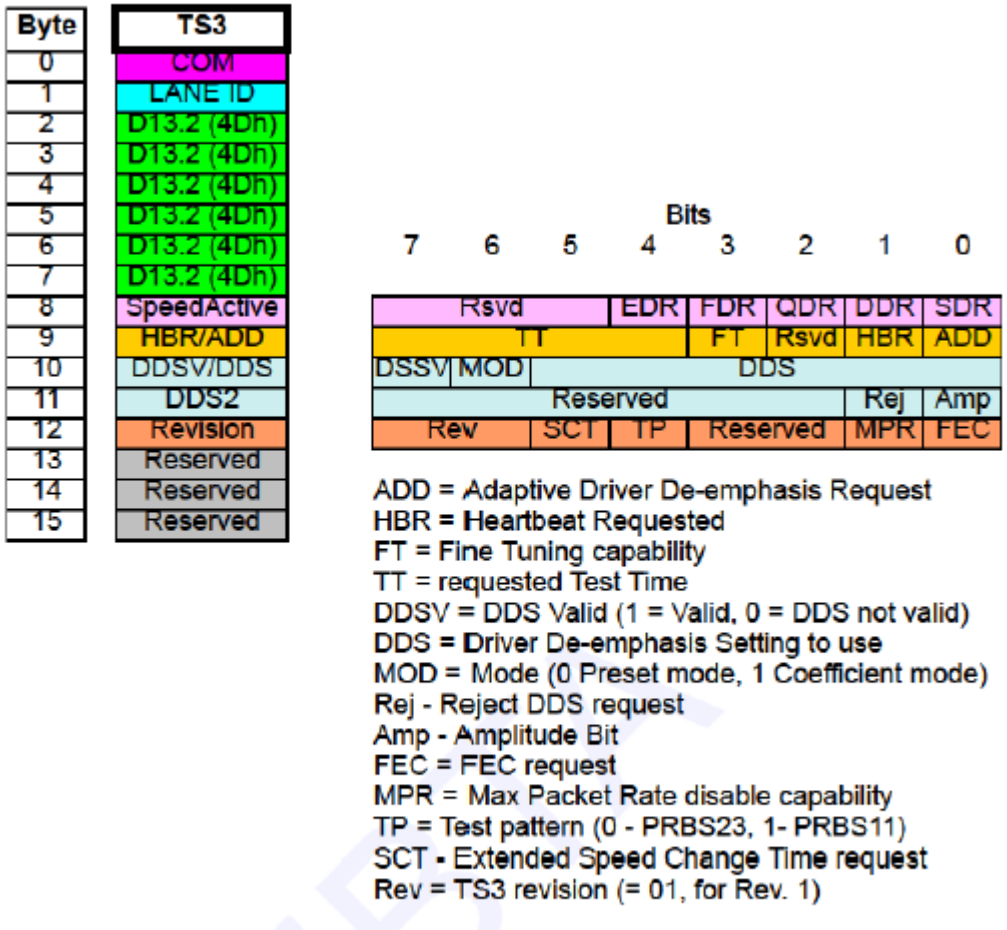
Claim 1	Disclosure
	and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 1	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 1	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 1	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 1	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

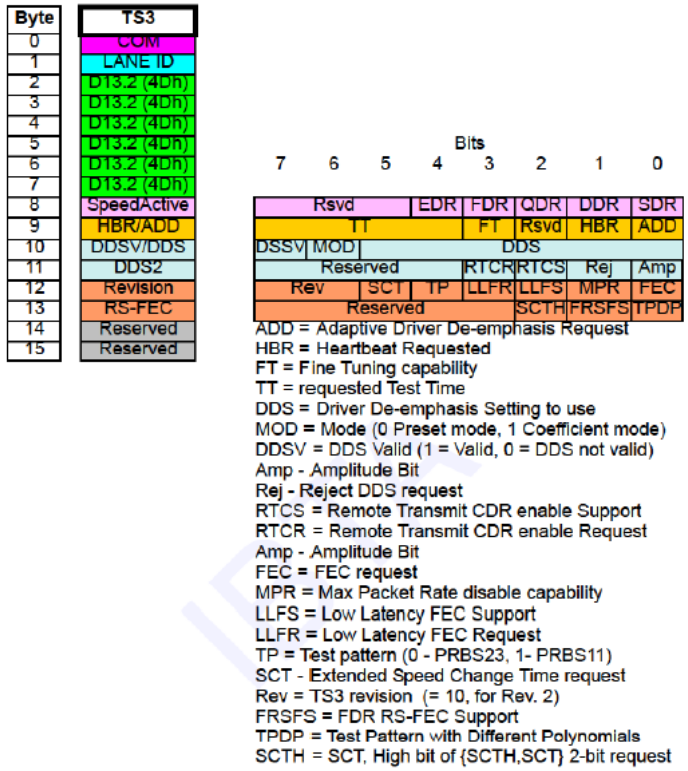
Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 1	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 1	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 1	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 1	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 1	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 1	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 1	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 1	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

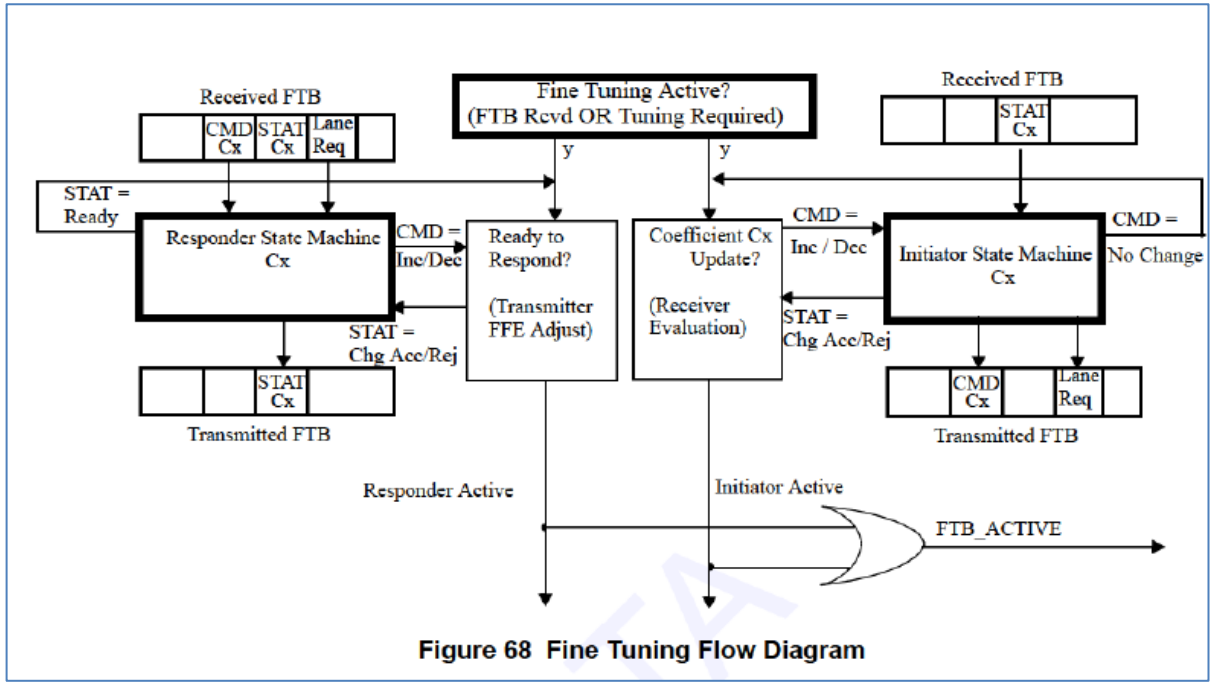
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 1	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 1	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 1	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 1	Disclosure

234	7:4	Tx1 input equalization	Transmitter input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 1	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 1	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"**FIG. 9** is a block diagram of a calibration system **900** for the pre-equalizer of **FIG. 8**. FIG. illustrates the calibration setup required to generate the tap coefficient values for the pre-equalizer system **800** (**FIG. 8**)."

Rafie, paragraph 83.

"The pre-equalizer **1008** tap coefficients can be updated through the tap coefficient memory **1026**.".

Rafie, paragraph 90.

Claim 1	Disclosure
	"For instance, the transmitter device can be configured to select a first path to adaptively initialize the coefficients before data is transmitted and a second path to continuously adjust the coefficients while data is being transmitted. More particularly, the processing control logic **102** can be configured to select the presence transition equalization path **114** when there are presence change events for the RF carrier signal (e.g., events corresponding to when the RF carrier signal transitions between being present and being absent on the antenna **106**). Once data is being transmitted, with pre-equalization using the coefficients generated by path **114**, the processing control logic **102** can select the adaptive feedback equalization path **112**, which can include logic circuitry that is configured to continuously adjust the coefficients based upon feedback received from the antenna relative to the updated coefficients." Ciacci, 4:39-54. <u>*U.S. Patent Publication No. 2014/0281067 ("Das Sharma")*</u> Das Sharma discloses a "link training and equalization procedure" which is a training phase during which initial coefficients are "adjusted." *See, e.g.*, Das Sharma at [0066], [0075]; *see also id*. at [0063] (it is "important to provide the capability to dynamically adjust the transmitter and receiver equalization settings"). "[O]nce the initial coefficients are computed…a new set of coefficients may be computed by adding a predefined constant or set of predefined constants to the computed set of coefficients" at each iteration of the training phase. *Id*. at [0124], [0136] ("multiple iterations may be performed to achieve the optimum link training and equalization transmitter…settings"). "[N]ew set[s] of coefficients" are "generated" and applied in an iterative fashion "until the target BER" (bit error rate) "is reached." *Id*. at [0081]. Das Sharma discloses that transceivers that include the registers storing different pre-equalizer coefficients update the initial pre-equalizer coefficients for FIR filters to optimize those coefficients to reduce the error rate. *See* Das Sharma at [0063], [0066], [0075], [0081], [0124], [0136].

Claim 1	Disclosure
	PCIe 3.1a The equalization procedure consists of up to four Phases, as described below. When operating at the 8.0 GT/s data rate, the Phase information is transmitted using the Equalization Control (EC) field in the TS1 Ordered Sets. Phase 0: The Downstream Port communicates the Transmitter preset values and the Receiver preset hints for each Lane to the Upstream Port using 8b/10b encoding. These values are communicated using the EQ TS2 Ordered Sets (defined in Section 4.2.4.1) in Recovery.RcvrCfg, when a data rate change to 8.0 GT/s has been negotiated, prior to transitioning to 8.0 GT/s data

Claim 1	Disclosure
	rate. These preset values are derived from the Upstream Port Transmitter Preset and Upstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. After the data rate change to 8.0 GT/s, the Upstream Port transmits TS1 Ordered Sets with the preset values it received. The preset values must be within the operable range defined in Section 4.3.3.5.2 if reduced swing will be used by the Transmitter. Phase 1: Both components make the Link operational enough at 8.0 GT/s data rate to be able to exchange TS1 Ordered Sets to complete remaining phases for the fine-tuning their Transmitter/Receiver pairs. It is expected that the Link will operate at a BER of less than 10^{-4} before the component is ready to move on to the next Phase. The Downstream Port initiates Phase 1 by transmitting TS1 Ordered Sets with EC=01b (indicating Phase 1) to the Upstream Port using the preset values in the Downstream Port Transmitter Preset and, optionally, the Downstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. The Upstream Port, after adjusting its Receiver, if necessary, to ensure that it can progress with the equalization process, receives these TS1 Ordered Sets and transitions to Phase 1 (where it transmits TS1 Ordered Sets with EC=01b). The Downstream Port ensures that it can reliably receive the bit stream from the Upstream Port to continue through the rest of the Phases when it receives TS1 Ordered Sets from the Upstream Port with EC=01b before it moves on to Phase 2. Phase 2: In this Phase the Upstream Port adjusts the Transmitter setting of the Downstream Port along with its own Receiver setting, independently, on each Lane, to ensure it receives the bit stream compliant with the requirements in Section 4.3 (e.g., all operational Downstream Lanes have a BER is less than 10^{-12}). The Downstream Port initiates the move to Phase 2 by transmitting TS1 Ordered Sets with EC=10b to the Upstream Port. The Downstream Port advertises the Transmitter coefficients and the preset it is using per the rules below in Phase 1 for preset only and in Phase 2 for preset and coefficients. The Upstream Port receives these Ordered Sets and may request different coefficient or preset settings and continue to evaluate each setting until it arrives at the best setting for operating the Downstream Lanes. After the Upstream Port has completed this Phase, it moves the Link to Phase 3 by transmitting TS1 Ordered Sets with EC=11b to the Downstream Port. Phase 3: In this Phase the Downstream Port adjusts the Transmitter setting of the Upstream Port along with its own Receiver setting, independently, on each Lane, using a handshake and evaluation process similar to Phase 2 with the exception that EC=11b. The Downstream Port signals the end of Phase 3 (and the equalization procedure) by transmitting TS1 Ordered Sets with EC=00b. PCIe 3.1a at 240-241.

Claim 1	Disclosure

4.3.3.5.2. Tx Equalization Presets

An 8.0 GT/s transmitter must support a specified number of presets, where the preset values are defined in terms of voltage ratios as illustrated in Figure 4-42. Presets are defined in terms of two ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GTs/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. Figure 4-42 is shown as an example of TxEQ and is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of 8.0 GT/s signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms, as shown later in this section.

The presets defined in Table 4-16 and Table 4-17 are numbered to match the designations in Section 4.2.3.1. Note, however, that in Section 4.2.3.1 the coefficients are defined as integers (using upper case "C"), while in the electrical section they are defined as floating point (using lower case "c").

PCIe 3.1a at 355.

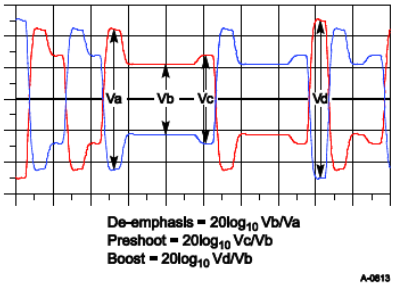
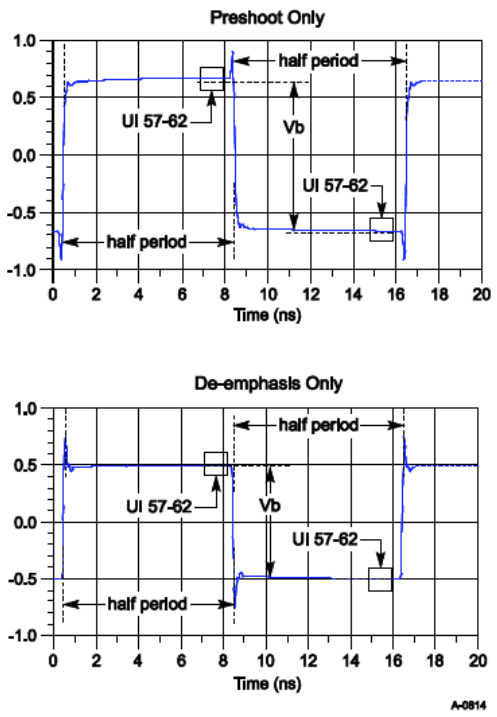


Figure 4-42: Definition of Tx Voltage Levels and Equalization Ratios

Figure 4-43 illustrates the waveforms that will be observed when measuring presets when using the 64-ones/64-zeroes sequence that is part of the compliance pattern. Depending on whether the preset implements de-emphasis, preshoot, or both the corresponding waveshape will differ. The two cases illustrated below show preshoot and de-emphasis, as can be observed by noting whether the boost occurs before or after each edge transition. For the case where both de-emphasis and preshoot are present, boost occurs both before and after each edge transition. Note that in all cases, however, the voltage of interest occurs during the flat portion (Vb) of the waveform, where it can be accurately measured independent of high frequency effects.

PCIe 3.1a at 356.

Claim 1	Disclosure
	 **Figure 4-43: Waveform Measurement Points for Pre-shoot and De-emphasis** PCIe 3.1a at 357.

Claim 1	Disclosure

Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

Notes:

1. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The allowable P10 boost range is defined by the coefficient space lying between the Min and Max Reduced Swing Limits as shown by the two diagonal lines in the example of Figure 4-45. This approach permits both full and reduced swing transmitters to use P10 for testing to their respective boost limits.

With the exception of P4 (for which both pre-shoot and de-emphasis are 0.0 dB) it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are 1 UI wide and therefore subject to attenuation by the package and the breakout channel. Instead the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval. Table 4-17 lists the preset values required to measure each of the Va and Vc values from which the preshoot or de-emphasis values may be derived.

PCIe 3.1a at 358.

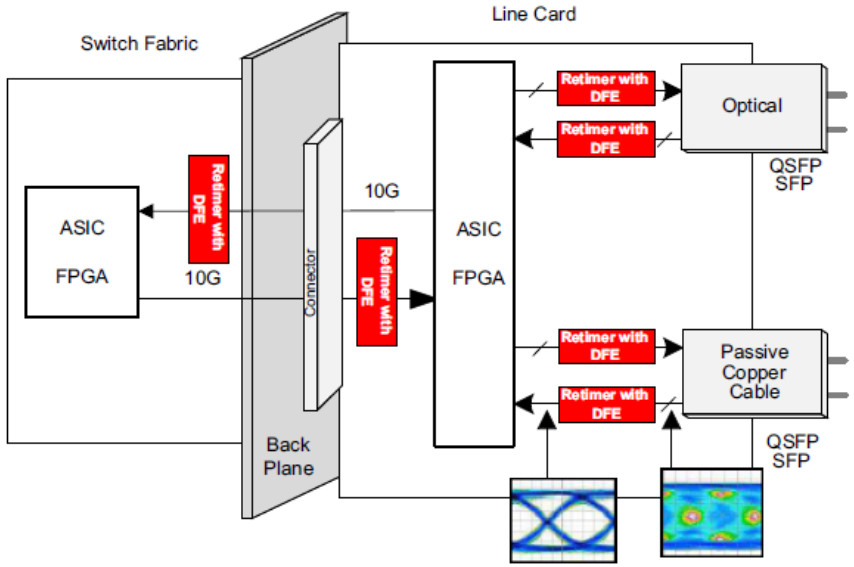
Claim 1	Disclosure
	Table 4-17: Preset Measurement Cross Reference Table PCIe 3.1a at 359.

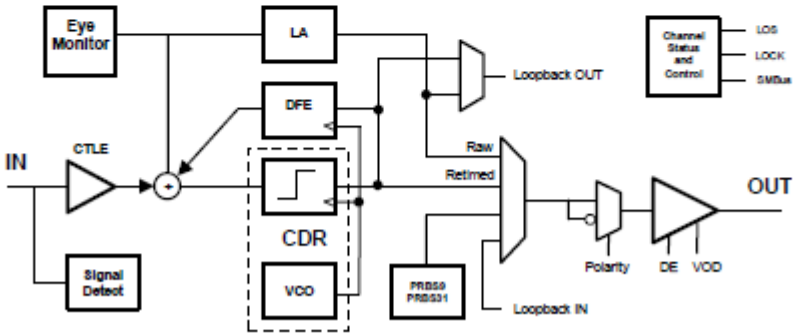
Table 4-17: Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P4	N/A	N/A
P1	P1/P4	N/A
P0	P0/P4	N/A
P9	N/A	P4/P9
P8	P8/P6	P3/P8
P7	P7/P5	P2/P7
P5	N/A	P4/P5
P6	N/A	P4/P6
P3	P3/P4	N/A
P2	P2/P4	N/A
P10	P10/P4	N/A

Claim 1	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 1	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 1	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 1	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 1	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 1	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

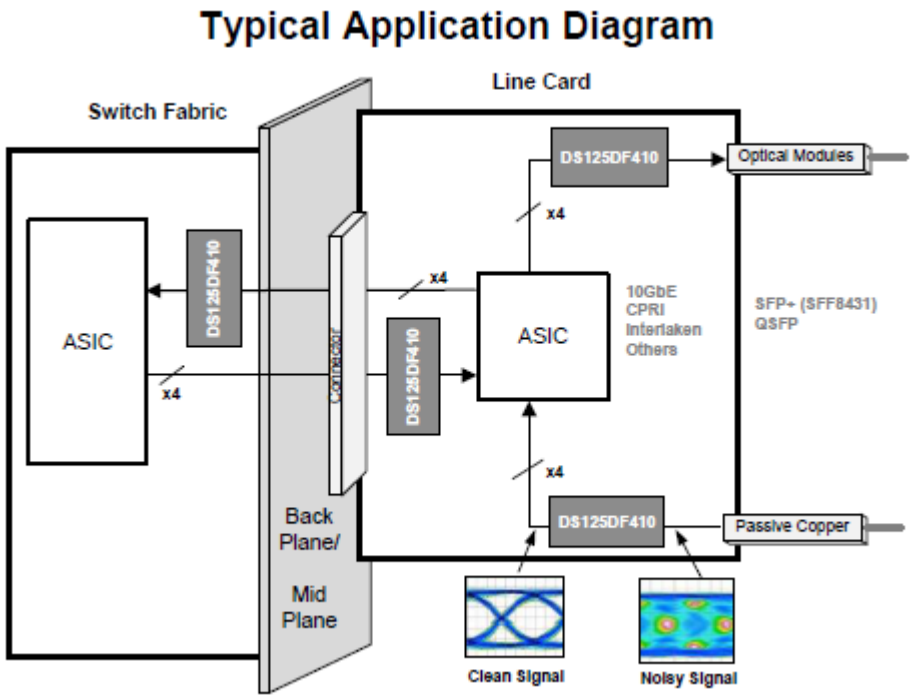
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

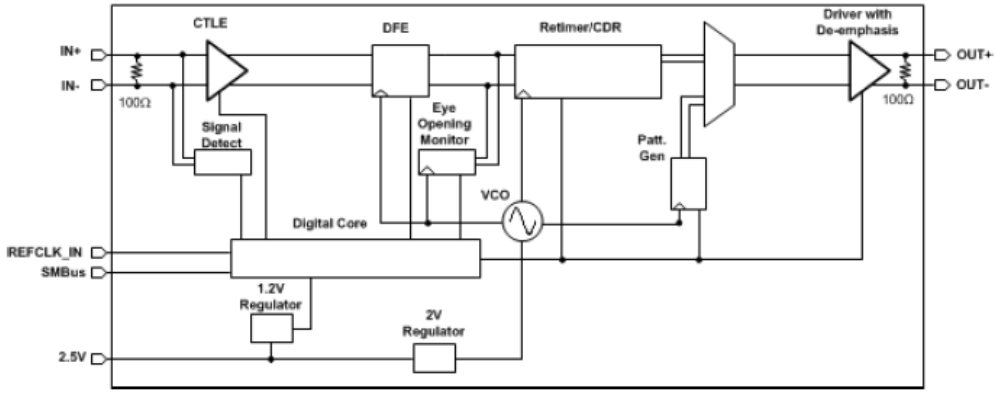
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 1	Disclosure
	 TI DS125DF410, 1.

Claim 1	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 1	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 1	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 1	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 1	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 1	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

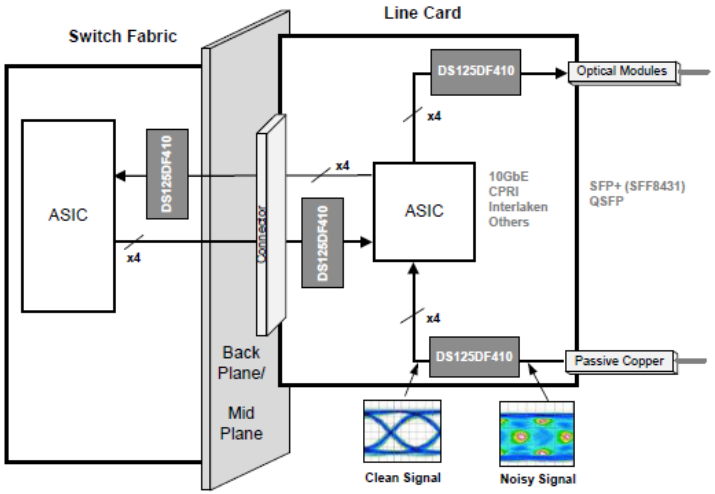
TI DS125DF410, 41.

Claim 1	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

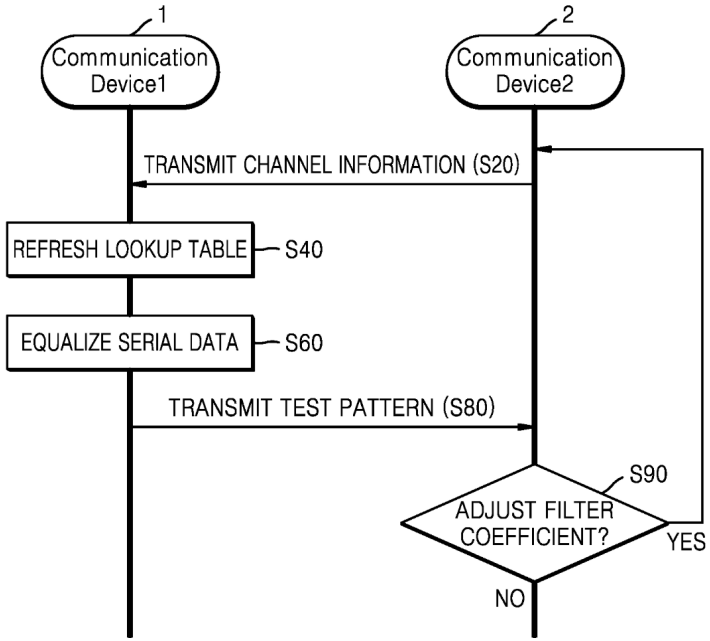
Claim 1	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 1	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

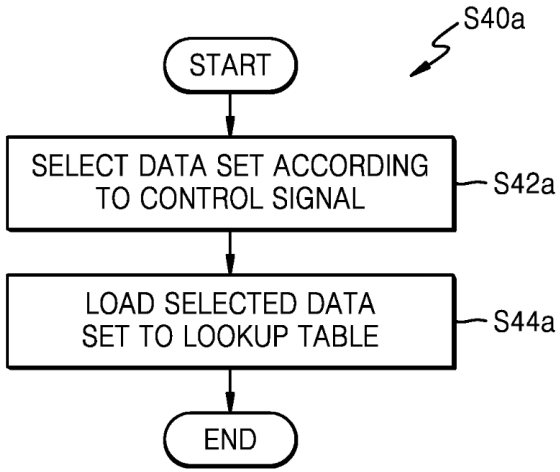
Claim 1	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

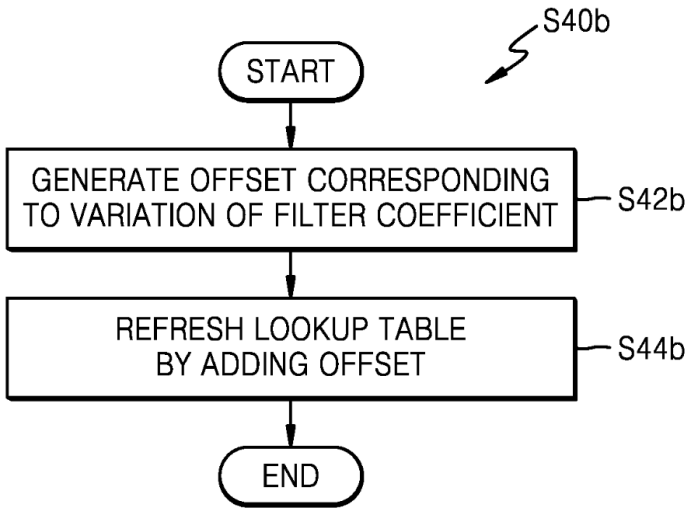
Claim 1	Disclosure
1[c] using the updated pre-equalizer coefficient values to convey a transmit data stream.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "FIG. 10 is a diagram illustrating an equalization method over time according to an exemplary embodiment of the disclosure. For example, the equalization method of FIG. 10 may be performed by the first communication device 1 including the TX equalizer 12 of FIG. 1 and the second communication device 2 communicating with the first communication device 1. The filter coefficients for equalization may be determined according to the equalization method illustrated in FIG. 10, and the method for determining the filter coefficients may be referred to as training of filter coefficients. It is assumed below that the first communication device 1 of FIG. 10 includes the components of the communication device 5 of FIG. 1, and FIG. 10 will be described with reference to FIG. 1. Referring to FIG. 10, in operation S20, the second communication device 2 may transmit channel information. For example, the second communication device 2 may first transmit, to the first communication device 1, channel information including information indicating one of the plurality of data sets, as described above with reference to FIG. 3.

Claim 1	Disclosure
	In operation S40, the first communication device 1 may refresh the lookup table LUT. For example, the protocol processor 30 of the first communication device 1 may extract information indicating a data set from the channel information received in operation S20 and may transmit the control signal CTRL including the extracted information to the TX equalizer 12. TX equalizer 12 may refresh the lookup table LUT based on the control signal CTRL. The lookup table LUT may include values of the digital signal DSIG corresponding to possible values of the symbol sequence extracted from the serial data SER. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information indicating a data set will be described with reference to FIG. 11. In operation S60, the first communication device 1 may equalize the serial data SER. For example, in the TX equalizer 12 of the first communication device 1, the lookup table LUT may output a digital signal (e.g., DSIG in FIG. 3) corresponding to the symbol sequence of the serial data SER, and the DAC 200 included in the TX equalizer 12 may convert the digital signal into an analog signal. Accordingly, an adder and a multiplier for multiplication and addition between the symbol sequence and the filter coefficient sequence for implementing the FIR filter 9 of FIG. 2 may be omitted. The example of operation S60 will be described with reference to FIG. 14. In operation S80, the first communication device 1 may transmit a test pattern. For example, the test pattern may include a pattern previously shared by the first communication device 1 and the second communication device 2, and the second communication device 2 may receive the test pattern through a channel (e.g., 7 of FIG. 1). In operation S90, the second communication device 2 may determine whether to adjust the filter coefficient. For example, the second communication device 2 may evaluate the test pattern received from the first communication device 1 and determine whether to adjust at least one of the coefficients of the FIR filter used for equalization of the first communication device 1 according to the evaluation result. As illustrated in FIG. 10, when it is determined not to adjust at least one of the filter coefficients, the training of the filter coefficients may be terminated and the first communication device 1 may transmit the signal, which is equalized according to the current filter coefficients, to the second communication device 2. On the other hand, when it is determined to adjust at least one of the filter coefficients, operation S20 may be performed. Unlike the initially performed operation S20, in operation S20, which is performed after operation S90, the second communication device 2 may transmit channel information, which includes information on the

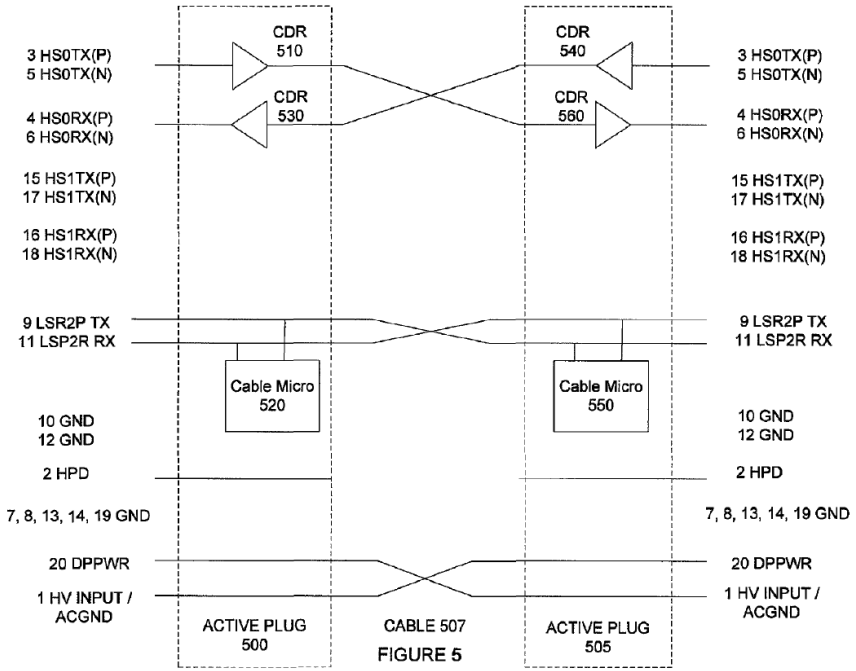
Claim 1	Disclosure
	variation of the filter coefficients, to the first communication device 1. Thereafter, unlike the initially performed operation S40, in operation S40, the first communication device 1 may refresh the lookup table LUT based on the information on the variation of the filter coefficients. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information on the variation of the filter coefficients will be described with reference to FIG. 12." Kang, 11:62-13:6 FIG. 10  Kang, FIG. 10

Claim 1	Disclosure
	"Referring to FIG. 11, operation S**40** *a* may include operations S**42** *a* and S**44** *a*. In operation S**42** *a*, an operation of selecting a data set according to the control signal CTRL may be performed. For example, the controller **110** of FIG. 3 may receive a control signal CTRL including information indicating one of k filter coefficient sequences and may control the data storage **120** to output one of first to k-th data sets SET**1** to SETk, which are stored in the data storage **120**, according to the control signal CTRL. In operation S**44** *a*, an operation of loading the selected data set into the lookup table **130** may be performed. For example, the controller **110** may control the data storage **120** and the lookup table **130** to store the second value VAL**2** outputted from the data storage **120** in the lookup table **130**. Referring to FIG. 12, operation S**40** *b* may include operations S**42** *b* and S**44** *b*. In operation S**42** *b*, an operation of generating an offset OFF corresponding to the variation of the filter coefficients may be performed. For example, the offset generator **150** of FIG. 6 may generate an offset OFF, based on the variation signal VAR and the index IDX provided from the controller **110′**. The variation signal VAR may indicate at least one of up, down, hold, and reset of the filter coefficient and may include a variation amount of the filter coefficient. An example of generating the offset OFF when the variation signal VAR indicates the reset of the filter coefficient will be described later with reference to FIG. 13. In operation S**44** *b*, an operation of refreshing the lookup table **130′** may be performed by adding the offset OFF. In some embodiments, the offset generator **150** may generate a positive offset OFF or a negative offset OFF, and thus the calculator **160** may perform an addition. In some embodiments, the offset generator **150** may generate the positive offset OFF, and thus the calculator **160** may perform addition or subtraction according to the control of the controller **110′**. The lookup table **130′** may be refreshed by storing the output value of the calculator **160**, that is, the third value VAL**3**, in the lookup table **130′**." Kang, 13:18-54

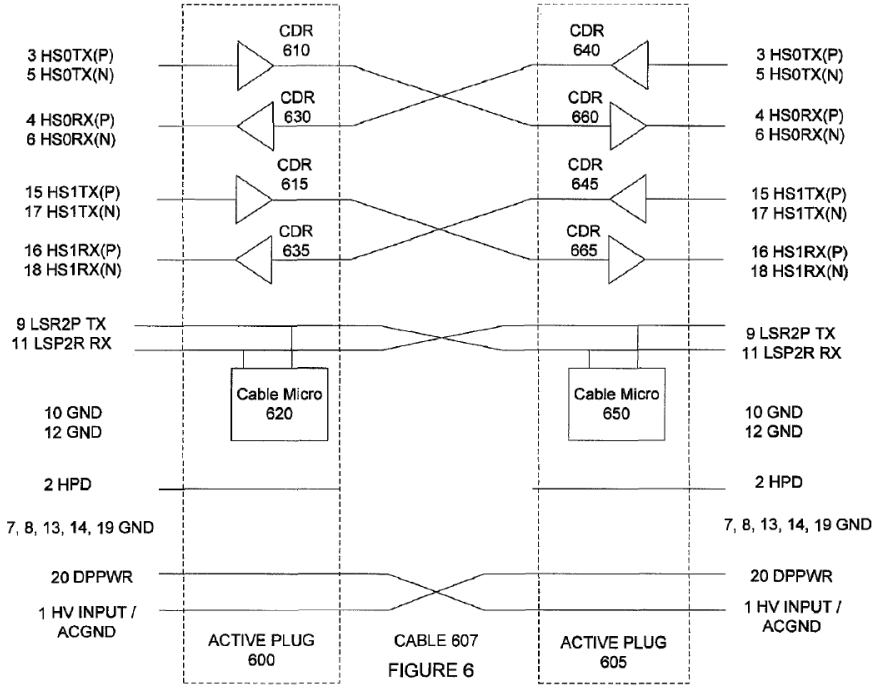
Claim 1	Disclosure
	FIG. 11  Kang, FIG. 11

Claim 1	Disclosure
	FIG. 12  Kang, FIG. 12 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**. Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**.

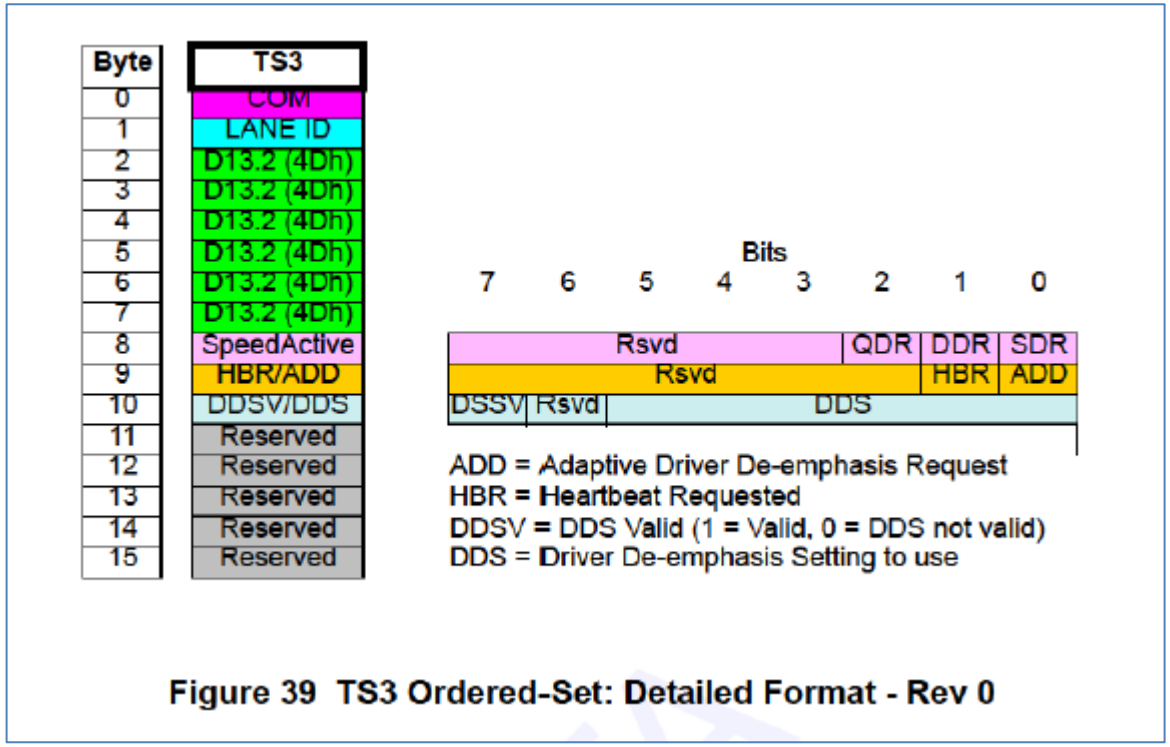
Claim 1	Disclosure
	The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables. In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used.

Claim 1	Disclosure
	In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5 "FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock

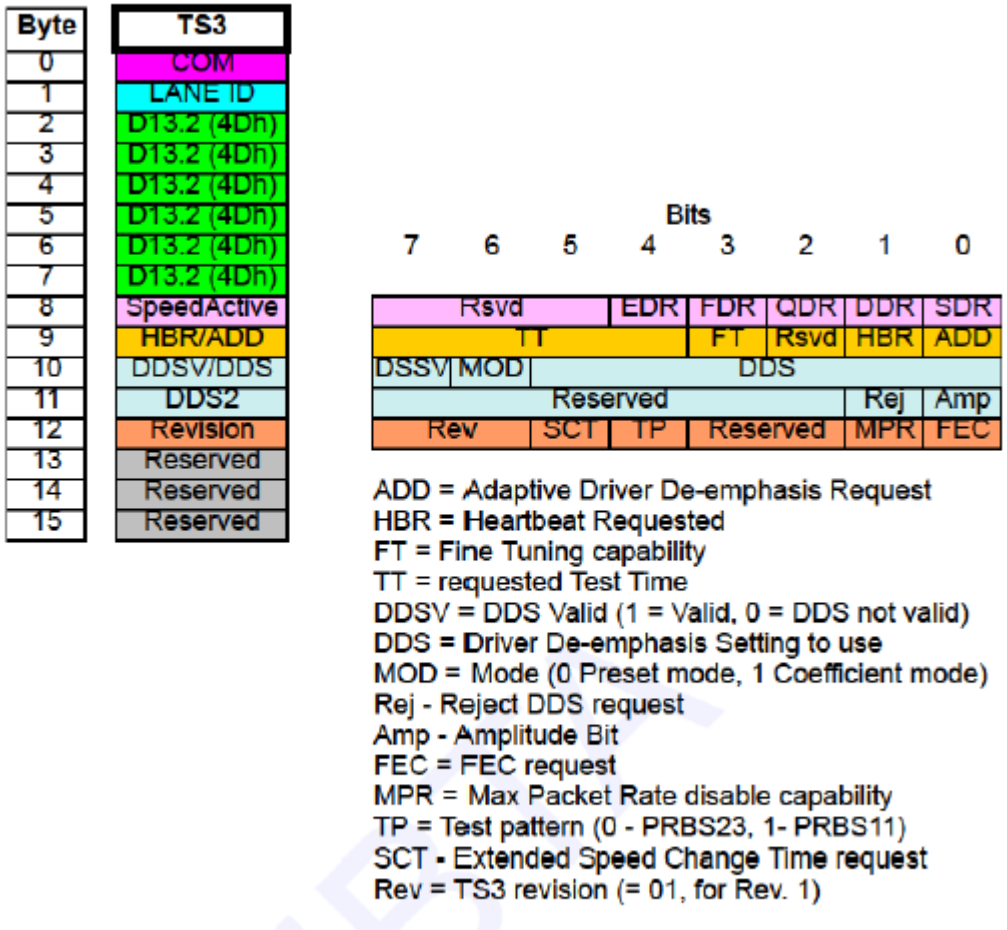
Claim 1	Disclosure
	and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 1	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 1	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 1	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 1	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

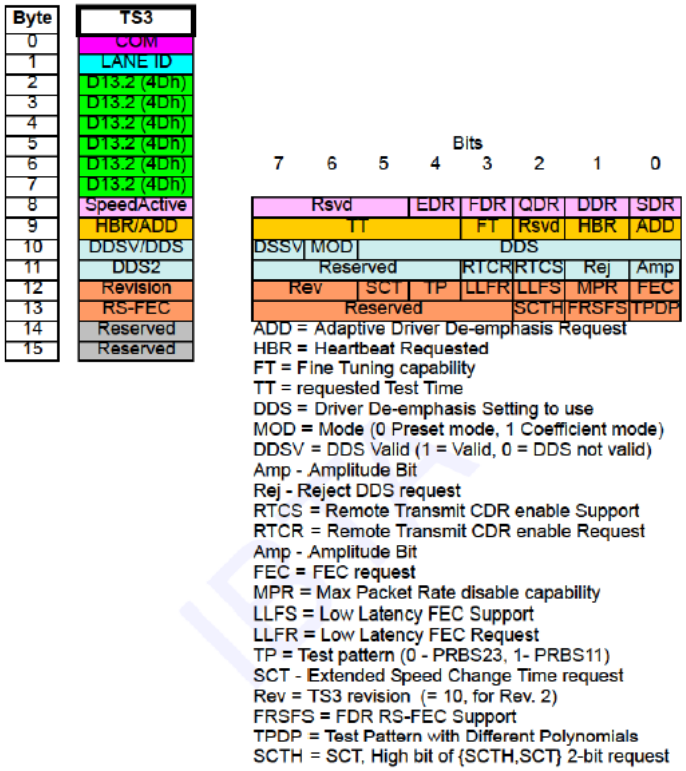
Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 1	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 1	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 1	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 1	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 1	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 1	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 1	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 1	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

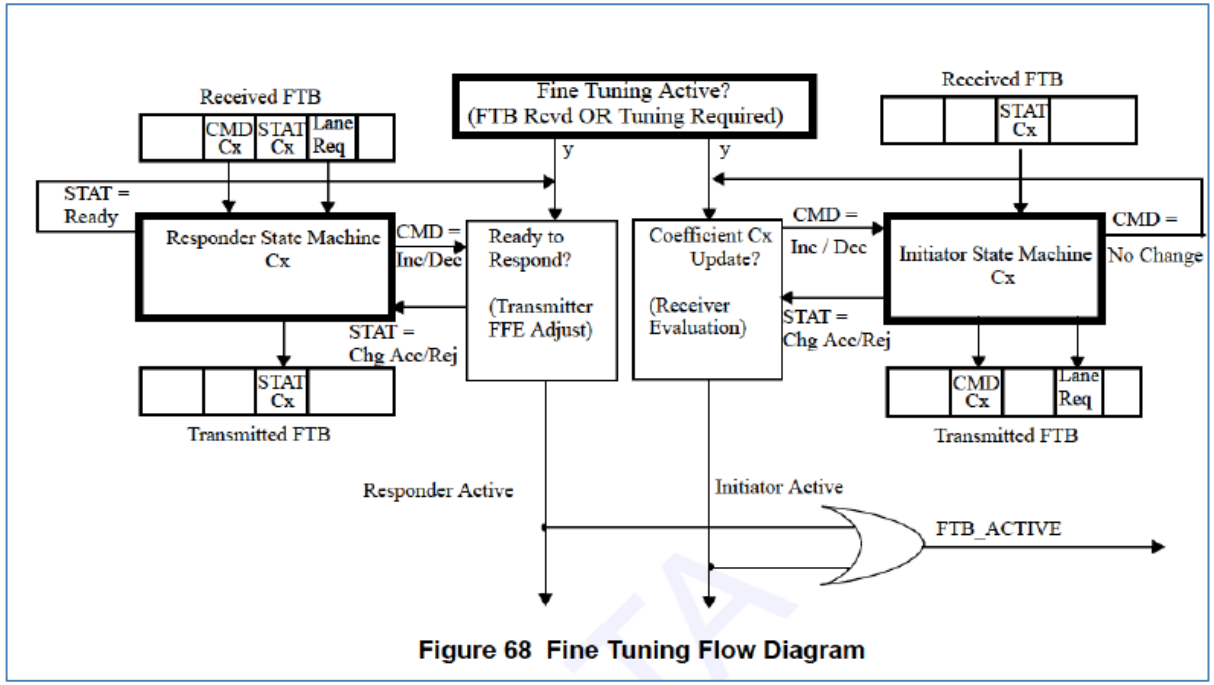
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 1	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 1	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 1	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 1	Disclosure

234	7:4	Tx1 input equalization	Transmitter input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 1	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 1	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					
74-94	All	Reserved - 21B	Reserved - Rx Channel Control	RW			

InfiniBand, Table 143 (p. 535)

"The pre-equalizer **1008** is operated in conjunction with a tap coefficient memory **1026**."
Rafie, paragraph 86.

"The pre-equalizer **1008** tap coefficients can be updated through the tap coefficient memory **1026**.".
Rafie, paragraph 90.

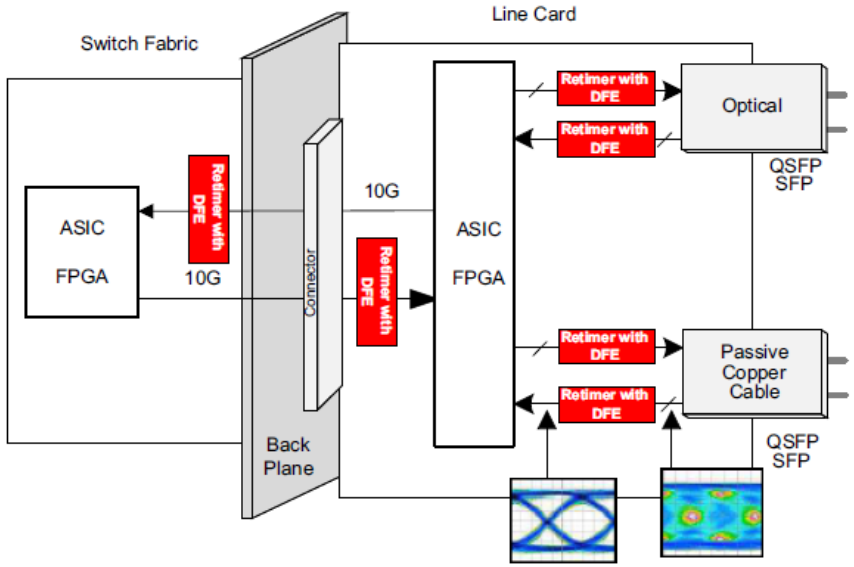
"For instance, the transmitter device can be configured to select a first path to adaptively initialize the coefficients before data is transmitted and a second path to continuously adjust the coefficients while data is being transmitted. More particularly, the processing control logic **102** can be configured to select the presence transition equalization path **114** when there are presence change events for the RF carrier signal

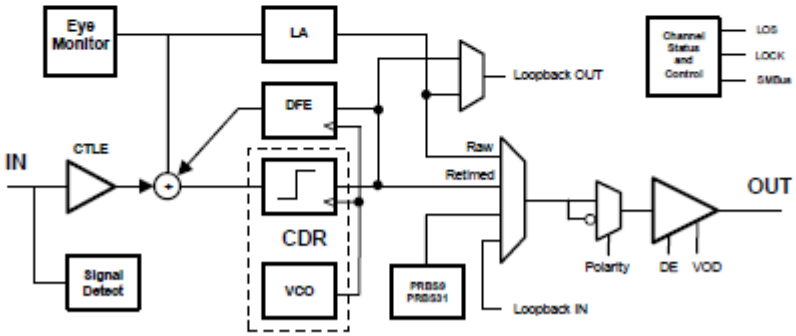
Claim 1	Disclosure
	(e.g., events corresponding to when the RF carrier signal transitions between being present and being absent on the antenna **106**). Once data is being transmitted, with pre-equalization using the coefficients generated by path **114**, the processing control logic **102** can select the adaptive feedback equalization path **112**, which can include logic circuitry that is configured to continuously adjust the coefficients based upon feedback received from the antenna relative to the updated coefficients." Ciacci, 4:39-54. *PCIe 3.1a* The equalization procedure consists of up to four Phases, as described below. When operating at the 8.0 GT/s data rate, the Phase information is transmitted using the Equalization Control (EC) field in the TS1 Ordered Sets. Phase 0: The Downstream Port communicates the Transmitter preset values and the Receiver preset hints for each Lane to the Upstream Port using 8b/10b encoding. These values are communicated using the EQ TS2 Ordered Sets (defined in Section 4.2.4.1) in Recovery.RcvrCfg, when a data rate change to 8.0 GT/s has been negotiated, prior to transitioning to 8.0 GT/s data

Claim 1	Disclosure
	rate. These preset values are derived from the Upstream Port Transmitter Preset and Upstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. After the data rate change to 8.0 GT/s, the Upstream Port transmits TS1 Ordered Sets with the preset values it received. The preset values must be within the operable range defined in Section 4.3.3.5.2 if reduced swing will be used by the Transmitter. Phase 1: Both components make the Link operational enough at 8.0 GT/s data rate to be able to exchange TS1 Ordered Sets to complete remaining phases for the fine-tuning their Transmitter/Receiver pairs. It is expected that the Link will operate at a BER of less than 10^{-4} before the component is ready to move on to the next Phase. The Downstream Port initiates Phase 1 by transmitting TS1 Ordered Sets with EC=01b (indicating Phase 1) to the Upstream Port using the preset values in the Downstream Port Transmitter Preset and, optionally, the Downstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. The Upstream Port, after adjusting its Receiver, if necessary, to ensure that it can progress with the equalization process, receives these TS1 Ordered Sets and transitions to Phase 1 (where it transmits TS1 Ordered Sets with EC=01b). The Downstream Port ensures that it can reliably receive the bit stream from the Upstream Port to continue through the rest of the Phases when it receives TS1 Ordered Sets from the Upstream Port with EC=01b before it moves on to Phase 2. Phase 2: In this Phase the Upstream Port adjusts the Transmitter setting of the Downstream Port along with its own Receiver setting, independently, on each Lane, to ensure it receives the bit stream compliant with the requirements in Section 4.3 (e.g., all operational Downstream Lanes have a BER is less than 10^{-12}). The Downstream Port initiates the move to Phase 2 by transmitting TS1 Ordered Sets with EC=10b to the Upstream Port. The Downstream Port advertises the Transmitter coefficients and the preset it is using per the rules below in Phase 1 for preset only and in Phase 2 for preset and coefficients. The Upstream Port receives these Ordered Sets and may request different coefficient or preset settings and continue to evaluate each setting until it arrives at the best setting for operating the Downstream Lanes. After the Upstream Port has completed this Phase, it moves the Link to Phase 3 by transmitting TS1 Ordered Sets with EC=11b to the Downstream Port. Phase 3: In this Phase the Downstream Port adjusts the Transmitter setting of the Upstream Port along with its own Receiver setting, independently, on each Lane, using a handshake and evaluation process similar to Phase 2 with the exception that EC=11b. The Downstream Port signals the end of Phase 3 (and the equalization procedure) by transmitting TS1 Ordered Sets with EC=00b. PCIe 3.1a at 240-241.

Claim 1	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 1	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 1	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 1	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

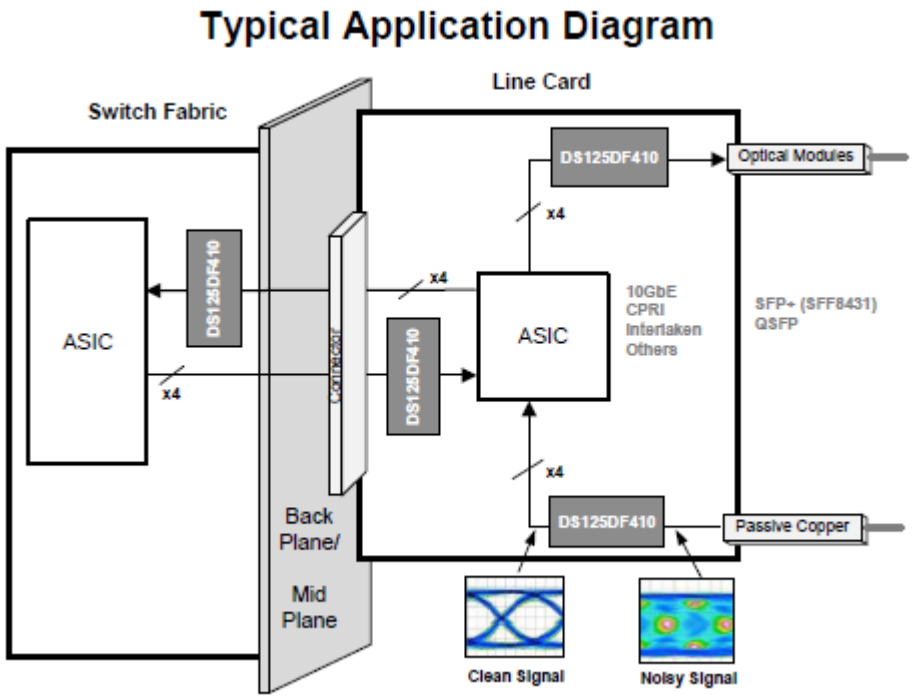
Claim 1	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 1	Disclosure
	7.5.1.26 Setting the Output De-Emphasis Setting *Register 0x15, bits 2:0 and bit 6* Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

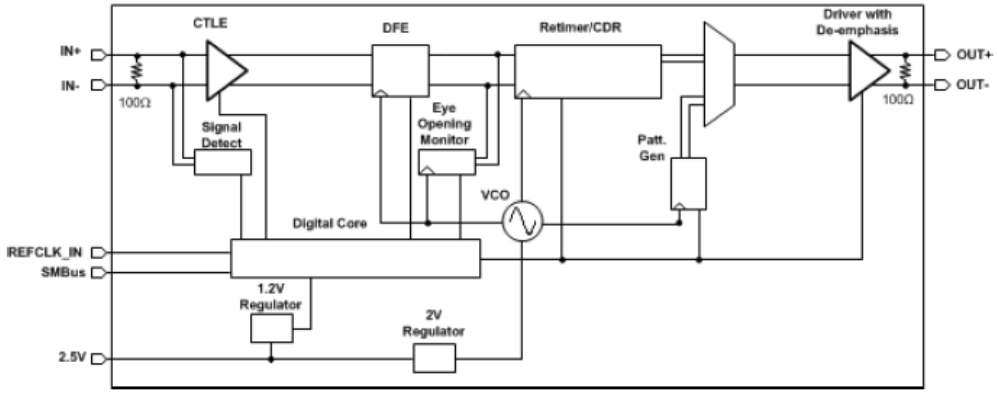
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 1	Disclosure
	 TI DS125DF410, 1.

Claim 1	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 1	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 1	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 1	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 1	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 1	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 1	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

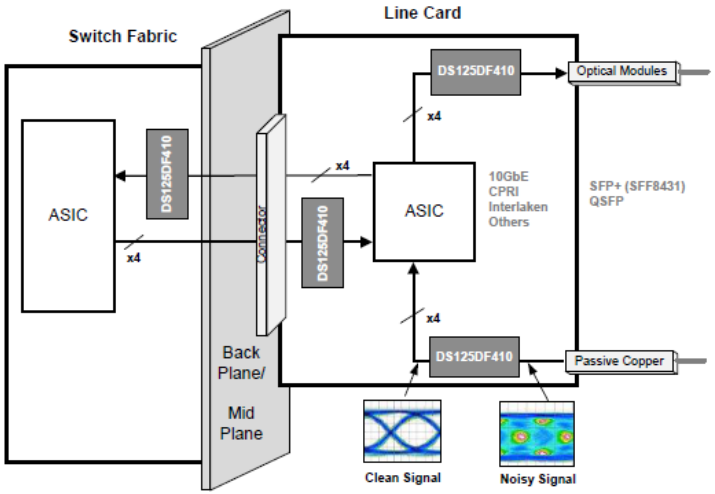
TI DS125DF410, 41.

Claim 1	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 1	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 1	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 1	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

Claim 1	Disclosure

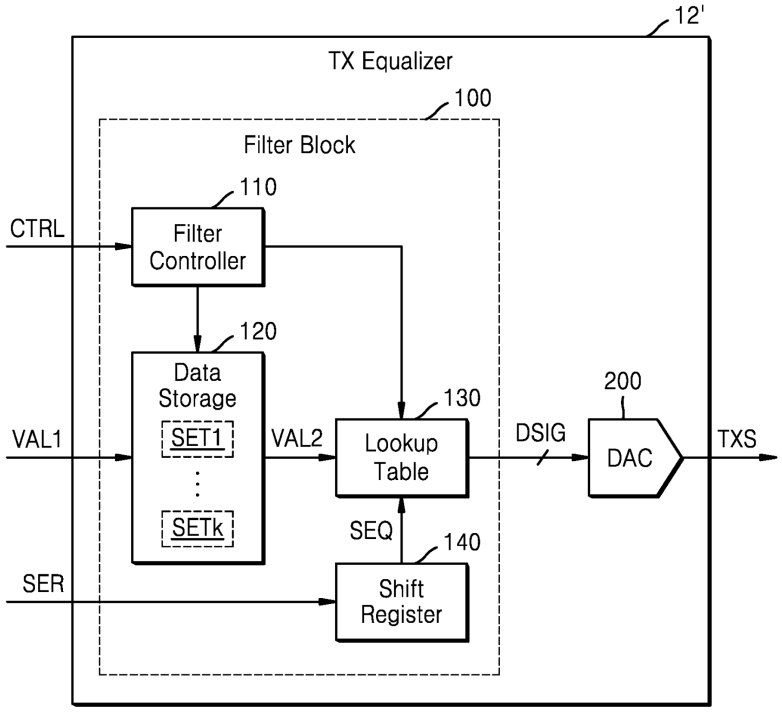
B. DEPENDENT CLAIM 2

Claim 2	Disclosure
2. The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

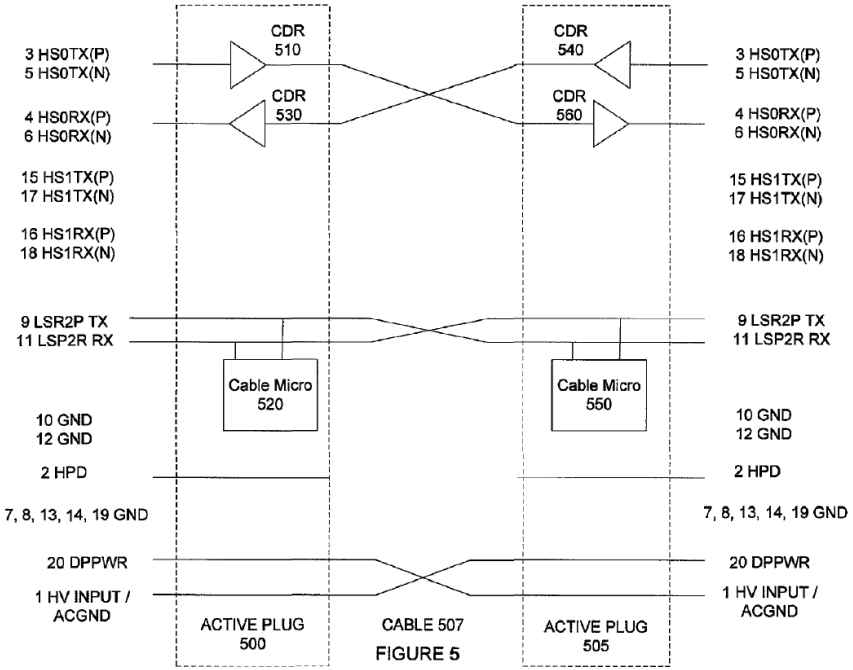
Claim 2	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 2	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

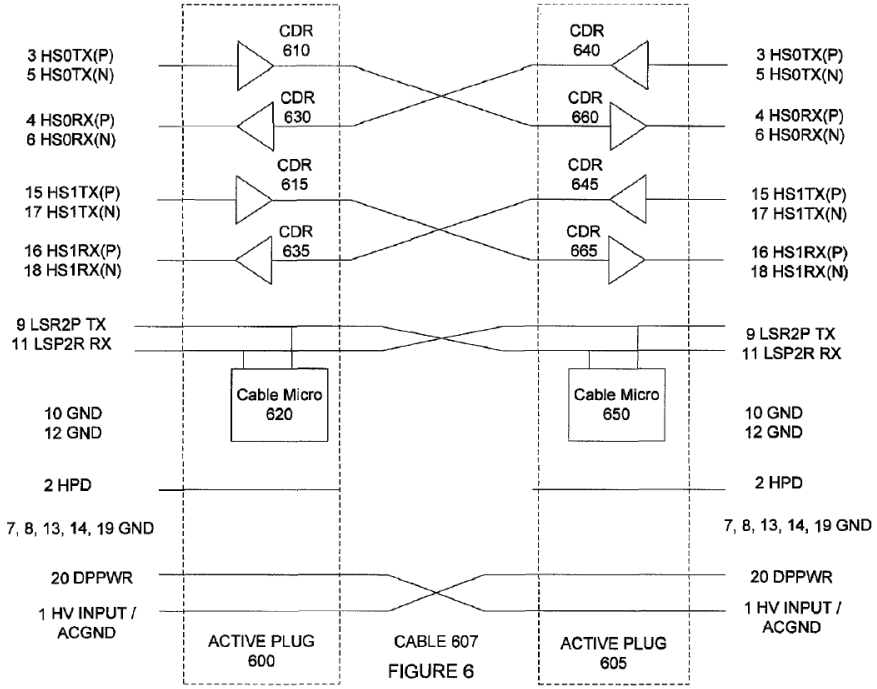
Claim 2	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

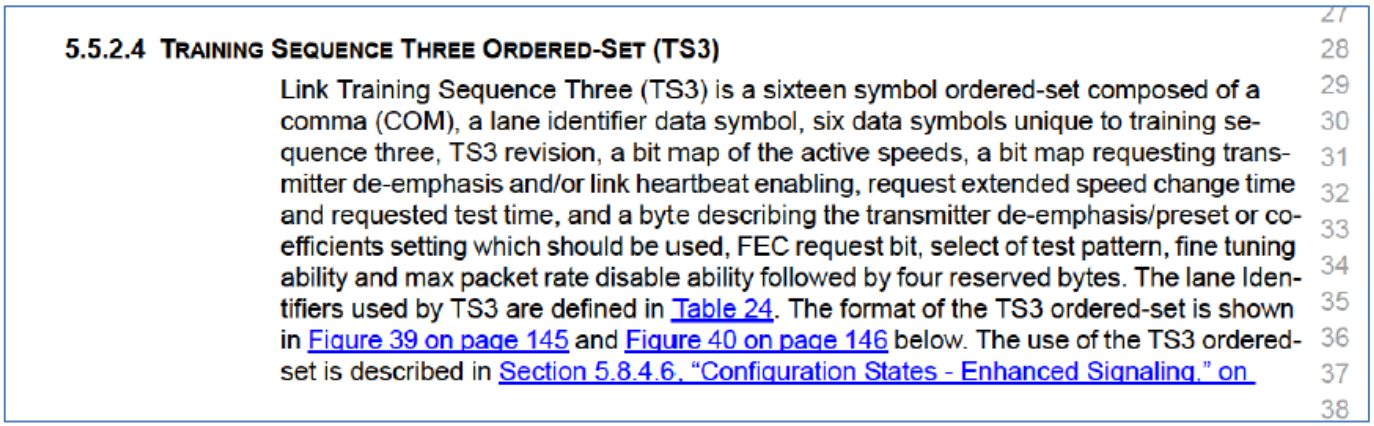
Claim 2	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 2	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 2	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

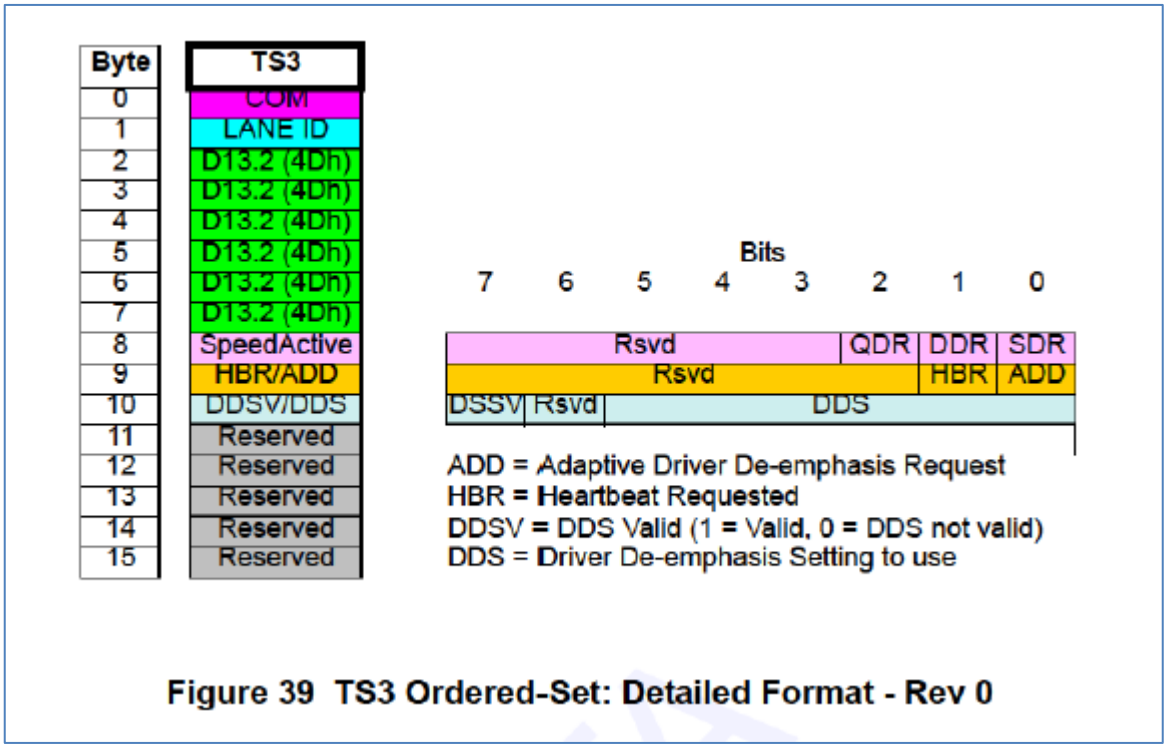
Claim 2	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 2	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 2	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63  InfiniBand, p. 144:27-145:1

5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)

Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on

Claim 2	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 2	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

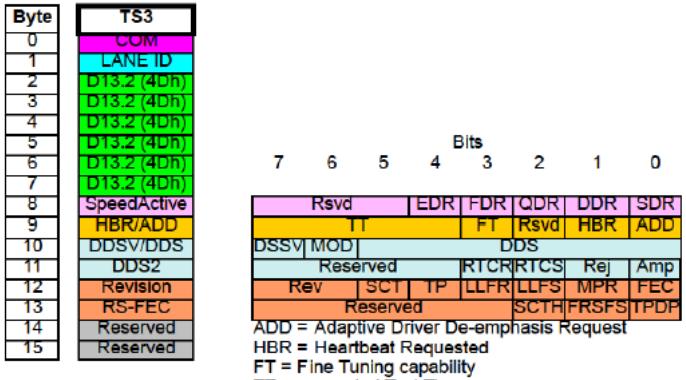
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 2	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 2	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 2	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 2	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 2	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 2	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 2	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 2	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

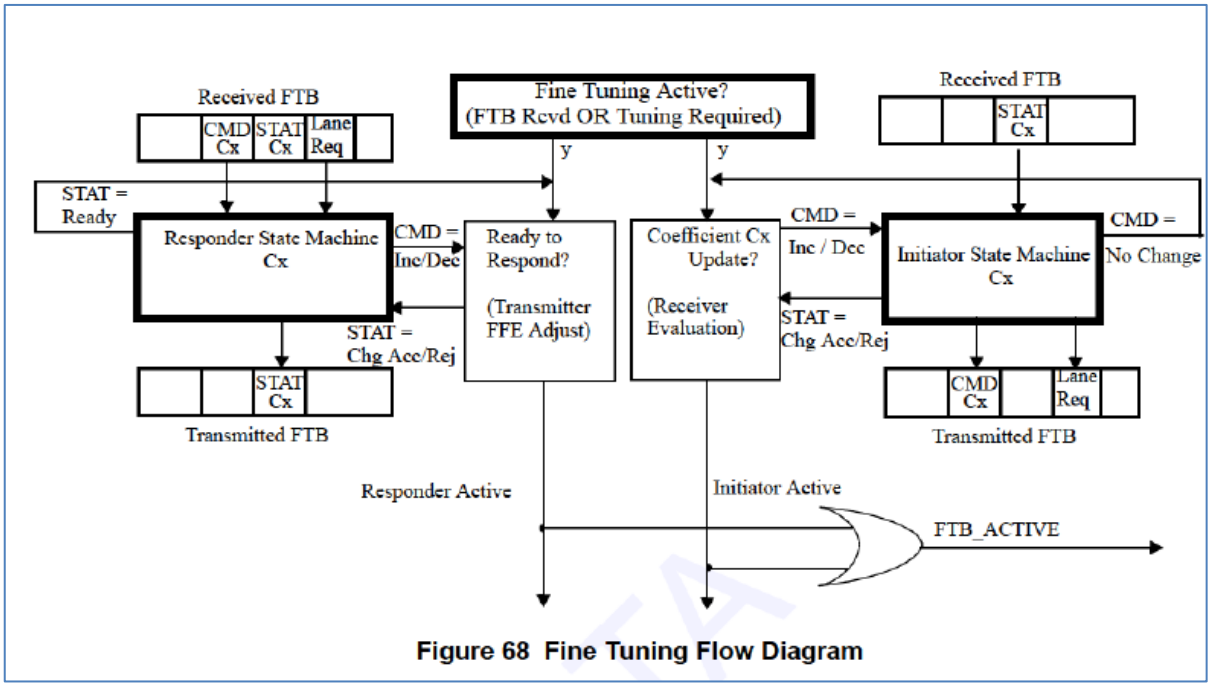
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 2	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 2	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 2	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 2	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 2	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 2	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"The digital pre-equalization of the present invention compensates frequency shaping commonly introduced by transmission components (e. g., front-end filters, antenna equipment).".

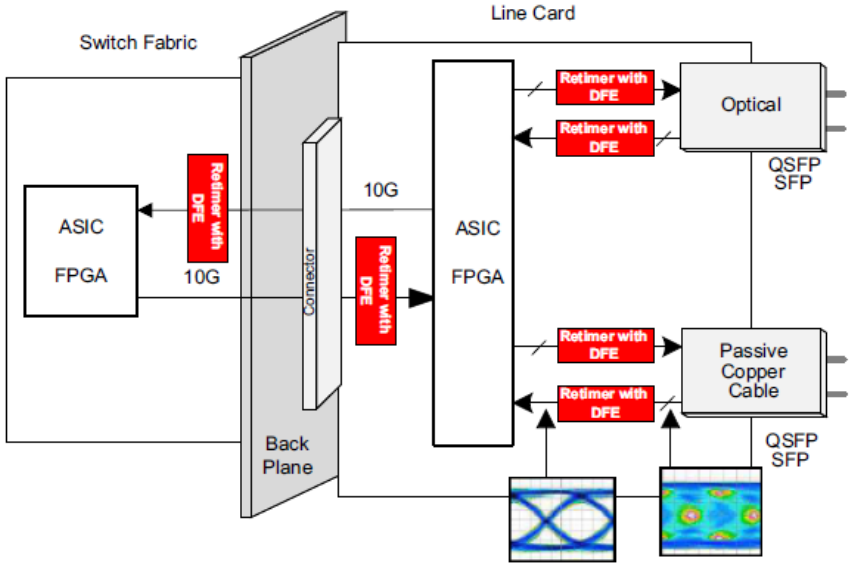
Balakrishnan, paragraph 22.

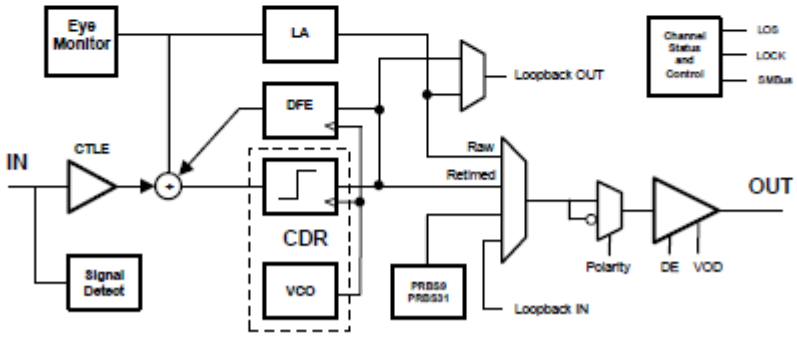
U.S. Patent Publication No. 2014/0281067 ("Das Sharma")

An ordinarily skilled artisan would known about losses in a chip-to-module channel between an active cable's transceiver and the host transceiver, which were routinely compensated for by of pre-equalization. *See, e.g.*, Das Sharma at [0075] (describing the use of equalization to compensate for different types of channel loss).

Claim 2	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 2	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 2	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 2	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 2	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 2	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

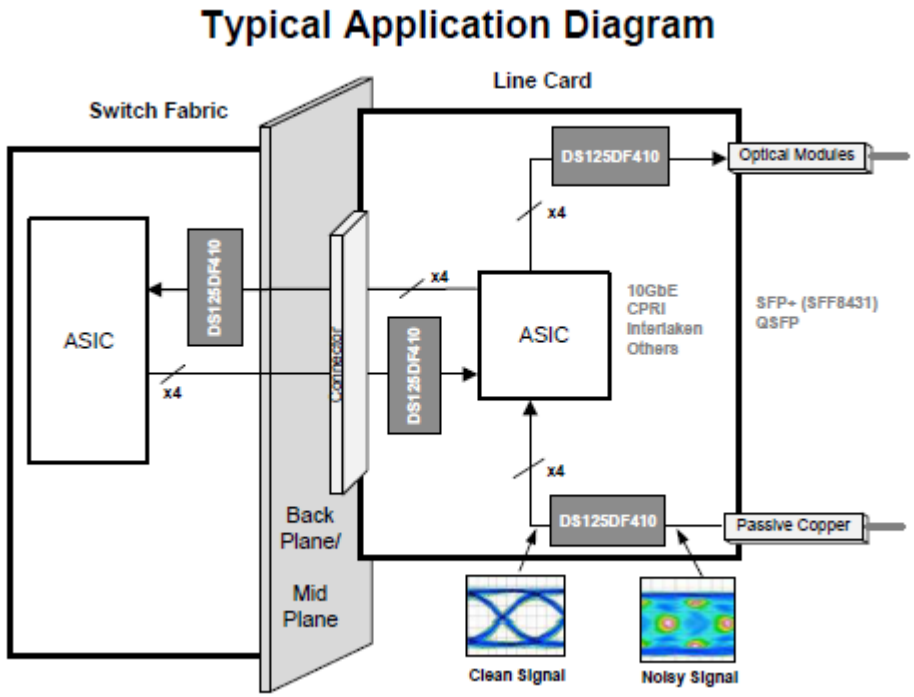
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

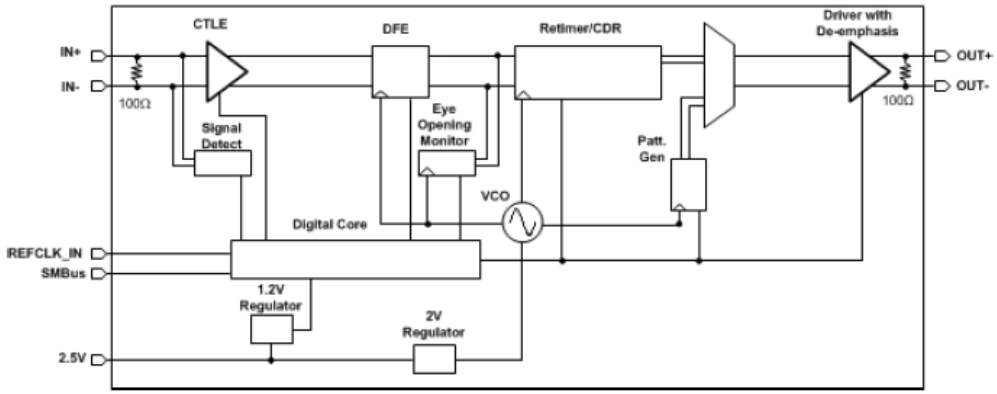
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 2	Disclosure
	 TI DS125DF410, 1.

Claim 2	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 2	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 2	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 2	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 2	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 2	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 2	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 2	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 2	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

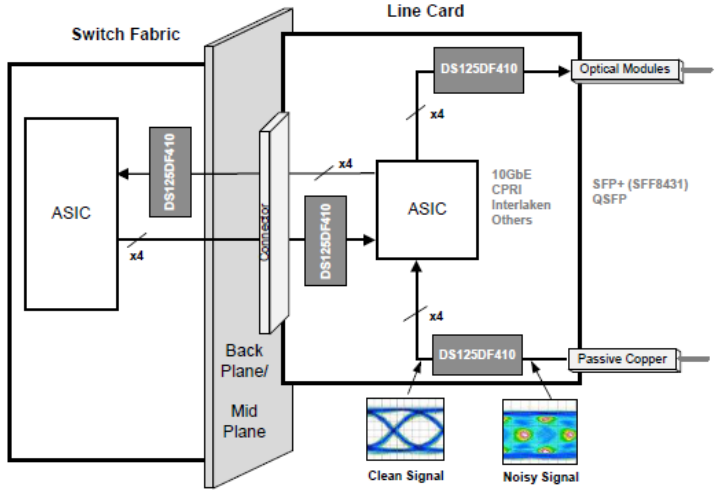
TI DS125DF410, 41.

Claim 2	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 2	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 2	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 2	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

Claim 2	Disclosure

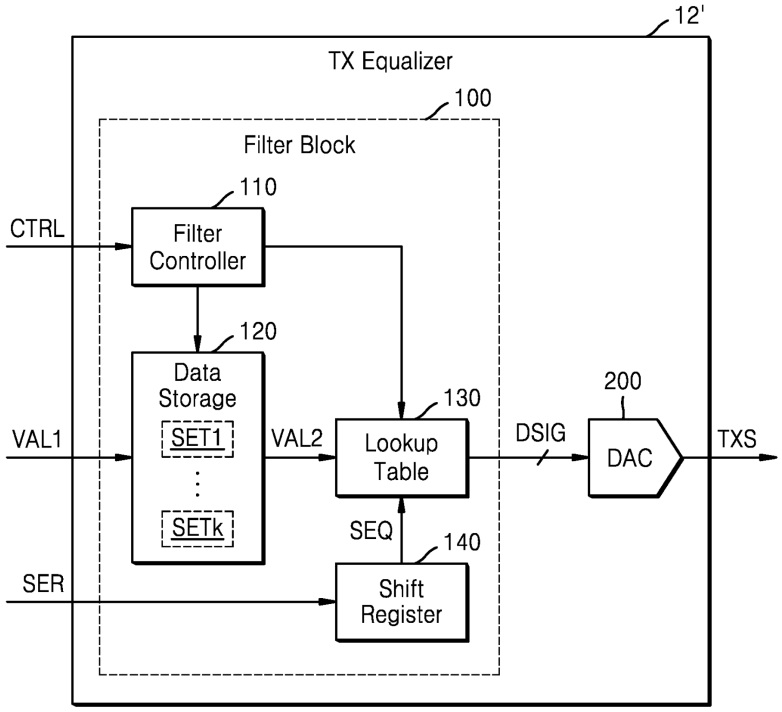
C. DEPENDENT CLAIM 3

Claim 3	Disclosure
3. The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

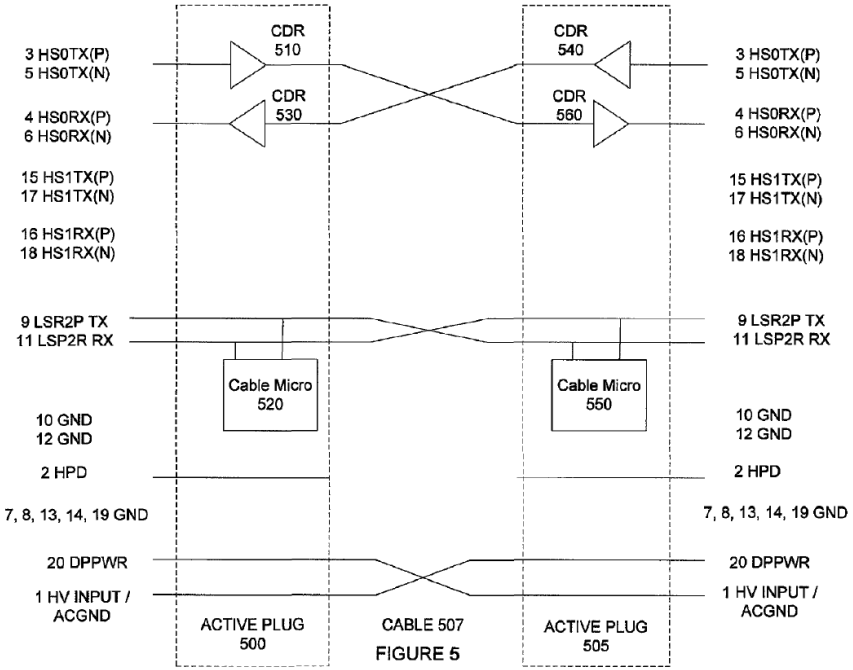
Claim 3	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 3	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

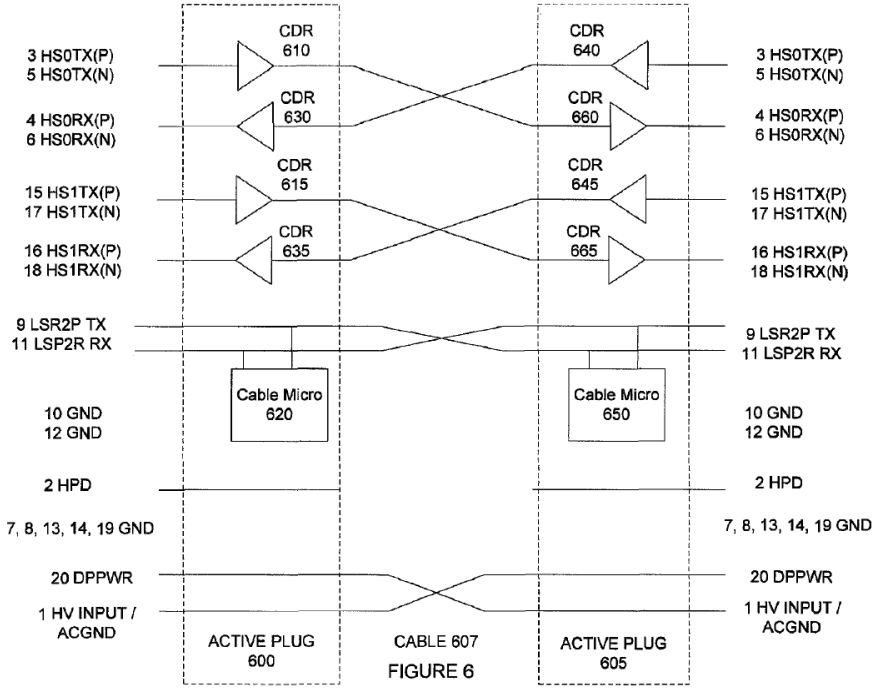
Claim 3	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 3	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

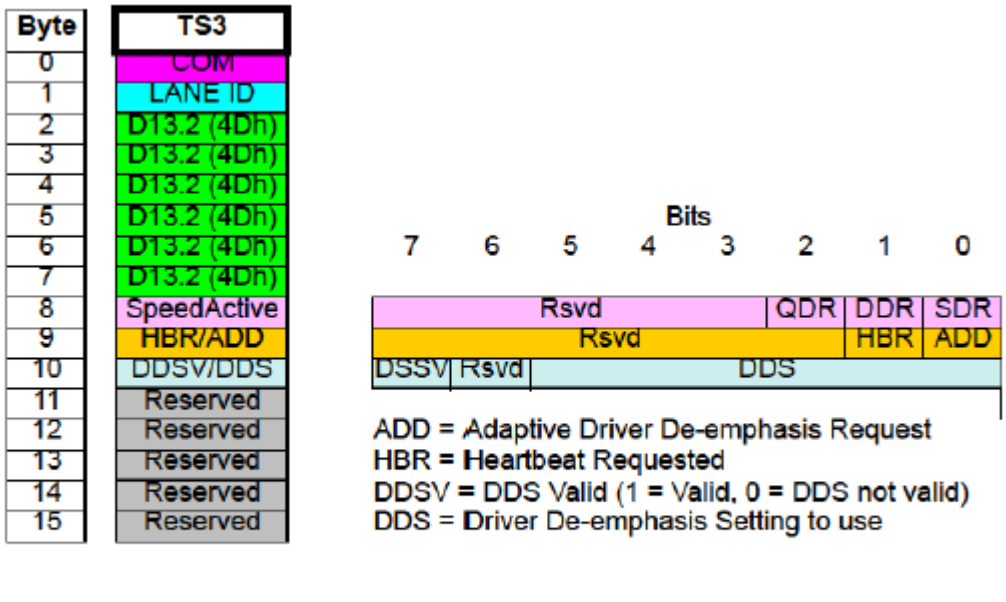
Claim 3	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 3	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 3	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 3	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 3	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 3	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 3	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

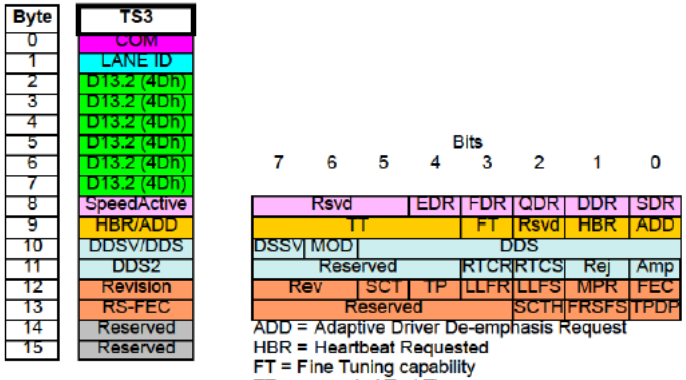
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 3	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 3	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 3	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 3	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 3	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 3	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 3	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 3	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

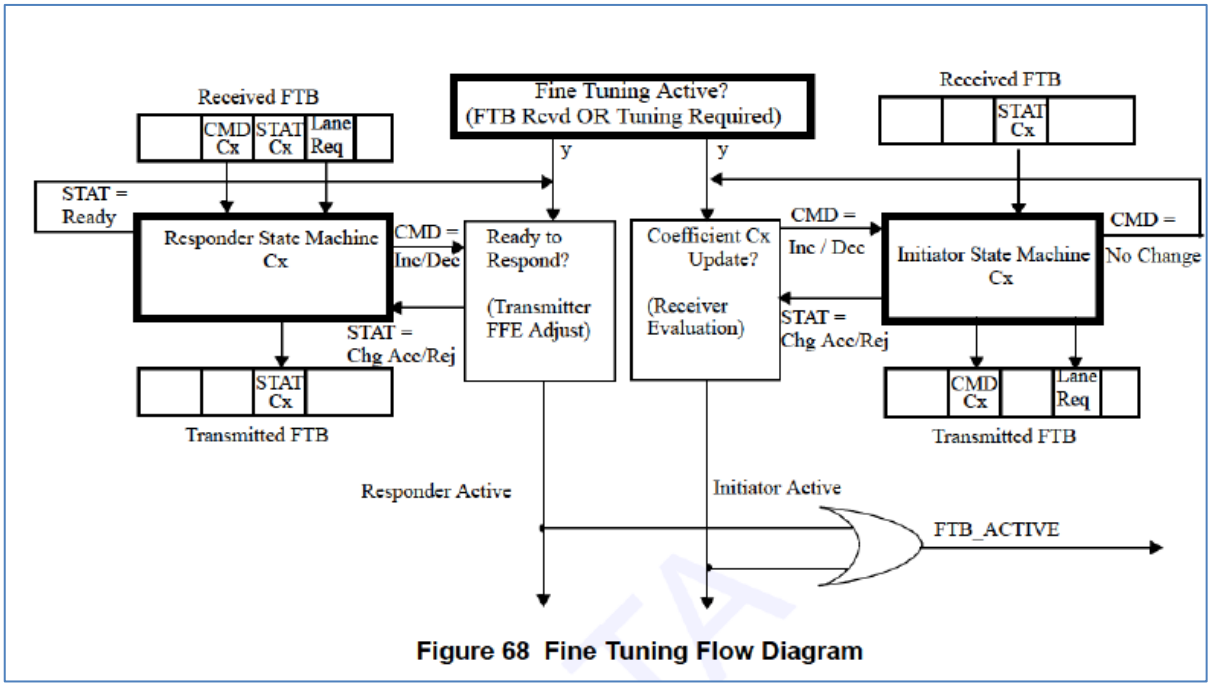
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 3	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 3	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 3	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required

Addr	Size	Type	Functions
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required

Addr	Size	Type	Functions
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional

Addr	Size	Type	Functions
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional

Addr	Size	Type	Functions
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies

Addr	Size	Type	Functions
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 3	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 3	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 3	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"The overall pre-equalizer **800** can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."
Rafie, paragraph 82.

U.S. Patent Publication No. 2014/0281067 ("Das Sharma")

Das Sharma describes pre-equalization "on a per transmitter-receiver pair basis to ensure interoperability" between the transmitter and the receiver in compensating for the channel's distortion. *See, e.g.*, Das Sharma at [0064]. An ordinarily skilled artisan knew that at least some of the different channel models

Claim 3	Disclosure
	presume different types of receiver equalization to ensure interoperability between different transmitter-receiver pairs, to ensure that they each mitigate channel degradation. *See, e.g.*, Das Sharma at [0064]. **1 Features** • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 3	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 3	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

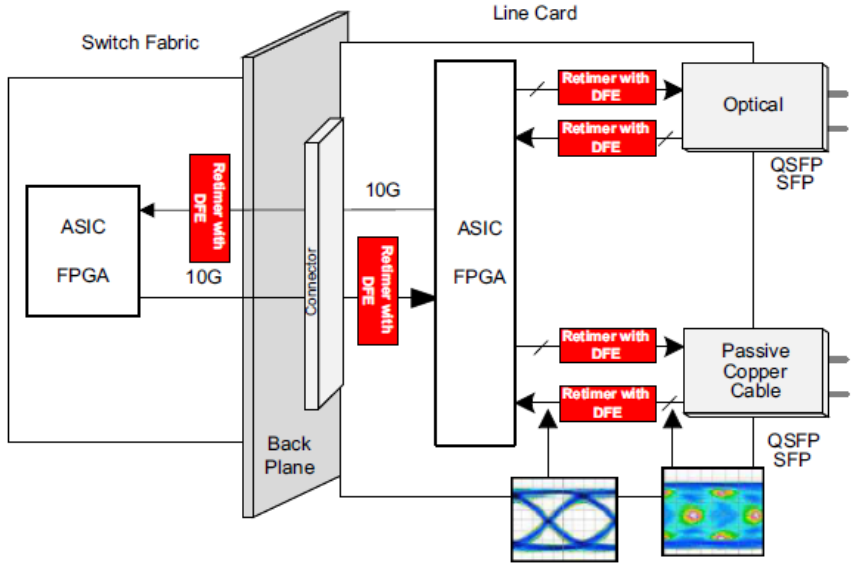
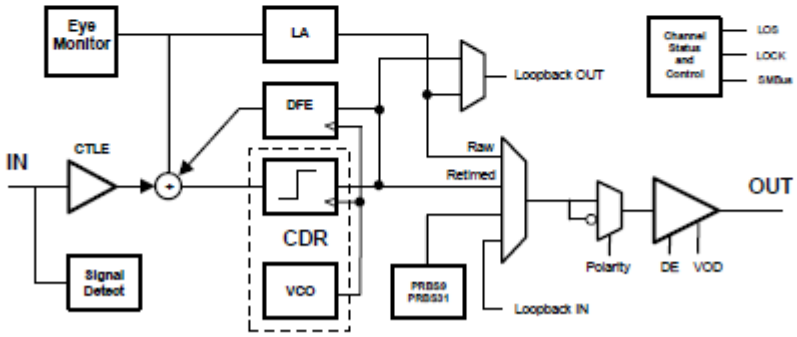


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 3	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 3	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 3	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

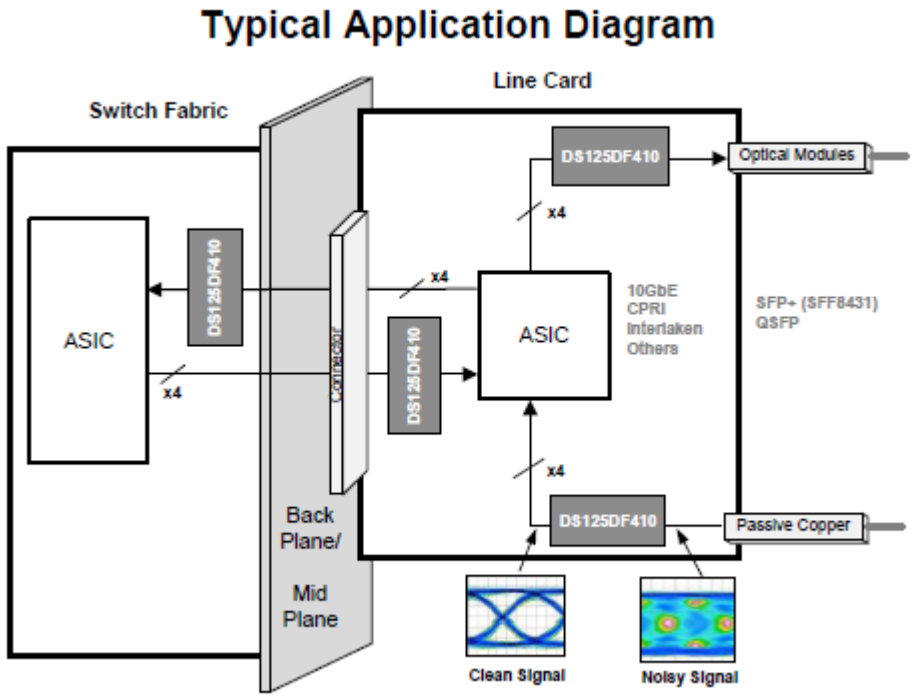
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

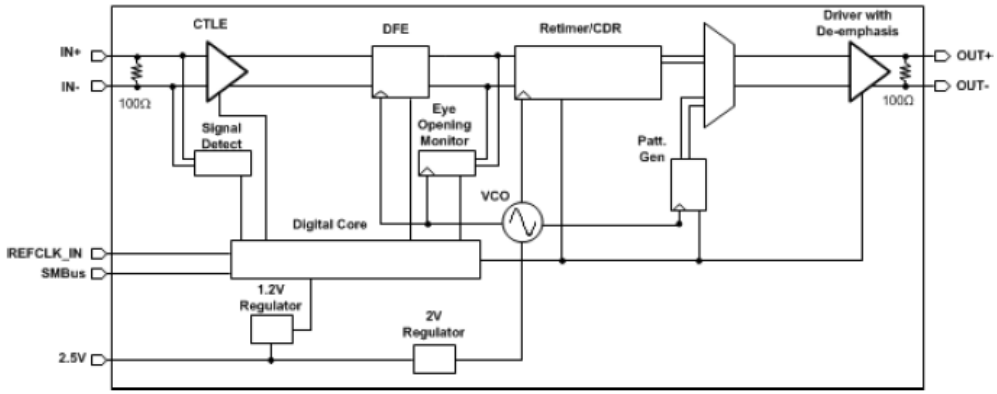
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 3	Disclosure
	 TI DS125DF410, 1.

Claim 3	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 3	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 3	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 3	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 3	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 3	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 3	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 3	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 3	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

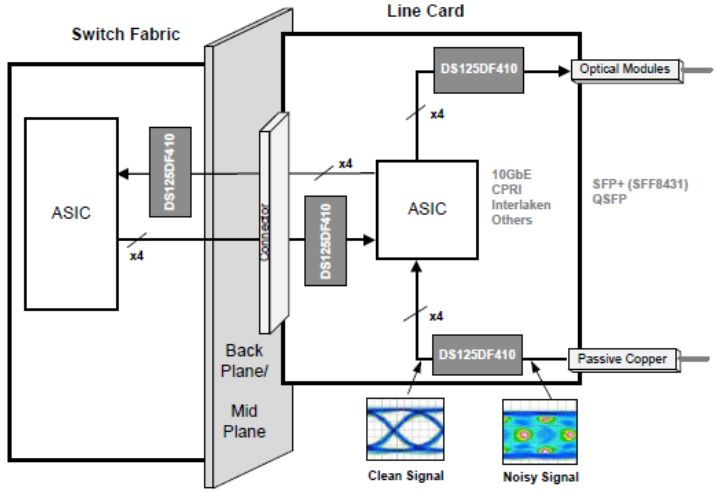
TI DS125DF410, 41.

Claim 3	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 3	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 3	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 3	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

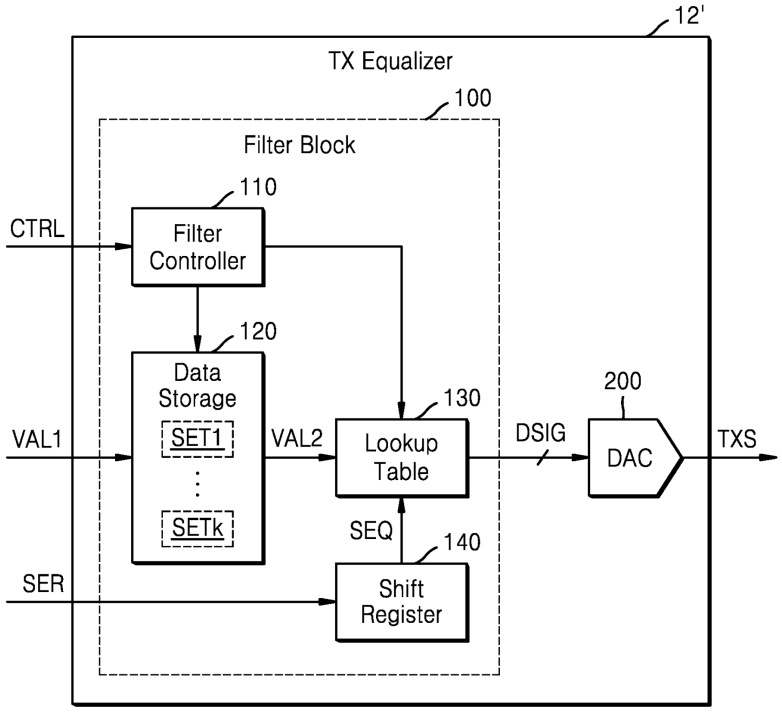
D. DEPENDENT CLAIM 4

Claim 4	Disclosure
4. The method of claim 1, wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

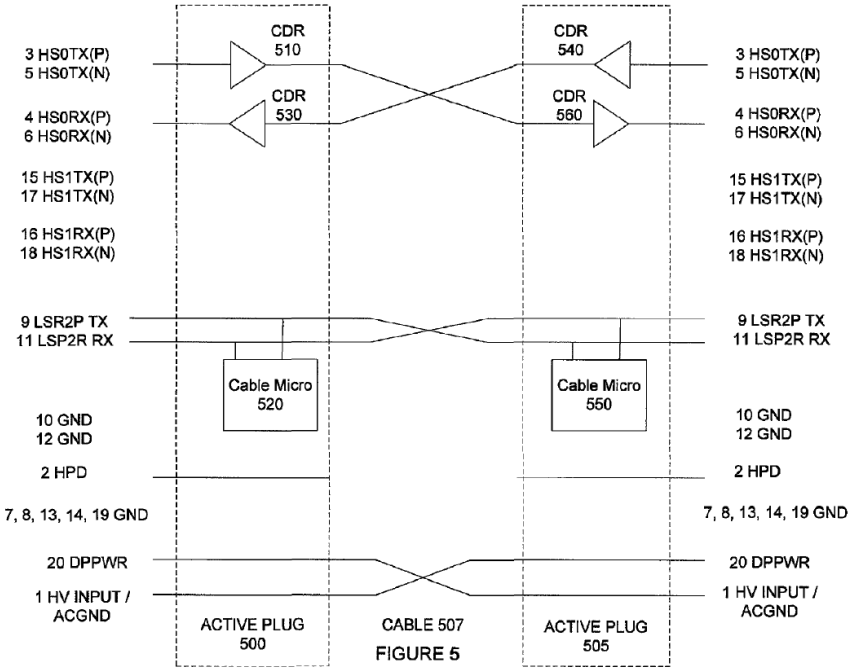
Claim 4	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 4	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

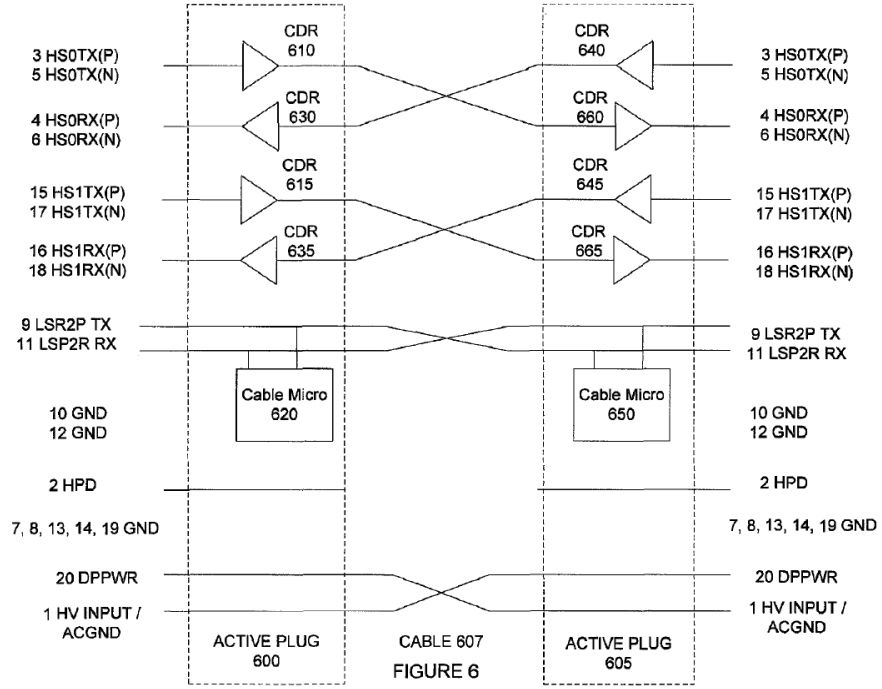
Claim 4	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 4	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 4	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

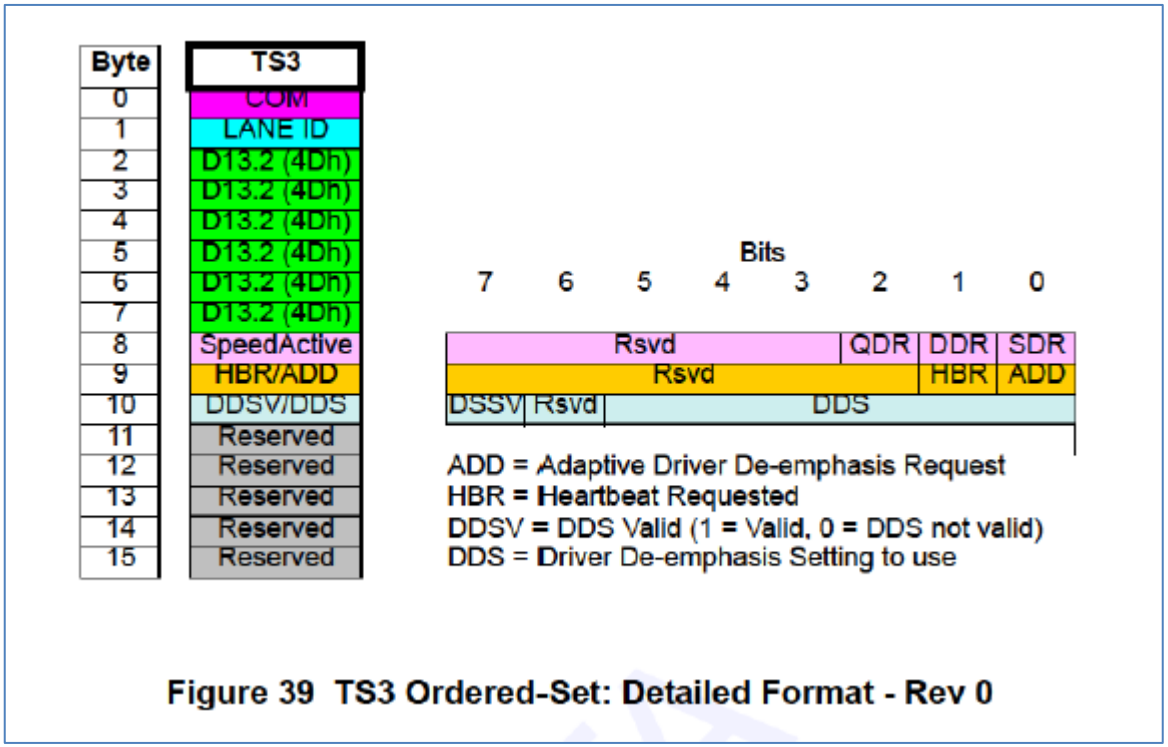
Claim 4	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 4	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 4	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 4	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 4	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 4	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

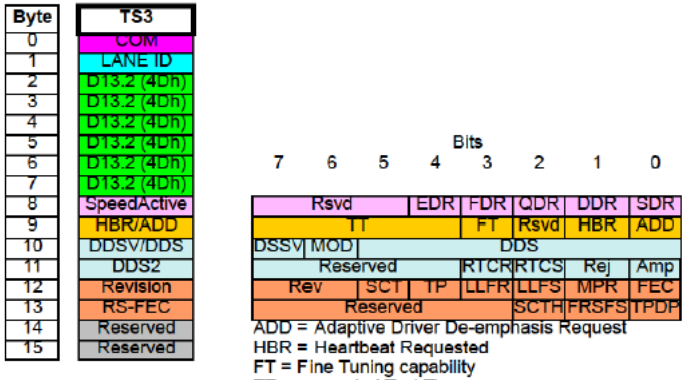
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 4	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits	7	6	5	4	3	2	1	0
	Rsvd			EDR	FDR	QDR	DDR	SDR
	TT				FT	Rsvd	HBR	ADD
	DSSV	MOD	DDS					
	Reserved				RTCR	RTCS	Rej	Amp
	Rev		SCT	TP	LLFR	LLFS	MPR	FEC
	Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 4	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 4	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 4	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 4	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 4	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 4	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 4	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

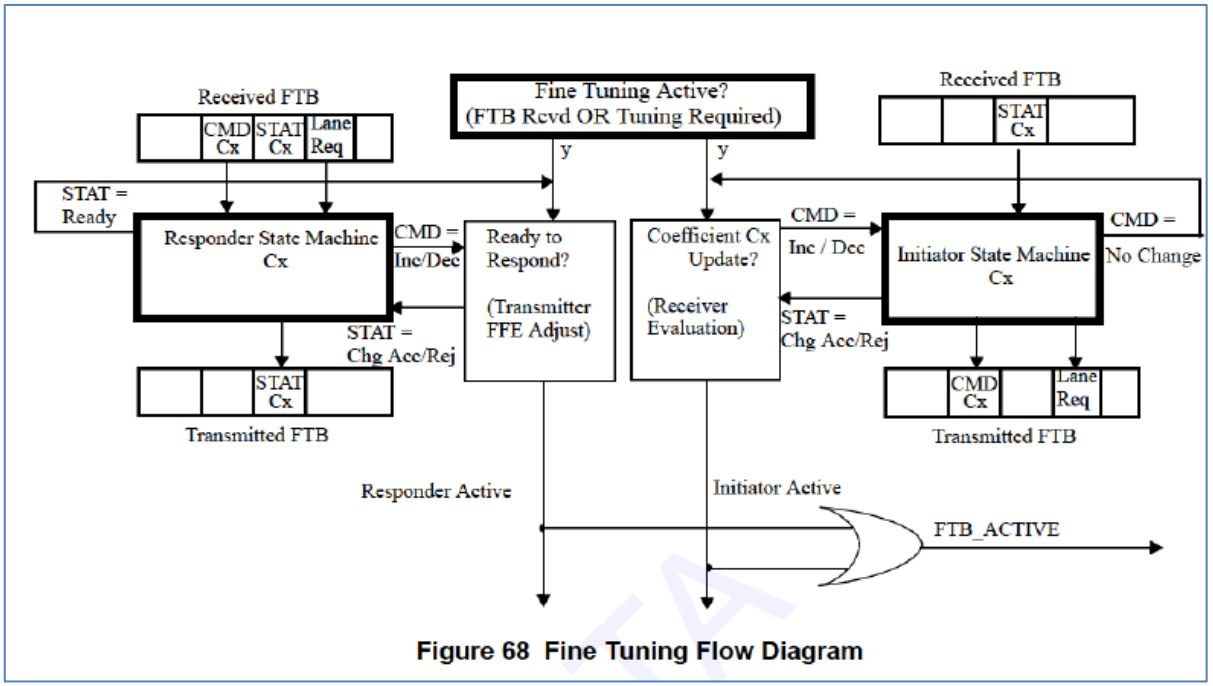
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 4	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 4	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 4	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required

Addr	Size	Type	Functions
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required

Addr	Size	Type	Functions
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional

Addr	Size	Type	Functions
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional

Addr	Size	Type	Functions
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies

Addr	Size	Type	Functions
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 4	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 4	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 4	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"In step **308**, a determination is made as to whether power thresholds for pre-equalization coefficients ahs been exceeded. In this step, when a CM is transmitting data during a DOCSIS periodic ranging process, pre-equalization coefficients are calculated."

Fox, p. 10.

"Once the initial QAM modulation order and R-S FEC parameters have been set, the system enters a "tracking" or "maintenance" mode, as shown in detail in the process steps **400** illustrated in **FIG. 4.** Specifically, the process steps **400** utilize ongoing CMTS receiver measurements, such as bit error rates,

Claim 4	Disclosure
	modulation error rates, and power measurements, to continually recalculate and optimize various CMTS receiver parameters in each channel's profile." Fox, p. 11. <u>*U.S. Patent Publication No. 2014/0281067 ("Das Sharma")*</u> Das Sharma discloses determining at the port transceiver which set of coefficients had the best performance characteristic (e.g., produced a signal with the smallest error). *See, e.g.*, Das Sharma at [0081] (describing testing multiple different sets of coefficients in an iterative fashion and determining a bit error rate for each). The '111 Patent describes testing each set of coefficients and selecting one that best performs best based on a performance characteristic such as "an error signal energy" or a "bit error rate." *See, e.g.*, '111 Patent at 2:4-5, 14:12-43, claims 5-6. The specification's only description supporting claim 4's selection of the register with the best performing coefficients is Figure 8, steps 802-812. *See id*. at 14:12-15:3. That disclosure describes actions by "training controller link or link controller" that receives test signals (steps 808 and 818) and selects the best performing register on a "***remote*** transmitter" that transmitted the test signals. *See id*. at 14:12-56. The "***remote*** transmitter" is "instructed to use those preset coefficients" from a register selected in step 812 "as a starting point" and "programs the pre-equalizer with the preset coefficients from the selected register and transmits a training pattern and/or data." *See id*. at 14:38-43. <u>*United States Patent No. 7,239,665 ("Mezer")*</u> Mezer discloses a selection is made from among the registers storing different sets of pre-computed pre-equalization coefficients by having the pluggable module transceiver send different instances of a test signal that were pre-equalized with the different set of coefficients and then selecting (at either the pluggable module transceiver or the port transceiver) the set of coefficients that performed best. *See, e.g.*,

Claim 4	Disclosure
	Mezer, 6:50-57 (describing determining a "channel type[]" to select between the different pre-computed channel models associated with different channel types). **1 Features** • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 4	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 4	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

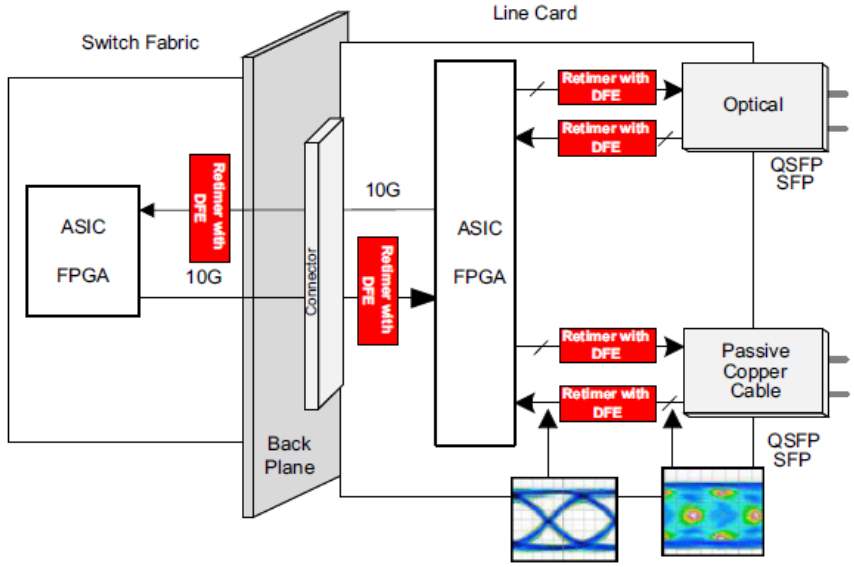
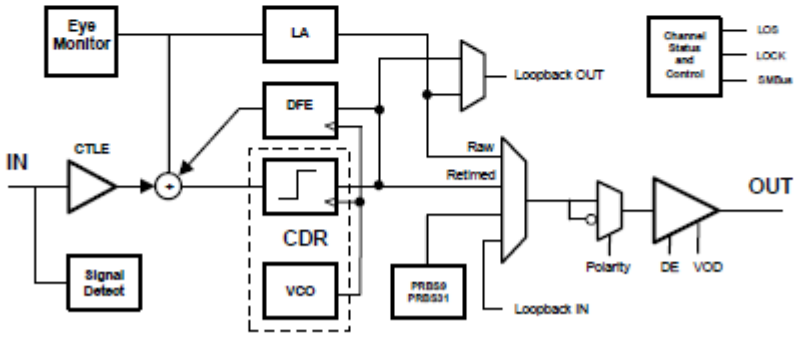


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 4	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 4	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 4	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

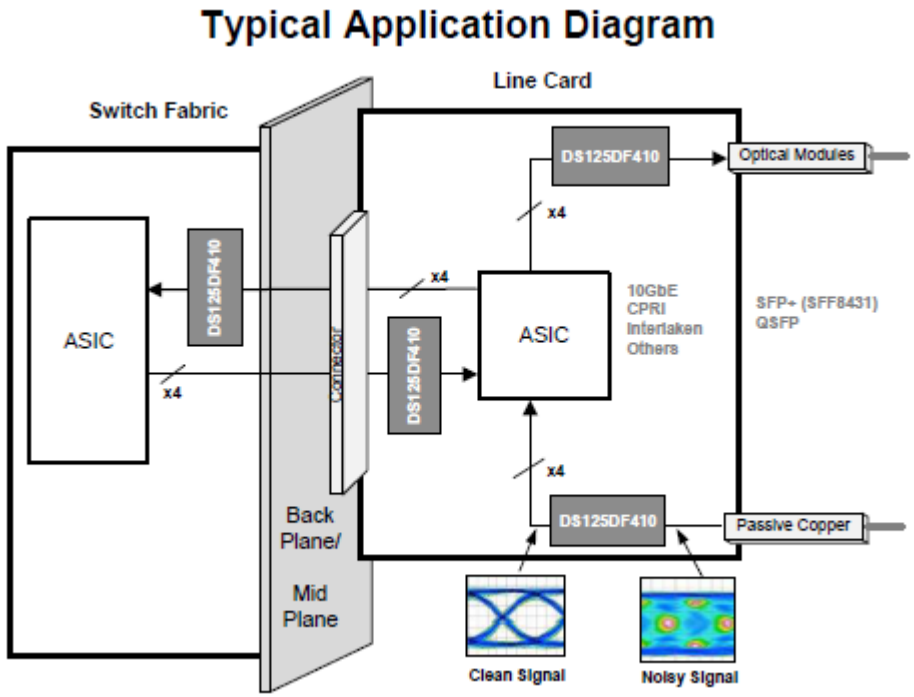
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

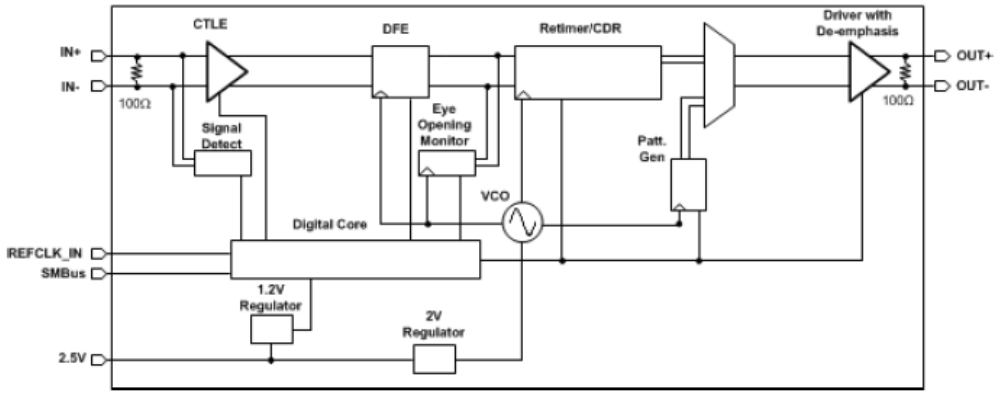
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 4	Disclosure
	 TI DS125DF410, 1.

Claim 4	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 4	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 4	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 4	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 4	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 4	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 4	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 4	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 4	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

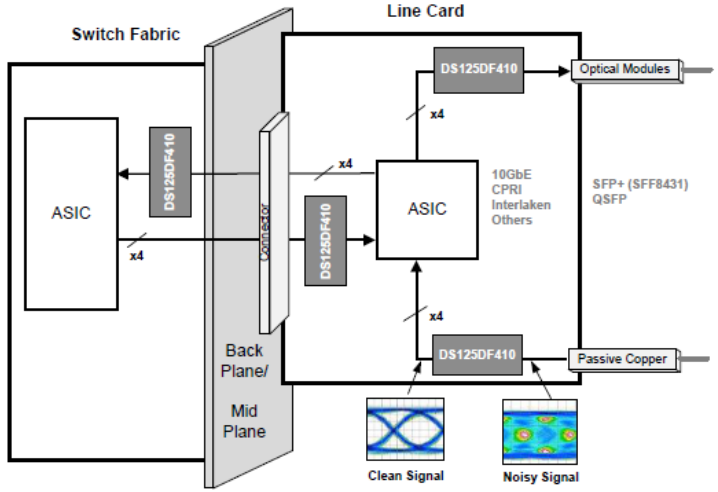
TI DS125DF410, 41.

Claim 4	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 4	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 4	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 4	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

Claim 4	Disclosure

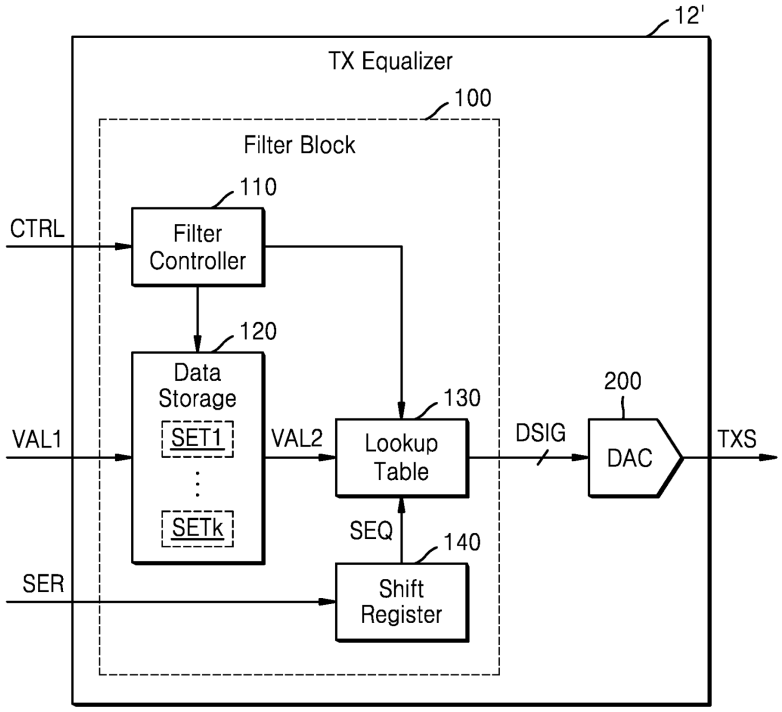
E. DEPENDENT CLAIM 5

Claim 5	Disclosure
5. The method of claim 4, wherein the performance characteristic is an error signal energy.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

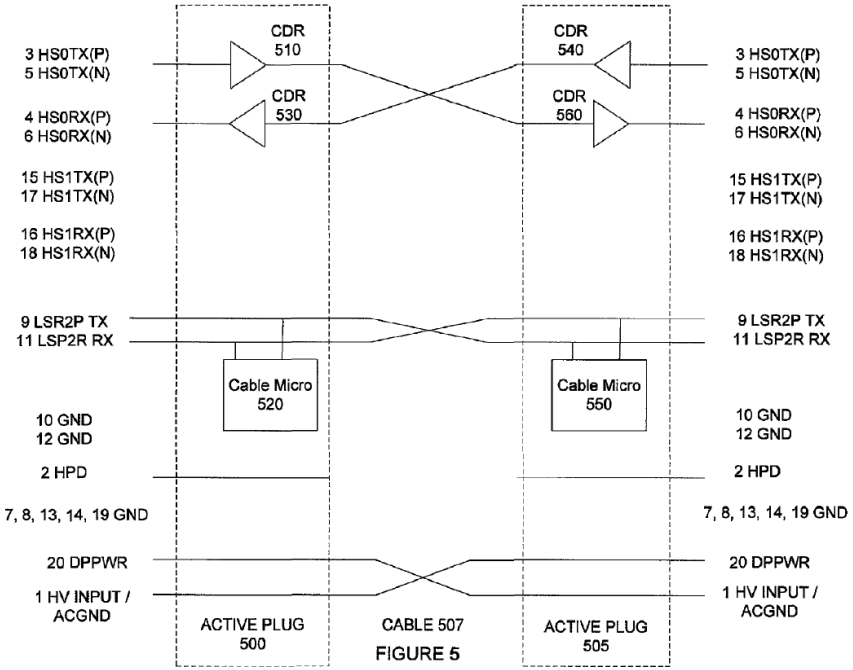
Claim 5	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 5	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

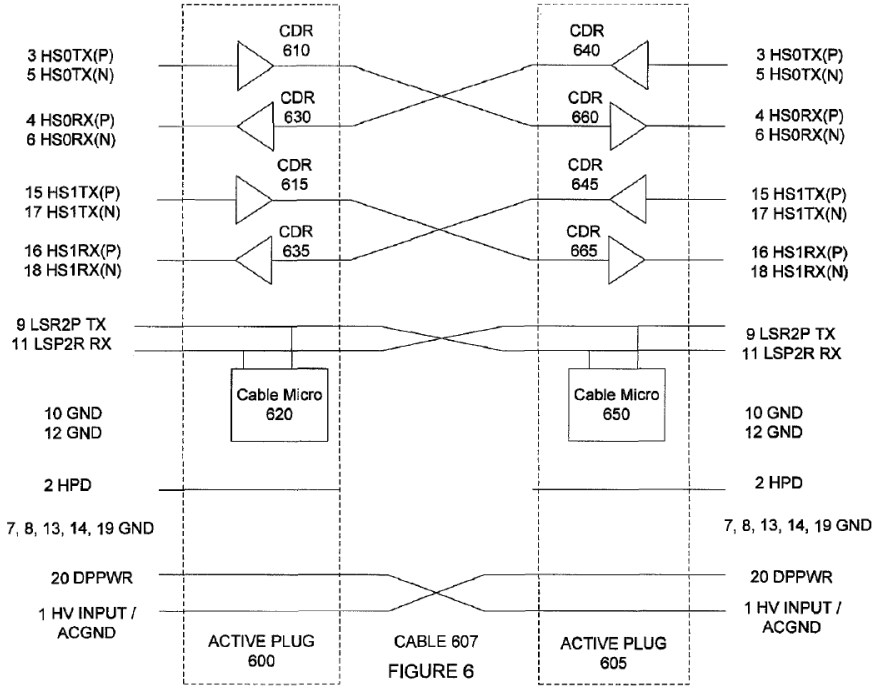
Claim 5	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 5	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 5	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

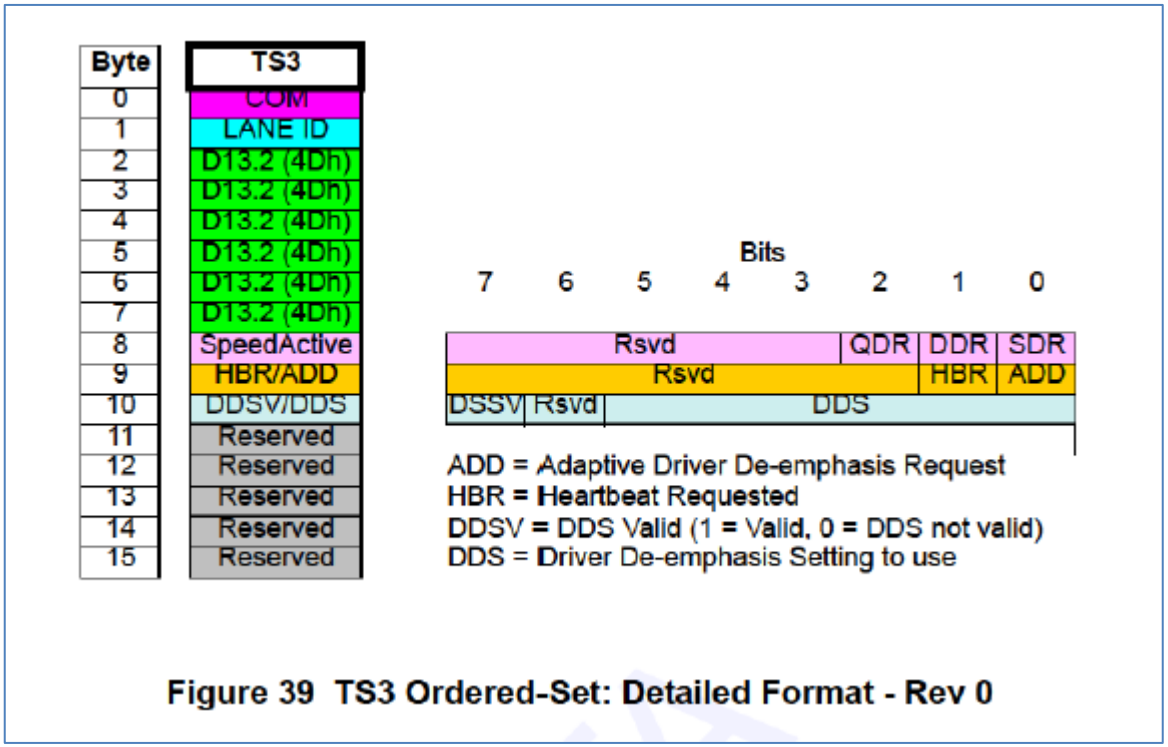
Claim 5	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 5	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 5	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 5	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 5	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 5	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

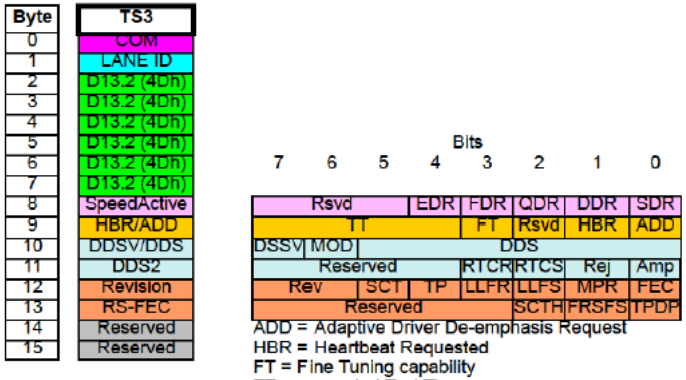
Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 5	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 5	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 5	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 5	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 5	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 5	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 5	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 5	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

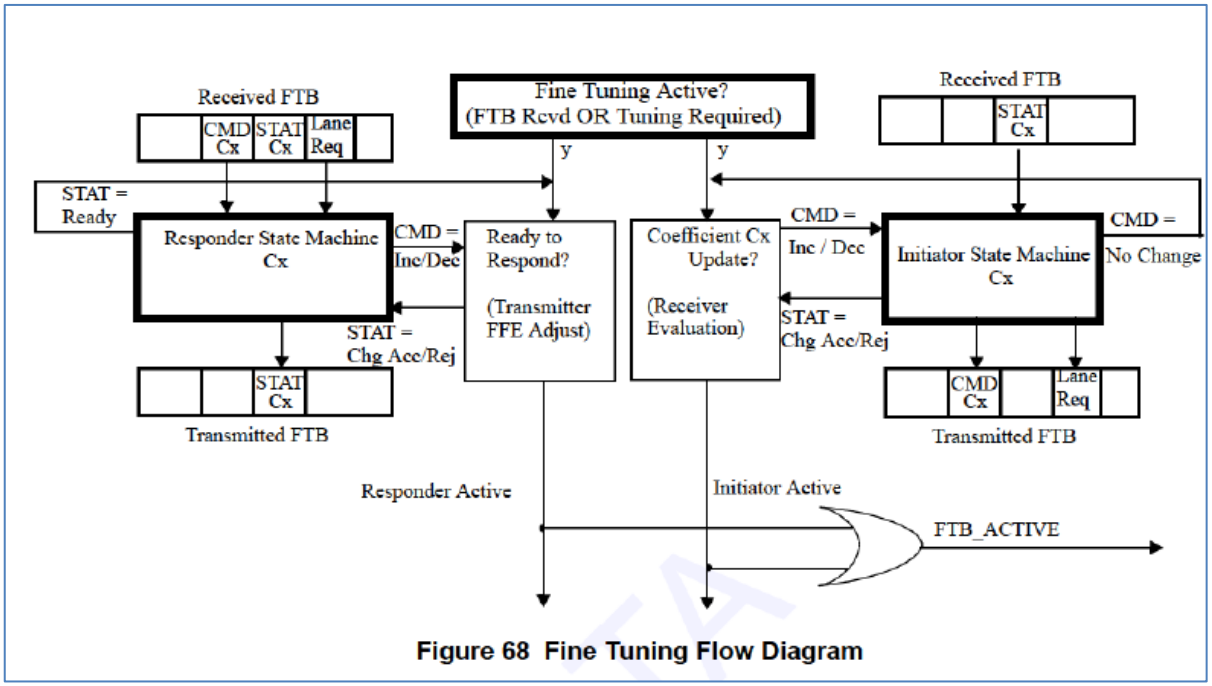
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 5	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 5	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 5	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 5	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 5	Disclosure
	Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 5	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"Once the initial QAM modulation order and R-S FEC parameters have been set, the system enters a "tracking" or "maintenance" mode, as shown in detail in the process steps 400 illustrated in FIG. 4. Specifically, the process steps 400 utilize ongoing CMTS receiver measurements, such as bit error rates, modulation error rates, and power measurements, to continually recalculate and optimize various CMTS receiver parameters in each channel's profile."

Fox, p. 11.

United States Patent No. 7,239,665 ("Mezer")

Mezer "adapt[s]" equalizer coefficients "on the basis of an error signal" that "indicates deviation of the" received training signal "from a pre-determined ideal signal profile." *See, e.g.*, Mezer, 2:27-49, 3:5-7. That

Claim 5	Disclosure
	meets the claimed "error signal energy." *See* '111 Patent at 14:29-30 ("measur[ing] error signals" represents "the difference between the equalized receive signals and an idealized receive signal"). **1 Features** • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 5	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 5	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

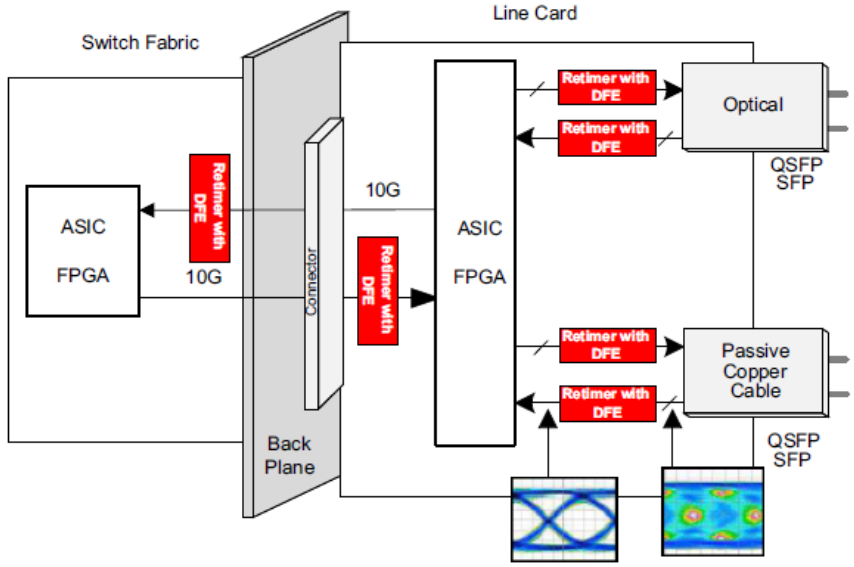
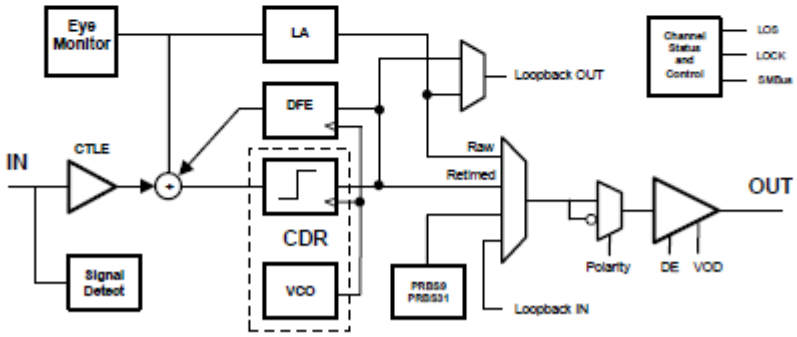


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 5	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 5	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 5	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

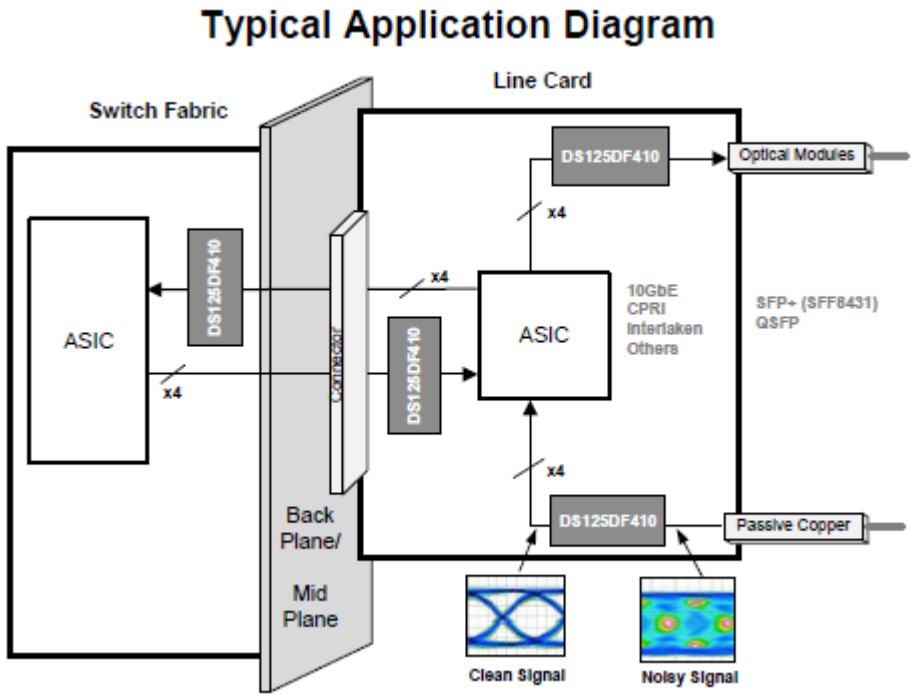
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

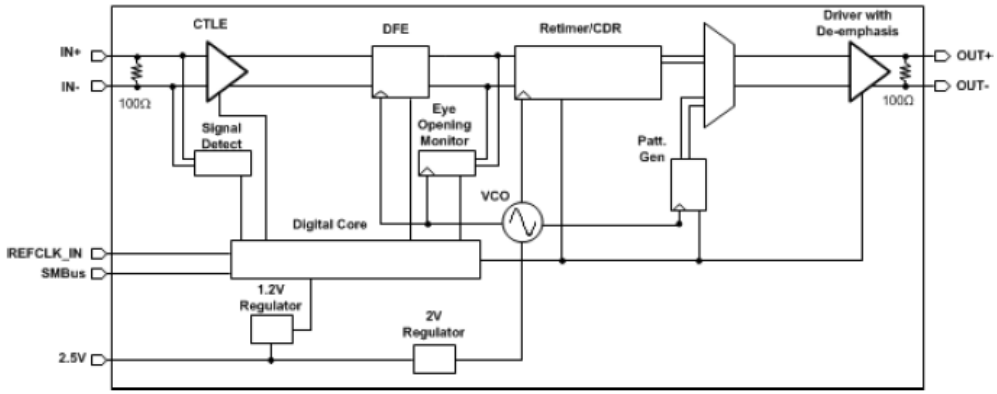
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 5	Disclosure
	 TI DS125DF410, 1.

Claim 5	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 5	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 5	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 5	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 5	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 5	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 5	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 5	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 5	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

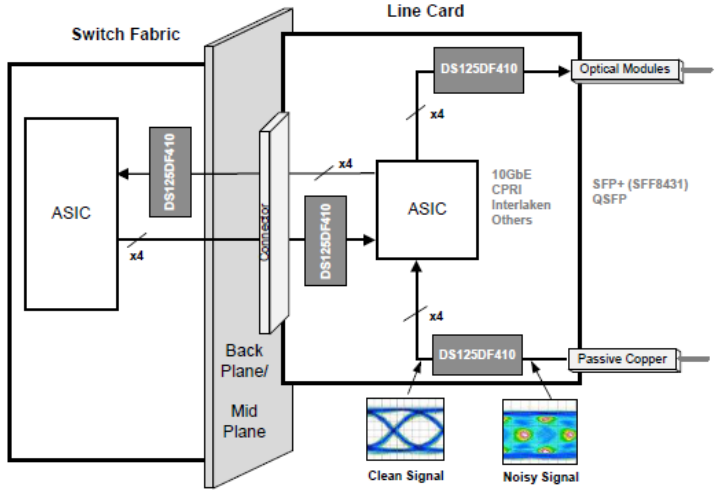
TI DS125DF410, 41.

Claim 5	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 5	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 5	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 5	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

Claim 5	Disclosure

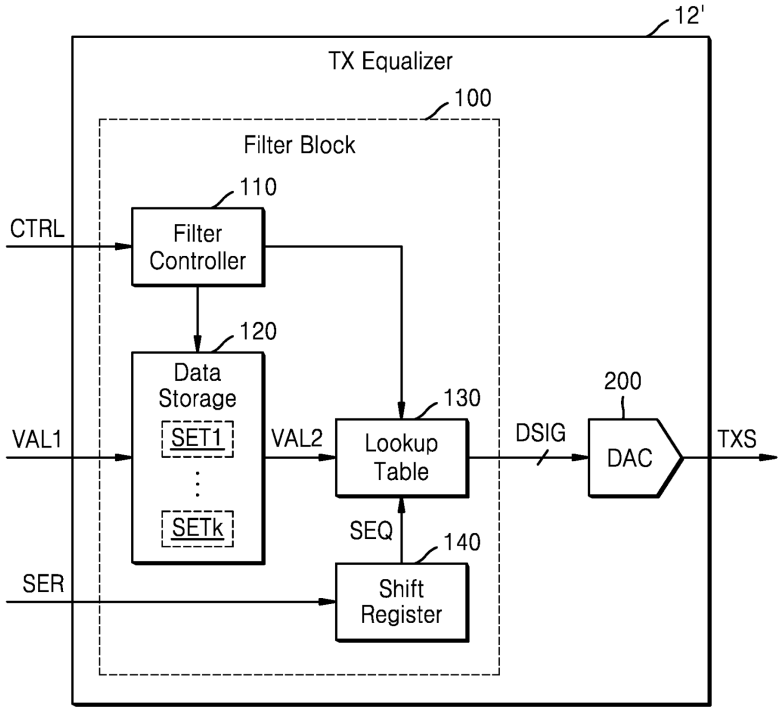
F. DEPENDENT CLAIM 6

Claim 6	Disclosure
6. The method of claim 4, wherein the performance characteristic is a bit error rate.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

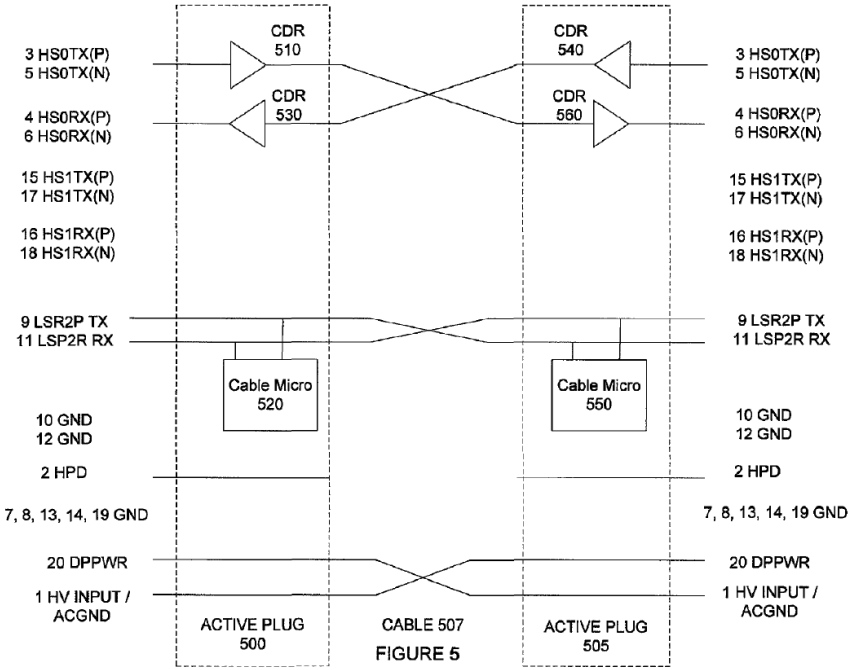
Claim 6	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 6	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

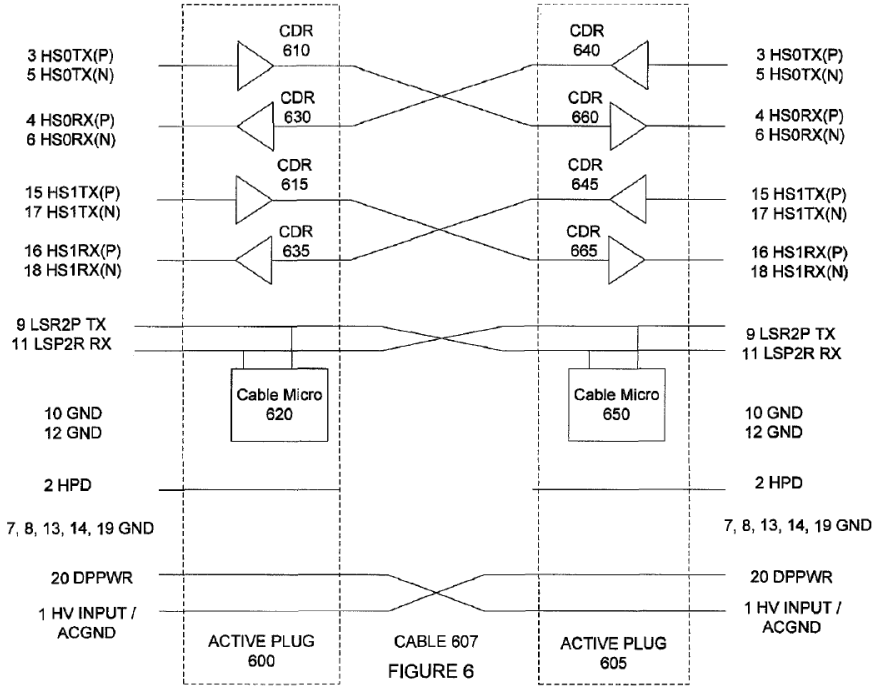
Claim 6	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 6	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 6	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

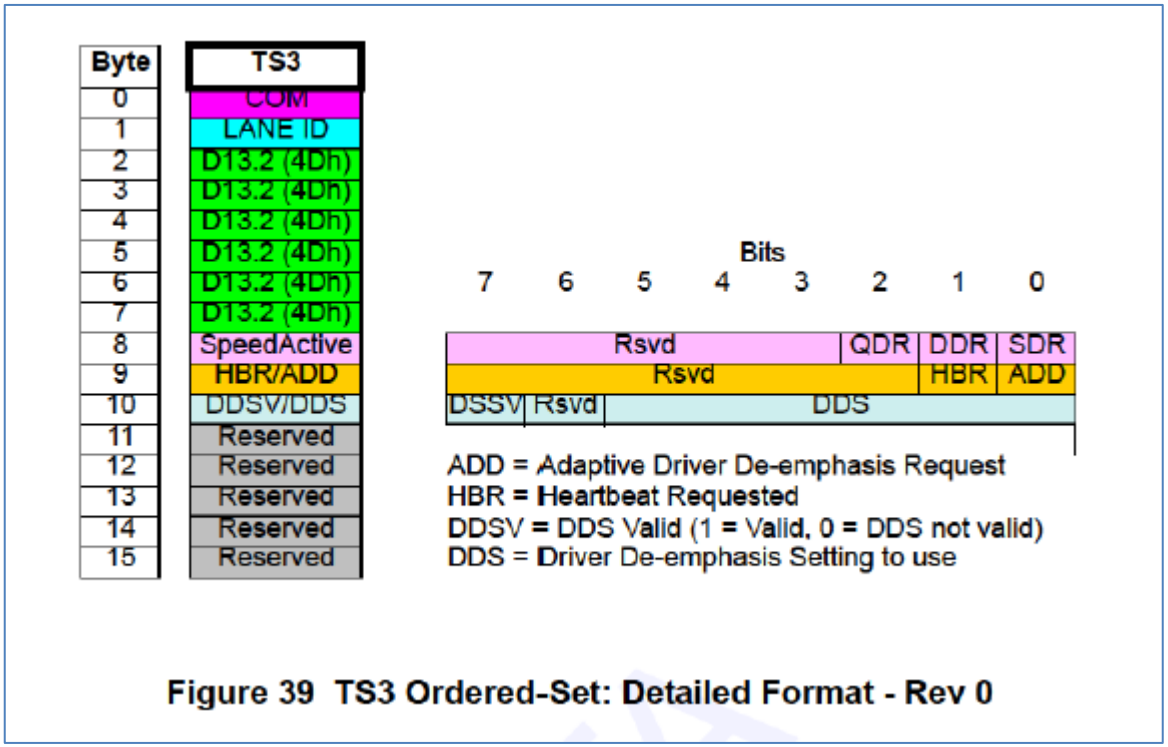
Claim 6	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 6	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 6	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 6	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 6	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 6	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

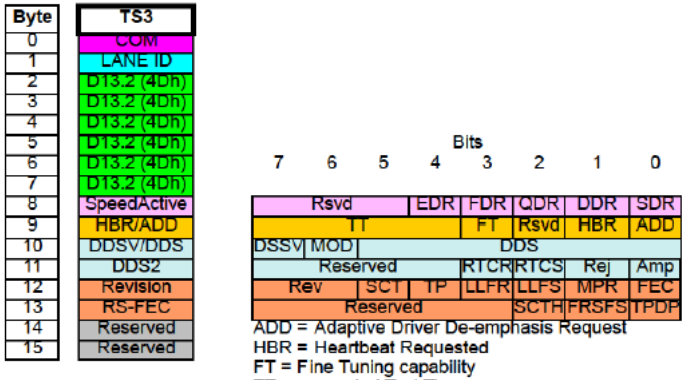
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 6	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 6	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 6	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 6	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 6	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 6	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 6	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 6	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

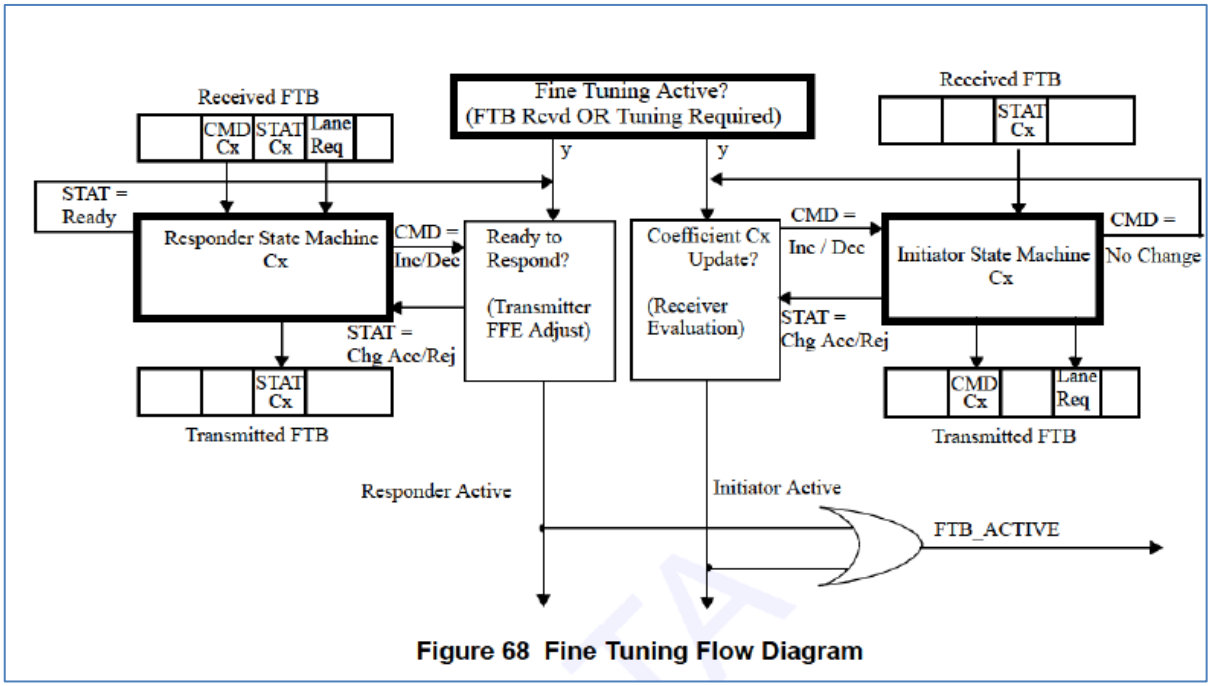
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 6	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 6	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 6	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required

Addr	Size	Type	Functions
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required

Addr	Size	Type	Functions
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional

Addr	Size	Type	Functions
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional

Addr	Size	Type	Functions
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies

Addr	Size	Type	Functions
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 6	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 6	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 6	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"Once the initial QAM modulation order and R-S FEC parameters have been set, the system enters a "tracking" or "maintenance" mode, as shown in detail in the process steps 400 illustrated in FIG. 4. Specifically, the process steps 400 utilize ongoing CMTS receiver measurements, such as bit error rates, modulation error rates, and power measurements, to continually recalculate and optimize various CMTS receiver parameters in each channel's profile."

Fox, p. 11.

	U.S. Patent Publication No. 2014/0281067 ("Das Sharma") Das Sharma teaches the use of bit error rate and explains that it may be "the ratio of the number of bits incorrectly received (errors) and the total number of bits received." *See, e.g.*, Das Sharma at [0076]-[0077]. **1 Features** • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 6	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 6	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

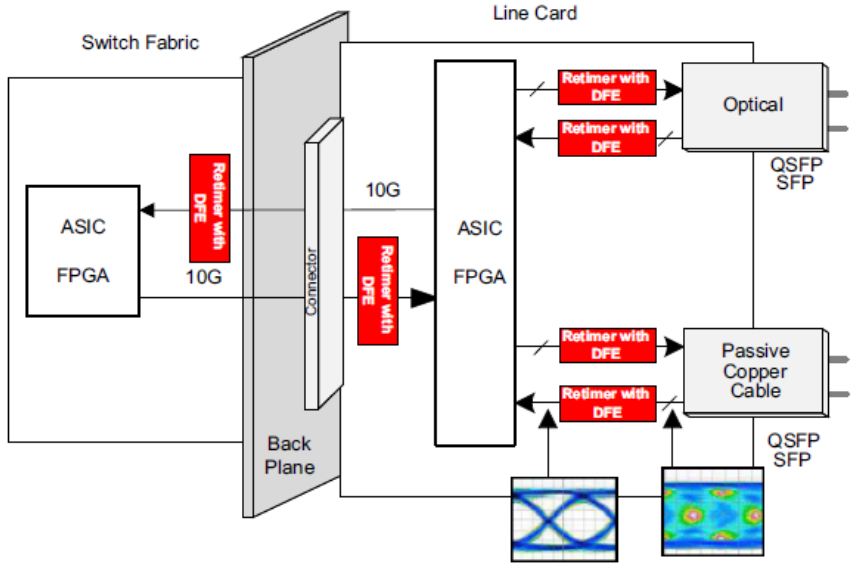
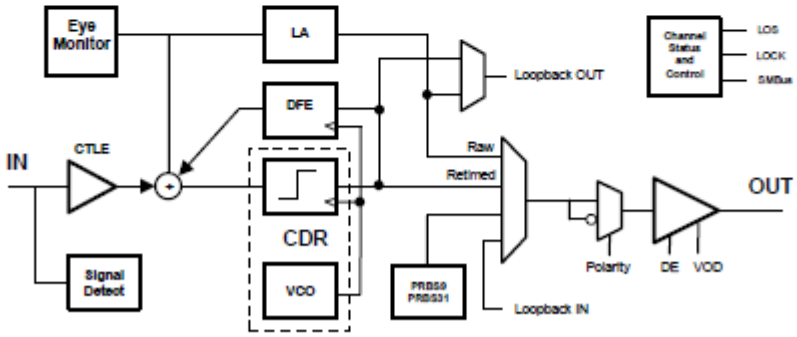


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 6	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 6	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 6	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

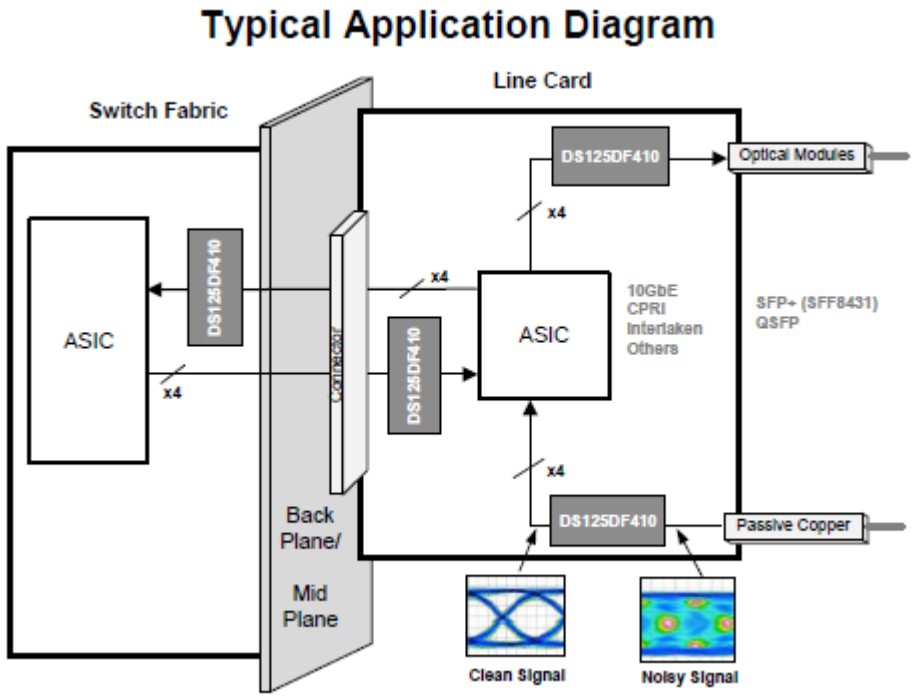
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

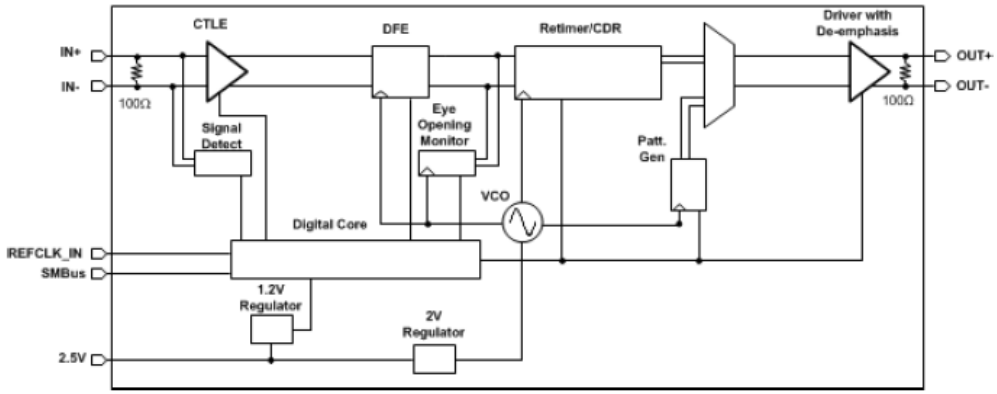
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 6	Disclosure
	 TI DS125DF410, 1.

Claim 6	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 6	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 6	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 6	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 6	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 6	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 6	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 6	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 6	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

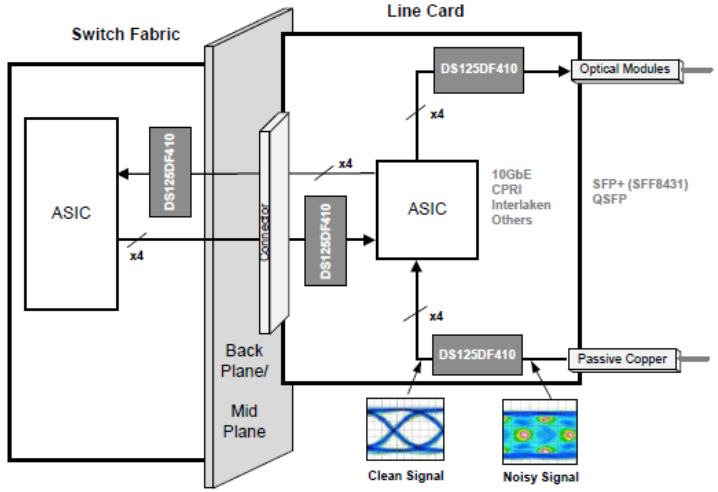
TI DS125DF410, 41.

Claim 6	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 6	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 6	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 6	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

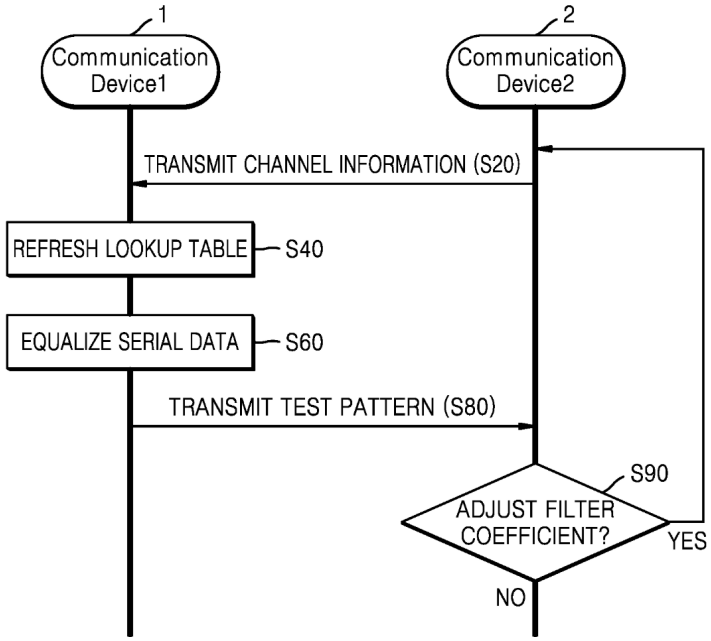
Exhibit C-12

Claim 6	Disclosure

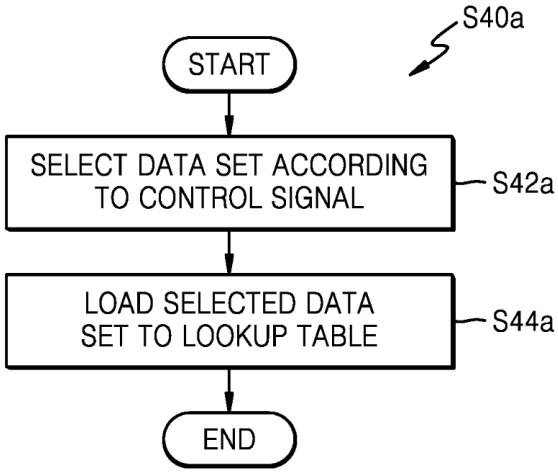
G. DEPENDENT CLAIM 7

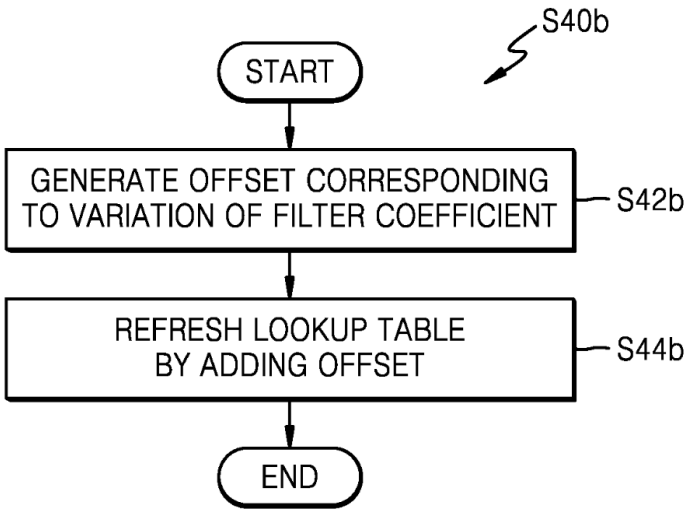
Claim 7	Disclosure
7. The method of claim 4, further comprising updating the selected register with the updated pre-equalizer coefficient values.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "FIG. 10 is a diagram illustrating an equalization method over time according to an exemplary embodiment of the disclosure. For example, the equalization method of FIG. 10 may be performed by the first communication device 1 including the TX equalizer 12 of FIG. 1 and the second communication device 2 communicating with the first communication device 1. The filter coefficients for equalization may be determined according to the equalization method illustrated in FIG. 10, and the method for determining the filter coefficients may be referred to as training of filter coefficients. It is assumed below that the first communication device 1 of FIG. 10 includes the components of the communication device 5 of FIG. 1, and FIG. 10 will be described with reference to FIG. 1. Referring to FIG. 10, in operation S20, the second communication device 2 may transmit channel information. For example, the second communication device 2 may first transmit, to the first communication device 1, channel information including information indicating one of the plurality of data sets, as described above with reference to FIG. 3. In operation S40, the first communication device 1 may refresh the lookup table LUT. For example, the protocol processor 30 of the first communication device 1 may extract information indicating a data set from the channel information received in operation S20 and may transmit the control signal CTRL

Claim 7	Disclosure
	including the extracted information to the TX equalizer 12. TX equalizer 12 may refresh the lookup table LUT based on the control signal CTRL. The lookup table LUT may include values of the digital signal DSIG corresponding to possible values of the symbol sequence extracted from the serial data SER. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information indicating a data set will be described with reference to FIG. 11. In operation S60, the first communication device 1 may equalize the serial data SER. For example, in the TX equalizer 12 of the first communication device 1, the lookup table LUT may output a digital signal (e.g., DSIG in FIG. 3) corresponding to the symbol sequence of the serial data SER, and the DAC 200 included in the TX equalizer 12 may convert the digital signal into an analog signal. Accordingly, an adder and a multiplier for multiplication and addition between the symbol sequence and the filter coefficient sequence for implementing the FIR filter 9 of FIG. 2 may be omitted. The example of operation S60 will be described with reference to FIG. 14. In operation S80, the first communication device 1 may transmit a test pattern. For example, the test pattern may include a pattern previously shared by the first communication device 1 and the second communication device 2, and the second communication device 2 may receive the test pattern through a channel (e.g., 7 of FIG. 1). In operation S90, the second communication device 2 may determine whether to adjust the filter coefficient. For example, the second communication device 2 may evaluate the test pattern received from the first communication device 1 and determine whether to adjust at least one of the coefficients of the FIR filter used for equalization of the first communication device 1 according to the evaluation result. As illustrated in FIG. 10, when it is determined not to adjust at least one of the filter coefficients, the training of the filter coefficients may be terminated and the first communication device 1 may transmit the signal, which is equalized according to the current filter coefficients, to the second communication device 2. On the other hand, when it is determined to adjust at least one of the filter coefficients, operation S20 may be performed. Unlike the initially performed operation S20, in operation S20, which is performed after operation S90, the second communication device 2 may transmit channel information, which includes information on the variation of the filter coefficients, to the first communication device 1. Thereafter, unlike the initially performed operation S40, in operation S40, the first communication device 1 may refresh the lookup table LUT based on the information on the variation of the filter coefficients. An example of operation S40 of

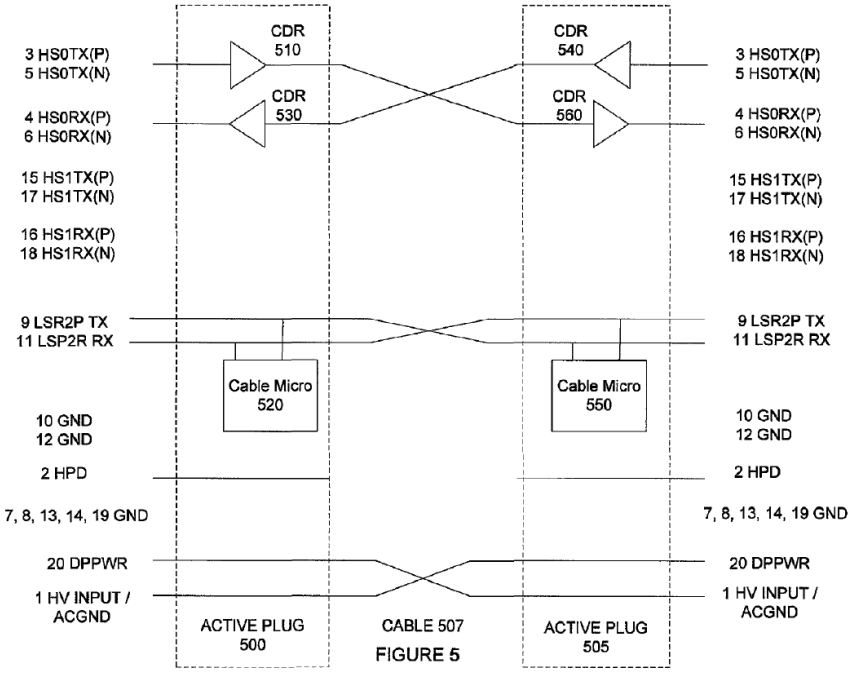
Claim 7	Disclosure
	refreshing the lookup table LUT in response to channel information including information on the variation of the filter coefficients will be described with reference to FIG. 12." Kang, 11:62-13:6 FIG. 10  Kang, FIG. 10 "Referring to FIG. 11, operation S**40** *a* may include operations S**42** *a* and S**44** *a*. In operation S**42** *a*, an operation of selecting a data set according to the control signal CTRL may be performed. For example, the controller **110** of FIG. 3 may receive a control signal CTRL including information indicating one of k

Claim 7	Disclosure
	filter coefficient sequences and may control the data storage **120** to output one of first to k-th data sets SET**1** to SETk, which are stored in the data storage **120**, according to the control signal CTRL. In operation S**44** *a*, an operation of loading the selected data set into the lookup table **130** may be performed. For example, the controller **110** may control the data storage **120** and the lookup table **130** to store the second value VAL**2** outputted from the data storage **120** in the lookup table **130**. Referring to FIG. 12, operation S**40** *b* may include operations S**42** *b* and S**44** *b*. In operation S**42** *b*, an operation of generating an offset OFF corresponding to the variation of the filter coefficients may be performed. For example, the offset generator **150** of FIG. 6 may generate an offset OFF, based on the variation signal VAR and the index IDX provided from the controller **110′**. The variation signal VAR may indicate at least one of up, down, hold, and reset of the filter coefficient and may include a variation amount of the filter coefficient. An example of generating the offset OFF when the variation signal VAR indicates the reset of the filter coefficient will be described later with reference to FIG. 13. In operation S**44** *b*, an operation of refreshing the lookup table **130′** may be performed by adding the offset OFF. In some embodiments, the offset generator **150** may generate a positive offset OFF or a negative offset OFF, and thus the calculator **160** may perform an addition. In some embodiments, the offset generator **150** may generate the positive offset OFF, and thus the calculator **160** may perform addition or subtraction according to the control of the controller **110′**. The lookup table **130′** may be refreshed by storing the output value of the calculator **160**, that is, the third value VAL**3**, in the lookup table **130′**." Kang, 13:18-54

Claim 7	Disclosure
	FIG. 11  Kang, FIG. 11

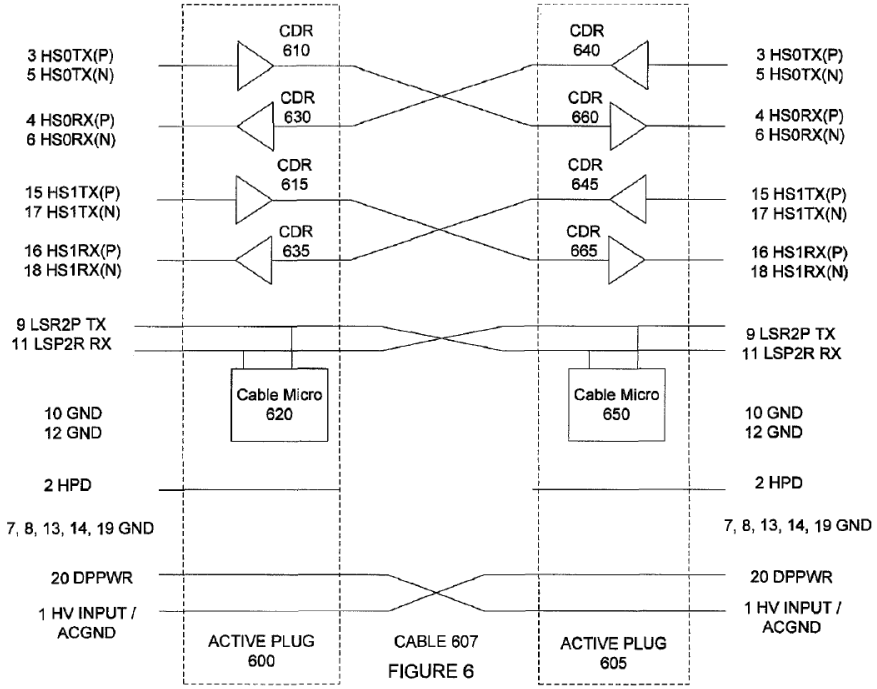
Claim 7	Disclosure
	FIG. 12  Kang, FIG. 12 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**. Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**.

Claim 7	Disclosure
	The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables. In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used.

Claim 7	Disclosure
	In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5 "FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock

Claim 7	Disclosure
	and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 7	Disclosure

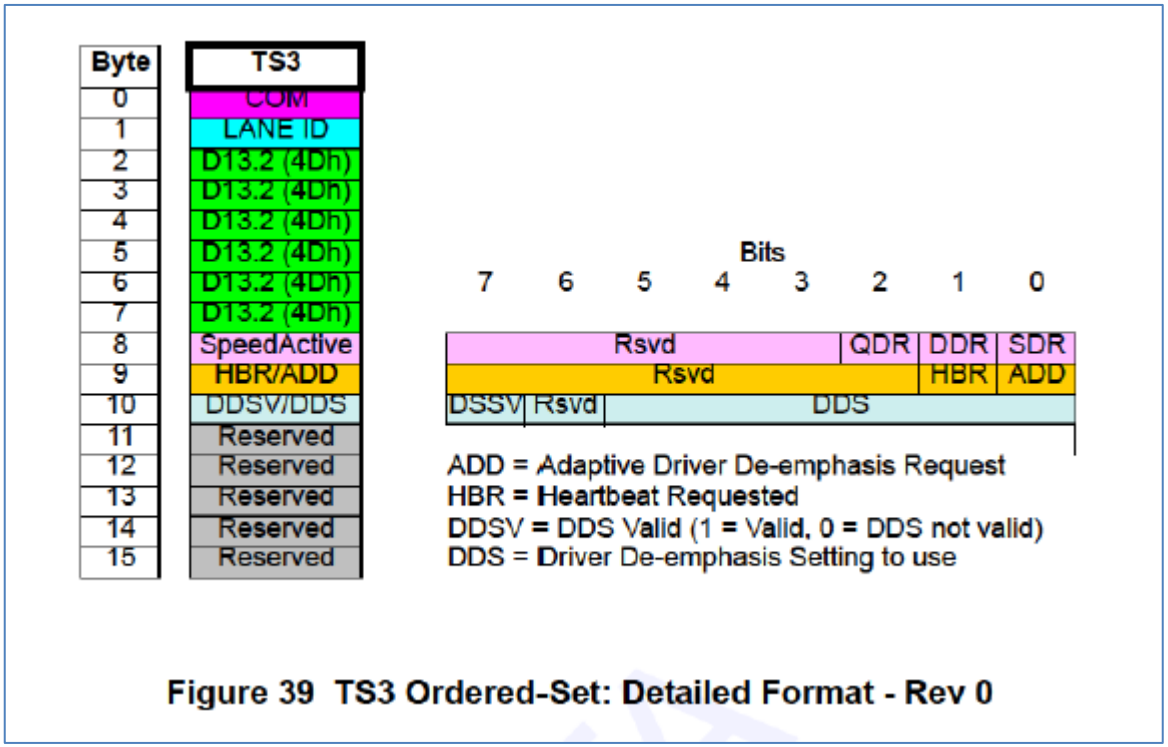


Cornelius, Figure 6

"In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 7	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 7	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 7	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

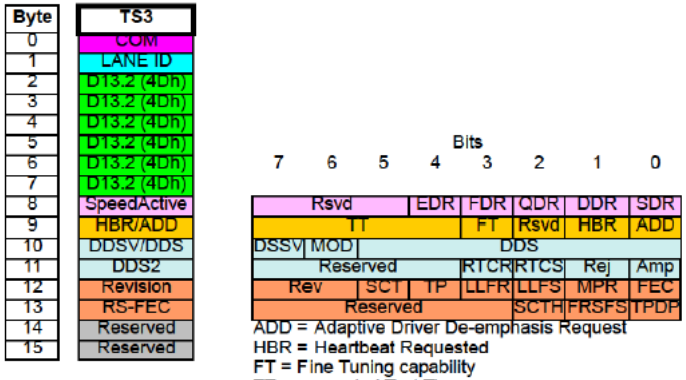
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 7	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 7	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 7	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 7	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 7	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 7	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 7	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 7	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

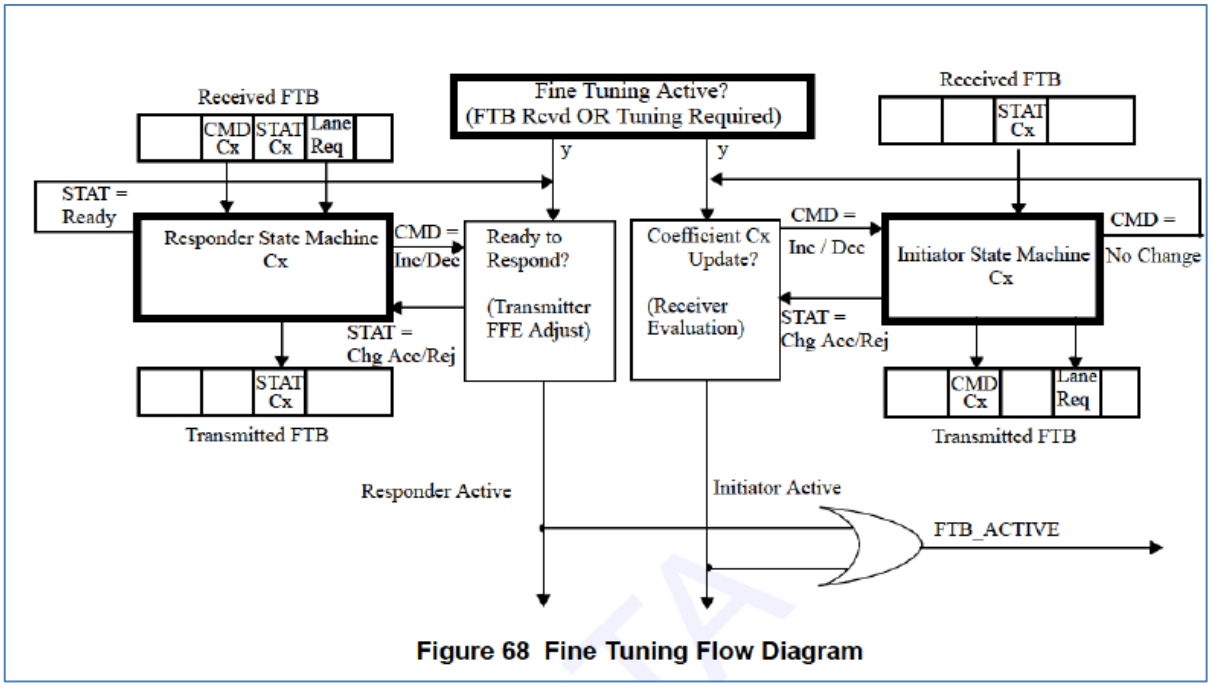
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 7	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 7	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 7	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required

Addr	Size	Type	Functions
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required

Addr	Size	Type	Functions
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional

Addr	Size	Type	Functions
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional

Addr	Size	Type	Functions
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies

Addr	Size	Type	Functions
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 7	Disclosure

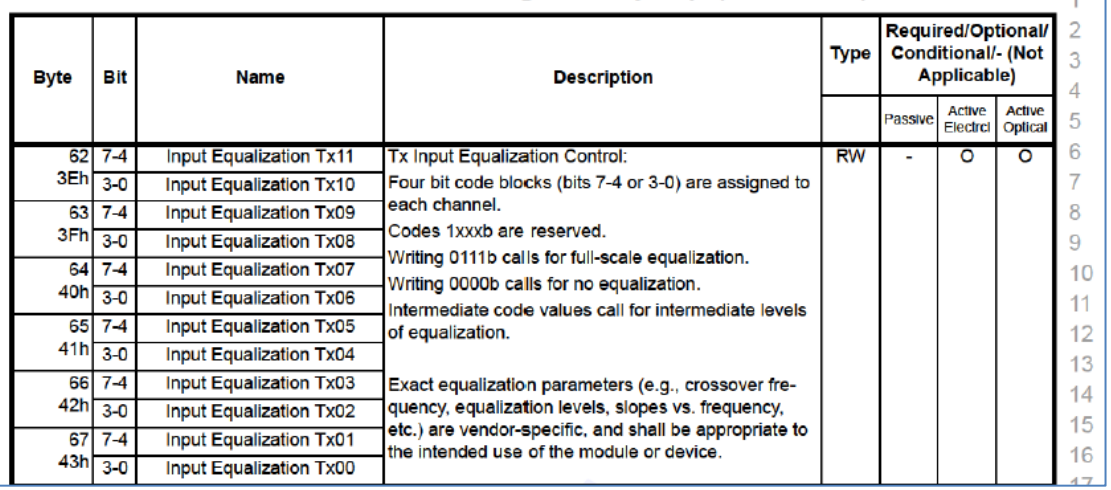
234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 7	Disclosure
	Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)  InfiniBand, Table 142 (p. 528)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

Claim 7	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"For instance, the transmitter device can be configured to select a first path to adaptively initialize the coefficients before data is transmitted and a second path to continuously adjust the coefficients while data is being transmitted. More particularly, the processing control logic **102** can be configured to select the presence transition equalization path **114** when there are presence change events for the RF carrier signal (e.g., events corresponding to when the RF carrier signal transitions between being present and being absent on the antenna **106**). Once data is being transmitted, with pre-equalization using the coefficients generated by path **114**, the processing control logic **102** can select the adaptive feedback equalization path **112**, which can include logic circuitry that is configured to continuously adjust the coefficients based upon feedback received from the antenna relative to the updated coefficients."
Ciacci, 4:39-54.

Claim 7	Disclosure
	"Once frequency response of front-end components has been characterized, this information can be stored in the digital base band on a configuration register (CFR), and thereby used to specify gain coefficients of the digital pre-equalizer." Balakrishnan, paragraph 27. <u>*U.S. Patent Publication No. 2014/0281067 ("Das Sharma")*</u> Das Sharma discloses a training phase during which the pre-equalizer coefficient values in a selected register for a transceiver filter are optimized to reduce the error rate. *See, e.g.*, Das Sharma at [0063], [0066], [0075], [0081], [0124], [0136].

Claim 7	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 7	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 7	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

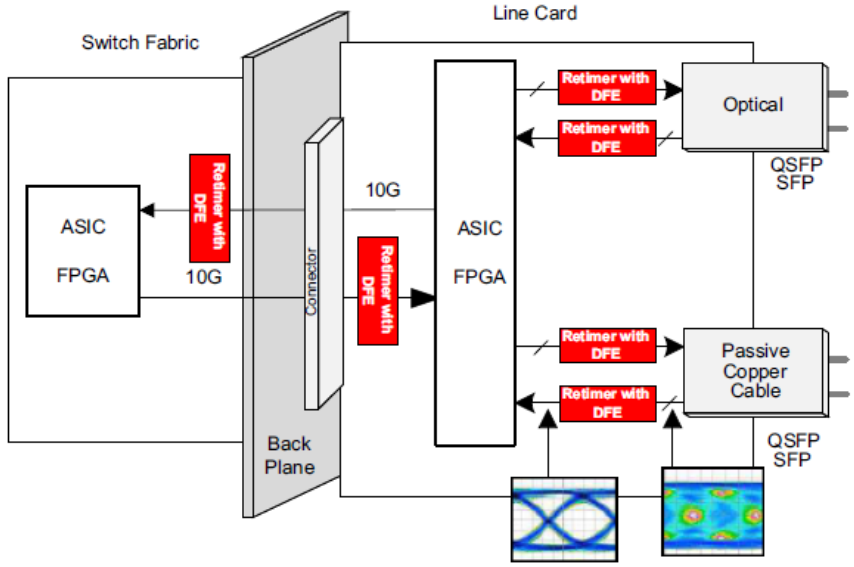
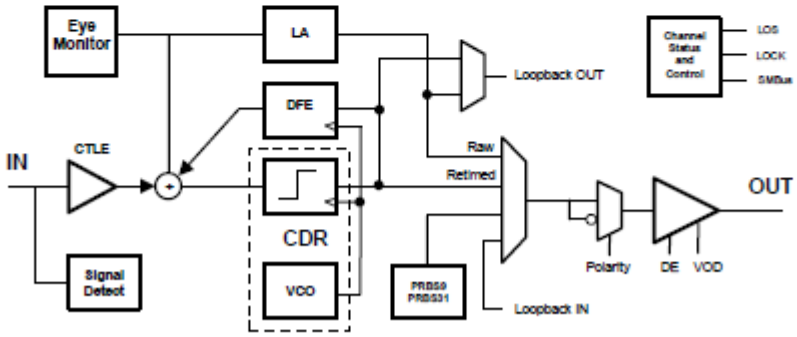


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 7	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 7	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 7	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

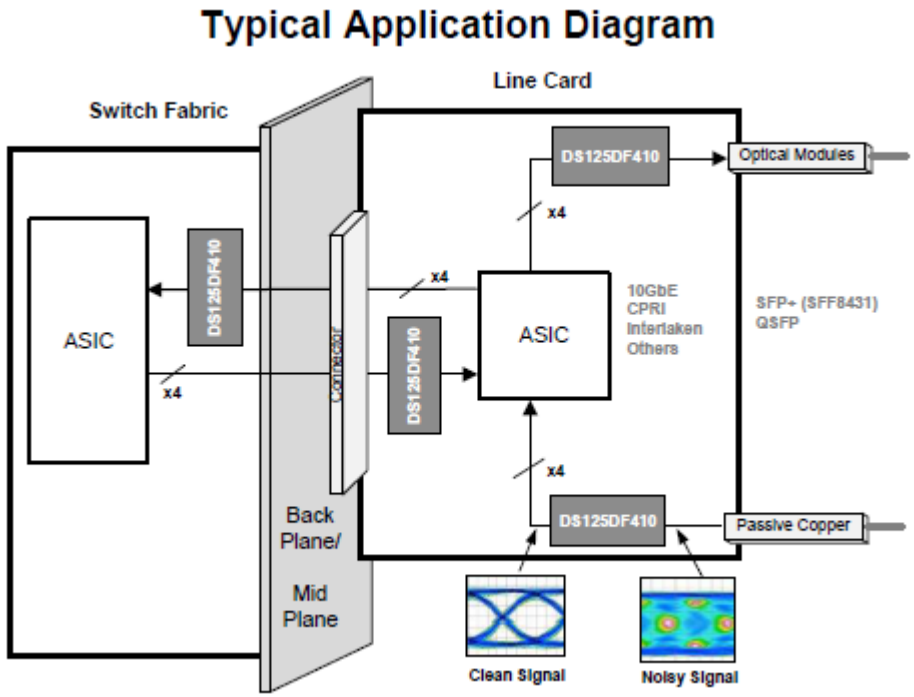
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

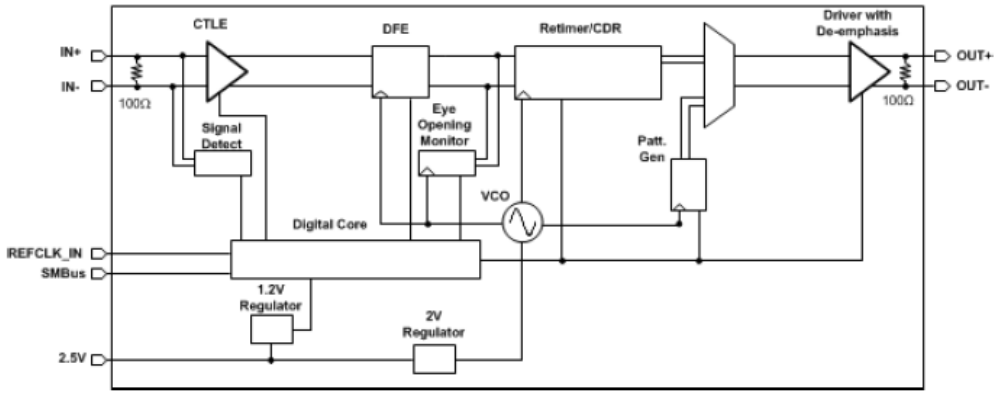
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 7	Disclosure
	 TI DS125DF410, 1.

Claim 7	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 7	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 7	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 7	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 7	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 7	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 7	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 7	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 7	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

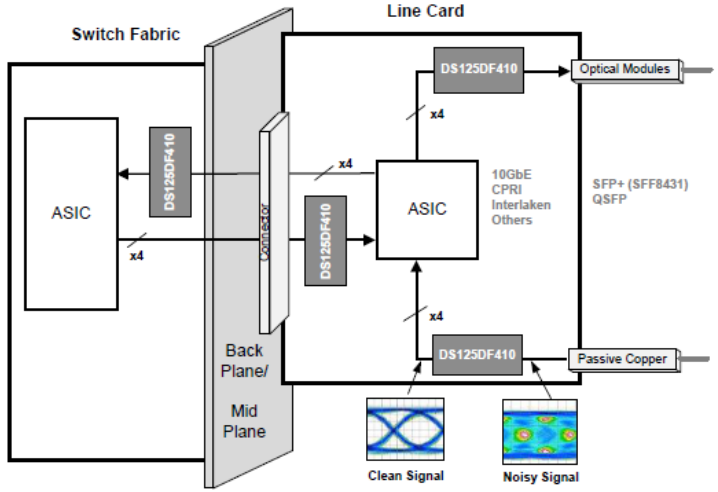
TI DS125DF410, 41.

Claim 7	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 7	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 7	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 7	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

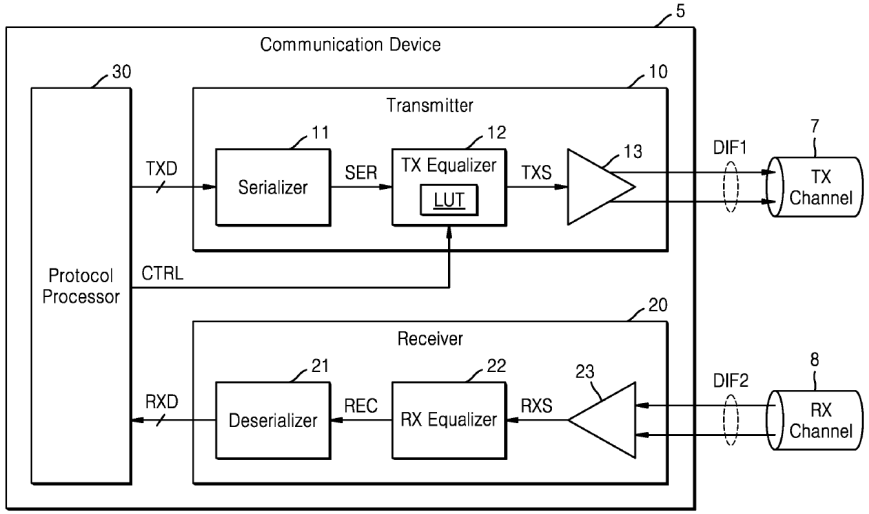
Exhibit C-12

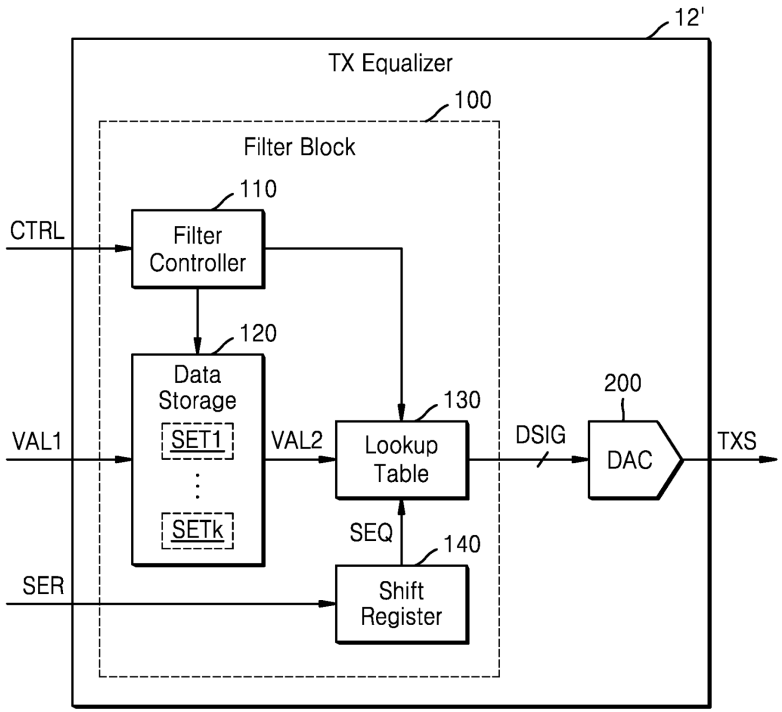
Claim 7	Disclosure

H. INDEPENDENT CLAIM 8

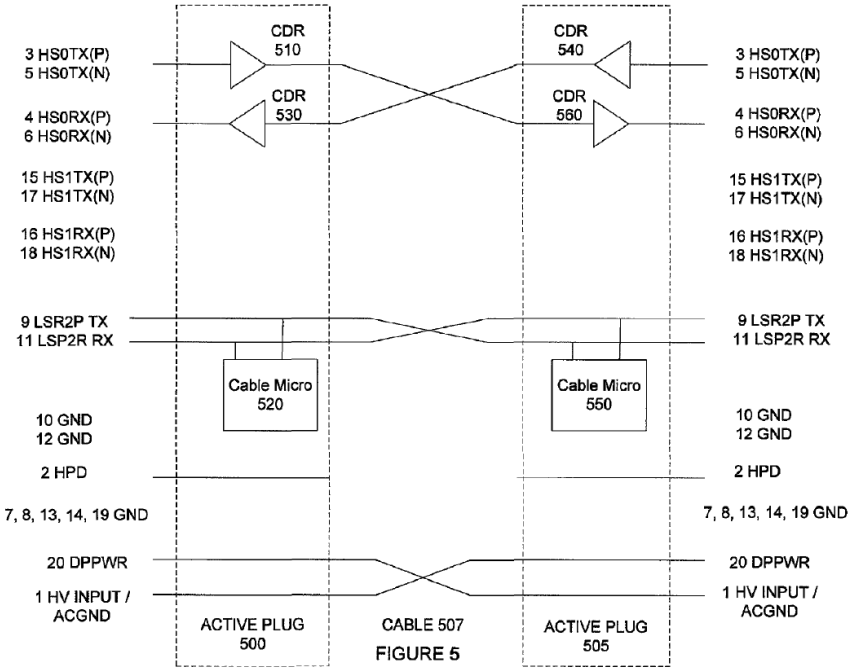
Claim 8	Disclosure
8[pre] A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "The disclosure relates to an equalizer, and more particularly, to an equalizer including a lookup table and a transmitter including the equalizer. In serial communication, an interconnection between a transmitter and a receiver, i.e., a channel, may distort signals. In order to compensate for distortion of signals generated in the channel, the transmitter and/or the receiver may include an equalizer. For example, the equalizer included in the transmitter may include a Finite Impulse Response (FIR) filter that provides an inverse transfer function of the transfer function of the channel. An equalizer including a high complexity filter may be necessary in order to precisely compensate for signal distortion while performing fast signal filtering for high speed serial communication. Further, in order to reduce power consumption and heat generation, an equalizer capable of reducing power consumption may be necessary." Kang, 1:13-30 "FIG. 1 is a block diagram illustrating a communication device **5** according to an exemplary embodiment of the disclosure. As shown in FIG. 1, the communication device **5** is capable of serial communication

Claim 8	Disclosure
	with a counterpart communication device via a TX channel **7** and an RX channel **8**. Although FIG. 1 illustrates that the communication device **5** communicates with the counterpart communication device through a full duplex communication scheme, i.e., two channels (the TX and RX channels **7** and **8**), according to some embodiments, the communication device **5** may communicate with the counterpart communication device through a half duplex communication scheme, i.e., one channel. The TX channel **7** or the RX channel **8** may refer to interconnection between the communication device **5** and the counterpart communication device, and serial data signals DIF**1** and DIF**2** may transfer through the TX channel **7** and the RX channel **8**, respectively. For example, the TX channel **7** or the RX channel **8** may include at least one of a conductive line of an integrated circuit, a pattern of a printed circuit board (PCB), a connector, and a cable. The serial data signals DIF**1** and DIF**2**, which respectively pass through the TX channel **7** and the RX channel **8**, may be differential signals as shown in FIG. 1 in some embodiments, or may be single signals unlike what is illustrated in FIG. 1. The communication device **5** may refer to any device in serial communication with the counterpart communication device via the TX channel **7** and the RX channel **8**. In some embodiments, the communication device **5** may be a die included in a semiconductor package and may be in serial communication with a counterpart communication device included in the same semiconductor package. In some embodiments, the communication device **5** may be a semiconductor package mounted on a PCB and may be in serial communication with the counterpart communication device mounted on the same PCB or mounted on another PCB. In some embodiments, the communication device **5** may be a system (e.g., a storage, a computing system, etc.) including at least one semiconductor package and a PCB and may be in serial communication with other systems. As shown in FIG. 1, the communication device **5** may include a transmitter **10**, a receiver **20**, and a protocol processor **30**. In some embodiments, the transmitter **10** and the receiver **20** may be implemented as one block as a transceiver. The transmitter **10**, the receiver **20**, and the protocol processor **30** may provide a physical layer of communication and may be collectively referred to as a SerDes (serializer/deserializer) for serial communication." Kang, 3:17-65.

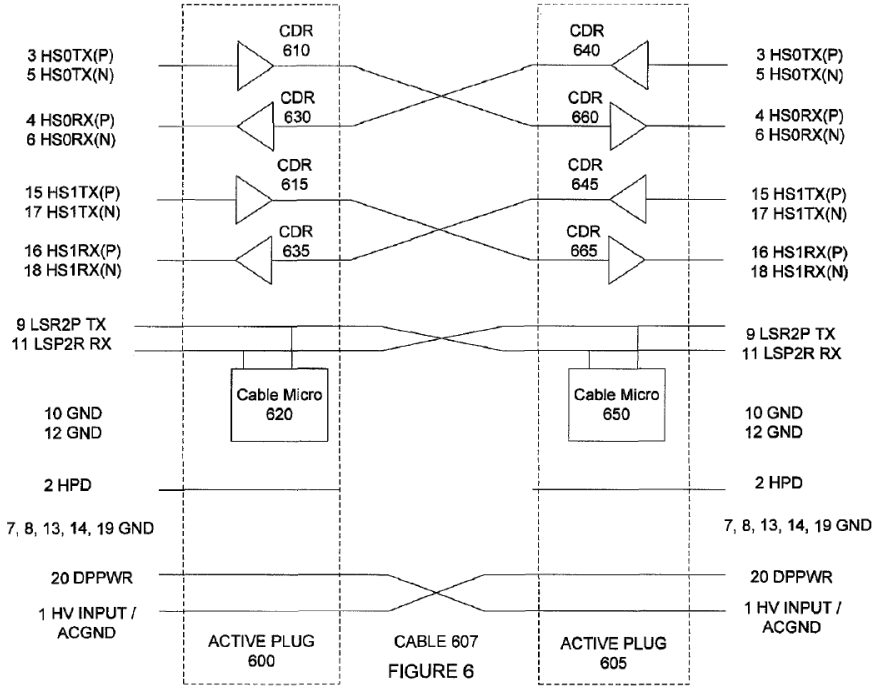
Claim 8	Disclosure
	FIG. 1  Kang, FIG. 1

Claim 8	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 8	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

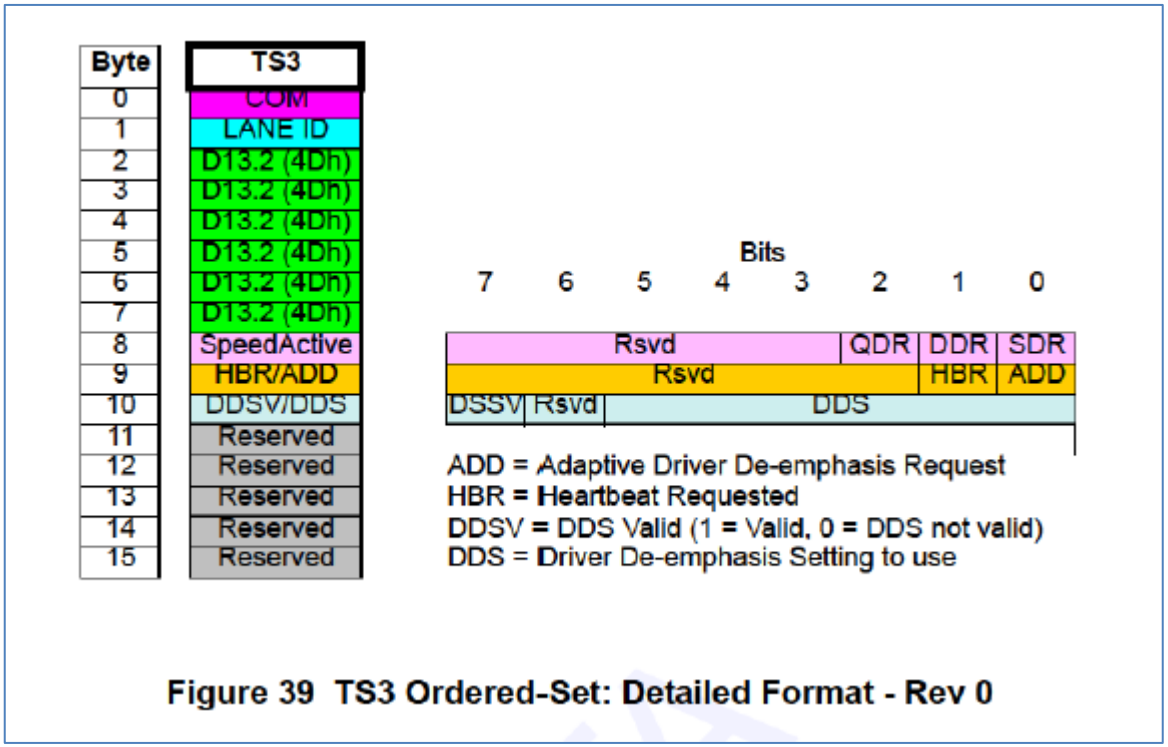
Claim 8	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 8	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 8	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 8	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 8	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 8	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

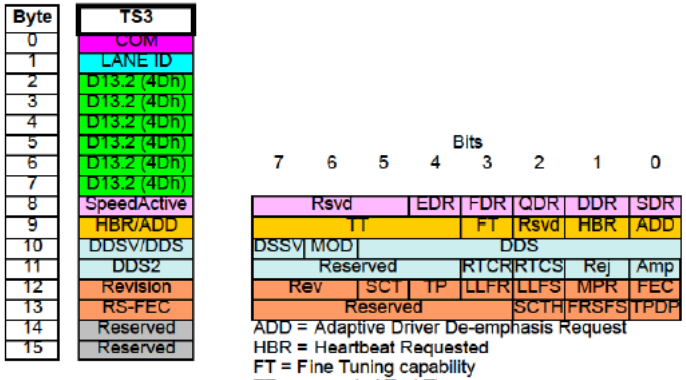
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 8	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits	7	6	5	4	3	2	1	0
	Rsvd			EDR	FDR	QDR	DDR	SDR
	TT				FT	Rsvd	HBR	ADD
	DSSV	MOD	DDS					
	Reserved				RTCR	RTCS	Rej	Amp
	Rev		SCT	TP	LLFR	LLFS	MPR	FEC
	Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 8	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 8	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 8	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 8	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 8	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 8	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 8	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

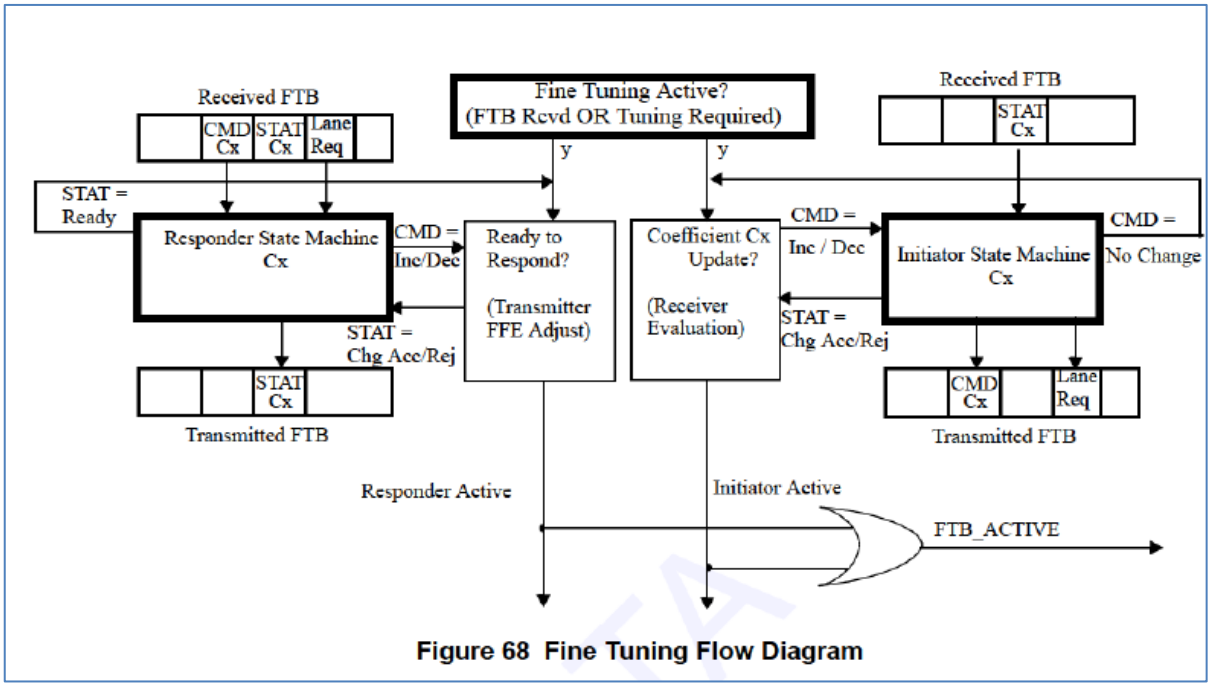
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 8	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 8	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 8	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required

Addr	Size	Type	Functions
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required

Addr	Size	Type	Functions
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional

Addr	Size	Type	Functions
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional

Addr	Size	Type	Functions
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies

Addr	Size	Type	Functions
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 8	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 8	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 8	Disclosure

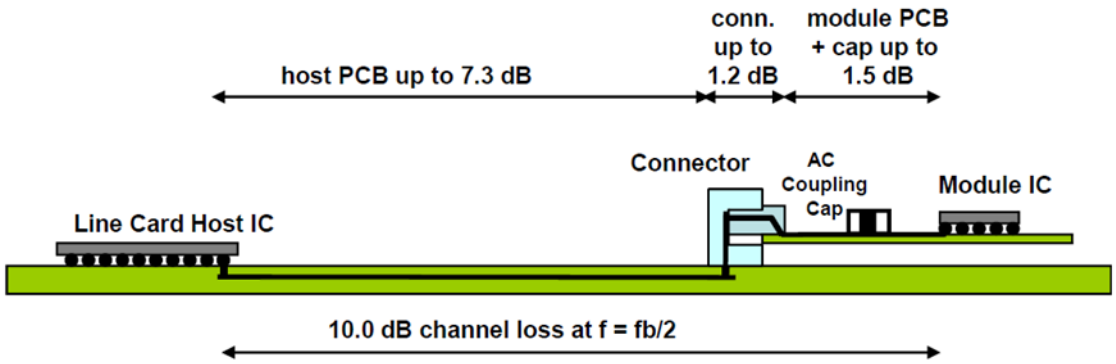
Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"To provide a high-performance radio link for high-speed systems employing spectrally-efficient modulation schemes, a reliable and robust transmitter radio link is required. Present embodiments of the current invention perform signal processing techniques to enhance the system performance and robustness of the transmitter portion of the transceiver."
Rafie, paragraph 47.

"Various embodiments are directed toward a communication device that includes a transceiver circuit that is configured to communicate by generating an RF carrier signal of around 13.56 MHz as consistent with various RFID technologies, such as ISO/IEC standard 14443."
Ciacci, 3:63-67.

Claim 8	Disclosure
	United States Patent No. 7,239,665 ("Mezer") Mezer describes supporting Ethernet, and such standards-compliant implementation was conventional. *See, e.g.*, at Mezer, 4:55-57, 6:62-7:3. This obvious implementation would have met the Ethernet standard's description of a chip-to-module communication link comprising a port connector coupling a port transceiver to a pluggable module transceiver. *See, e.g.*, IEEE 802.3bs-2017, 323-330 (Annex 120C), 350-372 (Annex 120E), 350 ("The chip-to-module interface is defined using a specification… that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0"); *see also* OIF-CEI-04.0, 334, Fig. 16-15 (below, showing a "Connector" receiving a pluggable module). **Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model** 

PCIe 3.1a

1.3. PCI Express Fabric Topology

A fabric is composed of point-to-point Links that interconnect a set of components – an example fabric topology is shown in Figure 1-2. This figure illustrates a single fabric instance referred to as a hierarchy – composed of a Root Complex (RC), multiple Endpoints (I/O devices), a Switch, and a PCI Express to PCI/PCI-X Bridge, all interconnected via PCI Express Links.

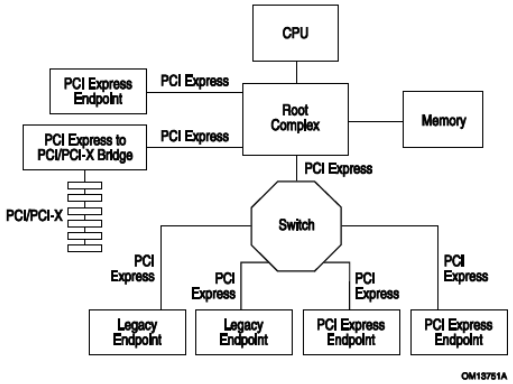


Figure 1-2: Example Topology

1.3.1. Root Complex

- A Root Complex (RC) denotes the root of an I/O hierarchy that connects the CPU/memory subsystem to the I/O.
- As illustrated in Figure 1-2, a Root Complex may support one or more PCI Express Ports. Each interface defines a separate hierarchy domain. Each hierarchy domain may be composed of a single Endpoint or a sub-hierarchy containing one or more Switch components and Endpoints.
- The capability to route peer-to-peer transactions between hierarchy domains through a Root Complex is optional and implementation dependent. For example, an implementation may incorporate a real or virtual Switch internally within the Root Complex to enable full peer-to-peer support in a software transparent way.

  Unlike the rules for a Switch, a Root Complex is generally permitted to split a packet into smaller packets when routing transactions peer-to-peer between hierarchy domains (except as noted below), e.g., split a single packet with a 256-byte payload into two packets of 128 bytes payload each. The resulting packets are subject to the normal packet formation rules contained in this specification (e.g., Max_Payload_Size, Read Completion Boundary, etc.). Component designers should note that splitting a packet into smaller packets may have negative performance

Claim 8	Disclosure
	consequences, especially for a transaction addressing a device behind a PCI Express to PCI/PCI-X bridge. Exception: A Root Complex that supports peer-to-peer routing of Vendor_Defined Messages is not permitted to split a Vendor_Defined Message packet into smaller packets except at 128-byte boundaries (i.e., all resulting packets except the last must be an integral multiple of 128 bytes in length) in order to retain the ability to forward the Message across a PCI Express to PCI/PCI-X Bridge. Refer to the *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0* for additional information. ❑ A Root Complex must support generation of configuration requests as a Requester. ❑ A Root Complex is permitted to support the generation of I/O Requests as a Requester. o A Root Complex is permitted to generate I/O Requests to either or both of locations 80h and 84h to a selected Root Port, without regard to that Root Port's PCI Bridge I/O decode configuration; it is recommended that this mechanism only be enabled when specifically needed. ❑ A Root Complex must not support Lock semantics as a Completer. ❑ A Root Complex is permitted to support generation of Locked Requests as a Requester. PCIe 3.1 at 50-51.

Claim 8	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 8	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 8	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

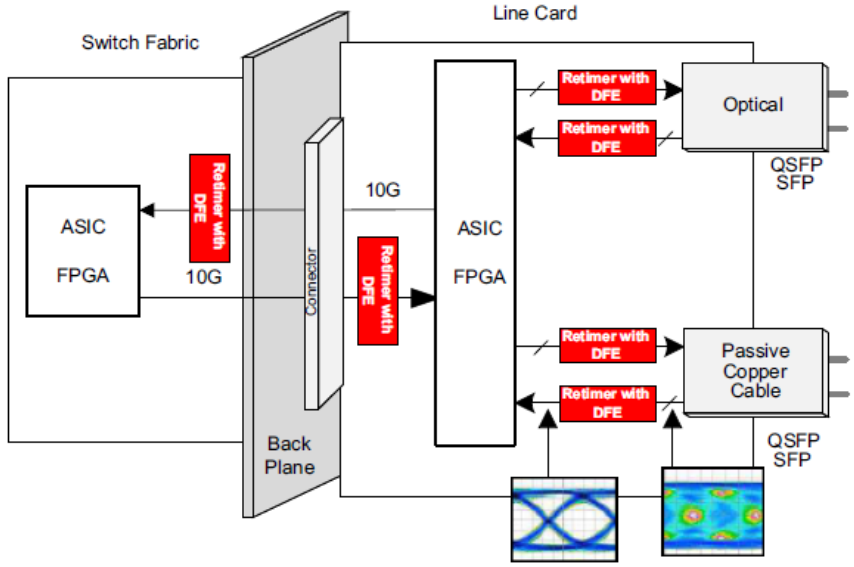
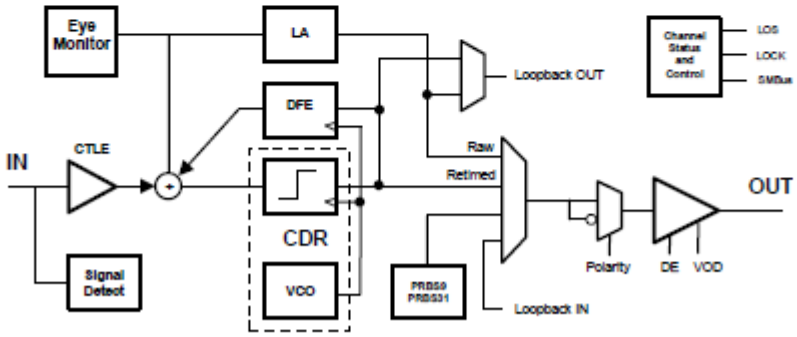


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 8	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 8	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 8	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

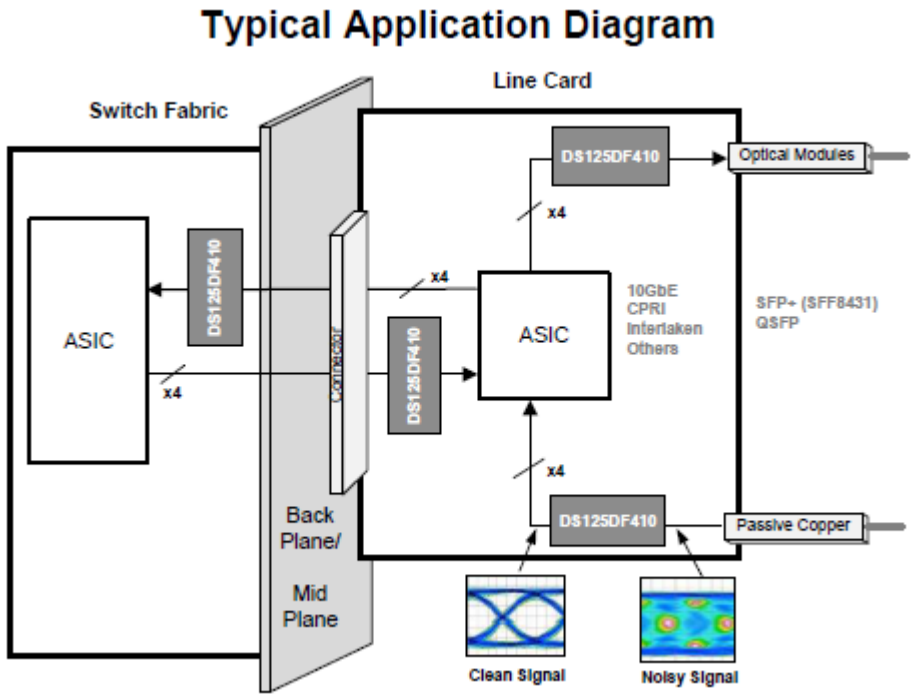
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

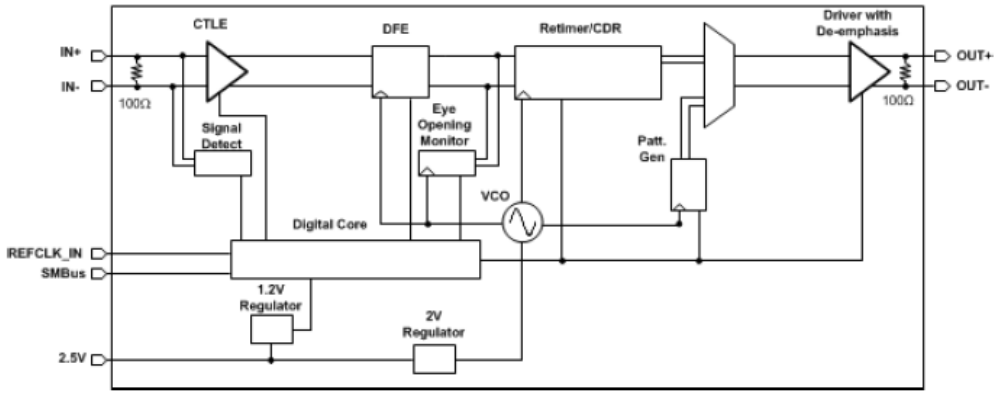
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 8	Disclosure
	 TI DS125DF410, 1.

Claim 8	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 8	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 8	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 8	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 8	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 8	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

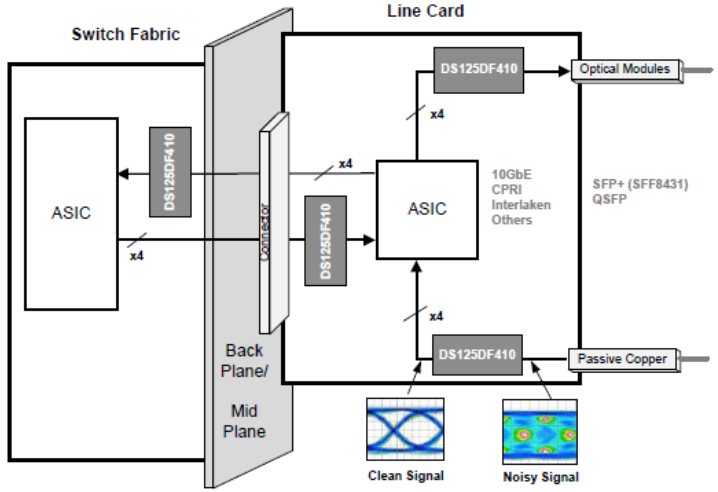
TI DS125DF410, 41.

Claim 8	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 8	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 8	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

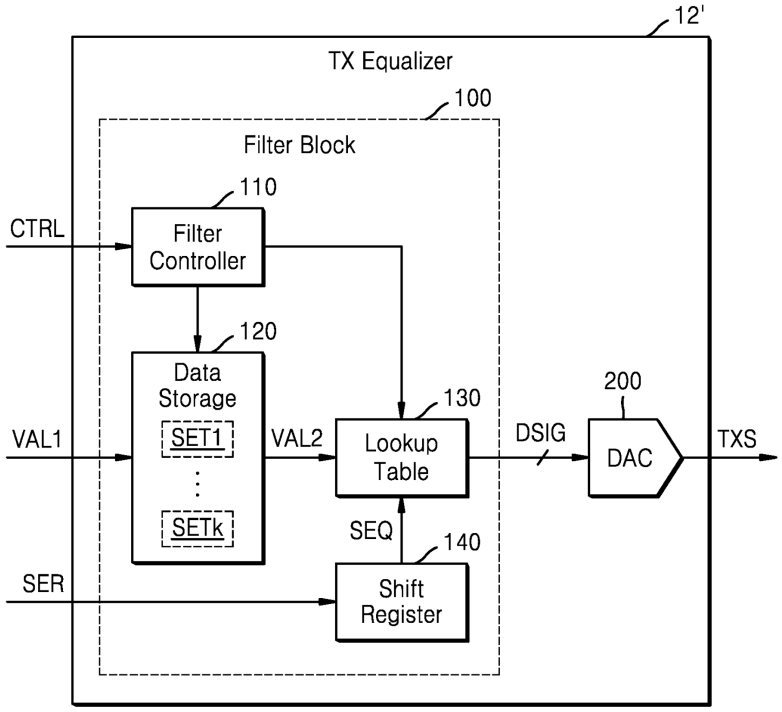
Claim 8	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Claim 8	Disclosure
8[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**." Kang, 5:20-42.

Claim 8	Disclosure
	"FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS, which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3.

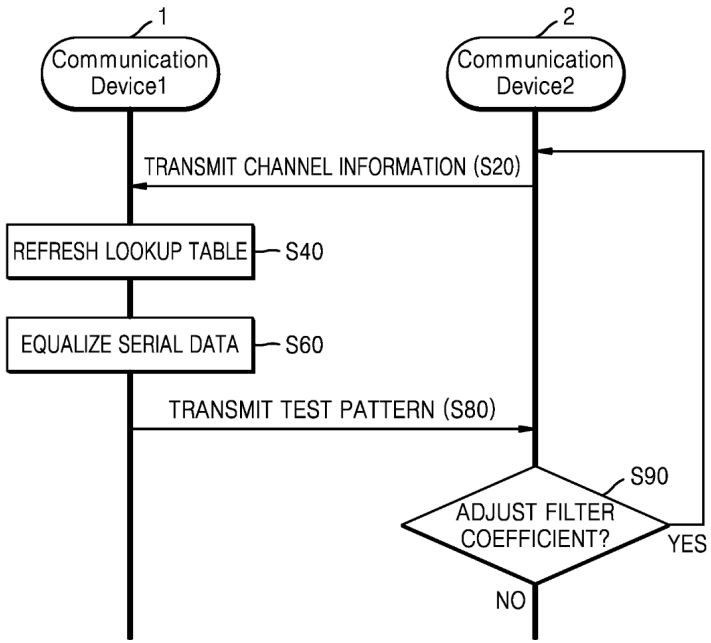
Claim 8	Disclosure
	The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively.

Claim 8	Disclosure
	The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

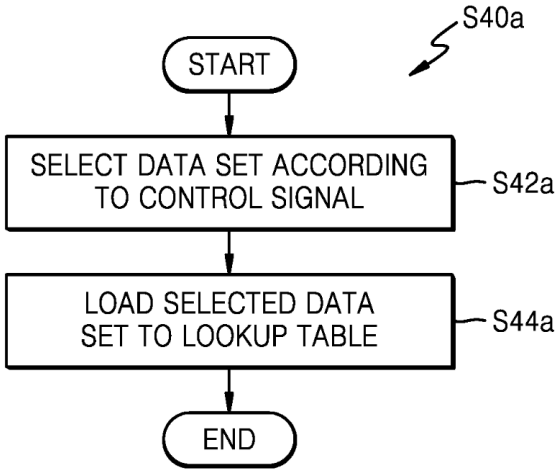
Claim 8	Disclosure
	FIG. 3  Kang, FIG. 3 "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the

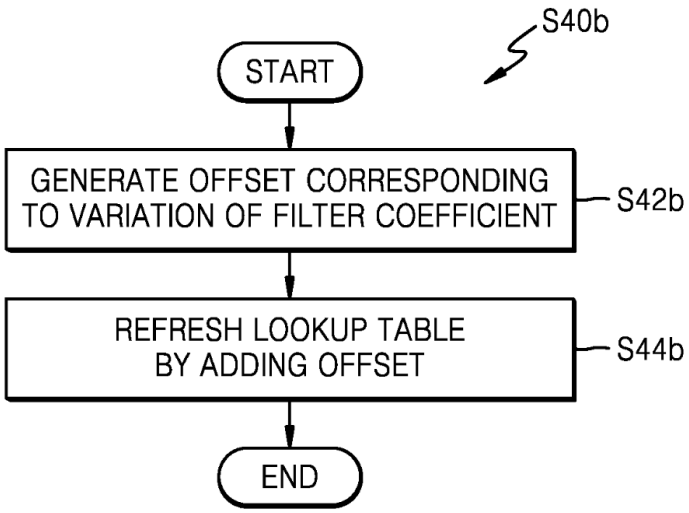
Claim 8	Disclosure
	equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "FIG. 10 is a diagram illustrating an equalization method over time according to an exemplary embodiment of the disclosure. For example, the equalization method of FIG. 10 may be performed by the first communication device 1 including the TX equalizer 12 of FIG. 1 and the second communication device 2 communicating with the first communication device 1. The filter coefficients for equalization may be determined according to the equalization method illustrated in FIG. 10, and the method for determining the filter coefficients may be referred to as training of filter coefficients. It is assumed below that the first communication device 1 of FIG. 10 includes the components of the communication device 5 of FIG. 1, and FIG. 10 will be described with reference to FIG. 1. Referring to FIG. 10, in operation S20, the second communication device 2 may transmit channel information. For example, the second communication device 2 may first transmit, to the first communication device 1, channel information including information indicating one of the plurality of data sets, as described above with reference to FIG. 3. In operation S40, the first communication device 1 may refresh the lookup table LUT. For example, the protocol processor 30 of the first communication device 1 may extract information indicating a data set from the channel information received in operation S20 and may transmit the control signal CTRL including the extracted information to the TX equalizer 12. TX equalizer 12 may refresh the lookup table LUT based on the control signal CTRL. The lookup table LUT may include values of the digital signal DSIG corresponding to possible values of the symbol sequence extracted from the serial data SER. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information indicating a data set will be described with reference to FIG. 11. In operation S60, the first communication device 1 may equalize the serial data SER. For example, in the TX equalizer 12 of the first communication device 1, the lookup table LUT may output a digital signal (e.g., DSIG in FIG. 3) corresponding to the symbol sequence of the serial data SER, and the DAC 200 included in the TX equalizer 12 may convert the digital signal into an analog signal. Accordingly, an adder and a multiplier for multiplication and addition between the symbol sequence and the filter coefficient

Claim 8	Disclosure
	sequence for implementing the FIR filter 9 of FIG. 2 may be omitted. The example of operation S60 will be described with reference to FIG. 14. In operation S80, the first communication device 1 may transmit a test pattern. For example, the test pattern may include a pattern previously shared by the first communication device 1 and the second communication device 2, and the second communication device 2 may receive the test pattern through a channel (e.g., 7 of FIG. 1). In operation S90, the second communication device 2 may determine whether to adjust the filter coefficient. For example, the second communication device 2 may evaluate the test pattern received from the first communication device 1 and determine whether to adjust at least one of the coefficients of the FIR filter used for equalization of the first communication device 1 according to the evaluation result. As illustrated in FIG. 10, when it is determined not to adjust at least one of the filter coefficients, the training of the filter coefficients may be terminated and the first communication device 1 may transmit the signal, which is equalized according to the current filter coefficients, to the second communication device 2. On the other hand, when it is determined to adjust at least one of the filter coefficients, operation S20 may be performed. Unlike the initially performed operation S20, in operation S20, which is performed after operation S90, the second communication device 2 may transmit channel information, which includes information on the variation of the filter coefficients, to the first communication device 1. Thereafter, unlike the initially performed operation S40, in operation S40, the first communication device 1 may refresh the lookup table LUT based on the information on the variation of the filter coefficients. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information on the variation of the filter coefficients will be described with reference to FIG. 12." Kang, 11:62-13:6

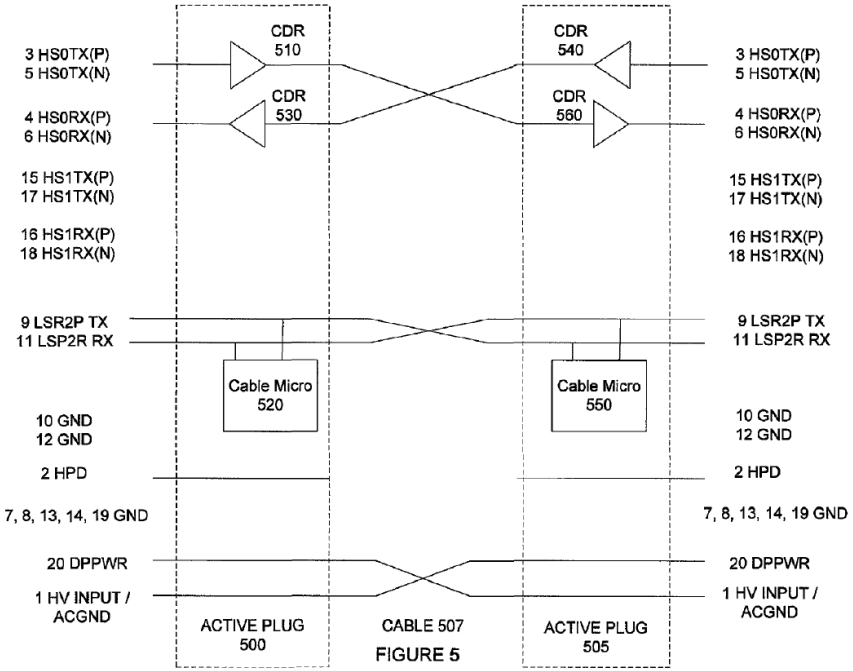
Claim 8	Disclosure
	FIG. 10  Kang, FIG. 10 "Referring to FIG. 11, operation S**40** *a* may include operations S**42** *a* and S**44** *a*. In operation S**42** *a*, an operation of selecting a data set according to the control signal CTRL may be performed. For example, the controller **110** of FIG. 3 may receive a control signal CTRL including information indicating one of k filter coefficient sequences and may control the data storage **120** to output one of first to k-th data sets SET**1** to SETk, which are stored in the data storage **120**, according to the control signal CTRL. In operation S**44** *a*, an operation of loading the selected data set into the lookup table **130** may be performed. For example, the controller **110** may control the data storage **120** and the lookup table **130** to store the second value VAL**2** outputted from the data storage **120** in the lookup table **130**.

Claim 8	Disclosure
	Referring to FIG. 12, operation S**40** *b* may include operations S**42** *b* and S**44** *b*. In operation S**42** *b*, an operation of generating an offset OFF corresponding to the variation of the filter coefficients may be performed. For example, the offset generator **150** of FIG. 6 may generate an offset OFF, based on the variation signal VAR and the index IDX provided from the controller **110′**. The variation signal VAR may indicate at least one of up, down, hold, and reset of the filter coefficient and may include a variation amount of the filter coefficient. An example of generating the offset OFF when the variation signal VAR indicates the reset of the filter coefficient will be described later with reference to FIG. 13. In operation S**44** *b*, an operation of refreshing the lookup table **130′** may be performed by adding the offset OFF. In some embodiments, the offset generator **150** may generate a positive offset OFF or a negative offset OFF, and thus the calculator **160** may perform an addition. In some embodiments, the offset generator **150** may generate the positive offset OFF, and thus the calculator **160** may perform addition or subtraction according to the control of the controller **110′**. The lookup table **130′** may be refreshed by storing the output value of the calculator **160**, that is, the third value VAL**3**, in the lookup table **130′**." Kang, 13:18-54

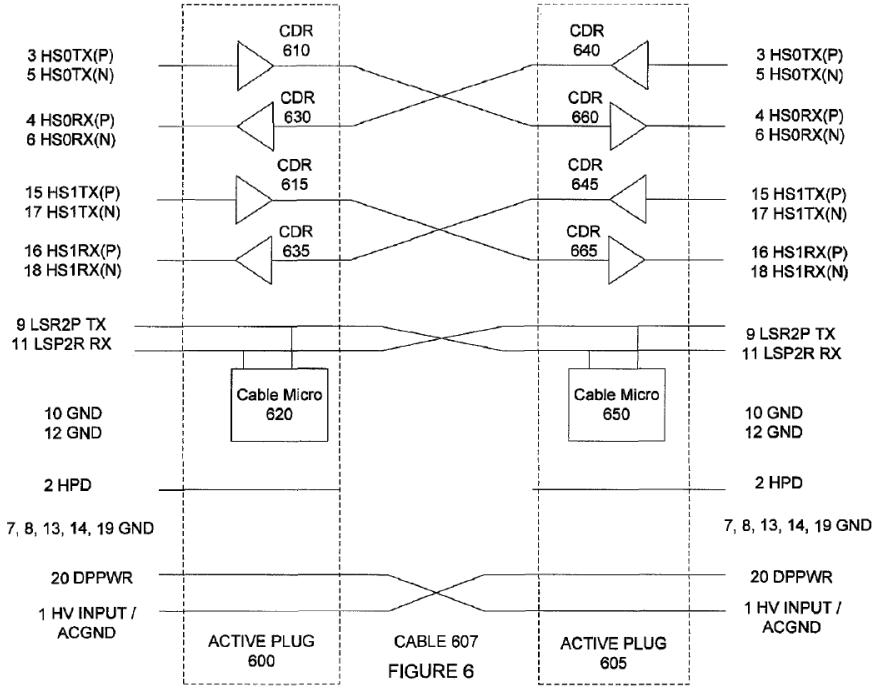
Claim 8	Disclosure
	FIG. 11  Kang, FIG. 11

Claim 8	Disclosure
	FIG. 12  Kang, FIG. 12 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**. Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**.

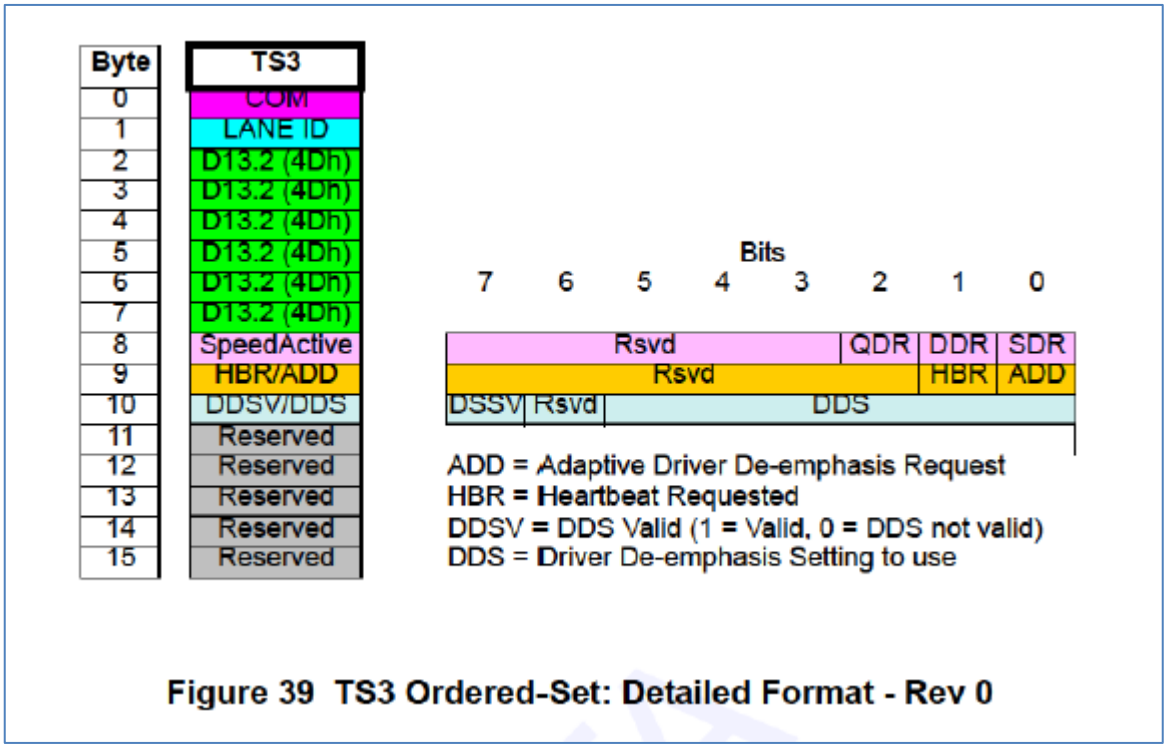
Claim 8	Disclosure
	The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables. In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used.

Claim 8	Disclosure
	In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5 "FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock

Claim 8	Disclosure
	and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 8	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 8	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 8	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 8	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

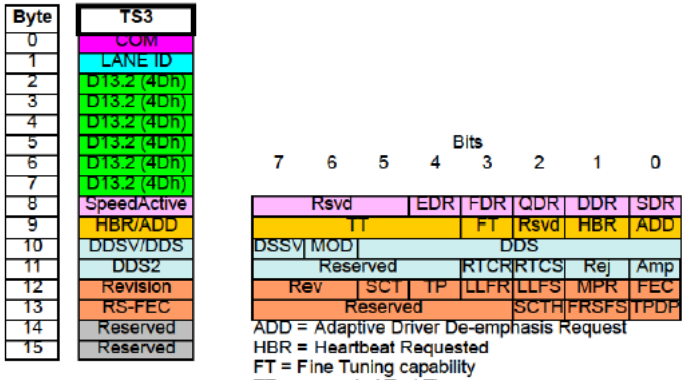
Bits	7	6	5	4	3	2	1	0
	Rsvd			EDR	FDR	QDR	DDR	SDR
	TT				FT	Rsvd	HBR	ADD
	DSSV	MOD	DDS					
	Reserved						Rej	Amp
	Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 8	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 8	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 8	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 8	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 8	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 8	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 8	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 8	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

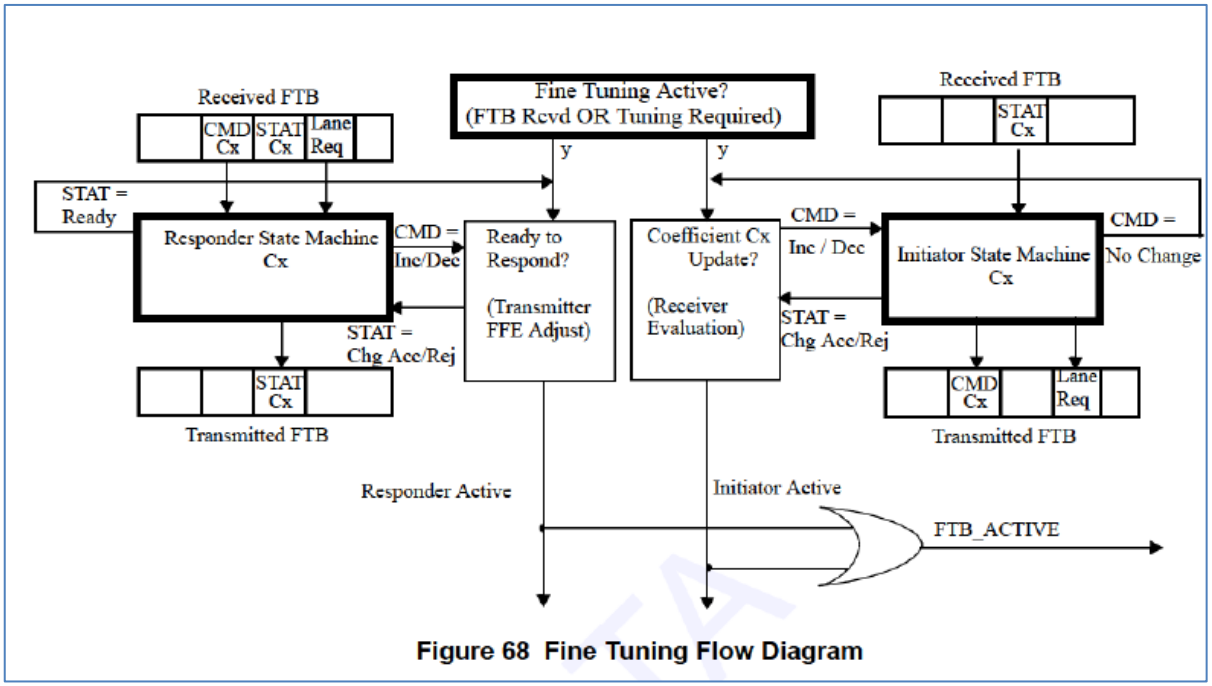
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 8	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 8	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 8	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required

Addr	Size	Type	Functions
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required

Addr	Size	Type	Functions
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional

Addr	Size	Type	Functions
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional

Addr	Size	Type	Functions
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies

Addr	Size	Type	Functions
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 8	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 8	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 8	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

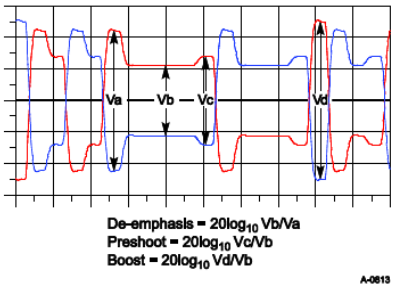
InfiniBand, Table 143 (p. 535)

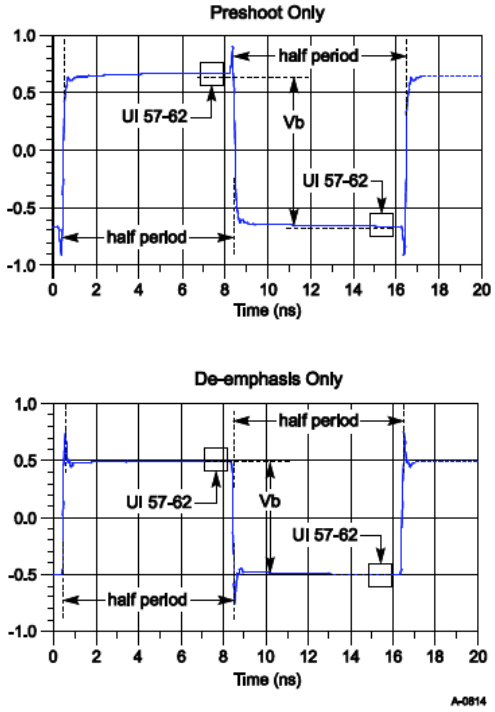
"The overall pre-equalizer **800** can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."

Rafie, paragraph 82.

"Digital pre-equalizer (PEQ) circuit **204** can be configured to introduce a distortion to the input signal to compensate for channel impairment. At power-on little or no information may be known about the channel. Accordingly, the digital PEQ circuit **204** can be initially configured with no distortion. In some

Claim 8	Disclosure
	embodiments, the digital PEQ circuit **204** can be initially configured with a distortion that is based upon a corresponding set of coefficients." Ciacci, 5:40-47. "The coefficients can then be used in combination with a pre-equalizer filter function of higher than first order" Ciacci, 8:2-4. *PCIe 3.1a* **4.3.3.5.2. Tx Equalization Presets** An 8.0 GT/s transmitter must support a specified number of presets, where the preset values are defined in terms of voltage ratios as illustrated in Figure 4-42. Presets are defined in terms of two ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Ve) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GTs/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. Figure 4-42 is shown as an example of TxEQ and is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of 8.0 GT/s signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms, as shown later in this section. The presets defined in Table 4-16 and Table 4-17 are numbered to match the designations in Section 4.2.3.1. Note, however, that in Section 4.2.3.1 the coefficients are defined as integers (using upper case "C"), while in the electrical section they are defined as floating point (using lower case "c"). PCIe 3.1a at 355.

Claim 8	Disclosure
	 **Figure 4-42: Definition of Tx Voltage Levels and Equalization Ratios** Figure 4-43 illustrates the waveforms that will be observed when measuring presets when using the 64-ones/64-zeroes sequence that is part of the compliance pattern. Depending on whether the preset implements de-emphasis, preshoot, or both the corresponding waveshape will differ. The two cases illustrated below show preshoot and de-emphasis, as can be observed by noting whether the boost occurs before or after each edge transition. For the case where both de-emphasis and preshoot are present, boost occurs both before and after each edge transition. Note that in all cases, however, the voltage of interest occurs during the flat portion (Vb) of the waveform, where it can be accurately measured independent of high frequency effects. PCIe 3.1a at 356.

Claim 8	Disclosure
	 Figure 4-43: Waveform Measurement Points for Pre-shoot and De-emphasis PCIe 3.1a at 357.

Claim 8	Disclosure

Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

Notes:

1. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The allowable P10 boost range is defined by the coefficient space lying between the Min and Max Reduced Swing Limits as shown by the two diagonal lines in the example of Figure 4-45. This approach permits both full and reduced swing transmitters to use P10 for testing to their respective boost limits.

With the exception of P4 (for which both pre-shoot and de-emphasis are 0.0 dB) it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are 1 UI wide and therefore subject to attenuation by the package and the breakout channel. Instead the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval. Table 4-17 lists the preset values required to measure each of the Va and Vc values from which the preshoot or de-emphasis values may be derived.

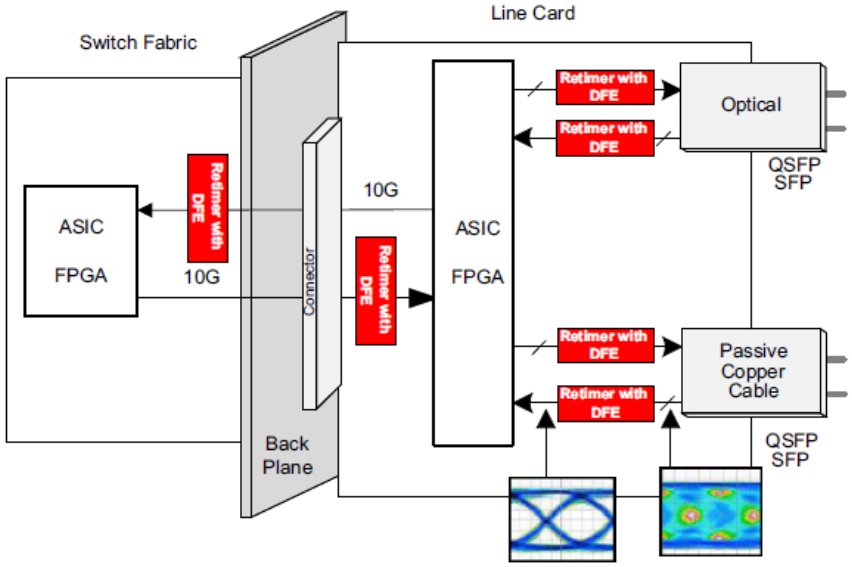
PCIe 3.1a at 358.

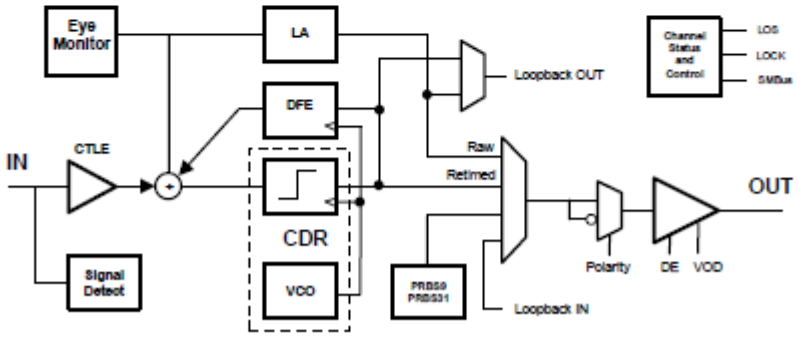
Claim 8	Disclosure
	Table 4-17: Preset Measurement Cross Reference Table PCIe 3.1a at 359.

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P4	N/A	N/A
P1	P1/P4	N/A
P0	P0/P4	N/A
P9	N/A	P4/P9
P8	P8/P6	P3/P8
P7	P7/P5	P2/P7
P5	N/A	P4/P5
P6	N/A	P4/P6
P3	P3/P4	N/A
P2	P2/P4	N/A
P10	P10/P4	N/A

Claim 8	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 8	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 8	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 8	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 8	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 8	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

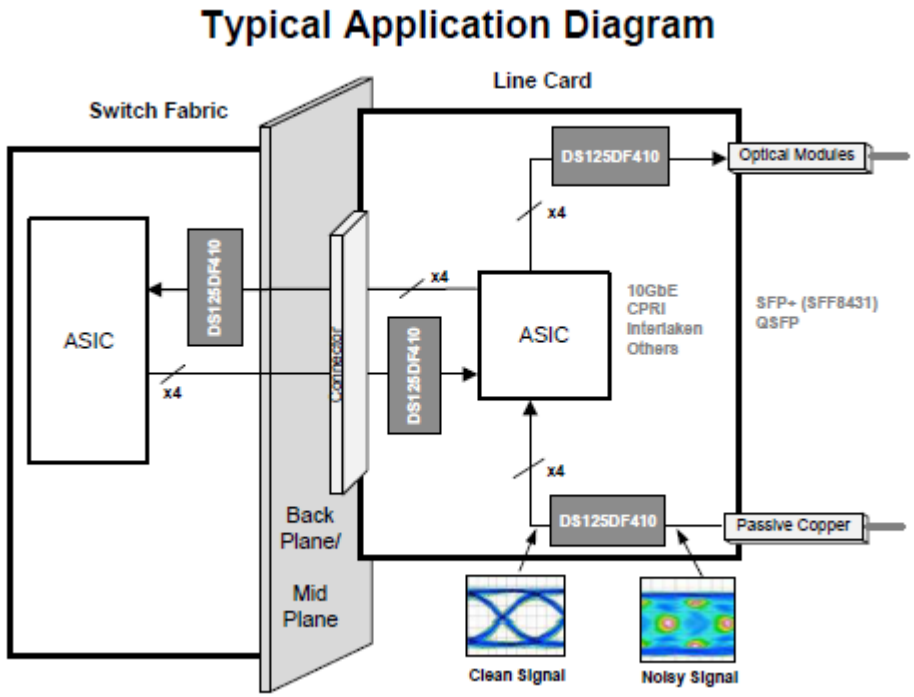
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

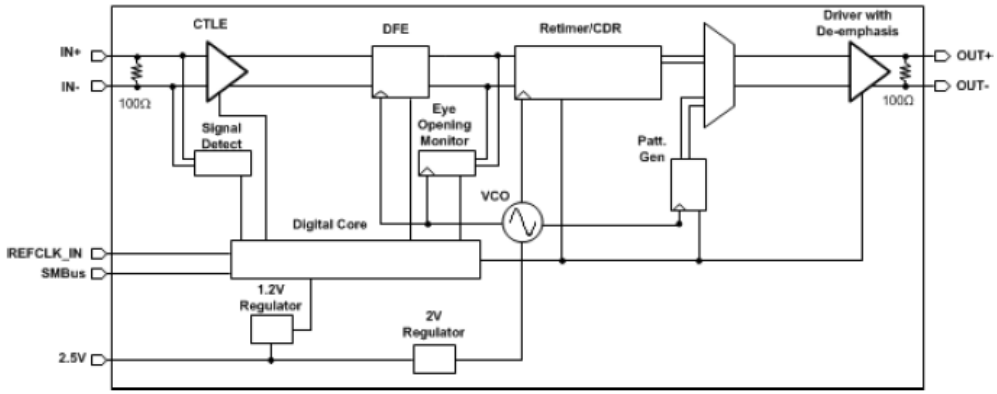
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 8	Disclosure
	 TI DS125DF410, 1.

Claim 8	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 8	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 8	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 8	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 8	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 8	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

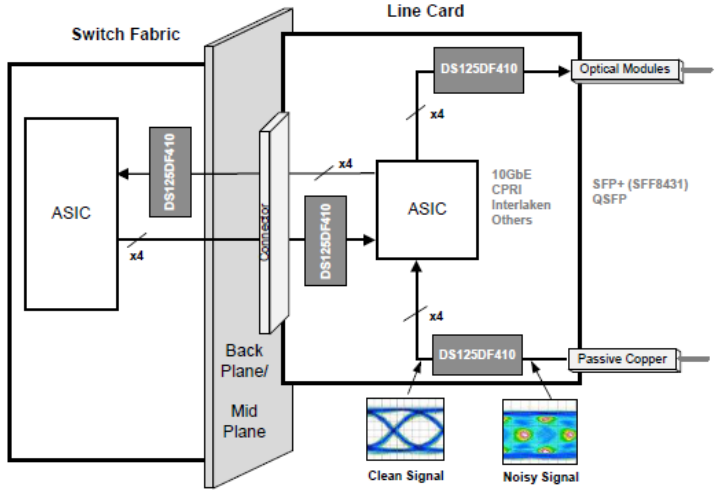
TI DS125DF410, 41.

Claim 8	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 8	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 8	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

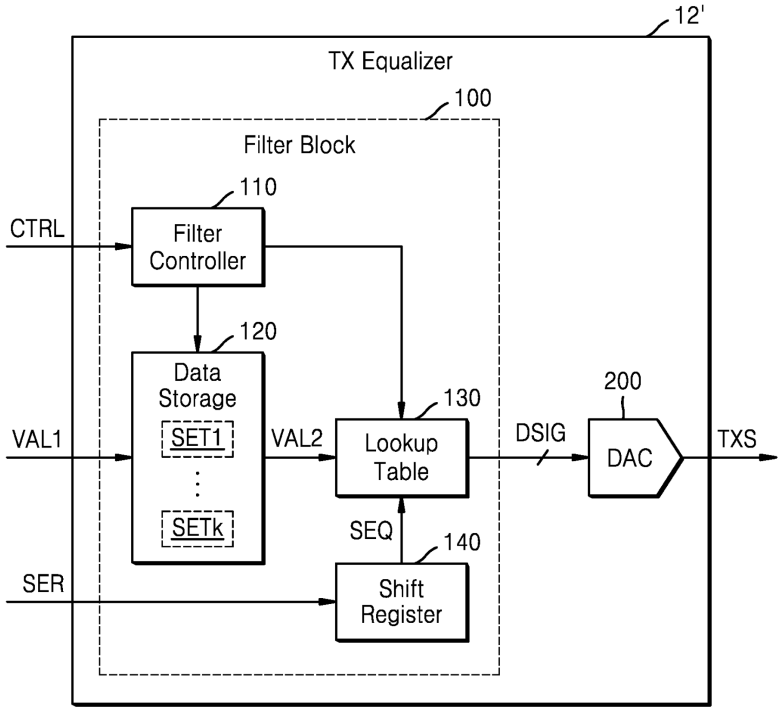
Claim 8	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Claim 8	Disclosure
8[b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model,	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**." Kang, 5:20-42.

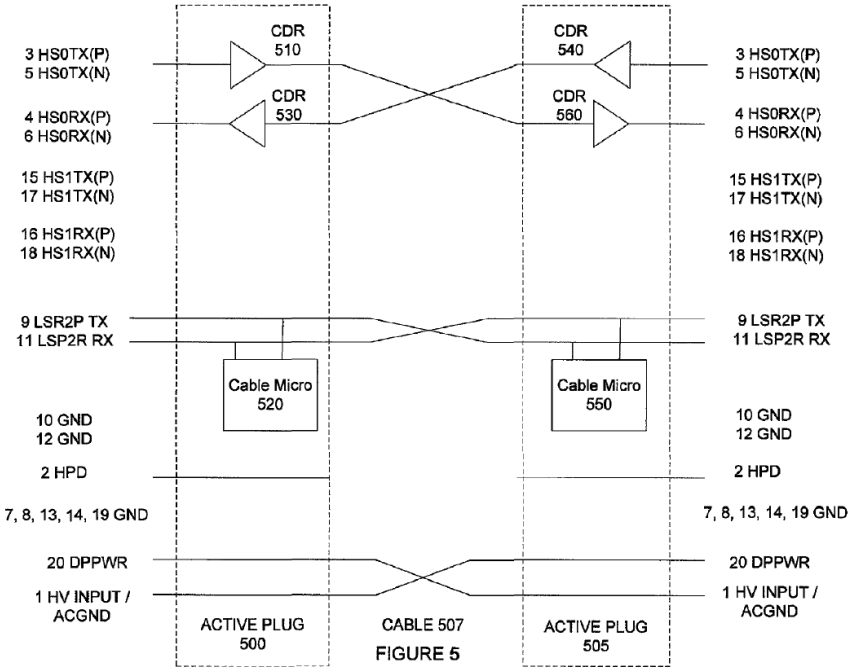
Claim 8	Disclosure
	"FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS, which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3.

Claim 8	Disclosure
	The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively.

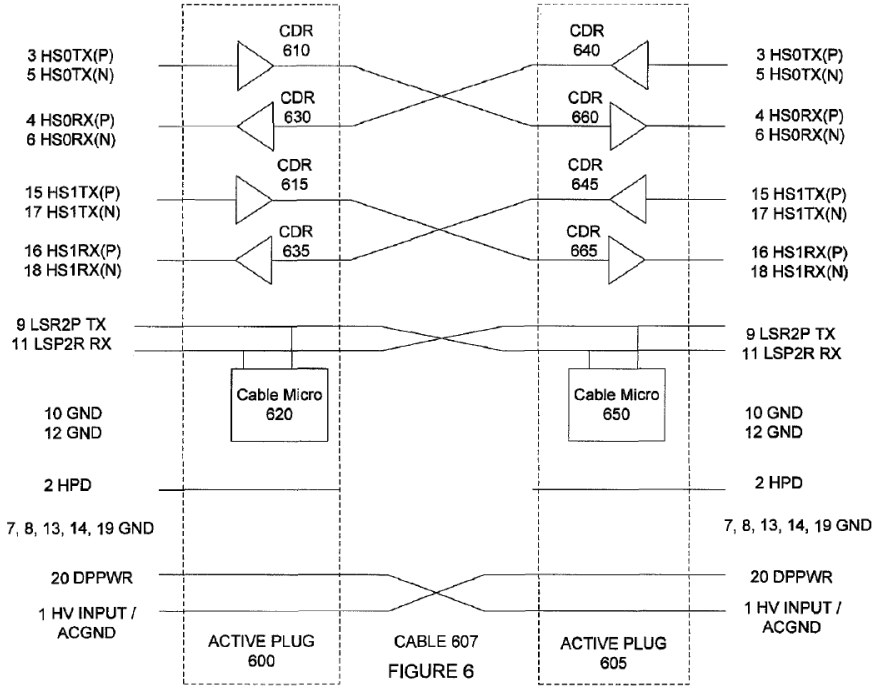
Claim 8	Disclosure
	The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 8	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

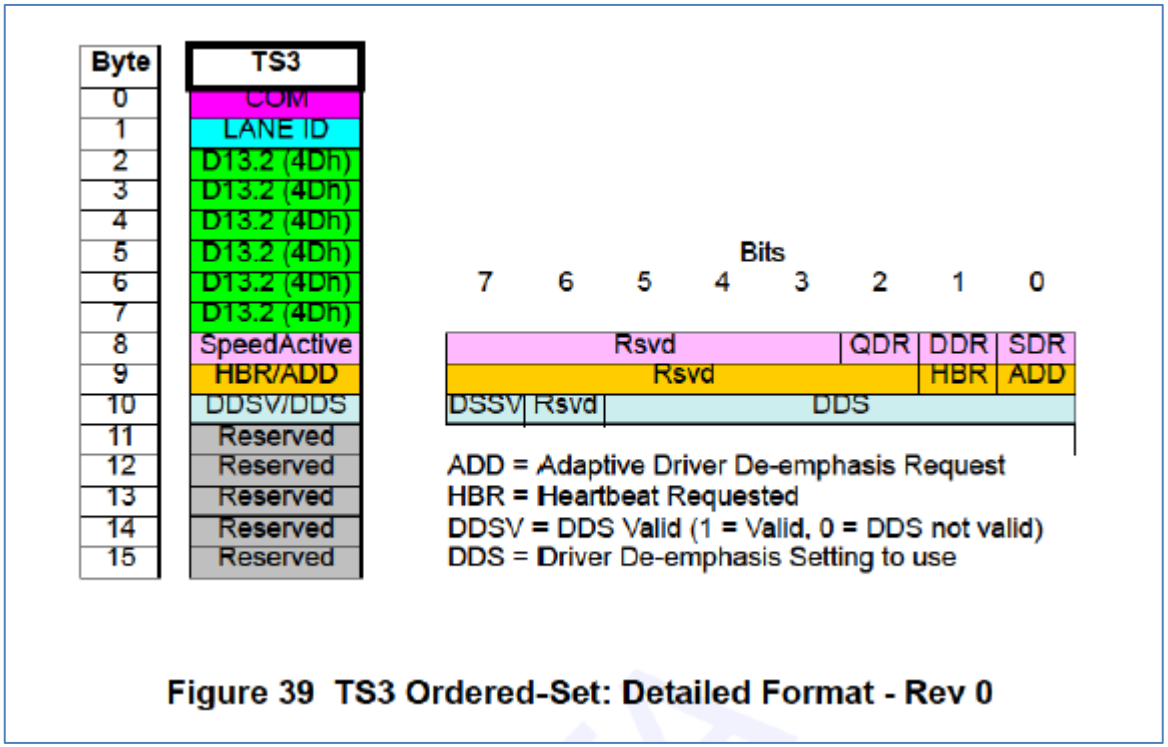
Claim 8	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 8	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 8	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 8	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 8	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 8	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 8	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

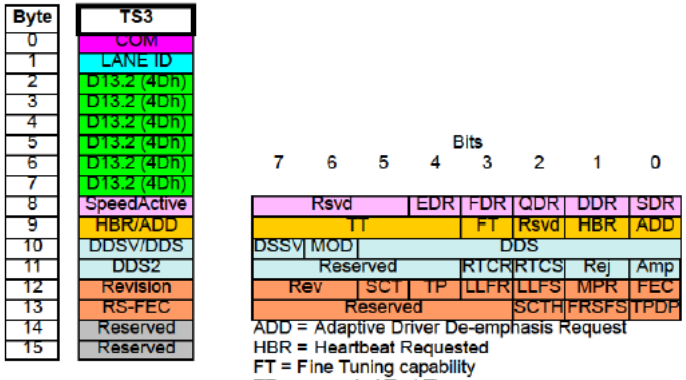
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 8	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 8	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 8	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 8	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 8	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 8	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 8	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 8	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

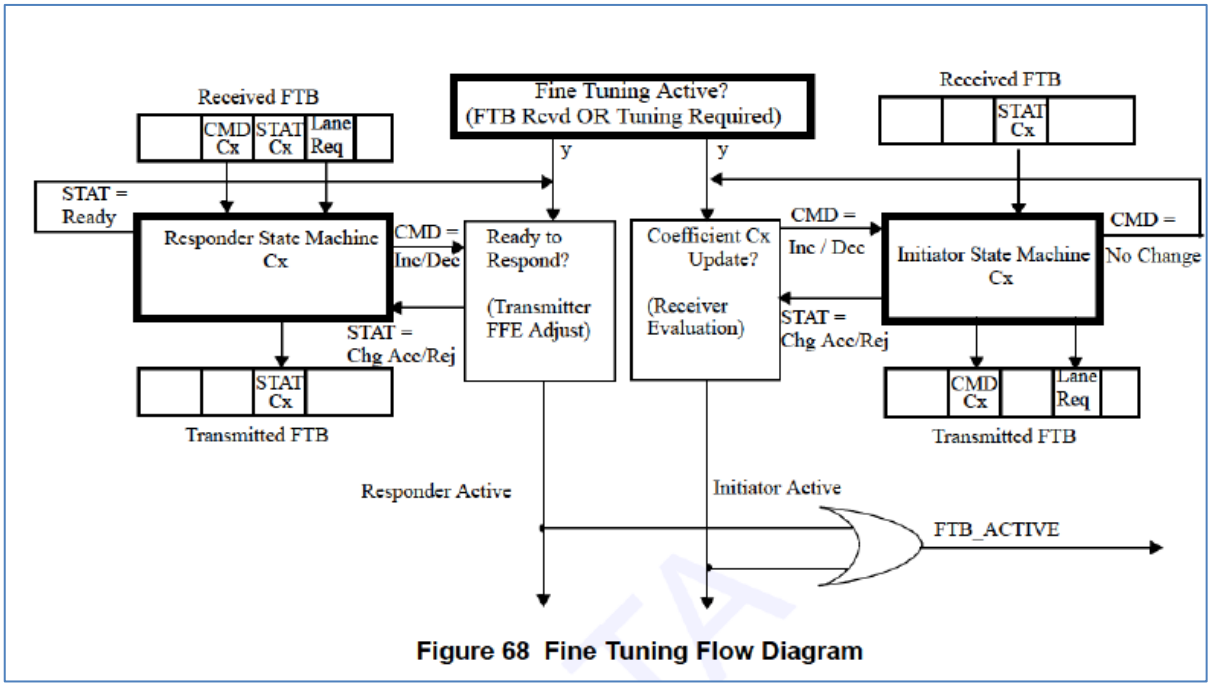
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 8	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 8	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 8	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required

Addr	Size	Type	Functions
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required

Addr	Size	Type	Functions
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional

Addr	Size	Type	Functions
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional

Addr	Size	Type	Functions
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies

Addr	Size	Type	Functions
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 8	Disclosure

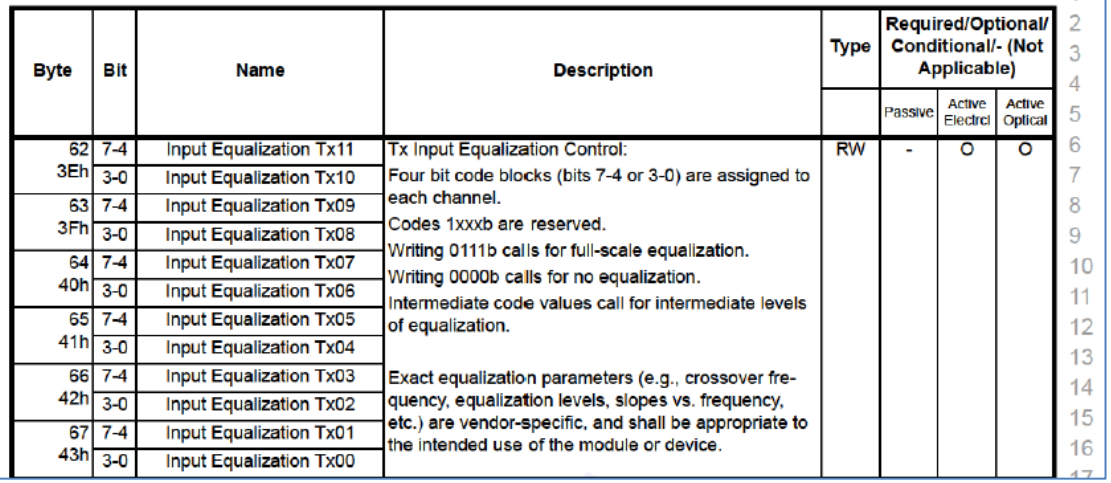
234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 8	Disclosure
	Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)  InfiniBand, Table 142 (p. 528)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

Claim 8	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

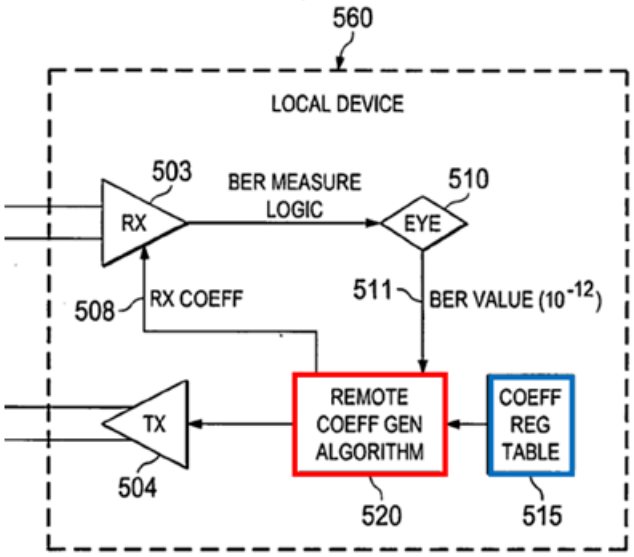
InfiniBand, Table 143 (p. 535)

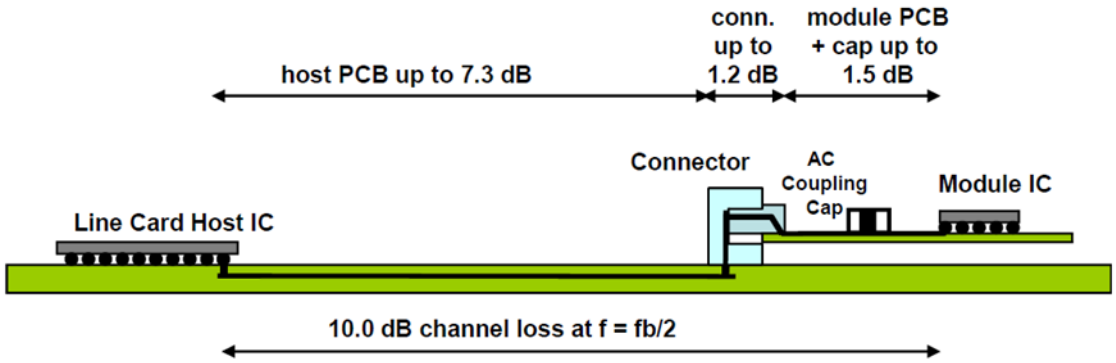
"The overall pre-equalizer **800** can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."

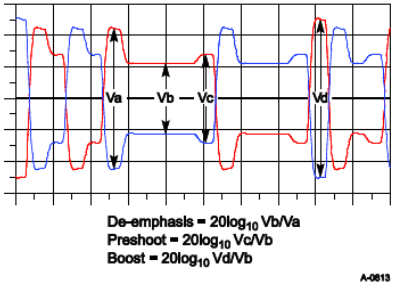
Rafie, paragraph 82.

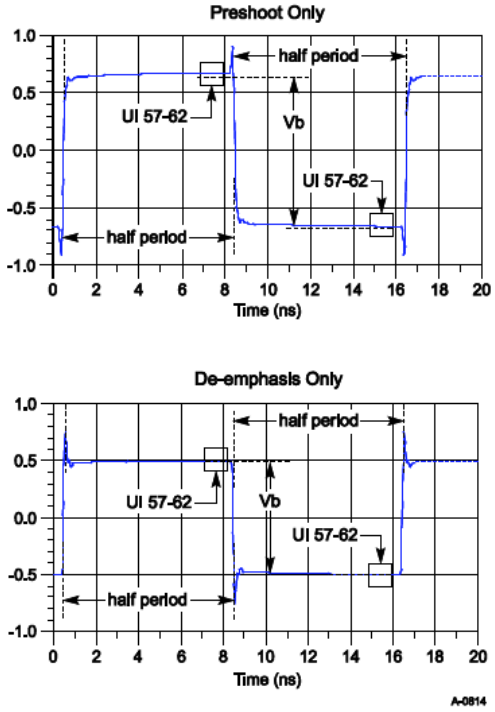
"Digital pre-equalizer (PEQ) circuit **204** can be configured to introduce a distortion to the input signal to compensate for channel impairment. At power-on little or no information may be known about the

Claim 8	Disclosure
	channel. Accordingly, the digital PEQ circuit **204** can be initially configured with no distortion. In some embodiments, the digital PEQ circuit **204** can be initially configured with a distortion that is based upon a corresponding set of coefficients." Ciacci, 5:40-47. "Once frequency response of front-end components has been characterized, this information can be stored in the digital base band on a configuration register (CFR), and thereby used to specify gain coefficients of the digital pre-equalizer." Balakrishnan, paragraph 27. *U.S. Patent Publication No. 2014/0281067 ("Das Sharma")* Das Sharma discloses selecting initial coefficient values for transmit filters for use in an adaptive pre-equalization training process from among the registers. *See, e.g.*, Das Sharma at [0078], [0193], Figure 5. Das Sharma discloses a coefficient register table is used by a coefficient algorithm module that provides a set of initial coefficients to the transceiver's transmission logic. *See id*. at [0078]. Figure 5 of Das Sharma shows the coefficient algorithm module (red) and coefficient register table (blue). *See id*. at [0078] ("coefficient algorithm module 520"). Das Sharma teaches that the coefficient algorithm module can be implemented by a microcontroller that includes the coefficient register table. *See id*. at [0078], [0193] (Das Sharma's "modules" can each be implemented via a "microcontroller" including "registers").

Claim 8	Disclosure
	 FIG. 5 *United States Patent No. 7,239,665 ("Mezer")* Mezer describes supporting Ethernet, and such standards-compliant implementation was conventional. *See, e.g.*, at Mezer, 4:55-57, 6:62-7:3. This obvious implementation would have met the Ethernet standard's description of a chip-to-module communication link comprising a port connector coupling a port transceiver to a pluggable module transceiver. *See, e.g.*, IEEE 802.3bs-2017, 323-330 (Annex 120C), 350-372 (Annex 120E), 350 ("The chip-to-module interface is defined using a specification… that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0"); *see also* OIF-CEI-04.0, 334, Fig. 16-15 (below, showing a "Connector" receiving a pluggable module).

Claim 8	Disclosure
	Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model  *PCIe 3.1a* **4.3.3.5.2. Tx Equalization Presets** An 8.0 GT/s transmitter must support a specified number of presets, where the preset values are defined in terms of voltage ratios as illustrated in Figure 4-42. Presets are defined in terms of two ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GTs/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. Figure 4-42 is shown as an example of TxEQ and is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of 8.0 GT/s signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms, as shown later in this section. The presets defined in Table 4-16 and Table 4-17 are numbered to match the designations in Section 4.2.3.1. Note, however, that in Section 4.2.3.1 the coefficients are defined as integers (using upper case "C"), while in the electrical section they are defined as floating point (using lower case "c"). PCIe 3.1a at 355.

Claim 8	Disclosure
	 **Figure 4-42: Definition of Tx Voltage Levels and Equalization Ratios** Figure 4-43 illustrates the waveforms that will be observed when measuring presets when using the 64-ones/64-zeroes sequence that is part of the compliance pattern. Depending on whether the preset implements de-emphasis, preshoot, or both the corresponding waveshape will differ. The two cases illustrated below show preshoot and de-emphasis, as can be observed by noting whether the boost occurs before or after each edge transition. For the case where both de-emphasis and preshoot are present, boost occurs both before and after each edge transition. Note that in all cases, however, the voltage of interest occurs during the flat portion (Vb) of the waveform, where it can be accurately measured independent of high frequency effects. PCIe 3.1a at 356.

Claim 8	Disclosure
	 Figure 4-43: Waveform Measurement Points for Pre-shoot and De-emphasis PCIe 3.1a at 357.

Claim 8	Disclosure

Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

Notes:

1. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The allowable P10 boost range is defined by the coefficient space lying between the Min and Max Reduced Swing Limits as shown by the two diagonal lines in the example of Figure 4-45. This approach permits both full and reduced swing transmitters to use P10 for testing to their respective boost limits.

With the exception of P4 (for which both pre-shoot and de-emphasis are 0.0 dB) it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are 1 UI wide and therefore subject to attenuation by the package and the breakout channel. Instead the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval. Table 4-17 lists the preset values required to measure each of the Va and Vc values from which the preshoot or de-emphasis values may be derived.

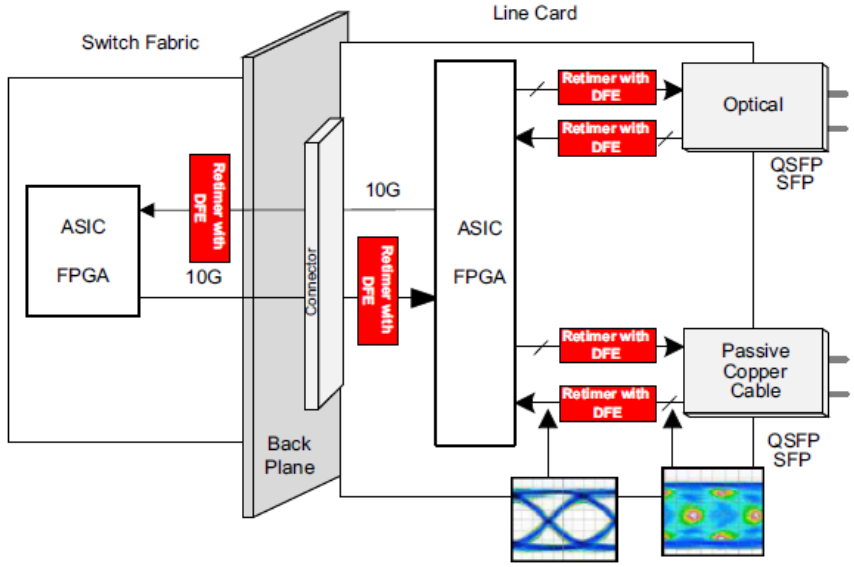
PCIe 3.1a at 358.

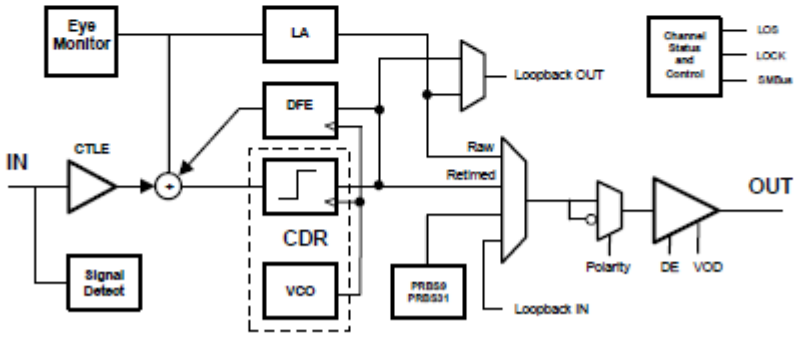
Claim 8	Disclosure
	Table 4-17: Preset Measurement Cross Reference Table PCIe 3.1a at 359.

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P4	N/A	N/A
P1	P1/P4	N/A
P0	P0/P4	N/A
P9	N/A	P4/P9
P8	P8/P6	P3/P8
P7	P7/P5	P2/P7
P5	N/A	P4/P5
P6	N/A	P4/P6
P3	P3/P4	N/A
P2	P2/P4	N/A
P10	P10/P4	N/A

Claim 8	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 8	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 8	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 8	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 8	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 8	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

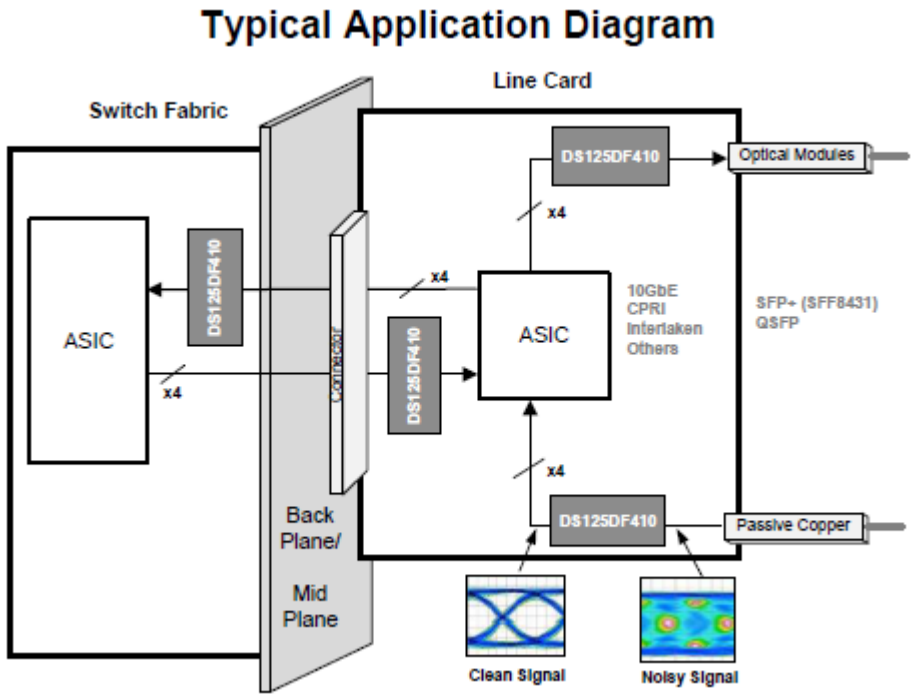
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

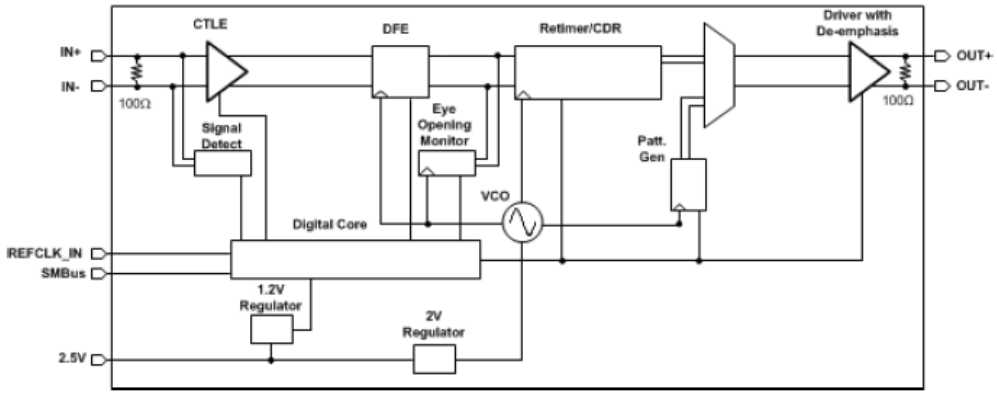
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 8	Disclosure
	 TI DS125DF410, 1.

Claim 8	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 8	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 8	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 8	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 8	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 8	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

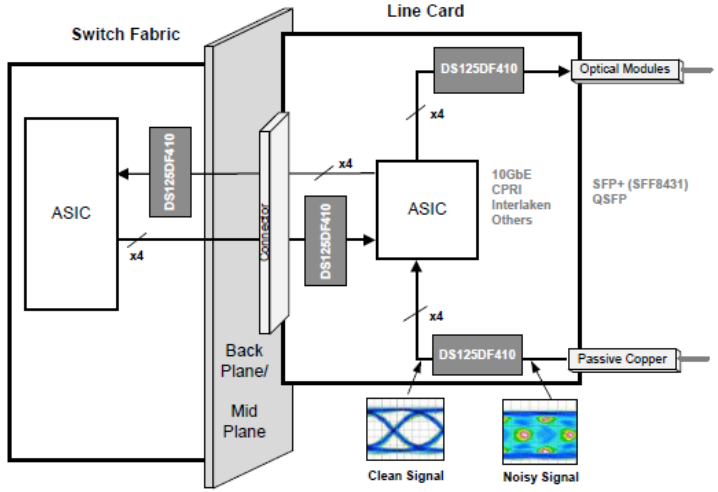
TI DS125DF410, 41.

Claim 8	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 8	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 8	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

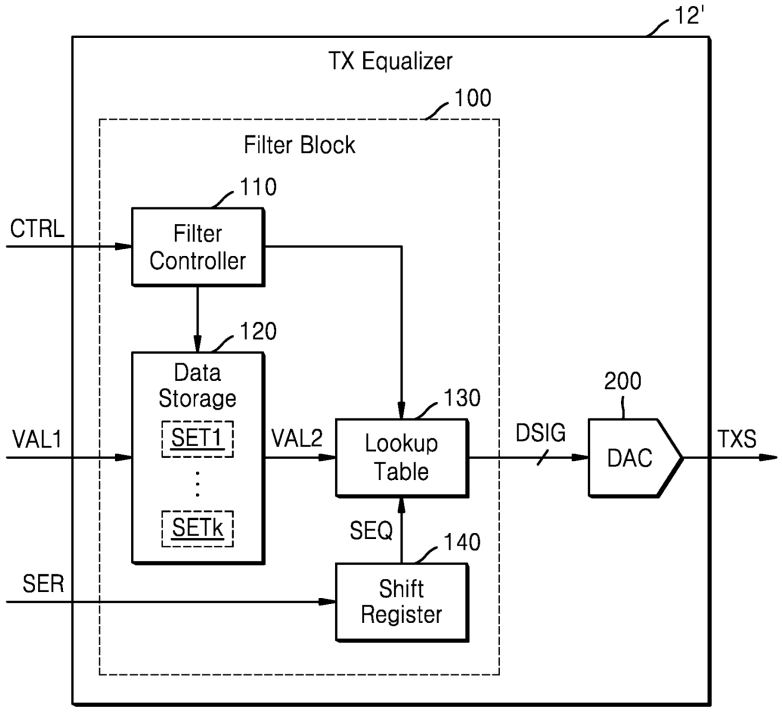
Claim 8	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Claim 8	Disclosure
8[c] the controller using one of the registers to set initial coefficient values for the one or more transmit filters.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**." Kang, 5:20-42.

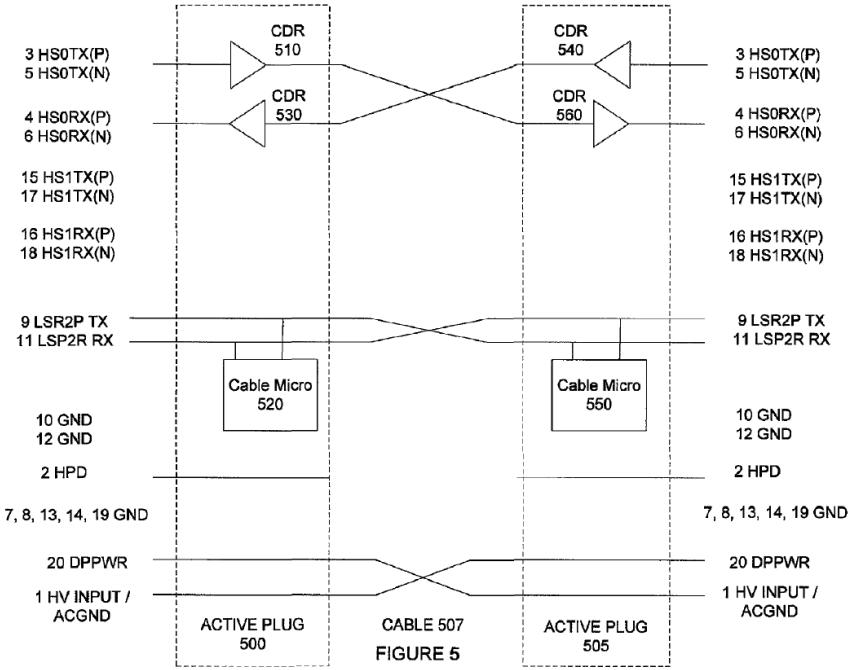
Claim 8	Disclosure
	"FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS, which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3.

Claim 8	Disclosure
	The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively.

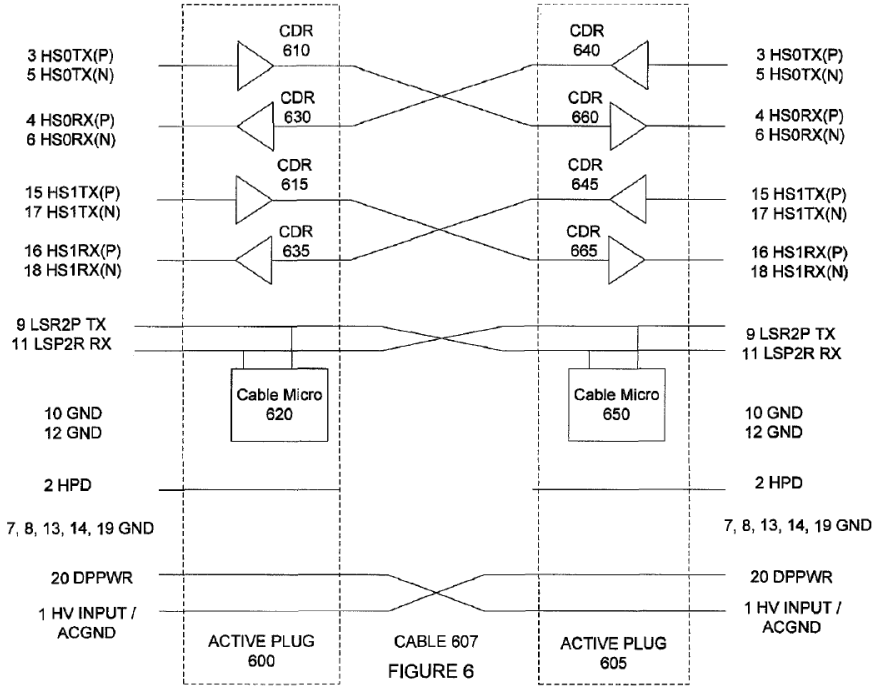
Claim 8	Disclosure
	The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 8	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

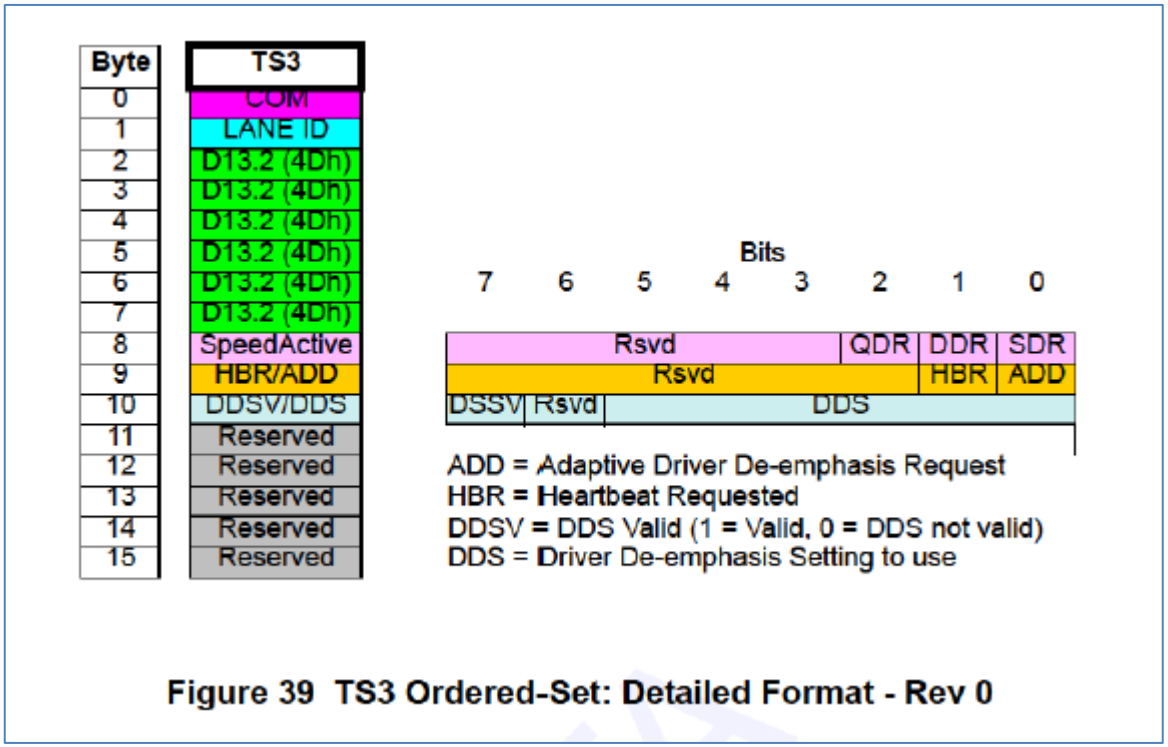
Claim 8	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 8	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 8	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 8	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 8	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 8	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 8	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

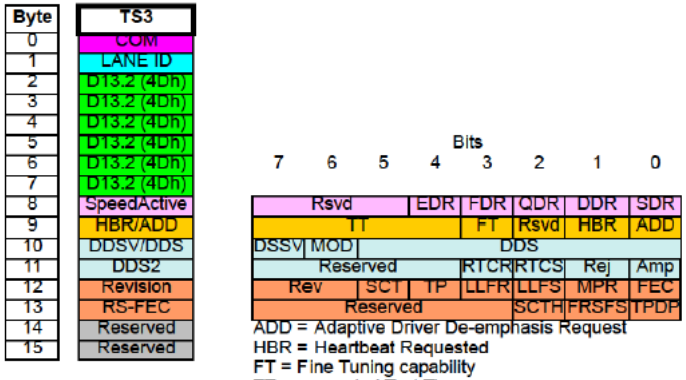
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 8	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 8	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 8	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 8	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 8	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 8	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 8	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 8	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

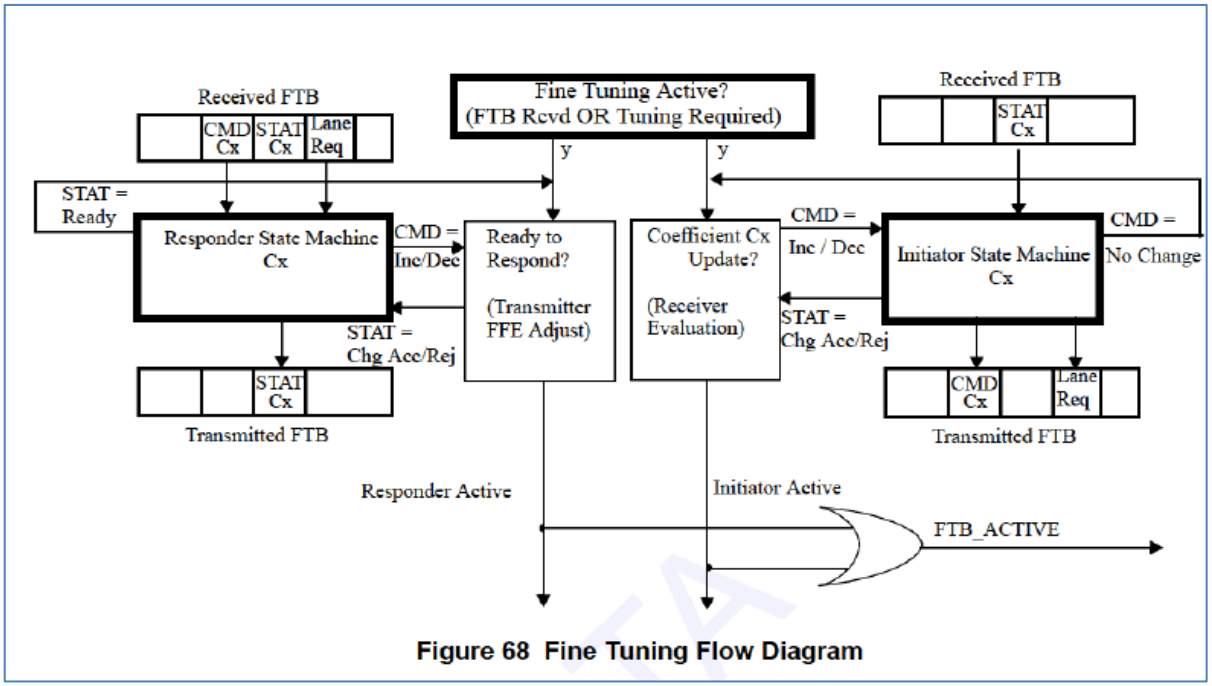
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 8	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 8	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 8	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required

Addr	Size	Type	Functions
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required

Addr	Size	Type	Functions
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional

Addr	Size	Type	Functions
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional

Addr	Size	Type	Functions
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies

Addr	Size	Type	Functions
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 8	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 8	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 8	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"The overall pre-equalizer **800** can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."

Rafie, paragraph 82.

"Digital pre-equalizer (PEQ) circuit **204** can be configured to introduce a distortion to the input signal to compensate for channel impairment. At power-on little or no information may be known about the channel. Accordingly, the digital PEQ circuit **204** can be initially configured with no distortion. In some

Claim 8	Disclosure
	embodiments, the digital PEQ circuit **204** can be initially configured with a distortion that is based upon a corresponding set of coefficients." Ciacci, 5:40-47. "Once frequency response of front-end components has been characterized, this information can be stored in the digital base band on a configuration register (CFR), and thereby used to specify gain coefficients of the digital pre-equalizer." Balakrishnan, paragraph 27. <u>*PCIe 3.1a*</u> The equalization procedure consists of up to four Phases, as described below. When operating at the 8.0 GT/s data rate, the Phase information is transmitted using the Equalization Control (EC) field in the TS1 Ordered Sets. Phase 0: The Downstream Port communicates the Transmitter preset values and the Receiver preset hints for each Lane to the Upstream Port using 8b/10b encoding. These values are communicated using the EQ TS2 Ordered Sets (defined in Section 4.2.4.1) in Recovery.RcvrCfg, when a data rate change to 8.0 GT/s has been negotiated, prior to transitioning to 8.0 GT/s data

Claim 8	Disclosure
	rate. These preset values are derived from the Upstream Port Transmitter Preset and Upstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. After the data rate change to 8.0 GT/s, the Upstream Port transmits TS1 Ordered Sets with the preset values it received. The preset values must be within the operable range defined in Section 4.3.3.5.2 if reduced swing will be used by the Transmitter. Phase 1: Both components make the Link operational enough at 8.0 GT/s data rate to be able to exchange TS1 Ordered Sets to complete remaining phases for the fine-tuning their Transmitter/Receiver pairs. It is expected that the Link will operate at a BER of less than 10^{-4} before the component is ready to move on to the next Phase. The Downstream Port initiates Phase 1 by transmitting TS1 Ordered Sets with EC=01b (indicating Phase 1) to the Upstream Port using the preset values in the Downstream Port Transmitter Preset and, optionally, the Downstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. The Upstream Port, after adjusting its Receiver, if necessary, to ensure that it can progress with the equalization process, receives these TS1 Ordered Sets and transitions to Phase 1 (where it transmits TS1 Ordered Sets with EC=01b). The Downstream Port ensures that it can reliably receive the bit stream from the Upstream Port to continue through the rest of the Phases when it receives TS1 Ordered Sets from the Upstream Port with EC=01b before it moves on to Phase 2. Phase 2: In this Phase the Upstream Port adjusts the Transmitter setting of the Downstream Port along with its own Receiver setting, independently, on each Lane, to ensure it receives the bit stream compliant with the requirements in Section 4.3 (e.g., all operational Downstream Lanes have a BER is less than 10^{-12}). The Downstream Port initiates the move to Phase 2 by transmitting TS1 Ordered Sets with EC=10b to the Upstream Port. The Downstream Port advertises the Transmitter coefficients and the preset it is using per the rules below in Phase 1 for preset only and in Phase 2 for preset and coefficients. The Upstream Port receives these Ordered Sets and may request different coefficient or preset settings and continue to evaluate each setting until it arrives at the best setting for operating the Downstream Lanes. After the Upstream Port has completed this Phase, it moves the Link to Phase 3 by transmitting TS1 Ordered Sets with EC=11b to the Downstream Port. Phase 3: In this Phase the Downstream Port adjusts the Transmitter setting of the Upstream Port along with its own Receiver setting, independently, on each Lane, using a handshake and evaluation process similar to Phase 2 with the exception that EC=11b. The Downstream Port signals the end of Phase 3 (and the equalization procedure) by transmitting TS1 Ordered Sets with EC=00b. PCIe 3.1a at 240-241.

Claim 8	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 8	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 8	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

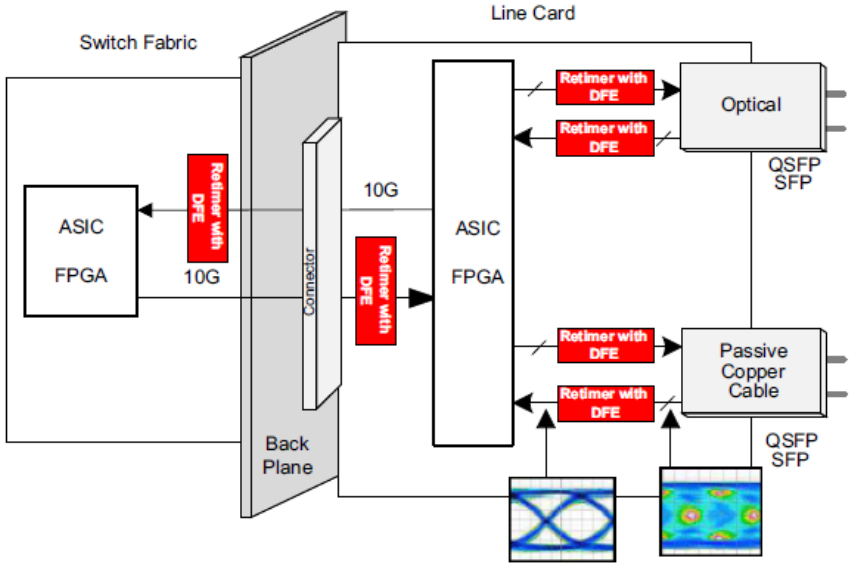
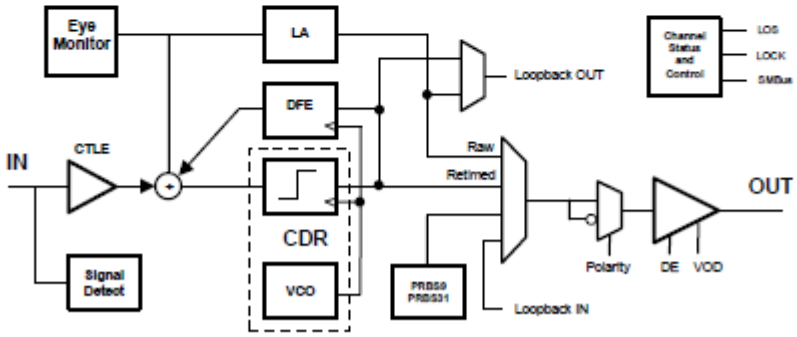


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 8	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 8	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 8	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

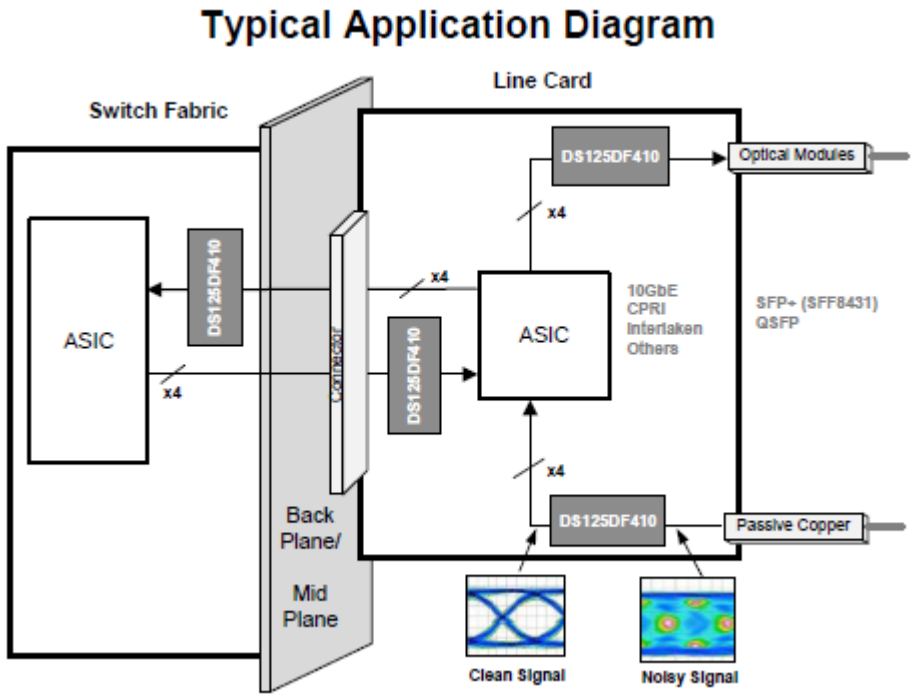
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

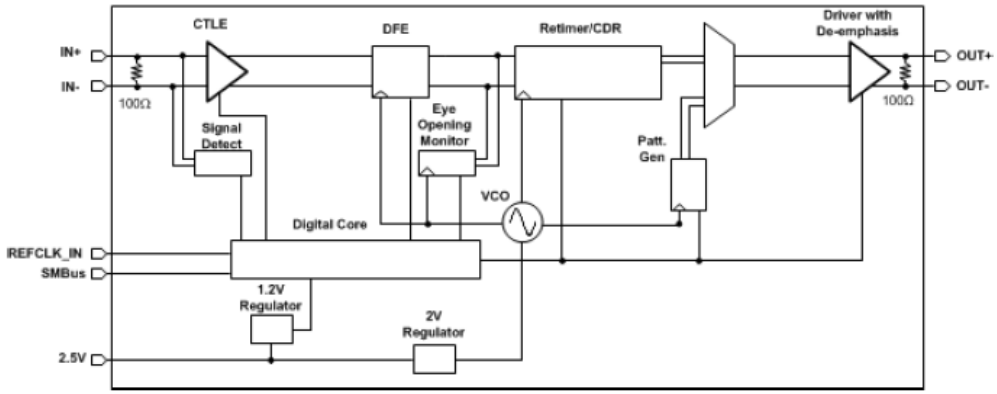
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 8	Disclosure
	 TI DS125DF410, 1.

Claim 8	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 8	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 8	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 8	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 8	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 8	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 8	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

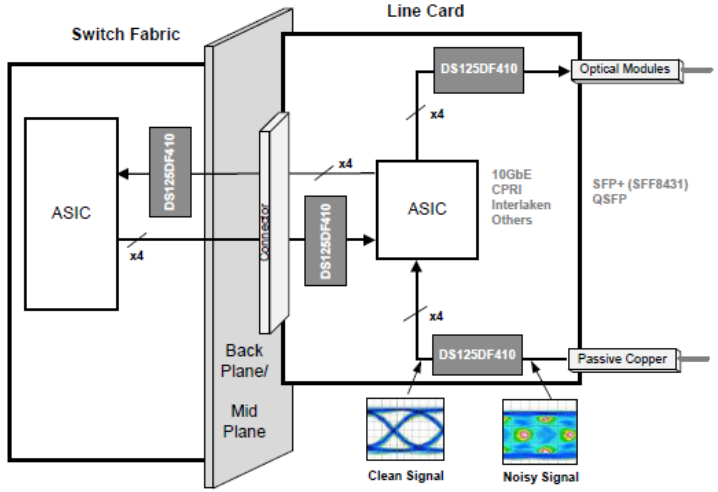
TI DS125DF410, 41.

Claim 8	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 8	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 8	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 8	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

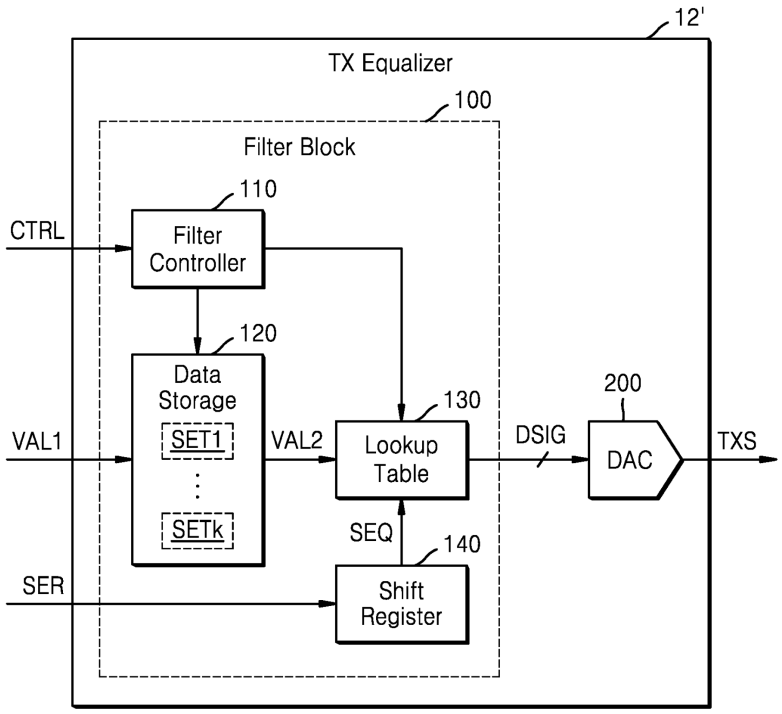
I. DEPENDENT CLAIM 9

Claim 9	Disclosure
9. The communications link of claim 8, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

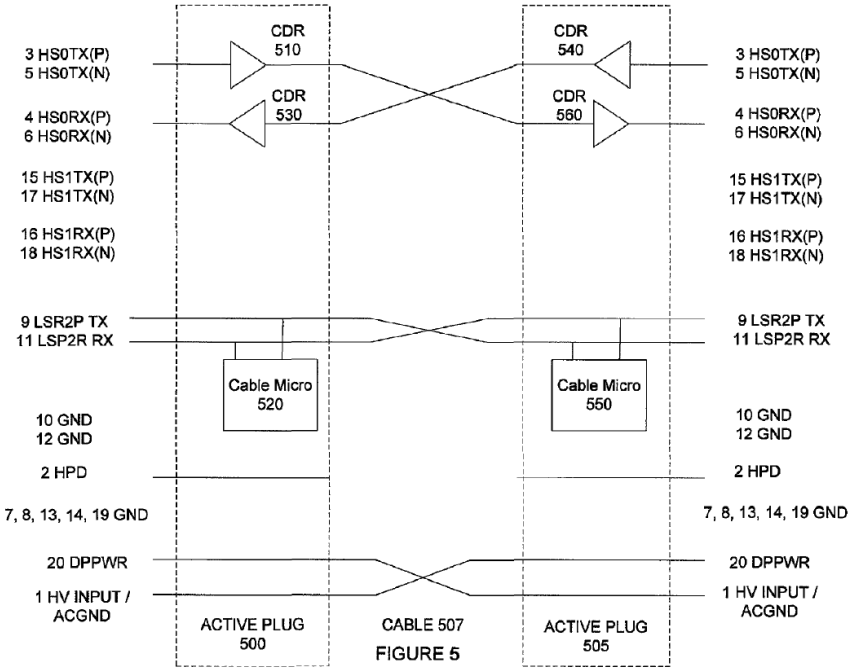
Claim 9	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 9	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

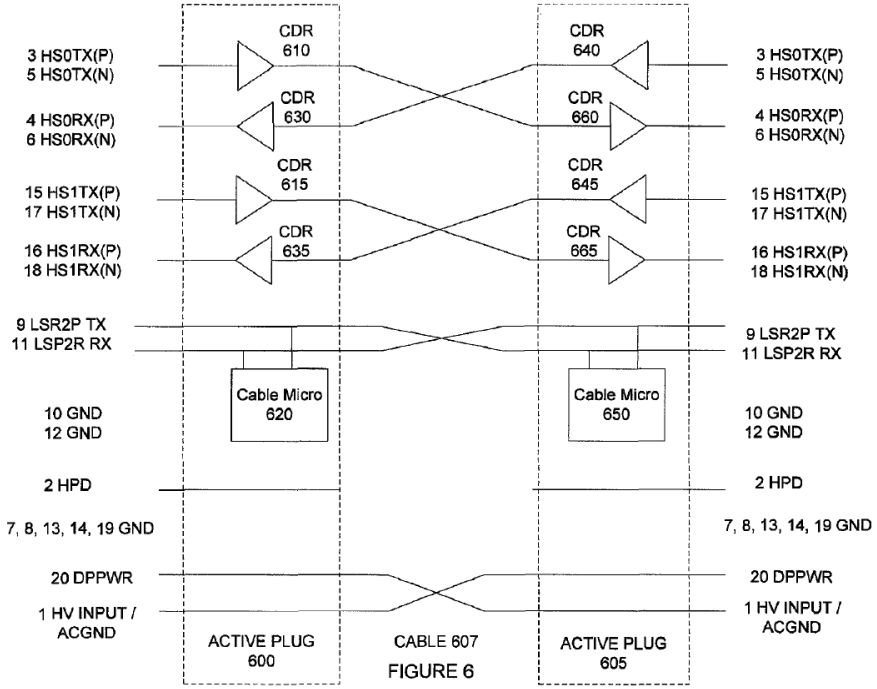
Claim 9	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 9	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 9	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

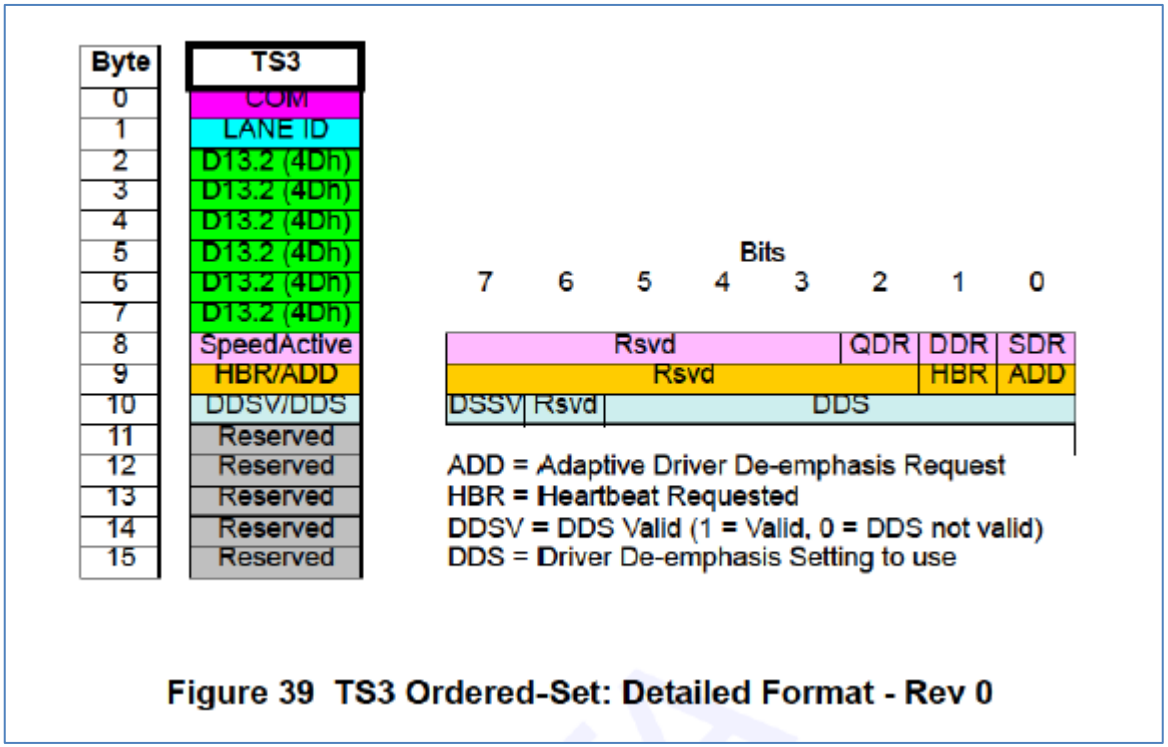
Claim 9	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 9	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 9	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 9	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 9	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 9	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

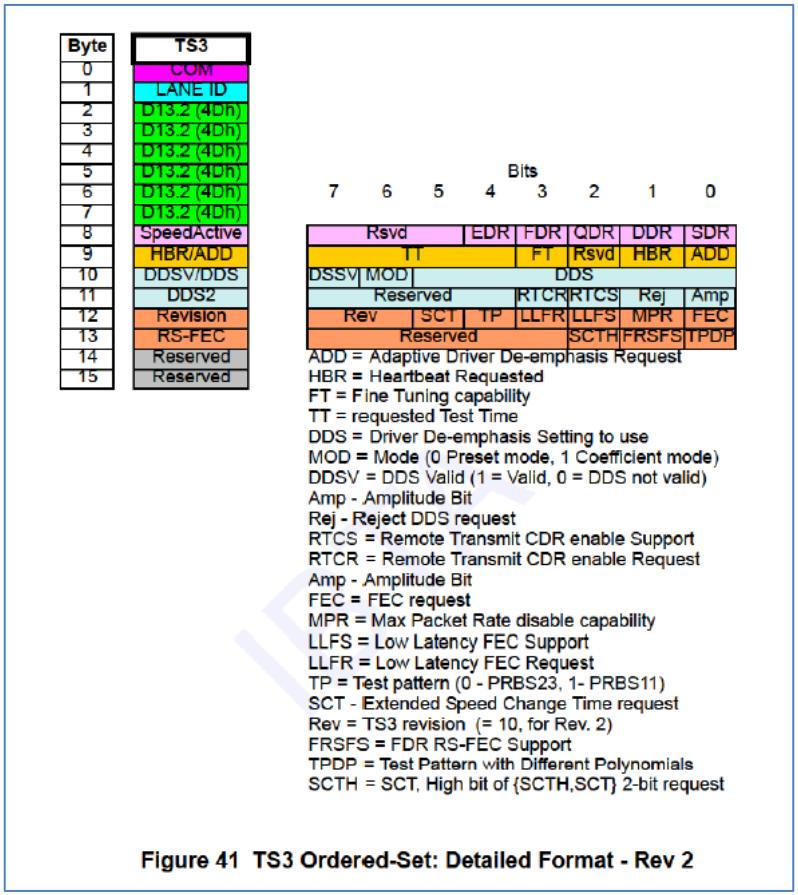
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 9	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 9	Disclosure
	5.5.2.4.1 Rev 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 9	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 9	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 9	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 9	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 9	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 9	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

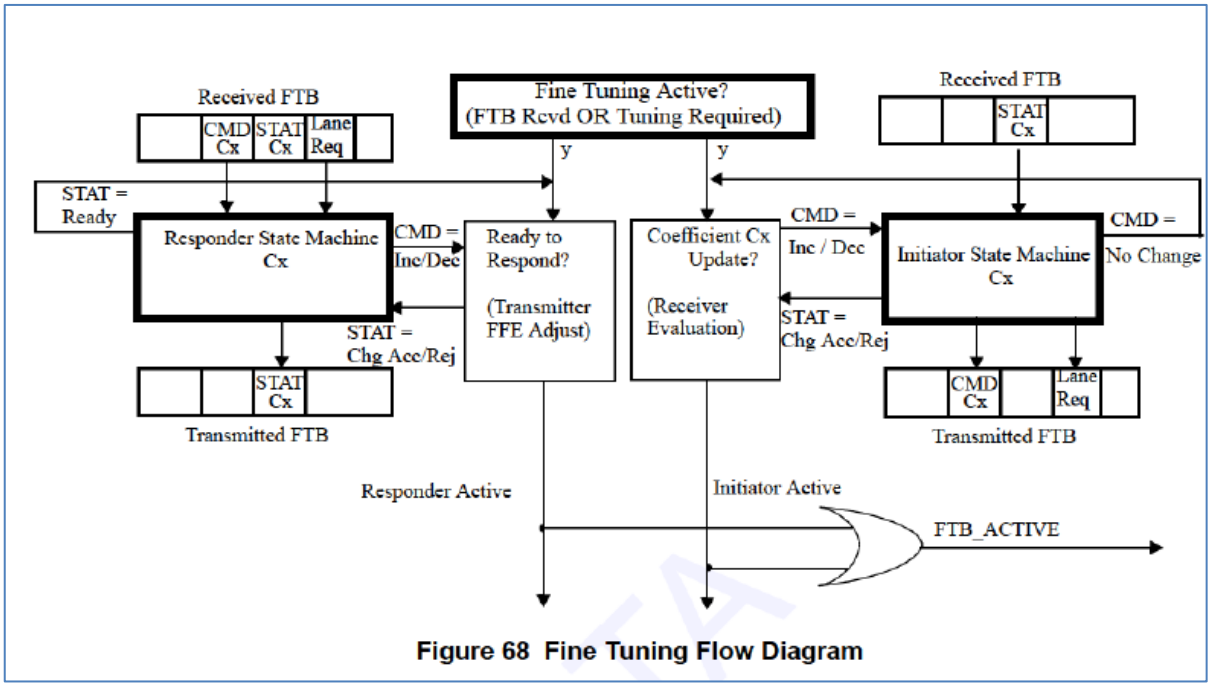
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 9	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 9	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 9	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 9	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 9	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 9	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"The digital pre-equalization of the present invention compensates frequency shaping commonly introduced by transmission components (e. g., front-end filters, antenna equipment).".

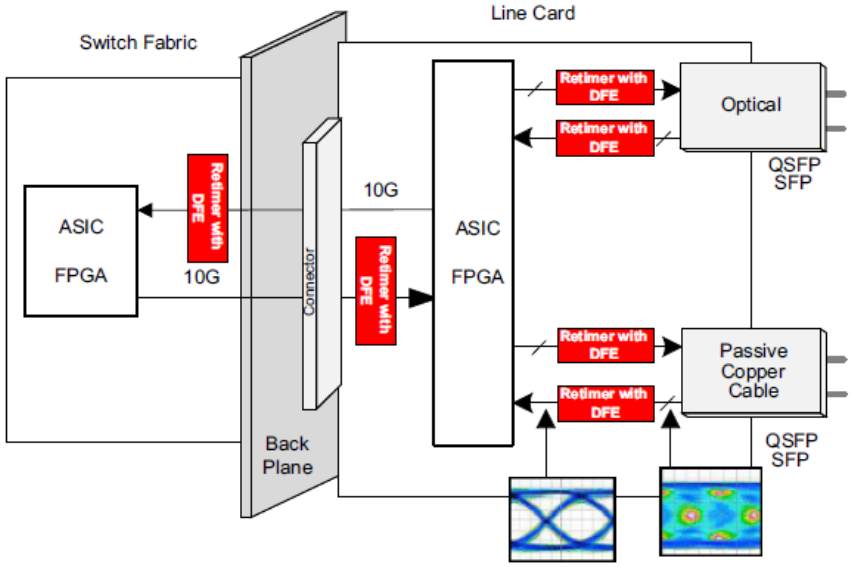
Balakrishnan, paragraph 22.

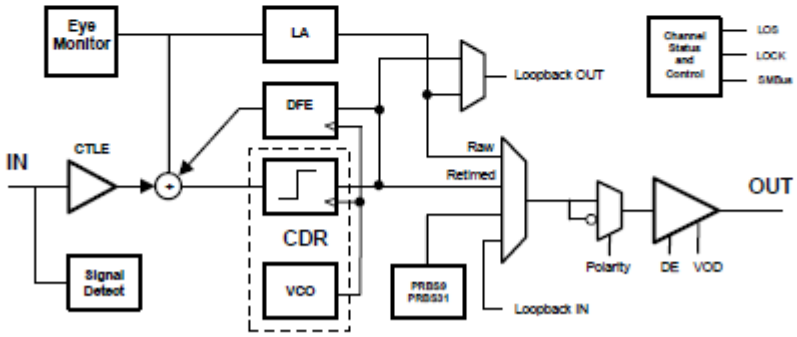
U.S. Patent Publication No. 2014/0281067 ("Das Sharma")

An ordinarily skilled artisan would known about losses in a chip-to-module channel between an active cable's transceiver and the host transceiver, which were routinely compensated for by of pre-equalization. *See, e.g.*, Das Sharma at [0075] (describing the use of equalization to compensate for different types of channel loss).

Claim 9	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 9	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 9	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 9	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 9	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 9	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

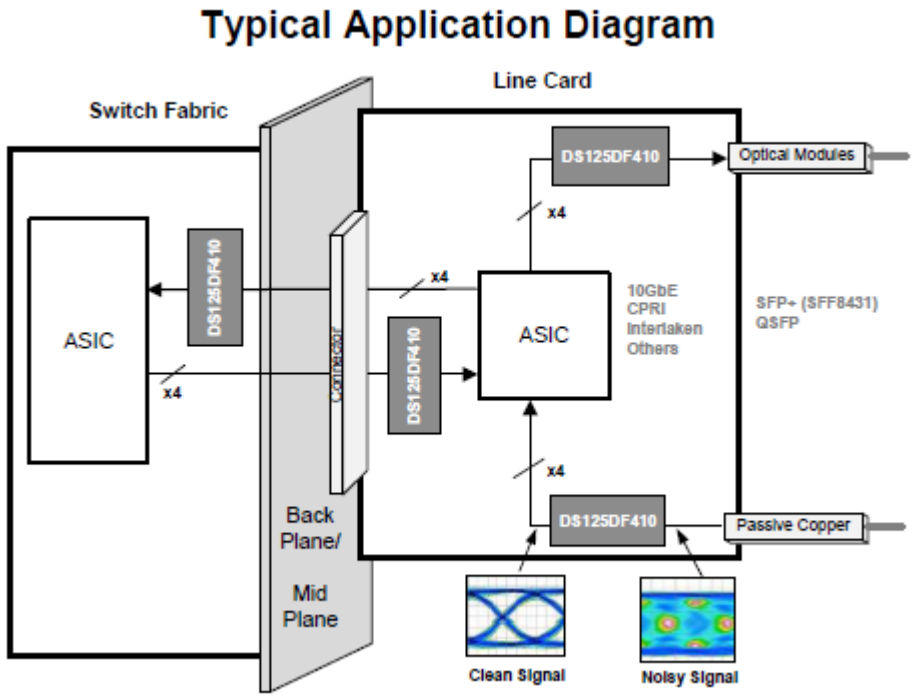
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

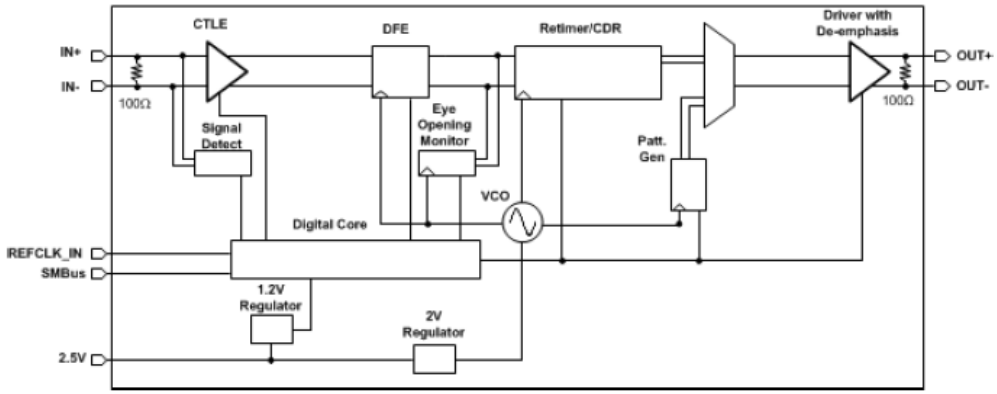
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 9	Disclosure
	 TI DS125DF410, 1.

Claim 9	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 9	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 9	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 9	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 9	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 9	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 9	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 9	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 9	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

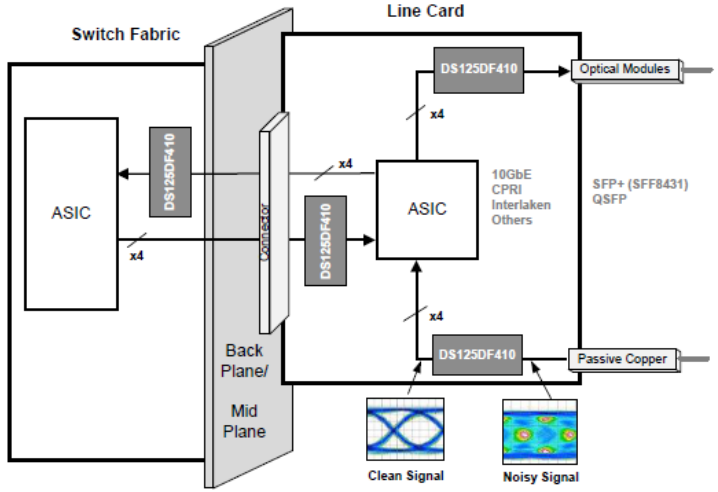
TI DS125DF410, 41.

Claim 9	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 9	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 9	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 9	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

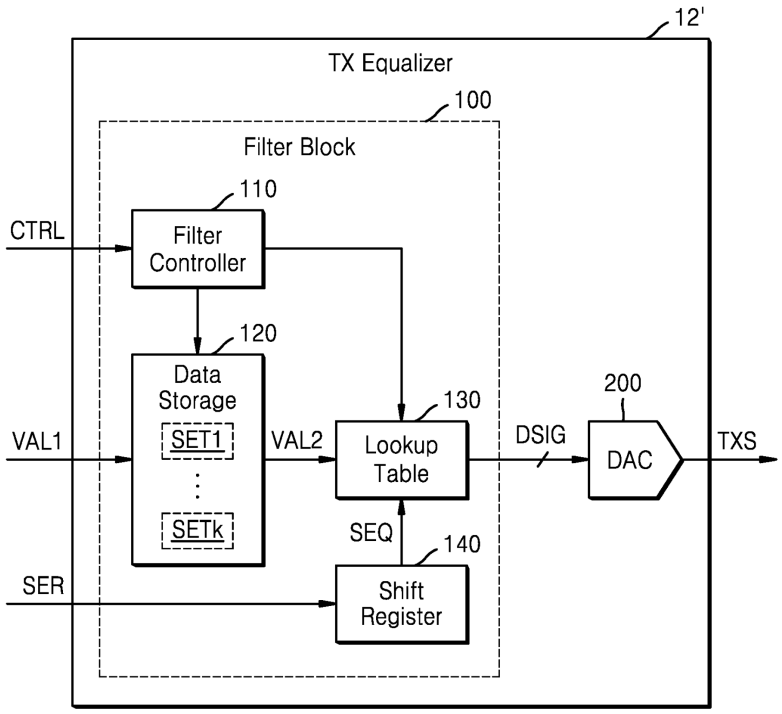
J. DEPENDENT CLAIM 10

Claim 10	Disclosure
10. The communications link of claim 8, wherein at least some of the different channel models presume different types of receiver equalization.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

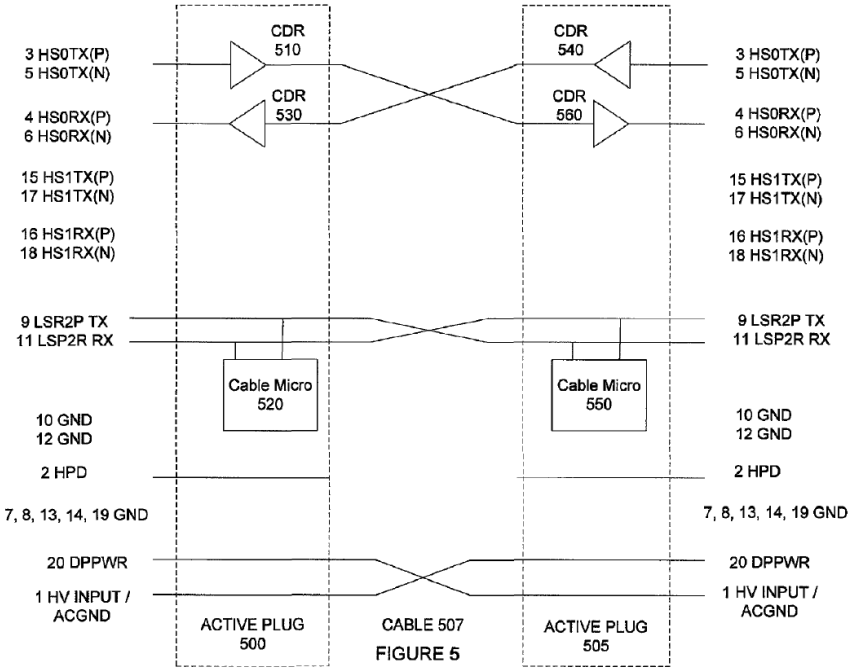
Claim 10	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 10	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

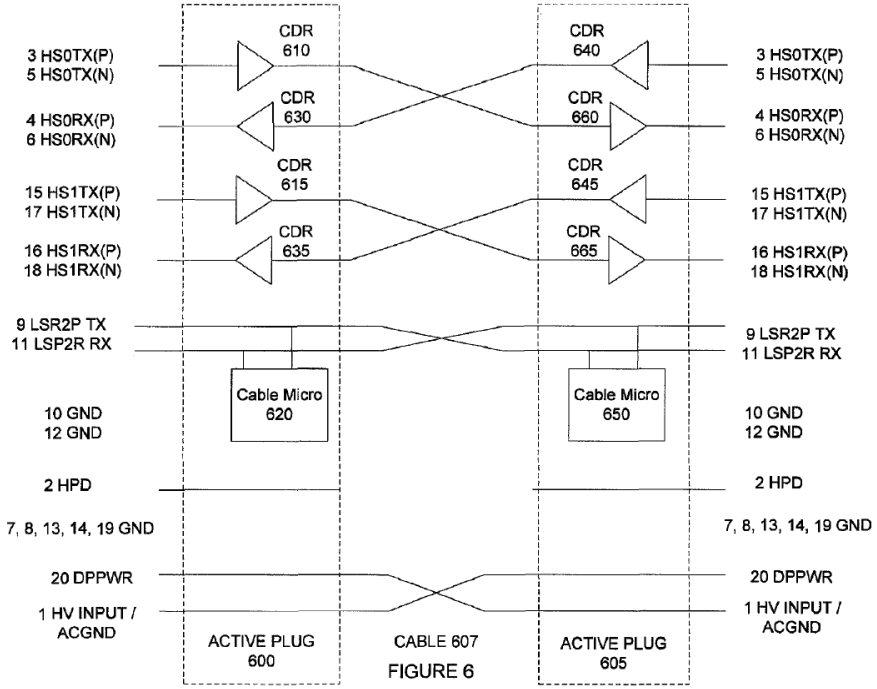
Claim 10	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 10	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 10	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

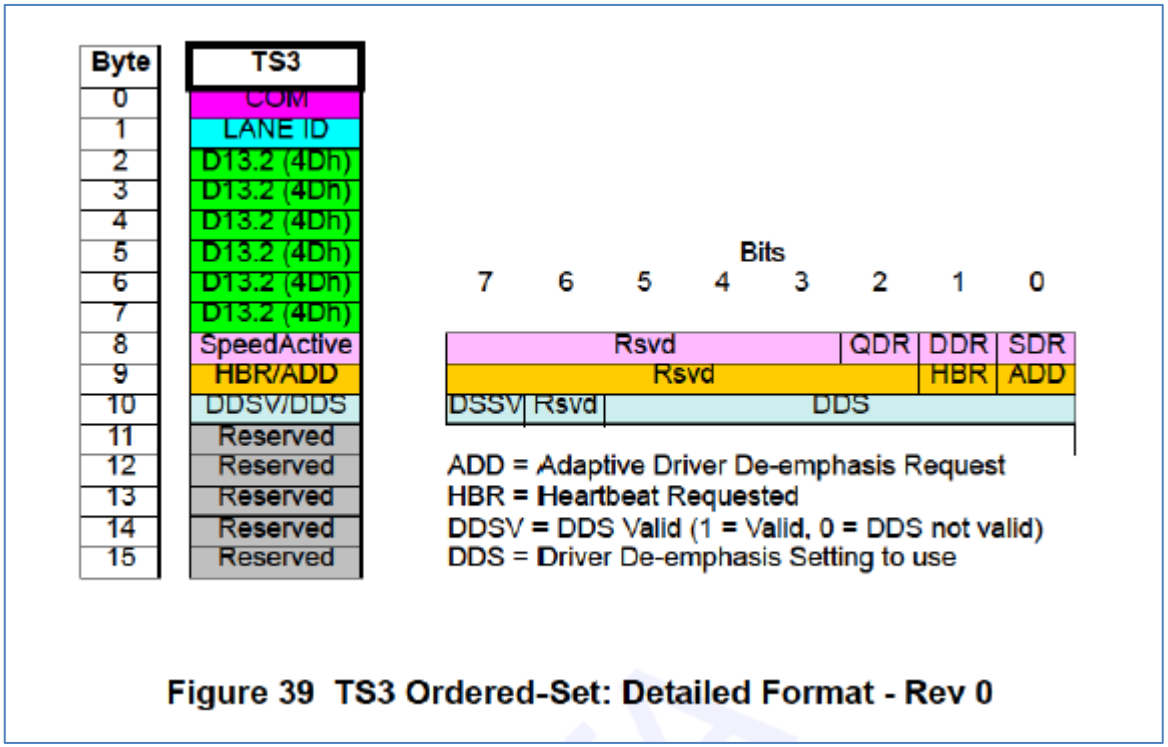
Claim 10	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 10	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 10	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 10	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 10	Disclosure

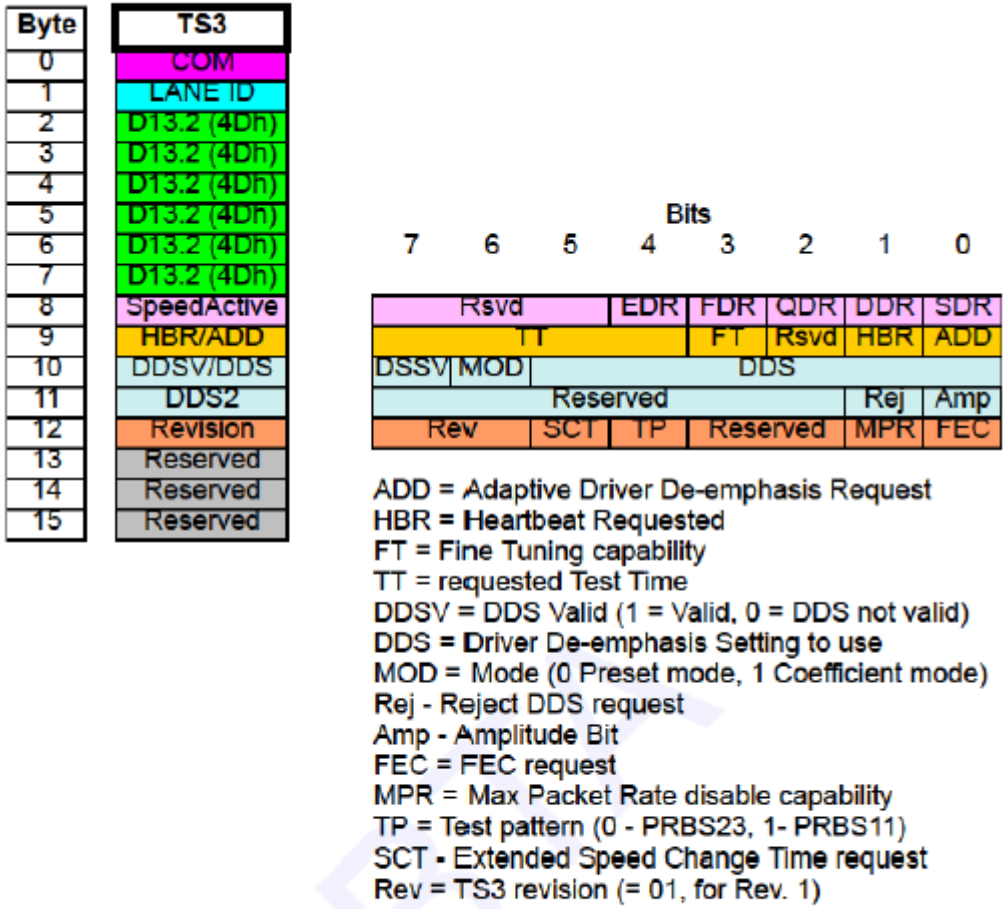


Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 10	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

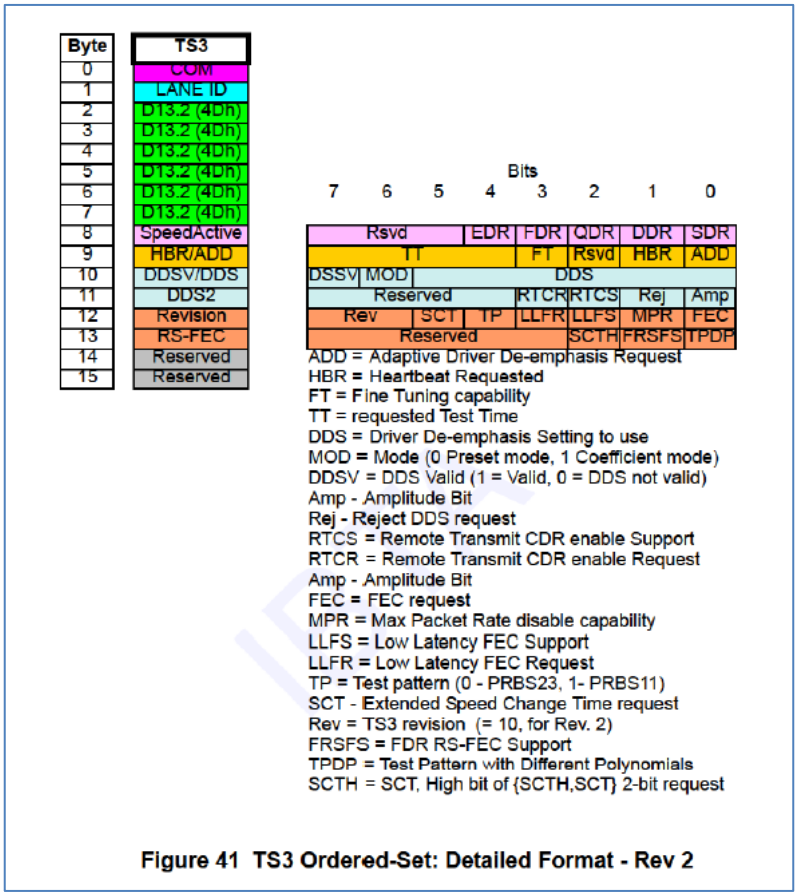
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 10	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 10	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 10	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 10	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 10	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 10	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 10	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 10	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

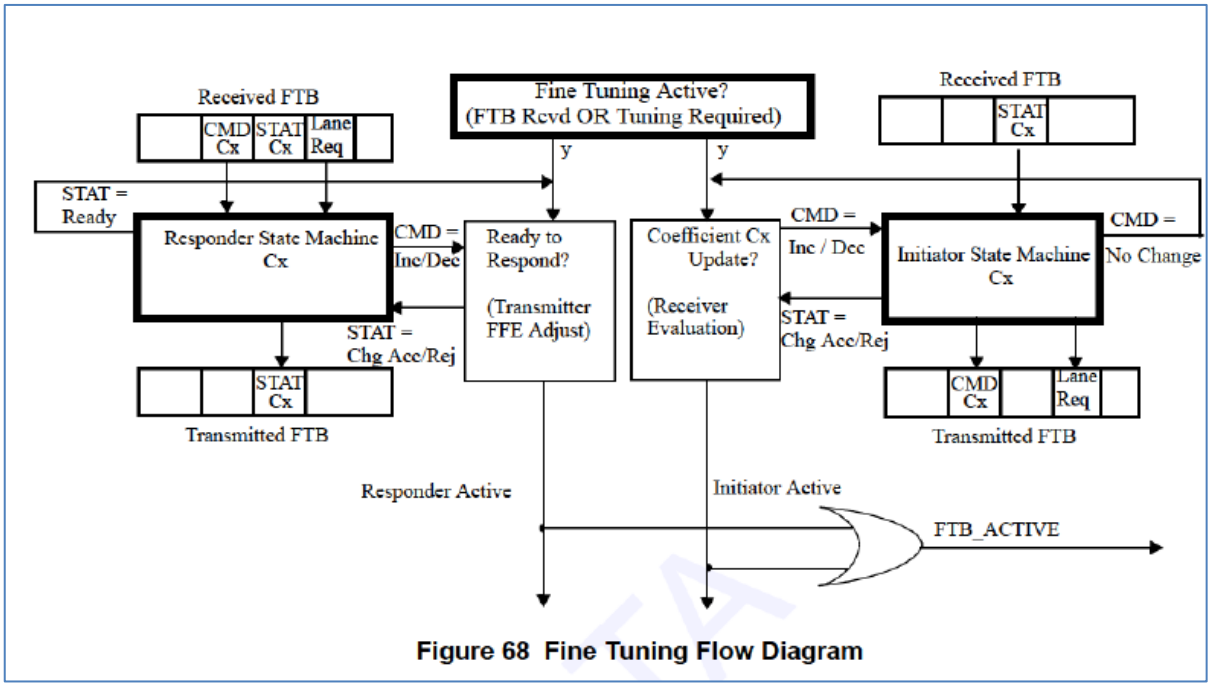
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 10	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 10	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 10	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required

Addr	Size	Type	Functions
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required

Addr	Size	Type	Functions
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional

Addr	Size	Type	Functions
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional

Addr	Size	Type	Functions
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies

Addr	Size	Type	Functions
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 10	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 10	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 10	Disclosure

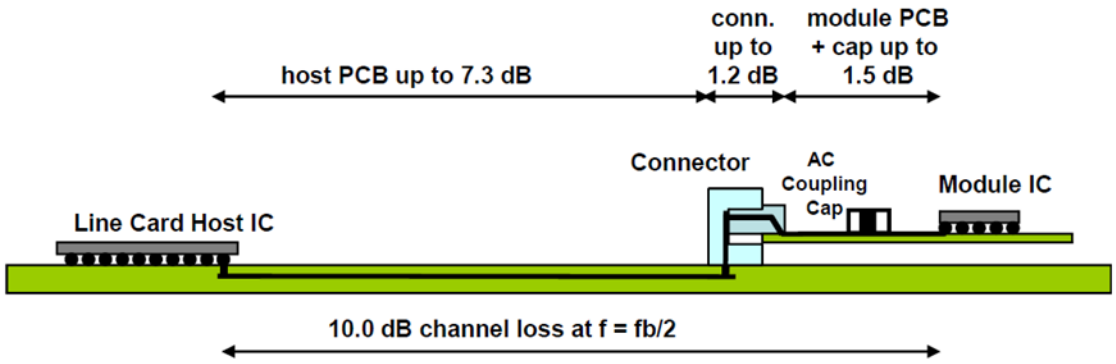
Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"The overall pre-equalizer **800** can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."

Rafie, paragraph 82.

	U.S. Patent Publication No. 2014/0281067 ("Das Sharma") Das Sharma describes pre-equalization "on a per transmitter-receiver pair basis to ensure interoperability" between the transmitter and the receiver in compensating for the channel's distortion. *See, e.g.*, Das Sharma at [0064]. An ordinarily skilled artisan knew that at least some of the different channel models presume different types of receiver equalization to ensure interoperability between different transmitter-receiver pairs, to ensure that they each mitigate channel degradation. *See, e.g.*, Das Sharma at [0064]. *United States Patent No. 7,239,665 ("Mezer")* Mezer describes supporting Ethernet, and such standards-compliant implementation was conventional. *See, e.g.*, at Mezer, 4:55-57, 6:62-7:3. This obvious implementation would have met the Ethernet standard's description of a chip-to-module communication link comprising a port connector coupling a port transceiver to a pluggable module transceiver. *See, e.g.*, IEEE 802.3bs-2017, 323-330 (Annex 120C), 350-372 (Annex 120E), 350 ("The chip-to-module interface is defined using a specification… that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0"); *see also* OIF-CEI-04.0, 334, Fig. 16-15 (below, showing a "Connector" receiving a pluggable module). **Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model** 

Claim 10	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 10	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 10	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

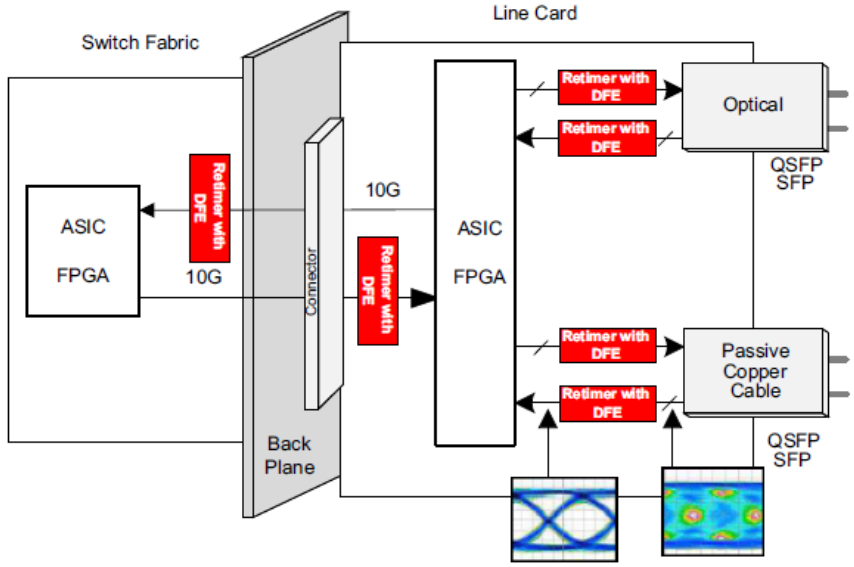
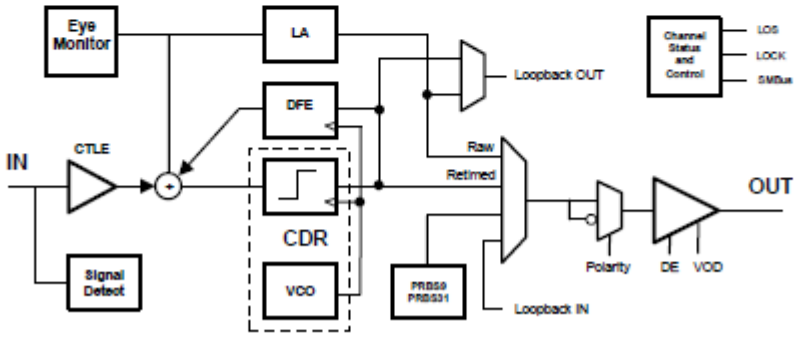


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 10	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 10	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 10	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

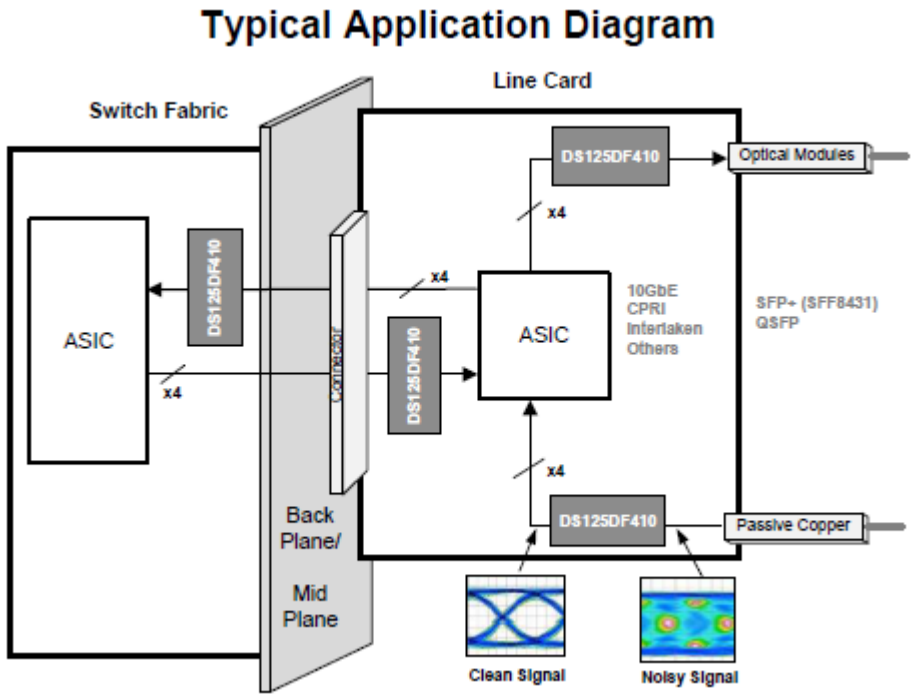
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

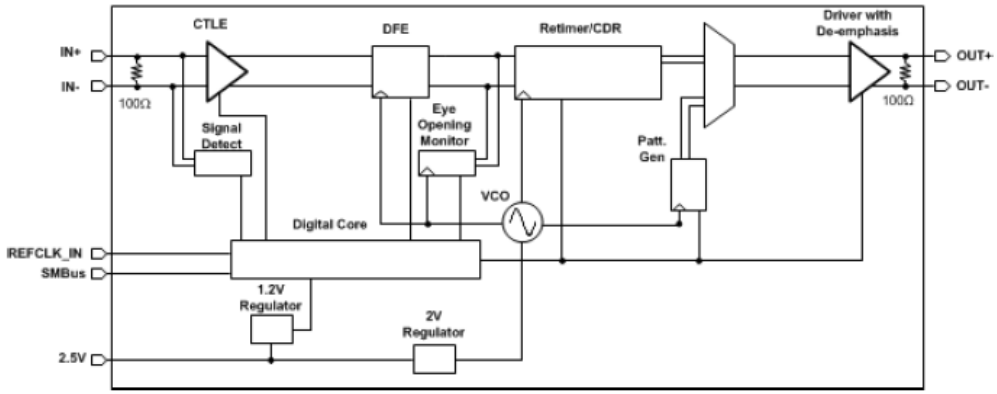
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 10	Disclosure
	 TI DS125DF410, 1.

Claim 10	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 10	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 10	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 10	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 10	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 10	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 10	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 10	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 10	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

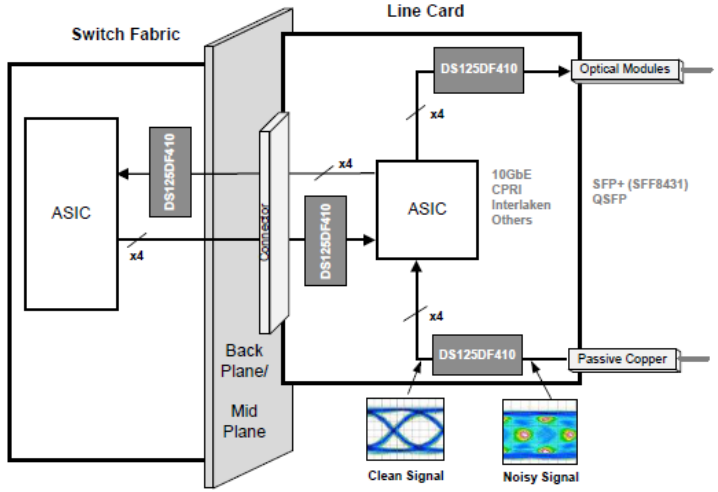
TI DS125DF410, 41.

Claim 10	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 10	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 10	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 10	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

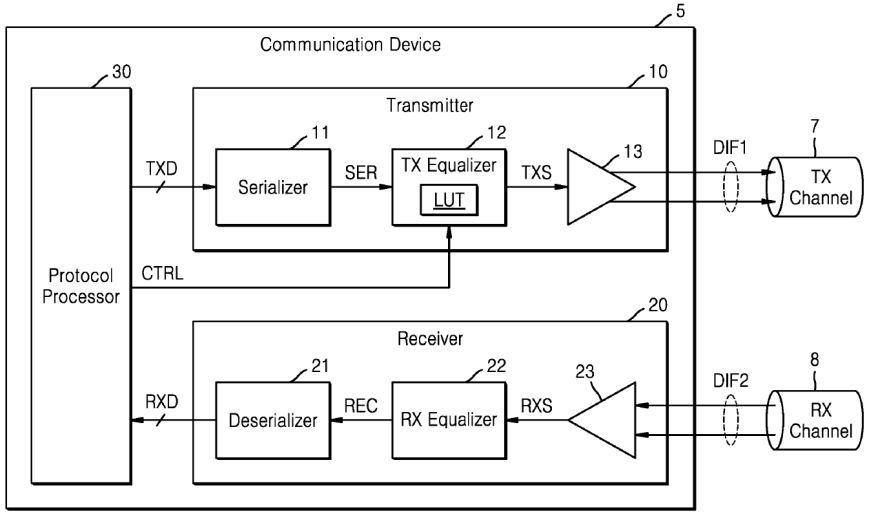
Exhibit C-12

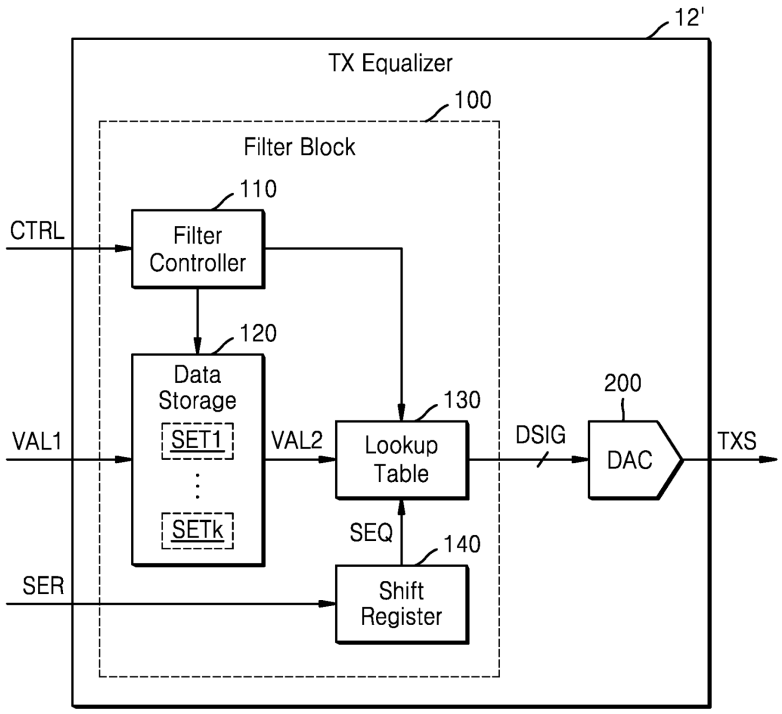
Claim 10	Disclosure

K. INDEPENDENT CLAIM 11

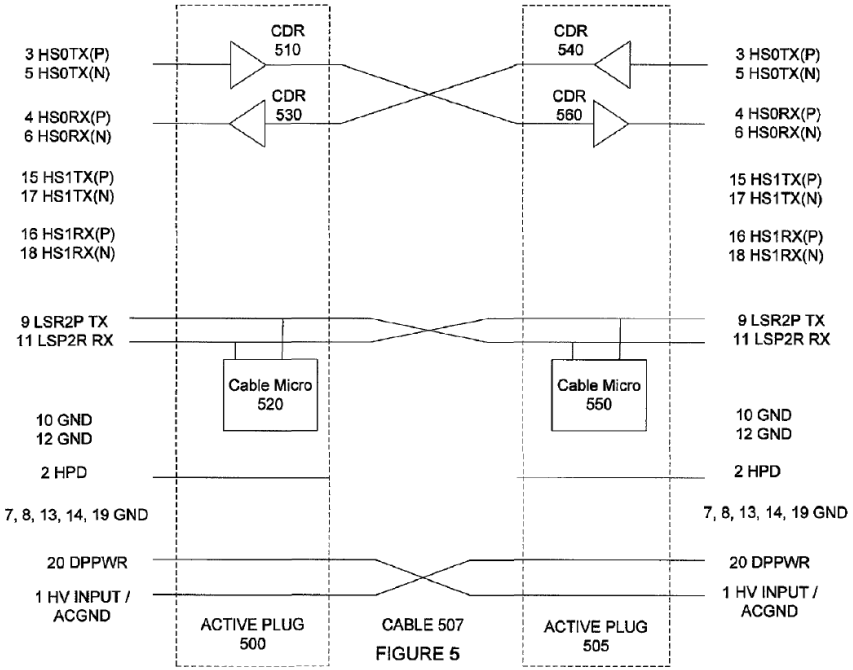
Claim 11	Disclosure
11[pre] A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "The disclosure relates to an equalizer, and more particularly, to an equalizer including a lookup table and a transmitter including the equalizer. In serial communication, an interconnection between a transmitter and a receiver, i.e., a channel, may distort signals. In order to compensate for distortion of signals generated in the channel, the transmitter and/or the receiver may include an equalizer. For example, the equalizer included in the transmitter may include a Finite Impulse Response (FIR) filter that provides an inverse transfer function of the transfer function of the channel. An equalizer including a high complexity filter may be necessary in order to precisely compensate for signal distortion while performing fast signal filtering for high speed serial communication. Further, in order to reduce power consumption and heat generation, an equalizer capable of reducing power consumption may be necessary." Kang, 1:13-30 "FIG. 1 is a block diagram illustrating a communication device **5** according to an exemplary embodiment of the disclosure. As shown in FIG. 1, the communication device **5** is capable of serial communication

Claim 11	Disclosure
	with a counterpart communication device via a TX channel **7** and an RX channel **8**. Although FIG. 1 illustrates that the communication device **5** communicates with the counterpart communication device through a full duplex communication scheme, i.e., two channels (the TX and RX channels **7** and **8**), according to some embodiments, the communication device **5** may communicate with the counterpart communication device through a half duplex communication scheme, i.e., one channel. The TX channel **7** or the RX channel **8** may refer to interconnection between the communication device **5** and the counterpart communication device, and serial data signals DIF**1** and DIF**2** may transfer through the TX channel **7** and the RX channel **8**, respectively. For example, the TX channel **7** or the RX channel **8** may include at least one of a conductive line of an integrated circuit, a pattern of a printed circuit board (PCB), a connector, and a cable. The serial data signals DIF**1** and DIF**2**, which respectively pass through the TX channel **7** and the RX channel **8**, may be differential signals as shown in FIG. 1 in some embodiments, or may be single signals unlike what is illustrated in FIG. 1. The communication device **5** may refer to any device in serial communication with the counterpart communication device via the TX channel **7** and the RX channel **8**. In some embodiments, the communication device **5** may be a die included in a semiconductor package and may be in serial communication with a counterpart communication device included in the same semiconductor package. In some embodiments, the communication device **5** may be a semiconductor package mounted on a PCB and may be in serial communication with the counterpart communication device mounted on the same PCB or mounted on another PCB. In some embodiments, the communication device **5** may be a system (e.g., a storage, a computing system, etc.) including at least one semiconductor package and a PCB and may be in serial communication with other systems. As shown in FIG. 1, the communication device **5** may include a transmitter **10**, a receiver **20**, and a protocol processor **30**. In some embodiments, the transmitter **10** and the receiver **20** may be implemented as one block as a transceiver. The transmitter **10**, the receiver **20**, and the protocol processor **30** may provide a physical layer of communication and may be collectively referred to as a SerDes (serializer/deserializer) for serial communication." Kang, 3:17-65.

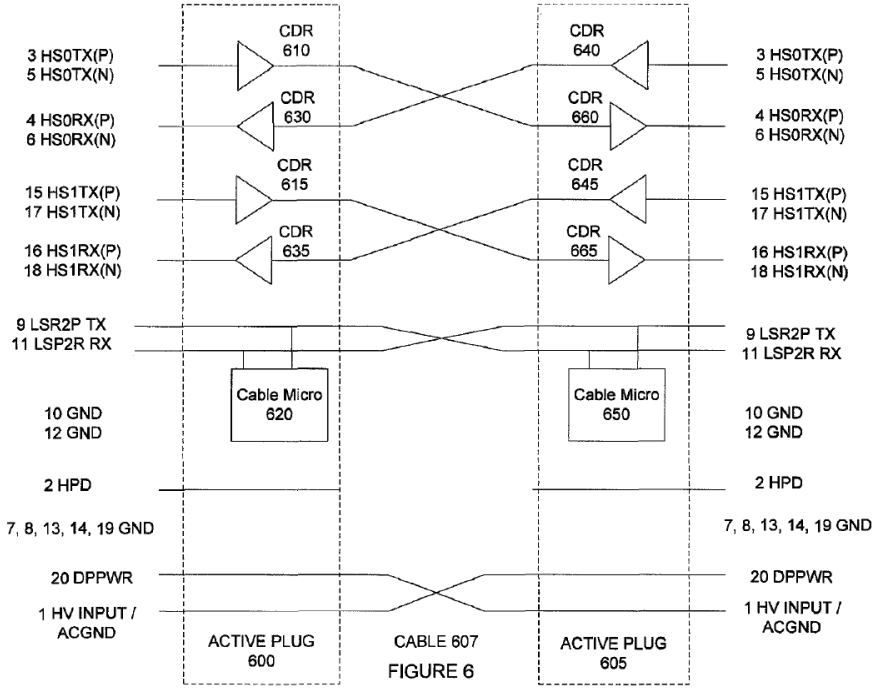
Claim 11	Disclosure
	FIG. 1  Kang, FIG. 1

Claim 11	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 11	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

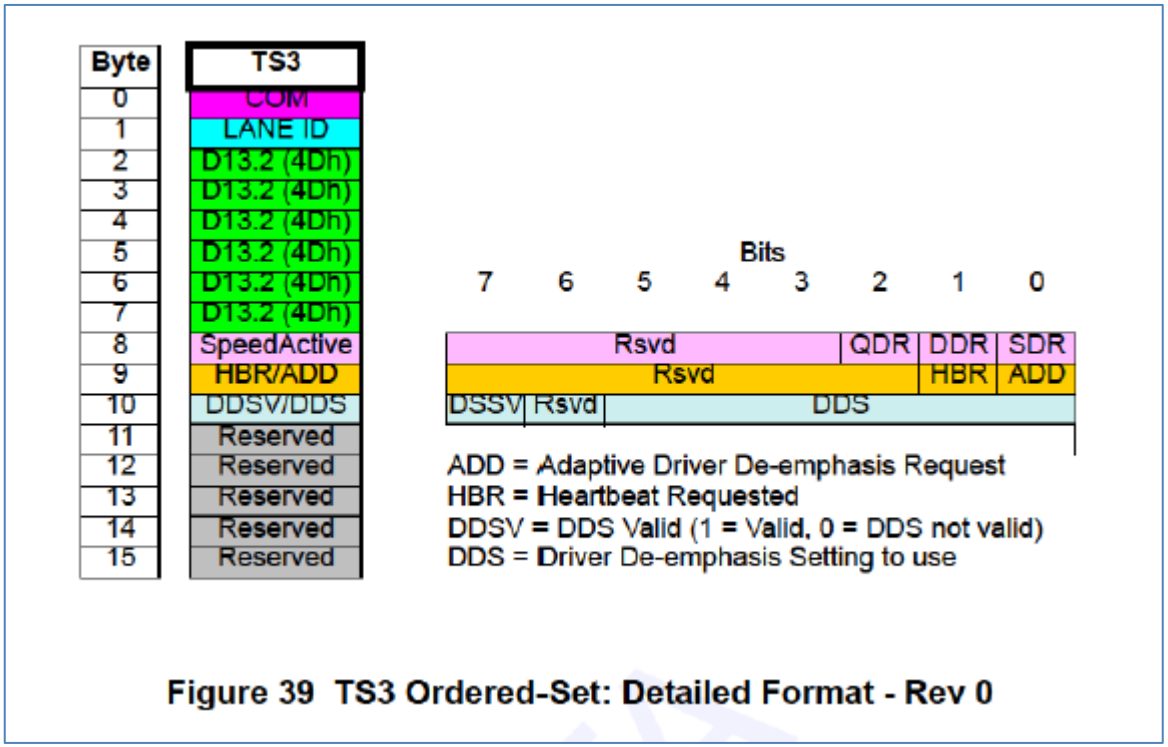
Claim 11	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 11	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 11	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 11	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 11	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 11	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

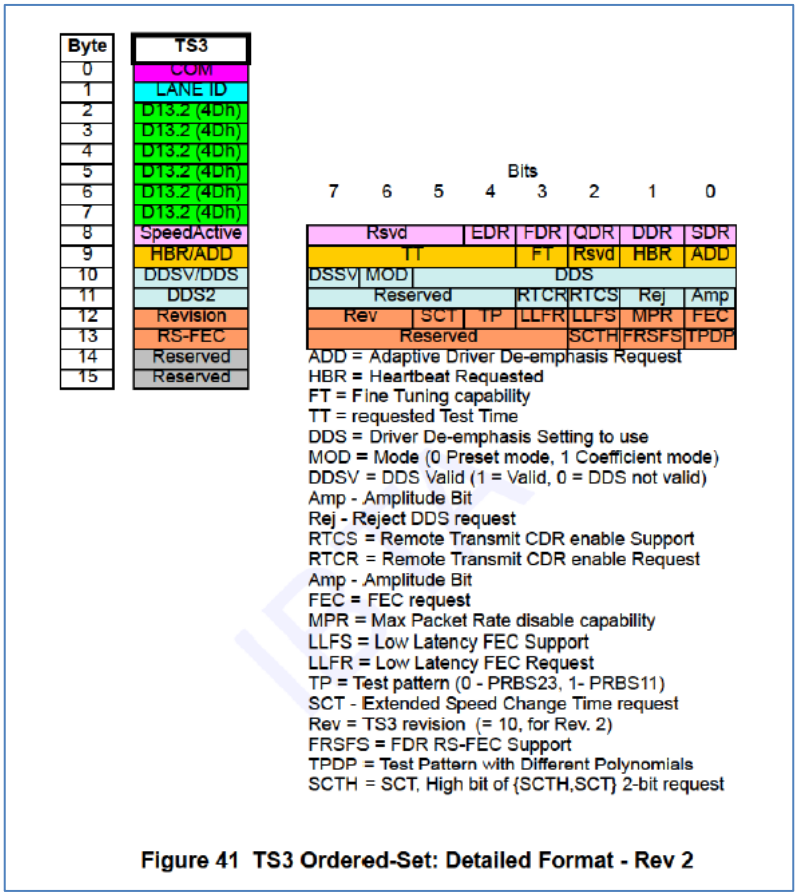
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 11	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 11	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 11	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 11	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 11	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 11	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 11	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 11	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

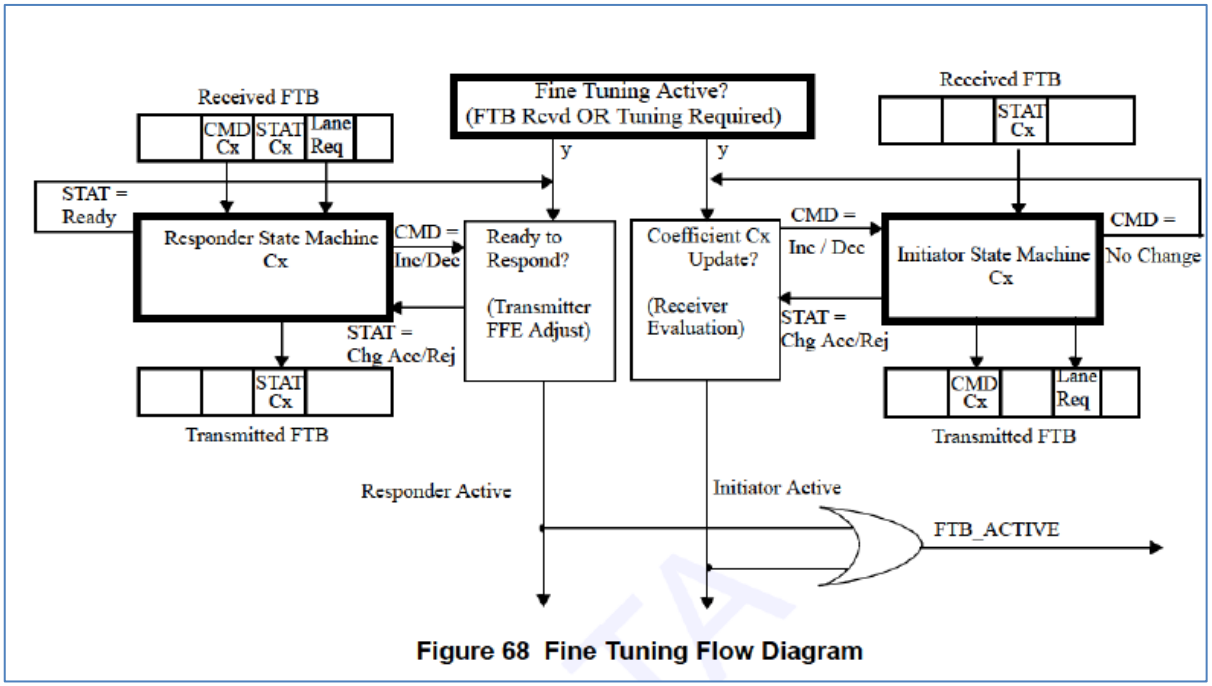
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 11	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 11	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 11	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 11	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 11	Disclosure
	Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 11	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

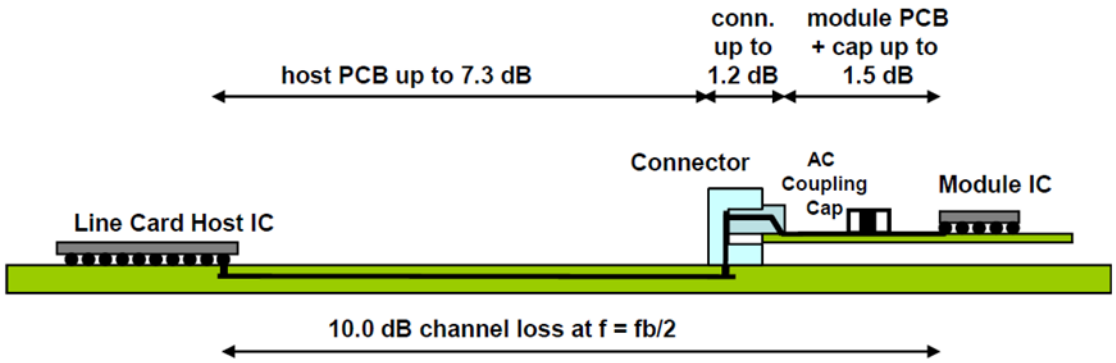
Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"To provide a high-performance radio link for high-speed systems employing spectrally-efficient modulation schemes, a reliable and robust transmitter radio link is required. Present embodiments of the current invention perform signal processing techniques to enhance the system performance and robustness of the transmitter portion of the transceiver."

Rafie, paragraph 47.

"Various embodiments are directed toward a communication device that includes a transceiver circuit that is configured to communicate by generating an RF carrier signal of around 13.56 MHz as consistent with various RFID technologies, such as ISO/IEC standard 14443."

Claim 11	Disclosure
	Ciacci, 3:63-67. *United States Patent No. 7,239,665 ("Mezer")* Mezer describes supporting Ethernet, and such standards-compliant implementation was conventional. *See, e.g.*, at Mezer, 4:55-57, 6:62-7:3. This obvious implementation would have met the Ethernet standard's description of a chip-to-module communication link comprising a port connector coupling a port transceiver to a pluggable module transceiver. *See, e.g.*, IEEE 802.3bs-2017, 323-330 (Annex 120C), 350-372 (Annex 120E), 350 ("The chip-to-module interface is defined using a specification… that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0"); *see also* OIF-CEI-04.0, 334, Fig. 16-15 (below, showing a "Connector" receiving a pluggable module). **Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model** 

PCIe 3.1a

1.3. PCI Express Fabric Topology

A fabric is composed of point-to-point Links that interconnect a set of components – an example fabric topology is shown in Figure 1-2. This figure illustrates a single fabric instance referred to as a hierarchy – composed of a Root Complex (RC), multiple Endpoints (I/O devices), a Switch, and a PCI Express to PCI/PCI-X Bridge, all interconnected via PCI Express Links.

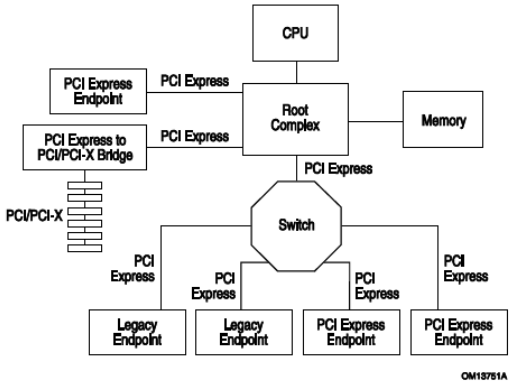


Figure 1-2: Example Topology

1.3.1. Root Complex

- A Root Complex (RC) denotes the root of an I/O hierarchy that connects the CPU/memory subsystem to the I/O.
- As illustrated in Figure 1-2, a Root Complex may support one or more PCI Express Ports. Each interface defines a separate hierarchy domain. Each hierarchy domain may be composed of a single Endpoint or a sub-hierarchy containing one or more Switch components and Endpoints.
- The capability to route peer-to-peer transactions between hierarchy domains through a Root Complex is optional and implementation dependent. For example, an implementation may incorporate a real or virtual Switch internally within the Root Complex to enable full peer-to-peer support in a software transparent way.

  Unlike the rules for a Switch, a Root Complex is generally permitted to split a packet into smaller packets when routing transactions peer-to-peer between hierarchy domains (except as noted below), e.g., split a single packet with a 256-byte payload into two packets of 128 bytes payload each. The resulting packets are subject to the normal packet formation rules contained in this specification (e.g., Max_Payload_Size, Read Completion Boundary, etc.). Component designers should note that splitting a packet into smaller packets may have negative performance

Claim 11	Disclosure
	consequences, especially for a transaction addressing a device behind a PCI Express to PCI/PCI-X bridge. Exception: A Root Complex that supports peer-to-peer routing of Vendor_Defined Messages is not permitted to split a Vendor_Defined Message packet into smaller packets except at 128-byte boundaries (i.e., all resulting packets except the last must be an integral multiple of 128 bytes in length) in order to retain the ability to forward the Message across a PCI Express to PCI/PCI-X Bridge. Refer to the *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0* for additional information. ❑ A Root Complex must support generation of configuration requests as a Requester. ❑ A Root Complex is permitted to support the generation of I/O Requests as a Requester. o A Root Complex is permitted to generate I/O Requests to either or both of locations 80h and 84h to a selected Root Port, without regard to that Root Port's PCI Bridge I/O decode configuration; it is recommended that this mechanism only be enabled when specifically needed. ❑ A Root Complex must not support Lock semantics as a Completer. ❑ A Root Complex is permitted to support generation of Locked Requests as a Requester. PCIe 3.1 at 50-51.

Claim 11	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 11	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 11	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

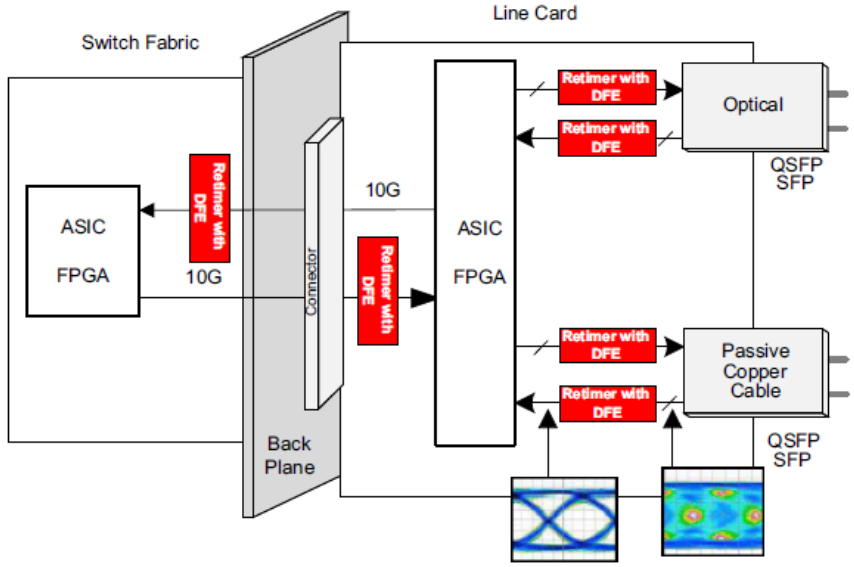
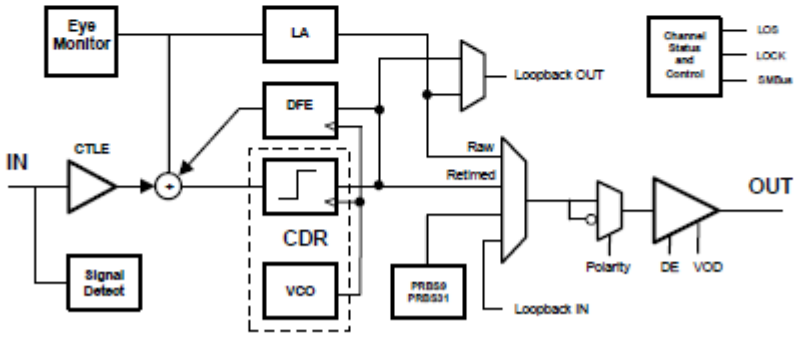


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 11	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 11	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 11	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

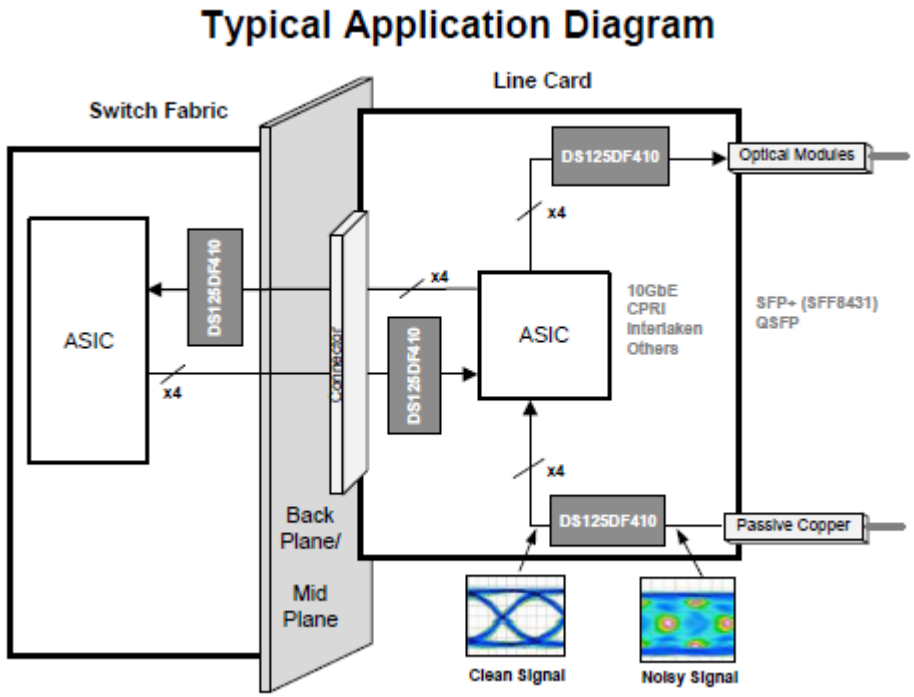
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

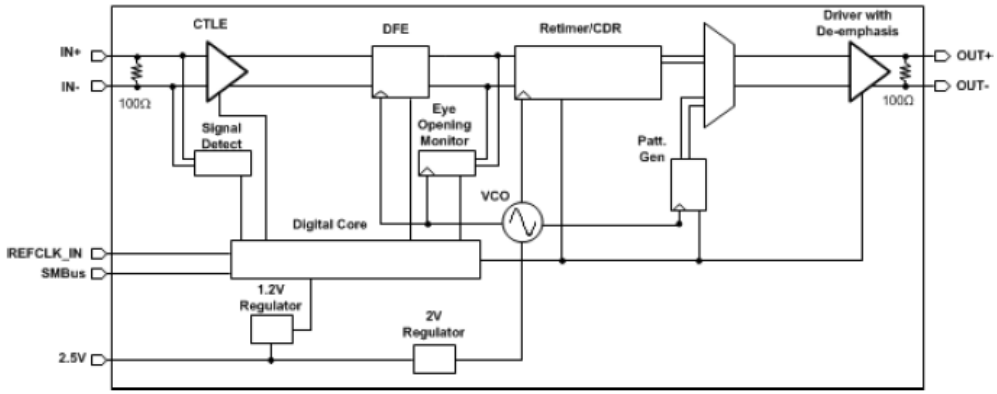
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 11	Disclosure
	 TI DS125DF410, 1.

Claim 11	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 11	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 11	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 11	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 11	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 11	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

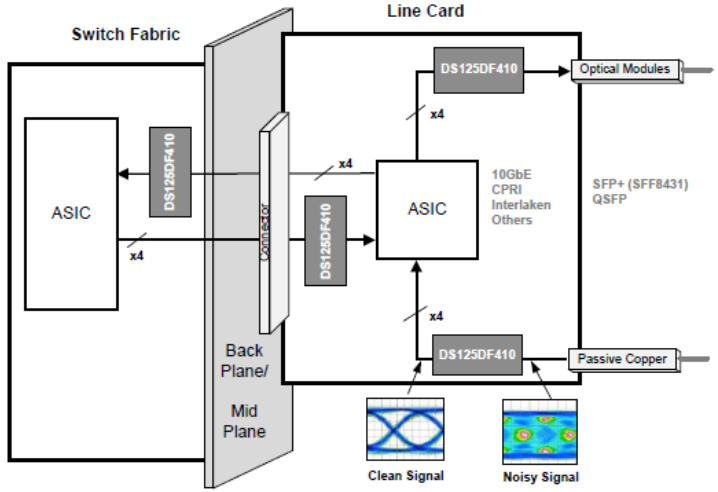
TI DS125DF410, 41.

Claim 11	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 11	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 11	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

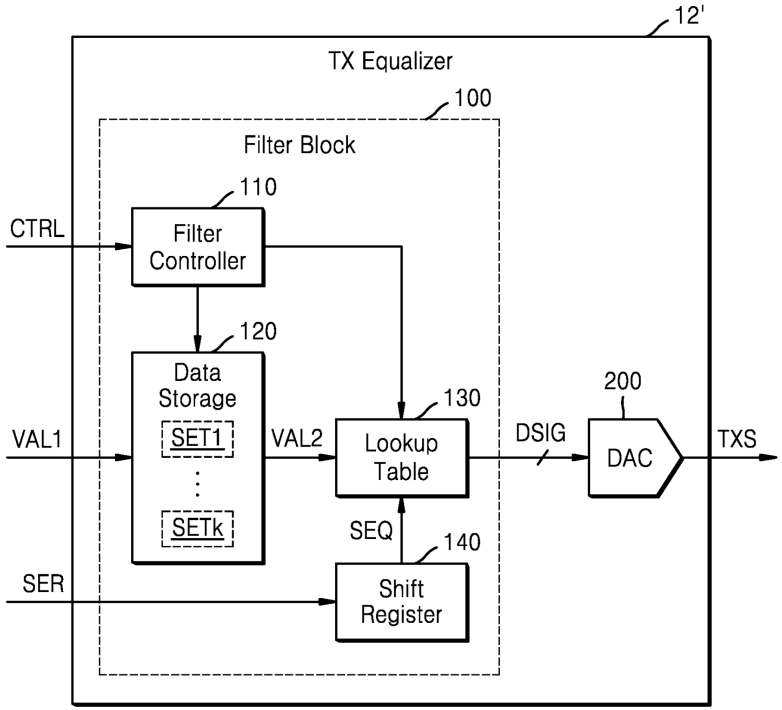
Claim 11	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Claim 11	Disclosure
11[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**." Kang, 5:20-42.

Claim 11	Disclosure
	"FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS, which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3.

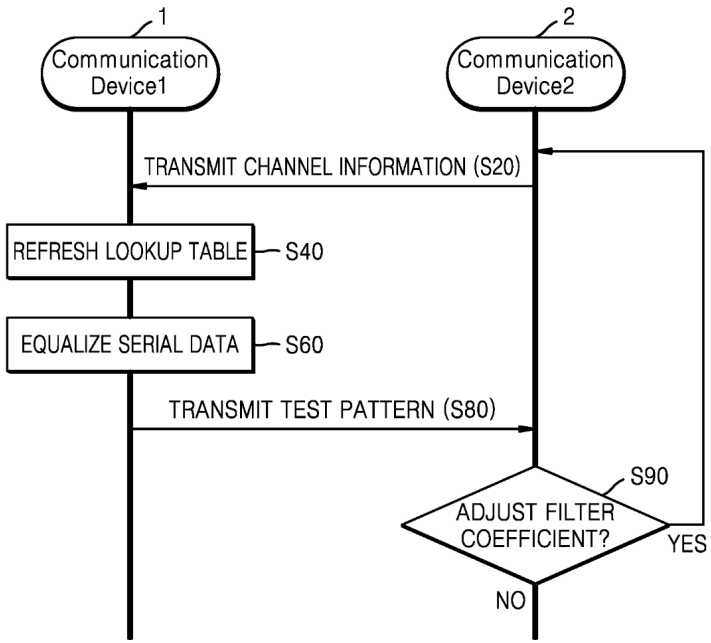
Claim 11	Disclosure
	The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively.

Claim 11	Disclosure
	The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

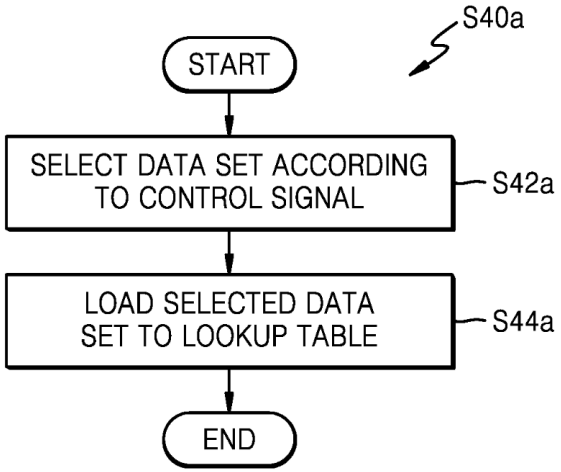
Claim 11	Disclosure
	FIG. 3  Kang, FIG. 3 "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the

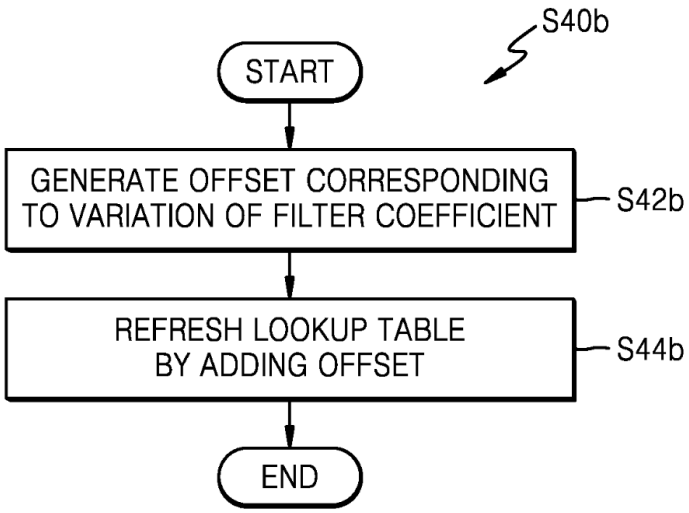
Claim 11	Disclosure
	equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "FIG. 10 is a diagram illustrating an equalization method over time according to an exemplary embodiment of the disclosure. For example, the equalization method of FIG. 10 may be performed by the first communication device 1 including the TX equalizer 12 of FIG. 1 and the second communication device 2 communicating with the first communication device 1. The filter coefficients for equalization may be determined according to the equalization method illustrated in FIG. 10, and the method for determining the filter coefficients may be referred to as training of filter coefficients. It is assumed below that the first communication device 1 of FIG. 10 includes the components of the communication device 5 of FIG. 1, and FIG. 10 will be described with reference to FIG. 1. Referring to FIG. 10, in operation S20, the second communication device 2 may transmit channel information. For example, the second communication device 2 may first transmit, to the first communication device 1, channel information including information indicating one of the plurality of data sets, as described above with reference to FIG. 3. In operation S40, the first communication device 1 may refresh the lookup table LUT. For example, the protocol processor 30 of the first communication device 1 may extract information indicating a data set from the channel information received in operation S20 and may transmit the control signal CTRL including the extracted information to the TX equalizer 12. TX equalizer 12 may refresh the lookup table LUT based on the control signal CTRL. The lookup table LUT may include values of the digital signal DSIG corresponding to possible values of the symbol sequence extracted from the serial data SER. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information indicating a data set will be described with reference to FIG. 11. In operation S60, the first communication device 1 may equalize the serial data SER. For example, in the TX equalizer 12 of the first communication device 1, the lookup table LUT may output a digital signal (e.g., DSIG in FIG. 3) corresponding to the symbol sequence of the serial data SER, and the DAC 200 included in the TX equalizer 12 may convert the digital signal into an analog signal. Accordingly, an adder and a multiplier for multiplication and addition between the symbol sequence and the filter coefficient

Claim 11	Disclosure
	sequence for implementing the FIR filter 9 of FIG. 2 may be omitted. The example of operation S60 will be described with reference to FIG. 14. In operation S80, the first communication device 1 may transmit a test pattern. For example, the test pattern may include a pattern previously shared by the first communication device 1 and the second communication device 2, and the second communication device 2 may receive the test pattern through a channel (e.g., 7 of FIG. 1). In operation S90, the second communication device 2 may determine whether to adjust the filter coefficient. For example, the second communication device 2 may evaluate the test pattern received from the first communication device 1 and determine whether to adjust at least one of the coefficients of the FIR filter used for equalization of the first communication device 1 according to the evaluation result. As illustrated in FIG. 10, when it is determined not to adjust at least one of the filter coefficients, the training of the filter coefficients may be terminated and the first communication device 1 may transmit the signal, which is equalized according to the current filter coefficients, to the second communication device 2. On the other hand, when it is determined to adjust at least one of the filter coefficients, operation S20 may be performed. Unlike the initially performed operation S20, in operation S20, which is performed after operation S90, the second communication device 2 may transmit channel information, which includes information on the variation of the filter coefficients, to the first communication device 1. Thereafter, unlike the initially performed operation S40, in operation S40, the first communication device 1 may refresh the lookup table LUT based on the information on the variation of the filter coefficients. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information on the variation of the filter coefficients will be described with reference to FIG. 12." Kang, 11:62-13:6

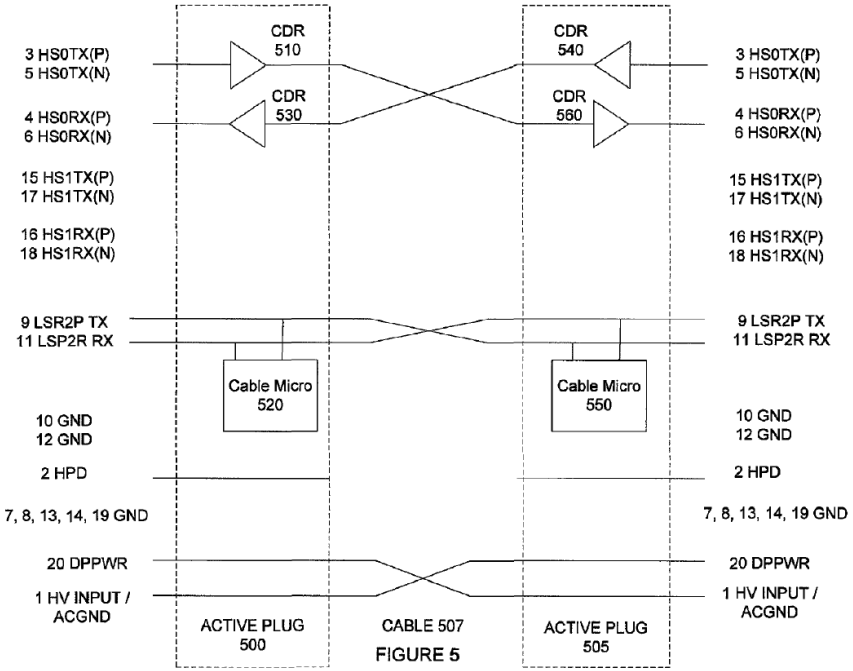
Claim 11	Disclosure
	FIG. 10  Kang, FIG. 10 "Referring to FIG. 11, operation S**40** *a* may include operations S**42** *a* and S**44** *a*. In operation S**42** *a*, an operation of selecting a data set according to the control signal CTRL may be performed. For example, the controller **110** of FIG. 3 may receive a control signal CTRL including information indicating one of k filter coefficient sequences and may control the data storage **120** to output one of first to k-th data sets SET**1** to SETk, which are stored in the data storage **120**, according to the control signal CTRL. In operation S**44** *a*, an operation of loading the selected data set into the lookup table **130** may be performed. For example, the controller **110** may control the data storage **120** and the lookup table **130** to store the second value VAL**2** outputted from the data storage **120** in the lookup table **130**.

Claim 11	Disclosure
	Referring to FIG. 12, operation S**40** *b* may include operations S**42** *b* and S**44** *b*. In operation S**42** *b*, an operation of generating an offset OFF corresponding to the variation of the filter coefficients may be performed. For example, the offset generator **150** of FIG. 6 may generate an offset OFF, based on the variation signal VAR and the index IDX provided from the controller **110′**. The variation signal VAR may indicate at least one of up, down, hold, and reset of the filter coefficient and may include a variation amount of the filter coefficient. An example of generating the offset OFF when the variation signal VAR indicates the reset of the filter coefficient will be described later with reference to FIG. 13. In operation S**44** *b*, an operation of refreshing the lookup table **130′** may be performed by adding the offset OFF. In some embodiments, the offset generator **150** may generate a positive offset OFF or a negative offset OFF, and thus the calculator **160** may perform an addition. In some embodiments, the offset generator **150** may generate the positive offset OFF, and thus the calculator **160** may perform addition or subtraction according to the control of the controller **110′**. The lookup table **130′** may be refreshed by storing the output value of the calculator **160**, that is, the third value VAL**3**, in the lookup table **130′**." Kang, 13:18-54

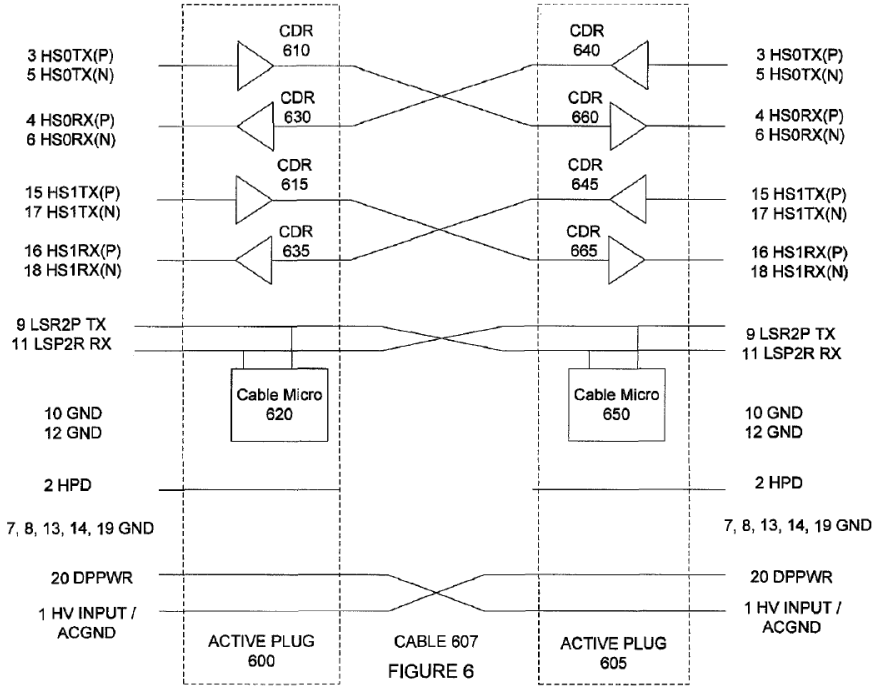
Claim 11	Disclosure
	FIG. 11  Kang, FIG. 11

Claim 11	Disclosure
	FIG. 12  Kang, FIG. 12 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**. Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**.

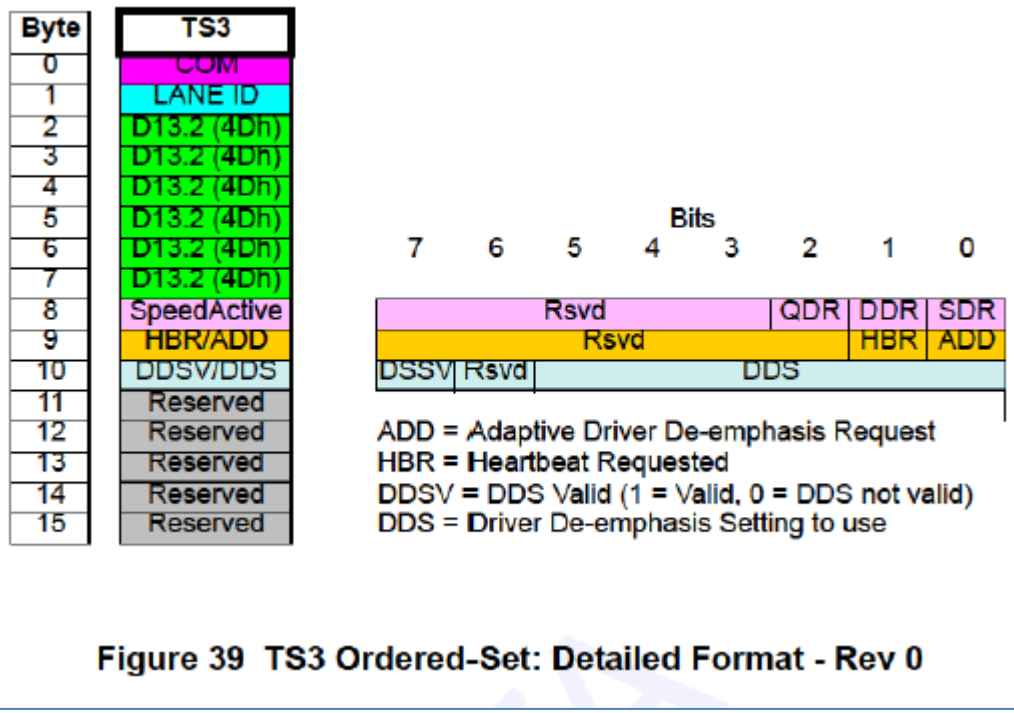
Claim 11	Disclosure
	The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables. In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used.

Claim 11	Disclosure
	In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5 "FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock

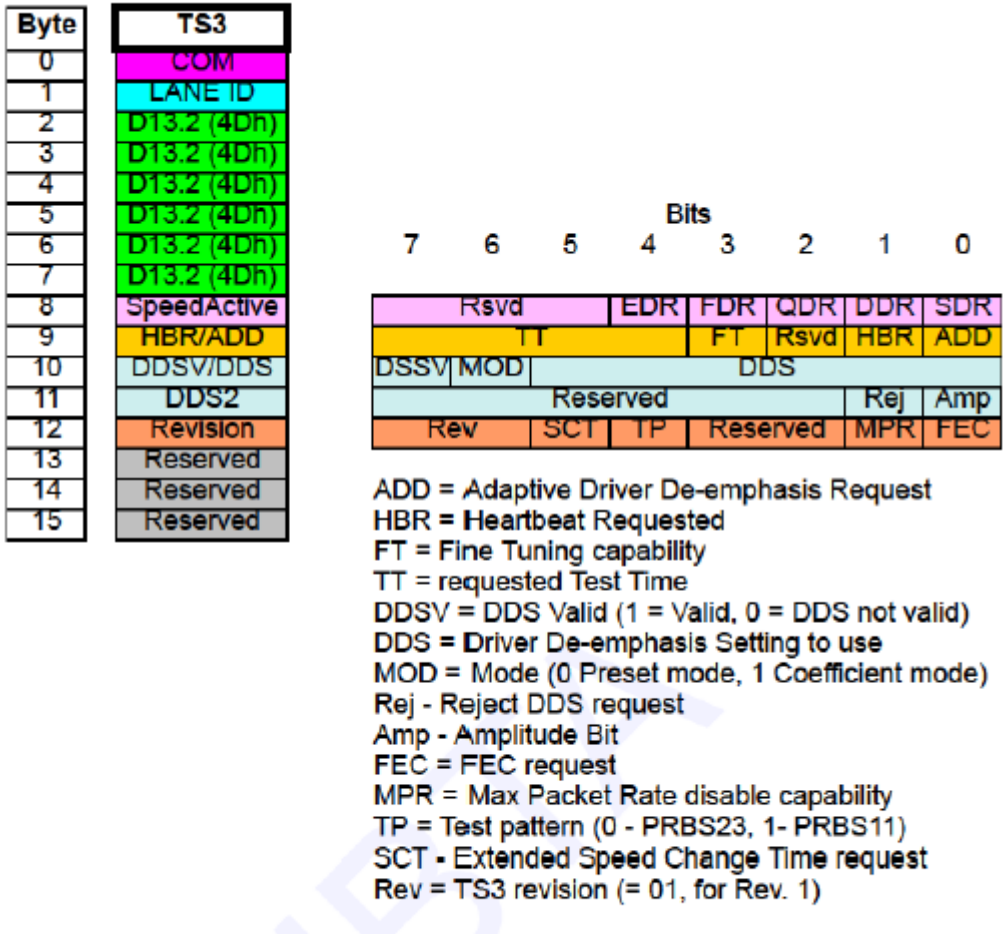
Claim 11	Disclosure
	and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 11	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 11	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 11	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 11	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

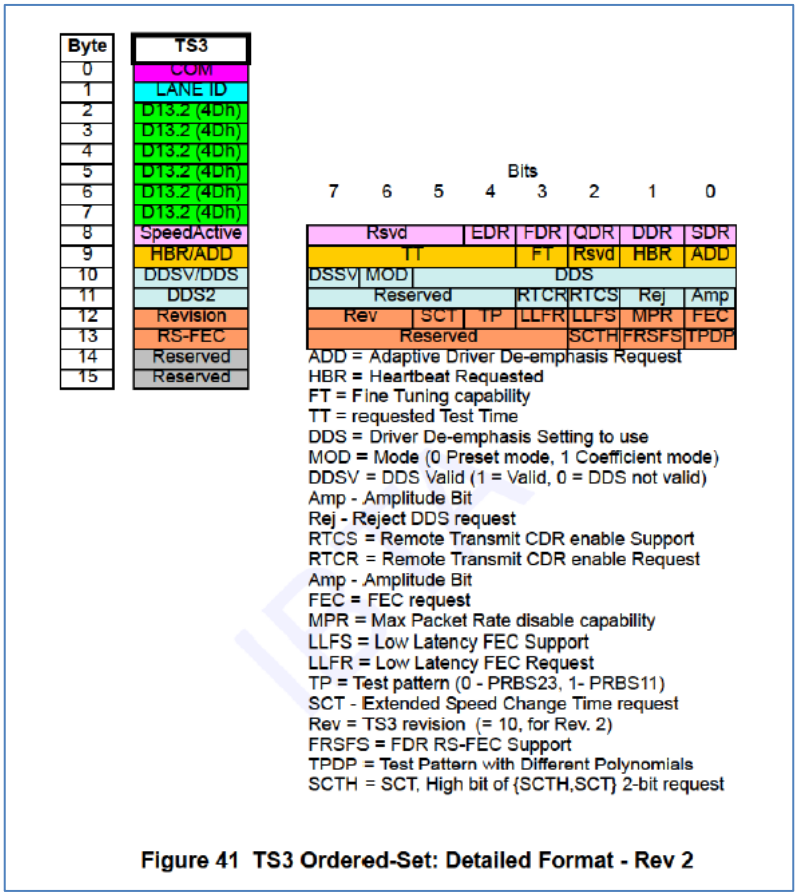
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 11	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 11	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 11	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 11	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 11	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 11	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 11	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 11	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

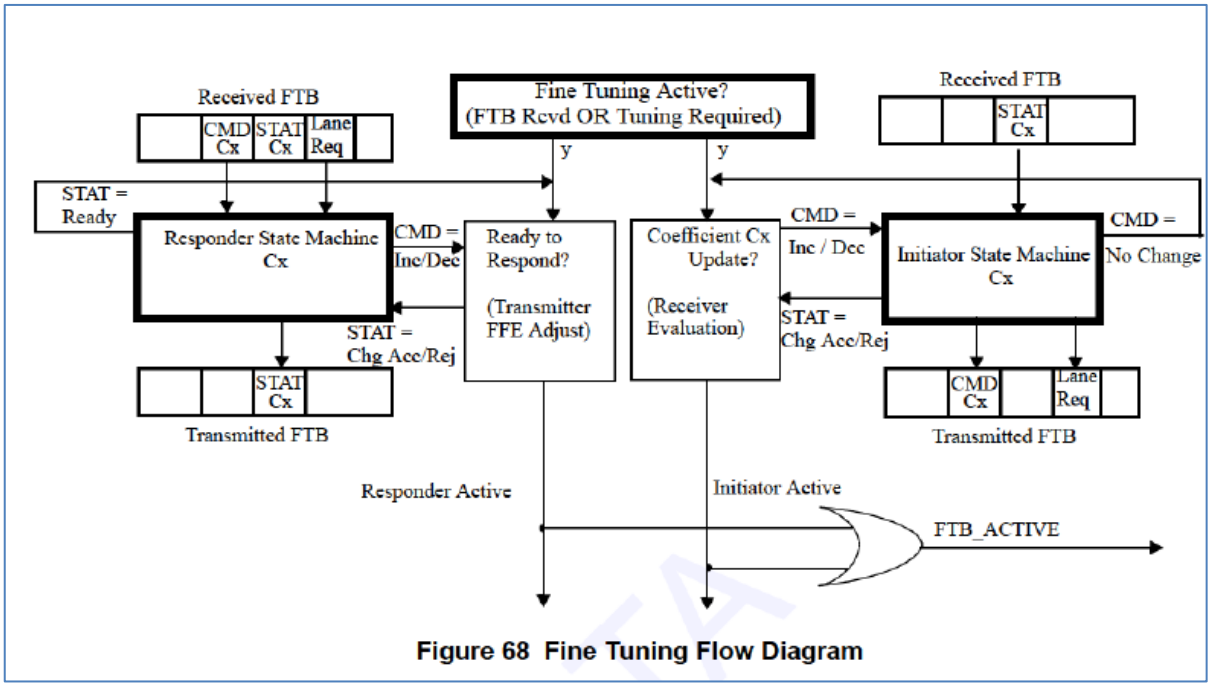
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 11	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 11	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 11	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 11	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 11	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 11	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

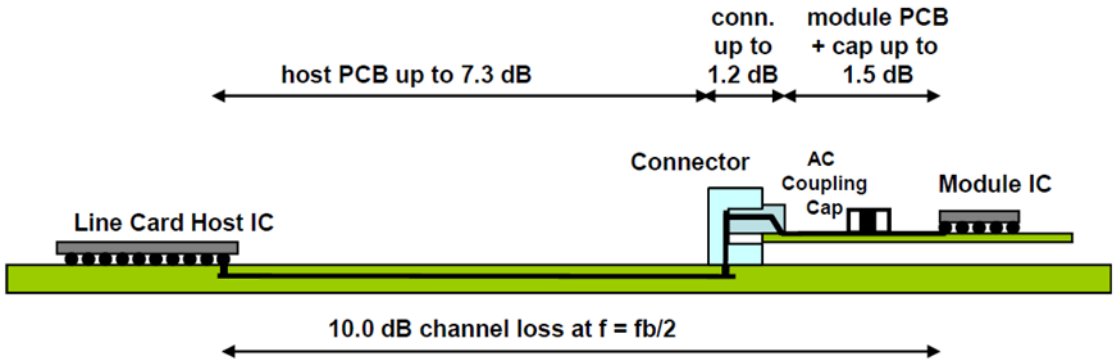
InfiniBand, Table 143 (p. 535)

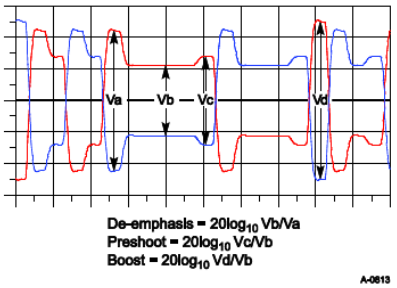
"The overall pre-equalizer 800 can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."

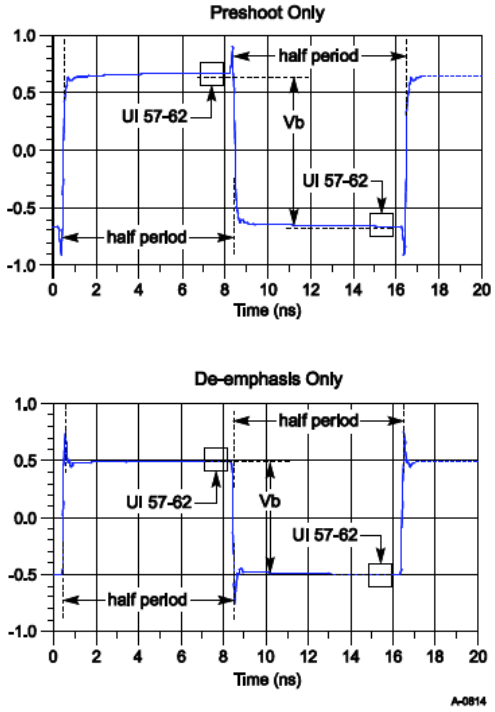
Rafie, paragraph 82.

"Digital pre-equalizer (PEQ) circuit 204 can be configured to introduce a distortion to the input signal to compensate for channel impairment. At power-on little or no information may be known about the channel. Accordingly, the digital PEQ circuit 204 can be initially configured with no distortion. In some

Claim 11	Disclosure
	embodiments, the digital PEQ circuit 204 can be initially configured with a distortion that is based upon a corresponding set of coefficients." Ciacci, 4:40-47. "The coefficients can then be used in combination with a pre-equalizer filter function of higher than first order." Ciacci, 8:2-4. *United States Patent No. 7,239,665 ("Mezer")* Mezer describes supporting Ethernet, and such standards-compliant implementation was conventional. *See, e.g.*, at Mezer, 4:55-57, 6:62-7:3. This obvious implementation would have met the Ethernet standard's description of a chip-to-module communication link comprising a port connector coupling a port transceiver to a pluggable module transceiver. *See, e.g.*, IEEE 802.3bs-2017, 323-330 (Annex 120C), 350-372 (Annex 120E), 350 ("The chip-to-module interface is defined using a specification… that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0"); *see also* OIF-CEI-04.0, 334, Fig. 16-15 (below, showing a "Connector" receiving a pluggable module).

Claim 11	Disclosure
	Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model  *PCIe 3.1a* **4.3.3.5.2. Tx Equalization Presets** An 8.0 GT/s transmitter must support a specified number of presets, where the preset values are defined in terms of voltage ratios as illustrated in Figure 4-42. Presets are defined in terms of two ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GTs/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. Figure 4-42 is shown as an example of TxEQ and is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of 8.0 GT/s signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms, as shown later in this section. The presets defined in Table 4-16 and Table 4-17 are numbered to match the designations in Section 4.2.3.1. Note, however, that in Section 4.2.3.1 the coefficients are defined as integers (using upper case "C"), while in the electrical section they are defined as floating point (using lower case "c"). PCIe 3.1a at 355.

Claim 11	Disclosure
	 **Figure 4-42: Definition of Tx Voltage Levels and Equalization Ratios** Figure 4-43 illustrates the waveforms that will be observed when measuring presets when using the 64-ones/64-zeroes sequence that is part of the compliance pattern. Depending on whether the preset implements de-emphasis, preshoot, or both the corresponding waveshape will differ. The two cases illustrated below show preshoot and de-emphasis, as can be observed by noting whether the boost occurs before or after each edge transition. For the case where both de-emphasis and preshoot are present, boost occurs both before and after each edge transition. Note that in all cases, however, the voltage of interest occurs during the flat portion (Vb) of the waveform, where it can be accurately measured independent of high frequency effects. PCIe 3.1a at 356.

Claim 11	Disclosure
	 **Figure 4-43: Waveform Measurement Points for Pre-shoot and De-emphasis** PCIe 3.1a at 357.

Claim 11	Disclosure

Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

Notes:

1. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The allowable P10 boost range is defined by the coefficient space lying between the Min and Max Reduced Swing Limits as shown by the two diagonal lines in the example of Figure 4-45. This approach permits both full and reduced swing transmitters to use P10 for testing to their respective boost limits.

With the exception of P4 (for which both pre-shoot and de-emphasis are 0.0 dB) it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are 1 UI wide and therefore subject to attenuation by the package and the breakout channel. Instead the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval. Table 4-17 lists the preset values required to measure each of the Va and Vc values from which the preshoot or de-emphasis values may be derived.

PCIe 3.1a at 358.

Claim 11	Disclosure
	Table 4-17: Preset Measurement Cross Reference Table PCIe 3.1a at 359.

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P4	N/A	N/A
P1	P1/P4	N/A
P0	P0/P4	N/A
P9	N/A	P4/P9
P8	P8/P6	P3/P8
P7	P7/P5	P2/P7
P5	N/A	P4/P5
P6	N/A	P4/P6
P3	P3/P4	N/A
P2	P2/P4	N/A
P10	P10/P4	N/A

Claim 11	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 11	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 11	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

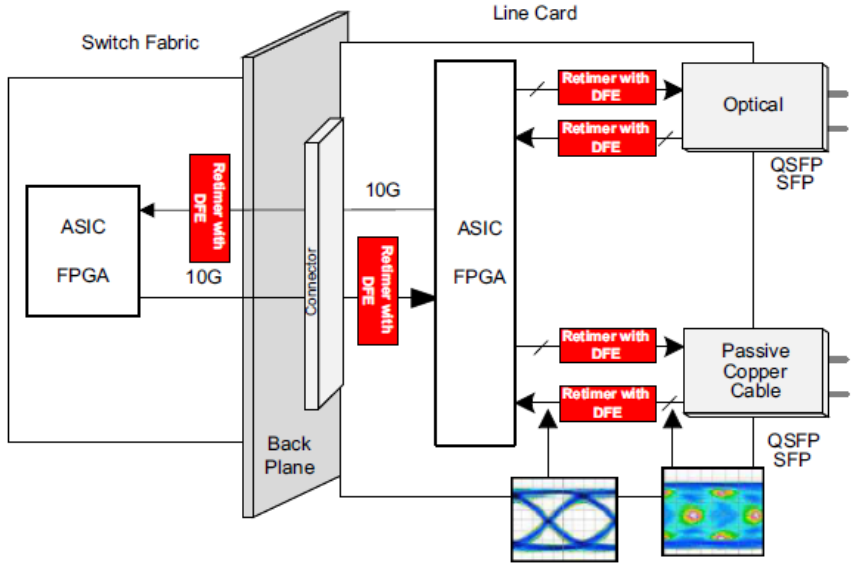
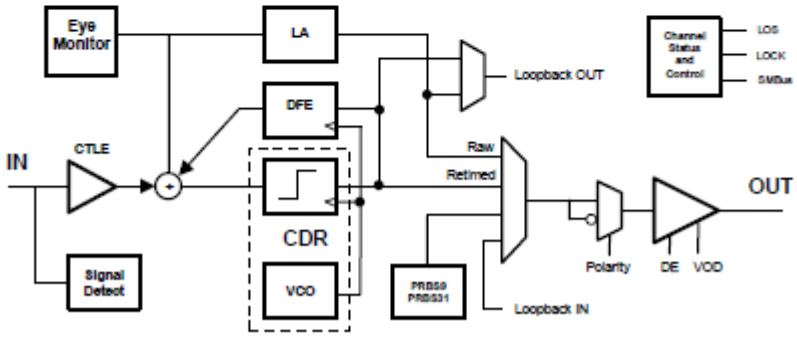


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 11	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 11	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 11	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

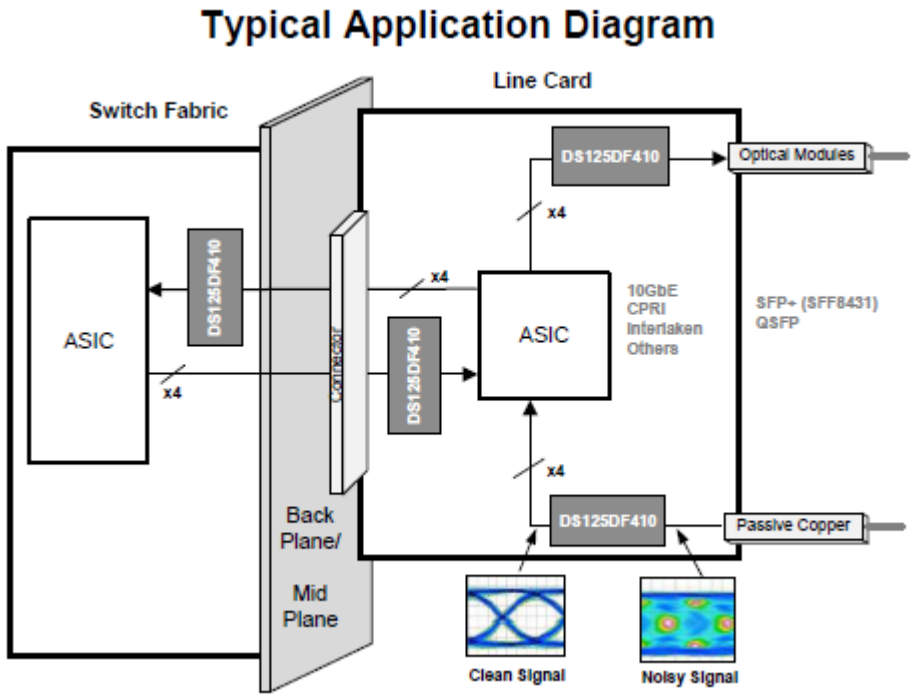
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

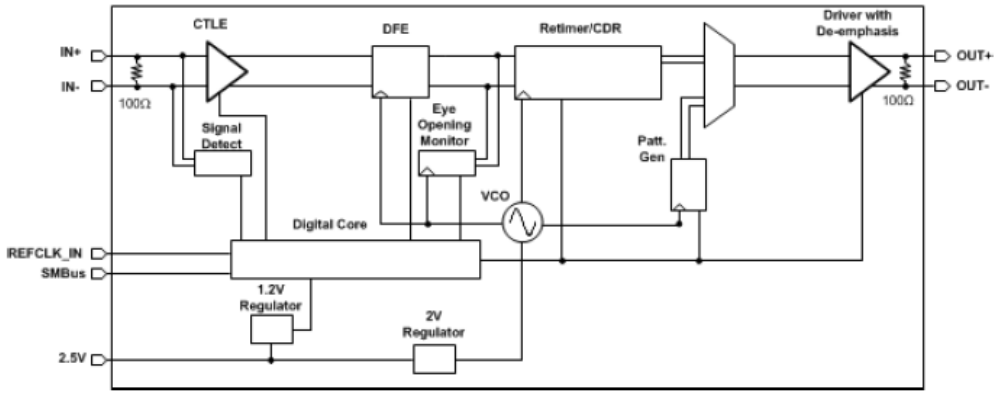
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 11	Disclosure
	 TI DS125DF410, 1.

Claim 11	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 11	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 11	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 11	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 11	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 11	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

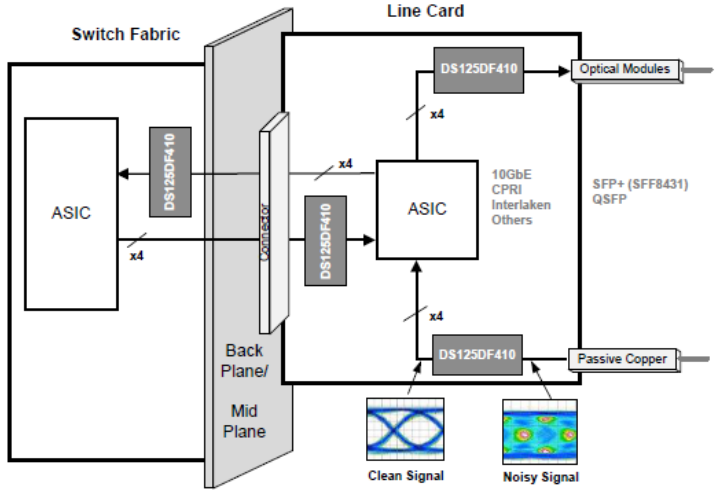
TI DS125DF410, 41.

Claim 11	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 11	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 11	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

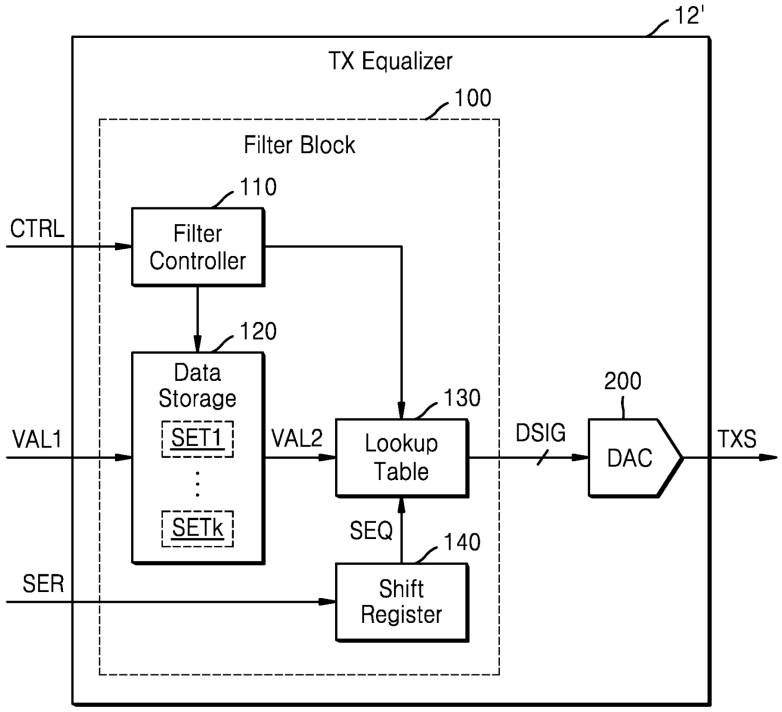
Claim 11	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Claim 11	Disclosure
11[b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic,	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**." Kang, 5:20-42.

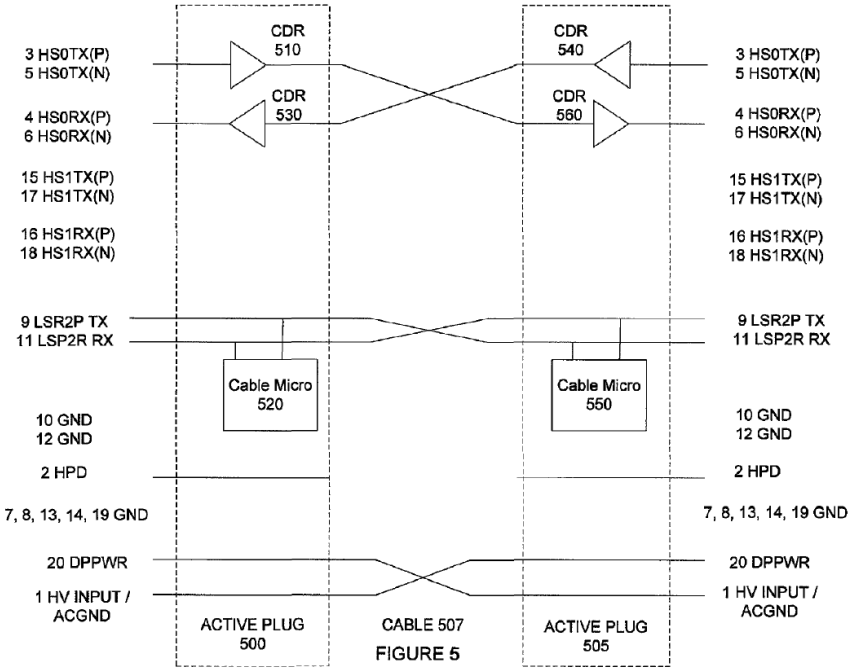
Claim 11	Disclosure
	"FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS, which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3.

Claim 11	Disclosure
	The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively.

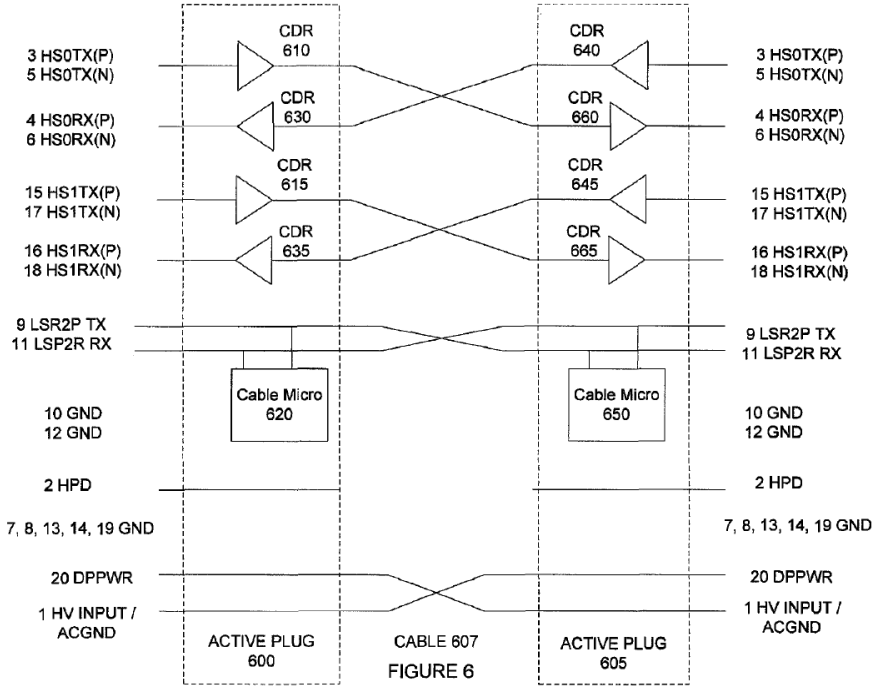
Claim 11	Disclosure
	The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 11	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 11	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

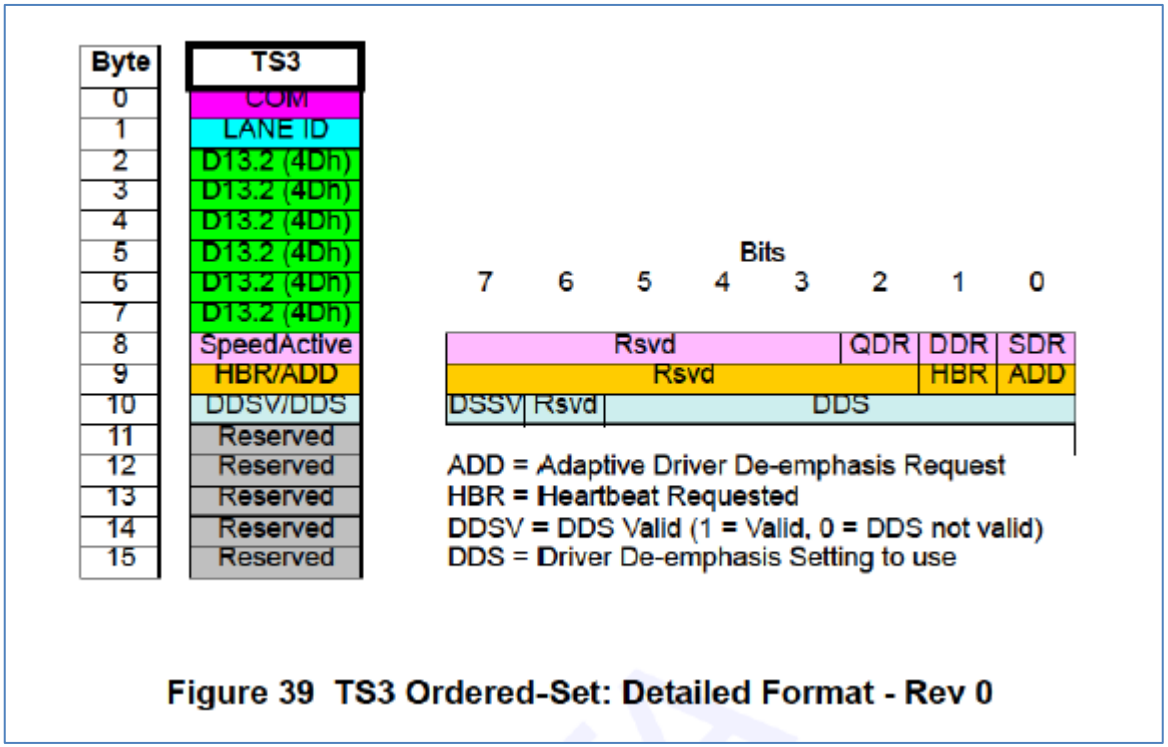
Claim 11	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 11	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 11	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 11	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 11	Disclosure

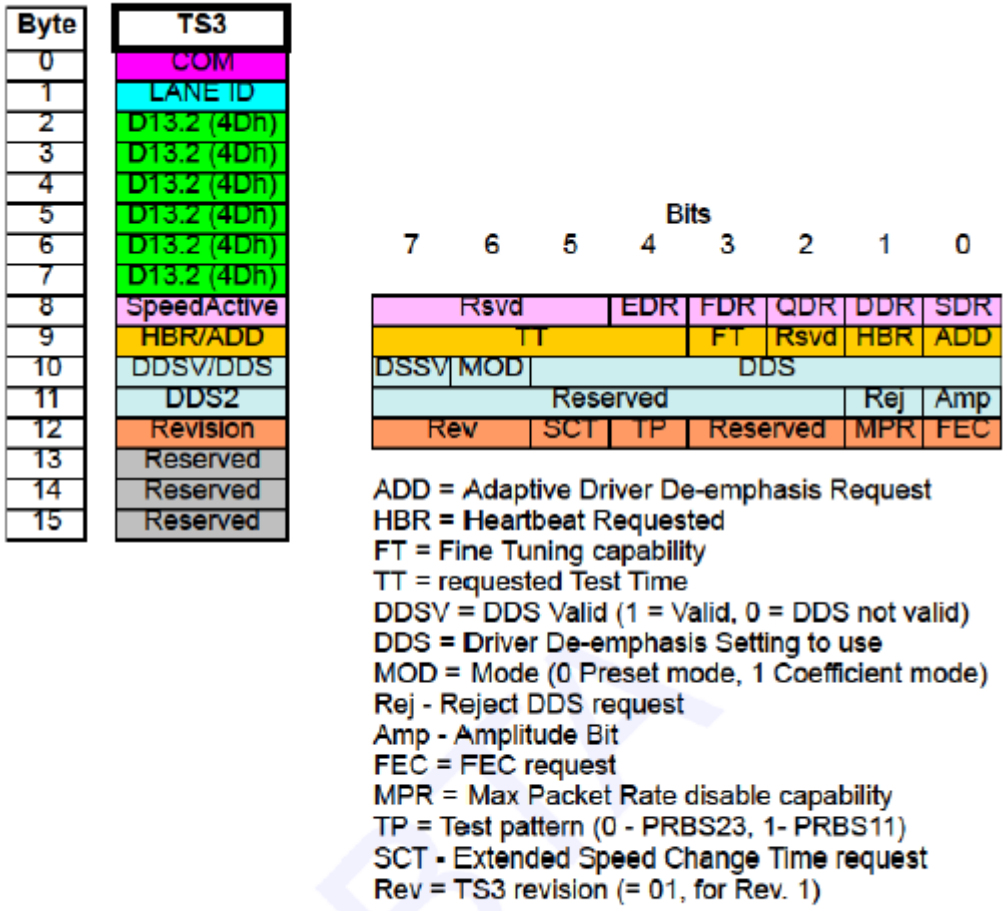


Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 11	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

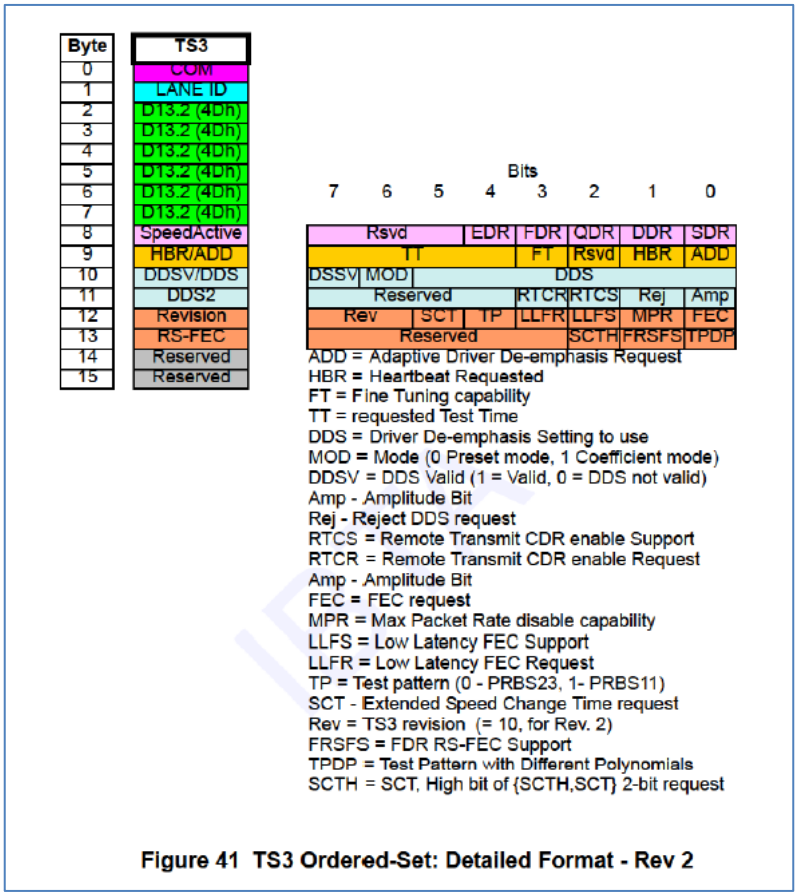
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 11	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 11	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 11	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 11	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 11	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 11	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 11	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 11	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

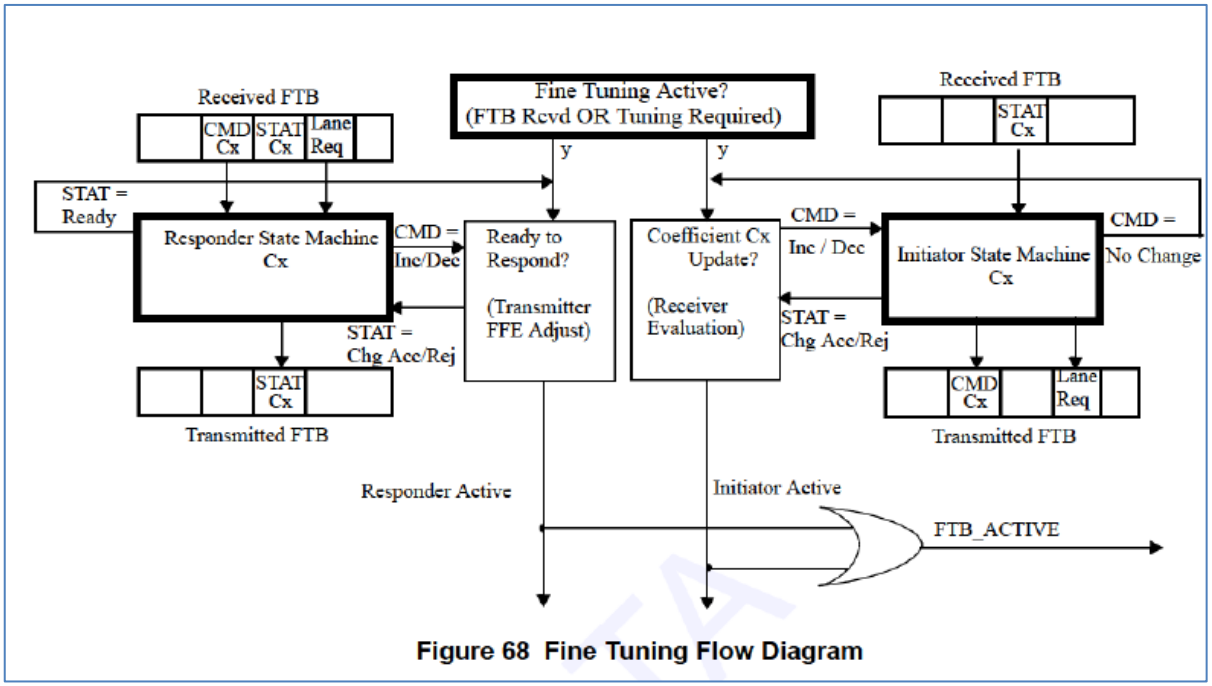
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 11	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 11	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 11	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 11	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 11	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 11	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

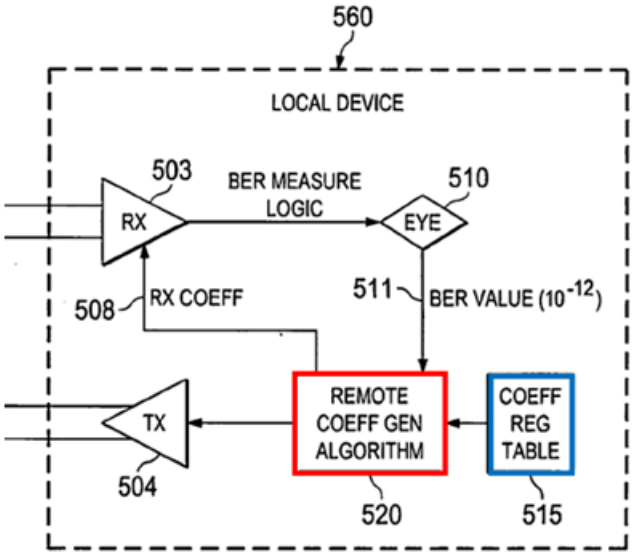
Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"The overall pre-equalizer **800** can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."
Rafie, paragraph 82.

"Digital pre-equalizer (PEQ) circuit **204** can be configured to introduce a distortion to the input signal to compensate for channel impairment. At power-on little or no information may be known about the channel. Accordingly, the digital PEQ circuit **204** can be initially configured with no distortion. In some

Claim 11	Disclosure
	embodiments, the digital PEQ circuit **204** can be initially configured with a distortion that is based upon a corresponding set of coefficients." Ciacci, 5:40-47. "Once frequency response of front-end components has been characterized, this information can be stored in the digital base band on a configuration register (CFR), and thereby used to specify gain coefficients of the digital pre-equalizer. Balakrishnan, paragraph 27. *U.S. Patent Publication No. 2014/0281067 ("Das Sharma")* Das Sharma discloses selecting initial coefficient values for transmit filters for use in an adaptive pre-equalization training process from among the registers. *See, e.g.*, Das Sharma at [0078], [0193], Figure 5. Das Sharma discloses a coefficient register table is used by a coefficient algorithm module that provides a set of initial coefficients to the transceiver's transmission logic. *See id*. at [0078]. Figure 5 of Das Sharma shows the coefficient algorithm module (red) and coefficient register table (blue). *See id*. at [0078] ("coefficient algorithm module 520"). Das Sharma teaches that the coefficient algorithm module can be implemented by a microcontroller that includes the coefficient register table. *See id*. at [0078], [0193] (Das Sharma's "modules" can each be implemented via a "microcontroller" including "registers").

Claim 11	Disclosure
	 FIG. 5

PCIe 3.1a

4.3.3.5.2. Tx Equalization Presets

An 8.0 GT/s transmitter must support a specified number of presets, where the preset values are defined in terms of voltage ratios as illustrated in Figure 4-42. Presets are defined in terms of two ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GTs/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. Figure 4-42 is shown as an example of TxEQ and is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of 8.0 GT/s signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms, as shown later in this section.

The presets defined in Table 4-16 and Table 4-17 are numbered to match the designations in Section 4.2.3.1. Note, however, that in Section 4.2.3.1 the coefficients are defined as integers (using upper case "C"), while in the electrical section they are defined as floating point (using lower case "c").

PCIe 3.1a at 355.

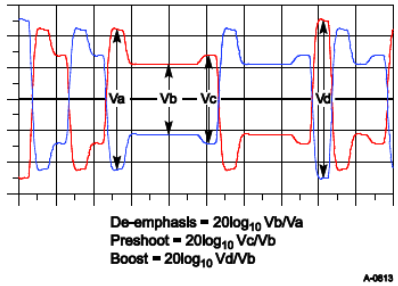
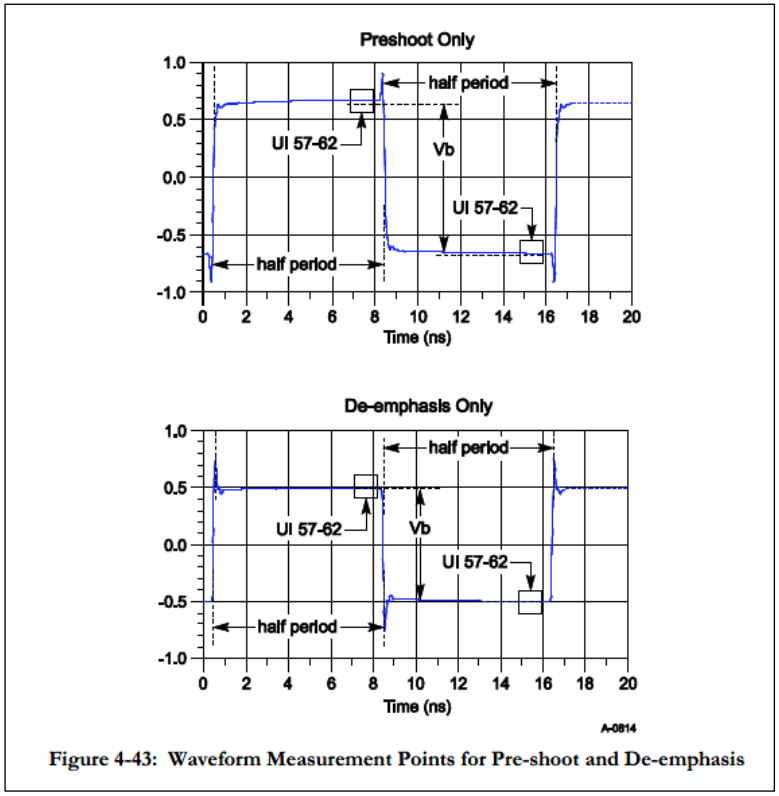


Figure 4-42: Definition of Tx Voltage Levels and Equalization Ratios

Figure 4-43 illustrates the waveforms that will be observed when measuring presets when using the 64-ones/64-zeroes sequence that is part of the compliance pattern. Depending on whether the preset implements de-emphasis, preshoot, or both the corresponding waveshape will differ. The two cases illustrated below show preshoot and de-emphasis, as can be observed by noting whether the boost occurs before or after each edge transition. For the case where both de-emphasis and preshoot are present, boost occurs both before and after each edge transition. Note that in all cases, however, the voltage of interest occurs during the flat portion (Vb) of the waveform, where it can be accurately measured independent of high frequency effects.

PCIe 3.1a at 356.

Claim 11	Disclosure
	 Figure 4-43: Waveform Measurement Points for Pre-shoot and De-emphasis PCIe 3.1a at 357.

Claim 11	Disclosure

Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

Notes:

1. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The allowable P10 boost range is defined by the coefficient space lying between the Min and Max Reduced Swing Limits as shown by the two diagonal lines in the example of Figure 4-45. This approach permits both full and reduced swing transmitters to use P10 for testing to their respective boost limits.

With the exception of P4 (for which both pre-shoot and de-emphasis are 0.0 dB) it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are 1 UI wide and therefore subject to attenuation by the package and the breakout channel. Instead the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval. Table 4-17 lists the preset values required to measure each of the Va and Vc values from which the preshoot or de-emphasis values may be derived.

PCIe 3.1a at 358.

Claim 11	Disclosure
	Table 4-17: Preset Measurement Cross Reference Table PCIe 3.1a at 359.

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P4	N/A	N/A
P1	P1/P4	N/A
P0	P0/P4	N/A
P9	N/A	P4/P9
P8	P8/P6	P3/P8
P7	P7/P5	P2/P7
P5	N/A	P4/P5
P6	N/A	P4/P6
P3	P3/P4	N/A
P2	P2/P4	N/A
P10	P10/P4	N/A

Claim 11	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 11	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 11	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

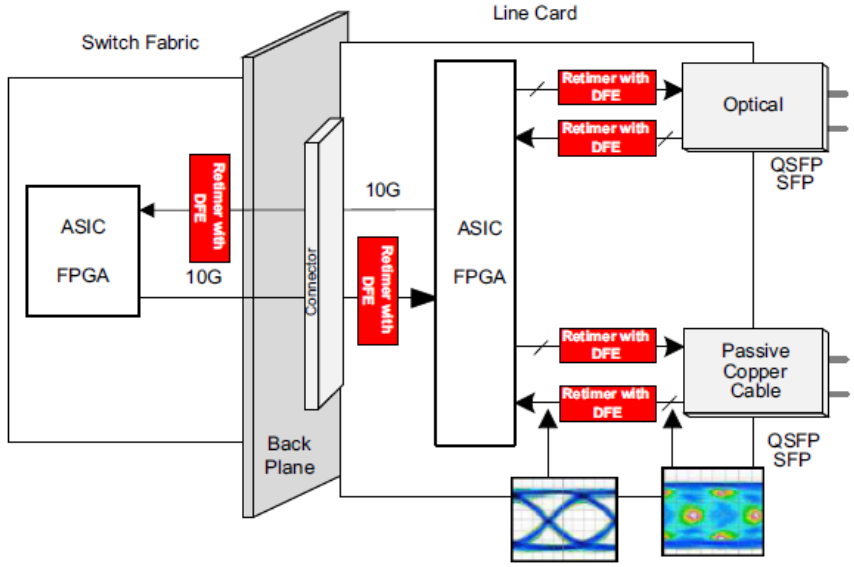
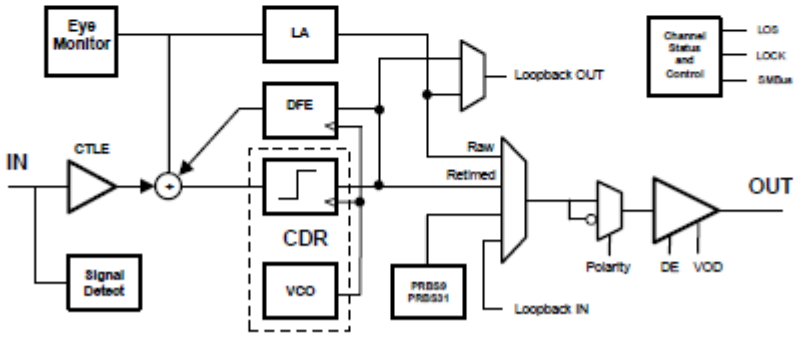


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 11	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 11	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 11	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

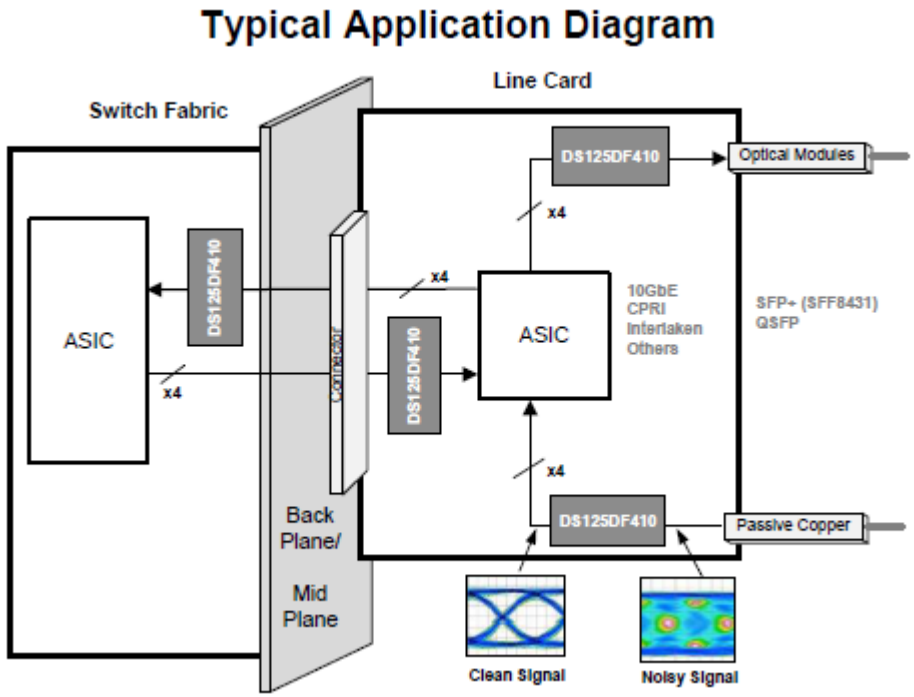
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

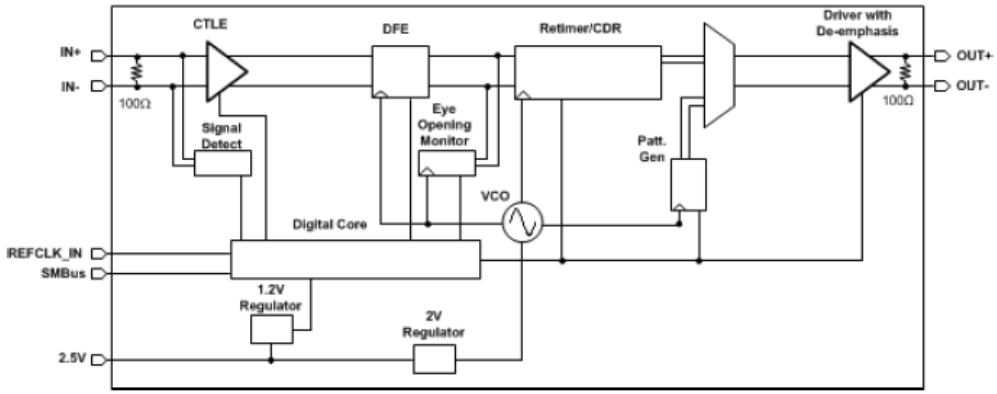
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 11	Disclosure
	 TI DS125DF410, 1.

Claim 11	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 11	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 11	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 11	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 11	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 11	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

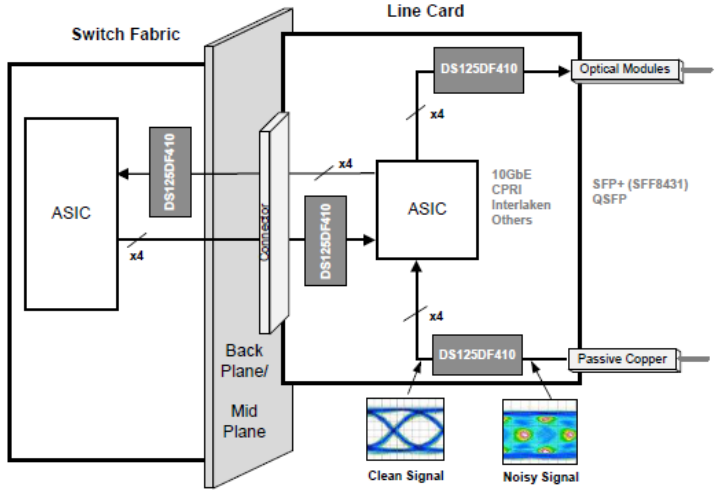
TI DS125DF410, 41.

Claim 11	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 11	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 11	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

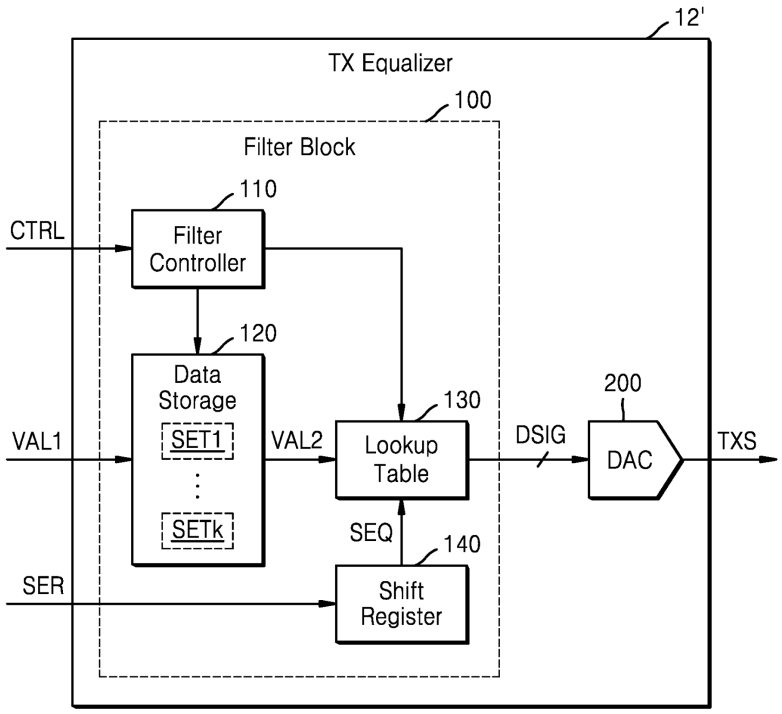
Claim 11	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Claim 11	Disclosure
11[c] the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**." Kang, 5:20-42.

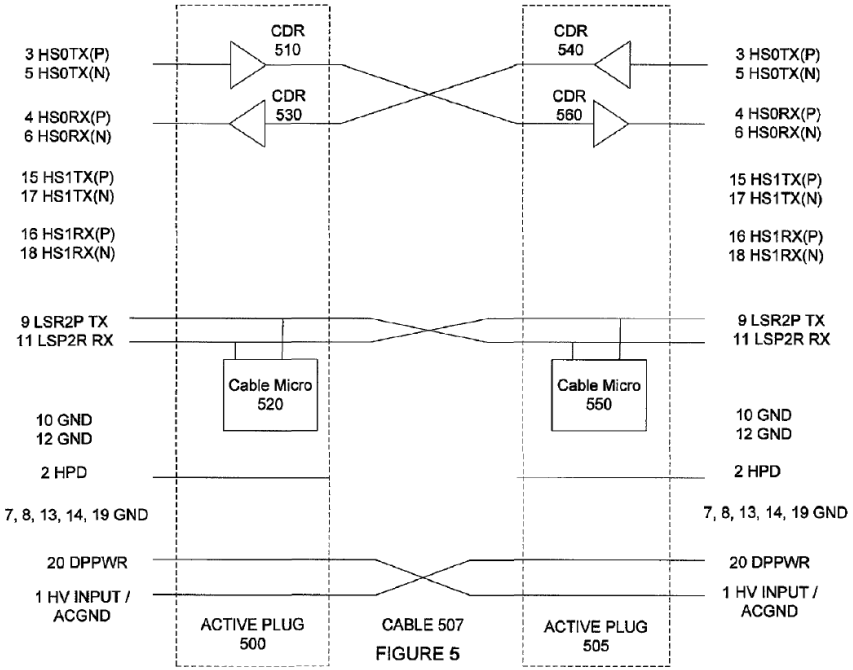
Claim 11	Disclosure
	"FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS, which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3.

Claim 11	Disclosure
	The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively.

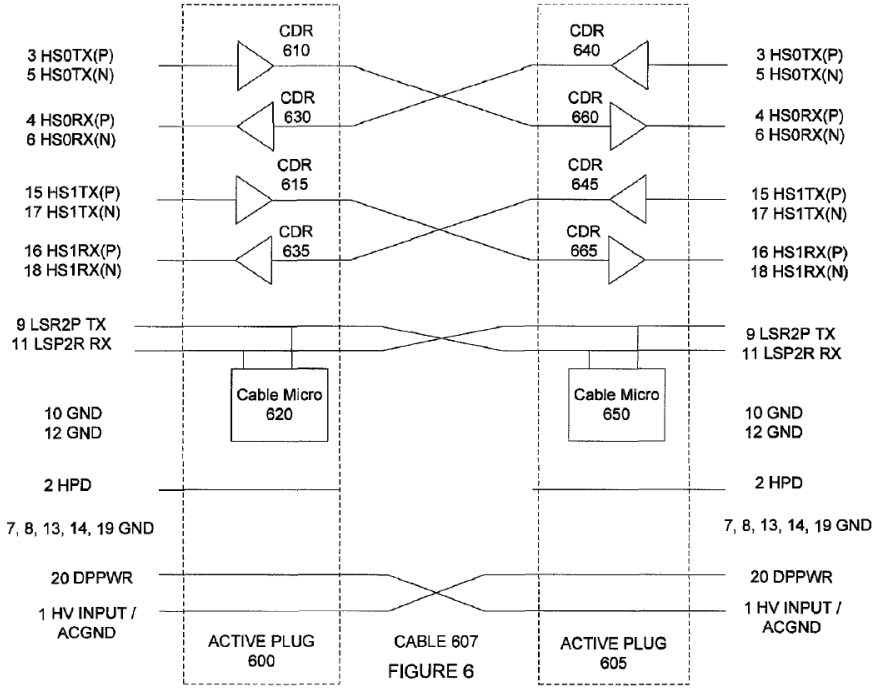
Claim 11	Disclosure
	The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 11	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

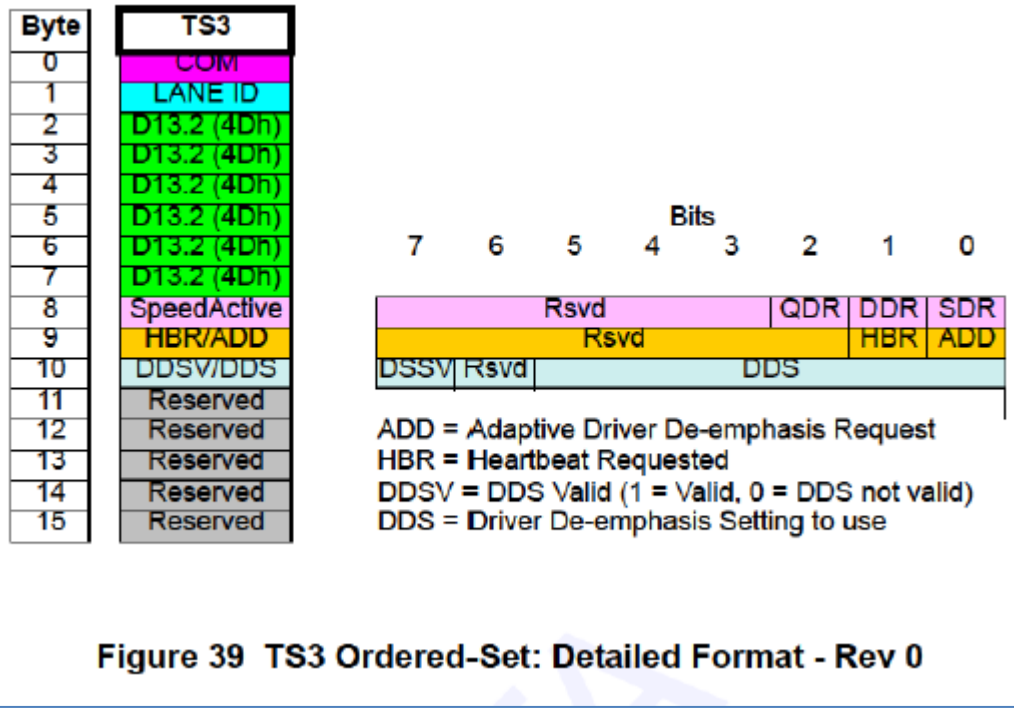
Claim 11	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 11	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 11	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 11	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 11	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 11	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 11	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

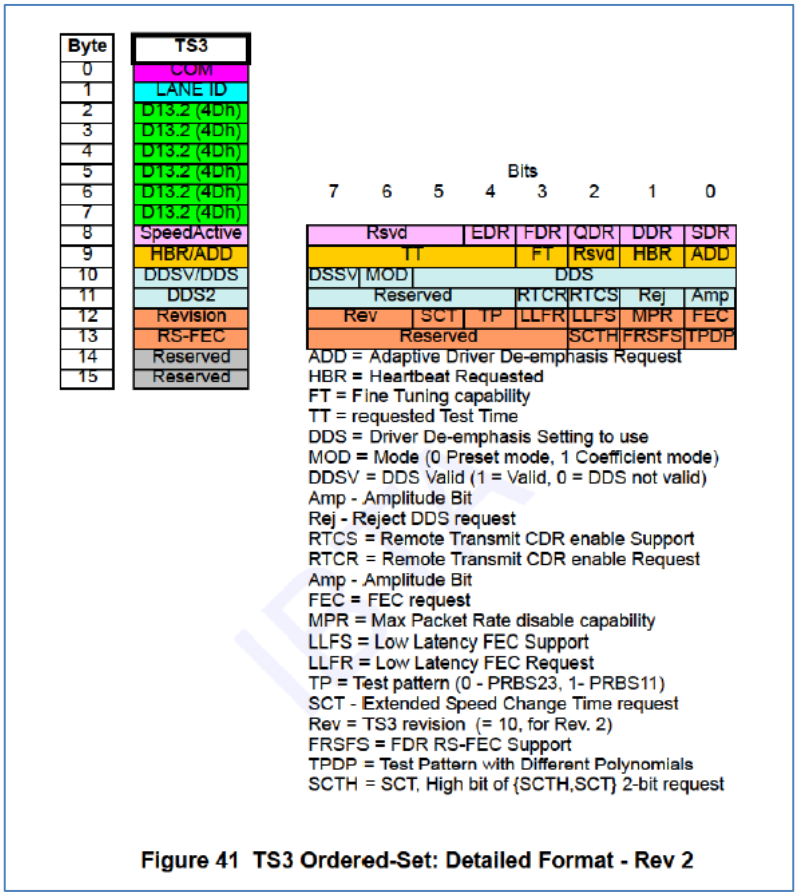
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 11	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 11	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 11	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 11	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 11	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 11	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 11	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 11	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

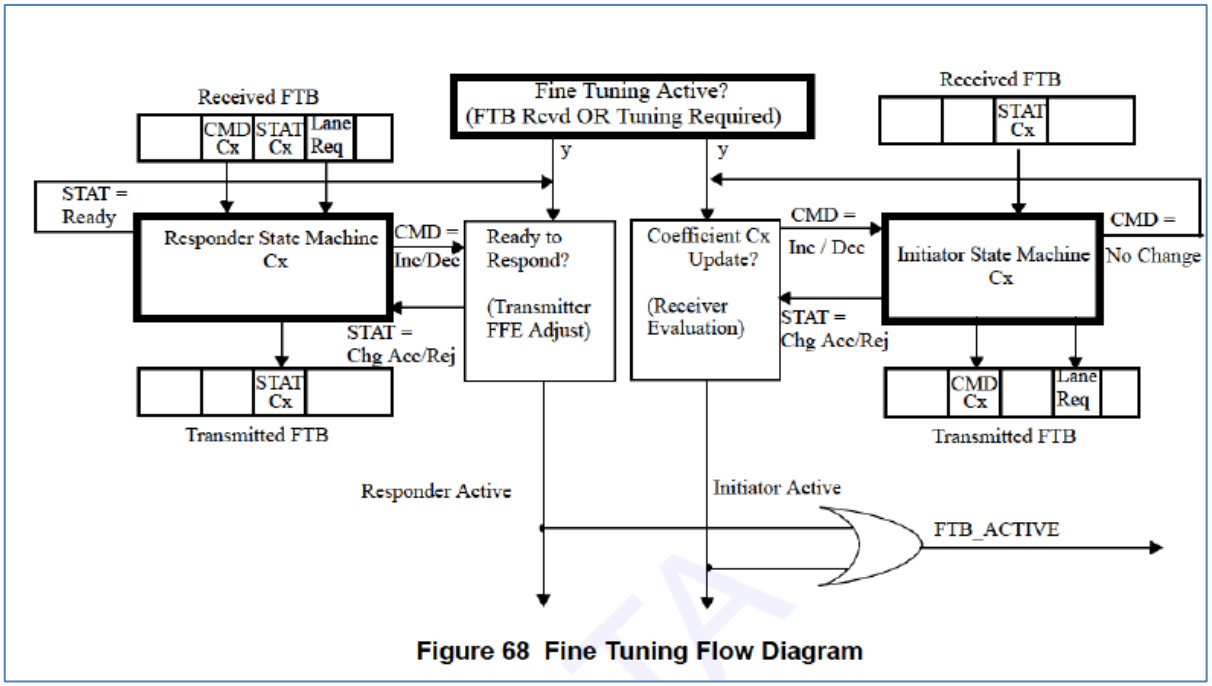
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 11	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 11	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 11	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 11	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 11	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 11	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"The overall pre-equalizer **800** can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."

Rafie, paragraph 82.

"Digital pre-equalizer (PEQ) circuit **204** can be configured to introduce a distortion to the input signal to compensate for channel impairment. At power-on little or no information may be known about the channel. Accordingly, the digital PEQ circuit **204** can be initially configured with no distortion. In some

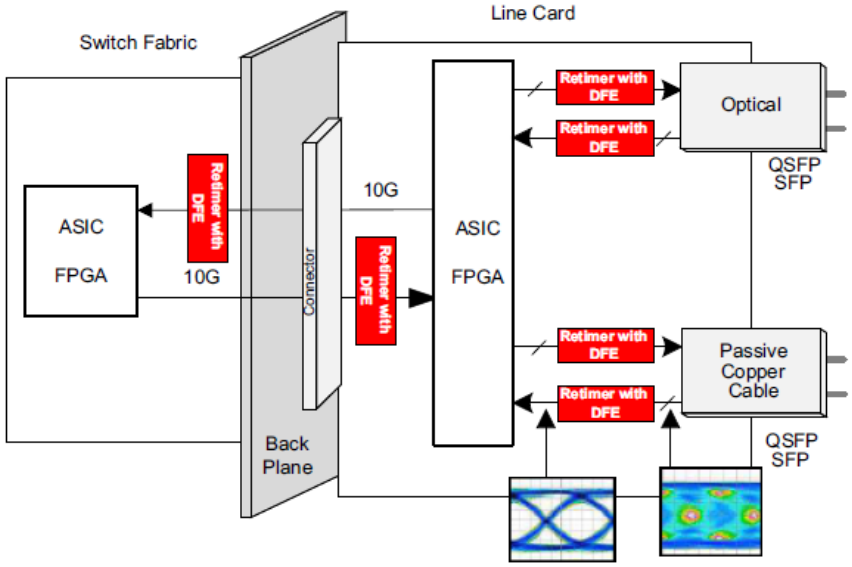
Claim 11	Disclosure
	embodiments, the digital PEQ circuit **204** can be initially configured with a distortion that is based upon a corresponding set of coefficients." Ciacci, 5:40-47. "Once frequency response of front-end components has been characterized, this information can be stored in the digital base band on a configuration register (CFR), and thereby used to specify gain coefficients of the digital pre-equalizer. Balakrishnan, paragraph 27. *U.S. Patent Publication No. 2014/0281067 ("Das Sharma")* Das Sharma discloses that, during its training phase, adapted equalization coefficients are determined by the receiving-side transceiver based on the received test signals and the adapted coefficients are then provided to transmitter-side transceiver. *See, e.g.*, Das Sharma at [0078], [0193], Figure 5. The '111 Patent describes testing each set of coefficients and selecting one that best performs best based on a performance characteristic such as "an error signal energy" or a "bit error rate." *See, e.g.*, '111 Patent at 2:4-5, 14:12-43, claims 5-6. The specification's only description supporting claim 4's selection of the register with the best performing coefficients is Figure 8, steps 802-812. *See id*. at 14:12-15:3. That disclosure describes actions by "training controller link or link controller" that receives test signals (steps 808 and 818) and selects the best performing register on a "***remote*** transmitter" that transmitted the test signals. *See id*. at 14:12-56. The "***remote*** transmitter" is "instructed to use those preset coefficients" from a register selected in step 812 "as a starting point" and "programs the pre-equalizer with the preset coefficients from the selected register and transmits a training pattern and/or data." *See id*. at 14:38-43.

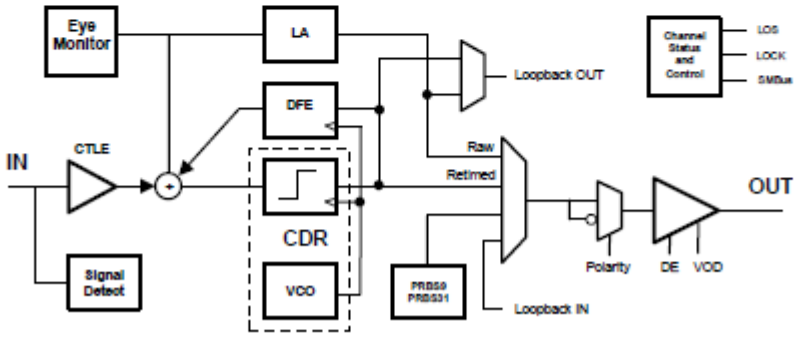
Claim 11	Disclosure
	United States Patent No. 7,239,665 ("Mezer") Mezer discloses a selection is made from among the registers storing different sets of pre-computed pre-equalization coefficients by having the pluggable module transceiver send different instances of a test signal that were pre-equalized with the different set of coefficients and then selecting (at either the pluggable module transceiver or the port transceiver) the set of coefficients that performed best. *See, e.g.*, Mezer, 6:50-57 (describing determining a "channel type[]" to select between the different pre-computed channel models associated with different channel types). *PCIe 3.1a* The equalization procedure consists of up to four Phases, as described below. When operating at the 8.0 GT/s data rate, the Phase information is transmitted using the Equalization Control (EC) field in the TS1 Ordered Sets. Phase 0: The Downstream Port communicates the Transmitter preset values and the Receiver preset hints for each Lane to the Upstream Port using 8b/10b encoding. These values are communicated using the EQ TS2 Ordered Sets (defined in Section 4.2.4.1) in Recovery.RcvrCfg, when a data rate change to 8.0 GT/s has been negotiated, prior to transitioning to 8.0 GT/s data

Claim 11	Disclosure
	rate. These preset values are derived from the Upstream Port Transmitter Preset and Upstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. After the data rate change to 8.0 GT/s, the Upstream Port transmits TS1 Ordered Sets with the preset values it received. The preset values must be within the operable range defined in Section 4.3.3.5.2 if reduced swing will be used by the Transmitter. Phase 1: Both components make the Link operational enough at 8.0 GT/s data rate to be able to exchange TS1 Ordered Sets to complete remaining phases for the fine-tuning their Transmitter/Receiver pairs. It is expected that the Link will operate at a BER of less than 10^{-4} before the component is ready to move on to the next Phase. The Downstream Port initiates Phase 1 by transmitting TS1 Ordered Sets with EC=01b (indicating Phase 1) to the Upstream Port using the preset values in the Downstream Port Transmitter Preset and, optionally, the Downstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. The Upstream Port, after adjusting its Receiver, if necessary, to ensure that it can progress with the equalization process, receives these TS1 Ordered Sets and transitions to Phase 1 (where it transmits TS1 Ordered Sets with EC=01b). The Downstream Port ensures that it can reliably receive the bit stream from the Upstream Port to continue through the rest of the Phases when it receives TS1 Ordered Sets from the Upstream Port with EC=01b before it moves on to Phase 2. Phase 2: In this Phase the Upstream Port adjusts the Transmitter setting of the Downstream Port along with its own Receiver setting, independently, on each Lane, to ensure it receives the bit stream compliant with the requirements in Section 4.3 (e.g., all operational Downstream Lanes have a BER is less than 10^{-12}). The Downstream Port initiates the move to Phase 2 by transmitting TS1 Ordered Sets with EC=10b to the Upstream Port. The Downstream Port advertises the Transmitter coefficients and the preset it is using per the rules below in Phase 1 for preset only and in Phase 2 for preset and coefficients. The Upstream Port receives these Ordered Sets and may request different coefficient or preset settings and continue to evaluate each setting until it arrives at the best setting for operating the Downstream Lanes. After the Upstream Port has completed this Phase, it moves the Link to Phase 3 by transmitting TS1 Ordered Sets with EC=11b to the Downstream Port. Phase 3: In this Phase the Downstream Port adjusts the Transmitter setting of the Upstream Port along with its own Receiver setting, independently, on each Lane, using a handshake and evaluation process similar to Phase 2 with the exception that EC=11b. The Downstream Port signals the end of Phase 3 (and the equalization procedure) by transmitting TS1 Ordered Sets with EC=00b. PCIe 3.1a at 240-241.

Claim 11	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

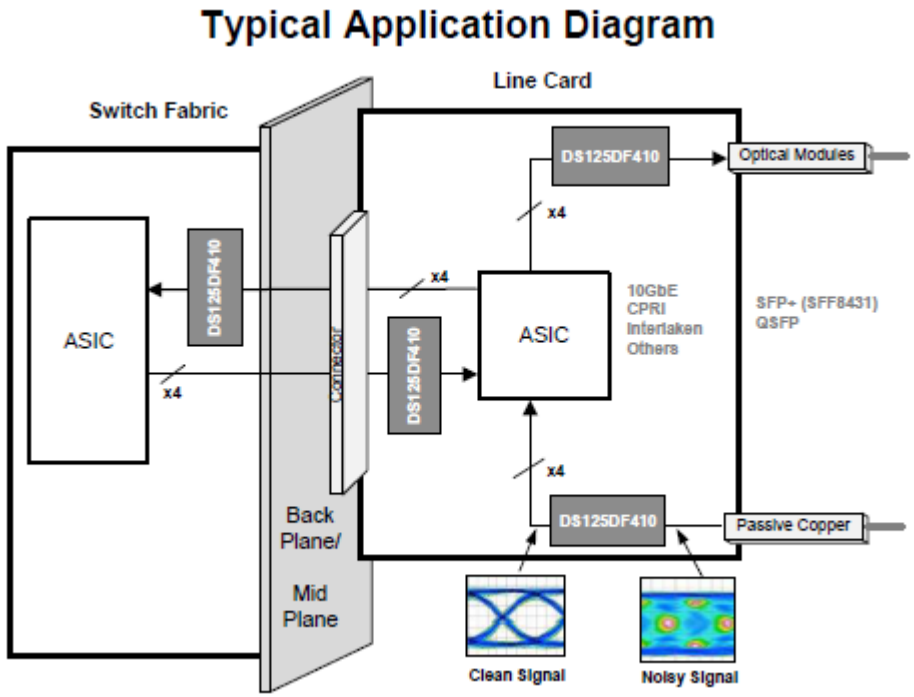
Claim 11	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 11	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 11	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

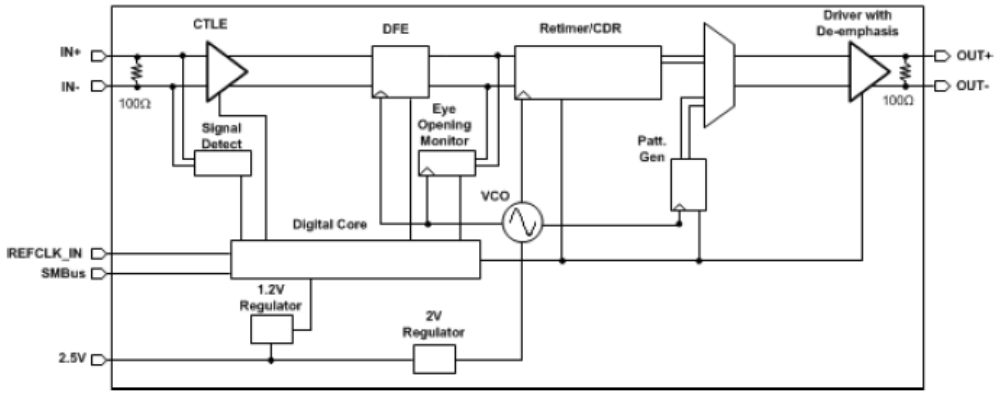
Claim 11	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 11	Disclosure
	7.5.1.26 Setting the Output De-Emphasis Setting *Register 0x15, bits 2:0 and bit 6* Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25. **Table 25. De-Emphasis Settings** PIN SETTING | REGISTER 0X15 BIT [2], drv_dem[2] | REGISTER 0X15 BIT [1], drv_dem[1] | REGISTER 0X15 BIT [0], drv_dem[0] | REGISTER 0X15 BIT [6], drv_dem_range | DE-EMPHASIS SETTTING (dB) 0 | 0 | 0 | 0 | 0 | 0.0 | 0 | 0 | 1 | 1 | -0.9 R | 0 | 0 | 1 | 0 | -1.5 | 0 | 1 | 0 | 1 | -2.0 | 0 | 1 | 1 | 1 | -2.8 | 1 | 0 | 0 | 1 | -3.3 F | 0 | 1 | 0 | 0 | -3.5 | 1 | 0 | 1 | 1 | -3.9 | 1 | 1 | 0 | 1 | -4.5 | 0 | 1 | 1 | 0 | -5.0 | 1 | 1 | 1 | 1 | -5.6 1 | 1 | 0 | 0 | 0 | -6.0 | 1 | 0 | 1 | 0 | -7.5 | 1 | 1 | 0 | 0 | -9.0 | 1 | 1 | 1 | 0 | -12.0 TI DS110DF111, 32.

Claim 11	Disclosure
	 TI DS125DF410, 1.

Claim 11	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 11	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 11	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 11	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 11	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 11	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 11	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

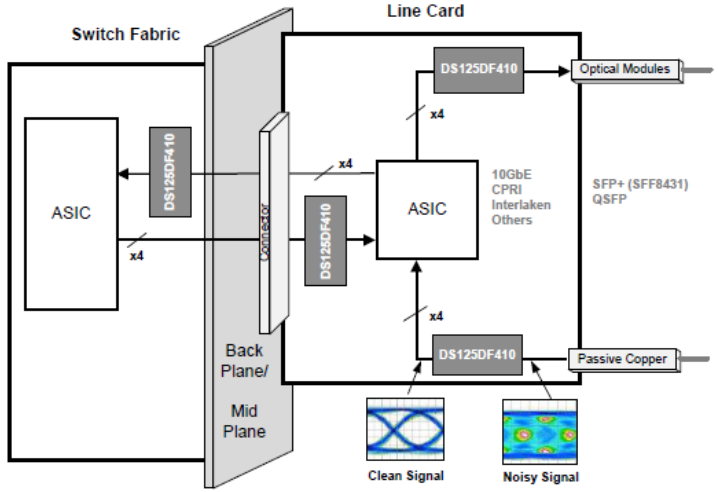
TI DS125DF410, 41.

Claim 11	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 11	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 11	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 11	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

L. DEPENDENT CLAIM 12

Claim 12	Disclosure
12. The communications link of claim 11, wherein the performance characteristic is an error signal energy.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

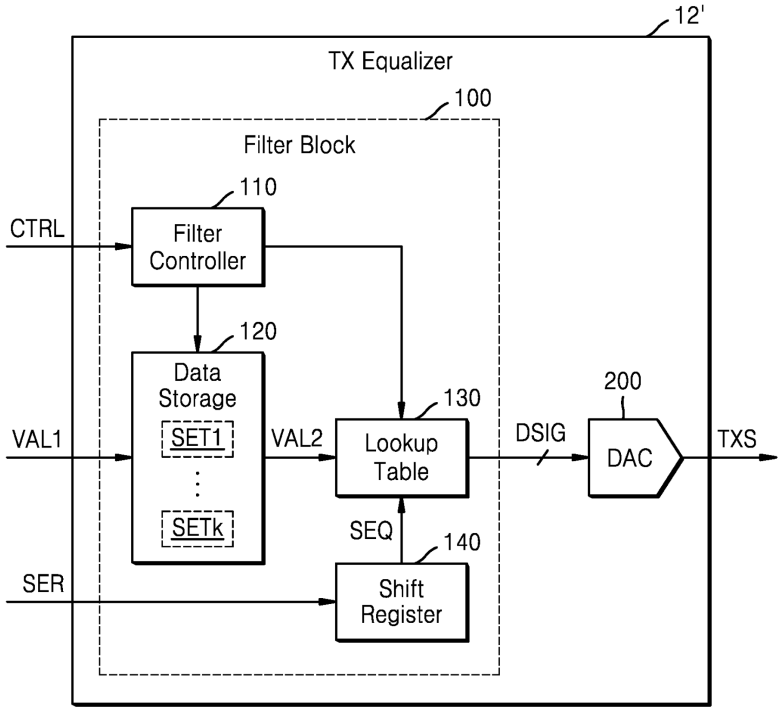
Claim 12	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 12	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

Claim 12	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 12	Disclosure

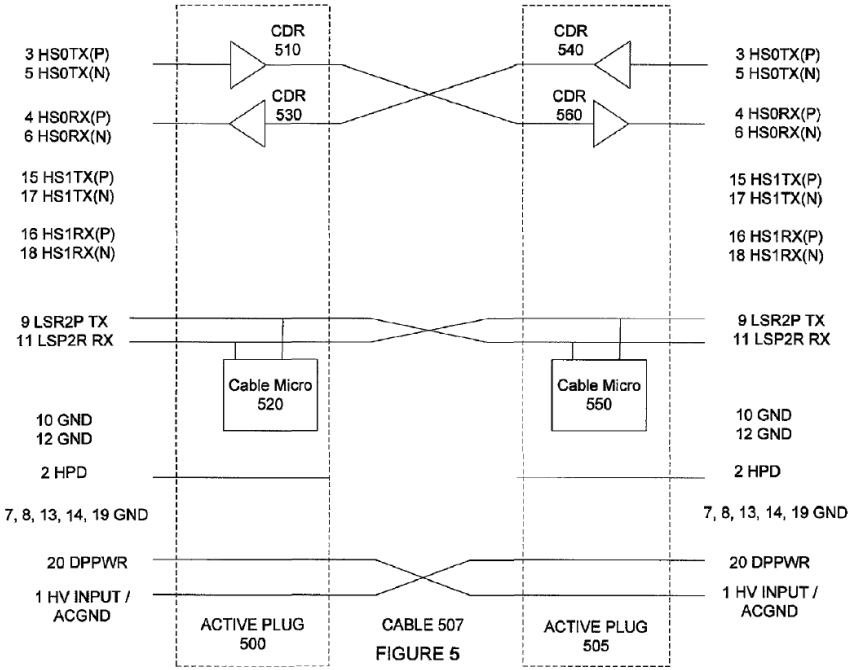
FIG. 3



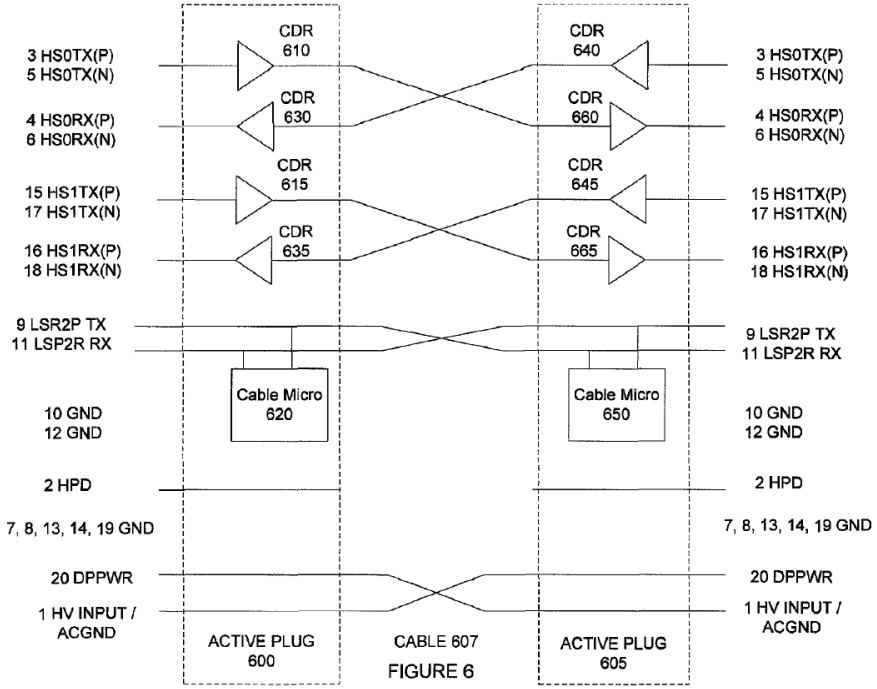
Kang, FIG. 3

"FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

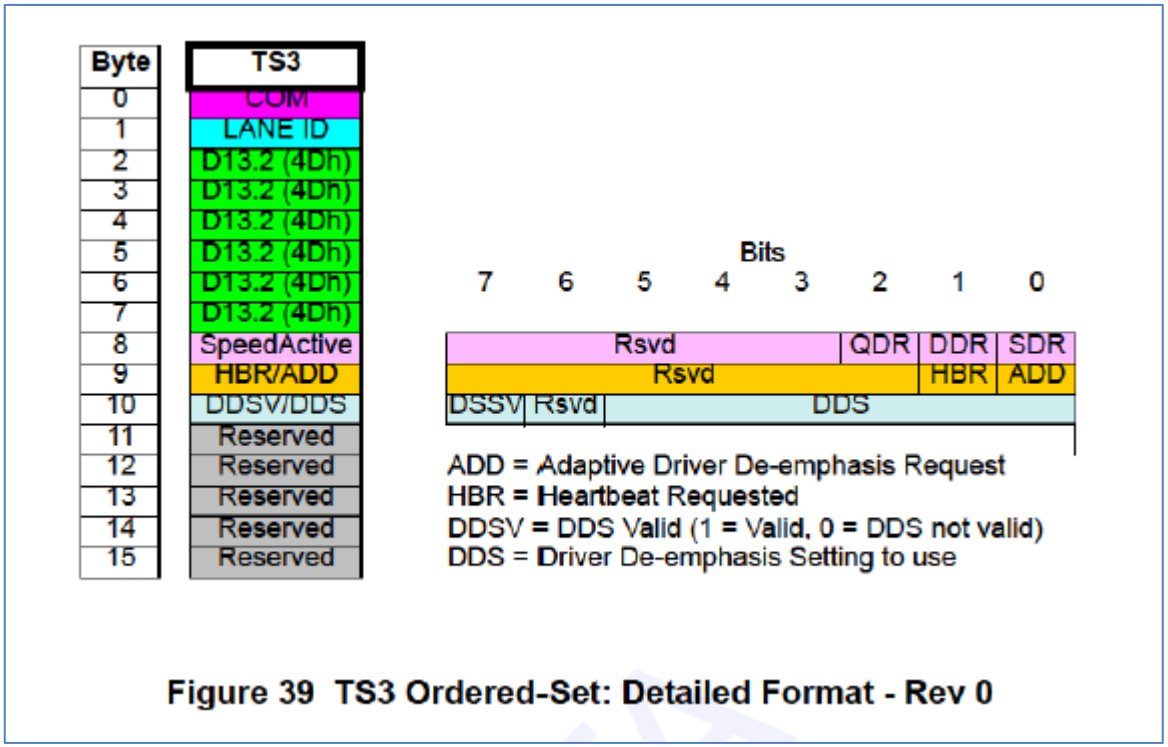
Claim 12	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 12	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

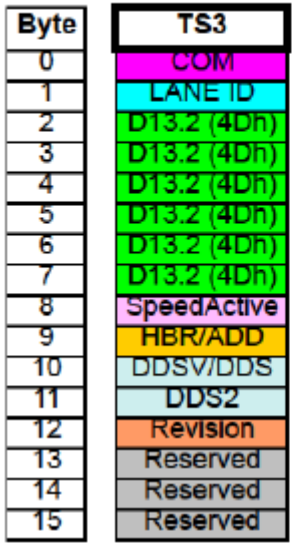
Claim 12	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 12	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

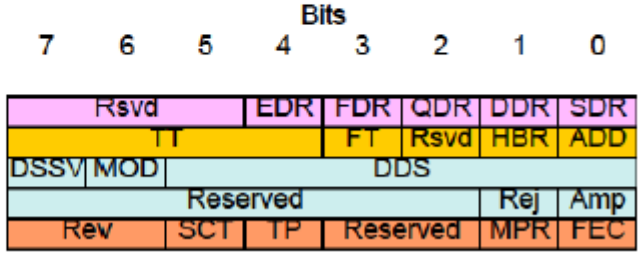
Claim 12	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 12	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 12	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved



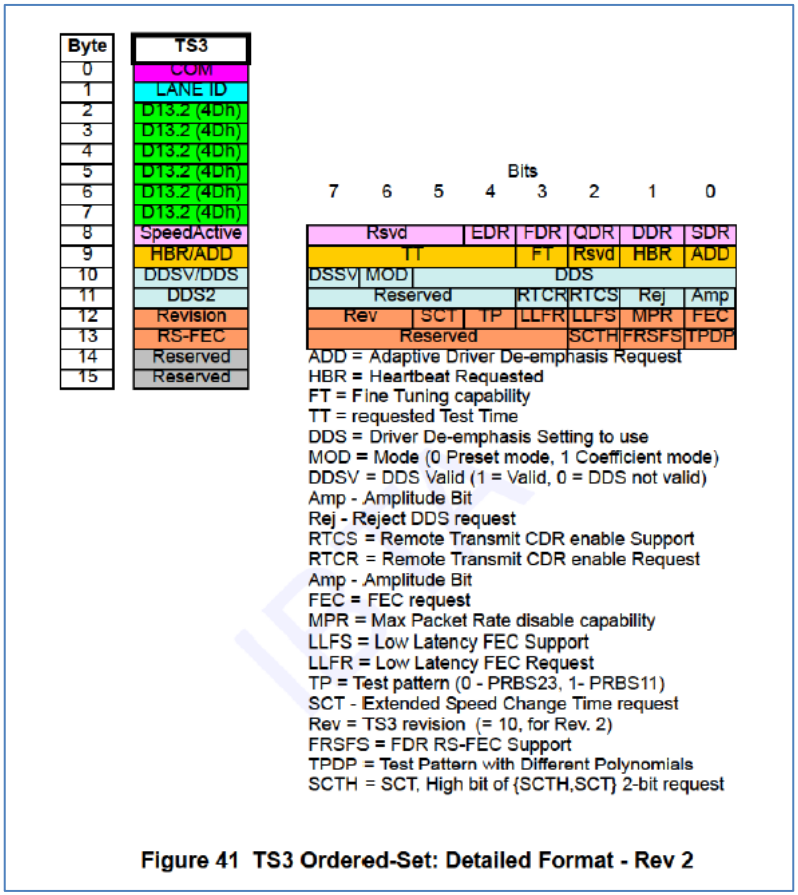
Bits 7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 12	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 12	Disclosure
	5.5.2.4.1 Rev 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 12	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 12	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 12	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 12	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 12	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 12	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

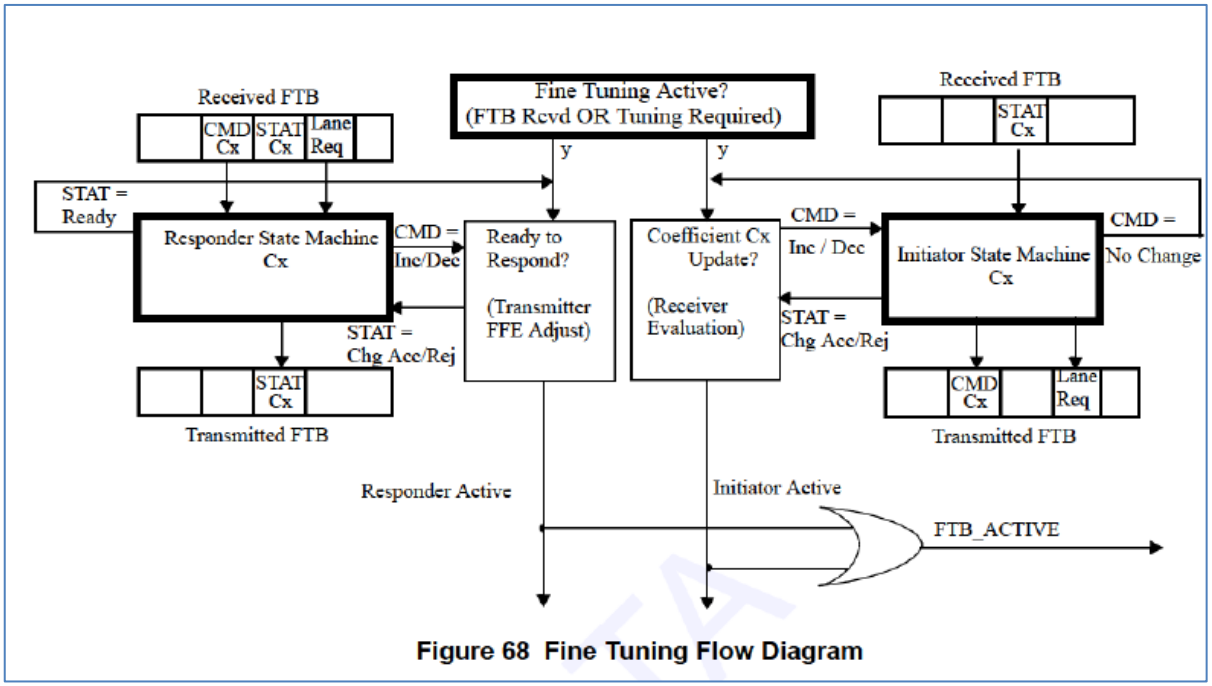
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 12	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 12	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 12	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 12	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 12	Disclosure
	Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 12	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"Once the initial QAM modulation order and R-S FEC parameters have been set, the system enters a "tracking" or "maintenance" mode, as shown in detail in the process steps **400** illustrated in **FIG. 4.** Specifically, the process steps **400** utilize ongoing CMTS receiver measurements, such as bit error rates, modulation error rates, and power measurements, to continually recalculate and optimize various CMTS receiver parameters in each channel's profile."

Fox, p. 11.

United States Patent No. 7,239,665 ("Mezer")

Mezer "adapt[s]" equalizer coefficients "on the basis of an error signal" that "indicates deviation of the" received training signal "from a pre-determined ideal signal profile." *See, e.g.*, Mezer, 2:27-49, 3:5-7. That

Claim 12	Disclosure
	meets the claimed "error signal energy." *See* '111 Patent at 14:29-30 ("measur[ing] error signals" represents "the difference between the equalized receive signals and an idealized receive signal"). **1 Features** • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 12	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 12	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

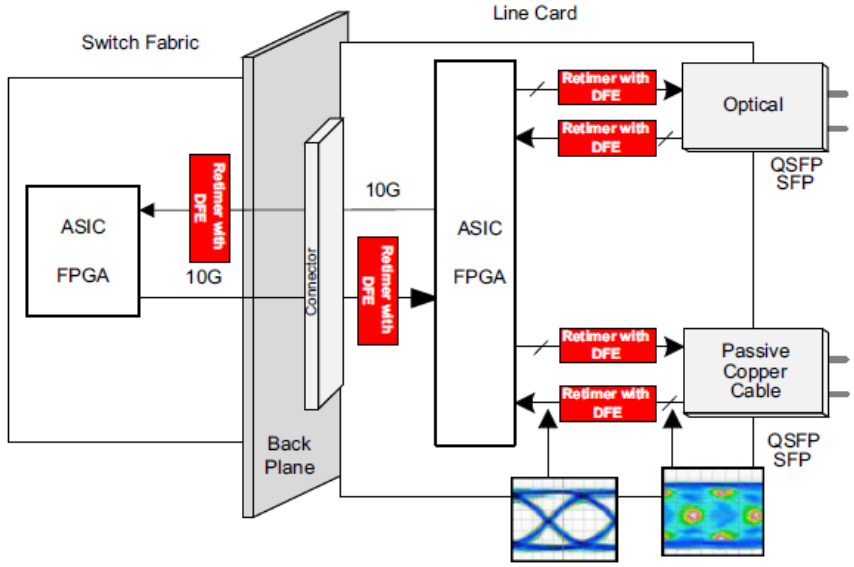
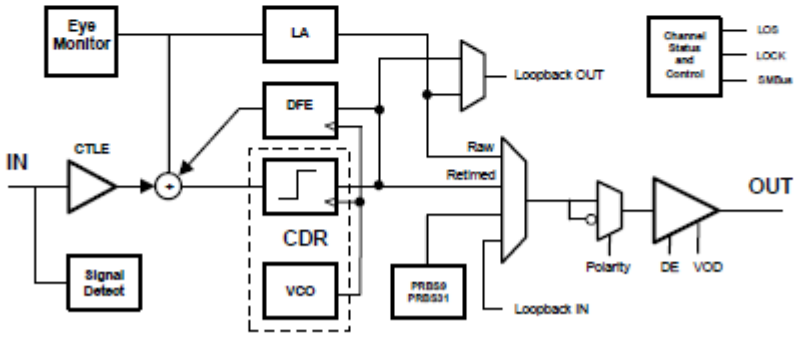


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 12	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 12	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 12	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

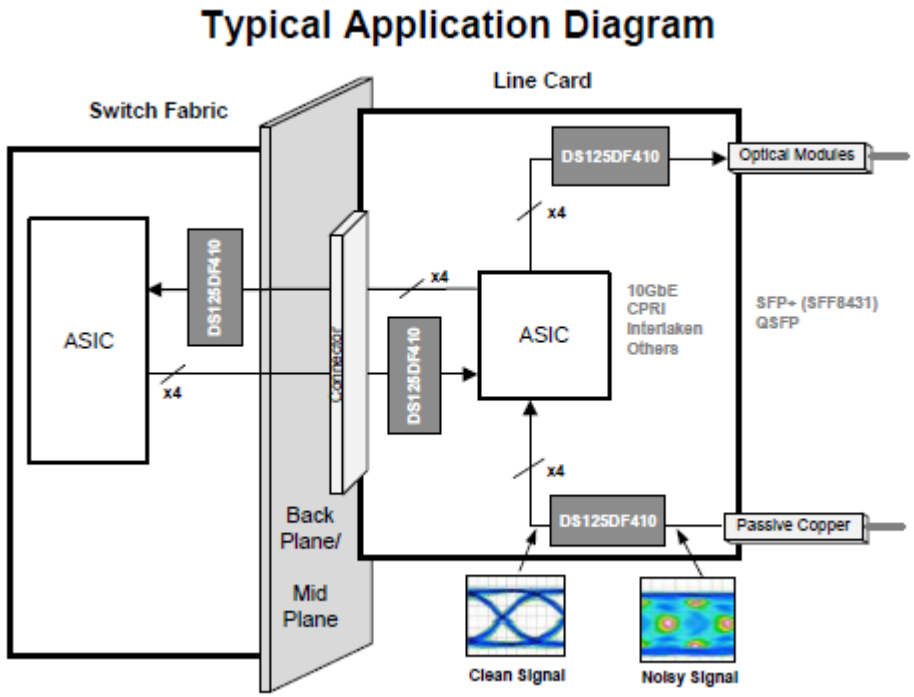
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

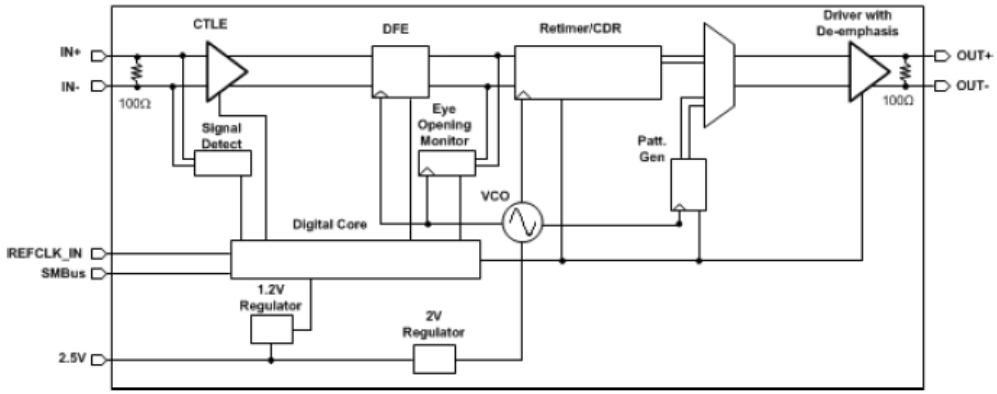
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 12	Disclosure
	 TI DS125DF410, 1.

Claim 12	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 12	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 12	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 12	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 12	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 12	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 12	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 12	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 12	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

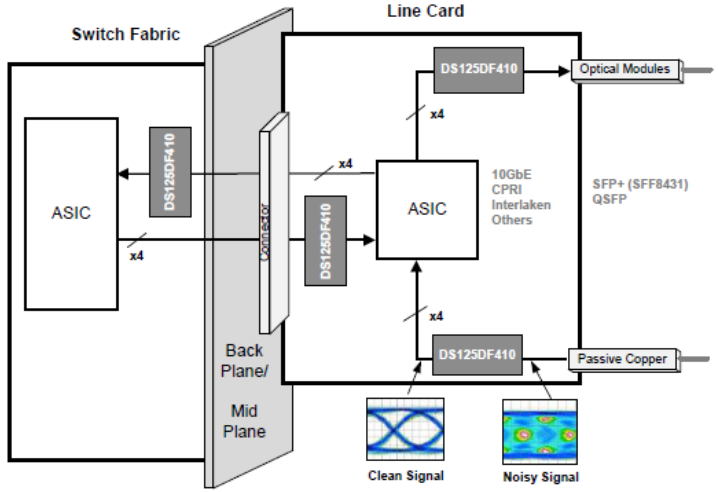
TI DS125DF410, 41.

Claim 12	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 12	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 12	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 12	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

Claim 12	Disclosure

M. DEPENDENT CLAIM 13

Claim 13	Disclosure
13. The communications link of claim 11, wherein the performance characteristic is a bit error rate.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

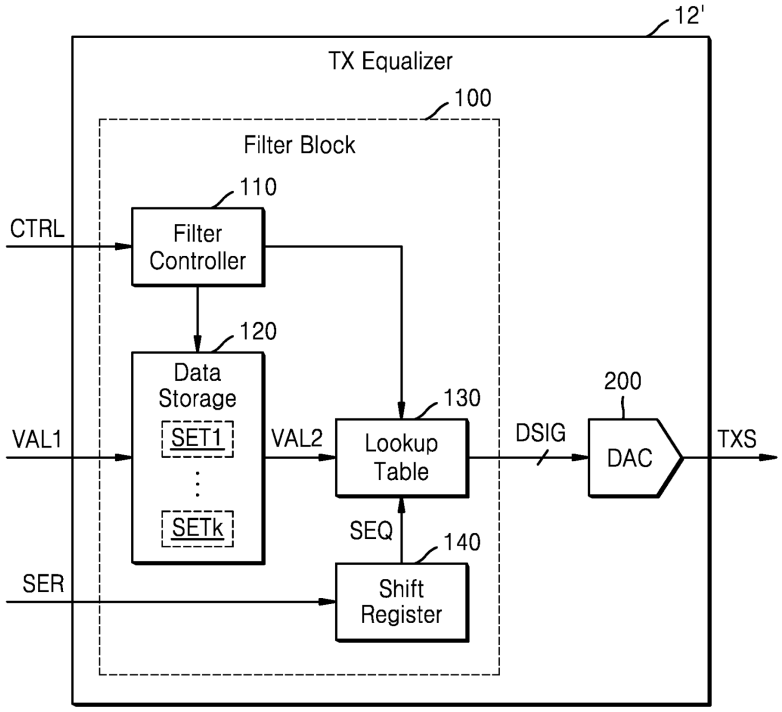
Claim 13	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 13	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

Claim 13	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 13	Disclosure

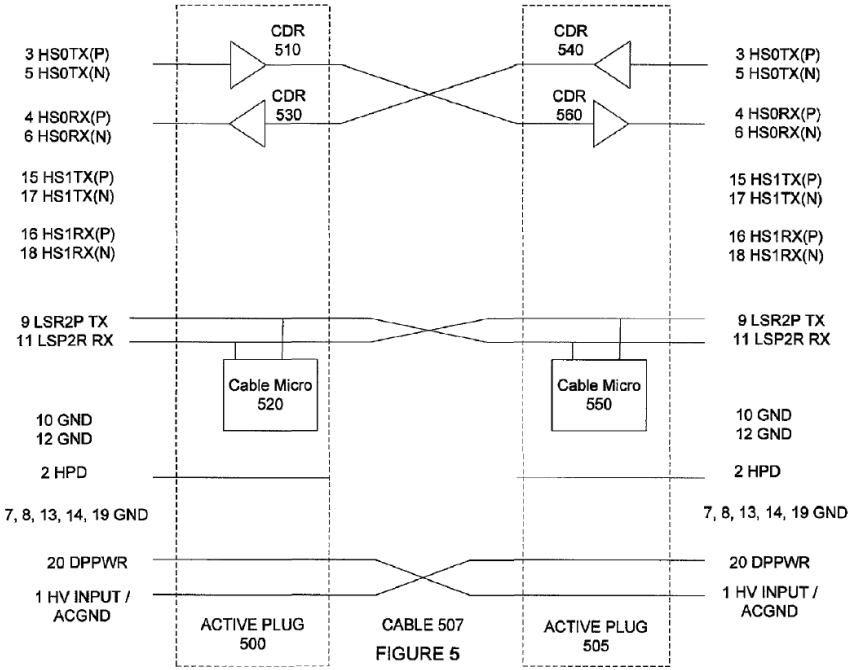
FIG. 3



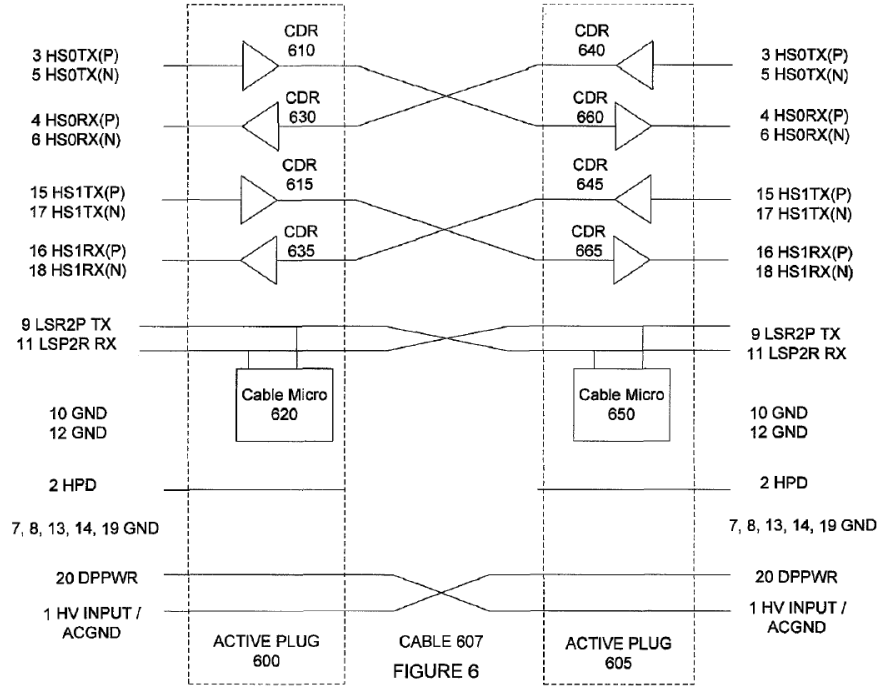
Kang, FIG. 3

"FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

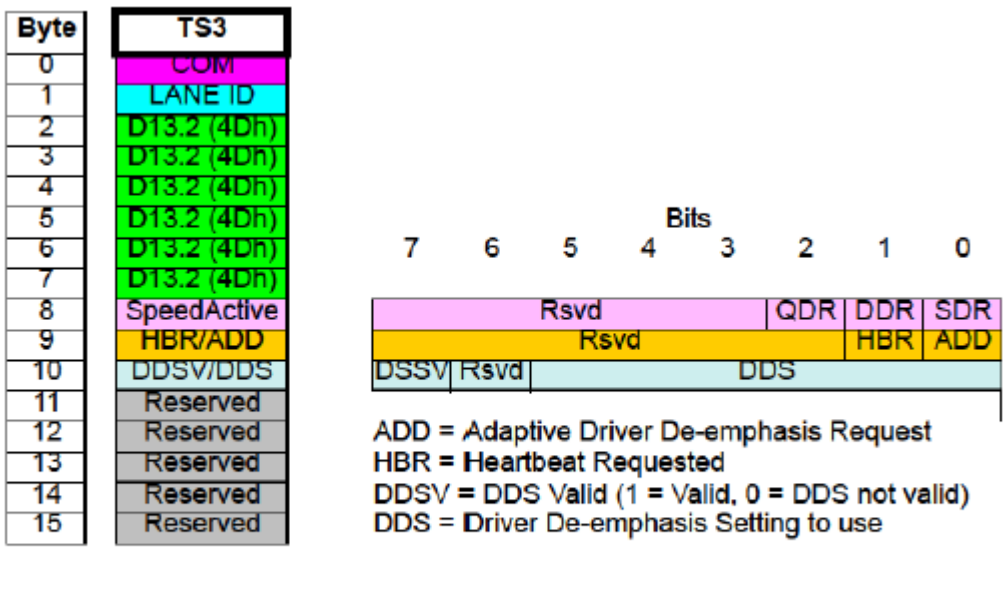
Claim 13	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 13	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

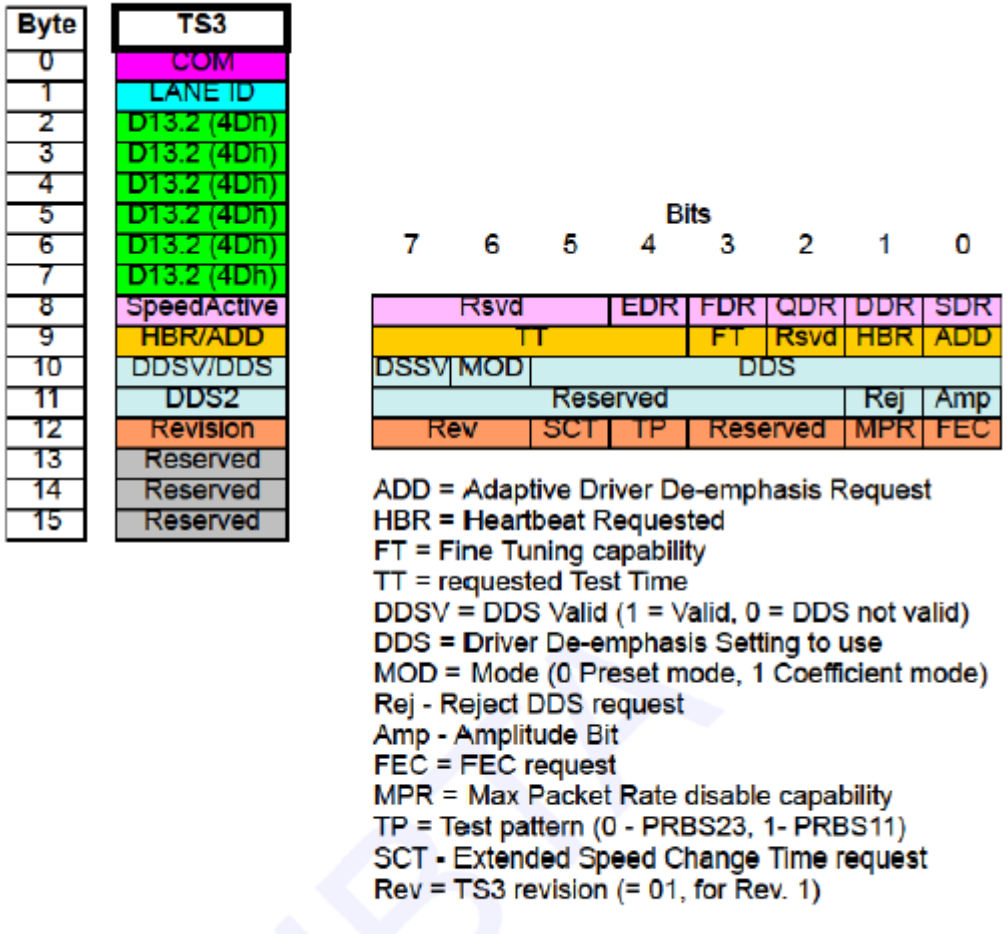
Claim 13	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 13	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 13	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 13	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 13	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

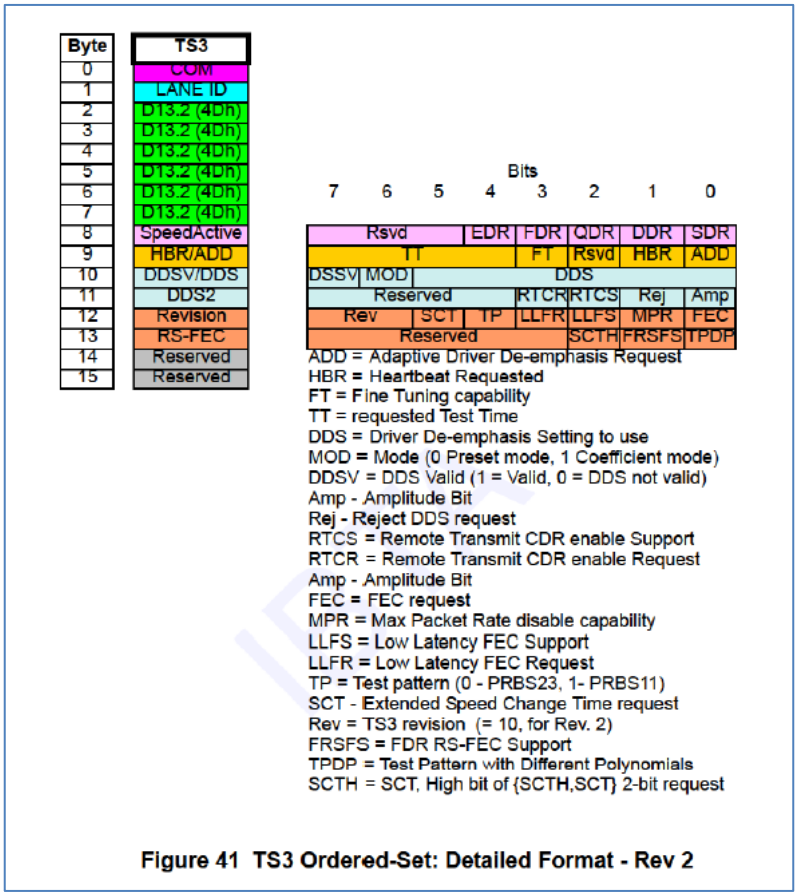
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 13	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 13	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 13	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 13	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 13	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 13	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 13	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 13	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

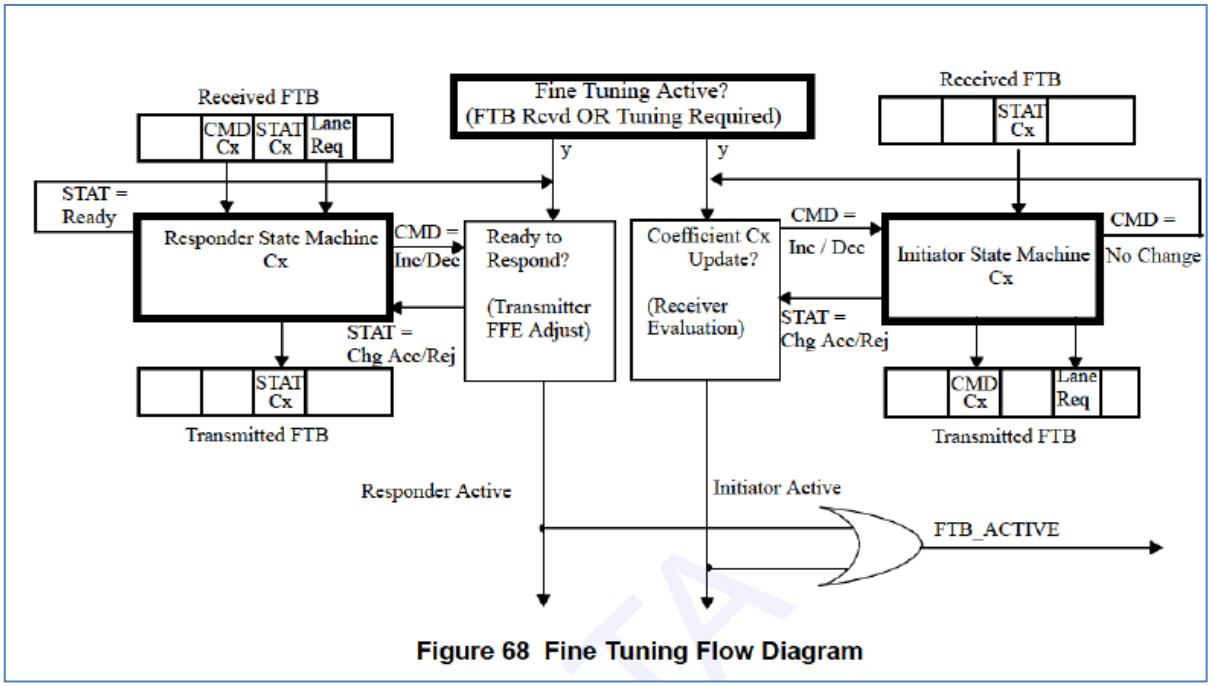
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 13	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 13	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 13	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 13	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 13	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 13	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"Once the initial QAM modulation order and R-S FEC parameters have been set, the system enters a "tracking" or "maintenance" mode, as shown in detail in the process steps **400** illustrated in **FIG. 4.** Specifically, the process steps **400** utilize ongoing CMTS receiver measurements, such as bit error rates, modulation error rates, and power measurements, to continually recalculate and optimize various CMTS receiver parameters in each channel's profile."

Fox, p. 11.

	U.S. Patent Publication No. 2014/0281067 ("Das Sharma") Das Sharma teaches the use of bit error rate and explains that it may be "the ratio of the number of bits incorrectly received (errors) and the total number of bits received." *See, e.g.*, Das Sharma at [0076]-[0077]. *United States Patent No. 7,239,665 ("Mezer")* Mezer "adapt[s]" equalizer coefficients "on the basis of an error signal" that "indicates deviation of the" received training signal "from a pre-determined ideal signal profile." *See, e.g.*, Mezer, 2:27-49, 3:5-7. That meets the claimed "error signal energy." *See* '111 Patent at 14:29-30 ("measur[ing] error signals" represents "the difference between the equalized receive signals and an idealized receive signal").

Claim 13	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 13	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 13	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

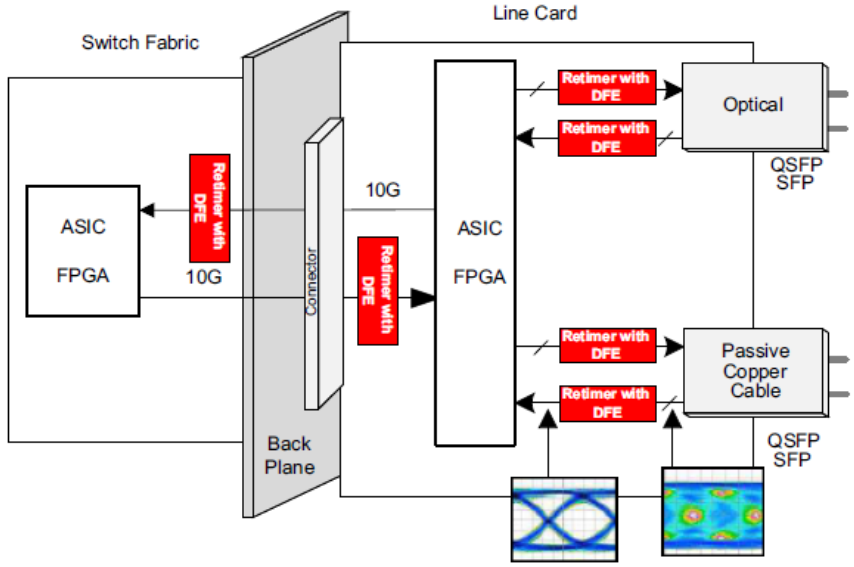
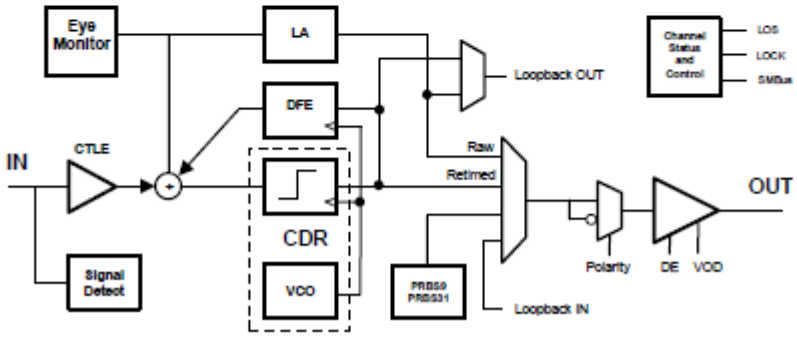


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 13	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 13	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 13	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

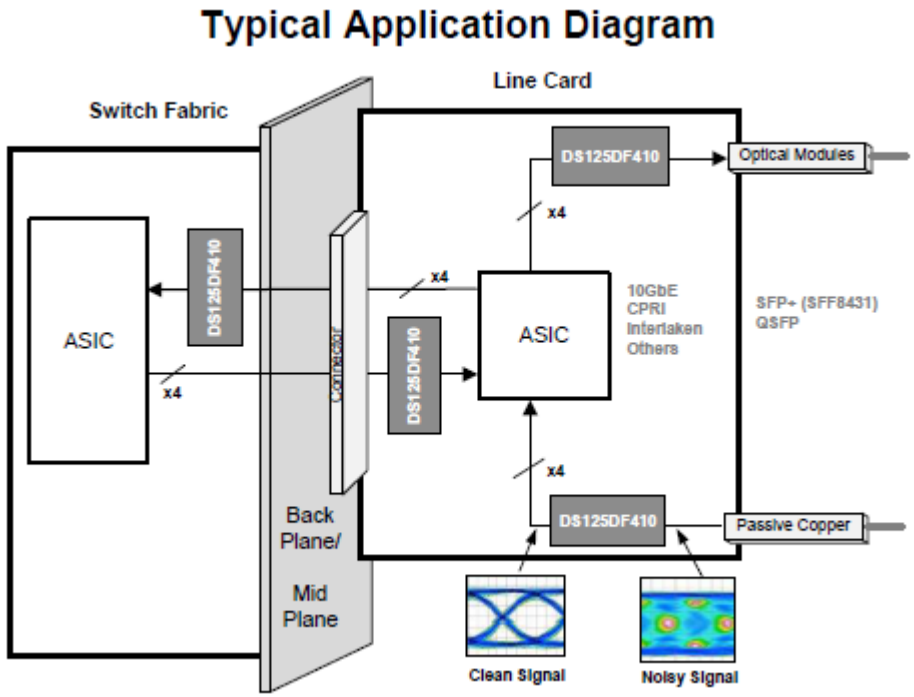
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

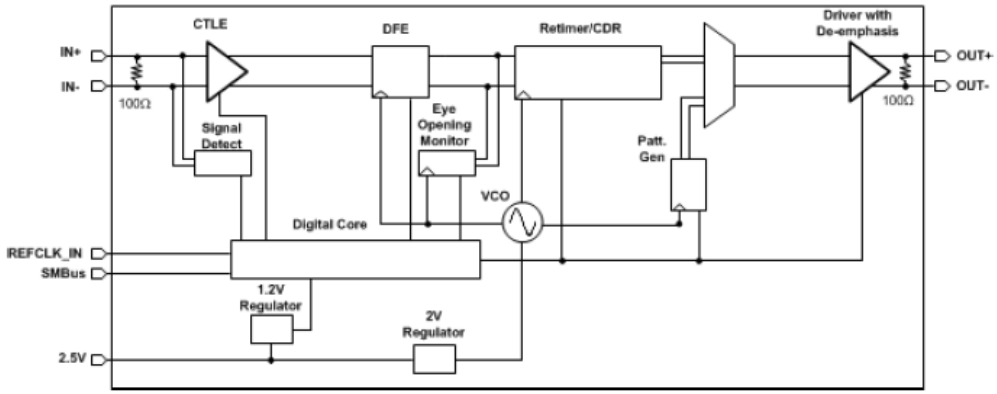
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 13	Disclosure
	 TI DS125DF410, 1.

Claim 13	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 13	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 13	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 13	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 13	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 13	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 13	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 13	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 13	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

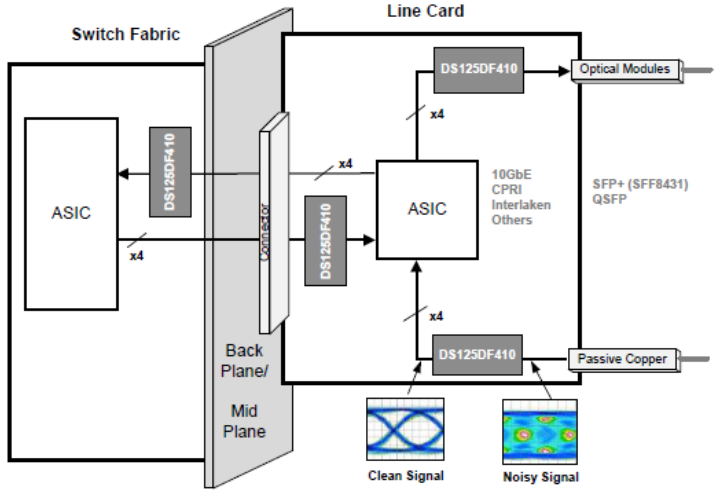
TI DS125DF410, 41.

Claim 13	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 13	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 13	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

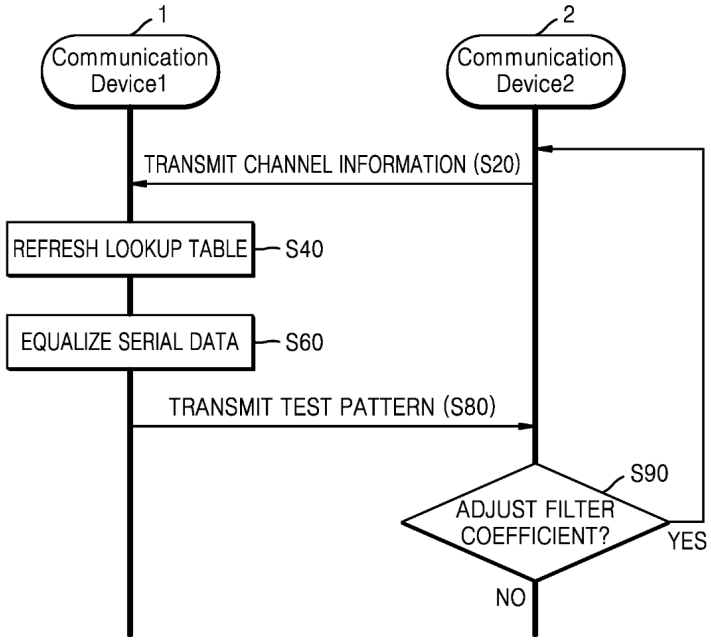
Claim 13	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

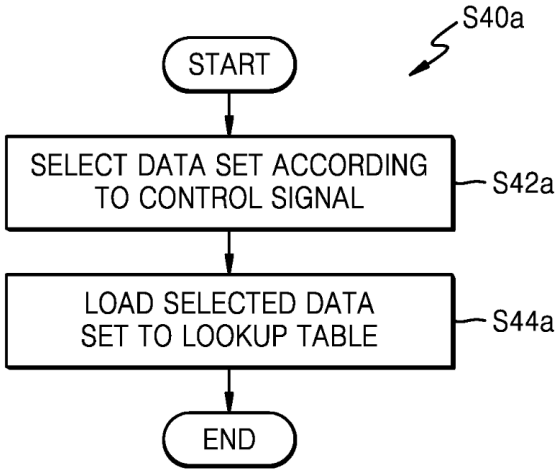
N. DEPENDENT CLAIM 14

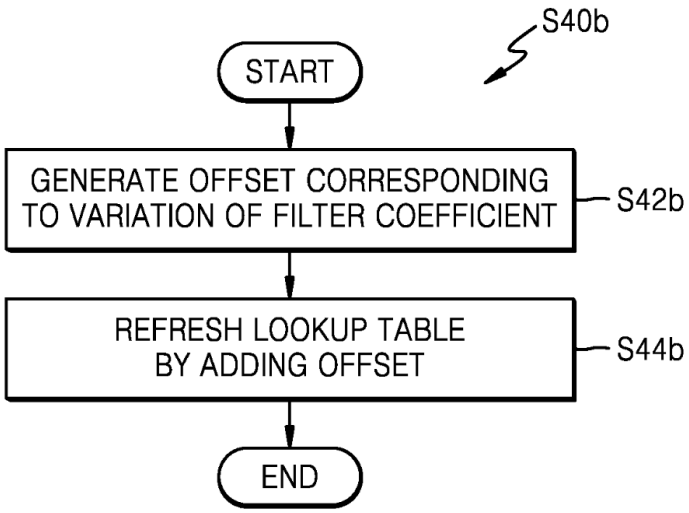
Claim 14	Disclosure
14. The communications link of claim 11, wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "FIG. 10 is a diagram illustrating an equalization method over time according to an exemplary embodiment of the disclosure. For example, the equalization method of FIG. 10 may be performed by the first communication device 1 including the TX equalizer 12 of FIG. 1 and the second communication device 2 communicating with the first communication device 1. The filter coefficients for equalization may be determined according to the equalization method illustrated in FIG. 10, and the method for determining the filter coefficients may be referred to as training of filter coefficients. It is assumed below that the first communication device 1 of FIG. 10 includes the components of the communication device 5 of FIG. 1, and FIG. 10 will be described with reference to FIG. 1. Referring to FIG. 10, in operation S20, the second communication device 2 may transmit channel information. For example, the second communication device 2 may first transmit, to the first communication device 1, channel information including information indicating one of the plurality of data sets, as described above with reference to FIG. 3. In operation S40, the first communication device 1 may refresh the lookup table LUT. For example, the protocol processor 30 of the first communication device 1 may extract information indicating a data set from the channel information received in operation S20 and may transmit the control signal CTRL

Claim 14	Disclosure
	including the extracted information to the TX equalizer 12. TX equalizer 12 may refresh the lookup table LUT based on the control signal CTRL. The lookup table LUT may include values of the digital signal DSIG corresponding to possible values of the symbol sequence extracted from the serial data SER. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information indicating a data set will be described with reference to FIG. 11. In operation S60, the first communication device 1 may equalize the serial data SER. For example, in the TX equalizer 12 of the first communication device 1, the lookup table LUT may output a digital signal (e.g., DSIG in FIG. 3) corresponding to the symbol sequence of the serial data SER, and the DAC 200 included in the TX equalizer 12 may convert the digital signal into an analog signal. Accordingly, an adder and a multiplier for multiplication and addition between the symbol sequence and the filter coefficient sequence for implementing the FIR filter 9 of FIG. 2 may be omitted. The example of operation S60 will be described with reference to FIG. 14. In operation S80, the first communication device 1 may transmit a test pattern. For example, the test pattern may include a pattern previously shared by the first communication device 1 and the second communication device 2, and the second communication device 2 may receive the test pattern through a channel (e.g., 7 of FIG. 1). In operation S90, the second communication device 2 may determine whether to adjust the filter coefficient. For example, the second communication device 2 may evaluate the test pattern received from the first communication device 1 and determine whether to adjust at least one of the coefficients of the FIR filter used for equalization of the first communication device 1 according to the evaluation result. As illustrated in FIG. 10, when it is determined not to adjust at least one of the filter coefficients, the training of the filter coefficients may be terminated and the first communication device 1 may transmit the signal, which is equalized according to the current filter coefficients, to the second communication device 2. On the other hand, when it is determined to adjust at least one of the filter coefficients, operation S20 may be performed. Unlike the initially performed operation S20, in operation S20, which is performed after operation S90, the second communication device 2 may transmit channel information, which includes information on the variation of the filter coefficients, to the first communication device 1. Thereafter, unlike the initially performed operation S40, in operation S40, the first communication device 1 may refresh the lookup table LUT based on the information on the variation of the filter coefficients. An example of operation S40 of

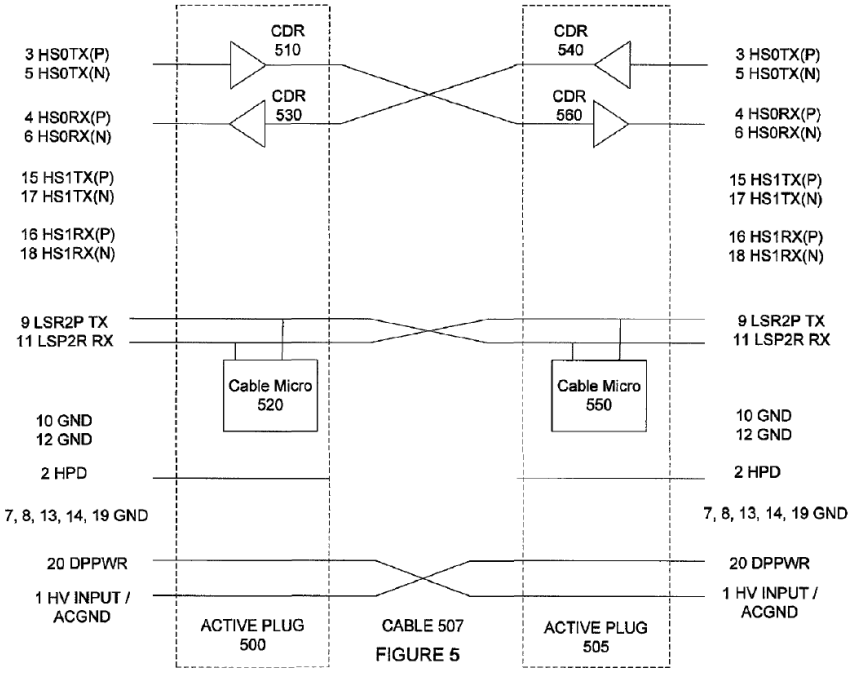
Claim 14	Disclosure
	refreshing the lookup table LUT in response to channel information including information on the variation of the filter coefficients will be described with reference to FIG. 12." Kang, 11:62-13:6 FIG. 10  Kang, FIG. 10 "Referring to FIG. 11, operation S**40** *a* may include operations S**42** *a* and S**44** *a*. In operation S**42** *a*, an operation of selecting a data set according to the control signal CTRL may be performed. For example, the controller **110** of FIG. 3 may receive a control signal CTRL including information indicating one of k

Claim 14	Disclosure
	filter coefficient sequences and may control the data storage **120** to output one of first to k-th data sets SET**1** to SETk, which are stored in the data storage **120**, according to the control signal CTRL. In operation S**44** *a*, an operation of loading the selected data set into the lookup table **130** may be performed. For example, the controller **110** may control the data storage **120** and the lookup table **130** to store the second value VAL**2** outputted from the data storage **120** in the lookup table **130**. Referring to FIG. 12, operation S**40** *b* may include operations S**42** *b* and S**44** *b*. In operation S**42** *b*, an operation of generating an offset OFF corresponding to the variation of the filter coefficients may be performed. For example, the offset generator **150** of FIG. 6 may generate an offset OFF, based on the variation signal VAR and the index IDX provided from the controller **110′**. The variation signal VAR may indicate at least one of up, down, hold, and reset of the filter coefficient and may include a variation amount of the filter coefficient. An example of generating the offset OFF when the variation signal VAR indicates the reset of the filter coefficient will be described later with reference to FIG. 13. In operation S**44** *b*, an operation of refreshing the lookup table **130′** may be performed by adding the offset OFF. In some embodiments, the offset generator **150** may generate a positive offset OFF or a negative offset OFF, and thus the calculator **160** may perform an addition. In some embodiments, the offset generator **150** may generate the positive offset OFF, and thus the calculator **160** may perform addition or subtraction according to the control of the controller **110′**. The lookup table **130′** may be refreshed by storing the output value of the calculator **160**, that is, the third value VAL**3**, in the lookup table **130′**." Kang, 13:18-54

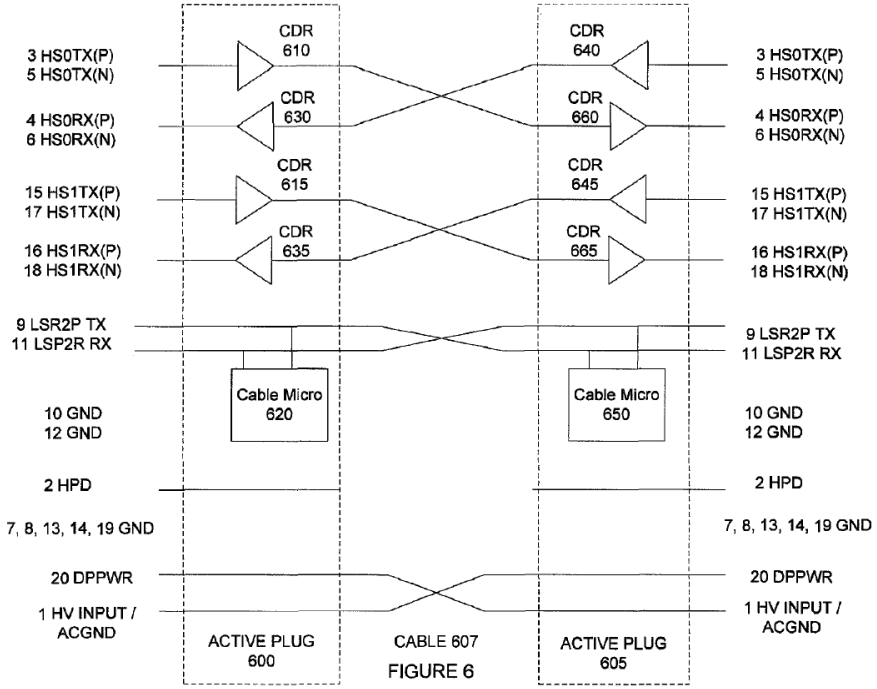
Claim 14	Disclosure
	FIG. 11  Kang, FIG. 11

Claim 14	Disclosure
	FIG. 12  Kang, FIG. 12 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**. Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**.

Claim 14	Disclosure
	The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables. In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used.

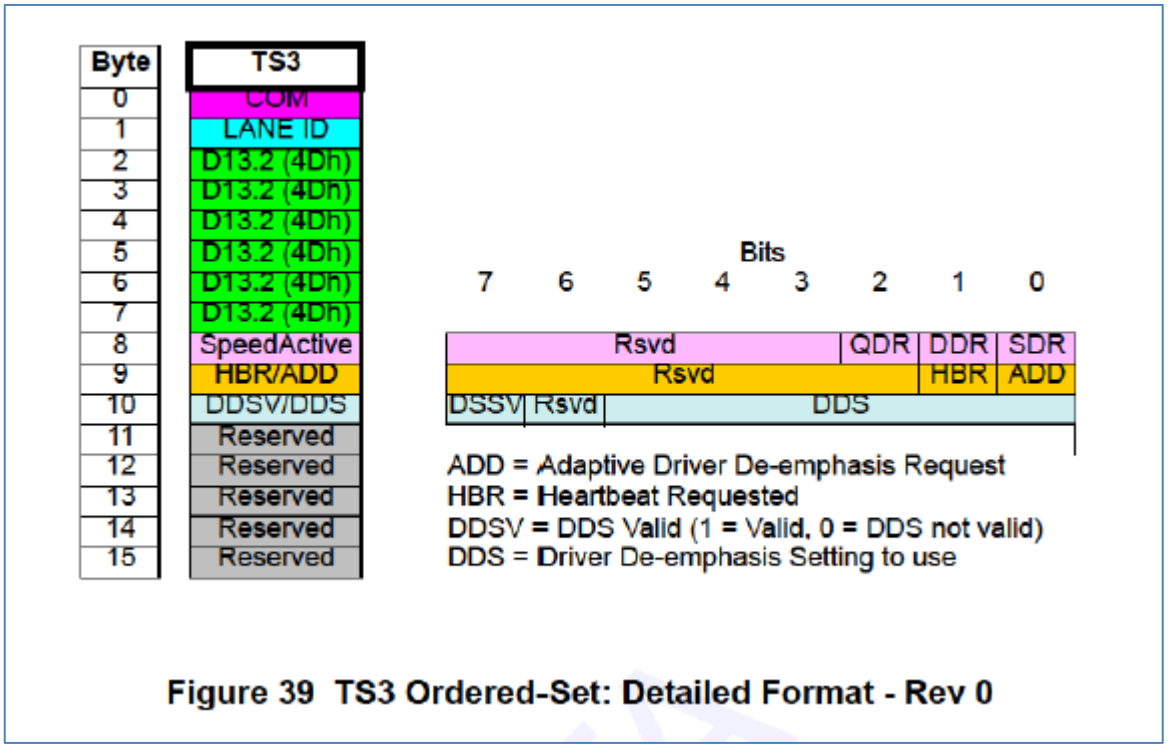
Claim 14	Disclosure
	In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5 "FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock

Claim 14	Disclosure
	and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 14	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 14	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 14	Disclosure

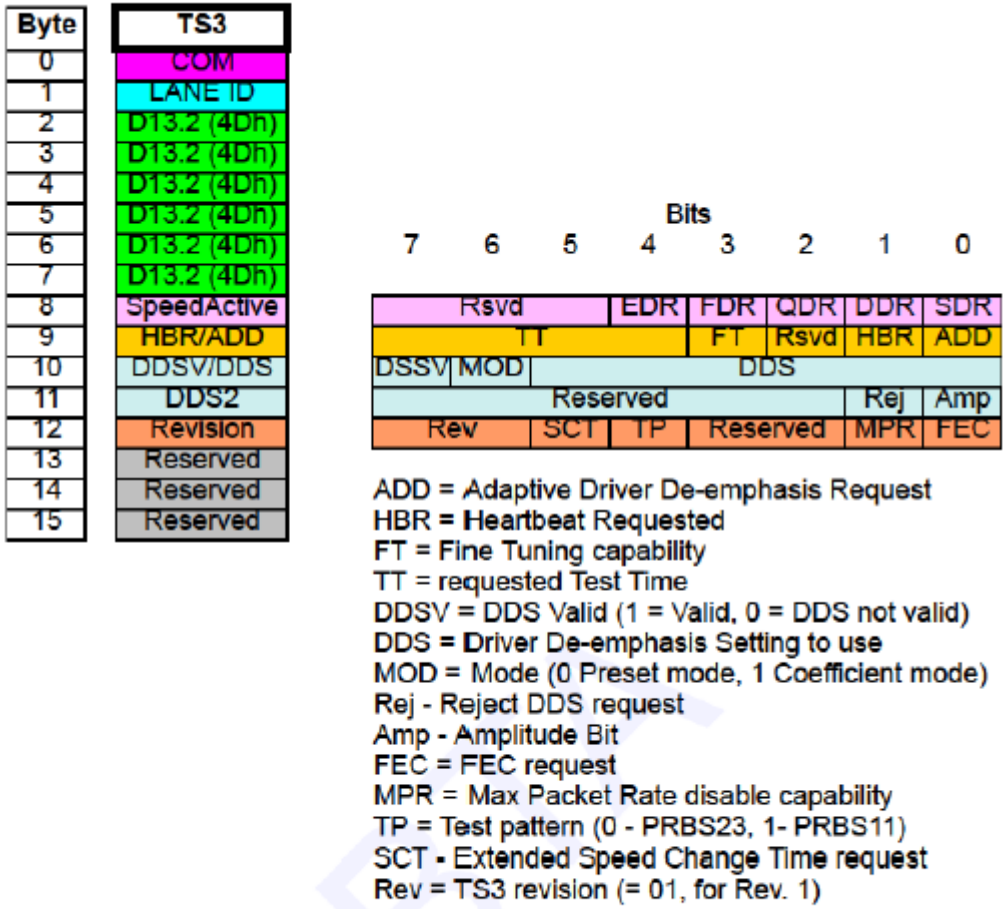


Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 14	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

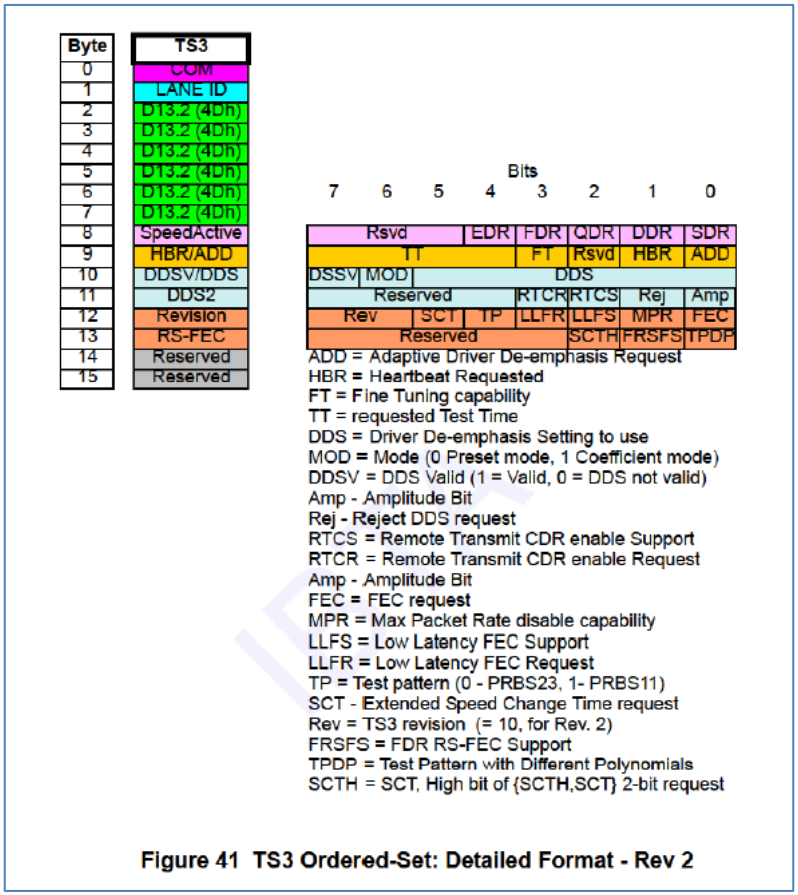
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 14	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits	7	6	5	4	3	2	1	0
	Rsvd			EDR	FDR	QDR	DDR	SDR
	TT				FT	Rsvd	HBR	ADD
	DSSV	MOD	DDS					
	Reserved				RTCR	RTCS	Rej	Amp
	Rev		SCT	TP	LLFR	LLFS	MPR	FEC
	Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 14	Disclosure
	5.5.2.4.1 Rev 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 14	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 14	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 14	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 14	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 14	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 14	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

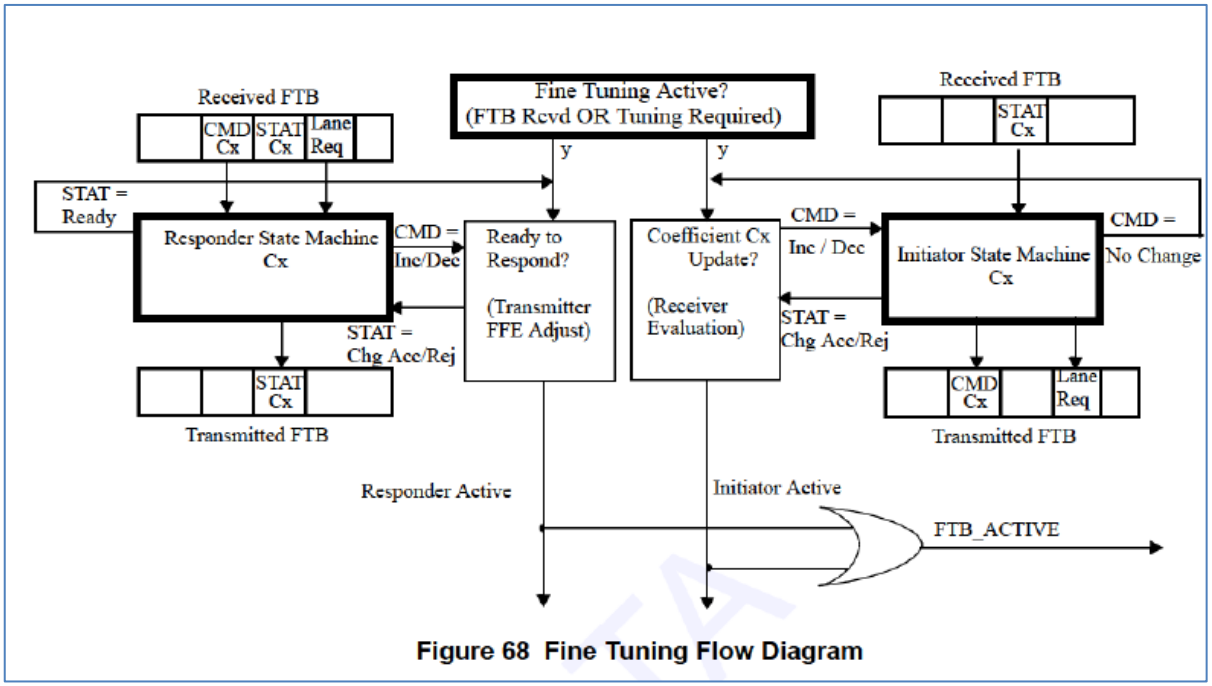
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 14	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 14	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 14	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 14	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 14	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 14	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

US 2003/0058959 (Rafie et al.): Discloses "**FIG. 9** is a block diagram of a calibration system **900** for the pre-equalizer of **FIG. 8**. FIG. illustrates the calibration setup required to generate the tap coefficient values for the pre-equalizer system **800** (**FIG. 8**)."

Rafie, paragraph 83.

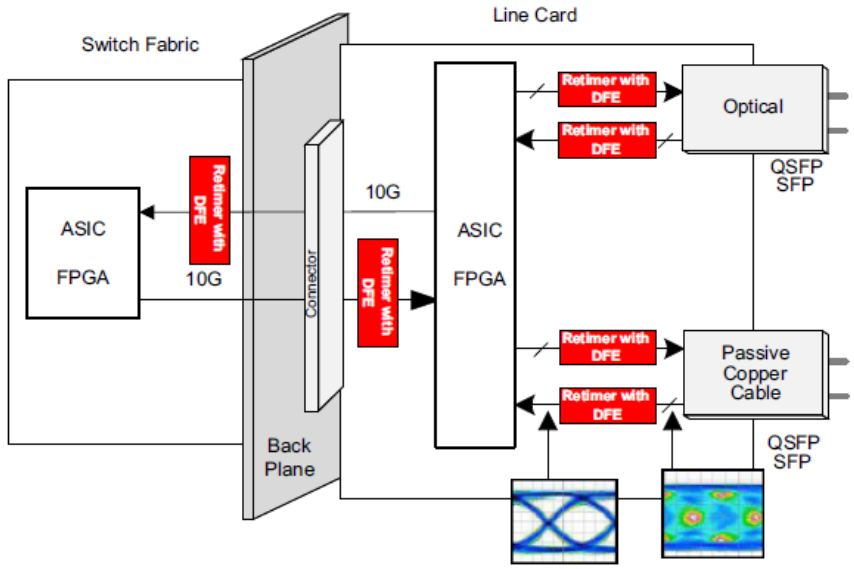
"The pre-equalizer **1008** tap coefficients can be updated through the tap coefficient memory **1026**.".

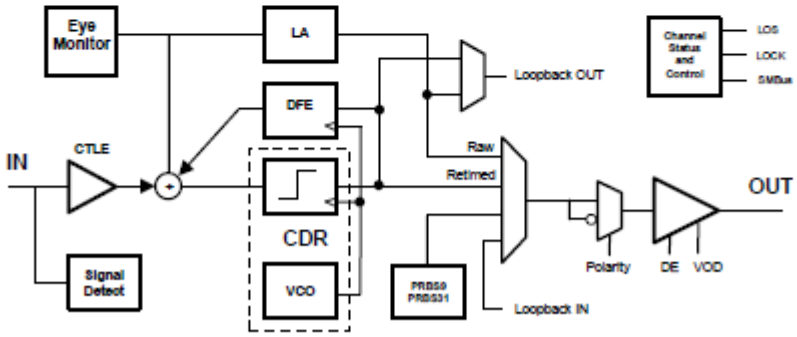
Rafie, paragraph 90.

Claim 14	Disclosure
	"For instance, the transmitter device can be configured to select a first path to adaptively initialize the coefficients before data is transmitted and a second path to continuously adjust the coefficients while data is being transmitted. More particularly, the processing control logic **102** can be configured to select the presence transition equalization path **114** when there are presence change events for the RF carrier signal (e.g., events corresponding to when the RF carrier signal transitions between being present and being absent on the antenna **106**). Once data is being transmitted, with pre-equalization using the coefficients generated by path **114**, the processing control logic **102** can select the adaptive feedback equalization path **112**, which can include logic circuitry that is configured to continuously adjust the coefficients based upon feedback received from the antenna relative to the updated coefficients." Ciacci 4:39-54. <u>*U.S. Patent Publication No. 2014/0281067 ("Das Sharma")*</u> Das Sharma discloses that host port transceiver generates updates for the coefficient values. *See, e.g.*, Das Sharma at [0078], [0193], Figure 5. Das Sharma discloses that the channel's receive side (e.g., receiving training signals) determined updated equalization coefficients, which it transferred to the transmitter side. *See, e.g.*, Das Sharma at [0078], [0193], Figure 5.

Claim 14	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 14	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 14	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 14	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 14	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 14	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

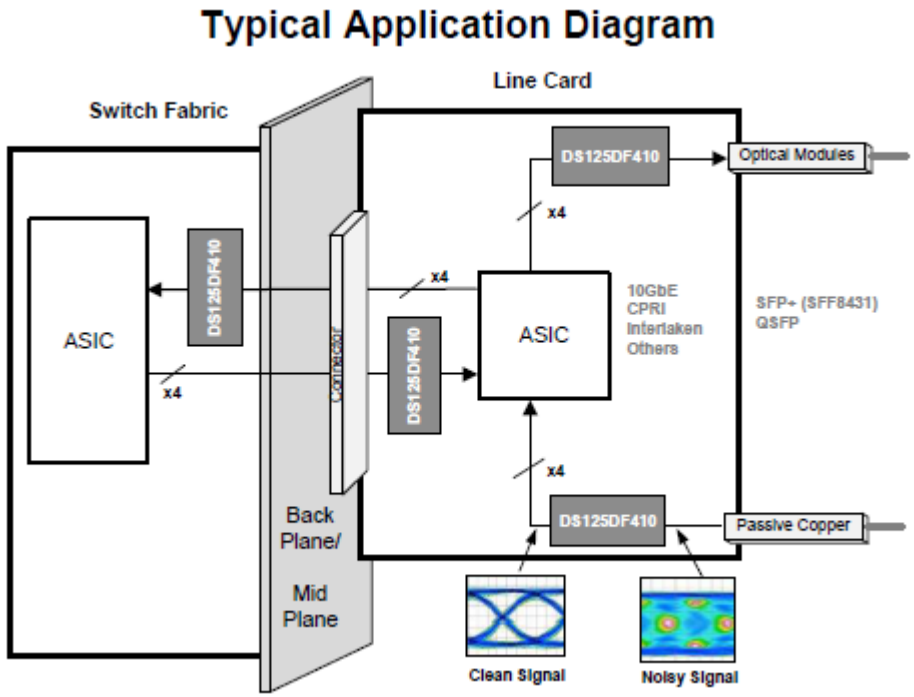
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

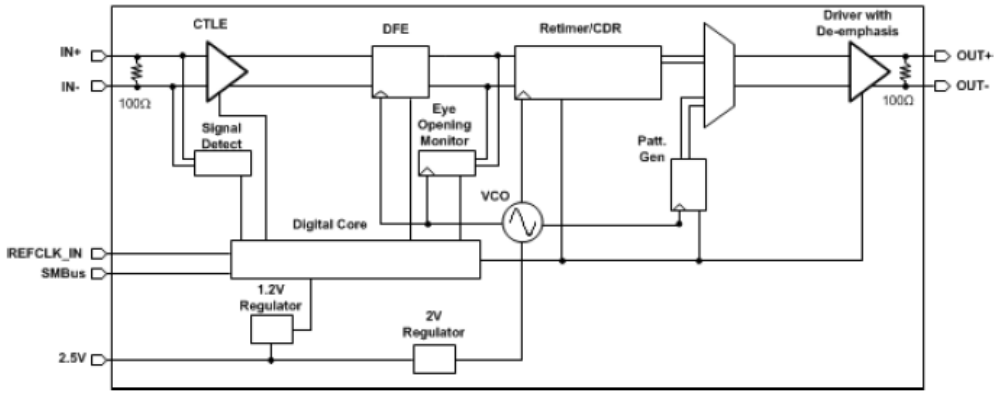
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 14	Disclosure
	 TI DS125DF410, 1.

Claim 14	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 14	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 14	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 14	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 14	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 14	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 14	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 14	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 14	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

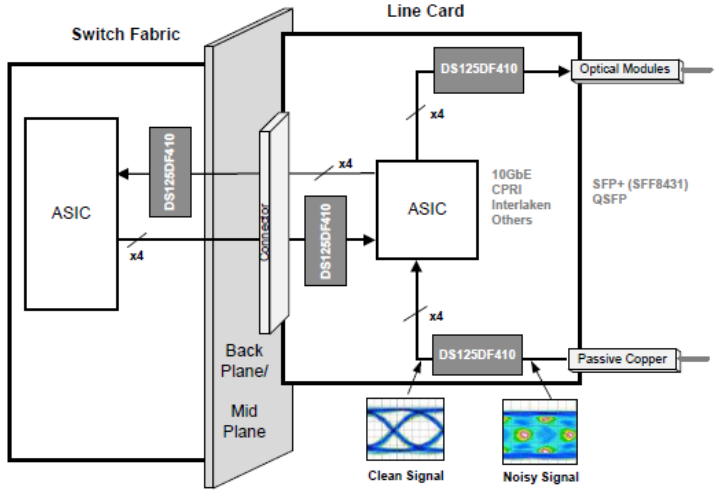
TI DS125DF410, 41.

Claim 14	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 14	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 14	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

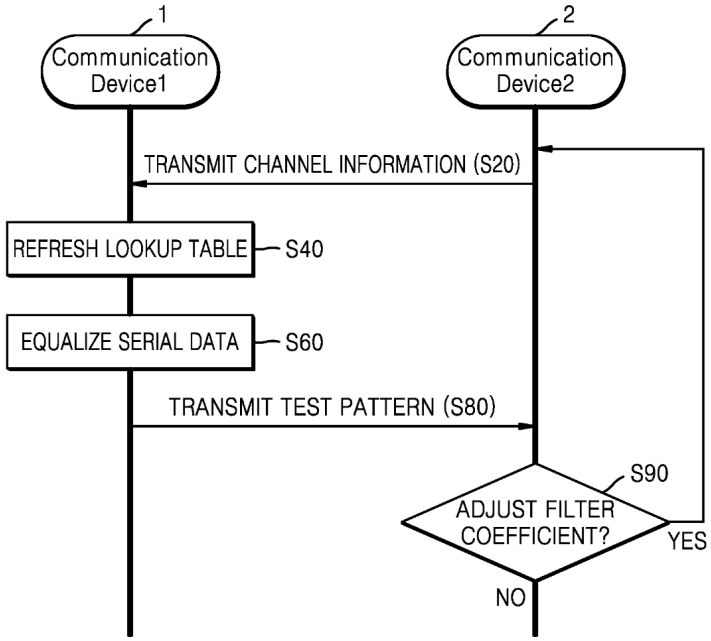
Claim 14	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

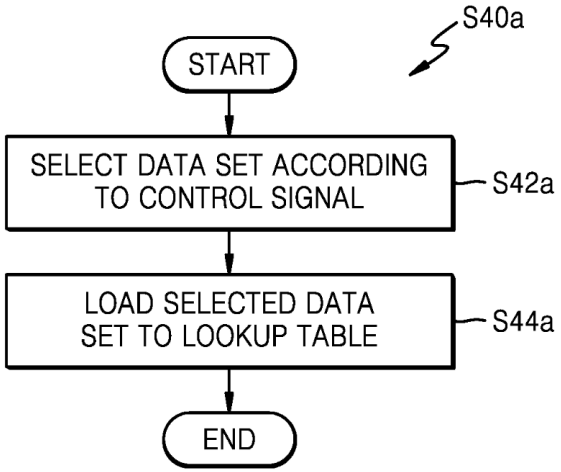
O. DEPENDENT CLAIM 15

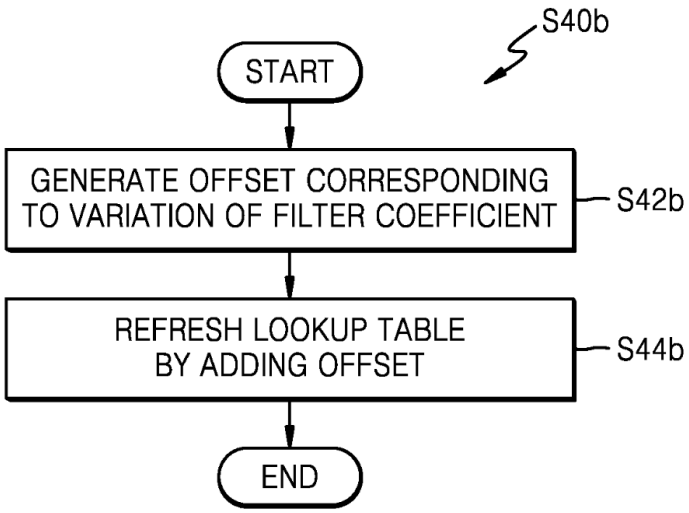
Claim 15	Disclosure
15. The communications link of claim 14, wherein the controller saves updated coefficient values in one of the registers.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "FIG. 10 is a diagram illustrating an equalization method over time according to an exemplary embodiment of the disclosure. For example, the equalization method of FIG. 10 may be performed by the first communication device 1 including the TX equalizer 12 of FIG. 1 and the second communication device 2 communicating with the first communication device 1. The filter coefficients for equalization may be determined according to the equalization method illustrated in FIG. 10, and the method for determining the filter coefficients may be referred to as training of filter coefficients. It is assumed below that the first communication device 1 of FIG. 10 includes the components of the communication device 5 of FIG. 1, and FIG. 10 will be described with reference to FIG. 1. Referring to FIG. 10, in operation S20, the second communication device 2 may transmit channel information. For example, the second communication device 2 may first transmit, to the first communication device 1, channel information including information indicating one of the plurality of data sets, as described above with reference to FIG. 3. In operation S40, the first communication device 1 may refresh the lookup table LUT. For example, the protocol processor 30 of the first communication device 1 may extract information indicating a data set from the channel information received in operation S20 and may transmit the control signal CTRL

Claim 15	Disclosure
	including the extracted information to the TX equalizer 12. TX equalizer 12 may refresh the lookup table LUT based on the control signal CTRL. The lookup table LUT may include values of the digital signal DSIG corresponding to possible values of the symbol sequence extracted from the serial data SER. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information indicating a data set will be described with reference to FIG. 11. In operation S60, the first communication device 1 may equalize the serial data SER. For example, in the TX equalizer 12 of the first communication device 1, the lookup table LUT may output a digital signal (e.g., DSIG in FIG. 3) corresponding to the symbol sequence of the serial data SER, and the DAC 200 included in the TX equalizer 12 may convert the digital signal into an analog signal. Accordingly, an adder and a multiplier for multiplication and addition between the symbol sequence and the filter coefficient sequence for implementing the FIR filter 9 of FIG. 2 may be omitted. The example of operation S60 will be described with reference to FIG. 14. In operation S80, the first communication device 1 may transmit a test pattern. For example, the test pattern may include a pattern previously shared by the first communication device 1 and the second communication device 2, and the second communication device 2 may receive the test pattern through a channel (e.g., 7 of FIG. 1). In operation S90, the second communication device 2 may determine whether to adjust the filter coefficient. For example, the second communication device 2 may evaluate the test pattern received from the first communication device 1 and determine whether to adjust at least one of the coefficients of the FIR filter used for equalization of the first communication device 1 according to the evaluation result. As illustrated in FIG. 10, when it is determined not to adjust at least one of the filter coefficients, the training of the filter coefficients may be terminated and the first communication device 1 may transmit the signal, which is equalized according to the current filter coefficients, to the second communication device 2. On the other hand, when it is determined to adjust at least one of the filter coefficients, operation S20 may be performed. Unlike the initially performed operation S20, in operation S20, which is performed after operation S90, the second communication device 2 may transmit channel information, which includes information on the variation of the filter coefficients, to the first communication device 1. Thereafter, unlike the initially performed operation S40, in operation S40, the first communication device 1 may refresh the lookup table LUT based on the information on the variation of the filter coefficients. An example of operation S40 of

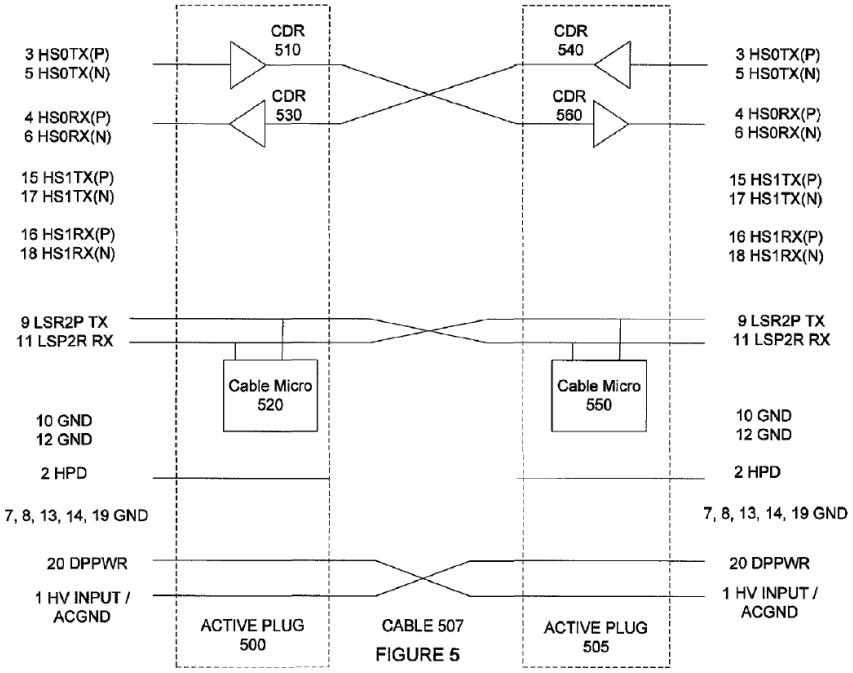
Claim 15	Disclosure
	refreshing the lookup table LUT in response to channel information including information on the variation of the filter coefficients will be described with reference to FIG. 12." Kang, 11:62-13:6 FIG. 10  Kang, FIG. 10 "Referring to FIG. 11, operation S**40** *a* may include operations S**42** *a* and S**44** *a*. In operation S**42** *a*, an operation of selecting a data set according to the control signal CTRL may be performed. For example, the controller **110** of FIG. 3 may receive a control signal CTRL including information indicating one of k

Claim 15	Disclosure
	filter coefficient sequences and may control the data storage **120** to output one of first to k-th data sets SET**1** to SETk, which are stored in the data storage **120**, according to the control signal CTRL. In operation S**44** *a*, an operation of loading the selected data set into the lookup table **130** may be performed. For example, the controller **110** may control the data storage **120** and the lookup table **130** to store the second value VAL**2** outputted from the data storage **120** in the lookup table **130**. Referring to FIG. 12, operation S**40** *b* may include operations S**42** *b* and S**44** *b*. In operation S**42** *b*, an operation of generating an offset OFF corresponding to the variation of the filter coefficients may be performed. For example, the offset generator **150** of FIG. 6 may generate an offset OFF, based on the variation signal VAR and the index IDX provided from the controller **110′**. The variation signal VAR may indicate at least one of up, down, hold, and reset of the filter coefficient and may include a variation amount of the filter coefficient. An example of generating the offset OFF when the variation signal VAR indicates the reset of the filter coefficient will be described later with reference to FIG. 13. In operation S**44** *b*, an operation of refreshing the lookup table **130′** may be performed by adding the offset OFF. In some embodiments, the offset generator **150** may generate a positive offset OFF or a negative offset OFF, and thus the calculator **160** may perform an addition. In some embodiments, the offset generator **150** may generate the positive offset OFF, and thus the calculator **160** may perform addition or subtraction according to the control of the controller **110′**. The lookup table **130′** may be refreshed by storing the output value of the calculator **160**, that is, the third value VAL**3**, in the lookup table **130′**." Kang, 13:18-54

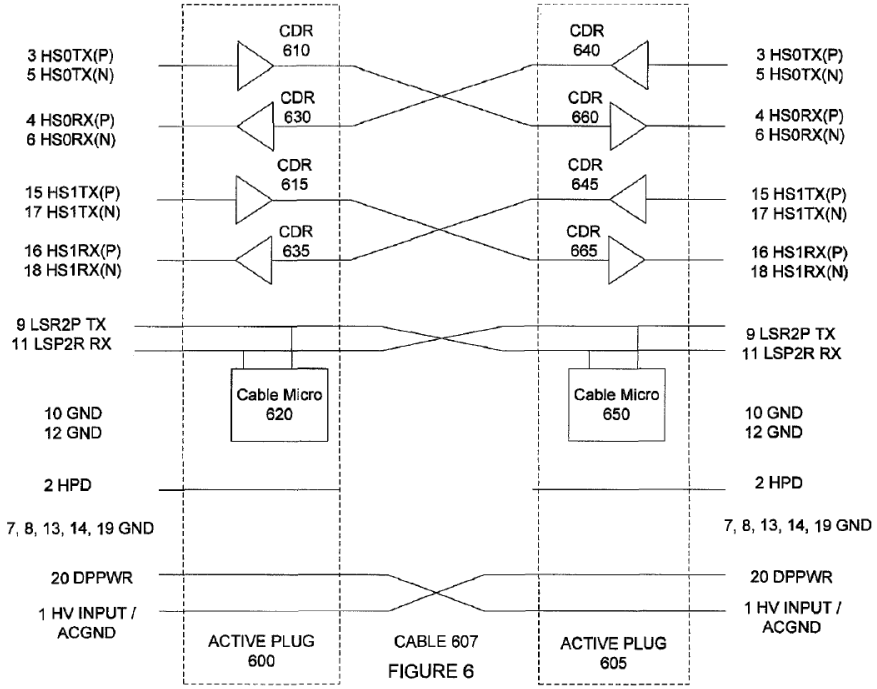
Claim 15	Disclosure
	FIG. 11  Kang, FIG. 11

Claim 15	Disclosure
	FIG. 12  Kang, FIG. 12 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**. Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**.

Claim 15	Disclosure
	The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables. In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used.

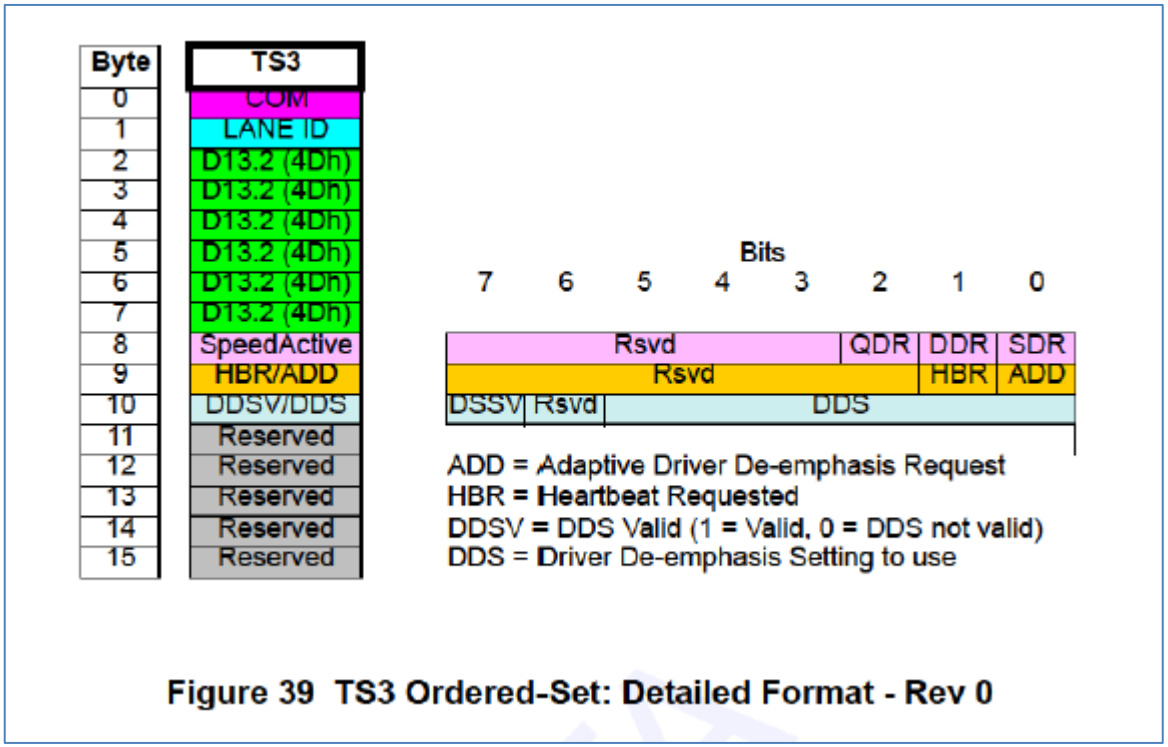
Claim 15	Disclosure
	In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5 "FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock

Claim 15	Disclosure
	and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 15	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 15	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 15	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 15	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

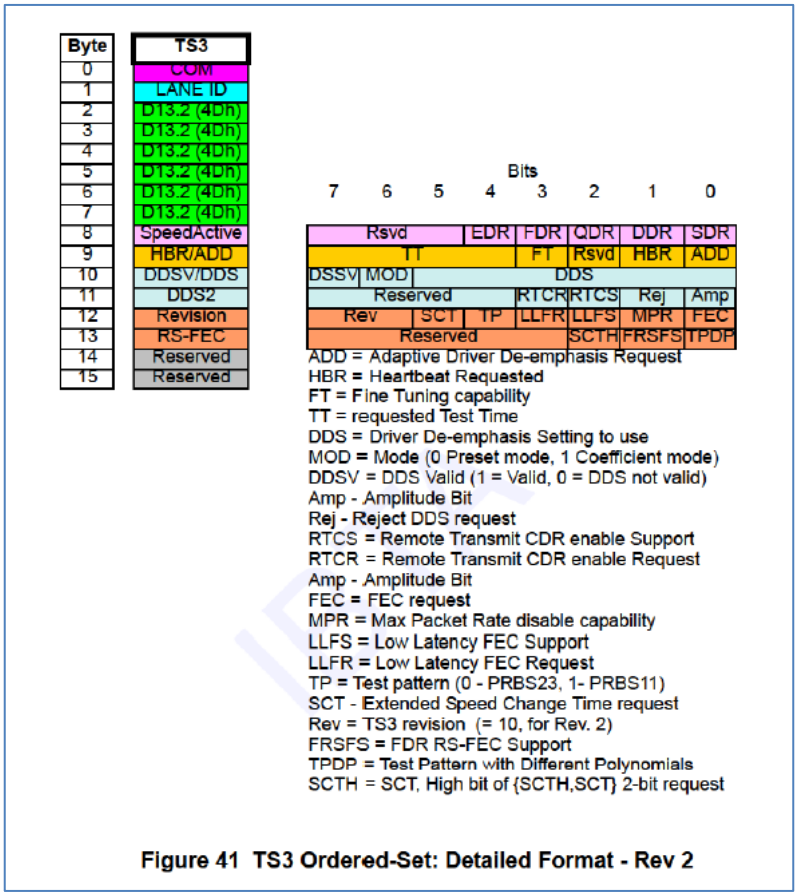
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 15	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits	7	6	5	4	3	2	1	0
	Rsvd			EDR	FDR	QDR	DDR	SDR
	TT				FT	Rsvd	HBR	ADD
	DSSV	MOD	DDS					
	Reserved				RTCR	RTCS	Rej	Amp
	Rev		SCT	TP	LLFR	LLFS	MPR	FEC
	Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 15	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 15	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 15	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 15	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 15	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 15	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 15	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

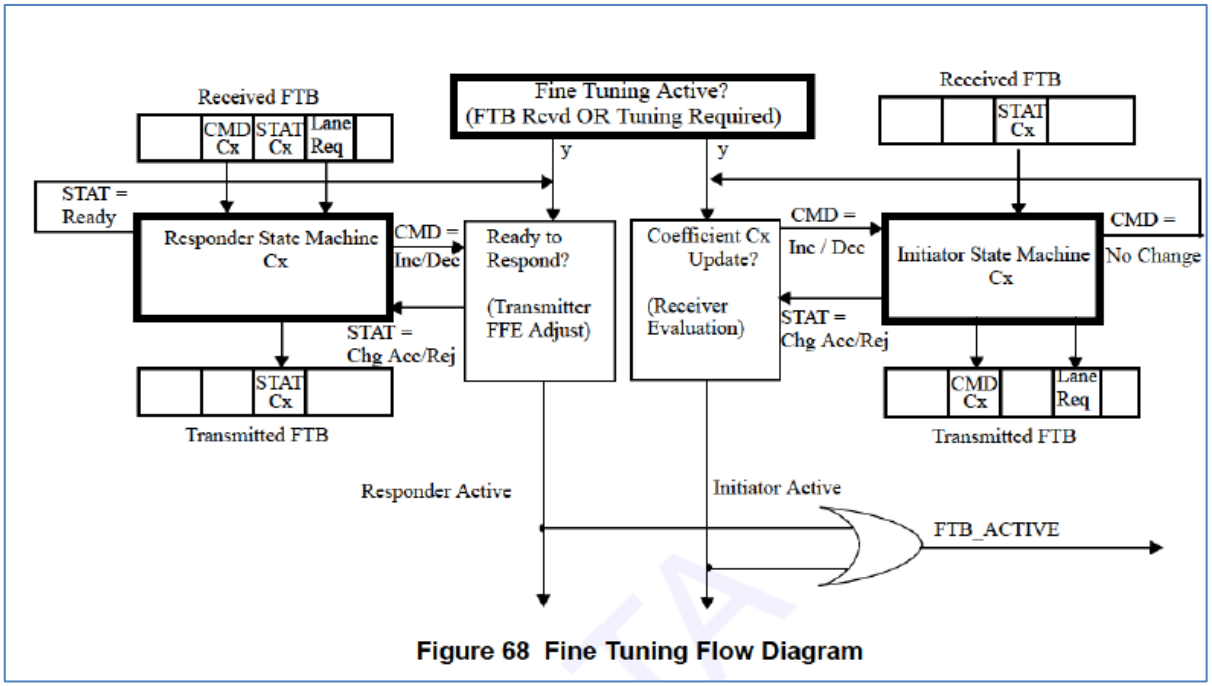
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 15	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 15	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 15	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 15	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 15	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 15	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"For instance, the transmitter device can be configured to select a first path to adaptively initialize the coefficients before data is transmitted and a second path to continuously adjust the coefficients while data is being transmitted. More particularly, the processing control logic **102** can be configured to select the presence transition equalization path **114** when there are presence change events for the RF carrier signal (e.g., events corresponding to when the RF carrier signal transitions between being present and being absent on the antenna **106**). Once data is being transmitted, with pre-equalization using the coefficients generated by path **114**, the processing control logic **102** can select the adaptive feedback equalization path **112**, which can include logic circuitry that is configured to continuously adjust the coefficients based upon feedback received from the antenna relative to the updated coefficients."

Claim 15	Disclosure
	Ciacci, 4:39-54. "Once frequency response of front-end components has been characterized, this information can be stored in the digital base band on a configuration register (CFR), and thereby used to specify gain coefficients of the digital pre-equalizer." Balakrishnan, paragraph 27. *U.S. Patent Publication No. 2014/0281067 ("Das Sharma")* Das Sharma discloses updating coefficient value stored in a register by using a controller. *See, e.g.*, Das Sharm at [0078], [0193].

Claim 15	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 15	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 15	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

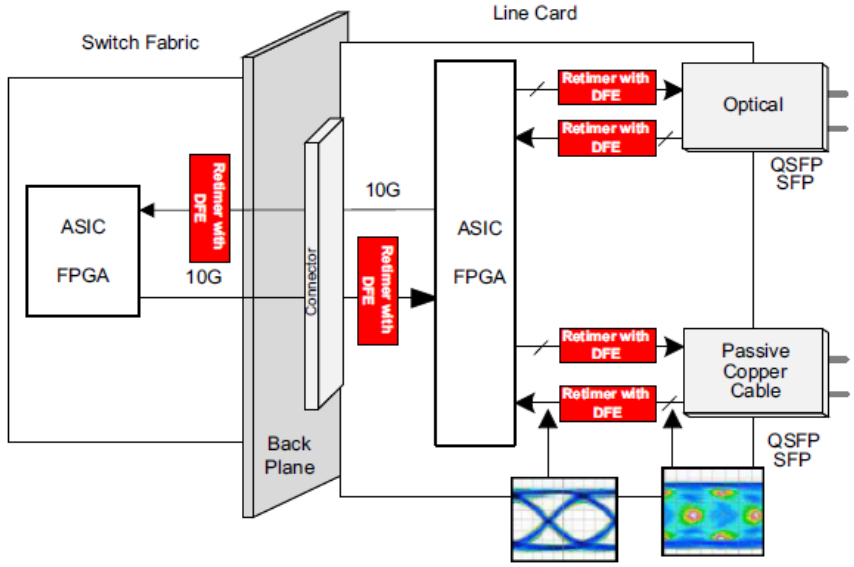
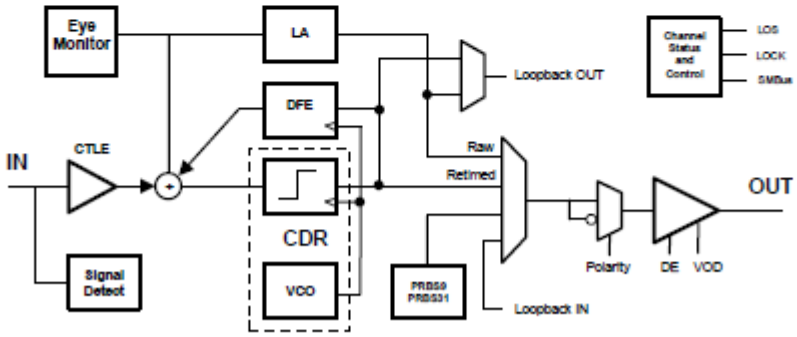


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 15	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 15	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 15	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

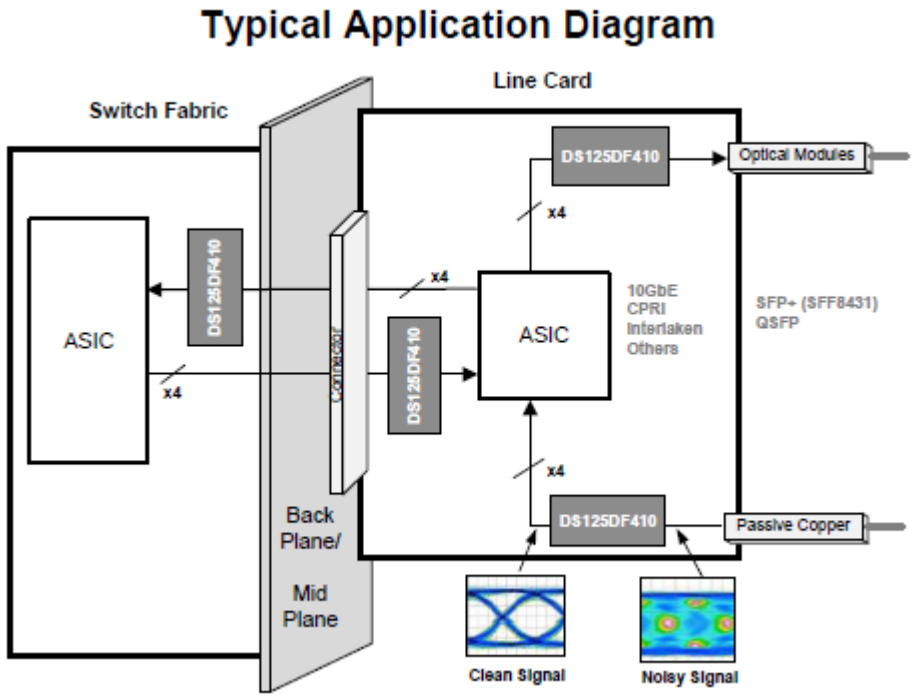
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

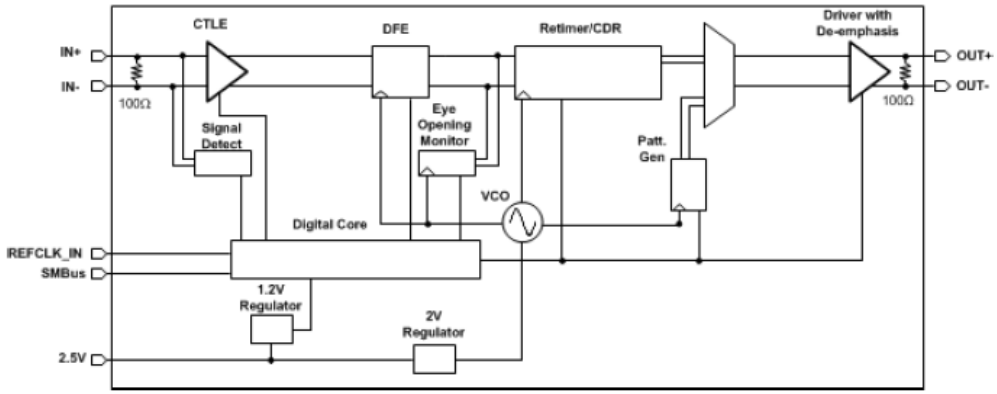
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 15	Disclosure
	 TI DS125DF410, 1.

Claim 15	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 15	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 15	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 15	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 15	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 15	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 15	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 15	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 15	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

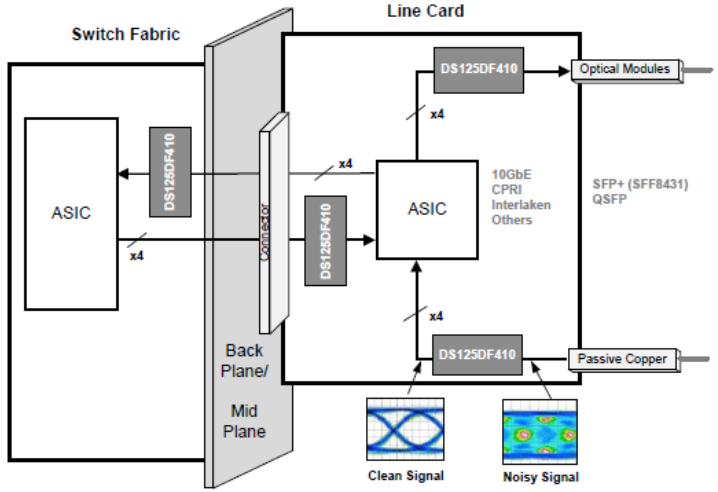
TI DS125DF410, 41.

Claim 15	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 15	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 15	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 15	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

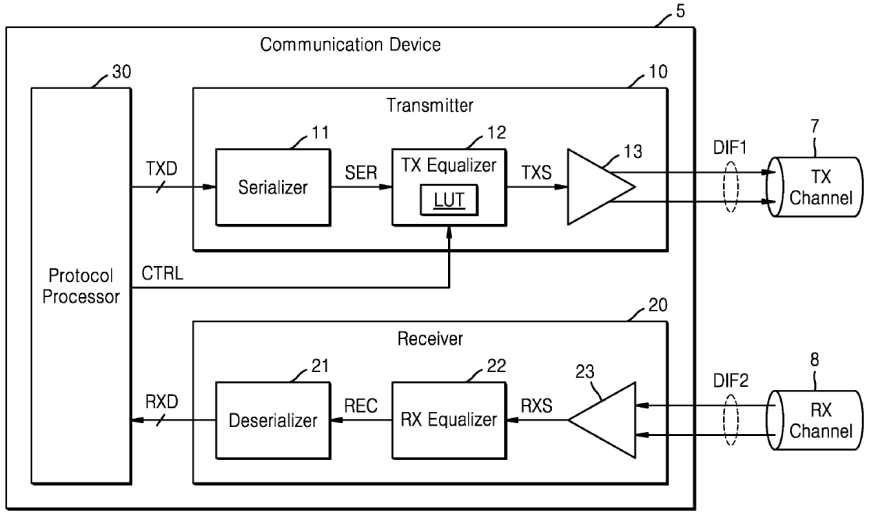
Exhibit C-12

Claim 15	Disclosure

P. INDEPENDENT CLAIM 16

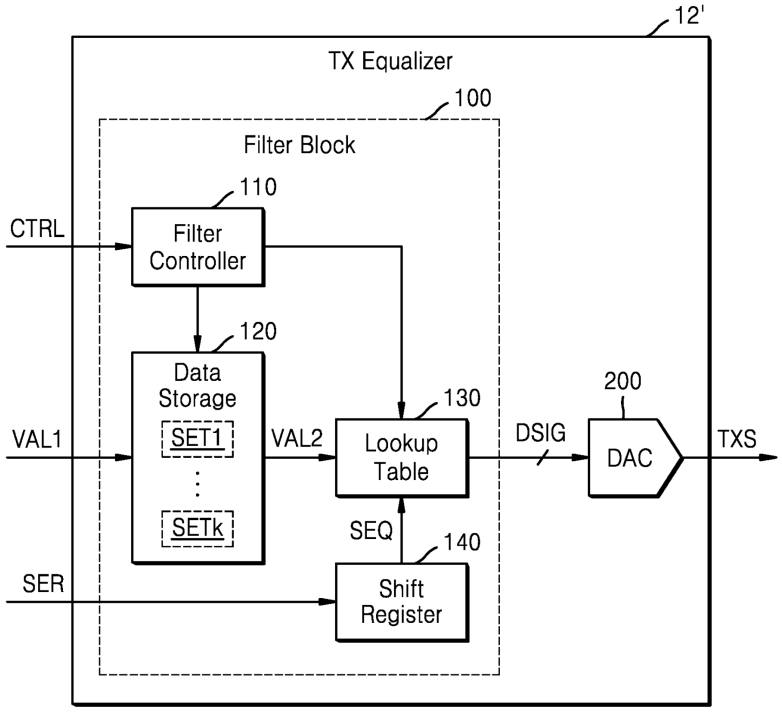
Claim 16	Disclosure
16[pre] A pluggable module transceiver including:	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "The disclosure relates to an equalizer, and more particularly, to an equalizer including a lookup table and a transmitter including the equalizer. In serial communication, an interconnection between a transmitter and a receiver, i.e., a channel, may distort signals. In order to compensate for distortion of signals generated in the channel, the transmitter and/or the receiver may include an equalizer. For example, the equalizer included in the transmitter may include a Finite Impulse Response (FIR) filter that provides an inverse transfer function of the transfer function of the channel. An equalizer including a high complexity filter may be necessary in order to precisely compensate for signal distortion while performing fast signal filtering for high speed serial communication. Further, in order to reduce power consumption and heat generation, an equalizer capable of reducing power consumption may be necessary." Kang, 1:13-30 "FIG. 1 is a block diagram illustrating a communication device **5** according to an exemplary embodiment of the disclosure. As shown in FIG. 1, the communication device **5** is capable of serial communication

Claim 16	Disclosure
	with a counterpart communication device via a TX channel **7** and an RX channel **8**. Although FIG. 1 illustrates that the communication device **5** communicates with the counterpart communication device through a full duplex communication scheme, i.e., two channels (the TX and RX channels **7** and **8**), according to some embodiments, the communication device **5** may communicate with the counterpart communication device through a half duplex communication scheme, i.e., one channel. The TX channel **7** or the RX channel **8** may refer to interconnection between the communication device **5** and the counterpart communication device, and serial data signals DIF**1** and DIF**2** may transfer through the TX channel **7** and the RX channel **8**, respectively. For example, the TX channel **7** or the RX channel **8** may include at least one of a conductive line of an integrated circuit, a pattern of a printed circuit board (PCB), a connector, and a cable. The serial data signals DIF**1** and DIF**2**, which respectively pass through the TX channel **7** and the RX channel **8**, may be differential signals as shown in FIG. 1 in some embodiments, or may be single signals unlike what is illustrated in FIG. 1. The communication device **5** may refer to any device in serial communication with the counterpart communication device via the TX channel **7** and the RX channel **8**. In some embodiments, the communication device **5** may be a die included in a semiconductor package and may be in serial communication with a counterpart communication device included in the same semiconductor package. In some embodiments, the communication device **5** may be a semiconductor package mounted on a PCB and may be in serial communication with the counterpart communication device mounted on the same PCB or mounted on another PCB. In some embodiments, the communication device **5** may be a system (e.g., a storage, a computing system, etc.) including at least one semiconductor package and a PCB and may be in serial communication with other systems. As shown in FIG. 1, the communication device **5** may include a transmitter **10**, a receiver **20**, and a protocol processor **30**. In some embodiments, the transmitter **10** and the receiver **20** may be implemented as one block as a transceiver. The transmitter **10**, the receiver **20**, and the protocol processor **30** may provide a physical layer of communication and may be collectively referred to as a SerDes (serializer/deserializer) for serial communication." Kang, 3:17-65.

Claim 16	Disclosure
	FIG. 1  Kang, FIG. 1

Claim 16	Disclosure

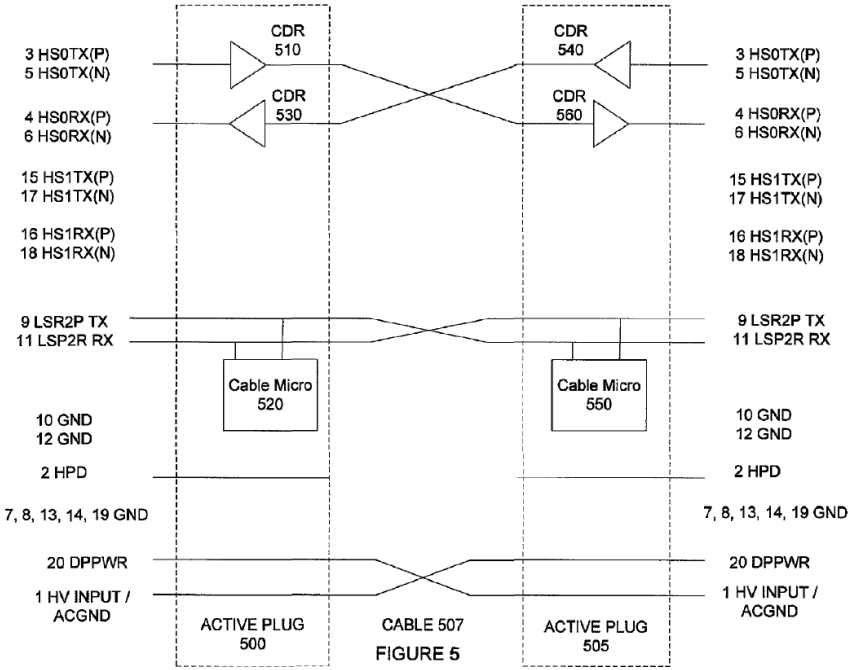
FIG. 3



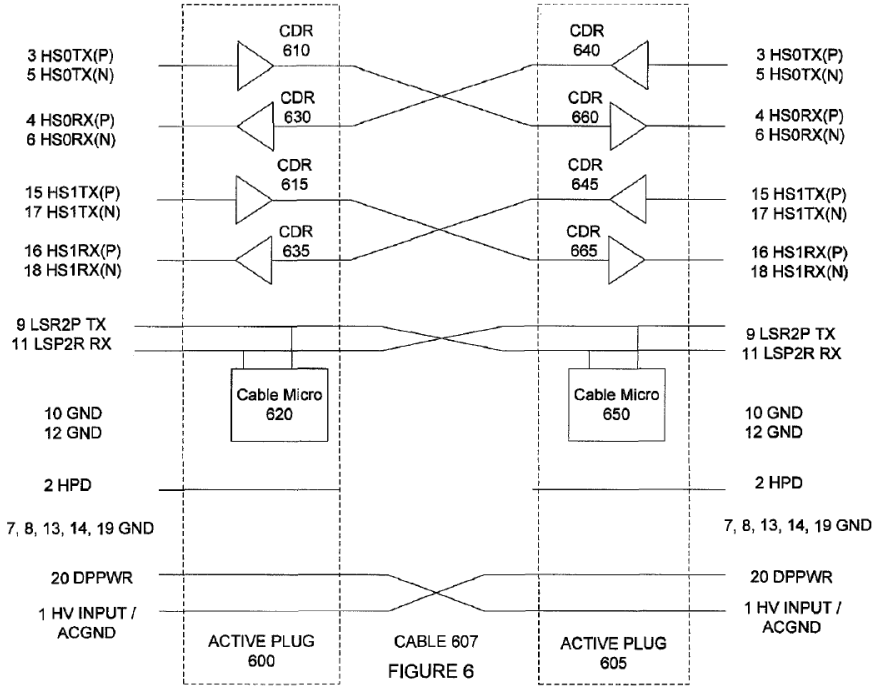
Kang, FIG. 3

"FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 16	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 16	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 16	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 16	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 16	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 16	Disclosure

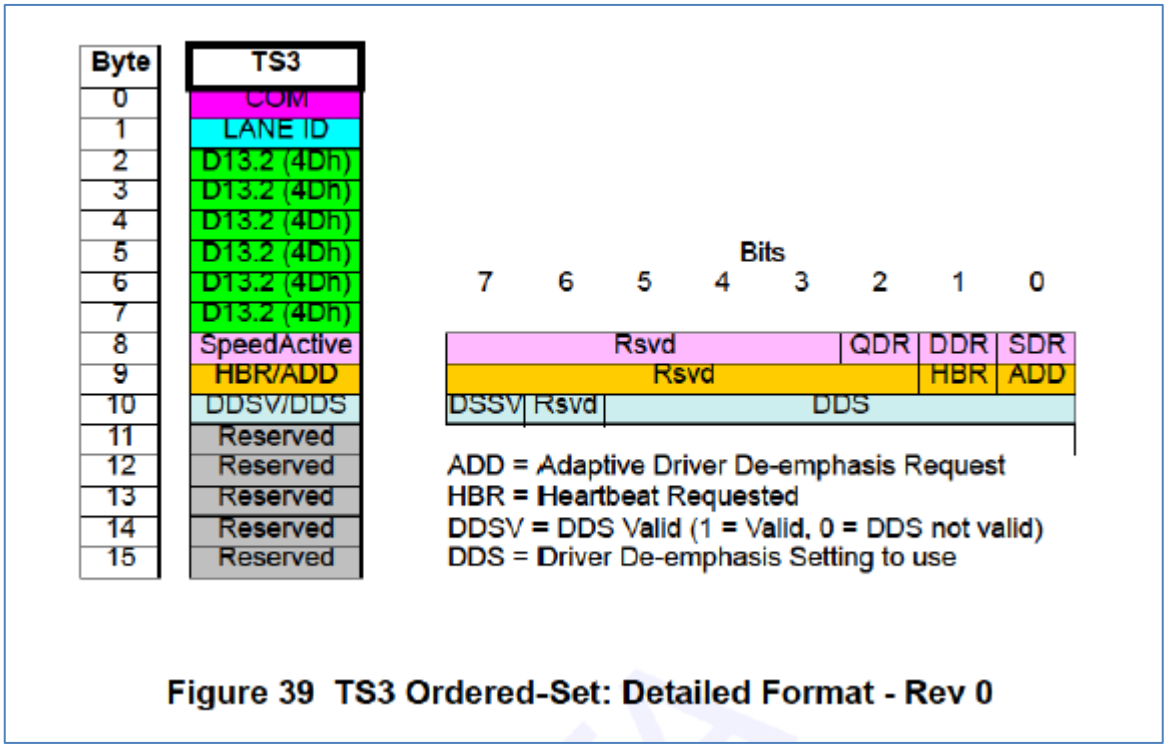
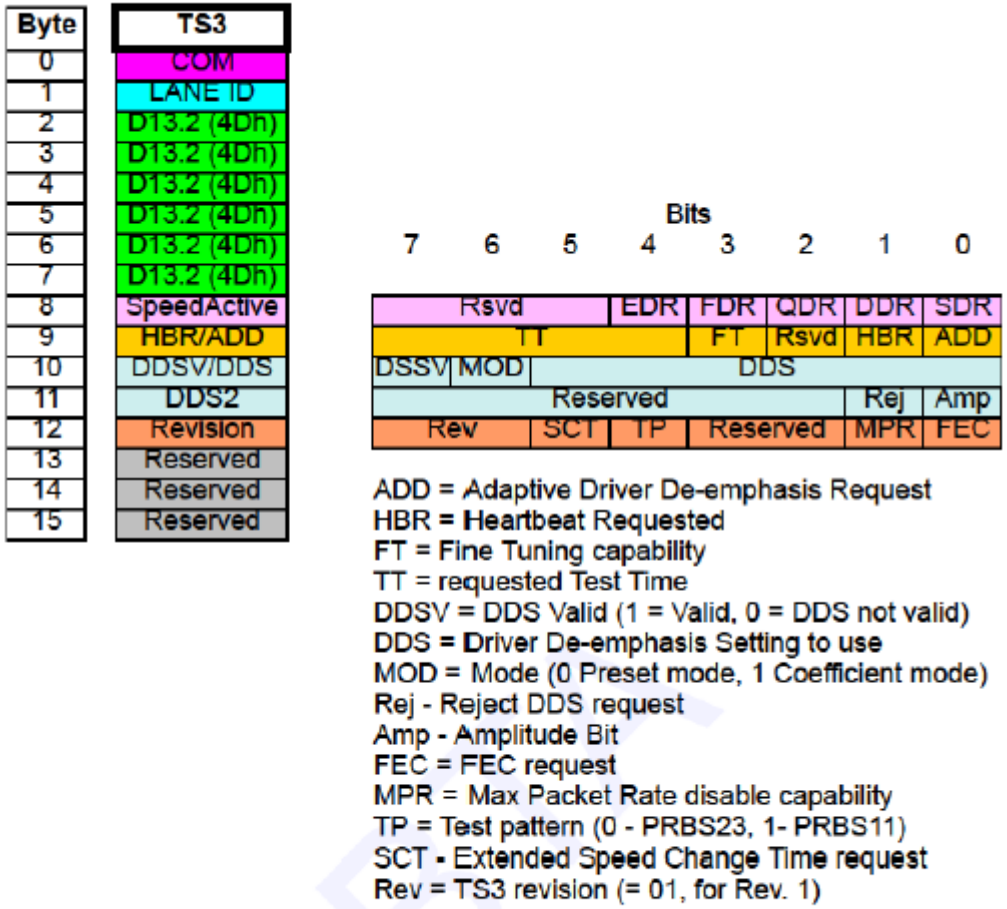


Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 16	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

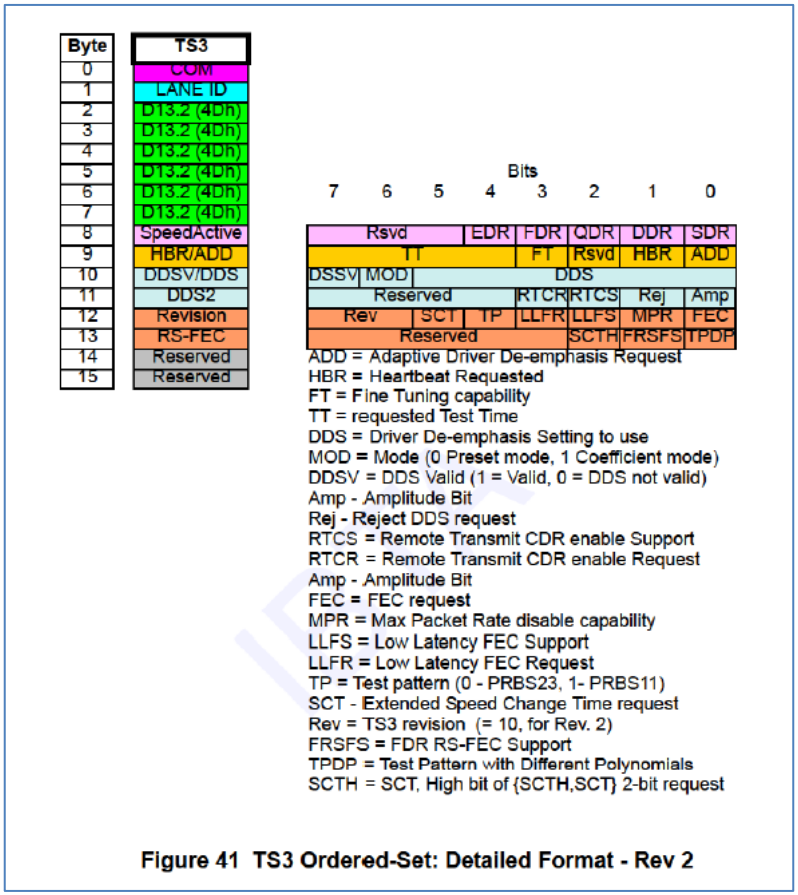
	Bits 7	6	5	4	3	2	1	0
	Rsvd			EDR	FDR	QDR	DDR	SDR
	TT				FT	Rsvd	HBR	ADD
	DSSV	MOD	DDS					
	Reserved						Rej	Amp
	Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 16	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits	7	6	5	4	3	2	1	0
	Rsvd			EDR	FDR	QDR	DDR	SDR
	TT				FT	Rsvd	HBR	ADD
	DSSV	MOD	DDS					
	Reserved				RTCR	RTCS	Rej	Amp
	Rev		SCT	TP	LLFR	LLFS	MPR	FEC
	Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 16	Disclosure

5.5.2.4.1 REV 0 TS3

Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field.

Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR).

InfiniBand, p. 147:34-42

Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283.

Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver.

The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity.

InfiniBand, p. 148:1-13

Claim 16	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 16	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 16	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 16	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 16	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 16	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

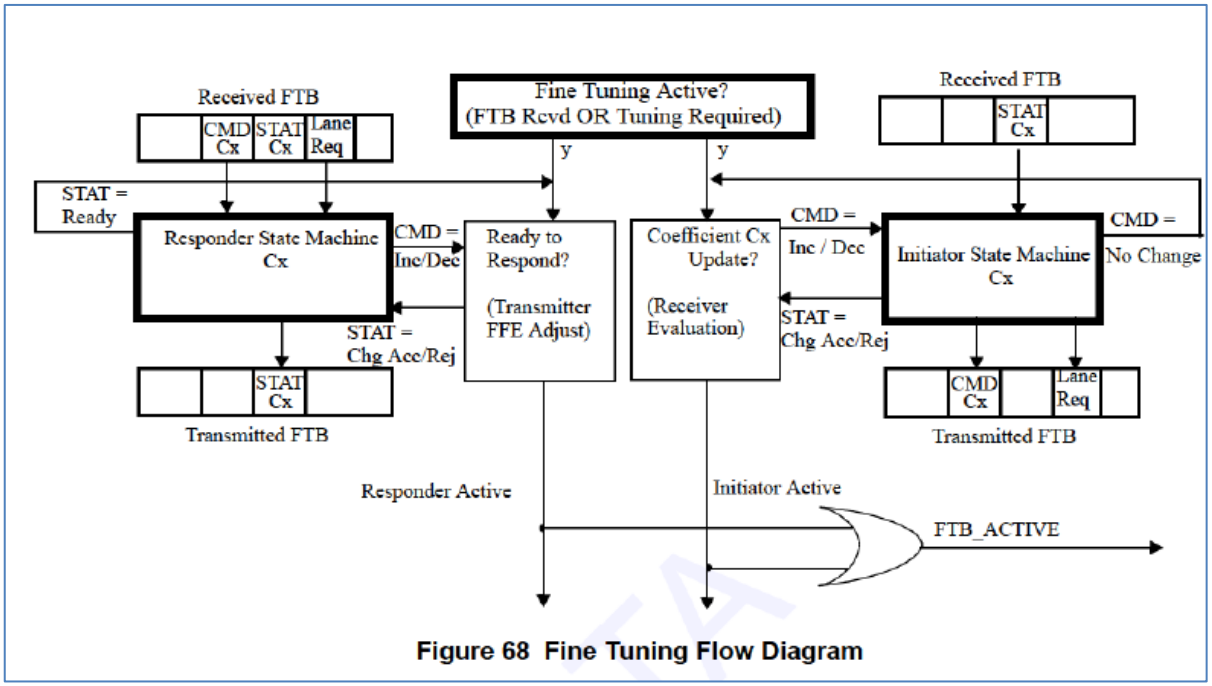
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 16	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 16	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 16	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 16	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 16	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 16	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

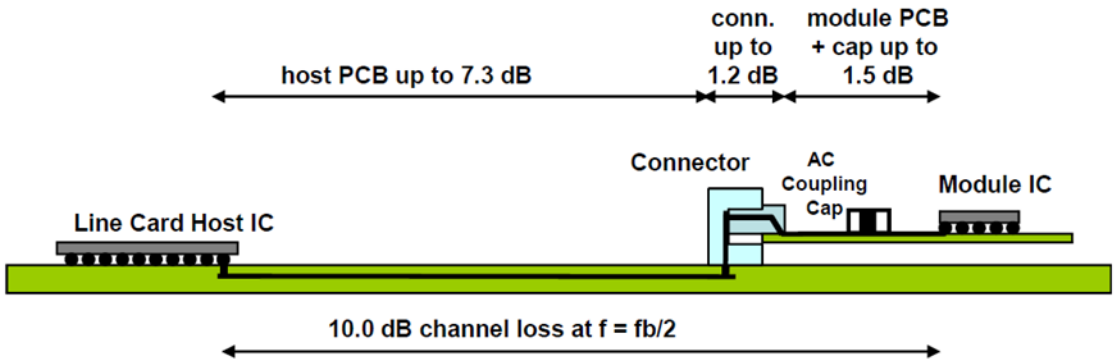
Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"To provide a high-performance radio link for high-speed systems employing spectrally-efficient modulation schemes, a reliable and robust transmitter radio link is required. Present embodiments of the current invention perform signal processing techniques to enhance the system performance and robustness of the transmitter portion of the transceiver."

Rafie, paragraph 47.

"Various embodiments are directed toward a communication device that includes a transceiver circuit that is configured to communicate by generating an RF carrier signal of around 13.56 MHz as consistent with various RFID technologies, such as ISO/IEC standard 14443."

Claim 16	Disclosure
	Ciacci, 3:63-67. *United States Patent No. 7,239,665 ("Mezer")* Mezer describes supporting Ethernet, and such standards-compliant implementation was conventional. *See, e.g.*, at Mezer, 4:55-57, 6:62-7:3. This obvious implementation would have met the Ethernet standard's description of a chip-to-module communication link comprising a port connector coupling a port transceiver to a pluggable module transceiver. *See, e.g.*, IEEE 802.3bs-2017, 323-330 (Annex 120C), 350-372 (Annex 120E), 350 ("The chip-to-module interface is defined using a specification… that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0"); *see also* OIF-CEI-04.0, 334, Fig. 16-15 (below, showing a "Connector" receiving a pluggable module). **Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model** 

PCIe 3.1a

1.3. PCI Express Fabric Topology

A fabric is composed of point-to-point Links that interconnect a set of components – an example fabric topology is shown in Figure 1-2. This figure illustrates a single fabric instance referred to as a hierarchy – composed of a Root Complex (RC), multiple Endpoints (I/O devices), a Switch, and a PCI Express to PCI/PCI-X Bridge, all interconnected via PCI Express Links.

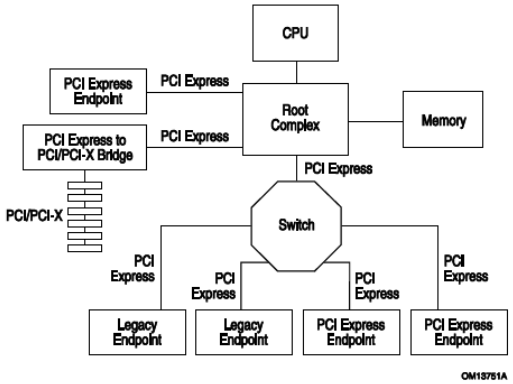


Figure 1-2: Example Topology

1.3.1. Root Complex

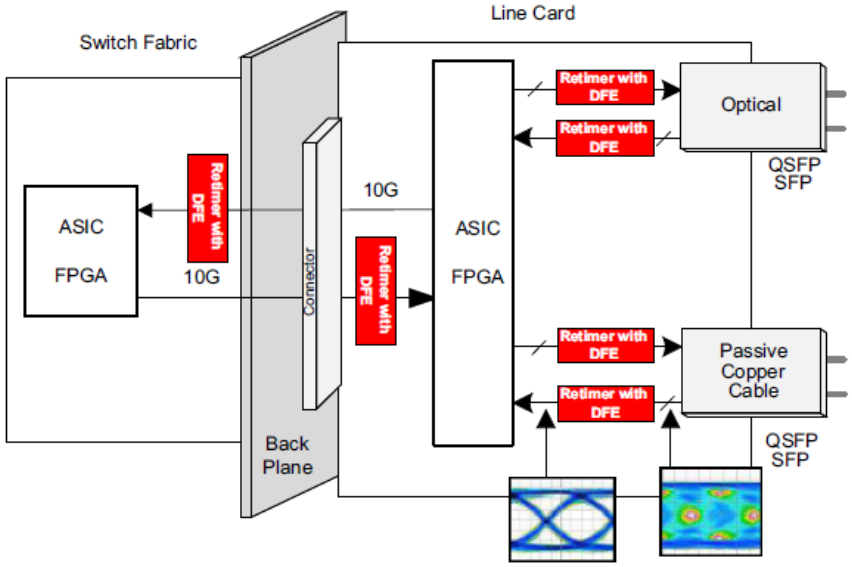
- A Root Complex (RC) denotes the root of an I/O hierarchy that connects the CPU/memory subsystem to the I/O.
- As illustrated in Figure 1-2, a Root Complex may support one or more PCI Express Ports. Each interface defines a separate hierarchy domain. Each hierarchy domain may be composed of a single Endpoint or a sub-hierarchy containing one or more Switch components and Endpoints.
- The capability to route peer-to-peer transactions between hierarchy domains through a Root Complex is optional and implementation dependent. For example, an implementation may incorporate a real or virtual Switch internally within the Root Complex to enable full peer-to-peer support in a software transparent way.

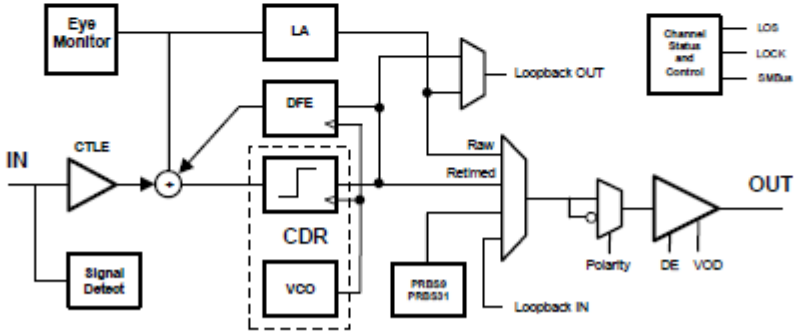
  Unlike the rules for a Switch, a Root Complex is generally permitted to split a packet into smaller packets when routing transactions peer-to-peer between hierarchy domains (except as noted below), e.g., split a single packet with a 256-byte payload into two packets of 128 bytes payload each. The resulting packets are subject to the normal packet formation rules contained in this specification (e.g., Max_Payload_Size, Read Completion Boundary, etc.). Component designers should note that splitting a packet into smaller packets may have negative performance

Claim 16	Disclosure
	consequences, especially for a transaction addressing a device behind a PCI Express to PCI/PCI-X bridge. Exception: A Root Complex that supports peer-to-peer routing of Vendor_Defined Messages is not permitted to split a Vendor_Defined Message packet into smaller packets except at 128-byte boundaries (i.e., all resulting packets except the last must be an integral multiple of 128 bytes in length) in order to retain the ability to forward the Message across a PCI Express to PCI/PCI-X Bridge. Refer to the *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0* for additional information. ❑ A Root Complex must support generation of configuration requests as a Requester. ❑ A Root Complex is permitted to support the generation of I/O Requests as a Requester. o A Root Complex is permitted to generate I/O Requests to either or both of locations 80h and 84h to a selected Root Port, without regard to that Root Port's PCI Bridge I/O decode configuration; it is recommended that this mechanism only be enabled when specifically needed. ❑ A Root Complex must not support Lock semantics as a Completer. ❑ A Root Complex is permitted to support generation of Locked Requests as a Requester. PCIe 3.1 at 50-51.

Claim 16	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 16	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 16	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 16	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 16	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 16	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

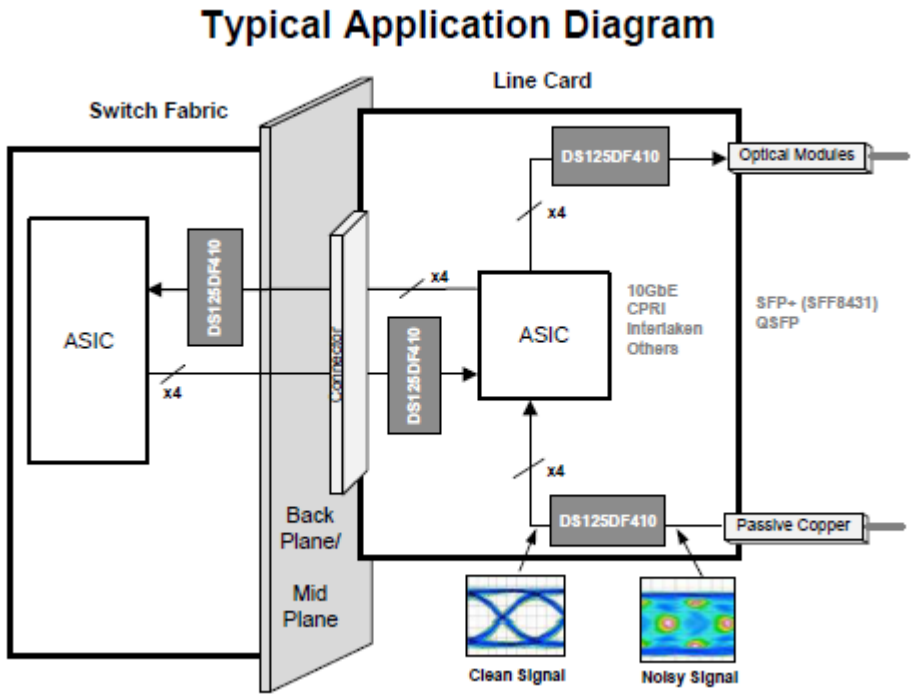
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

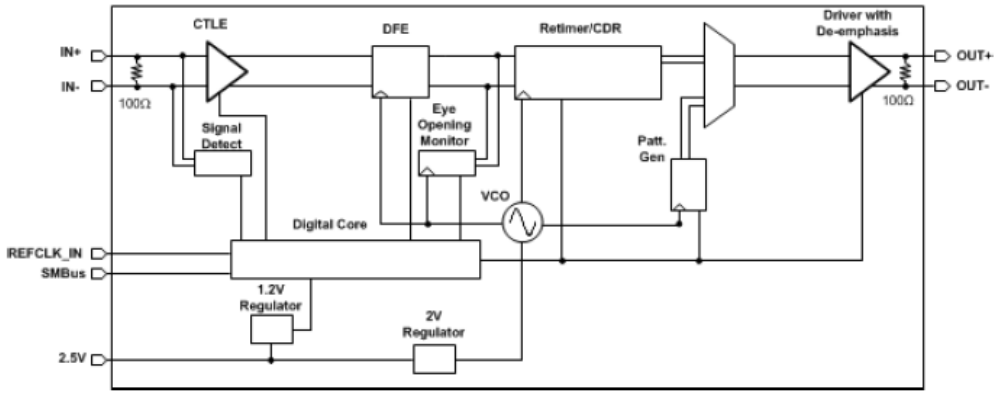
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 16	Disclosure
	 TI DS125DF410, 1.

Claim 16	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 16	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 16	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 16	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 16	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 16	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

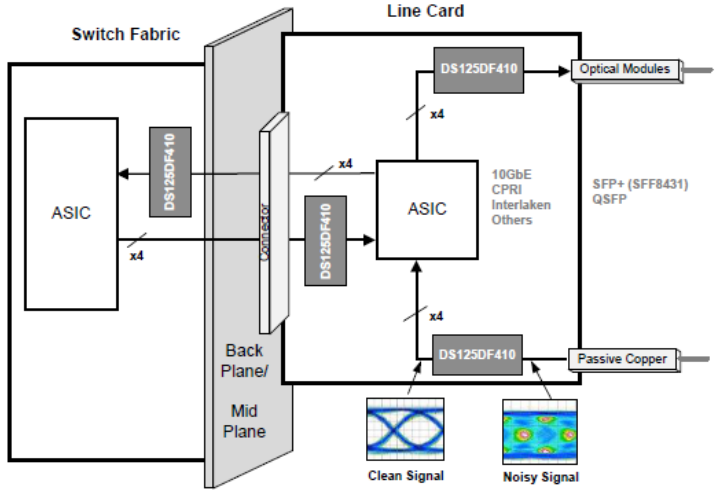
TI DS125DF410, 41.

Claim 16	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 16	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 16	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

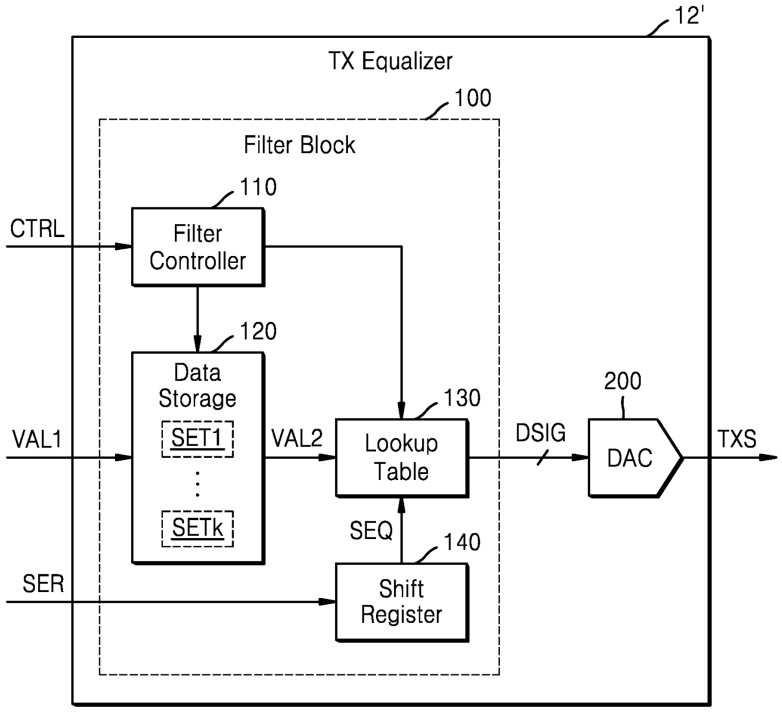
Claim 16	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Claim 16	Disclosure
16[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to a port transceiver; and	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**." Kang, 5:20-42.

Claim 16	Disclosure
	"FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS, which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3.

Claim 16	Disclosure
	The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively.

Claim 16	Disclosure
	The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

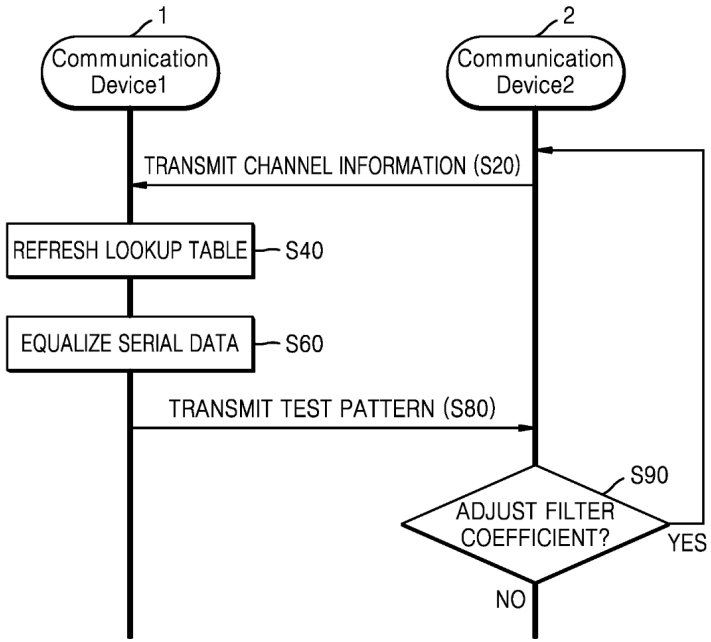
Claim 16	Disclosure
	FIG. 3  Kang, FIG. 3 "An integrated circuit for generating an equalized signal, according to a channel, from serial data includes a shift register that extracts a symbol sequence from the serial data. A data storage stores values of an equalized digital signal corresponding to potential symbol sequences corresponding to a filter coefficient sequence. A lookup table outputs the equalized digital signal of a value corresponding to the extracted symbol sequence. A digital-to-analog converter (DAC) converts the equalized digital signal into the

Claim 16	Disclosure
	equalized signal. A controller refreshes the lookup table, based on at least one of values stored in the data storage and values included in the lookup table, in response to a control signal." Kang, Abstract "FIG. 10 is a diagram illustrating an equalization method over time according to an exemplary embodiment of the disclosure. For example, the equalization method of FIG. 10 may be performed by the first communication device 1 including the TX equalizer 12 of FIG. 1 and the second communication device 2 communicating with the first communication device 1. The filter coefficients for equalization may be determined according to the equalization method illustrated in FIG. 10, and the method for determining the filter coefficients may be referred to as training of filter coefficients. It is assumed below that the first communication device 1 of FIG. 10 includes the components of the communication device 5 of FIG. 1, and FIG. 10 will be described with reference to FIG. 1. Referring to FIG. 10, in operation S20, the second communication device 2 may transmit channel information. For example, the second communication device 2 may first transmit, to the first communication device 1, channel information including information indicating one of the plurality of data sets, as described above with reference to FIG. 3. In operation S40, the first communication device 1 may refresh the lookup table LUT. For example, the protocol processor 30 of the first communication device 1 may extract information indicating a data set from the channel information received in operation S20 and may transmit the control signal CTRL including the extracted information to the TX equalizer 12. TX equalizer 12 may refresh the lookup table LUT based on the control signal CTRL. The lookup table LUT may include values of the digital signal DSIG corresponding to possible values of the symbol sequence extracted from the serial data SER. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information indicating a data set will be described with reference to FIG. 11. In operation S60, the first communication device 1 may equalize the serial data SER. For example, in the TX equalizer 12 of the first communication device 1, the lookup table LUT may output a digital signal (e.g., DSIG in FIG. 3) corresponding to the symbol sequence of the serial data SER, and the DAC 200 included in the TX equalizer 12 may convert the digital signal into an analog signal. Accordingly, an adder and a multiplier for multiplication and addition between the symbol sequence and the filter coefficient

Claim 16	Disclosure
	sequence for implementing the FIR filter 9 of FIG. 2 may be omitted. The example of operation S60 will be described with reference to FIG. 14. In operation S80, the first communication device 1 may transmit a test pattern. For example, the test pattern may include a pattern previously shared by the first communication device 1 and the second communication device 2, and the second communication device 2 may receive the test pattern through a channel (e.g., 7 of FIG. 1). In operation S90, the second communication device 2 may determine whether to adjust the filter coefficient. For example, the second communication device 2 may evaluate the test pattern received from the first communication device 1 and determine whether to adjust at least one of the coefficients of the FIR filter used for equalization of the first communication device 1 according to the evaluation result. As illustrated in FIG. 10, when it is determined not to adjust at least one of the filter coefficients, the training of the filter coefficients may be terminated and the first communication device 1 may transmit the signal, which is equalized according to the current filter coefficients, to the second communication device 2. On the other hand, when it is determined to adjust at least one of the filter coefficients, operation S20 may be performed. Unlike the initially performed operation S20, in operation S20, which is performed after operation S90, the second communication device 2 may transmit channel information, which includes information on the variation of the filter coefficients, to the first communication device 1. Thereafter, unlike the initially performed operation S40, in operation S40, the first communication device 1 may refresh the lookup table LUT based on the information on the variation of the filter coefficients. An example of operation S40 of refreshing the lookup table LUT in response to channel information including information on the variation of the filter coefficients will be described with reference to FIG. 12." Kang, 11:62-13:6

Claim 16	Disclosure

FIG. 10

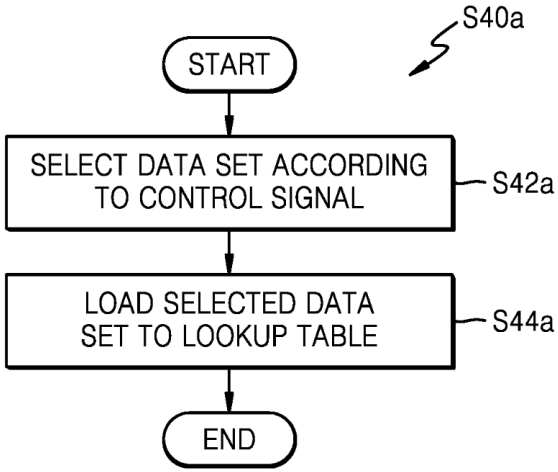


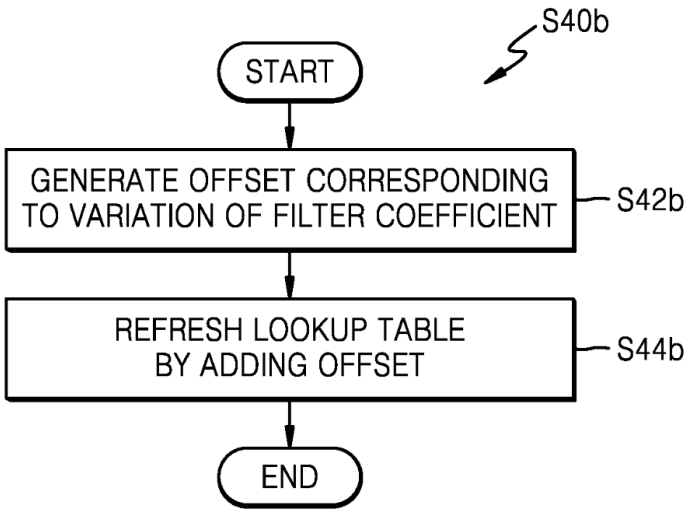
Kang, FIG. 10

"Referring to FIG. 11, operation S**40** *a* may include operations S**42** *a* and S**44** *a*. In operation S**42** *a*, an operation of selecting a data set according to the control signal CTRL may be performed. For example, the controller **110** of FIG. 3 may receive a control signal CTRL including information indicating one of k filter coefficient sequences and may control the data storage **120** to output one of first to k-th data sets SET**1** to SETk, which are stored in the data storage **120**, according to the control signal CTRL.

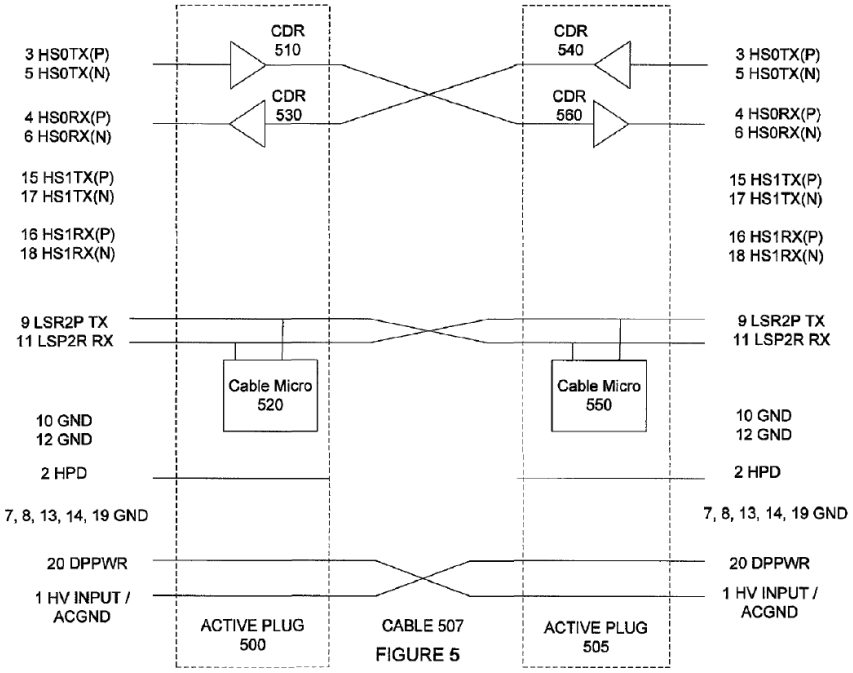
In operation S**44** *a*, an operation of loading the selected data set into the lookup table **130** may be performed. For example, the controller **110** may control the data storage **120** and the lookup table **130** to store the second value VAL**2** outputted from the data storage **120** in the lookup table **130**.

Claim 16	Disclosure
	Referring to FIG. 12, operation S**40** *b* may include operations S**42** *b* and S**44** *b*. In operation S**42** *b*, an operation of generating an offset OFF corresponding to the variation of the filter coefficients may be performed. For example, the offset generator **150** of FIG. 6 may generate an offset OFF, based on the variation signal VAR and the index IDX provided from the controller **110′**. The variation signal VAR may indicate at least one of up, down, hold, and reset of the filter coefficient and may include a variation amount of the filter coefficient. An example of generating the offset OFF when the variation signal VAR indicates the reset of the filter coefficient will be described later with reference to FIG. 13. In operation S**44** *b*, an operation of refreshing the lookup table **130′** may be performed by adding the offset OFF. In some embodiments, the offset generator **150** may generate a positive offset OFF or a negative offset OFF, and thus the calculator **160** may perform an addition. In some embodiments, the offset generator **150** may generate the positive offset OFF, and thus the calculator **160** may perform addition or subtraction according to the control of the controller **110′**. The lookup table **130′** may be refreshed by storing the output value of the calculator **160**, that is, the third value VAL**3**, in the lookup table **130′**." Kang, 13:18-54

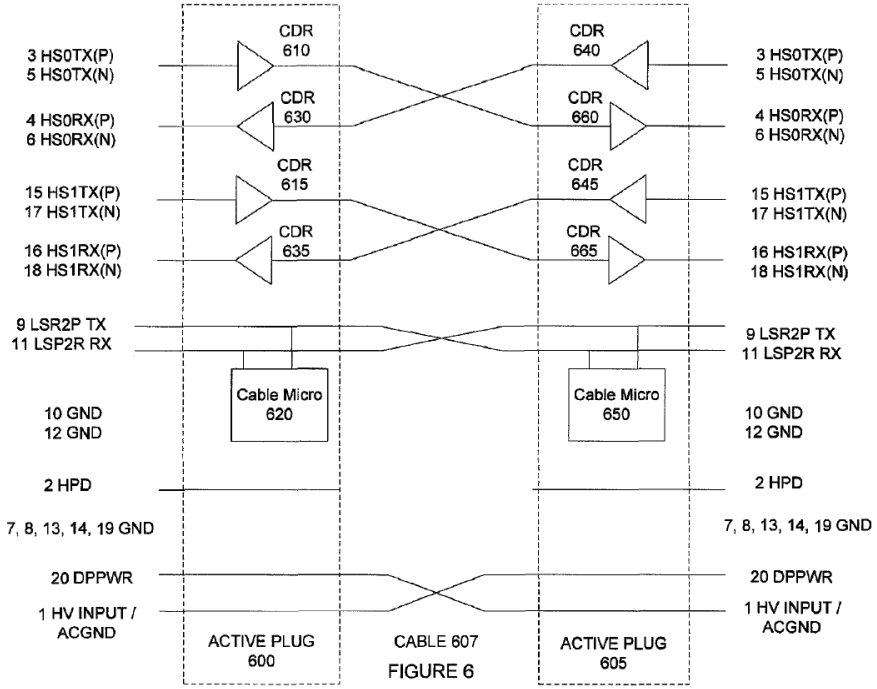
Claim 16	Disclosure
	FIG. 11  Kang, FIG. 11

Claim 16	Disclosure
	FIG. 12  Kang, FIG. 12 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**. Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**.

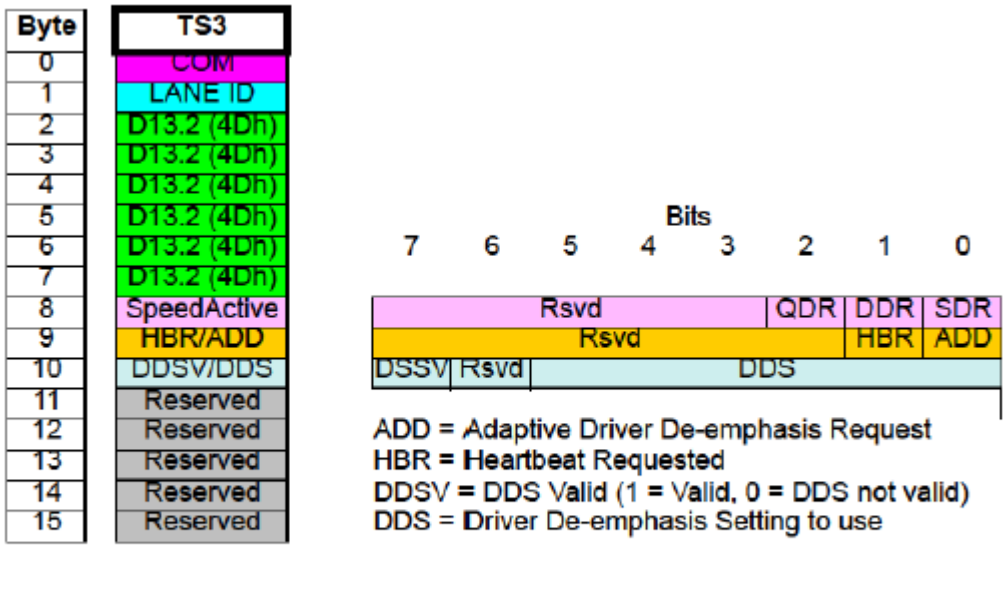
Claim 16	Disclosure
	The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables. In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used.

Claim 16	Disclosure
	In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5 "FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock

Claim 16	Disclosure
	and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 16	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 16	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 16	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 16	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

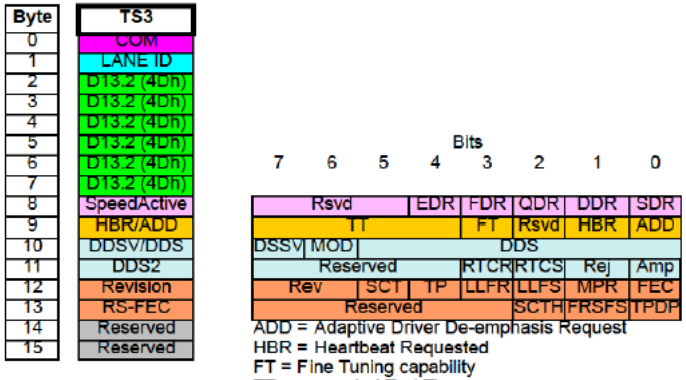
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 16	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits	7	6	5	4	3	2	1	0
	Rsvd			EDR	FDR	QDR	DDR	SDR
	TT				FT	Rsvd	HBR	ADD
	DSSV	MOD	DDS					
	Reserved				RTCR	RTCS	Rej	Amp
	Rev		SCT	TP	LLFR	LLFS	MPR	FEC
	Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 16	Disclosure

5.5.2.4.1 REV 0 TS3

Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field.

Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR).

InfiniBand, p. 147:34-42

Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283.

Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver.

The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity.

InfiniBand, p. 148:1-13

Claim 16	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 16	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 16	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 16	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 16	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 16	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

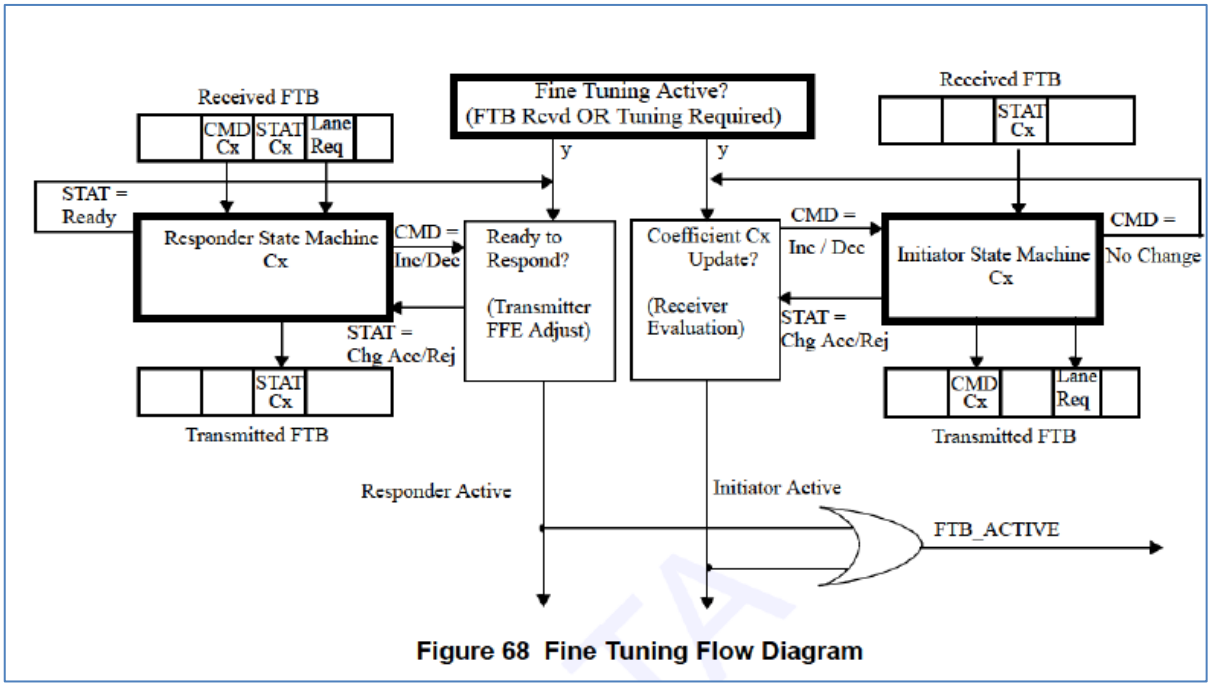
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 16	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 16	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 16	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required

Addr	Size	Type	Functions
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required

Addr	Size	Type	Functions
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional

Addr	Size	Type	Functions
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional

Addr	Size	Type	Functions
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies

Addr	Size	Type	Functions
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 16	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 16	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 16	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

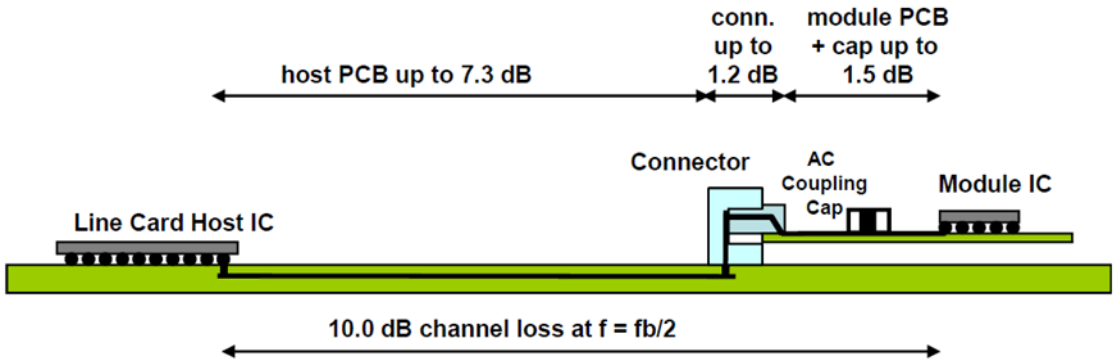
InfiniBand, Table 143 (p. 535)

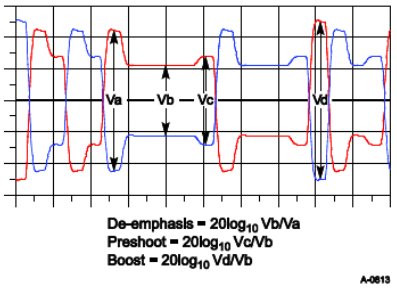
"The overall pre-equalizer **800** can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."

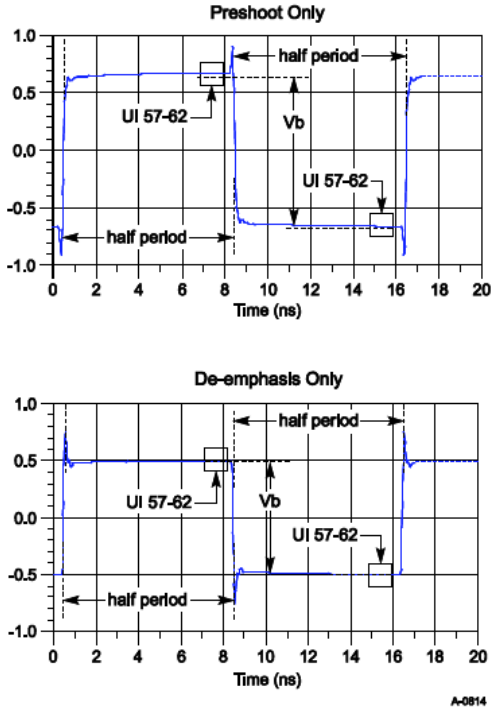
Rafie, paragraph 82.

"Digital pre-equalizer (PEQ) circuit **204** can be configured to introduce a distortion to the input signal to compensate for channel impairment. At power-on little or no information may be known about the channel. Accordingly, the digital PEQ circuit **204** can be initially configured with no distortion. In some

Claim 16	Disclosure
	embodiments, the digital PEQ circuit **204** can be initially configured with a distortion that is based upon a corresponding set of coefficients." Ciacci, 5:40-47. "The coefficients can then be used in combination with a pre-equalizer filter function of higher than first order" Ciacci, 8:2-4. *United States Patent No. 7,239,665 ("Mezer")* Mezer describes supporting Ethernet, and such standards-compliant implementation was conventional. *See, e.g.*, at Mezer, 4:55-57, 6:62-7:3. This obvious implementation would have met the Ethernet standard's description of a chip-to-module communication link comprising a port connector coupling a port transceiver to a pluggable module transceiver. *See, e.g.*, IEEE 802.3bs-2017, 323-330 (Annex 120C), 350-372 (Annex 120E), 350 ("The chip-to-module interface is defined using a specification… that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0"); *see also* OIF-CEI-04.0, 334, Fig. 16-15 (below, showing a "Connector" receiving a pluggable module).

Claim 16	Disclosure
	Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model  *PCIe 3.1a* **4.3.3.5.2. Tx Equalization Presets** An 8.0 GT/s transmitter must support a specified number of presets, where the preset values are defined in terms of voltage ratios as illustrated in Figure 4-42. Presets are defined in terms of two ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GTs/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. Figure 4-42 is shown as an example of TxEQ and is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of 8.0 GT/s signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms, as shown later in this section. The presets defined in Table 4-16 and Table 4-17 are numbered to match the designations in Section 4.2.3.1. Note, however, that in Section 4.2.3.1 the coefficients are defined as integers (using upper case "C"), while in the electrical section they are defined as floating point (using lower case "c"). PCIe 3.1a at 355.

Claim 16	Disclosure
	 **Figure 4-42: Definition of Tx Voltage Levels and Equalization Ratios** Figure 4-43 illustrates the waveforms that will be observed when measuring presets when using the 64-ones/64-zeroes sequence that is part of the compliance pattern. Depending on whether the preset implements de-emphasis, preshoot, or both the corresponding waveshape will differ. The two cases illustrated below show preshoot and de-emphasis, as can be observed by noting whether the boost occurs before or after each edge transition. For the case where both de-emphasis and preshoot are present, boost occurs both before and after each edge transition. Note that in all cases, however, the voltage of interest occurs during the flat portion (Vb) of the waveform, where it can be accurately measured independent of high frequency effects. PCIe 3.1a at 356.

Claim 16	Disclosure
	 Figure 4-43: Waveform Measurement Points for Pre-shoot and De-emphasis PCIe 3.1a at 357.

Claim 16	Disclosure

Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

Notes:

1. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The allowable P10 boost range is defined by the coefficient space lying between the Min and Max Reduced Swing Limits as shown by the two diagonal lines in the example of Figure 4-45. This approach permits both full and reduced swing transmitters to use P10 for testing to their respective boost limits.

With the exception of P4 (for which both pre-shoot and de-emphasis are 0.0 dB) it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are 1 UI wide and therefore subject to attenuation by the package and the breakout channel. Instead the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval. Table 4-17 lists the preset values required to measure each of the Va and Vc values from which the preshoot or de-emphasis values may be derived.

PCIe 3.1a at 358.

Claim 16	Disclosure
	Table 4-17: Preset Measurement Cross Reference Table PCIe 3.1a at 359.

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P4	N/A	N/A
P1	P1/P4	N/A
P0	P0/P4	N/A
P9	N/A	P4/P9
P8	P8/P6	P3/P8
P7	P7/P5	P2/P7
P5	N/A	P4/P5
P6	N/A	P4/P6
P3	P3/P4	N/A
P2	P2/P4	N/A
P10	P10/P4	N/A

Claim 16	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 16	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 16	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

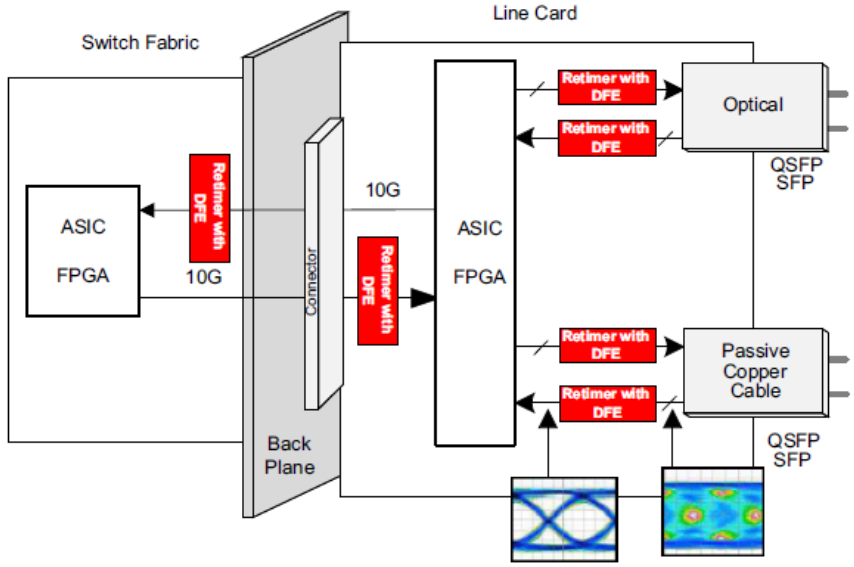
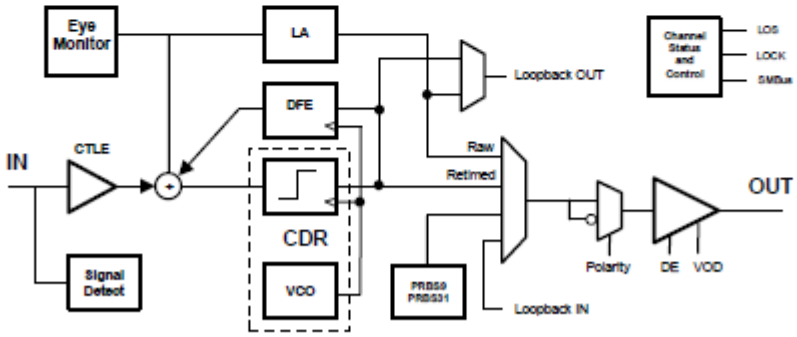


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 16	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 16	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 16	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

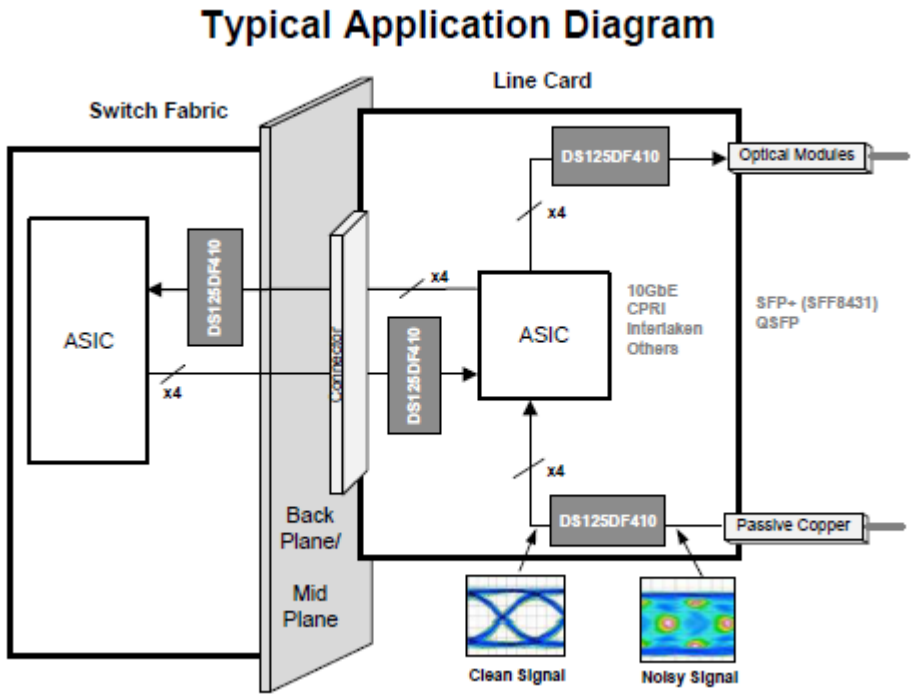
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

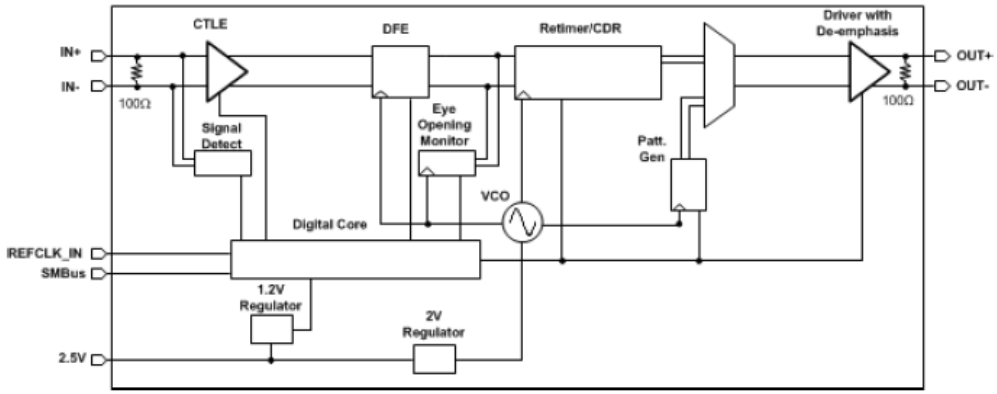
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 16	Disclosure
	 TI DS125DF410, 1.

Claim 16	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 16	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 16	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 16	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 16	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 16	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

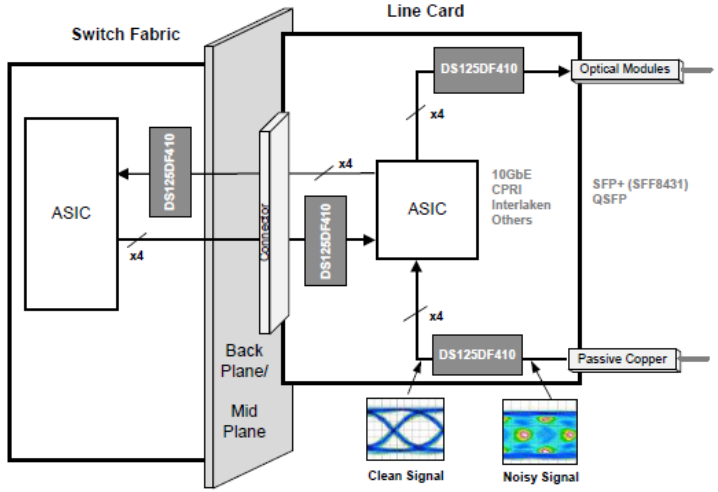
TI DS125DF410, 41.

Claim 16	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 16	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 16	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

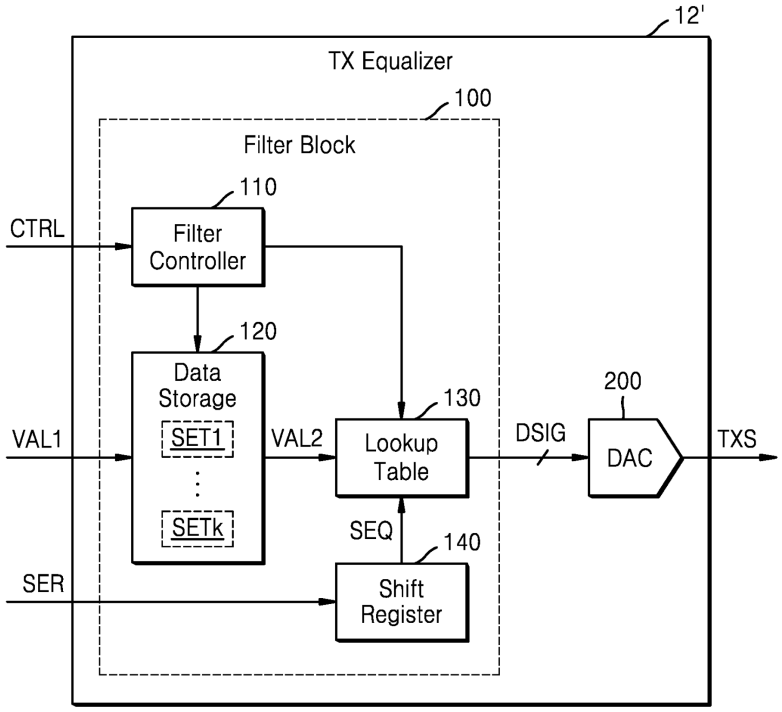
Claim 16	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Claim 16	Disclosure
16[b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model,	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**." Kang, 5:20-42.

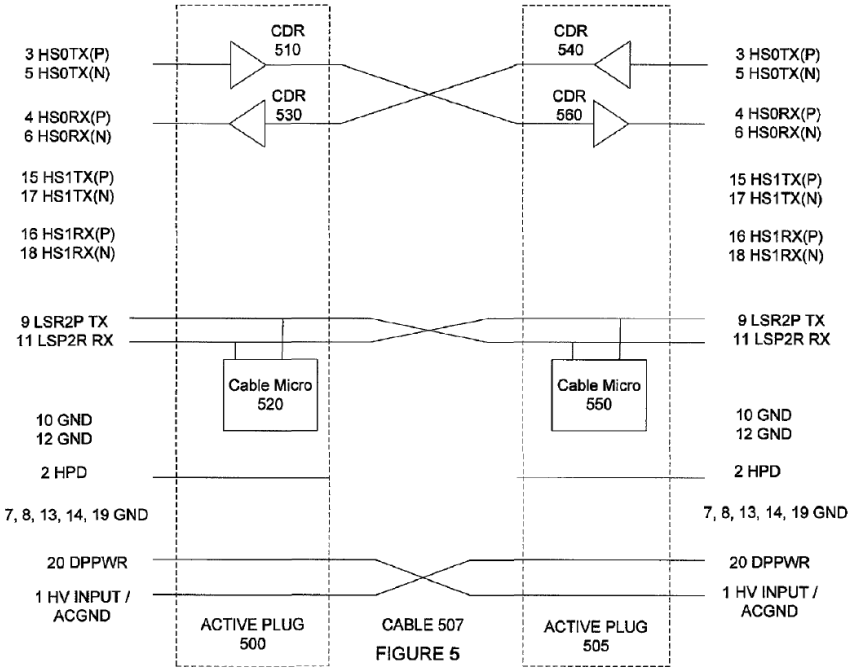
Claim 16	Disclosure
	"FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS, which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3.

Claim 16	Disclosure
	The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively.

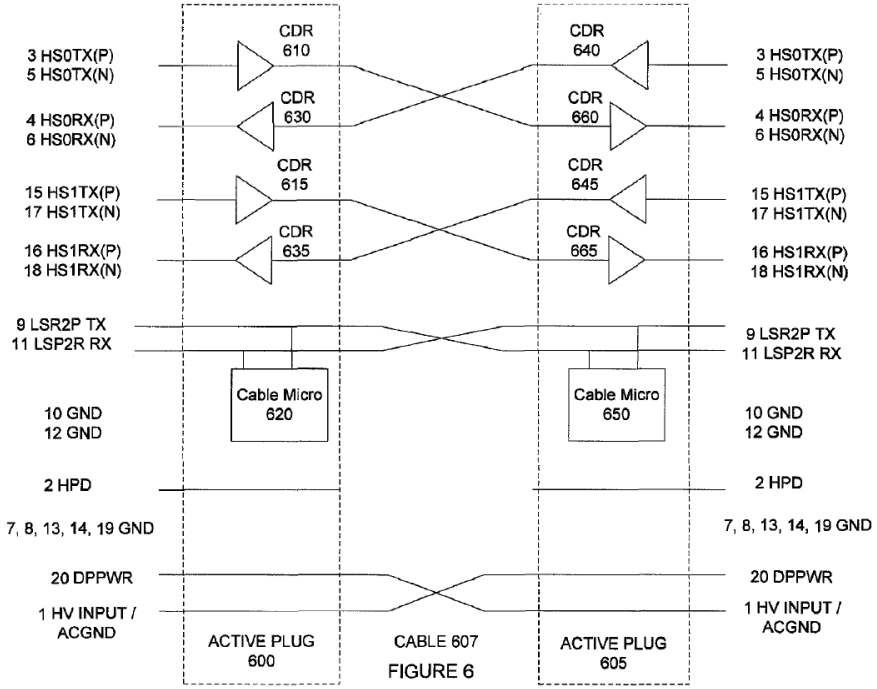
Claim 16	Disclosure
	The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 16	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 16	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 16	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 16	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 16	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 16	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 16	Disclosure

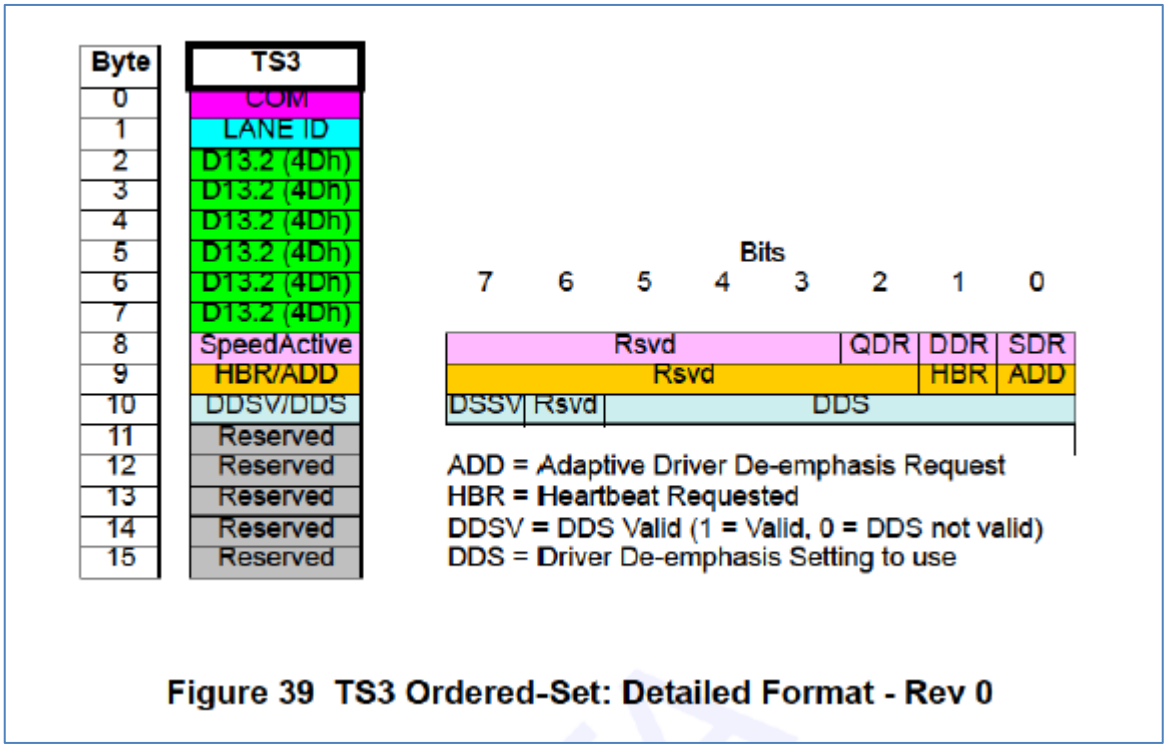


Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 16	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

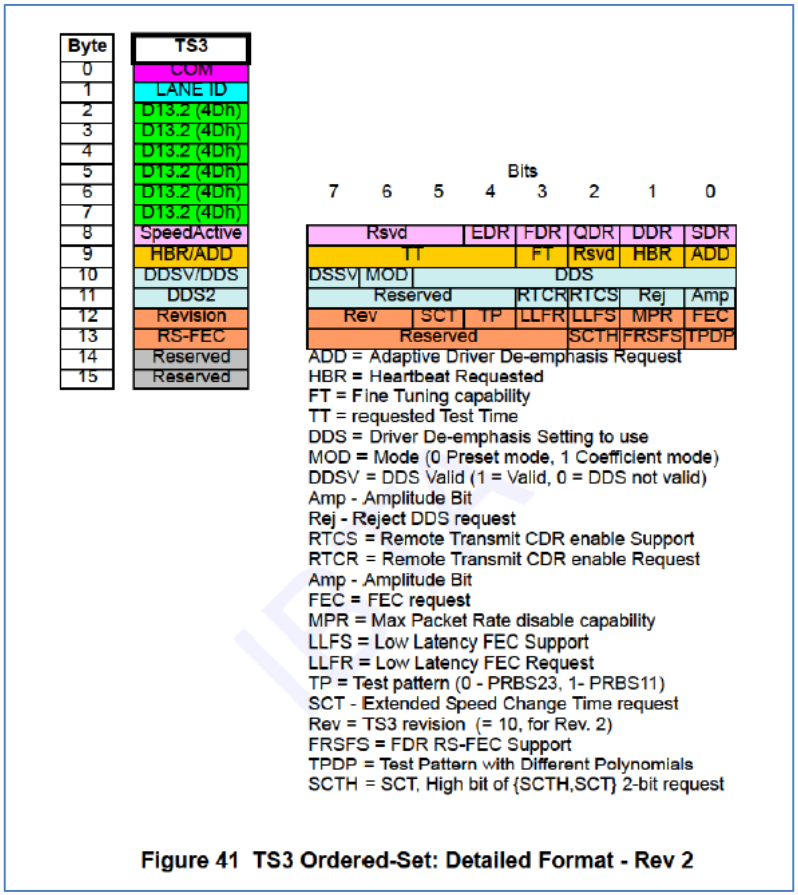
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 16	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 16	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 16	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 16	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 16	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 16	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 16	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 16	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

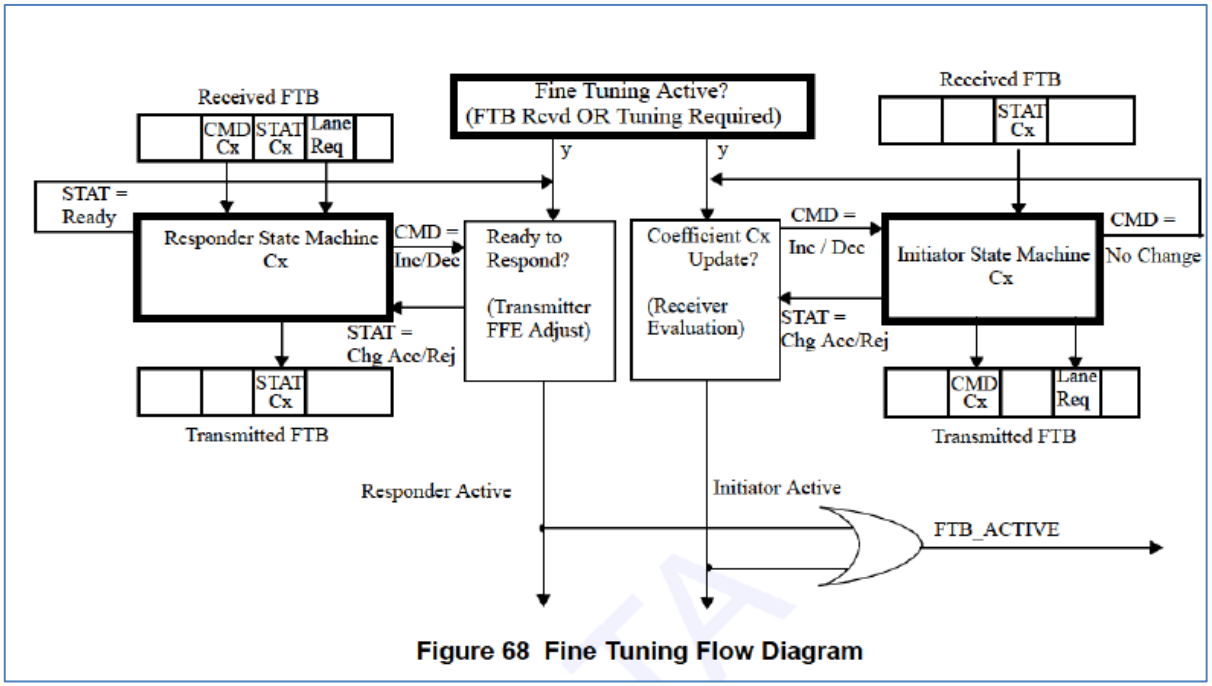
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 16	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 16	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 16	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 16	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 16	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 16	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

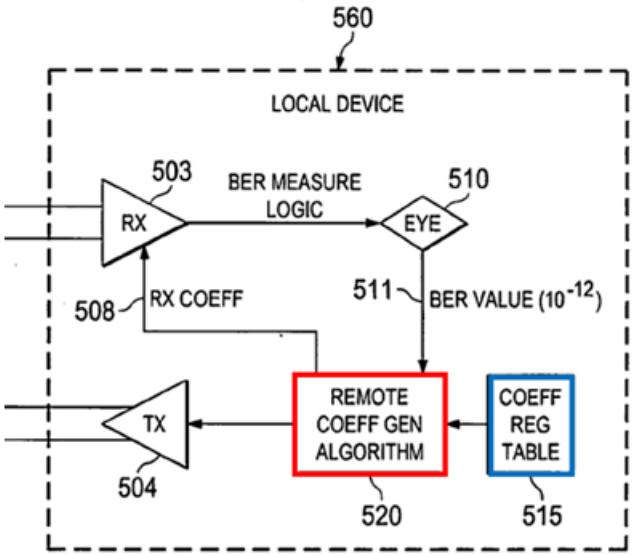
InfiniBand, Table 143 (p. 535)

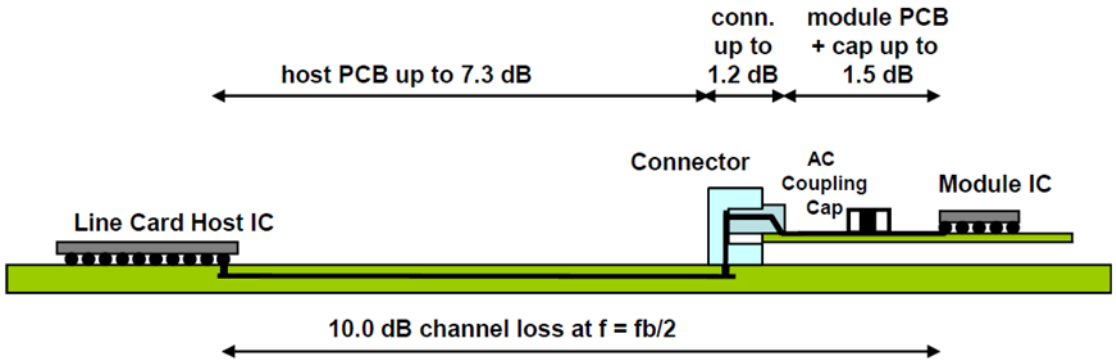
"The overall pre-equalizer **800** can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."

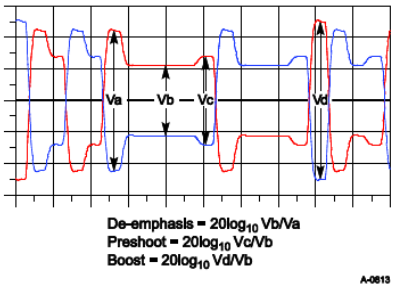
Rafie, paragraph 82.

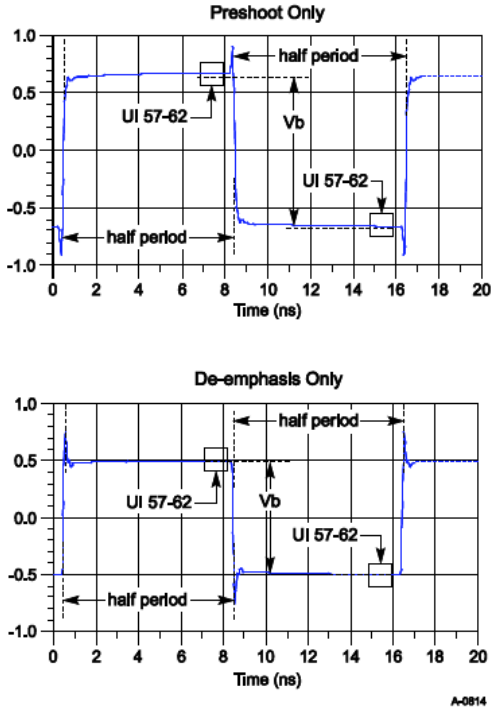
"Digital pre-equalizer (PEQ) circuit **204** can be configured to introduce a distortion to the input signal to compensate for channel impairment. At power-on little or no information may be known about the channel. Accordingly, the digital PEQ circuit **204** can be initially configured with no distortion. In some

Claim 16	Disclosure
	embodiments, the digital PEQ circuit **204** can be initially configured with a distortion that is based upon a corresponding set of coefficients." Ciacci, 5:40-47. "Once frequency response of front-end components has been characterized, this information can be stored in the digital base band on a configuration register (CFR), and thereby used to specify gain coefficients of the digital pre-equalizer. Balakrishnan, paragraph 27. *U.S. Patent Publication No. 2014/0281067 ("Das Sharma")* Das Sharma discloses selecting initial coefficient values for transmit filters for use in an adaptive pre-equalization training process from among the registers. *See, e.g.*, Das Sharma at [0078], [0193], Figure 5. Das Sharma discloses a coefficient register table is used by a coefficient algorithm module that provides a set of initial coefficients to the transceiver's transmission logic. *See id*. at [0078]. Figure 5 of Das Sharma shows the coefficient algorithm module (red) and coefficient register table (blue). *See id*. at [0078] ("coefficient algorithm module 520"). Das Sharma teaches that the coefficient algorithm module can be implemented by a microcontroller that includes the coefficient register table. *See id*. at [0078], [0193] (Das Sharma's "modules" can each be implemented via a "microcontroller" including "registers").

Claim 16	Disclosure
	 FIG. 5 *United States Patent No. 7,239,665 ("Mezer")* Mezer describes supporting Ethernet, and such standards-compliant implementation was conventional. *See, e.g.*, at Mezer, 4:55-57, 6:62-7:3. This obvious implementation would have met the Ethernet standard's description of a chip-to-module communication link comprising a port connector coupling a port transceiver to a pluggable module transceiver. *See, e.g.*, IEEE 802.3bs-2017, 323-330 (Annex 120C), 350-372 (Annex 120E), 350 ("The chip-to-module interface is defined using a specification… that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0"); *see also* OIF-CEI-04.0, 334, Fig. 16-15 (below, showing a "Connector" receiving a pluggable module).

Claim 16	Disclosure
	Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model  *PCIe 3.1a* **4.3.3.5.2. Tx Equalization Presets** An 8.0 GT/s transmitter must support a specified number of presets, where the preset values are defined in terms of voltage ratios as illustrated in Figure 4-42. Presets are defined in terms of two ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GTs/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. Figure 4-42 is shown as an example of TxEQ and is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of 8.0 GT/s signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms, as shown later in this section. The presets defined in Table 4-16 and Table 4-17 are numbered to match the designations in Section 4.2.3.1. Note, however, that in Section 4.2.3.1 the coefficients are defined as integers (using upper case "C"), while in the electrical section they are defined as floating point (using lower case "c"). PCIe 3.1a at 355.

Claim 16	Disclosure
	 **Figure 4-42: Definition of Tx Voltage Levels and Equalization Ratios** Figure 4-43 illustrates the waveforms that will be observed when measuring presets when using the 64-ones/64-zeroes sequence that is part of the compliance pattern. Depending on whether the preset implements de-emphasis, preshoot, or both the corresponding waveshape will differ. The two cases illustrated below show preshoot and de-emphasis, as can be observed by noting whether the boost occurs before or after each edge transition. For the case where both de-emphasis and preshoot are present, boost occurs both before and after each edge transition. Note that in all cases, however, the voltage of interest occurs during the flat portion (Vb) of the waveform, where it can be accurately measured independent of high frequency effects. PCIe 3.1a at 356.

Claim 16	Disclosure
	 Figure 4-43: Waveform Measurement Points for Pre-shoot and De-emphasis PCIe 3.1a at 357.

Claim 16	Disclosure

Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

Notes:

1. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The allowable P10 boost range is defined by the coefficient space lying between the Min and Max Reduced Swing Limits as shown by the two diagonal lines in the example of Figure 4-45. This approach permits both full and reduced swing transmitters to use P10 for testing to their respective boost limits.

With the exception of P4 (for which both pre-shoot and de-emphasis are 0.0 dB) it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are 1 UI wide and therefore subject to attenuation by the package and the breakout channel. Instead the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval. Table 4-17 lists the preset values required to measure each of the Va and Vc values from which the preshoot or de-emphasis values may be derived.

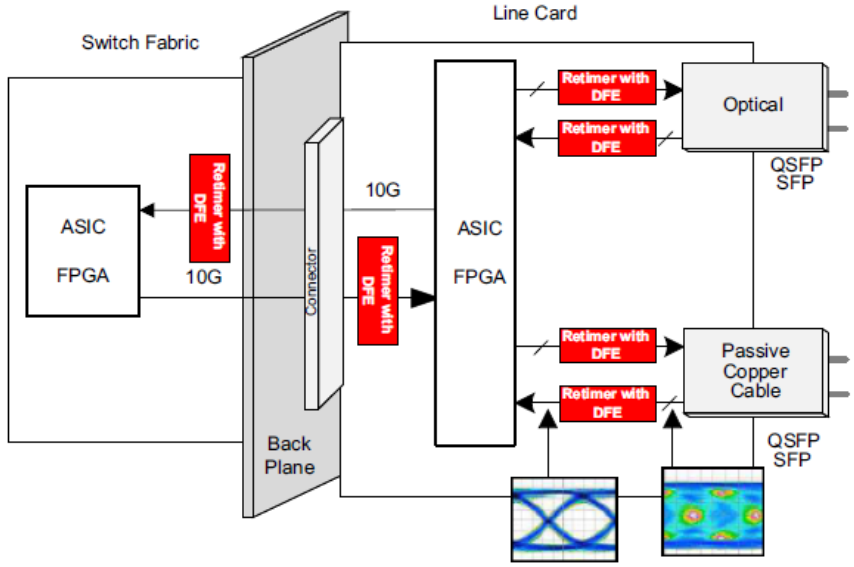
PCIe 3.1a at 358.

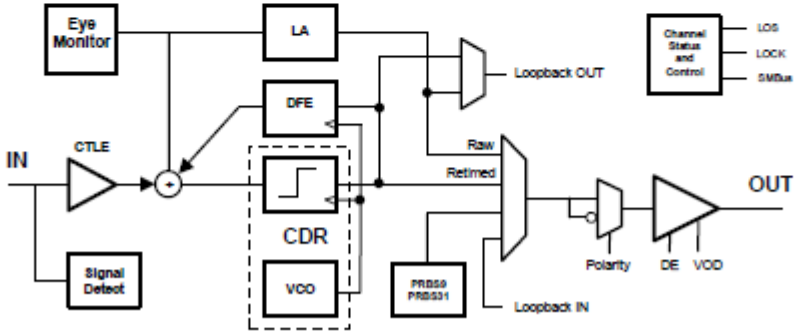
Claim 16	Disclosure
	Table 4-17: Preset Measurement Cross Reference Table PCIe 3.1a at 359.

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P4	N/A	N/A
P1	P1/P4	N/A
P0	P0/P4	N/A
P9	N/A	P4/P9
P8	P8/P6	P3/P8
P7	P7/P5	P2/P7
P5	N/A	P4/P5
P6	N/A	P4/P6
P3	P3/P4	N/A
P2	P2/P4	N/A
P10	P10/P4	N/A

Claim 16	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 16	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 16	Disclosure
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. **8.2 Typical Application** Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  **Figure 9. Typical Application** TI DS110DF111, 43.

Claim 16	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 16	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 16	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

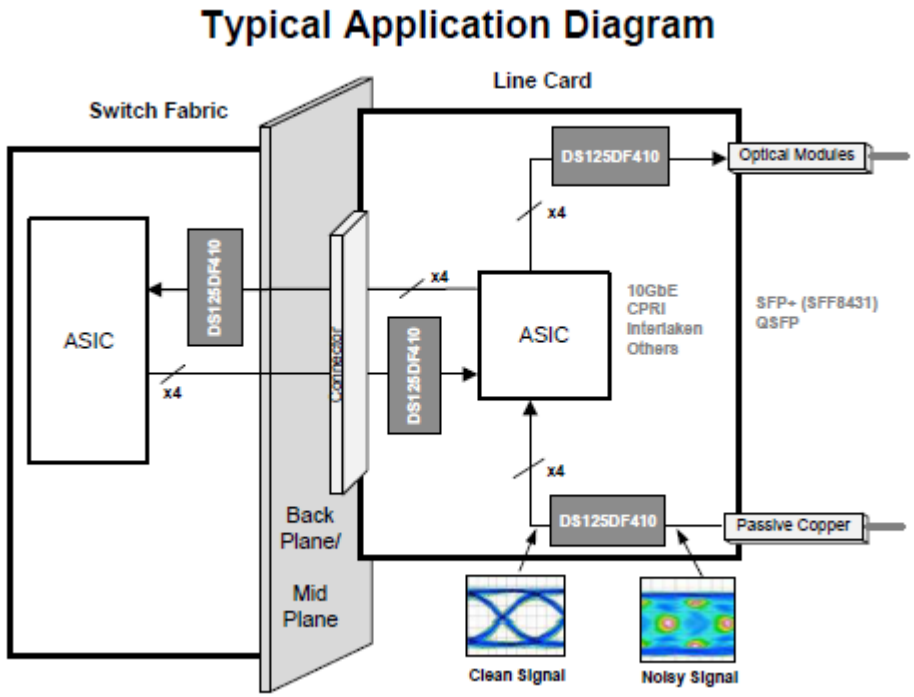
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

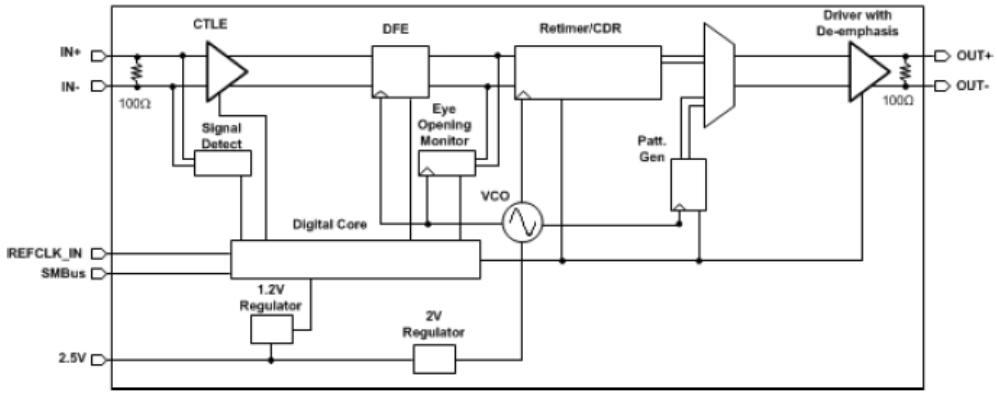
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 16	Disclosure
	 TI DS125DF410, 1.

Claim 16	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 16	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 16	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 16	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 16	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 16	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

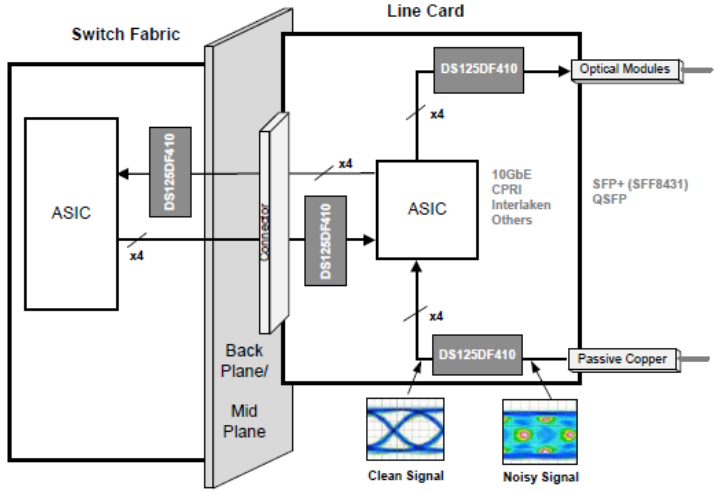
TI DS125DF410, 41.

Claim 16	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 16	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 16	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

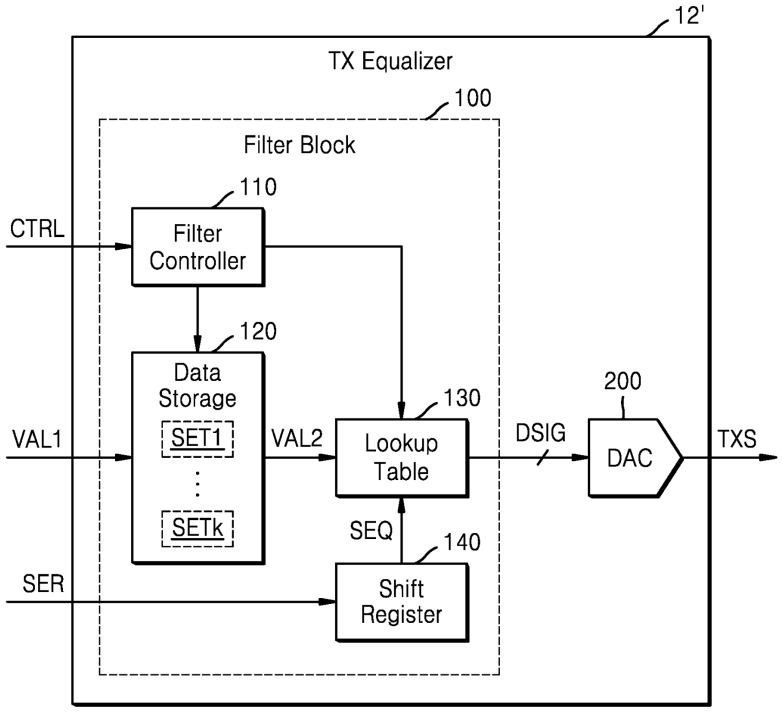
Claim 16	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Claim 16	Disclosure
16[c] the controller using one of the registers to set initial coefficient values for the one or more transmit filters.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**." Kang, 5:20-42.

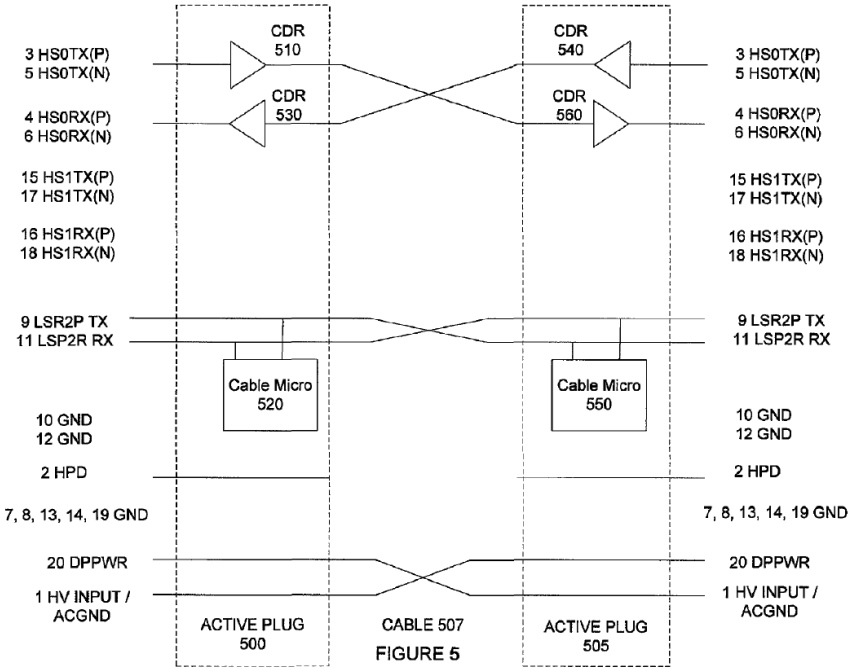
Claim 16	Disclosure
	"FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS, which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3.

Claim 16	Disclosure
	The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively.

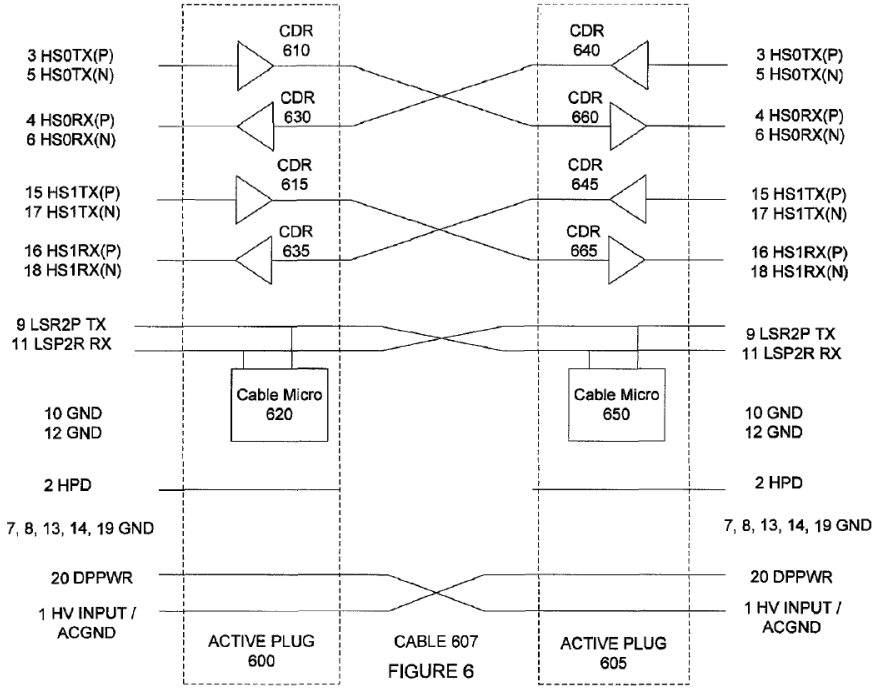
Claim 16	Disclosure
	The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 16	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 16	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 16	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 16	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 16	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 16	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 16	Disclosure

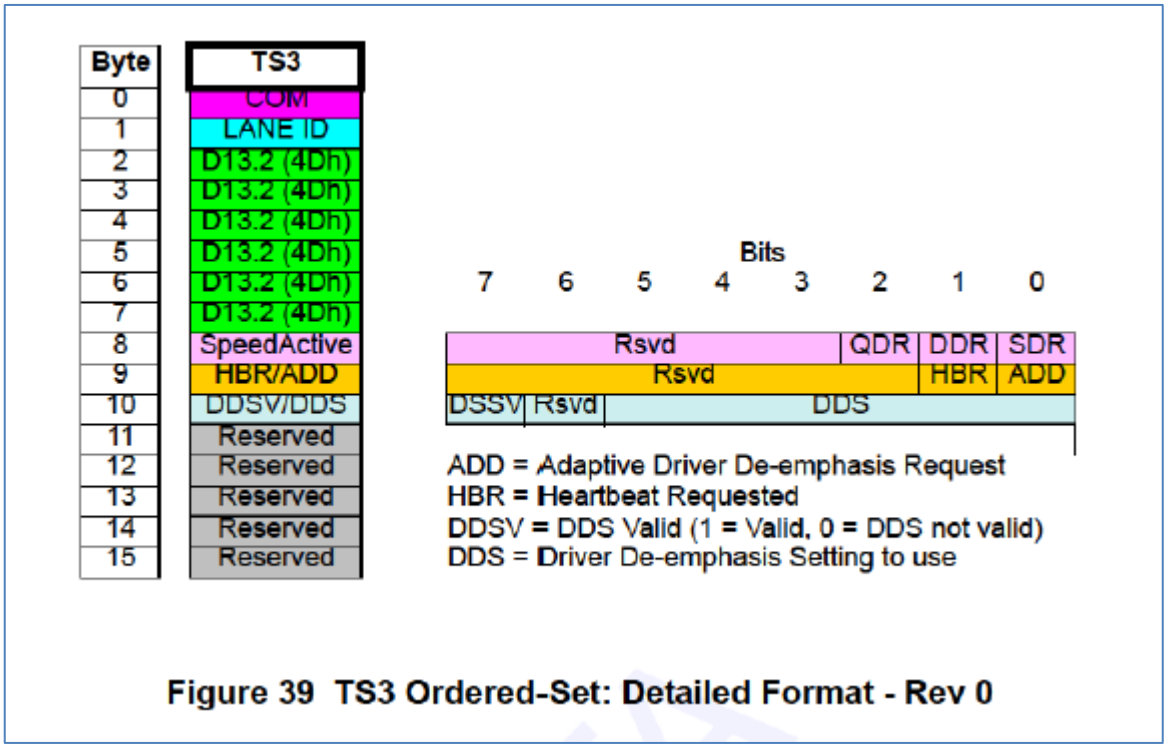
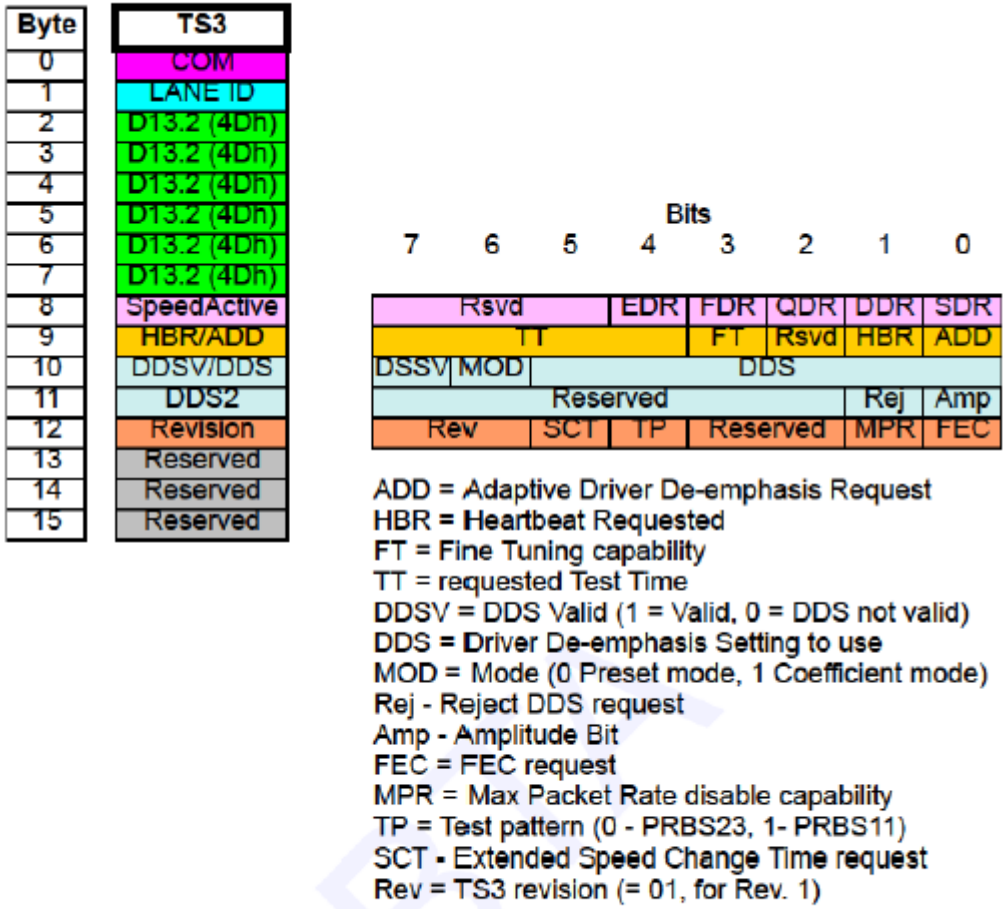


Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 16	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

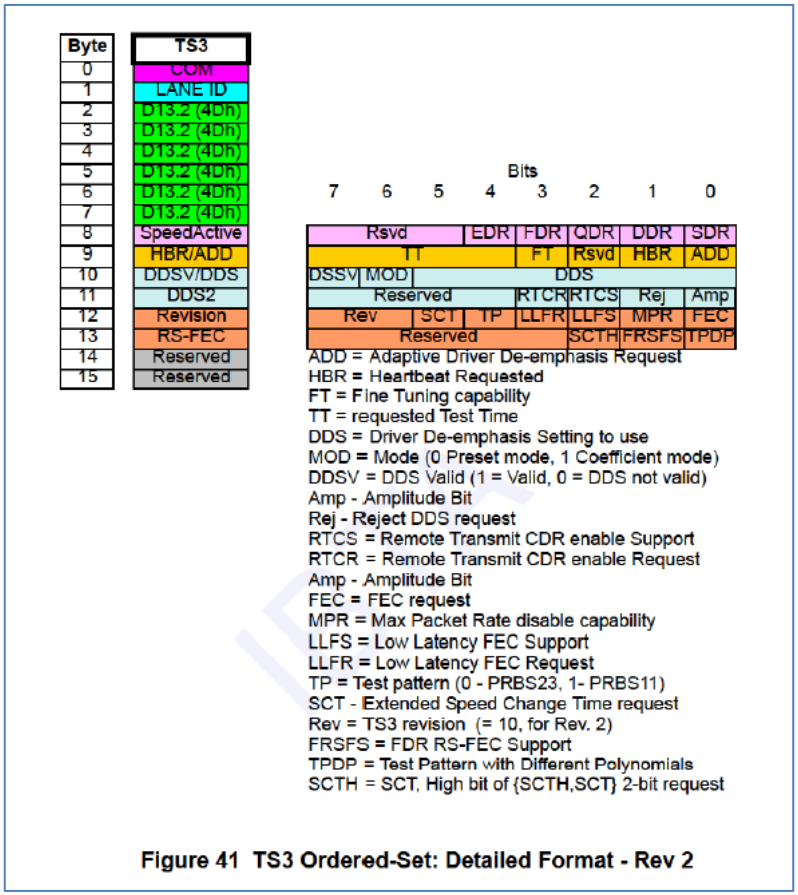
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 16	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits	7	6	5	4	3	2	1	0
	Rsvd			EDR	FDR	QDR	DDR	SDR
	TT				FT	Rsvd	HBR	ADD
	DSSV	MOD	DDS					
	Reserved				RTCR	RTCS	Rej	Amp
	Rev		SCT	TP	LLFR	LLFS	MPR	FEC
	Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 16	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 16	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 16	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 16	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 16	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 16	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 16	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

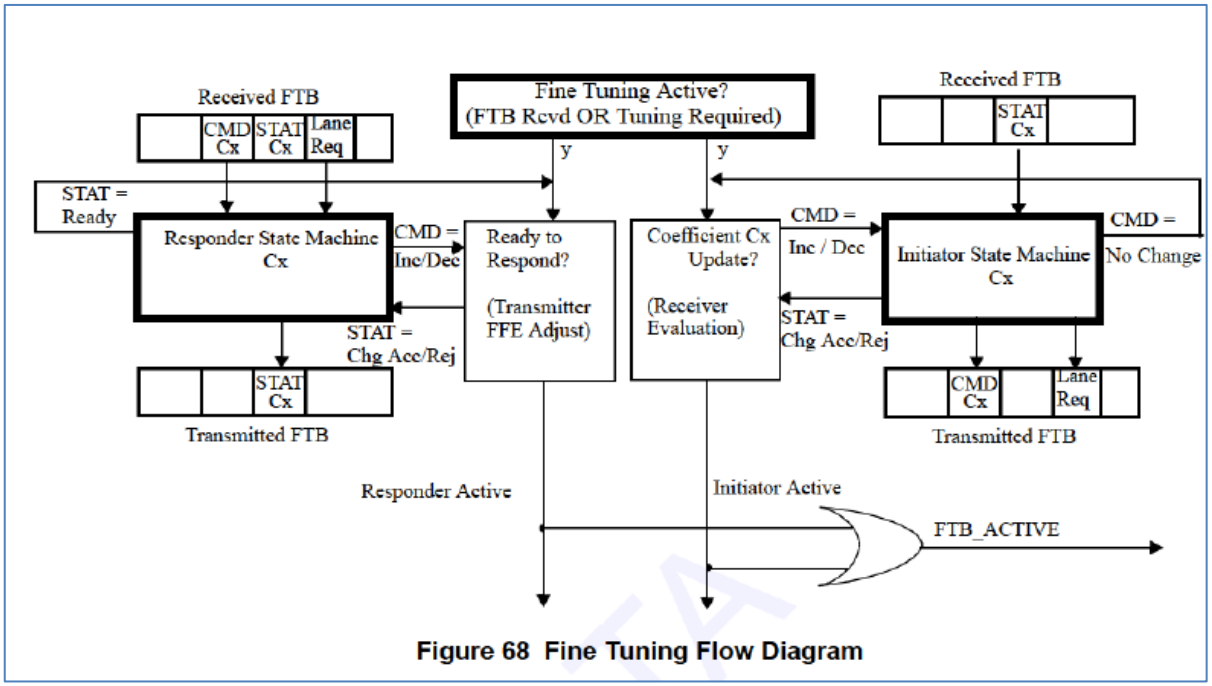
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 16	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 16	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 16	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required

Addr	Size	Type	Functions
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required

Addr	Size	Type	Functions
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional

Addr	Size	Type	Functions
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional

Addr	Size	Type	Functions
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies

Addr	Size	Type	Functions
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 16	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 16	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 16	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"The overall pre-equalizer **800** can be programmed to have N different tap coefficient sets each corresponding to a different operating frequency range. This feature is primarily provided to account for any possible frequency dependency of the linear characteristics of the RF components."

Rafie, paragraph 82.

"Digital pre-equalizer (PEQ) circuit **204** can be configured to introduce a distortion to the input signal to compensate for channel impairment. At power-on little or no information may be known about the channel. Accordingly, the digital PEQ circuit **204** can be initially configured with no distortion. In some

Claim 16	Disclosure
	embodiments, the digital PEQ circuit **204** can be initially configured with a distortion that is based upon a corresponding set of coefficients." Ciacci, 5:40-47. "Once frequency response of front-end components has been characterized, this information can be stored in the digital base band on a configuration register (CFR), and thereby used to specify gain coefficients of the digital pre-equalizer. Balakrishnan, paragraph 27. *PCIe 3.1a* The equalization procedure consists of up to four Phases, as described below. When operating at the 8.0 GT/s data rate, the Phase information is transmitted using the Equalization Control (EC) field in the TS1 Ordered Sets. Phase 0: The Downstream Port communicates the Transmitter preset values and the Receiver preset hints for each Lane to the Upstream Port using 8b/10b encoding. These values are communicated using the EQ TS2 Ordered Sets (defined in Section 4.2.4.1) in Recovery.RcvrCfg, when a data rate change to 8.0 GT/s has been negotiated, prior to transitioning to 8.0 GT/s data

Claim 16	Disclosure
	rate. These preset values are derived from the Upstream Port Transmitter Preset and Upstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. After the data rate change to 8.0 GT/s, the Upstream Port transmits TS1 Ordered Sets with the preset values it received. The preset values must be within the operable range defined in Section 4.3.3.5.2 if reduced swing will be used by the Transmitter. Phase 1: Both components make the Link operational enough at 8.0 GT/s data rate to be able to exchange TS1 Ordered Sets to complete remaining phases for the fine-tuning their Transmitter/Receiver pairs. It is expected that the Link will operate at a BER of less than 10^{-4} before the component is ready to move on to the next Phase. The Downstream Port initiates Phase 1 by transmitting TS1 Ordered Sets with EC=01b (indicating Phase 1) to the Upstream Port using the preset values in the Downstream Port Transmitter Preset and, optionally, the Downstream Port Receiver Preset Hint fields of each Lane's Equalization Control register. The Upstream Port, after adjusting its Receiver, if necessary, to ensure that it can progress with the equalization process, receives these TS1 Ordered Sets and transitions to Phase 1 (where it transmits TS1 Ordered Sets with EC=01b). The Downstream Port ensures that it can reliably receive the bit stream from the Upstream Port to continue through the rest of the Phases when it receives TS1 Ordered Sets from the Upstream Port with EC=01b before it moves on to Phase 2. Phase 2: In this Phase the Upstream Port adjusts the Transmitter setting of the Downstream Port along with its own Receiver setting, independently, on each Lane, to ensure it receives the bit stream compliant with the requirements in Section 4.3 (e.g., all operational Downstream Lanes have a BER is less than 10^{-12}). The Downstream Port initiates the move to Phase 2 by transmitting TS1 Ordered Sets with EC=10b to the Upstream Port. The Downstream Port advertises the Transmitter coefficients and the preset it is using per the rules below in Phase 1 for preset only and in Phase 2 for preset and coefficients. The Upstream Port receives these Ordered Sets and may request different coefficient or preset settings and continue to evaluate each setting until it arrives at the best setting for operating the Downstream Lanes. After the Upstream Port has completed this Phase, it moves the Link to Phase 3 by transmitting TS1 Ordered Sets with EC=11b to the Downstream Port. Phase 3: In this Phase the Downstream Port adjusts the Transmitter setting of the Upstream Port along with its own Receiver setting, independently, on each Lane, using a handshake and evaluation process similar to Phase 2 with the exception that EC=11b. The Downstream Port signals the end of Phase 3 (and the equalization procedure) by transmitting TS1 Ordered Sets with EC=00b. PCIe 3.1a at 240-241.

Claim 16	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 16	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 16	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

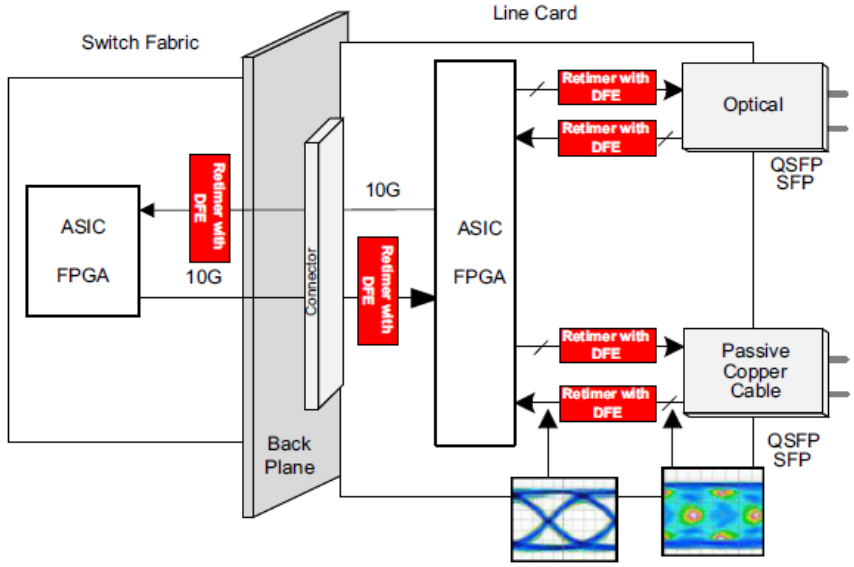
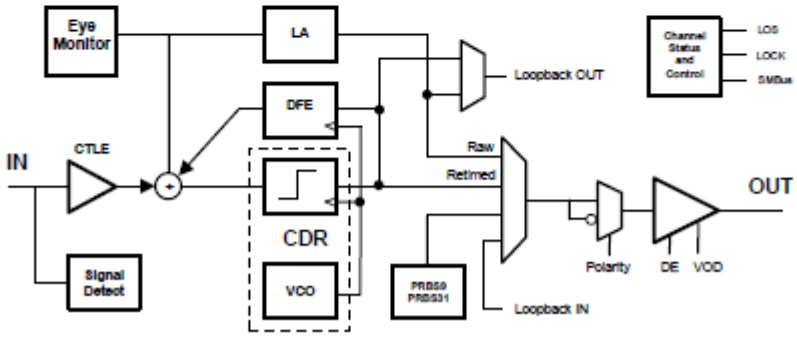


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 16	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 16	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 16	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

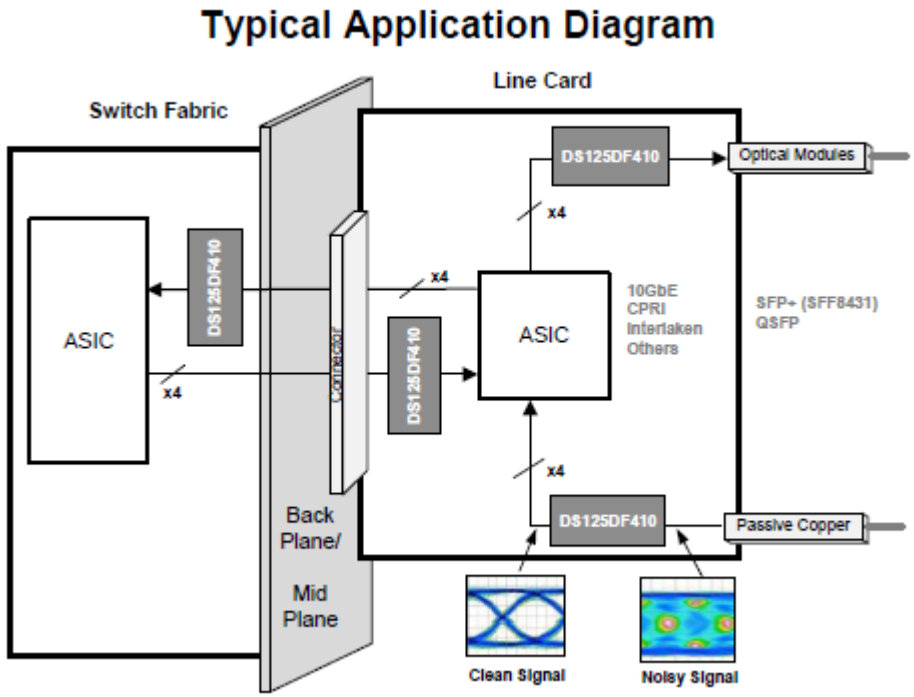
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

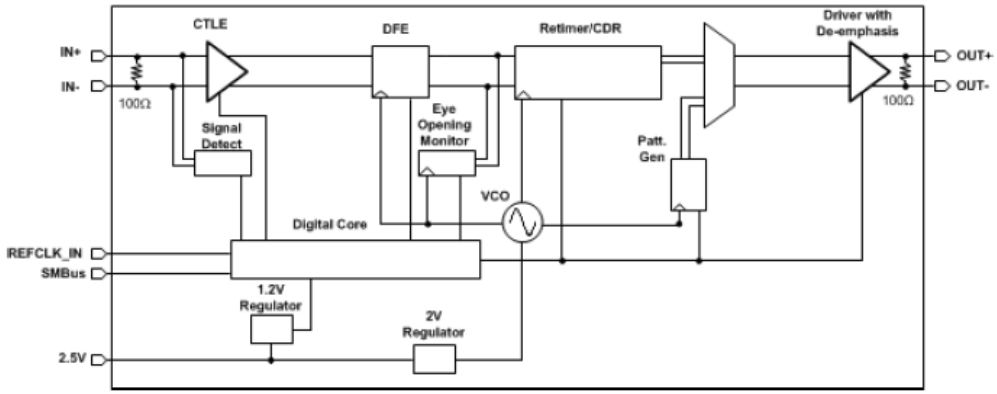
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 16	Disclosure
	 TI DS125DF410, 1.

Claim 16	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 16	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 16	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 16	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 16	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 16	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 16	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

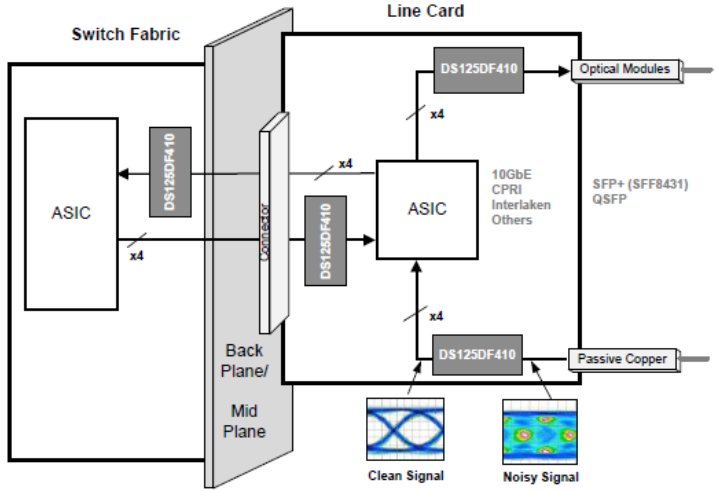
TI DS125DF410, 41.

Claim 16	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 16	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 16	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 16	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

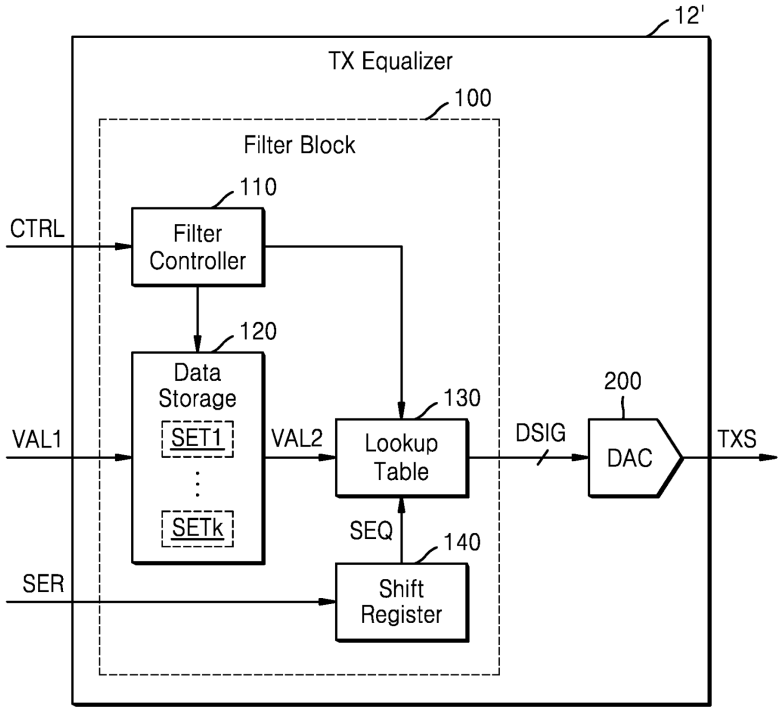
Q. DEPENDENT CLAIM 17

Claim 17	Disclosure
17. The pluggable module transceiver of claim 16, wherein the port transceiver determines a performance characteristic for each register.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

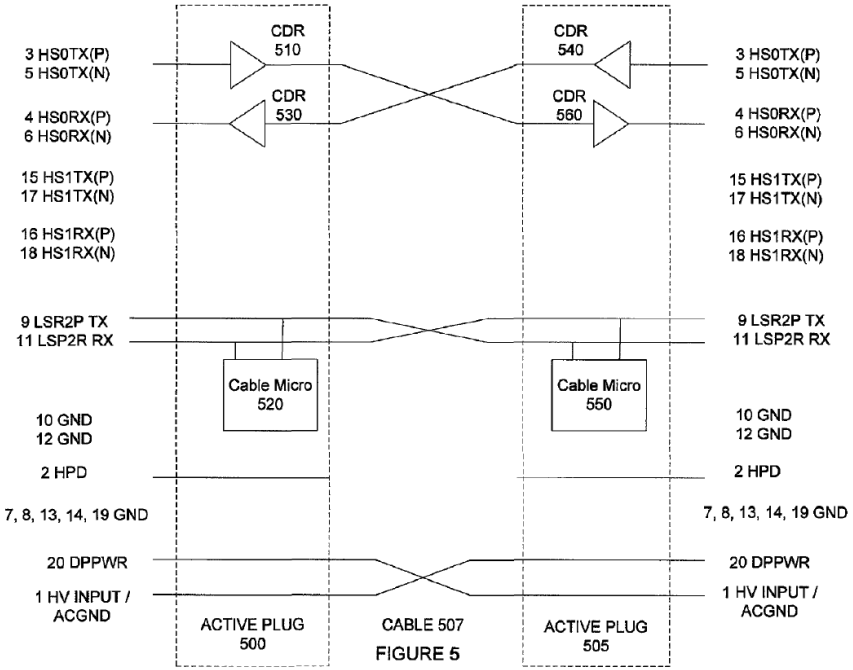
Claim 17	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 17	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

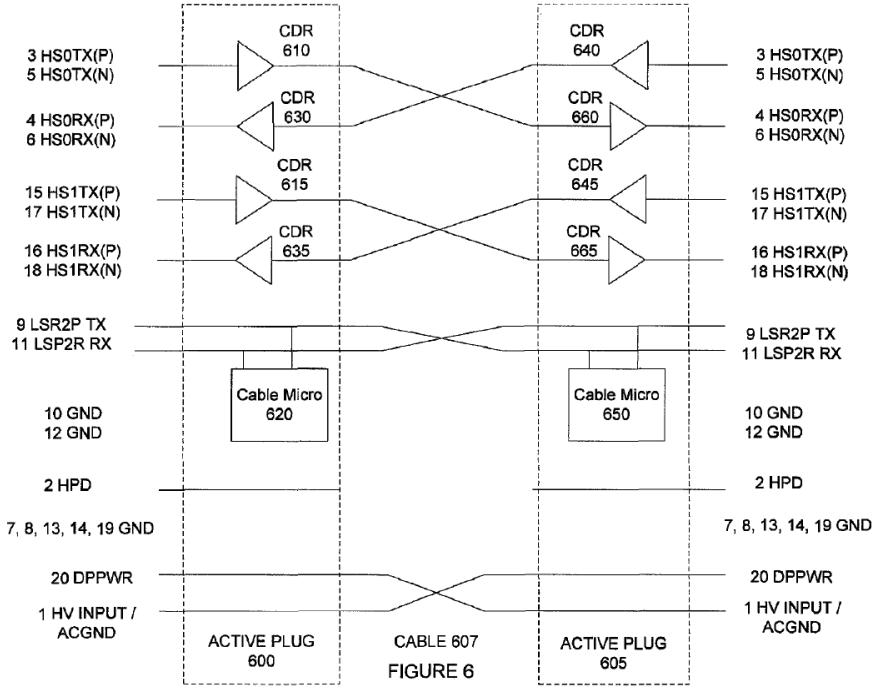
Claim 17	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 17	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

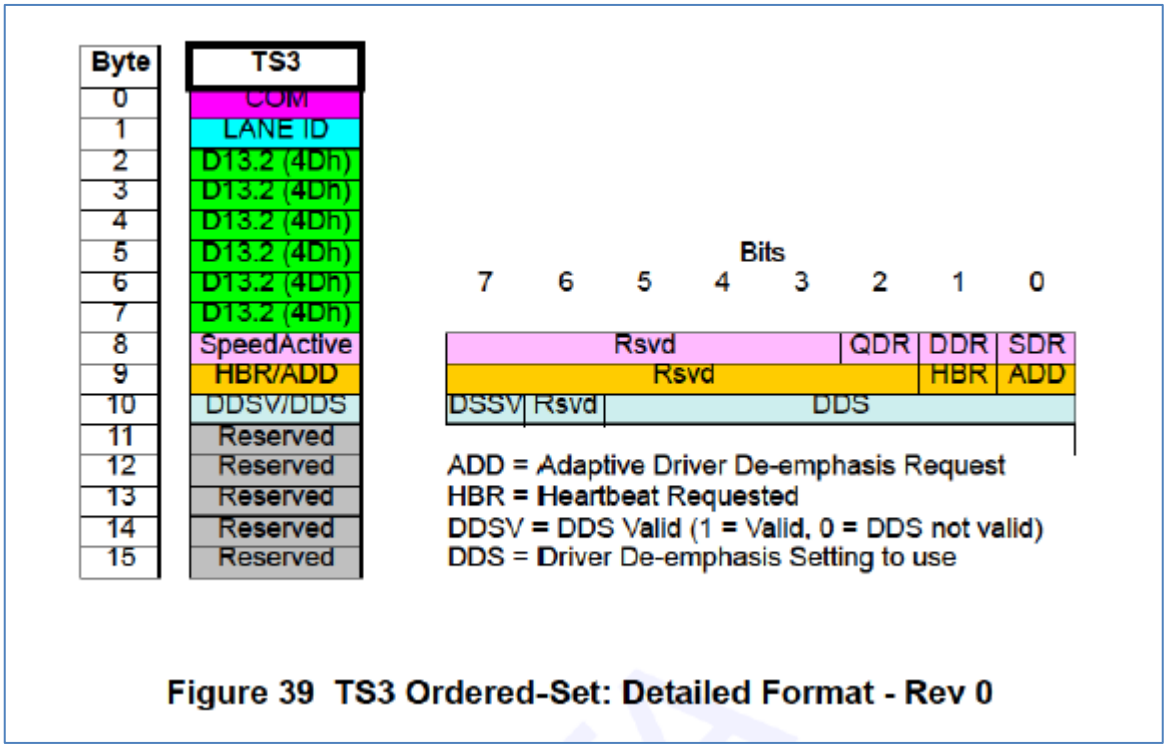
Claim 17	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 17	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

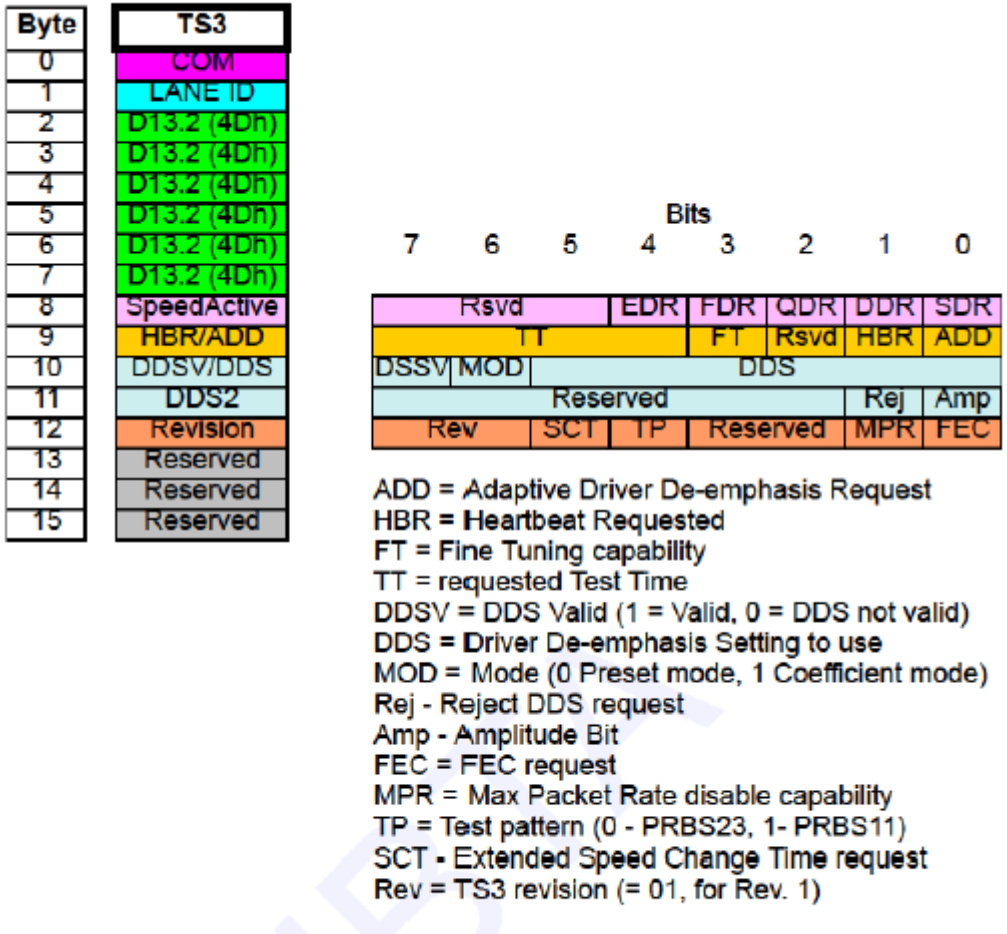
Claim 17	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 17	Disclosure
	 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 17	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 17	Disclosure
	 **Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0** InfiniBand, Figure 39 (p. 145)

Claim 17	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

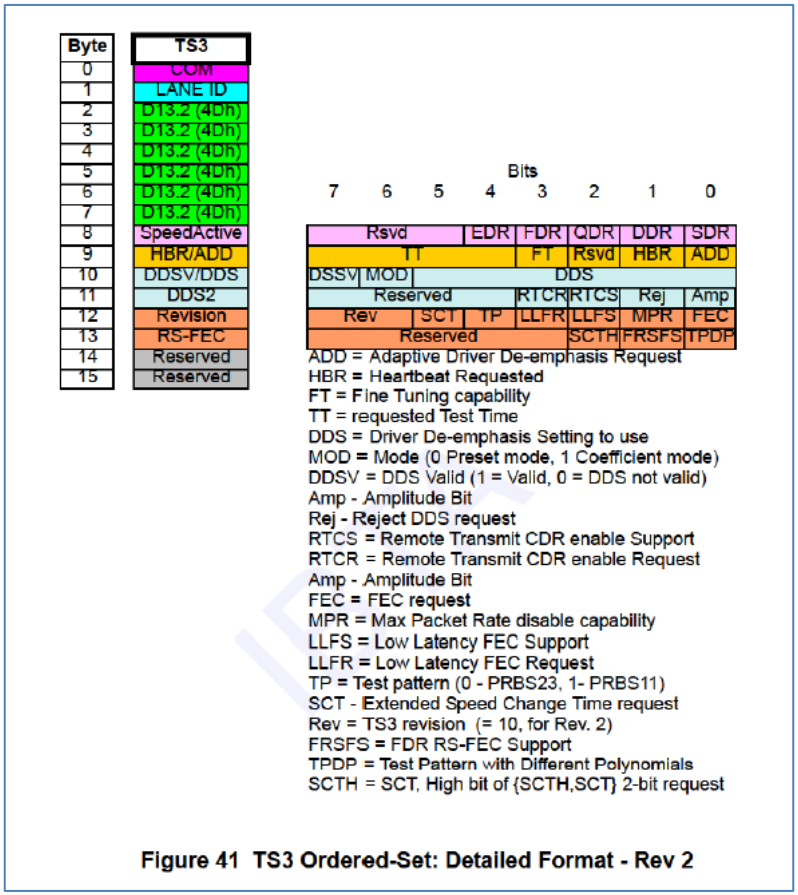
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 17	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 17	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 17	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 17	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 17	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 17	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 17	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 17	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

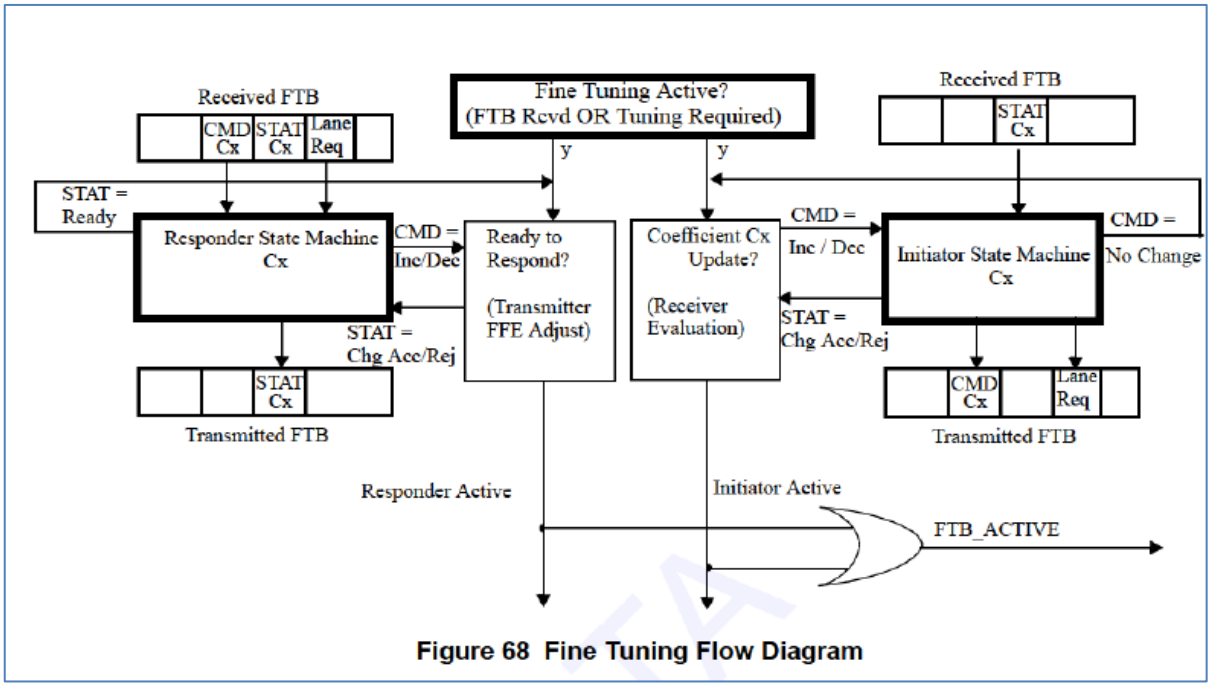
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 17	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 17	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 17	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 17	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 17	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 17	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"In step **308**, a determination is made as to whether power thresholds for pre-equalization coefficients ahs been exceeded. In this step, when a CM is transmitting data during a DOCSIS periodic ranging process, pre-equalization coefficients are calculated."

Fox, p. 10.

Claim 17	Disclosure
	"Once the initial QAM modulation order and R-S FEC parameters have been set, the system enters a "tracking" or "maintenance" mode, as shown in detail in the process steps **400** illustrated in **FIG. 4.** Specifically, the process steps **400** utilize ongoing CMTS receiver measurements, such as bit error rates, modulation error rates, and power measurements, to continually recalculate and optimize various CMTS receiver parameters in each channel's profile." Fox, p. 11.

Claim 17	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 17	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 17	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

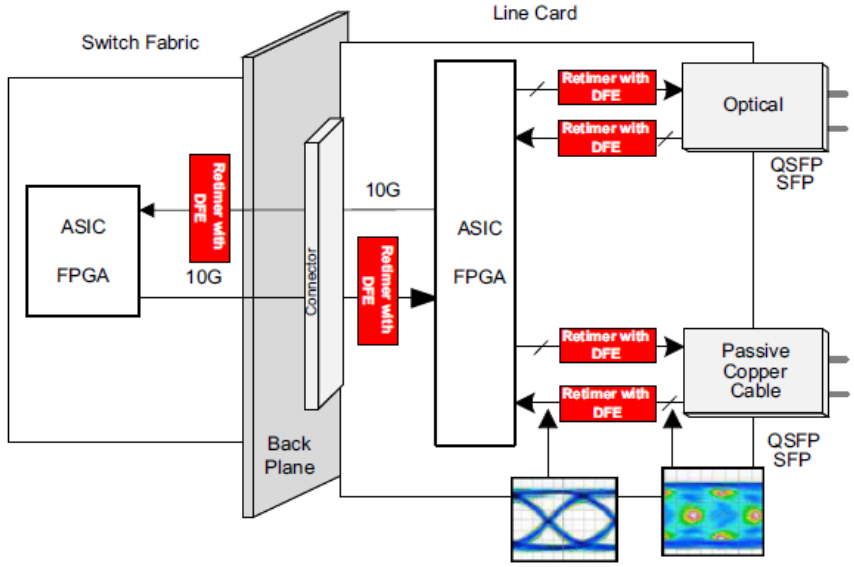
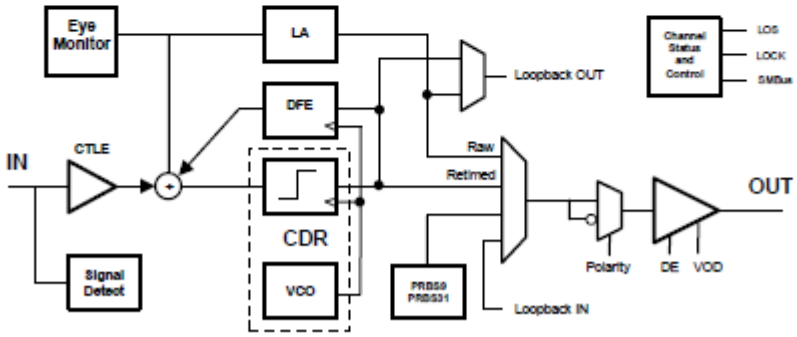


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 17	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 17	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 17	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

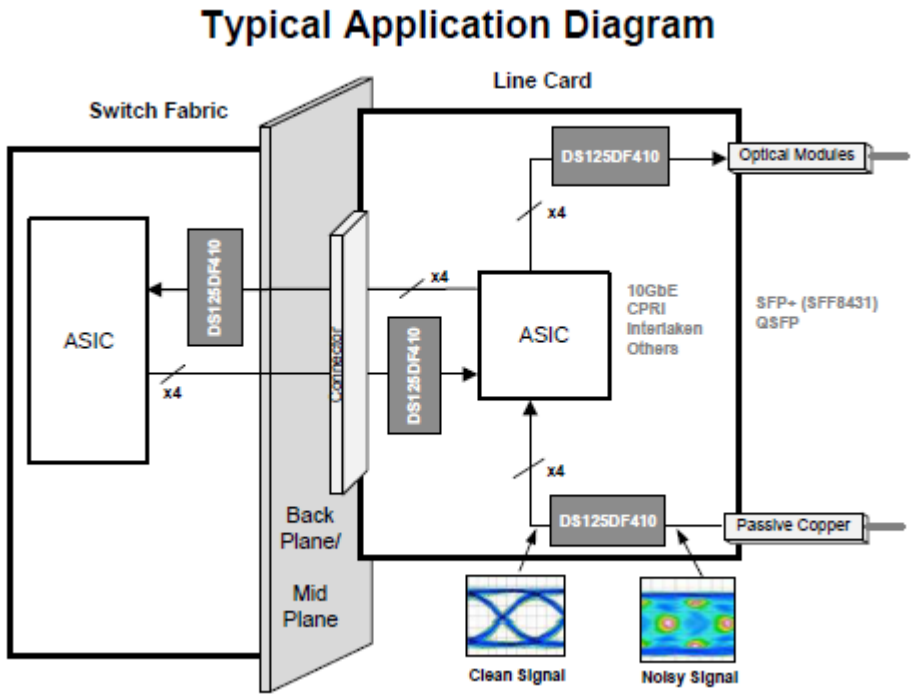
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

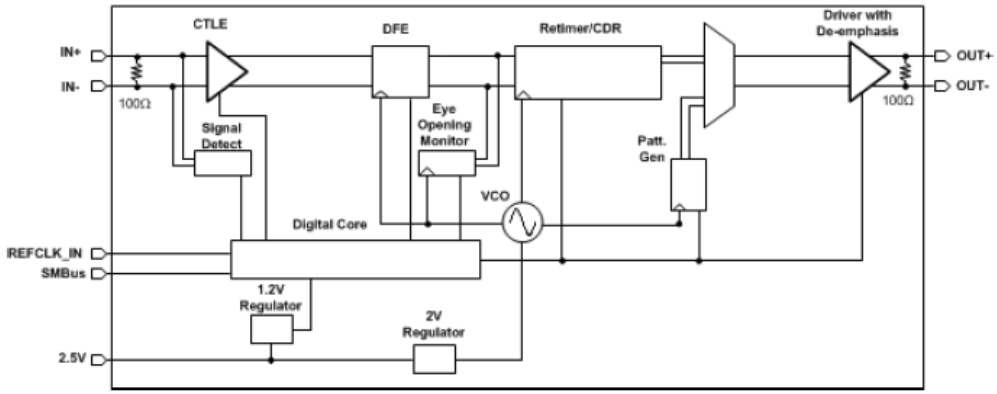
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 17	Disclosure
	 TI DS125DF410, 1.

Claim 17	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 17	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 17	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 17	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 17	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 17	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 17	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 17	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 17	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

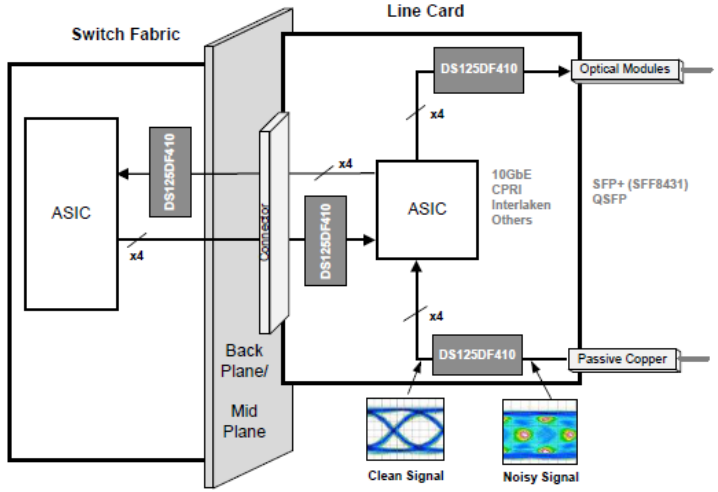
TI DS125DF410, 41.

Claim 17	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 17	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 17	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 17	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

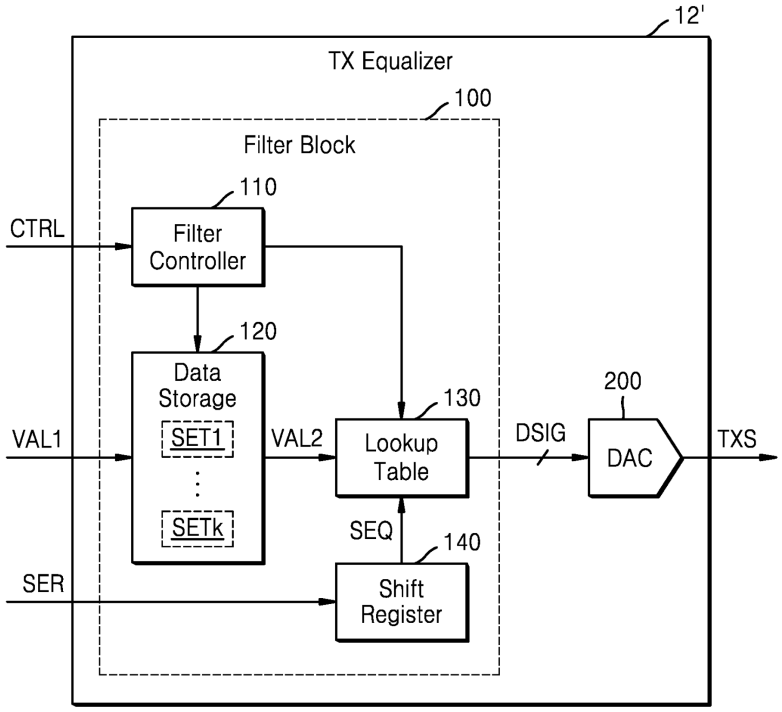
R. DEPENDENT CLAIM 18

Claim 18	Disclosure
18. The pluggable module transceiver of claim 17, wherein the performance characteristic is an error signal energy.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

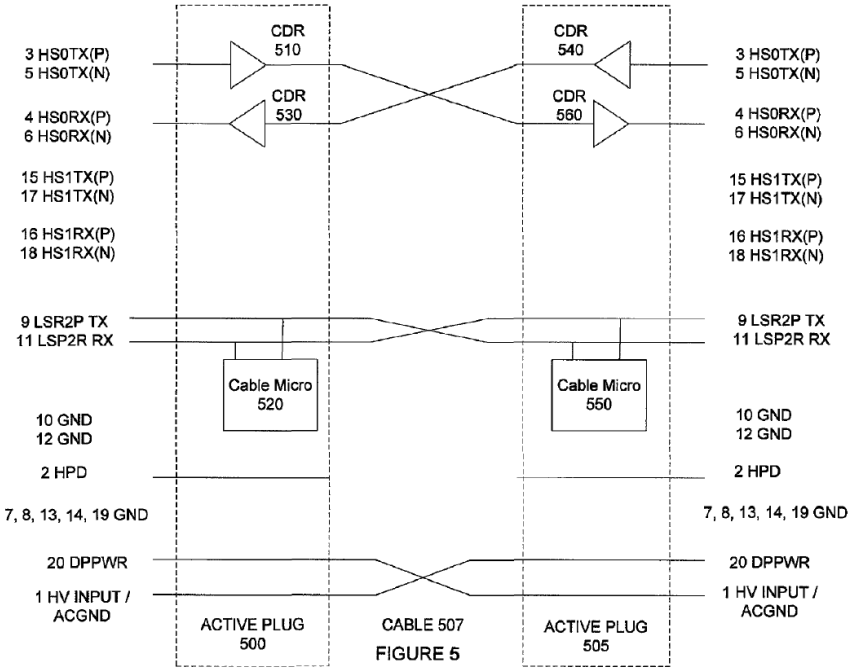
Claim 18	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 18	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

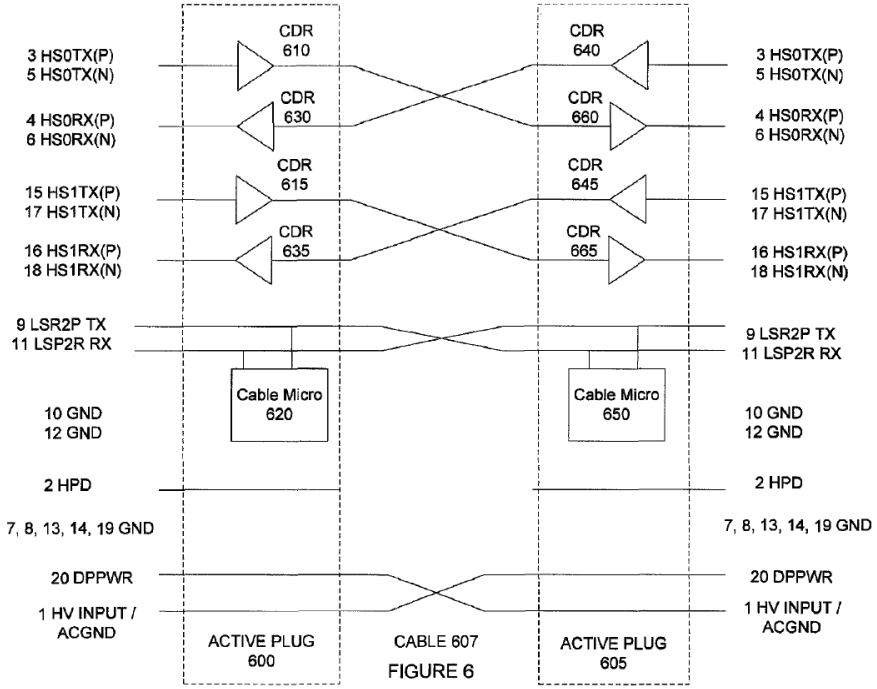
Claim 18	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 18	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 18	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 18	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 18	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 18	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 18	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 18	Disclosure

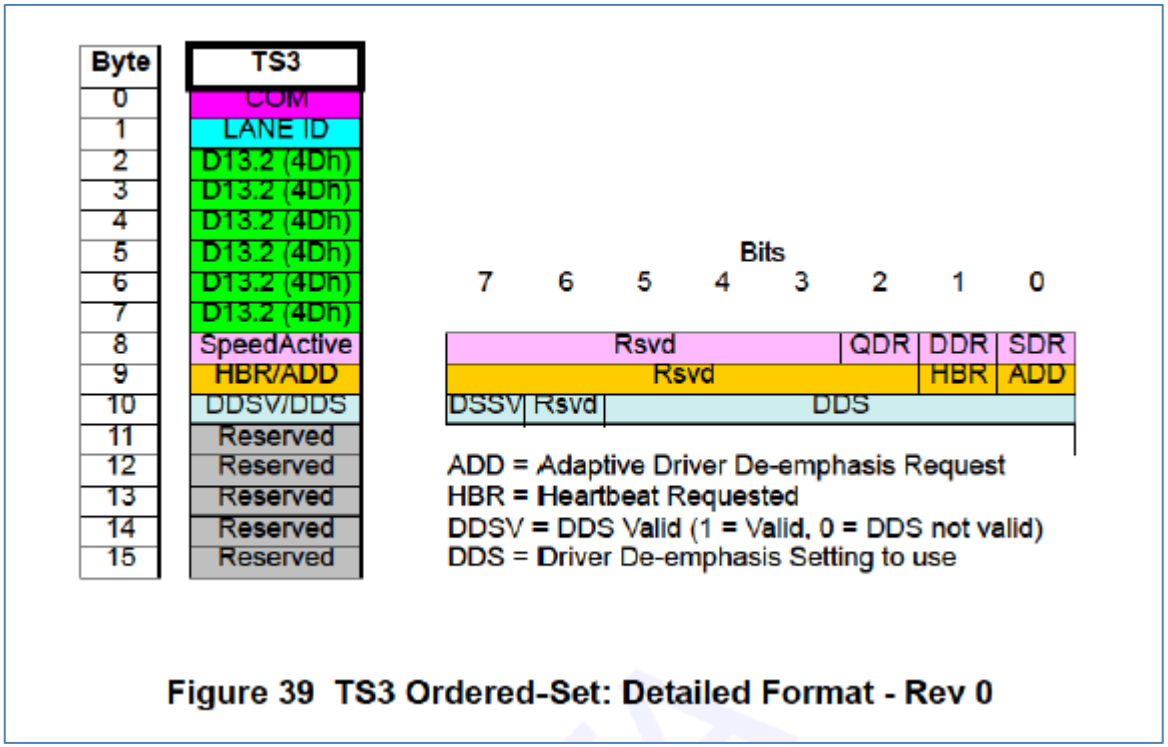
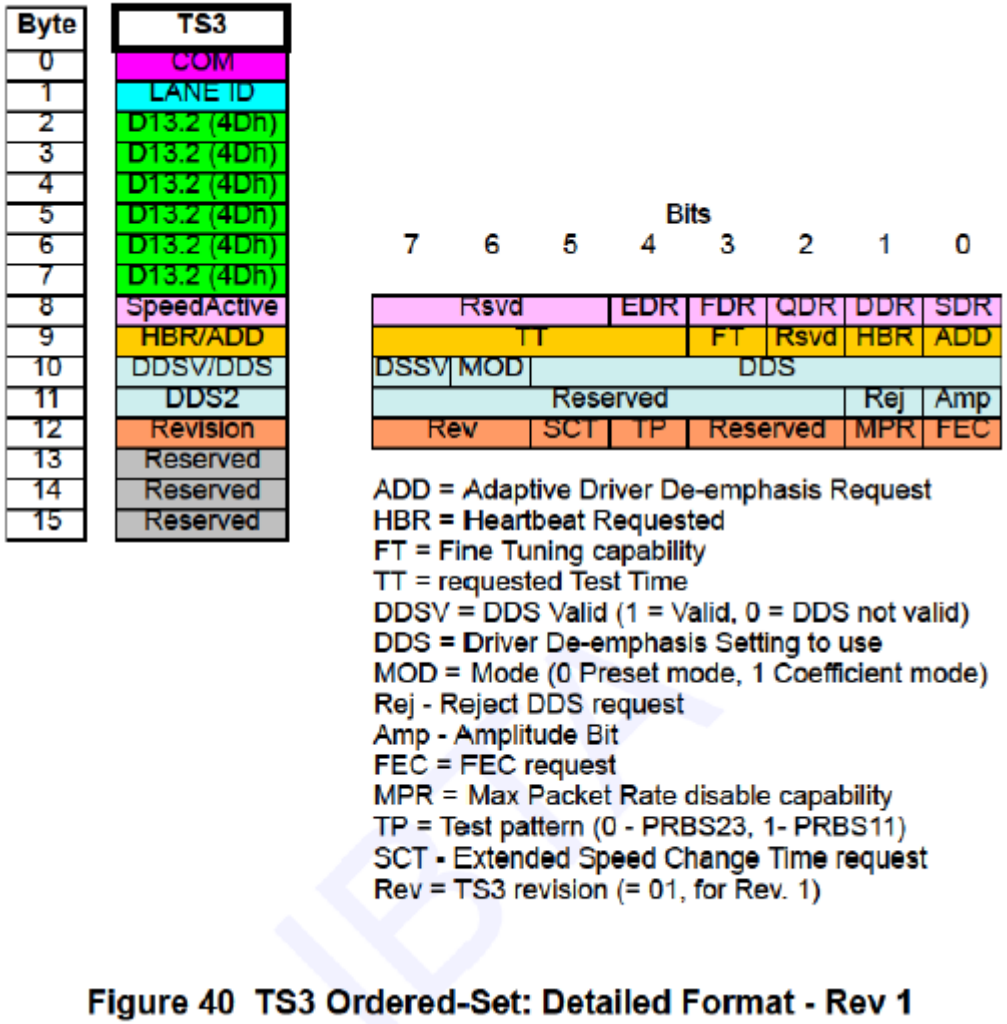


Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 18	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

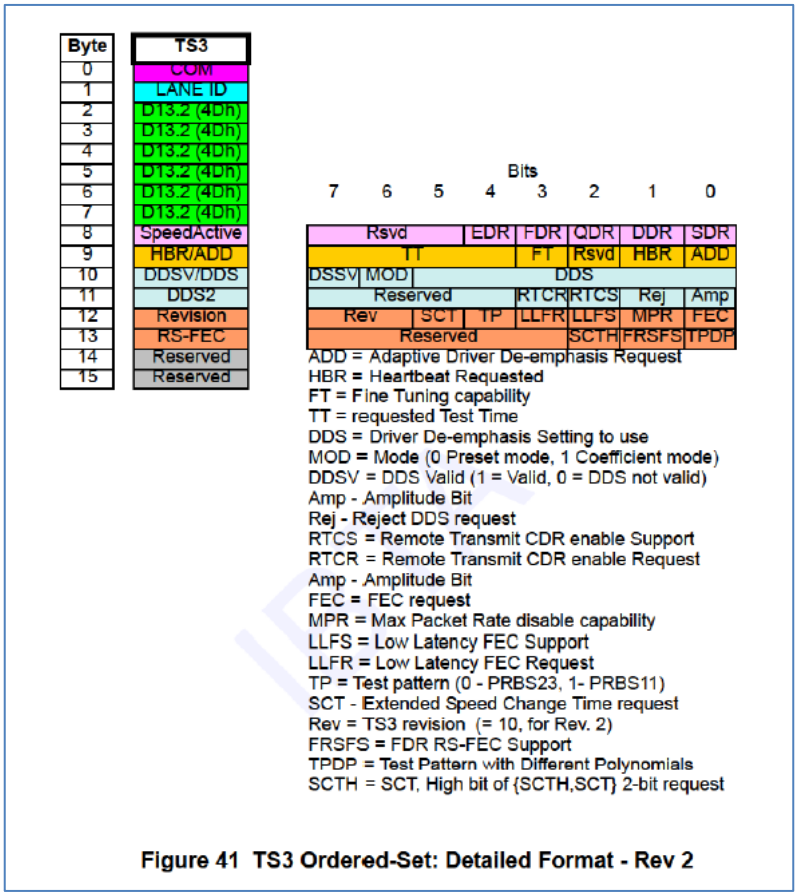
	Bits 7	6	5	4	3	2	1	0
	Rsvd			EDR	FDR	QDR	DDR	SDR
	TT				FT	Rsvd	HBR	ADD
	DSSV	MOD	DDS					
	Reserved						Rej	Amp
	Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 18	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 18	Disclosure
	5.5.2.4.1 REV 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 18	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 18	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 18	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 18	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 18	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 18	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

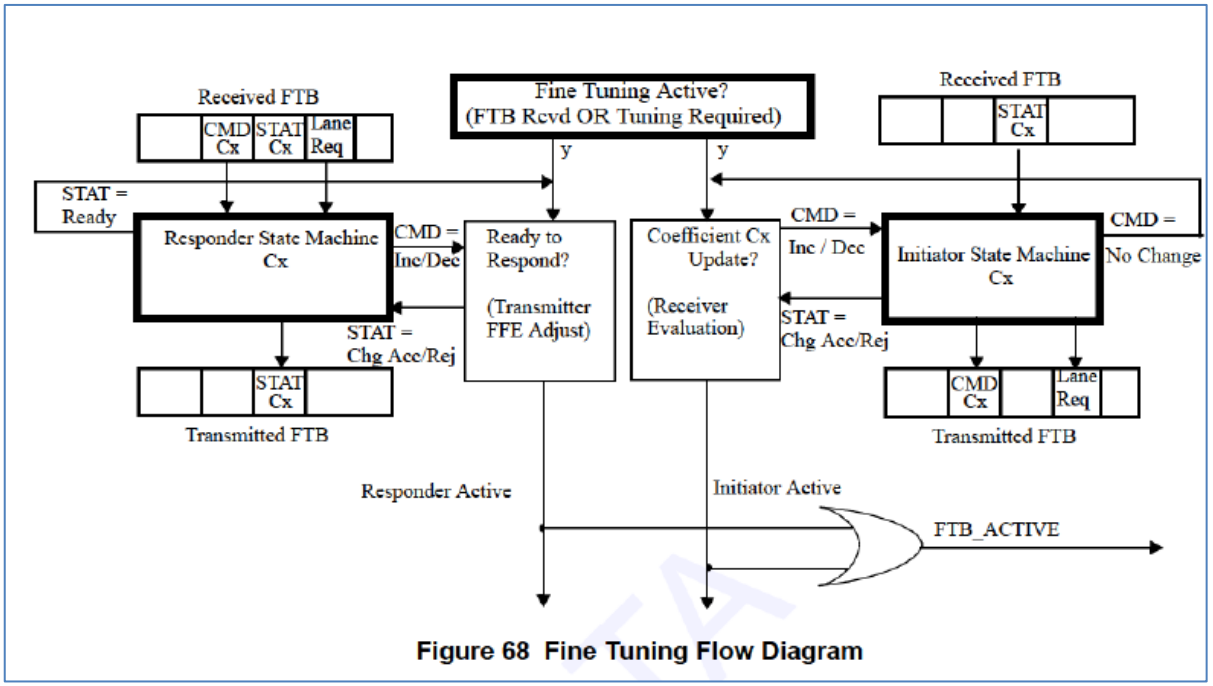
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 18	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 18	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 18	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 18	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 18	Disclosure
	Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7) InfiniBand, Table 142 (p. 528)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

Claim 18	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"Once the initial QAM modulation order and R-S FEC parameters have been set, the system enters a "tracking" or "maintenance" mode, as shown in detail in the process steps **400** illustrated in **FIG. 4.** Specifically, the process steps **400** utilize ongoing CMTS receiver measurements, such as bit error rates, modulation error rates, and power measurements, to continually recalculate and optimize various CMTS receiver parameters in each channel's profile."

Fox, p. 11.

	United States Patent No. 7,239,665 ("Mezer") Mezer "adapt[s]" equalizer coefficients "on the basis of an error signal" that "indicates deviation of the" received training signal "from a pre-determined ideal signal profile." *See, e.g.*, Mezer, 2:27-49, 3:5-7. That meets the claimed "error signal energy." *See* '111 Patent at 14:29-30 ("measur[ing] error signals" represents "the difference between the equalized receive signals and an idealized receive signal"). **1 Features** • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI

Claim 18	Disclosure
	TI DS110DF111, 1. **3 Description** The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 18	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

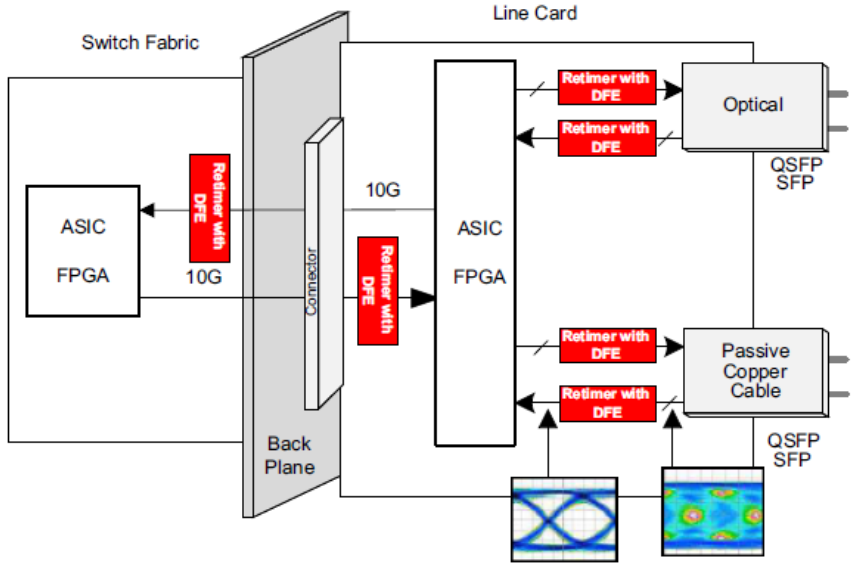
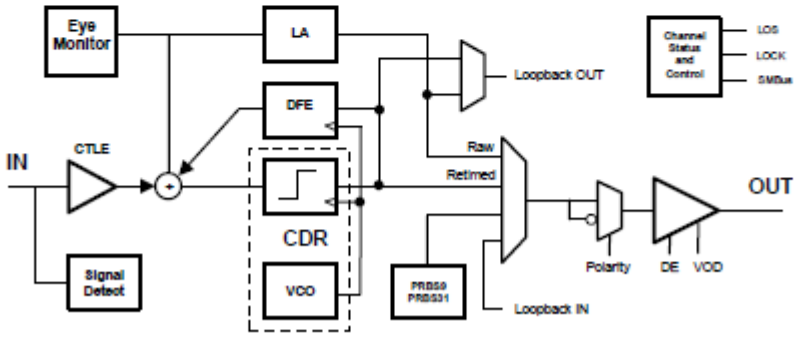


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 18	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 18	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 18	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

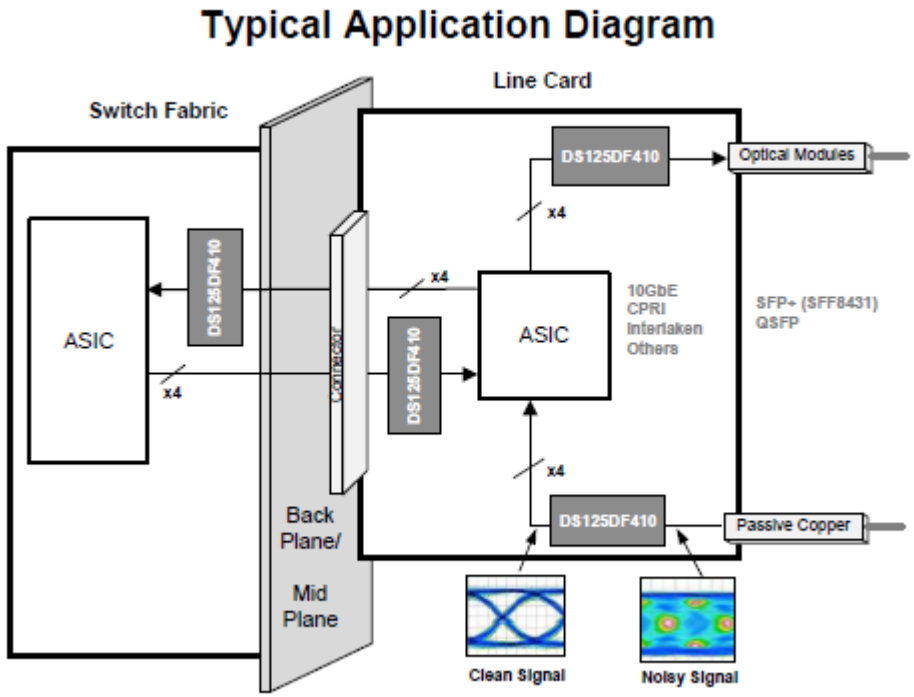
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

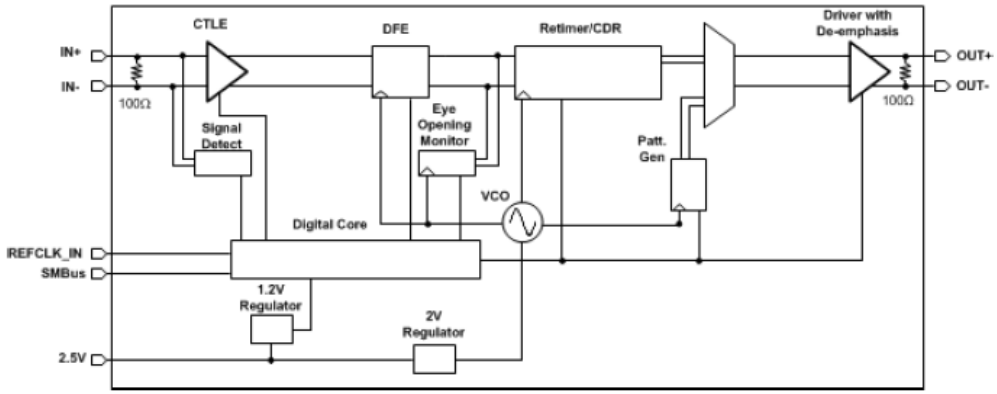
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 18	Disclosure
	 TI DS125DF410, 1.

Claim 18	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 18	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 18	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 18	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 18	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 18	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 18	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 18	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 18	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

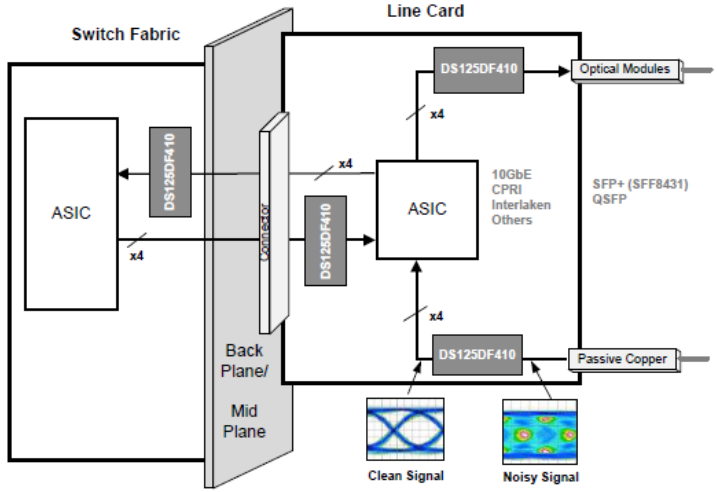
TI DS125DF410, 41.

Claim 18	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 18	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 18	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 18	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.

Exhibit C-12

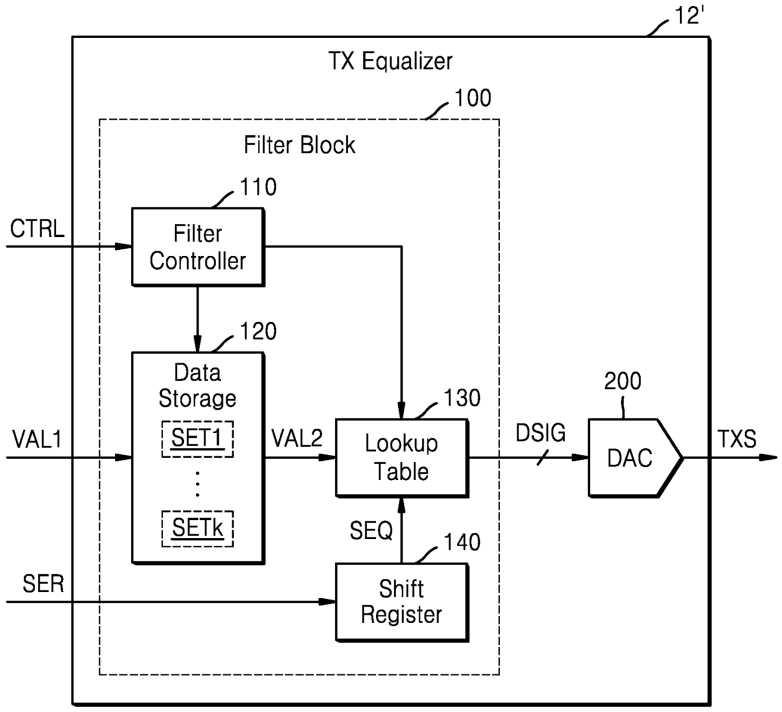
S. DEPENDENT CLAIM 19

Claim 19	Disclosure
19. The pluggable module transceiver of claim 17, wherein the performance characteristic is a bit error rate.	For example, and without limitation, at least under Credo's apparent infringement theory, the following obviousness references disclose this limitation based on at least the following exemplary citations: "The TX equalizer **12** may receive the serial data SER from the serializer **11** and may generate the TX signal TXS. The TX equalizer **12** may perform equalization to compensate for distortion of the serial data signal DIF**1** generated in the TX channel **7**, e.g., Inter-Symbol Interference (ISI). In some embodiments, the TX equalizer **12** may include a Finite Impulse Response (FIR) filter, as described below with reference to FIG. 2, and the FIR filter may generate a TX signal TXS by operating a symbol sequence extracted from serial data SER with a filter coefficient sequence. In high-speed serial communication such as 56 Gbps, the distortion of the serial data signal DIF**1** may be intensified, and thus the TX equalizer **12** may be required to perform sophisticated equalization. As described below, the TX equalizer **12** may implement by an FIR filter that provides high efficiency by using a lookup table LUT." Kang, 4:49-64. "The lookup table LUT included in the TX equalizer **12** may be refreshable, and the TX equalizer **12** may refresh the lookup table LUT based on the control signal CTRL received from the protocol processor **30**. For example, as described later with reference to FIG. 3, the TX equalizer **12** may select one of a plurality of filter coefficient sequences based on the control signal CTRL and may load a data set corresponding to the selected filter coefficient sequence to the lookup table LUT. Further, as will be described later with reference to FIG. 6 and the like, the TX equalizer **12** may extract the variation of the filter coefficient from the control signal CTRL and may refresh the lookup table LUT by adding the offset according to the variation of the filter coefficient. As such, the TX equalizer **12** may efficiently support protocols that define programmable equalization by using the refreshable lookup table LUT. In the present specification, the TX equalizer **12** may be referred to as an equalizer, and exemplary embodiments of the disclosure will be described primarily with reference to the TX equalizer **12**. However, it will be understood that the exemplary embodiments of the disclosure may also be applied to an equalizer which is different from the TX equalizer **12**, such as an RX equalizer **22** of the receiver **20**."

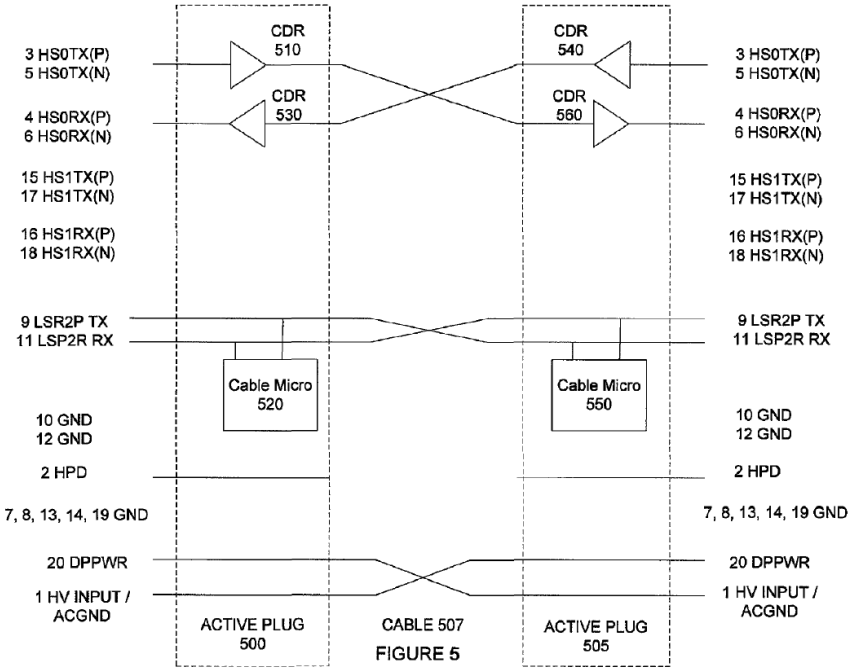
Claim 19	Disclosure
	Kang, 5:20-42. "FIG. 2 is a block diagram showing an example of a related-art FIR filter **9**. Specifically, FIG. 2 schematically illustrates the operation of the FIR filter **9** for generating the TX signal TXS from the serial data SER, and in the example of FIG. 2, the FIR filter **9** may operate as a 4-tap feed forward equalizer (FFE). The number and type of taps of the FIR filter **9** of the present application are not limited to this. The FIR filter **9** may calculate the symbol sequence in the serial data SER and a filter coefficient sequence including the filter coefficients of the FIR filter **9**. For example, as shown in FIG. 2, the symbol sequence may include four symbols S**1**, S**2**, S**3**, and S**4** corresponding to four filter coefficients C**1**, C**2**, C**3**, and C**4** of the filter coefficient sequence, respectively. The four symbols S**1**, S**2**, S**3**, and S**4** may be multiplied with the four filter coefficients C**1**, C**2**, C**3**, and C**4**, respectively, and the multiplication results may be summed. Namely, a result value Y according to a symbol sequence and a filter coefficient sequence may be calculated as shown in Equation 1 below. $Y=S1\cdot C1+S2\cdot C2+S3\cdot C3+S4\cdot C4$ [Equation 1] As such, as illustrated in FIG. 2, the serial data SER including symbols corresponding to the predetermined levels may be equalized as the TX signal TXS including a waveform modified according to the characteristics of the TX channel **7**." Kang, 6:14-35 "FIG. 3 is a block diagram illustrating a TX equalizer **12′** according to an exemplary embodiment of the disclosure. As described above with reference to FIG. 1, the TX equalizer **12′** of FIG. 3 may receive the serial data SER and the control signal CTRL, output the TX signal TXS, and may include a lookup table **130**. Hereinafter, FIG. 3 will be described with reference to FIG. 1. Referring to FIG. 3, the TX equalizer **12′** may include a filter block **100** and a digital-to-analog converter (DAC) **200**. The filter block **100** may generate a computed signal, i.e., a digital signal DSIG, from the filter coefficient sequence and the symbol sequence extracted from the serial data SER, as described above with reference to FIG. 2, and the DAC **200** may convert the digital signal DSIG into a TX signal TXS,

Claim 19	Disclosure
	which is an analog signal. The filter block **100** may include a controller **110**, a data storage **120**, the lookup table **130**, and a shift register **140**, as shown in FIG. 3. The shift register **140** may receive the serial data SER and may extract the symbol sequence SEQ from the serial data SER. An example of the operation of the shift register **140** will be described later with reference to FIG. 4." Kang, 7:1-22. "The data storage **120** may store values of the digital signal DSIG corresponding to possible values of the symbol sequence SEQ. The data storage **120** may have any structure for storing the values of the digital signal DSIG. The data storage **120** may include volatile memories, such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and the like in some embodiments, and may include nonvolatile memories such as Electrically Erasable Programmable Read-Only Memory (EEPROM), a flash memory, Phase Change Random Access Memory (PRAM), Resistance Random Access Memory (RRAM), a Nano Floating Gate Memory (NFGM), Polymer Random Access Memory (PoRAM), Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FRAM), and the like in some embodiments. The data storage **120** may also include a plurality of registers and may be referred to as a register set. An example of the values stored in the data storage **120** will be described later with reference to FIG. 5. In some embodiments, the values stored in the data storage **120** may be refreshed. For example, the data storage **120** may be rewritable. As illustrated in FIG. 3, the data storage **120** may receive a first value VAL**1** from outside the TX equalizer **12′** (e.g., the protocol processor **30** of FIG. 1), and as the first value VAL**1** is stored in the data storage **120**, the previously stored values may be changed. For example, the protocol processor **30** may store values of the digital signal DISG by providing the first value VAL**1** to the data storage **120** when the operation of the communication device **5** starts. In addition, the protocol processor **30** may generate the first value VAL**1** based on the RX data RXD. In some embodiments, the data storage **120** may store values of the digital signal DSIG grouped into a plurality of sets of data corresponding to a plurality of filter coefficient sequences. For example, as shown in FIG. 3, the data storage **120** may store a first to a k-th data sets SET**1** to SETk when k is an integer greater than 1, and the first to the k-th data sets SET**1** to SETk may store the same or different values of the digital signal DSIG for the same symbol sequence, respectively. For example, the protocol may predefine k filter coefficient sequences and define a process by which a transmitting side and a receiving

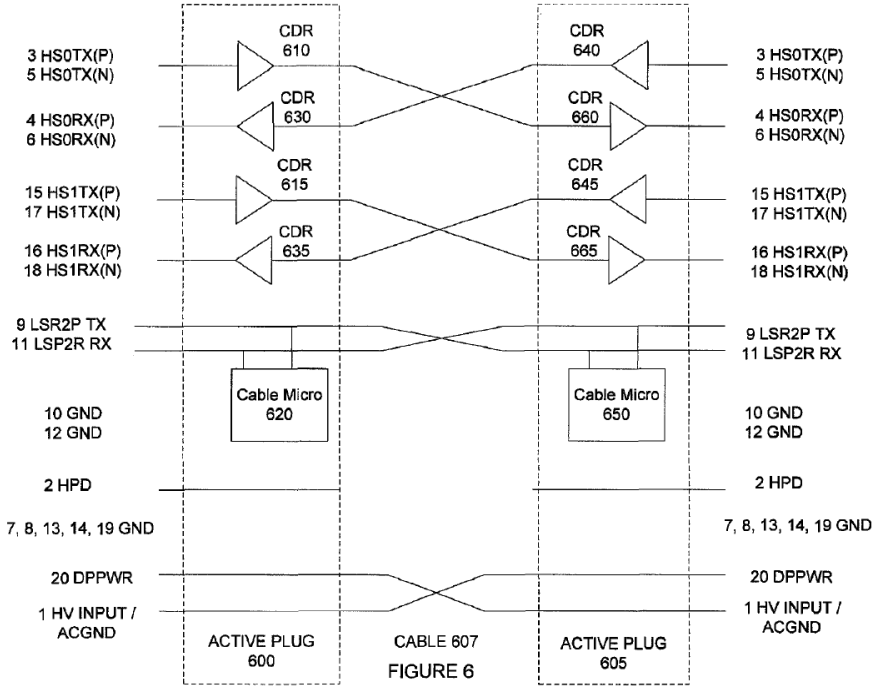
Claim 19	Disclosure
	side select one of the k filter coefficient sequences. The data storage **120** may store first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively. The lookup table **130** may output digital signals DSIG having a value corresponding to the symbol sequence SEQ. The lookup table **130** may include values of the digital signals DSIG, corresponding to possible values of the symbol sequence SEQ, for example, values corresponding to one of the first to k-th data sets SET**1** to SETk. For example, when 7-bit digital signals DSIG are provided to the DAC **200**, and the symbol sequence SEQ includes 4 symbols as 2-bit symbols according to 4-level pulse amplitude modulation (PAM**4**), one data set may include 256 pieces of data composed of 7 bits. In some embodiments, the lookup table **130** may be implemented as a memory that includes a cell array and receives the symbol sequence SEQ as an address. In some embodiments, the lookup table **130** may include a plurality of registers and may include a multiplexer which outputs values stored in at least some of the plurality of registers as digital signals DISG according to the symbol sequence SEQ. The controller **110** may receive the control signal CTRL and may control the data storage **120** and the lookup table **130**. The controller **110** may refresh the lookup table **130** by loading at least some of the values stored in the data storage **120** to the lookup table **130** in response to the control signal CTRL. For example, the protocol processor **30** may provide the TX equalizer **12′** with a control signal CTRL including information indicating one of the k filter coefficient sequences based on the RX data RXD. In response to the control signal CTRL, the controller **110** may control the data storage **120** to output the values included in one of the first to k-th data sets SET**1** to SETk corresponding to the k filter coefficient sequences, respectively, as a second value VAL**2** and may control the lookup table **130** to store the second value VAL**2** in the lookup table **130.**" Kang, 7:23-8:33.

Claim 19	Disclosure
	FIG. 3  Kang, FIG. 3 "FIG. 5 illustrates an active cable consistent with an embodiment of the present invention. For simplicity, only circuitry associated with the high-speed operation is shown. This cable includes two active plugs **500** and **505**, one on each end of cable **507**. Each active plug includes dual clock and data recovery circuits for retiming data. Specifically, active plug **500** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **520** may be used to configure clock and data recovery circuits **510** and **530** in active plug **500**.

Claim 19	Disclosure
	Similarly, active plug **505** provides high-speed transmission signals on pins **3** and **5**, and receives high-speed signals on pins **4** and **6**. A cable microcontroller **550** may be used to configure clock and data recovery circuits **540** and **560**. The clock and data recovery circuits may provide and receive signals in a variety of formats. For example, these circuits may include optical receivers and transmitters, such that cable **507** becomes a mix of fiber optic and electrical wires. In various embodiments of the present invention, the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate. Also, loopback paths may be included for diagnostic purposes. For example, the output of CDR **510** may be connected as an input to CDR **530**, while the output of CDR **540** may be an input to CDR **560**. This loopback path allows an HSIO device to determine the location of transmission errors as they arise. This loopback path may also be used in training or calibration routines, as described below. In other embodiments, the cable can self-communicate from end-to-end for diagnostic purposes. Other features that may be included for diagnostics include eye size measurements. In various embodiments of the present invention, the cable may be configured. In this specific embodiment of the present invention, circuitry in cable plug **500** may be configured using cable microcontroller **520**, while circuitry in cable plug **505** may be configured using cable microcontroller **550**. In other embodiments in the present invention, other circuits may be used to configure either or both plugs **500** and **505**. In this specific embodiment of the present invention, operational parameters, modes, and other aspects and characteristics of the plug circuitry may be configured. Information for this configuration may include parameters for control, diagnostics, tests, configuration, circuit monitoring, as well as other parameters. The ability to configure a cable in this way allows cables to adapt to new hosts and devices as the cable is used in various system applications. Information regarding the identification of cable type, vendor, and other identifying information may be available from hosts or devices and cables. Exchange of this information may be used to properly configure and drive circuitry in hosts or devices as well as cables.

Claim 19	Disclosure
	In this specific embodiment of the present invention, configuration and identification information may be read from and written to the cable using LSx signals on pins **9** and **11**, though in other embodiments of the present invention, other signal pins may be used. In various embodiments of the present invention, code in the cable microcontrollers **520** and **550** may be changed, reconfigured, upgraded, or updated. This code may be encrypted for security reasons. Also, data provided during a code change, reconfiguration, or update may be encrypted as well." Cornelius, 6:11-7:6  FIGURE 5 Cornelius, Figure 5

Claim 19	Disclosure
	"FIG. 6 illustrates an active cable consistent with an embodiment of the present invention. Again, only circuitry associated with the high-speed paths is shown for simplicity. In this example, additional clock and data recovery circuits **615** and **635** have been added to active plug **600**, while clock and data recovery circuits **645** and **665** have been added to active plug **605**. In these and other embodiments of the present invention, circuitry in the plugs may be powered by one or both of the devices being connected by the cable. For example, a host device connected to plug **600** may provide power for plugs **600** and **605**, as well as a host connected to plug **605**. In other examples, a device connected to plug **605** may receive a high voltage from a host connected to plug **600**, the device may provide power to plugs **600** and **605**. In still other examples, a host connected to plug **600** may provide power to plug **600** and a device connected to plug **605** may provide power to plug **605**. Specific examples of this can be found in co-pending U.S. patent application Ser. No. 13/173,979, titled Power Distribution Inside Cable, which is incorporated by reference. Again, embodiments of the present invention allow signals sharing pins between the two standards to not interfere with each other. Accordingly, embodiments of the present invention employ circuit components to help isolate the signal paths. Examples are shown in the following figures." Cornelius, 8:20-45

Claim 19	Disclosure
	 FIGURE 6 Cornelius, Figure 6 "In various embodiments of the present invention, the reliability and accuracy of data connections may be improved by calibrating or training circuitry in the hosts, cables, and other devices. This circuitry may include circuits to compensate for cable skew, cross talk (particularly in a connector), channel compensation (such as equalization or cancellation of reflections), and other such circuitry. These circuits may be adjusted using various parameters. In various embodiments of the present invention, parameters for these circuits may be calibrated or otherwise determined by the manufacture and stored as presets for loading during operation. In other embodiments of the present invention, these parameters may be determined while the system is connected. This training or calibration may occur during power up, restart, or other periodical or event-based time. These or other routines may be used to calibrate the path from a

Claim 19	Disclosure
	host to a near end of the cable, the path through the cable, and the path from the cable to a device or other host." Cornelius, 11:45-63 **5.5.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)** Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, TS3 revision, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, request extended speed change time and requested test time, and a byte describing the transmitter de-emphasis/preset or coefficients setting which should be used, FEC request bit, select of test pattern, fine tuning ability and max packet rate disable ability followed by four reserved bytes. The lane identifiers used by TS3 are defined in Table 24. The format of the TS3 ordered-set is shown in Figure 39 on page 145 and Figure 40 on page 146 below. The use of the TS3 ordered-set is described in Section 5.8.4.6, "Configuration States - Enhanced Signaling," on InfiniBand, p. 144:27-145:1

Claim 19	Disclosure

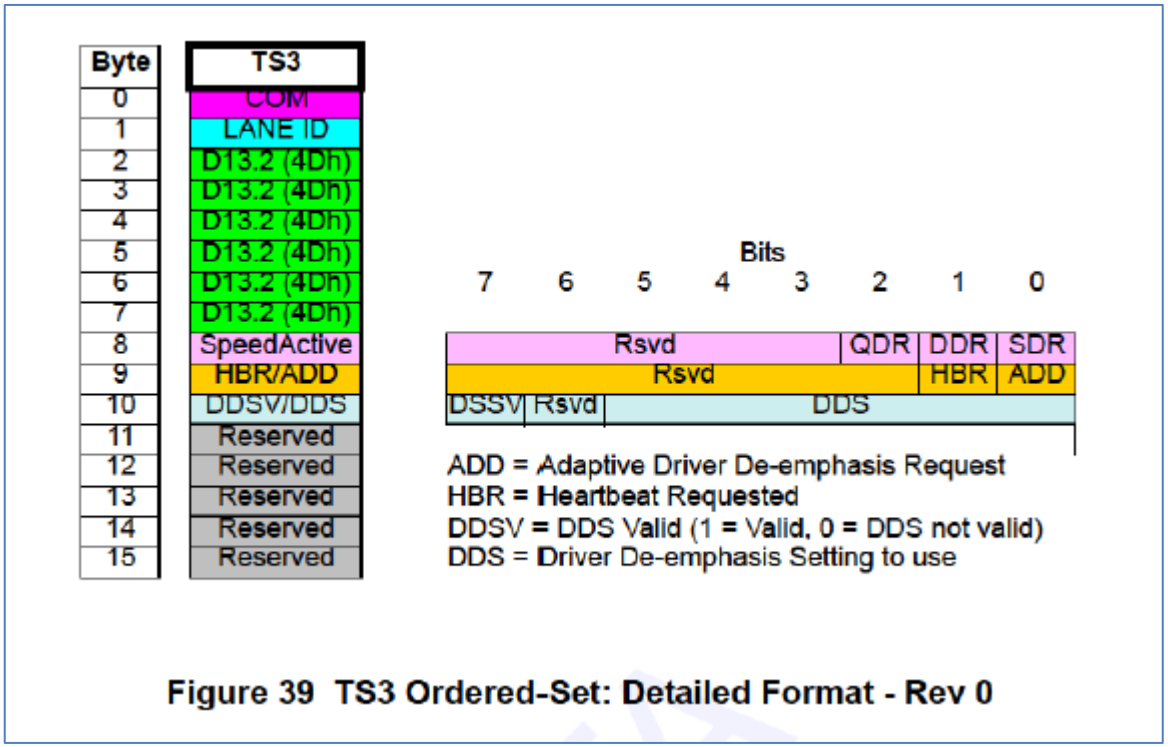


Figure 39 TS3 Ordered-Set: Detailed Format - Rev 0

InfiniBand, Figure 39 (p. 145)

Claim 19	Disclosure

Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	Reserved
14	Reserved
15	Reserved

Bits

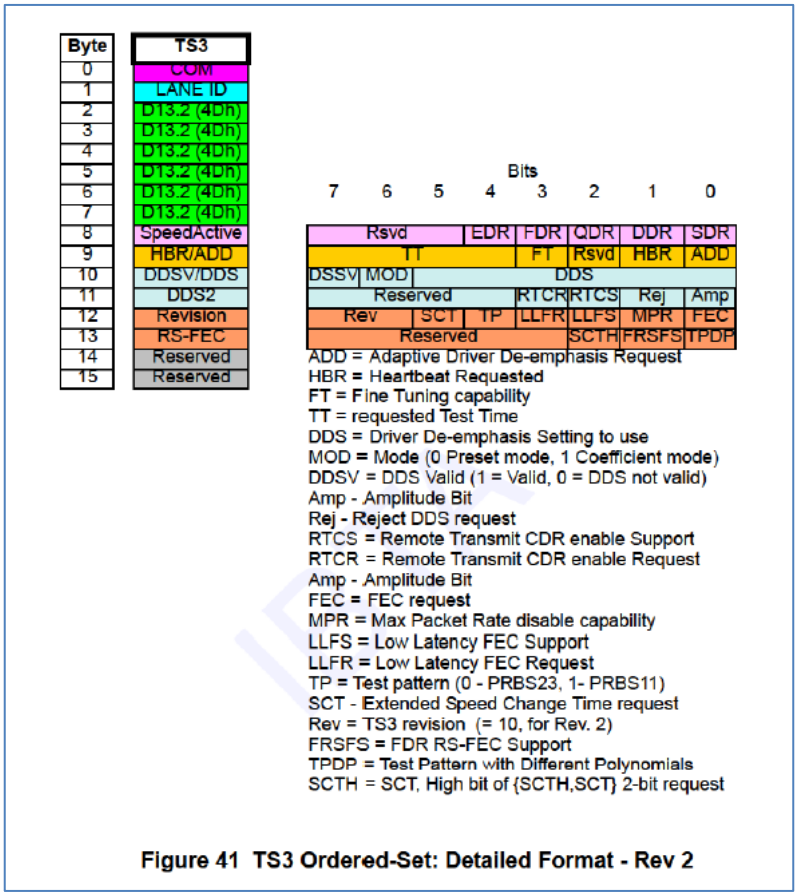
7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved						Rej	Amp
Rev		SCT	TP	Reserved		MPR	FEC

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
Rej - Reject DDS request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 01, for Rev. 1)

Figure 40 TS3 Ordered-Set: Detailed Format - Rev 1

InfiniBand, Figure 40 (p. 146)

Claim 19	Disclosure



Byte	TS3
0	COM
1	LANE ID
2	D13.2 (4Dh)
3	D13.2 (4Dh)
4	D13.2 (4Dh)
5	D13.2 (4Dh)
6	D13.2 (4Dh)
7	D13.2 (4Dh)
8	SpeedActive
9	HBR/ADD
10	DDSV/DDS
11	DDS2
12	Revision
13	RS-FEC
14	Reserved
15	Reserved

Bits

7	6	5	4	3	2	1	0
Rsvd			EDR	FDR	QDR	DDR	SDR
TT				FT	Rsvd	HBR	ADD
DSSV	MOD	DDS					
Reserved				RTCR	RTCS	Rej	Amp
Rev		SCT	TP	LLFR	LLFS	MPR	FEC
Reserved					SCTH	FRSFS	TPDP

ADD = Adaptive Driver De-emphasis Request
HBR = Heartbeat Requested
FT = Fine Tuning capability
TT = requested Test Time
DDS = Driver De-emphasis Setting to use
MOD = Mode (0 Preset mode, 1 Coefficient mode)
DDSV = DDS Valid (1 = Valid, 0 = DDS not valid)
Amp - Amplitude Bit
Rej - Reject DDS request
RTCS = Remote Transmit CDR enable Support
RTCR = Remote Transmit CDR enable Request
Amp - Amplitude Bit
FEC = FEC request
MPR = Max Packet Rate disable capability
LLFS = Low Latency FEC Support
LLFR = Low Latency FEC Request
TP = Test pattern (0 - PRBS23, 1- PRBS11)
SCT - Extended Speed Change Time request
Rev = TS3 revision (= 10, for Rev. 2)
FRSFS = FDR RS-FEC Support
TPDP = Test Pattern with Different Polynomials
SCTH = SCT, High bit of {SCTH,SCT} 2-bit request

Figure 41 TS3 Ordered-Set: Detailed Format - Rev 2

InfiniBand, Figure 41 (p. 147)

Claim 19	Disclosure
	5.5.2.4.1 Rev 0 TS3 Symbol 8, the *SpeedActive* link speed identifier, is used to identify and advertise the speeds at which the Link/Phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the ***SM.PortInfo(LinkSpeedEnabled)*** field. Symbol 9 indicates whether the sender is requesting adaptive driver de-emphasis (ADD), and whether heartbeat is enabled and requested (HBR). InfiniBand, p. 147:34-42 Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in Section 6.5.2, "Equalization for InfiniBand Release 1.2.1 Devices," on page 281 and Section 6.5.3, "Equalization for InfiniBand Release 1.3 Devices," on page 283. Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver. The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101100 0101) for both the positive and negative running disparity. InfiniBand, p. 148:1-13

Claim 19	Disclosure
	Implementation Note With a multi lane port some lanes may complete the equalization training process before other lanes. When a single lane requires equalization training the port will request equalization training by setting the ADD bit in byte 9 on all lanes of the port. Lanes that have completed the equalization training shall clear the DDSV bit in byte 10 to indicate than no change to the peer transmitter setting is required. InfiniBand, p. 150:2-10 **5.8.2 LINK INITIALIZATION AND TRAINING OPTIONS** Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections. InfiniBand, p. 192:29-35

Claim 19	Disclosure
	The TS3 exchange is also used to establish whether adaptive driver de-emphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. At QDR and lower bit rates for equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4 ms duration each. On each 4 ms slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver. At bit rates higher than QDR for equalization training, each transmitter sends PRBS23 or PRBS11 at the maximum speed commonly active in both ports (FDR or EDR), for a pre-negotiated time. The generation of the transmitted PRBS is described in Section 5.8.4.6.6.14, "PRBS Test Pattern," on page 218. The pre-negotiated time is achieved by choosing the highest Test Time (TT) advertised in the TS3 by both ports, the test encoding is described in Table 41 on page 192. The receiver should perform a receiver test to determine if the current transmitter setting is optimal and sufficient for the tested speed, the receiver test, equalization and decision protocol is outside the scope of this specification. The receiver should allow for stabilization time at the start and end of the test time. At the start a receiver shall allow for at least 4 ms stabilization time when [SCTH,SCT]=[0,0] and 16, 32, or 64 ms, when [SCTH,SCT]=01, 10, or 11, respectively. At the end of the test time the receiver stabilization time is undefined but it is recommended to use a 4 ms stabilization time. The stabilization time shall not be used by the receiver for receiver testing. InfiniBand, 205:5-31

Claim 19	Disclosure
	Implementation Note: Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium. Achieving ideal adaptive equalization over different backplanes and over the wide variety of copper and optical media of the various distances used for InfiniBand™ links is a very complex problem. The algorithm described here for QDR and lower speeds (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each), and the algorithm for FDR and EDR speeds (combination of Preset setting options, High- and Low-Amplitude ranges, and incremental changes to the C_{-1}, C_0, and C_{+1} tap weights during link initialization, as well the Fine Tuning Algorithm for incremental adjustment while the link is operational) provides mechanisms for both transmitter and receiver equalization with moderate complexity. The algorithms also allow interoperability with ports that don't implement adaptive equalization. Since the maximum physical length of an InfiniBand link at Rel. 1.3, using single mode optical fiber links, is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this amount. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in Section 5.8.5, "State Machine Delays and Timeouts," on page 226, the window of proper transmitter-equalized data within the 4 ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots. InfiniBand, 208:15-42

Claim 19	Disclosure
	A port may be connected to a medium that requires speed dependent configuration such as equalization configuration or CDR control. In addition, a port that supports remote Remote Transmit CDR enable (Transmitted RTCS is set) shall set the medium transmit CDR setting based on the received Transmit CDR enable Request (RTCS). Setting the attached medium properties may require additional setting time and stabilization time. The transmitter port shall guarantee that the medium settings are applied and that a valid training pattern is transmitted out of the attached physical medium by the end of the 4, 16, 32, or 64 ms speed change time. The remaining test time is used for receiver test. It is highly recommended that an implementation will stop its equalization process some time before the completion of the test time to ensure that all the equalization is performed while the peer port is in Config.Test. The transmitter equalization is set to the preset or coefficients requested in the received TS3 in Config.CfgEnhanced state. The receiver attempts to receive PRBS23 or PRBS11 while optionally adjusting receiver equalization settings. InfiniBand, 216:21-33

Claim 19	Disclosure
	5.13 FINE TUNING For FDR and higher data rate devices, a fine tuning algorithm is defined to allow for minor transmitter equalization adjustments while the link is up, to account for temperature variation or improve on very high bit error ratios. Fine tuning is allowed during LinkUp as a background process while normal data and link packets are flowing. Either link partner is allowed to initiate a sequence of commands to adjust their link partner's transmitter coefficients. The incremental change of each fine tuning request is intended to be small enough that link errors are avoided and traffic flow is not affected. This section covers the parametric exchange protocol but leaves the management of the coefficient changes and receiver evaluation to vendor-specific implementations. **o5-5:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the Fine Tuning capability as defined in Section 5.13, "Fine Tuning," on page 247. InfiniBand, 247:24-38

Claim 19	Disclosure

For FIR tap definition see Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, and Section 6.6.5.1, "FDR Transmitter Equalizer Implementation," on page 297.

FTB CMD (Byte 2)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

Each 2 bit field:

00 - No Change
01 - Increase
10 - Decrease
11 - Reserved

FTB STAT (Byte 3)

[1:0] - C_{+1} FIR Tap
[3:2] - C_0 FIR Tap
[5:4] - C_{-1} FIR Tap
[7:6] - Reserved

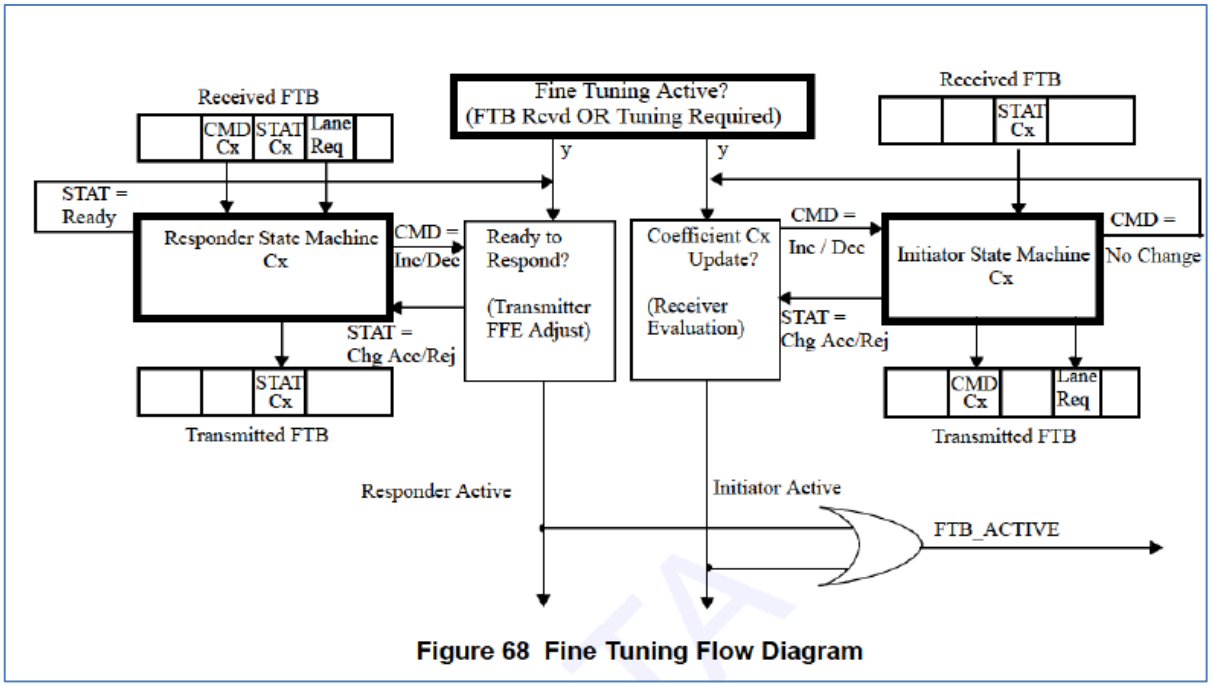
Each 2 bit field:

00 - Ready
01 - Change Accept
10 - Change Reject
11 - Reserved

FTB Lane Req (Byte 5)

[7:0] - Lane Identifier - Uses the Lane ID mapping described in Table 24 on page 144.

InfiniBand, p. 248:3-36

Claim 19	Disclosure
	 **Figure 68 Fine Tuning Flow Diagram** InfiniBand, Figure 68 (p. 250)

Claim 19	Disclosure
	5.16 FDR AND HIGHER RATE TRANSMITTER EQUALIZATION An transmitter capable of FDR or higher data rates shall implement a coefficient-based equalization mode in order to support fine-grained control over Tx equalization resolution. Additionally, a transmitter shall support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via the equalization process in Config.CfgEnhanced, as described in Section 5.8.4.6.5, "Config.CfgEnhanced State - Release 1.3.1 Enhanced Signaling," on page 212. The coefficient space is also controllable via the fine tuning algorithm described in Section 5.13, "Fine Tuning," on page 247. All transmitters must implement support for the equalization procedure, whereas receivers may optionally implement it. Implementation of transmitter equalization is described in Section 6.6.5, "Host Driver Output Characteristics for FDR," on page 294 and Section 6.6.6, "Host Driver Output Characteristics for EDR," on page 303. **o5-7:** All ports claiming compliance with InfiniBand Rel. 1.3 shall implement the FDR and Higher Rate Transmitter Equalization capability as defined in Section 5.16, "FDR and Higher Rate Transmitter Equalization," on page 257, for FDR and higher data rates. InfiniBand, 250:9-27

Claim 19	Disclosure

8.5 QSFP+ Memory Map

The memory map for QSFP+ is summarized in Figure 163.

Lower Page (1010 000x) - Required			
Addr	**Size**	**Type**	**Functions**
0-2	3	RO	ID and status
2-21	19	RO	Interrupt Flags
22-23	12	RO	Module Monitor - Temperature
26-27	12	RO	Module Monitor - Voltage
30-33	4	RO	Vendor Specific
34-41	8	RO	Channel Monitors - Rx Input Optical Power
42-49	8	RO	Ch. Monitors - Tx Bias Current
50-57	8	RO	Ch Monitors - Tx Optical Power
66-81	16	RO	Vendor Specific
86-97	12	R/W	Control
100-106	7	R/W	Module and Channel Mask
108-111	4	R/W	Free Side Device Properties
119-122	4	R/W	Password Change Entry Area
123-126	4	R/W	Password Entry Area
127	1	R/W	Upper Page Select Byte (00h, 01h, 02h, or 03h)

Upper Page 00 - Required			
Addr	**Size**	**Type**	**Functions**
128-191	64	RO	Base ID Fields
192-223	32		Extended ID Fields
224-255	32		Vendor Specific ID

Upper Page 01 - Optional			
Addr	**Size**	**Type**	**Functions**
128	1	RO	CC_APPS: Check code for the Application Select Table
129	1		AST Table Length (TL) (TL Range: 0-62)
130-131	2		Application Code Entry 0
132-133	2		Application Code Entry 1
other Application Code Entries			
130+2*TL-131+2*TL	2		Application Code Entry TL
Remainder			Reserved

Upper Page 02 - Optional			
Addr	**Size**	**Type**	**Functions**
128-255	128	R/W	User EEPROM Data If Upper Page 00 byte 129 bit 4 is set, bytes 128-137 store the CLEI code for the module.

Upper Page 03 - Optional for Cable Assemblies			
Addr	**Size**	**Type**	**Functions**
128-175	48	RO	Module Device Thresholds
176-223	48	RO	Channel Threshold
224	1	RO	Tx EQ & Rx Emphasis Magnitude
226-233	12	RW	Vendor Specific Channel Controls
234-241	4	RW	Channel Controls: Tx equalization, Rx emphasis, Rx amplitude, Tx/Rx squelch, Rx output disable
242-253	12	RW	Channel Monitor Masks
254-255	2	RW	Reserved

Notes:

RO = Read-Only,
R/W = Read/Write

Ranges not specified are Reserved

The term "Module" in this specification corresponds to the term "Free Side Device" (or "Module") in the SFF-8636 documentation.

Figure 163 QSFP+ Memory Map

InfiniBand, p. 489

Claim 19	Disclosure

234	7:4	Tx1 input equalization	Transmitter Input equalization levels 1111-1011: Reserved 1010, 1001, 1000: 10, 9, 8 dB - not required for InfiniBand modules 0111: 7 dB 0110: 6 dB 0101: 5 dB 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No EQ Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Tx2 input equalization		O	0000b	O	0000b
235	7:4	Tx3 input equalization		O	0000b	O	0000b
	3:0	Tx4 input equalization		O	0000b	O	0000b

InfiniBand, Table 141 (p. 512)

Table 141 QSFP+ upper page 03 memory map (Sheet 3 of 5)

Address (Byte number)	Bit (s)	Name	Comment	Passive copper, Active Copper, Active Optical		Optical Module	
				R/O/C	Default	R/O/C	Default
236	7:4	Rx1 output emphasis	Receiver Output Emphasis levels 1xxx: Vendor Specific 0111, 0110, 0101: 7, 6, 5 dB - not required for InfiniBand modules 0100: 4 dB 0011: 3 dB 0010: 2 dB 0001: 1 dB 0000: 0 dB - No Emphasis Where the specification compliance given in bytes 131 -138 or byte 192 defines input equalization ranges (for example, CEI-28G-VSR), that specification takes precedence.	O	0000b	O	0000b
	3:0	Rx2 output emphasis		O	0000b	O	0000b
237	7:4	Rx3 output emphasis		O	0000b	O	0000b
	3:0	Rx4 output emphasis		O	0000b	O	0000b

InfiniBand, Table 141 (p. 513)

Claim 19	Disclosure

Table 142 CXP Tx Lower Page Memory Map (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/- (Not Applicable)		
					Passive	Active Electrcl	Active Optical
62 3Eh	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
	3-0	Input Equalization Tx10					
63 3Fh	7-4	Input Equalization Tx09					
	3-0	Input Equalization Tx08					
64 40h	7-4	Input Equalization Tx07					
	3-0	Input Equalization Tx06					
65 41h	7-4	Input Equalization Tx05					
	3-0	Input Equalization Tx04					
66 42h	7-4	Input Equalization Tx03					
	3-0	Input Equalization Tx02					
67 43h	7-4	Input Equalization Tx01					
	3-0	Input Equalization Tx00					

InfiniBand, Table 142 (p. 528)

Claim 19	Disclosure

Table 143 CXP Rx Lower Page Memory Map (Optional) (Sheet 6 of 7)

Byte	Bit	Name	Description	Type	Required/Optional/ Conditional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output De-emphasis Rx11	Rx Output De-emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale De-emphasis. Writing 0000b calls for minimum De-emphasis. Writing intermediate code values calls for intermediate levels of De-emphasis.	RW	-	O	O
	3-0	Output De-emphasis Rx10					
69 45h	7-4	Output De-emphasis Rx09					
	3-0	Output De-emphasis Rx08					
70 46h	7-4	Output De-emphasis Rx07					
	3-0	Output De-emphasis Rx06					
71 47h	7-4	Output De-emphasis Rx05					
	3-0	Output De-emphasis Rx04					
72 48h	7-4	Output De-emphasis Rx03					
	3-0	Output De-emphasis Rx02					
73 49h	7-4	Output De-emphasis Rx01					
	3-0	Output De-emphasis Rx00					

InfiniBand, Table 143 (p. 535)

"Once the initial QAM modulation order and R-S FEC parameters have been set, the system enters a "tracking" or "maintenance" mode, as shown in detail in the process steps **400** illustrated in **FIG. 4.** Specifically, the process steps **400** utilize ongoing CMTS receiver measurements, such as bit error rates, modulation error rates, and power measurements, to continually recalculate and optimize various CMTS receiver parameters in each channel's profile."

Fox, p. 11.

Claim 19	Disclosure
	1 Features • Pin-Compatible Retimer Family – DS110DF111 With DFE: 8.5 to 11.3 Gbps – DS125DF111 With DFE: 9.8 to 12.5 Gbps • Adaptive CTLE Up to 34 dB Boost at 5.65 GHz • Self-Tuning 5-Tap DFE • Raw Equalized and Retimed Data Loopback • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Settable TX De-Emphasis Driver 0 to –12 dB • Low Power Consumption: 200 mW/Channel • Locks to Half, Quarter, and Eighth Data Rates for Legacy Support • On-Chip Eye Monitor (EOM), PRBS Generator • Input Signal Detection, CDR Lock Detection/Indicator • Single 3.3-V or 2.5-V ±5% Power Supply • SMBus, EEPROM, or Pin-Based Configuration • 4.0-mm × 4.0-mm, 24-Pin QFN Package • Operating Temp Range: –40°C to 85°C **2 Applications** • Front Port Optical Interconnects • SFF-8431 • 10G/1G Ethernet • CPRI TI DS110DF111, 1.

Claim 19	Disclosure
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. TI DS110DF111, 1.

Claim 19	Disclosure

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

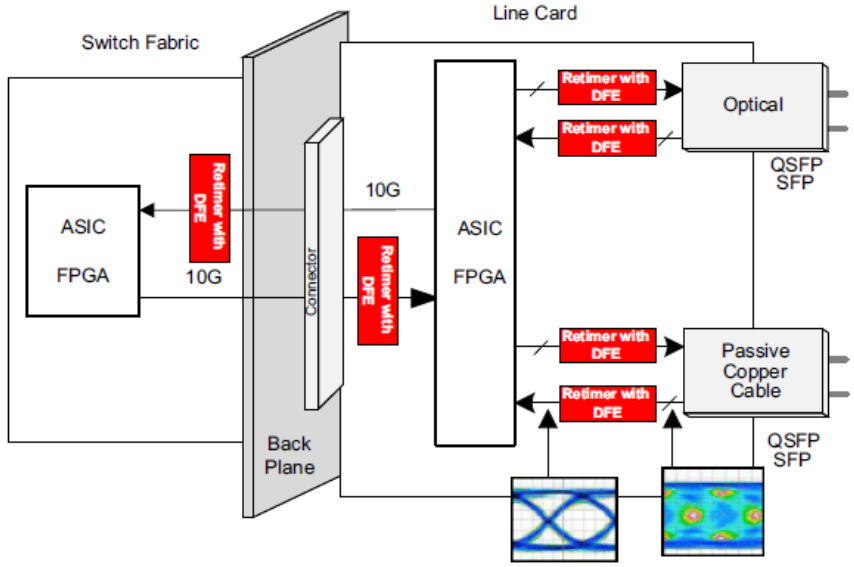
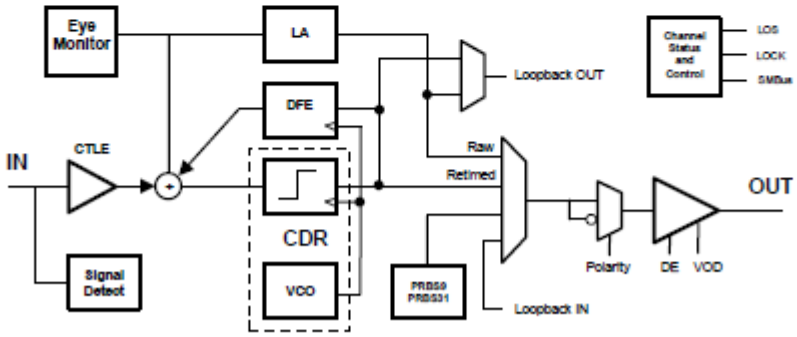


Figure 9. Typical Application

TI DS110DF111, 43.

Claim 19	Disclosure
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. **7.2 Functional Block Diagram**  Figure 6. DS110DF111 Data Path Block Diagram TI DS110DF111, 10.

Claim 19	Disclosure
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. TI DS110DF111, 10-11.

Claim 19	Disclosure

7.5.1.26 Setting the Output De-Emphasis Setting

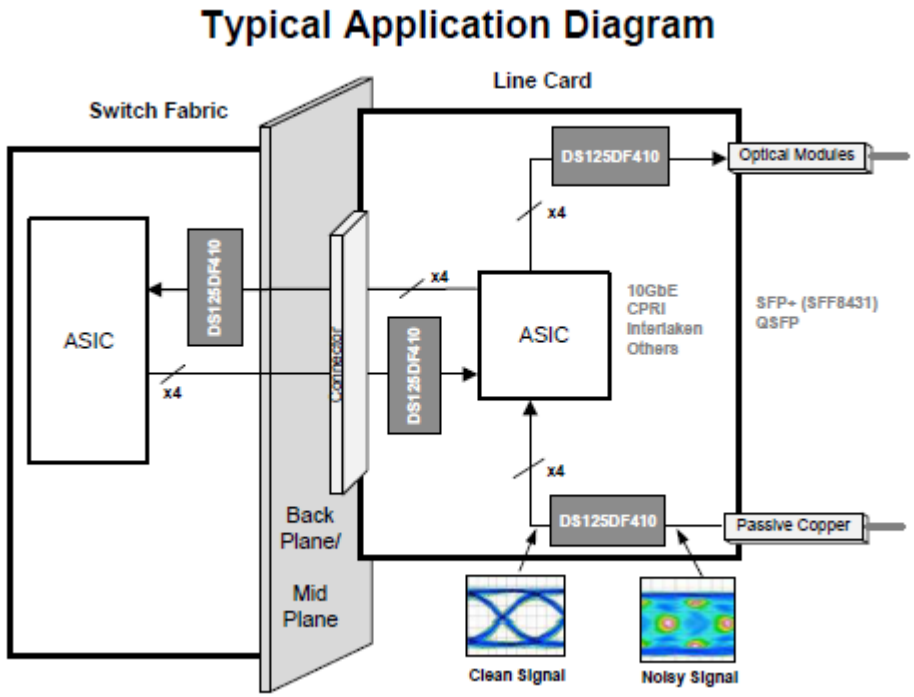
Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

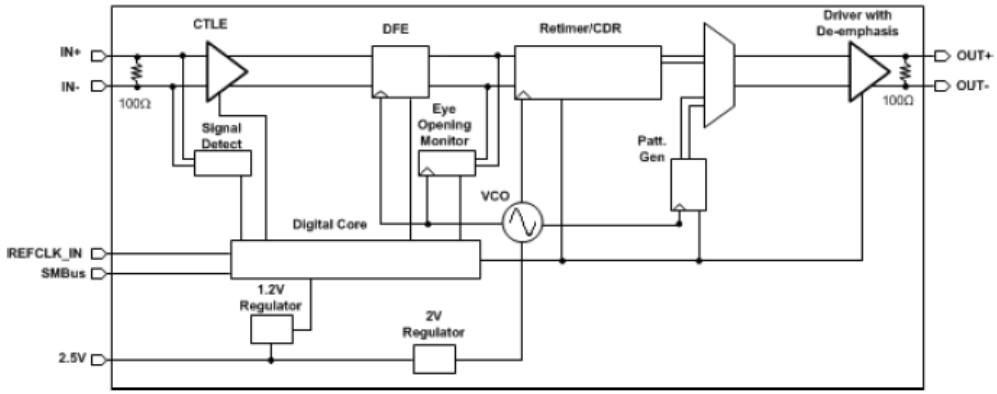
PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

TI DS110DF111, 32.

Claim 19	Disclosure
	 TI DS125DF410, 1.

Claim 19	Disclosure
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps TI DS125DF410, 1.

Claim 19	Disclosure
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps TI DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. TI DS125DF410, 1.

Claim 19	Disclosure
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** TI DS125DF410, 8.

Claim 19	Disclosure
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. TI DS125DF410, 30.

Claim 19	Disclosure

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

TI DS125DF410, 33.

Claim 19	Disclosure
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. TI DS125DF410, 33.

Claim 19	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

TI DS125DF410, 39.

Claim 19	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

TI DS125DF410, 40.

Claim 19	Disclosure

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

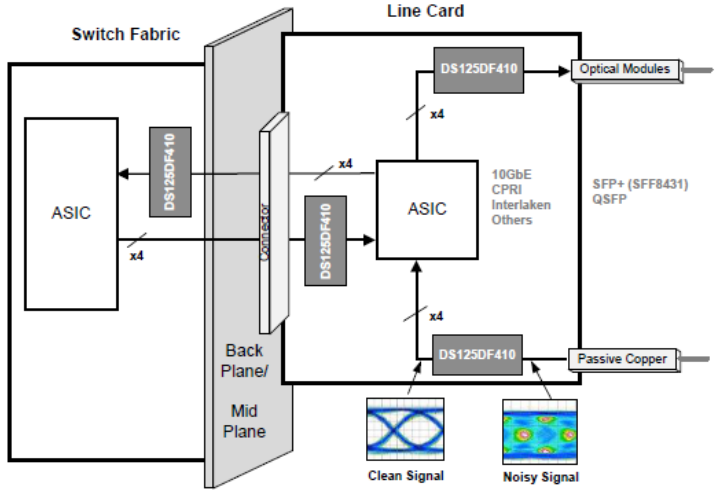
TI DS125DF410, 41.

Claim 19	Disclosure

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

TI DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 19	Disclosure
	TI DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** TI DS125DF410, 50.

Claim 19	Disclosure
	7.4.4.6 Driver Output De-Emphasis The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. TI DS125DF410, 17.

Claim 19	Disclosure
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. TI DS125DF410, 21.