

Exhibit C-3

Invalidity of U.S. Patent No. 11,032,111 (the “’111 Patent”) in View of U.S. Patent No. 10,715,357 (“Ran”)

Ran was filed on April 30, 2019, published July 14, 2020, and claims priority to Provisional Application No. 62/722,517 filed on August 24, 2018. Ran qualifies as prior art under at least 35 U.S.C. § § 102(a)(1) and 102(a)(2) (AIA).

The Provisional Application No. US 62/722,517 related to Ran (“Ran Provisional”) supports the disclosures of Ran and provides the written disclosure under 35 U.S.C. §112 for at least Ran’s Claim 1. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1380-81 (Fed. Cir. 2015). Exemplary citations to the Ran Provisional are provided in conjunction with the below disclosures to Ran. Such citations are merely exemplary of the support provided in the Ran Provisional and Respondents reserve the right to rely on any other portion of the Ran Provisional as further support.

The Administrative Law Judge has not yet construed the claims and therefore the meaning of the terms in the claims has yet to be resolved. The support identified here for limitations of the Asserted Claims of the ’111 Patent is responsive to Complainant’s apparent infringement contentions in its Complaint, which Respondents disagree with. As such, nothing in Respondents’ claim charts should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Respondents’ understanding of the proper scope of the Asserted Claims of the ’111 Patent.

All cross-references should be understood to include material that is cross-referenced within the cross-reference. Where a particular Figure is cited, the citation should be understood to encompass the caption and description of the Figure as well as any text relating to or describing the Figure. Conversely, where particular text referring to a Figure is cited, the citation should be understood to include the Figure as well. Respondents reserve the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Complainant’s infringement and/or domestic industry contentions, and/or information obtained during discovery as the case progresses.

To the extent Complainant alleges that Ran does not disclose any particular limitation of the Asserted Claims of the ’111 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the ’111 Patent to modify Ran and/or to combine the teachings of Ran with other prior art references, including but not limited to the prior art references cited in the Cover Pleading and the relevant section(s) of claim charts for other prior art references for the ’111 Patent in a manner that would have rendered the Asserted Claims invalid as obvious.

Because Complainant has yet to identify any limitation of the Asserted Claims of the ’111 Patent that it contends is not fully disclosed by Ran, either alone or in combination with other prior art cited by Respondents, Respondents expressly reserve the right to rebut any such contention, including by identifying additional obviousness combinations, if any such contention is made by

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Complainant. Respondents further reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Cover Pleading.

A. INDEPENDENT CLAIM 1

Claim 1	Ran
1[pre] A SerDes communications method that comprises, in a transceiver:	To the extent the preamble is limiting, Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host.” Ran, 1:34-41; Ran Provisional at 2. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4.

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Claim 1	Ran
	“Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “FIG. 10 depicts an example of a data center. Various embodiments can be used in or with the data center of FIG. 10 to adjust transmitter equalizer settings for any electrical or optical signal transmitter. As shown in FIG. 10, data center 1000 may include an optical fabric 1012. Optical fabric 1012 may generally include a combination of optical signaling media (such as optical cabling) and optical switching infrastructure via which any particular sled in data center 1000 can send signals to (and receive signals from) the other sleds in data center 1000. The signaling connectivity that optical fabric 1012 provides to any given sled may include connectivity both to other sleds in a same rack and sleds in other racks. Data center 1000 includes four racks 1002A to 1002D and racks 1002A to 1002D house respective pairs of sleds 1004A-1 and 1004A-2, 1004B-1 and 1004B-2, 1004C-1 and 1004C-2, and 1004D-1 and 1004D-2. Thus, in this example, data center 1000 includes a total of eight sleds. Optical fabric 1012 can provide

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	sled signaling connectivity with one or more of the seven other sleds. For example, via optical fabric 10012, sled 1004A-1 in rack 1002A may possess signaling connectivity with sled 1004A-2 in rack 1002A, as well as the six other sleds 1004B-1, 1004B-2, 1004C-1, 1004C-2, 1004D-1, and 1004D-2 that are distributed among the other racks 1002B, 1002C, and 1002D of data center 1000. The embodiments are not limited to this example. For example, fabric 1012 can provide optical and/or electrical signaling.” Ran, 16:64-17:23; Ran Provisional at 14, 16. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55; Ran Provisional at 16-18. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; ; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; ; Ran Provisional at 16-18.

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	“Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; ; Ran Provisional at 16-18.

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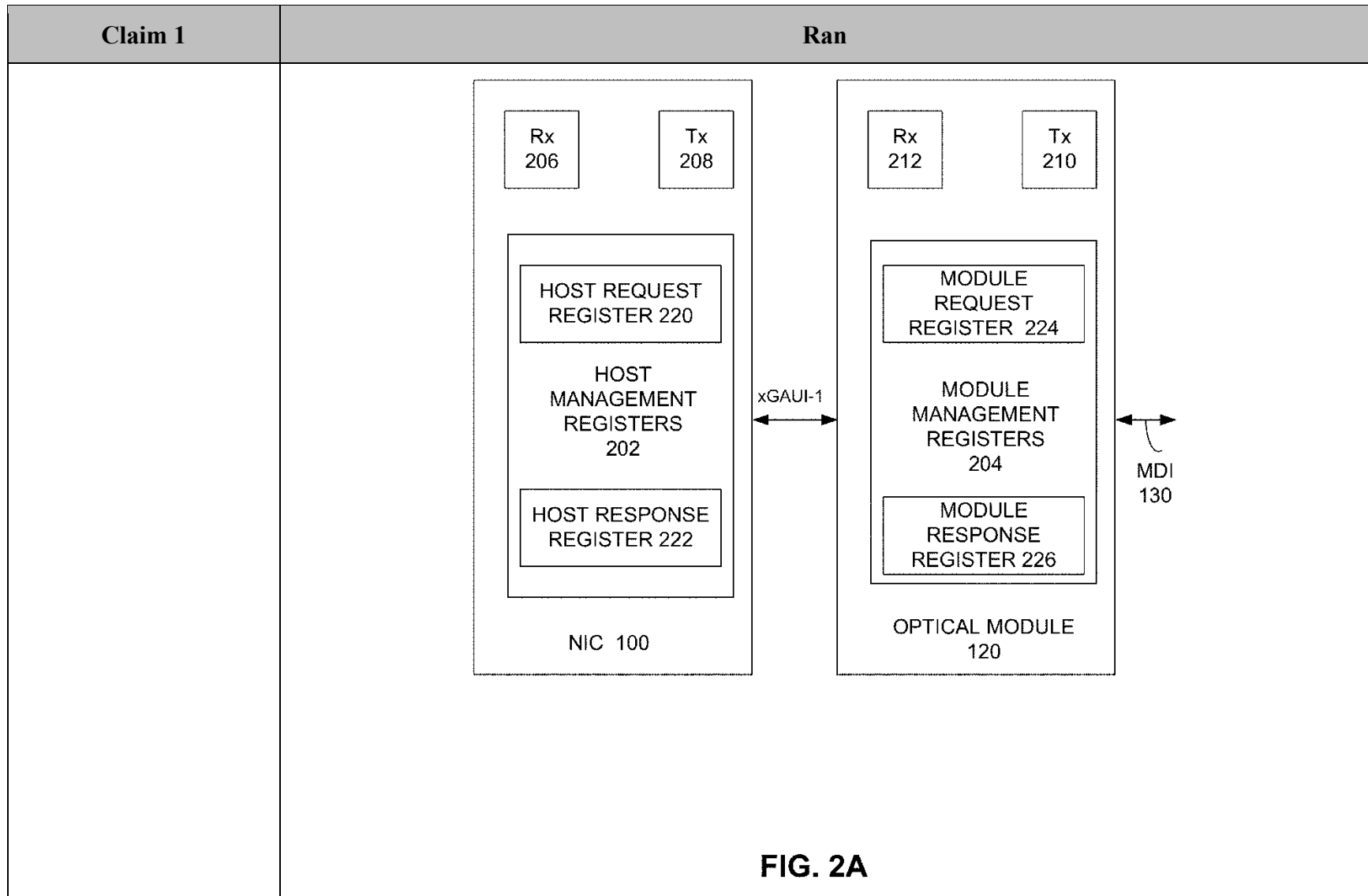


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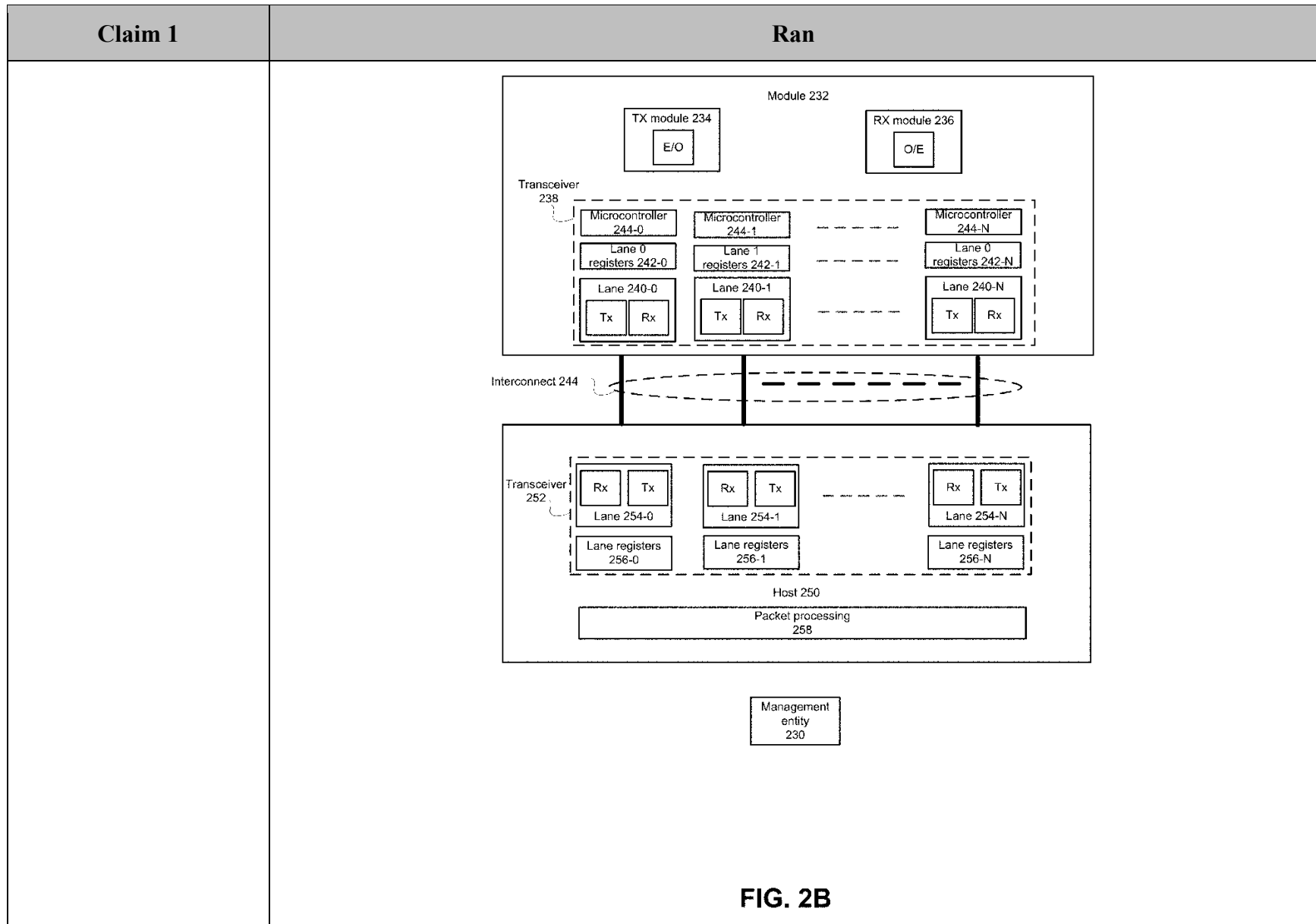


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	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

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Claim 1	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
1	1	Preset3																													
1	0	Preset2																													
0	1	Preset1																													
0	0	Co-efficient Control																													
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1	1	PAM4 with precoding																													
1	0	PAM4																													
0	1	Reserved																													
0	0	PAM2																													

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	To the extent that this preamble is not disclosed, either explicitly or inherently, by Ran, this preamble is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[a] selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host.” Ran, 1:34-41; Ran Provisional at 2. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules

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	will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4. “Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily

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	fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause 136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “FIG. 2A illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface (AUI) Chip-to-Module (C2M) to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUI) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. In addition, the system can be used for C2C intercommunications.” Ran, 5:4-14; Ran Provisional at 7. “Host management registers 202 in the network interface controller 100 include a host request register 220 and a host response register 222. Module management registers 224 in the optical

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	module 120 include a module request register 224 and a module response register 226. The host management registers 202 and module management registers 204 are used at least in connection with two-way communications to perform timing recovery and equalization for a single-lane xGAUI-1 electrical link between the network interface controller 100 and the optical module 120 or other electrical interconnect module device.” Ran, 5:15-25; Ran Provisional at 7. “The request registers, host request register 220 and module request register 224, will be described in conjunction with FIGS. 3A-3E. The response registers, host response register 222 and module response register 226, will be described in conjunction with FIGS. 4A and 4B.” Ran, 5:34-38; Ran Provisional at 7-8. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8.

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	“The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8. “The host request register 220 can be written-to by the management entity. Writing this register has the effect of conveying the request message from module request register 224 of optical module 120 to the network interface controller 100 via host request register 220, which may change the equalization setting of one or more equalizer taps as requested. A response message can be generated by writing to host response register 222.” Ran, 6:5-12; Ran Provisional at 7-8. “For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8.

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	“The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog

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	converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Module 232 can be communicatively coupled to host 250 by an interconnect 244. Interconnect 244 can be electrical signal conductors that couple pins or holes of lane 240-0 to 240-N of a pluggable module 232 to holes or pins of lanes 254-0 to 254-N of host 250. Host 250 can transmit or receive signals in electrical format to or from module 232. In some examples, module 232 provides optical communications to and from any optical medium for host 250.” Ran, 7:60-67; Ran Provisional at 7-8.

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	“Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10.

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Claim 1	Ran
	“A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of –1. With a three bit

Exhibit C-3

Claim 1	Ran
	coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive

Exhibit C-3

Claim 1	Ran
	signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

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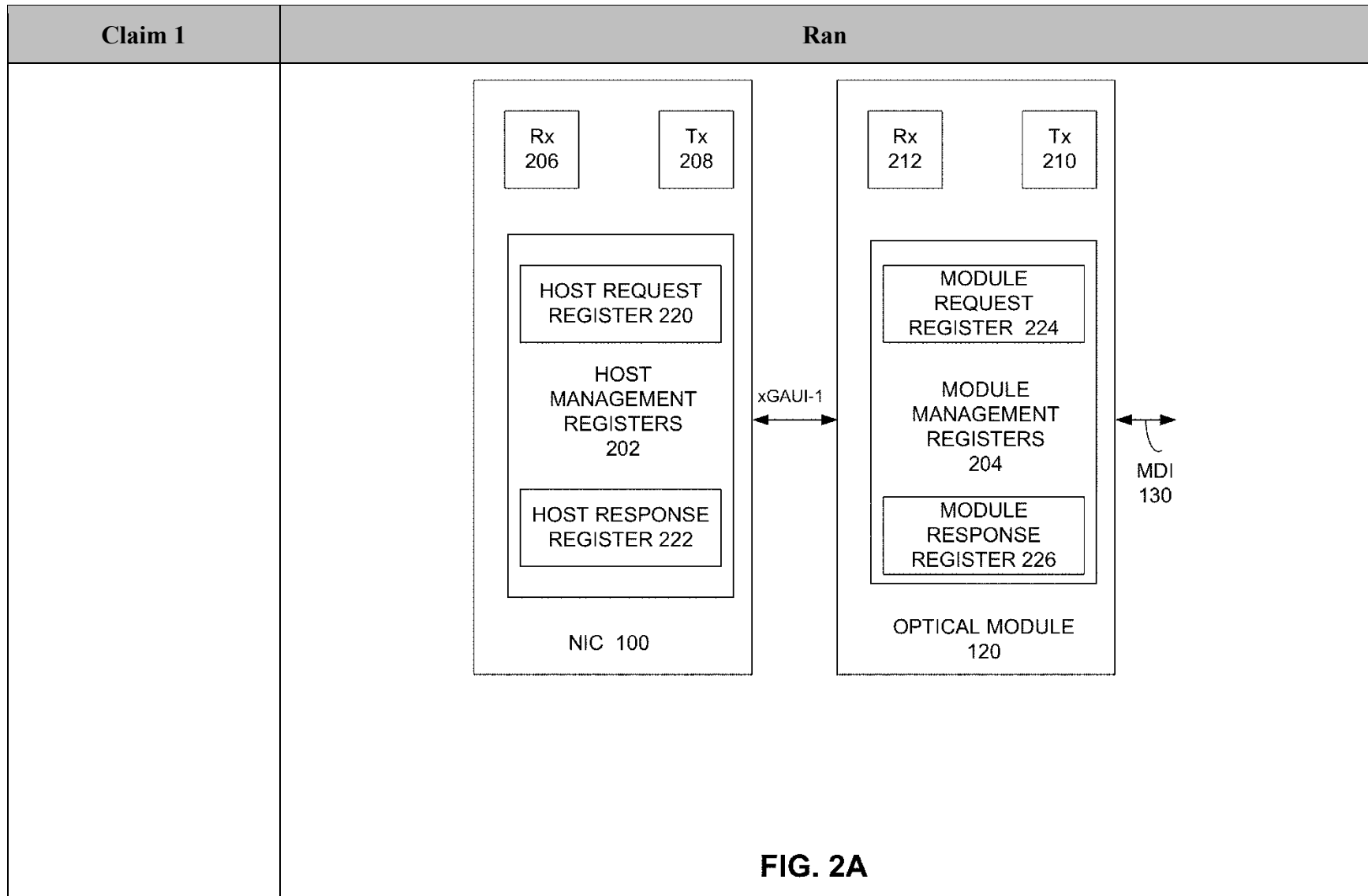


Exhibit C-3

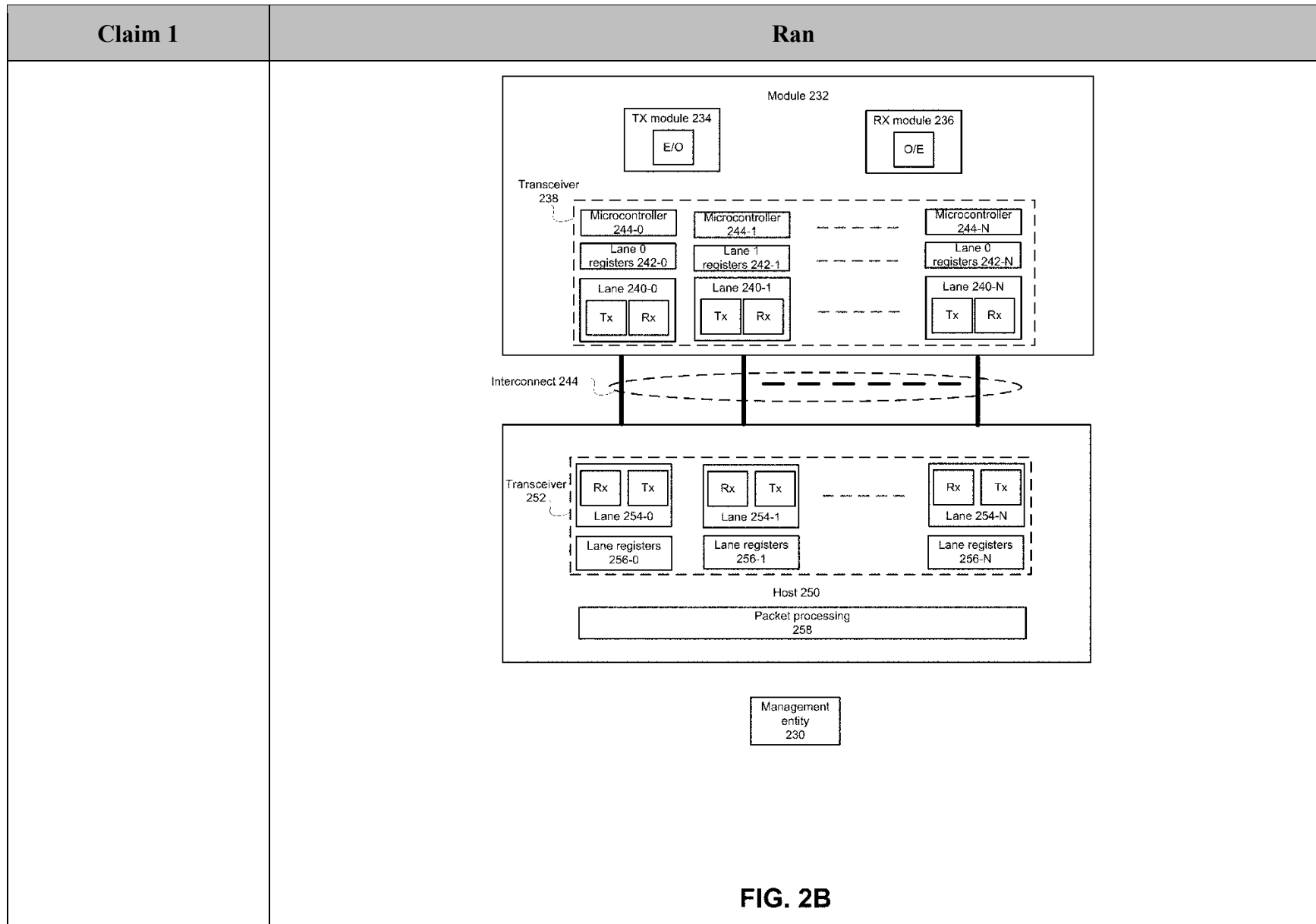


Exhibit C-3

Claim 1	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

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Claim 1	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
1	1	Preset3																													
1	0	Preset2																													
0	1	Preset1																													
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0	1	Reserved																													
0	0	PAM2																													

Exhibit C-3

Claim 1	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[b] updating the initial pre-equalizer coefficient values during a training phase; and	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4.

Exhibit C-3

Claim 1	Ran
	“Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause

Exhibit C-3

Claim 1	Ran
	136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8. “The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8.

Exhibit C-3

Claim 1	Ran
	“For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8. “The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to

Exhibit C-3

Claim 1	Ran
	enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-

Exhibit C-3

Claim 1	Ran
	0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The

Exhibit C-3

Claim 1	Ran
	parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10. “A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not

Exhibit C-3

Claim 1	Ran
	require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-

Exhibit C-3

Claim 1	Ran
	to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18.

Exhibit C-3

Claim 1	Ran
	“Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

Exhibit C-3

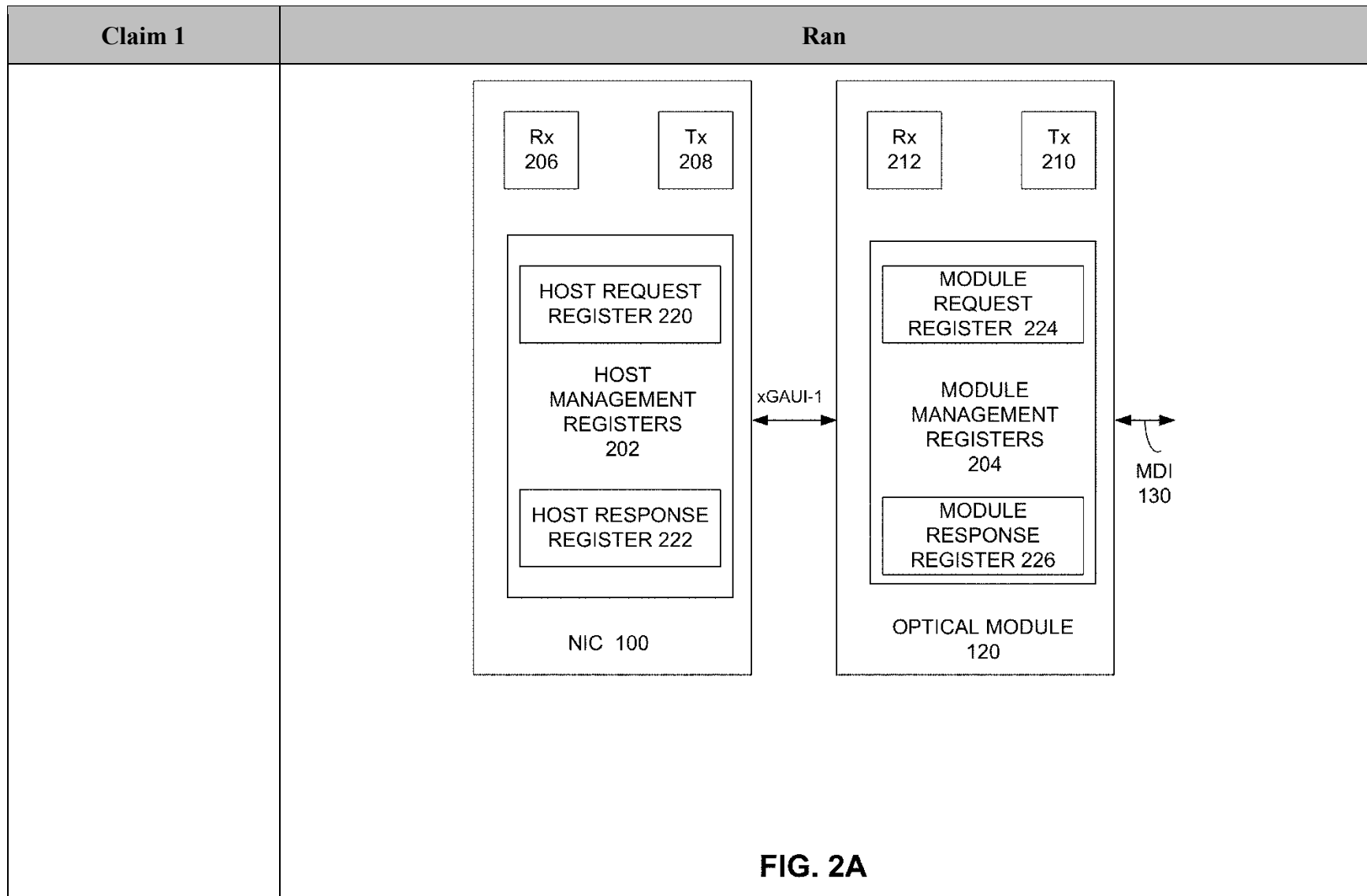


Exhibit C-3

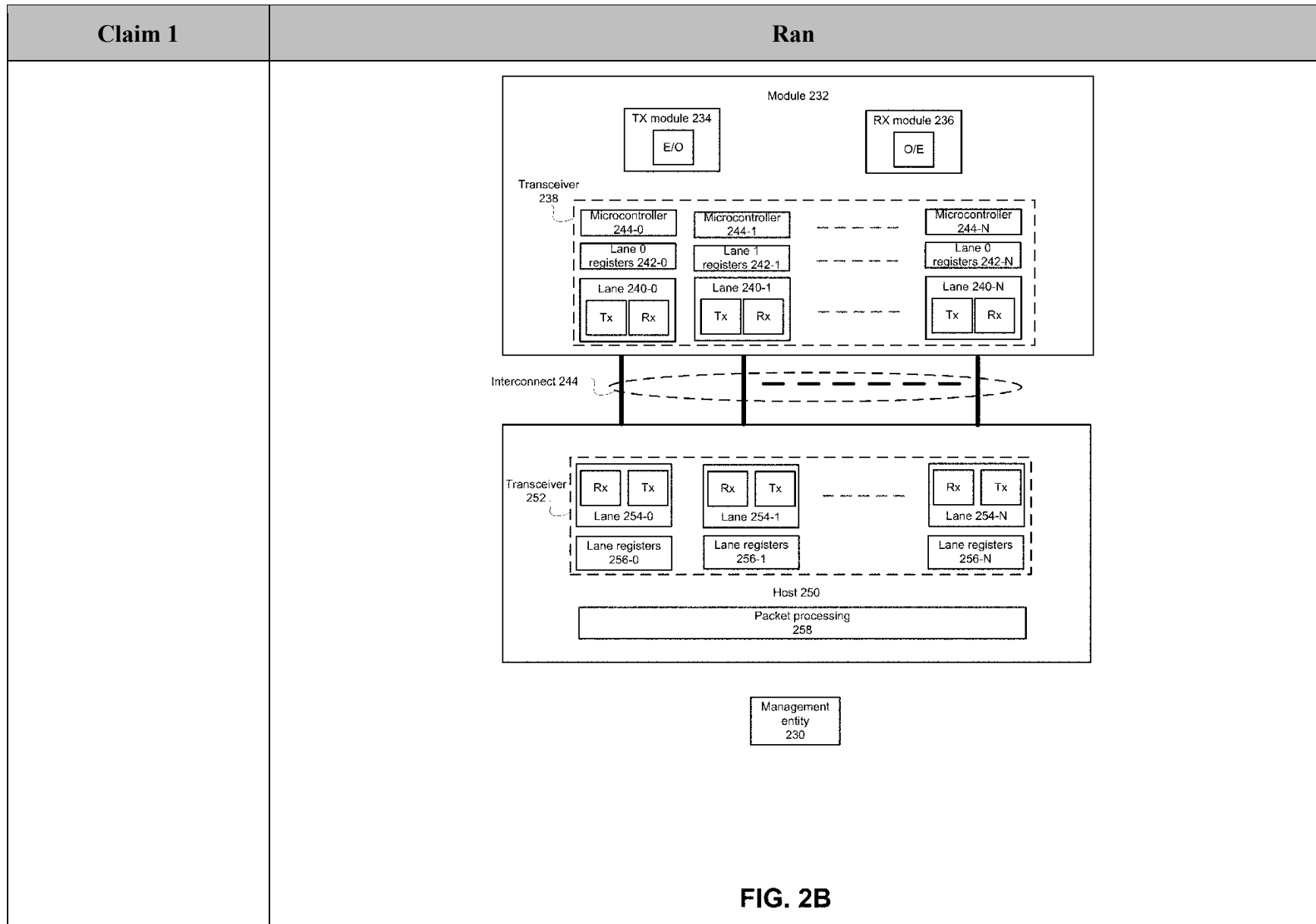


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Claim 1	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

Exhibit C-3

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Bit 13	Bit 12	Description																													
1	1	Preset3																													
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Exhibit C-3

Claim 1	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[c] using the updated pre-equalizer coefficient values to convey a transmit data stream.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4.

Exhibit C-3

Claim 1	Ran
	“Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause

Exhibit C-3

Claim 1	Ran
	136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8. “The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8.

Exhibit C-3

Claim 1	Ran
	“For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8. “The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to

Exhibit C-3

Claim 1	Ran
	enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-

Exhibit C-3

Claim 1	Ran
	0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The

Exhibit C-3

Claim 1	Ran
	parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10. “A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not

Exhibit C-3

Claim 1	Ran
	require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-

Exhibit C-3

Claim 1	Ran
	to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18.

Exhibit C-3

Claim 1	Ran
	“Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

Exhibit C-3

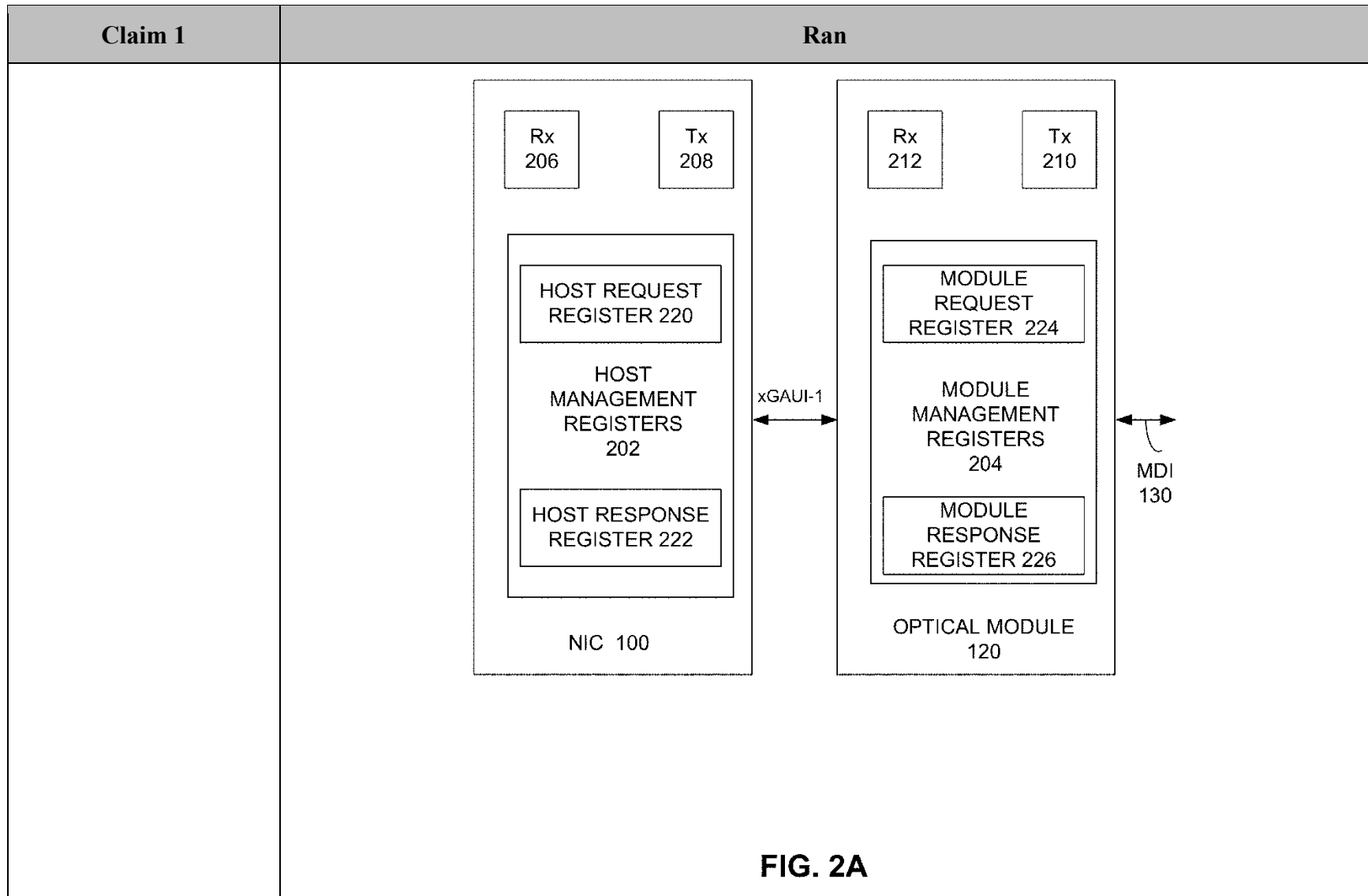


Exhibit C-3

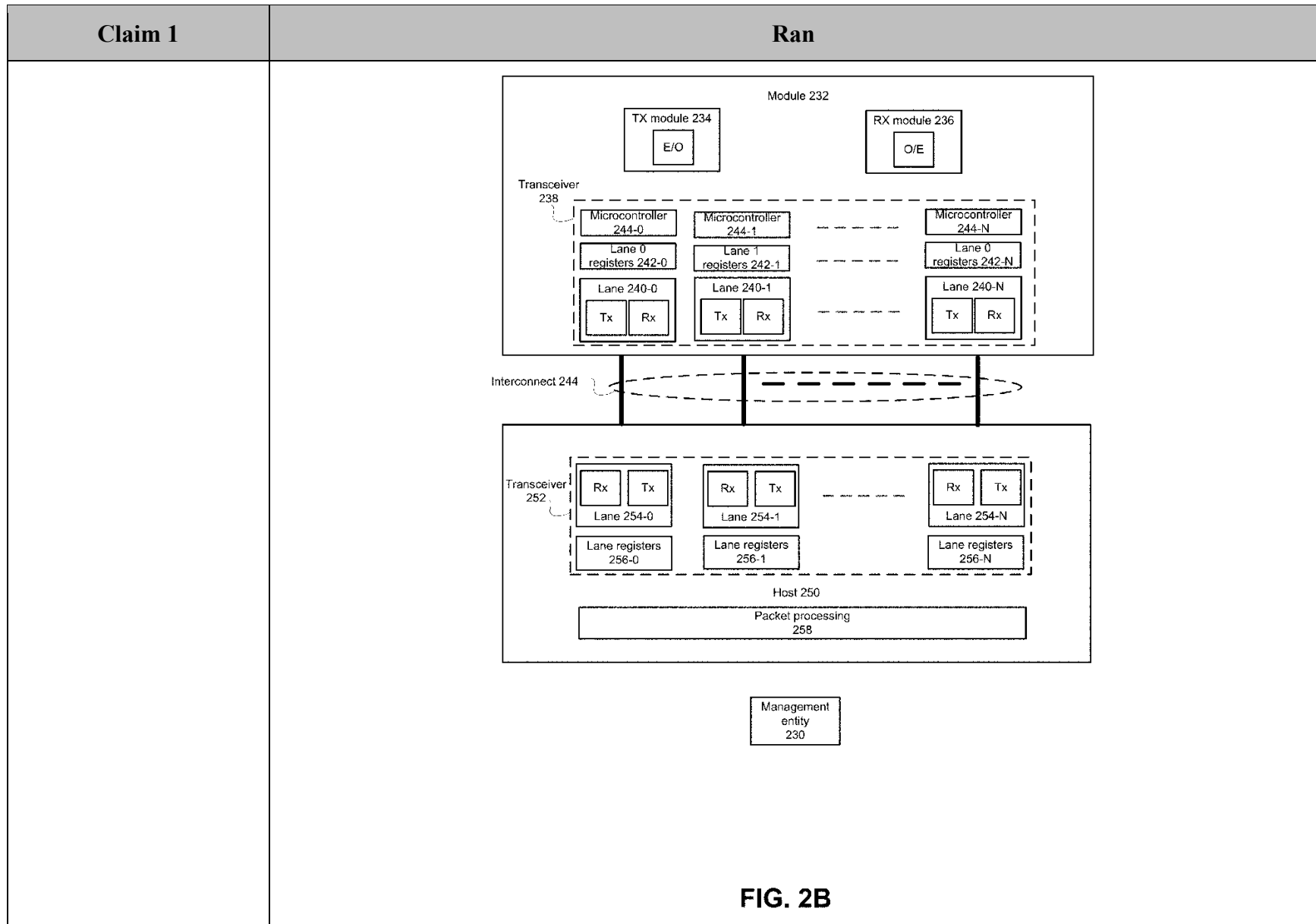


Exhibit C-3

Claim 1	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

Exhibit C-3

Claim 1	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
1	1	Preset3																													
1	0	Preset2																													
0	1	Preset1																													
0	0	Co-efficient Control																													
Bit 9	Bit 8	Description																													
1	1	PAM4 with precoding																													
1	0	PAM4																													
0	1	Reserved																													
0	0	PAM2																													

Exhibit C-3

Claim 1	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

Exhibit C-3

B. DEPENDENT CLAIM 2

Claim 2	Ran
2. The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.	Ran discloses and/or renders obvious this limitation. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management

Exhibit C-3

Claim 2	Ran
	entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10. “A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used

Exhibit C-3

Claim 2	Ran
	for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap

Exhibit C-3

Claim 2	Ran
	c(0), and a post-cursor tap c(1). The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

Exhibit C-3

Claim 2	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

Exhibit C-3

C. DEPENDENT CLAIM 3

Claim 3	Ran
3. The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 3	Ran
	“The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over

Exhibit C-3

Claim 3	Ran
	the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of

Exhibit C-3

Claim 3	Ran
	registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two-bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10.

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Claim 3	Ran
	“FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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D. DEPENDENT CLAIM 4

Claim 4	Ran
4. The method of claim 1, wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 4	Ran
	“The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over

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Claim 4	Ran
	the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of

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Claim 4	Ran
	registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two-bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10.

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Claim 4	Ran
	“FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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E. DEPENDENT CLAIM 5

Claim 5	Ran
5. The method of claim 4, wherein the performance characteristic is an error signal energy.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 5	Ran
	“The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “The management entity may use the indication of “receiver ready” bit set to ‘1’ to permit transmission of real data (as opposed to training data) from the host transmitter to the module for transmission to a remote

Exhibit C-3

Claim 5	Ran
	station (link partner). If the indication of “receiver ready” bit is not set to ‘1’, return to block 600 and the receiver can continue to tune any transmitter equalizer settings for the same lane. For example, the “receiver ready” bit can be set to ‘1’ if a sufficiently low bit error rate (BER) is detected by the receiver.” Ran, 12:41-50; Ran Provisional at 12-13. “For example, equalization coefficients selected for a communications link between blades or other devices may need to be modified after the communications link is established to handle variations in operating conditions, for example, temperature and humidity that may cause an increase in bit errors over the communications link.” Ran, 15:45-50; Ran Provisional at 12-13. “FIG. 8 depicts a network interface. Various embodiments can use the network interface or be used by the network interface. Network interface 800 can use transceiver 802, processors 804, transmit queue 806, receive queue 808, memory 810, and bus interface 812, and DMA engine 852. Transceiver 802 can be capable of receiving and transmitting packets in conformance with the applicable protocols such as Ethernet as described in IEEE 802.3, although other protocols may be used. Transceiver 802 can receive and transmit packets from and to a network via a network medium (not depicted). Transceiver 802 can include PHY circuitry 814 and media access control (MAC) circuitry 816. PHY circuitry 814 can include encoding and decoding circuitry (not shown) to encode and decode data packets according to applicable physical layer specifications or standards. MAC circuitry 816 can be configured to assemble data to be transmitted into packets, that include destination and source addresses along with network control information and error detection hash values. Processors 804 can be any a combination of a: processor, core, graphics processing unit (GPU), field programmable gate array (FPGA), application specific integrated circuit (ASIC), or other programmable hardware device that allow programming of network interface 800. For example, processors 804 can provide for identification of a resource to use to perform a workload and generation of a bitstream for execution on the selected resource. For example, a “smart network interface” can provide packet processing capabilities in the network interface using processors 804.” Ran, 15:51-16:12; Ran Provisional at 12-14. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the

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Claim 5	Ran
	communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55; Ran Provisional at 16-18. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems

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Claim 5	Ran
	and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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F. DEPENDENT CLAIM 6

Claim 6	Ran
6. The method of claim 4, wherein the performance characteristic is a bit error rate.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

Exhibit C-3

Claim 6	Ran
	“The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “The management entity may use the indication of “receiver ready” bit set to ‘1’ to permit transmission of real data (as opposed to training data) from the host transmitter to the module for transmission to a remote

Exhibit C-3

Claim 6	Ran
	station (link partner). If the indication of “receiver ready” bit is not set to ‘1’, return to block 600 and the receiver can continue to tune any transmitter equalizer settings for the same lane. For example, the “receiver ready” bit can be set to ‘1’ if a sufficiently low bit error rate (BER) is detected by the receiver.” Ran, 12:41-50; Ran Provisional at 12-13. “For example, equalization coefficients selected for a communications link between blades or other devices may need to be modified after the communications link is established to handle variations in operating conditions, for example, temperature and humidity that may cause an increase in bit errors over the communications link.” Ran, 15:45-50; Ran Provisional at 12-13. “FIG. 8 depicts a network interface. Various embodiments can use the network interface or be used by the network interface. Network interface 800 can use transceiver 802, processors 804, transmit queue 806, receive queue 808, memory 810, and bus interface 812, and DMA engine 852. Transceiver 802 can be capable of receiving and transmitting packets in conformance with the applicable protocols such as Ethernet as described in IEEE 802.3, although other protocols may be used. Transceiver 802 can receive and transmit packets from and to a network via a network medium (not depicted). Transceiver 802 can include PHY circuitry 814 and media access control (MAC) circuitry 816. PHY circuitry 814 can include encoding and decoding circuitry (not shown) to encode and decode data packets according to applicable physical layer specifications or standards. MAC circuitry 816 can be configured to assemble data to be transmitted into packets, that include destination and source addresses along with network control information and error detection hash values. Processors 804 can be any a combination of a: processor, core, graphics processing unit (GPU), field programmable gate array (FPGA), application specific integrated circuit (ASIC), or other programmable hardware device that allow programming of network interface 800. For example, processors 804 can provide for identification of a resource to use to perform a workload and generation of a bitstream for execution on the selected resource. For example, a “smart network interface” can provide packet processing capabilities in the network interface using processors 804.” Ran, 15:51-16:12; Ran Provisional at 12-14. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the

Exhibit C-3

Claim 6	Ran
	communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55; Ran Provisional at 16-18. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems

Exhibit C-3

Claim 6	Ran
	and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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G. DEPENDENT CLAIM 7

Claim 7	Ran
7. The method of claim 4, further comprising updating the selected register with the updated pre-equalizer coefficient values.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 7	Ran
	“The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over

Exhibit C-3

Claim 7	Ran
	the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of

Exhibit C-3

Claim 7	Ran
	registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two-bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10.

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Claim 7	Ran
	“FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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H. INDEPENDENT CLAIM 8

Claim 8	Ran
8[pre] A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:	To the extent the preamble is limiting, Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host.” Ran, 1:34-41; Ran Provisional at 2. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is

Exhibit C-3

Claim 8	Ran
	established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “FIG. 2A illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface (AUI) Chip-to-Module (C2M) to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUI) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. In addition, the system can be used for C2C intercommunications.” Ran, 5:4-14; Ran Provisional at 7. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used

Exhibit C-3

Claim 8	Ran
	to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8.

Exhibit C-3

Claim 8	Ran
	“FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “FIG. 10 depicts an example of a data center. Various embodiments can be used in or with the data center of FIG. 10 to adjust transmitter equalizer settings for any electrical or optical signal transmitter. As shown in FIG. 10, data center 1000 may include an optical fabric 1012. Optical fabric 1012 may generally include a combination of optical signaling media (such as optical cabling) and optical switching infrastructure via which any particular sled in data center 1000 can send signals to (and receive signals from) the other sleds in data center 1000. The signaling connectivity that optical fabric 1012 provides to any given sled may include connectivity both to other sleds in a same rack and sleds in other racks. Data center 1000 includes four racks 1002A to 1002D and racks 1002A to 1002D house respective pairs of sleds 1004A-1 and 1004A-2, 1004B-1 and 1004B-2, 1004C-1 and 1004C-2, and 1004D-1 and 1004D-2. Thus, in this example, data center 1000 includes a total of eight sleds. Optical fabric 1012 can provide sled signaling connectivity with one or more of the seven other sleds. For example, via optical fabric 1012, sled 1004A-1 in rack 1002A may possess signaling connectivity with sled 1004A-2 in rack 1002A, as well as the six other sleds 1004B-1, 1004B-2, 1004C-1, 1004C-2, 1004D-1, and 1004D-2 that are distributed among the other racks 1002B, 1002C, and 1002D of data center 1000. The embodiments are not limited to this example. For example, fabric 1012 can provide optical and/or electrical signaling.” Ran, 16:64-17:23; Ran Provisional at 14, 16. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive

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Claim 8	Ran
	signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55; Ran Provisional at 16-18. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; ; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; ; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; ; Ran Provisional at 16-18.

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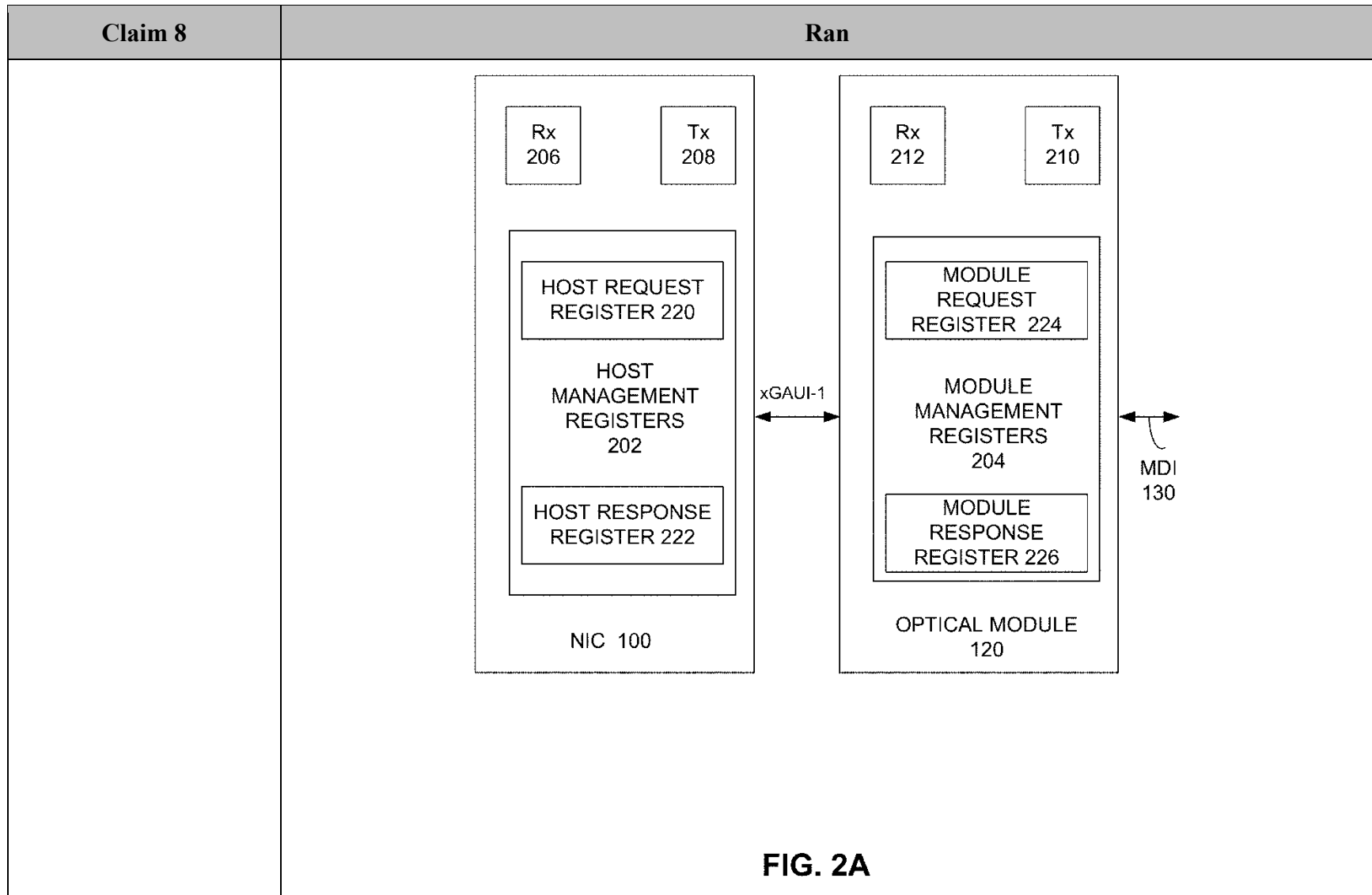


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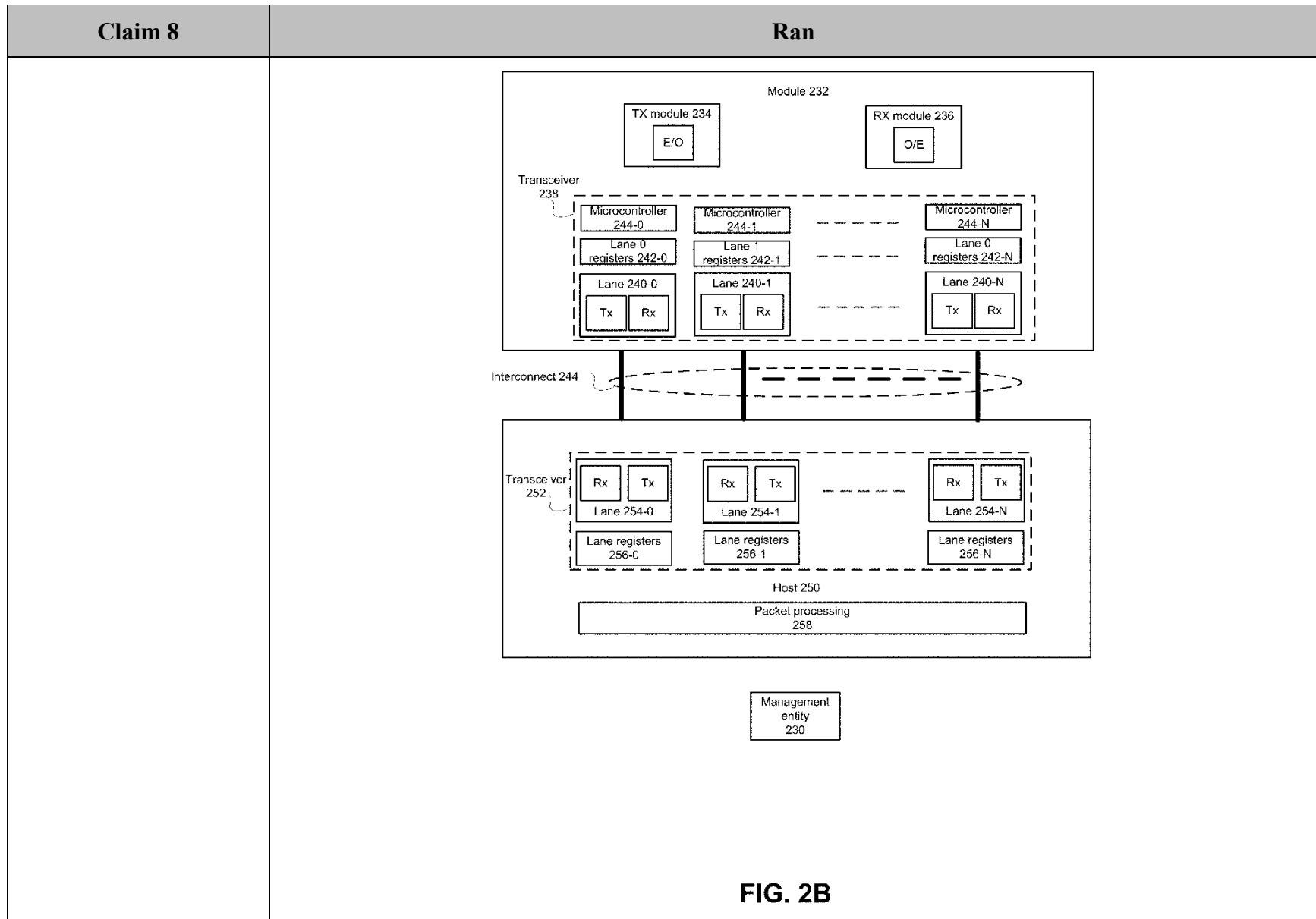


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Claim 8	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

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Claim 8	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
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Exhibit C-3

Claim 8	Ran
	To the extent that this preamble is not disclosed, either explicitly or inherently, by Ran, this preamble is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4.

Exhibit C-3

Claim 8	Ran
	“Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause

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Claim 8	Ran
	136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8. “The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8.

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Claim 8	Ran
	“For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8. “The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to

Exhibit C-3

Claim 8	Ran
	enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-

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Claim 8	Ran
	0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The

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Claim 8	Ran
	parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10. “A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not

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Claim 8	Ran
	require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-

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Claim 8	Ran
	to-module interface. The FFE 550 includes a pre-cursor tap c(−2), a pre-cursor tap c(−1), a cursor tap c(0), and a post-cursor tap c(1). The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

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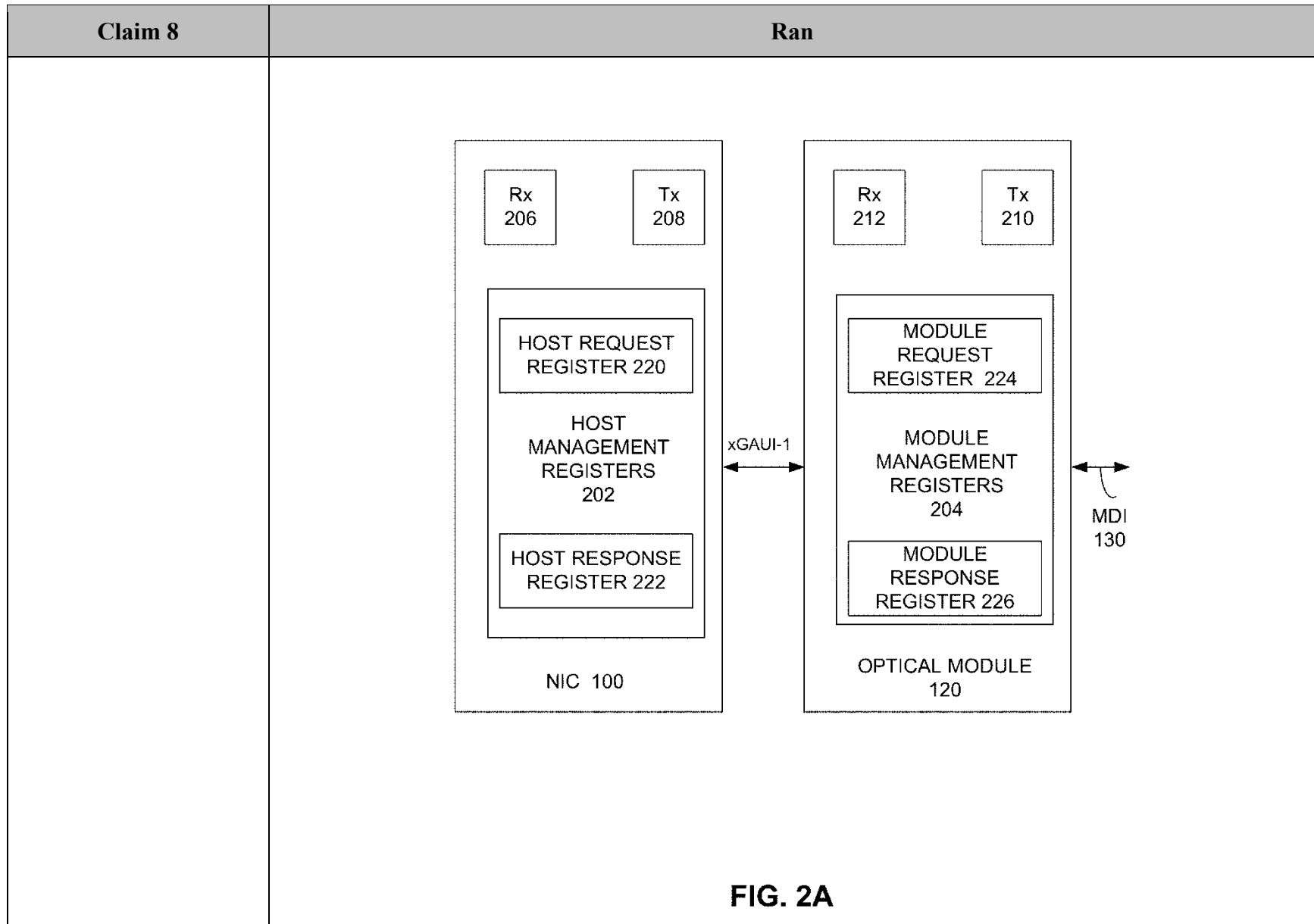


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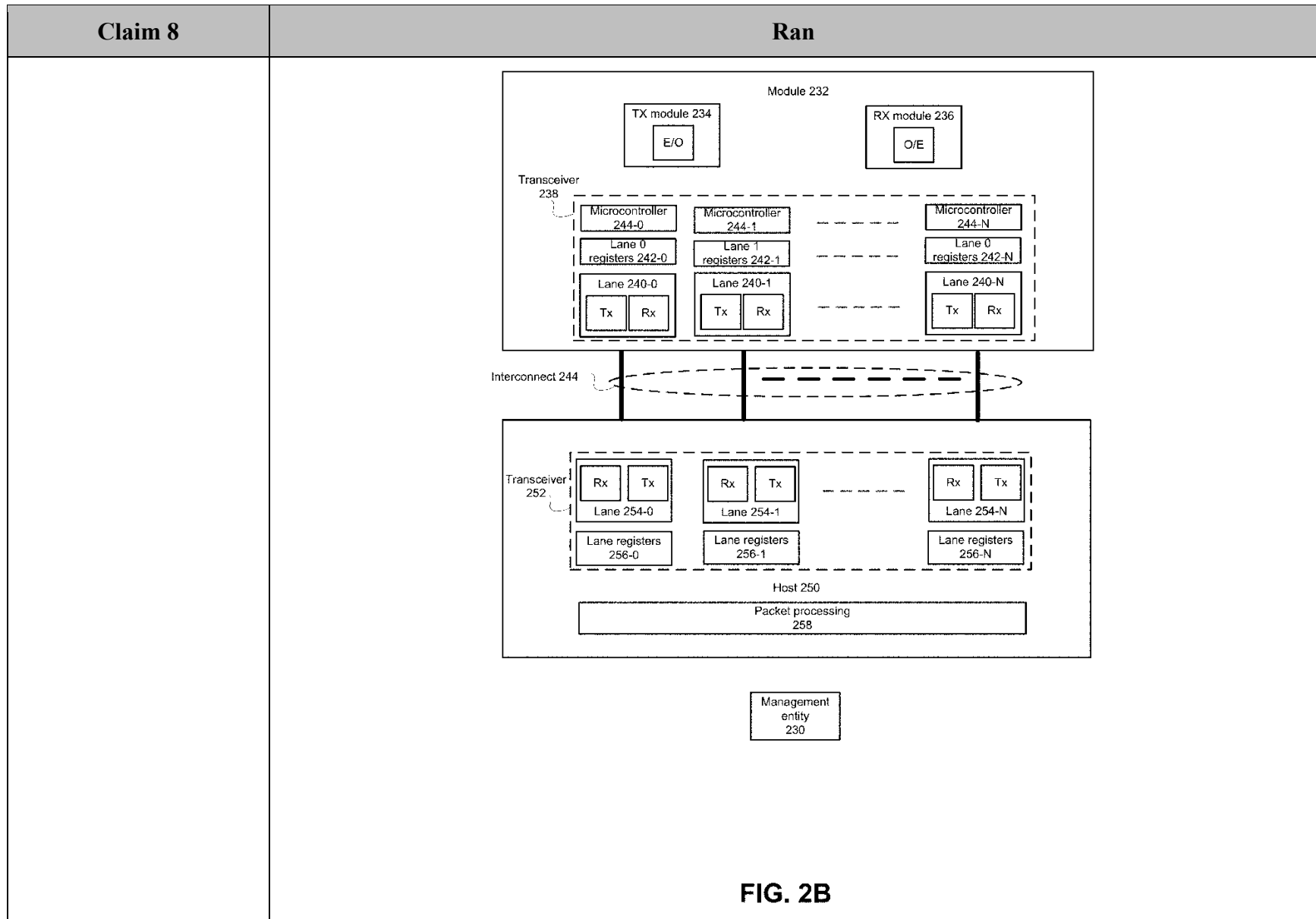


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Claim 8	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

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Claim 8	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
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Exhibit C-3

Claim 8	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model,	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host.” Ran, 1:34-41; Ran Provisional at 2. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules

Exhibit C-3

Claim 8	Ran
	will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4. “Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily

Exhibit C-3

Claim 8	Ran
	fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause 136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “FIG. 2A illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface (AUI) Chip-to-Module (C2M) to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUI) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. In addition, the system can be used for C2C intercommunications.” Ran, 5:4-14; Ran Provisional at 7. “Host management registers 202 in the network interface controller 100 include a host request register 220 and a host response register 222. Module management registers 224 in the optical

Exhibit C-3

Claim 8	Ran
	module 120 include a module request register 224 and a module response register 226. The host management registers 202 and module management registers 204 are used at least in connection with two-way communications to perform timing recovery and equalization for a single-lane xGAUI-1 electrical link between the network interface controller 100 and the optical module 120 or other electrical interconnect module device.” Ran, 5:15-25; Ran Provisional at 7. “The request registers, host request register 220 and module request register 224, will be described in conjunction with FIGS. 3A-3E. The response registers, host response register 222 and module response register 226, will be described in conjunction with FIGS. 4A and 4B.” Ran, 5:34-38; Ran Provisional at 7-8. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8.

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Claim 8	Ran
	“The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8. “The host request register 220 can be written-to by the management entity. Writing this register has the effect of conveying the request message from module request register 224 of optical module 120 to the network interface controller 100 via host request register 220, which may change the equalization setting of one or more equalizer taps as requested. A response message can be generated by writing to host response register 222.” Ran, 6:5-12; Ran Provisional at 7-8. “For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8.

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Claim 8	Ran
	“The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog

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Claim 8	Ran
	converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Module 232 can be communicatively coupled to host 250 by an interconnect 244. Interconnect 244 can be electrical signal conductors that couple pins or holes of lane 240-0 to 240-N of a pluggable module 232 to holes or pins of lanes 254-0 to 254-N of host 250. Host 250 can transmit or receive signals in electrical format to or from module 232. In some examples, module 232 provides optical communications to and from any optical medium for host 250.” Ran, 7:60-67; Ran Provisional at 7-8.

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Claim 8	Ran
	“Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10.

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Claim 8	Ran
	“A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of –1. With a three bit

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Claim 8	Ran
	coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive

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Claim 8	Ran
	signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

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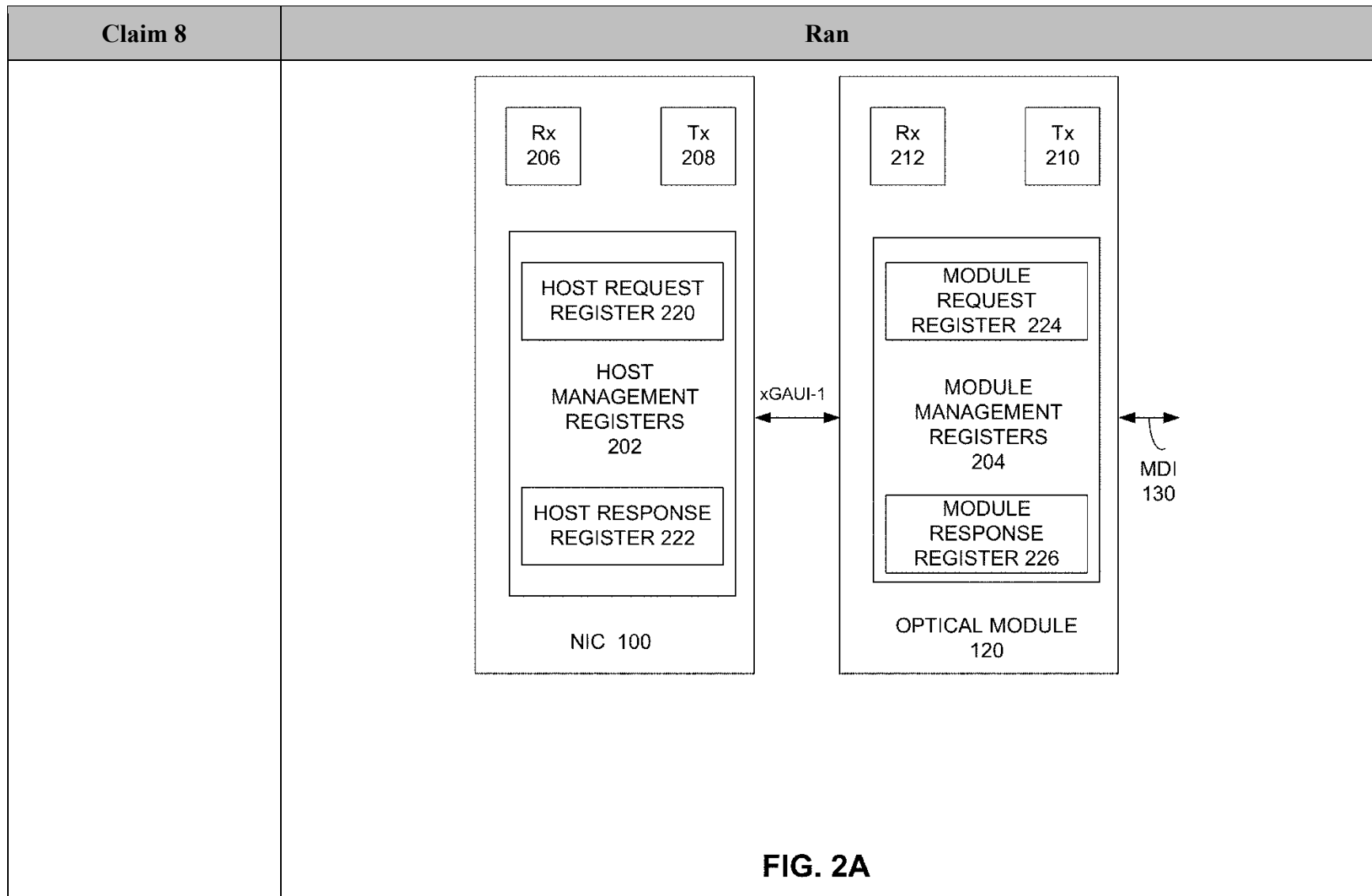


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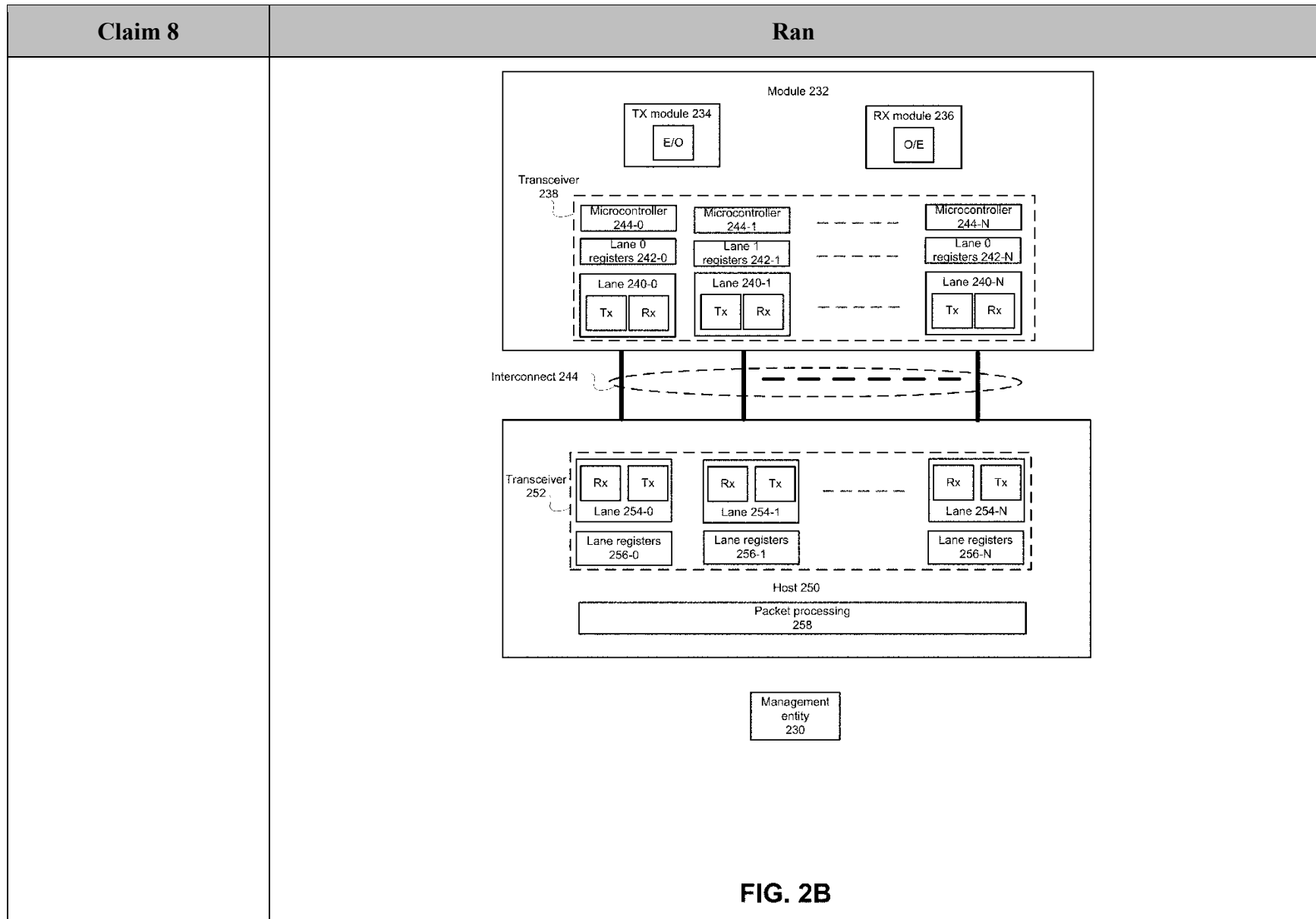


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Claim 8	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

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Claim 8	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
1	1	Preset3																													
1	0	Preset2																													
0	1	Preset1																													
0	0	Co-efficient Control																													
Bit 9	Bit 8	Description																													
1	1	PAM4 with precoding																													
1	0	PAM4																													
0	1	Reserved																													
0	0	PAM2																													

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Claim 8	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[c] the controller using one of the registers to set initial coefficient values for the one or more transmit filters.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4.

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Claim 8	Ran
	“Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause

Exhibit C-3

Claim 8	Ran
	136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8. “The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8.

Exhibit C-3

Claim 8	Ran
	“For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8. “The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to

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Claim 8	Ran
	enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-

Exhibit C-3

Claim 8	Ran
	0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The

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Claim 8	Ran
	parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10. “A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not

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Claim 8	Ran
	require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-

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Claim 8	Ran
	to-module interface. The FFE 550 includes a pre-cursor tap c(−2), a pre-cursor tap c(−1), a cursor tap c(0), and a post-cursor tap c(1). The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

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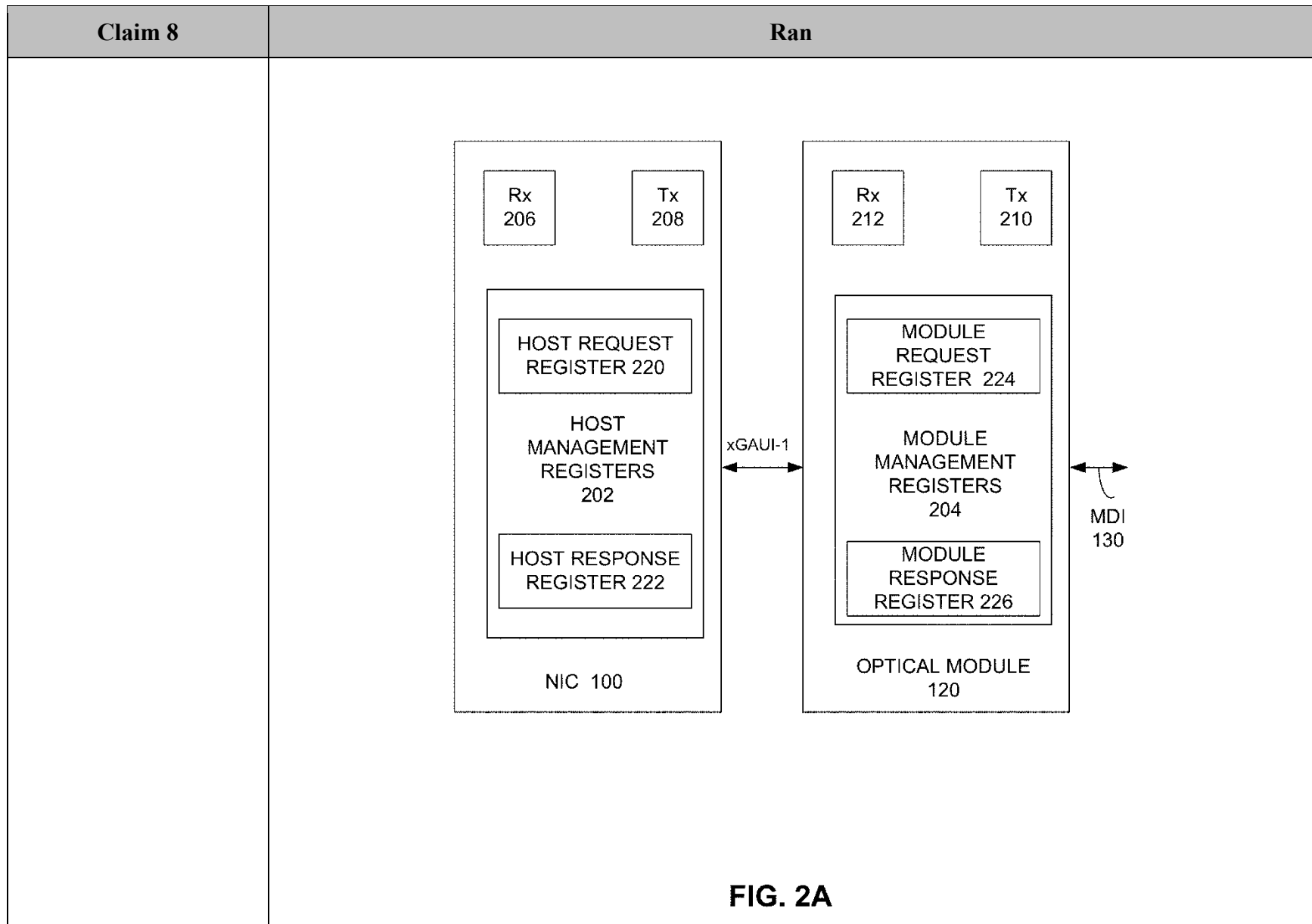


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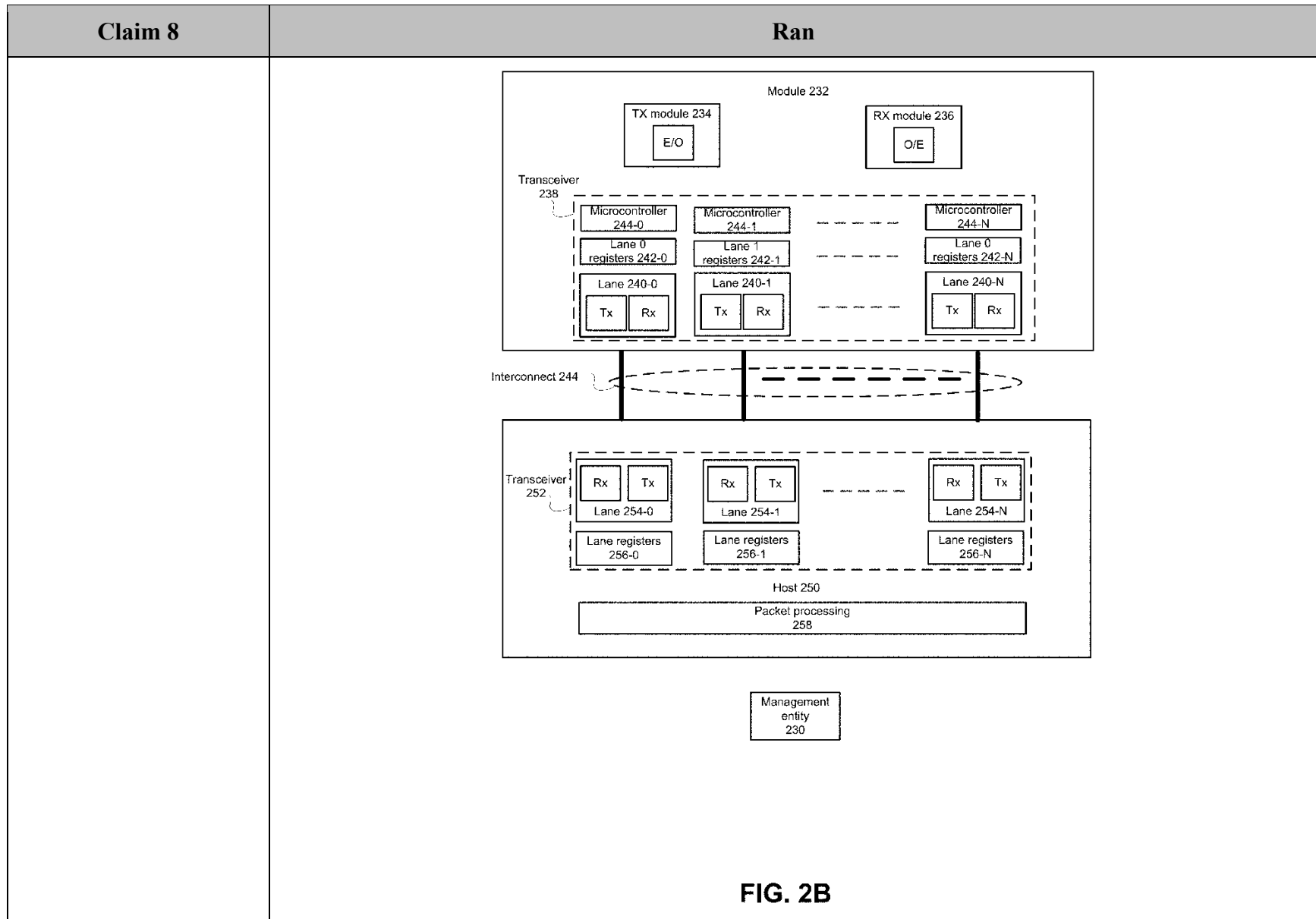


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Claim 8	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

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Claim 8	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
1	1	Preset3																													
1	0	Preset2																													
0	1	Preset1																													
0	0	Co-efficient Control																													
Bit 9	Bit 8	Description																													
1	1	PAM4 with precoding																													
1	0	PAM4																													
0	1	Reserved																													
0	0	PAM2																													

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Claim 8	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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I. DEPENDENT CLAIM 9

Claim 9	Ran
9. The communications link of claim 8, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.	Ran discloses and/or renders obvious this limitation. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management

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Claim 9	Ran
	entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10. “A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used

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Claim 9	Ran
	for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap

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Claim 9	Ran
	c(0), and a post-cursor tap c(1). The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

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Claim 9	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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J. DEPENDENT CLAIM 10

Claim 10	Ran
10. The communications link of claim 8, wherein at least some of the different channel models presume different types of receiver equalization.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 10	Ran
	“The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over

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Claim 10	Ran
	the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of

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Claim 10	Ran
	registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two-bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10.

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Claim 10	Ran
	“FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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K. INDEPENDENT CLAIM 11

Claim 11	Ran
11[pre] A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:	To the extent the preamble is limiting, Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host.” Ran, 1:34-41; Ran Provisional at 2. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is

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Claim 11	Ran
	established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “FIG. 2A illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface (AUI) Chip-to-Module (C2M) to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUI) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. In addition, the system can be used for C2C intercommunications.” Ran, 5:4-14; Ran Provisional at 7. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used

Exhibit C-3

Claim 11	Ran
	to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8.

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Claim 11	Ran
	“FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “FIG. 10 depicts an example of a data center. Various embodiments can be used in or with the data center of FIG. 10 to adjust transmitter equalizer settings for any electrical or optical signal transmitter. As shown in FIG. 10, data center 1000 may include an optical fabric 1012. Optical fabric 1012 may generally include a combination of optical signaling media (such as optical cabling) and optical switching infrastructure via which any particular sled in data center 1000 can send signals to (and receive signals from) the other sleds in data center 1000. The signaling connectivity that optical fabric 1012 provides to any given sled may include connectivity both to other sleds in a same rack and sleds in other racks. Data center 1000 includes four racks 1002A to 1002D and racks 1002A to 1002D house respective pairs of sleds 1004A-1 and 1004A-2, 1004B-1 and 1004B-2, 1004C-1 and 1004C-2, and 1004D-1 and 1004D-2. Thus, in this example, data center 1000 includes a total of eight sleds. Optical fabric 1012 can provide sled signaling connectivity with one or more of the seven other sleds. For example, via optical fabric 1012, sled 1004A-1 in rack 1002A may possess signaling connectivity with sled 1004A-2 in rack 1002A, as well as the six other sleds 1004B-1, 1004B-2, 1004C-1, 1004C-2, 1004D-1, and 1004D-2 that are distributed among the other racks 1002B, 1002C, and 1002D of data center 1000. The embodiments are not limited to this example. For example, fabric 1012 can provide optical and/or electrical signaling.” Ran, 16:64-17:23; Ran Provisional at 14, 16. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive

Exhibit C-3

Claim 11	Ran
	signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55; Ran Provisional at 16-18. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; ; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; ; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; ; Ran Provisional at 16-18.

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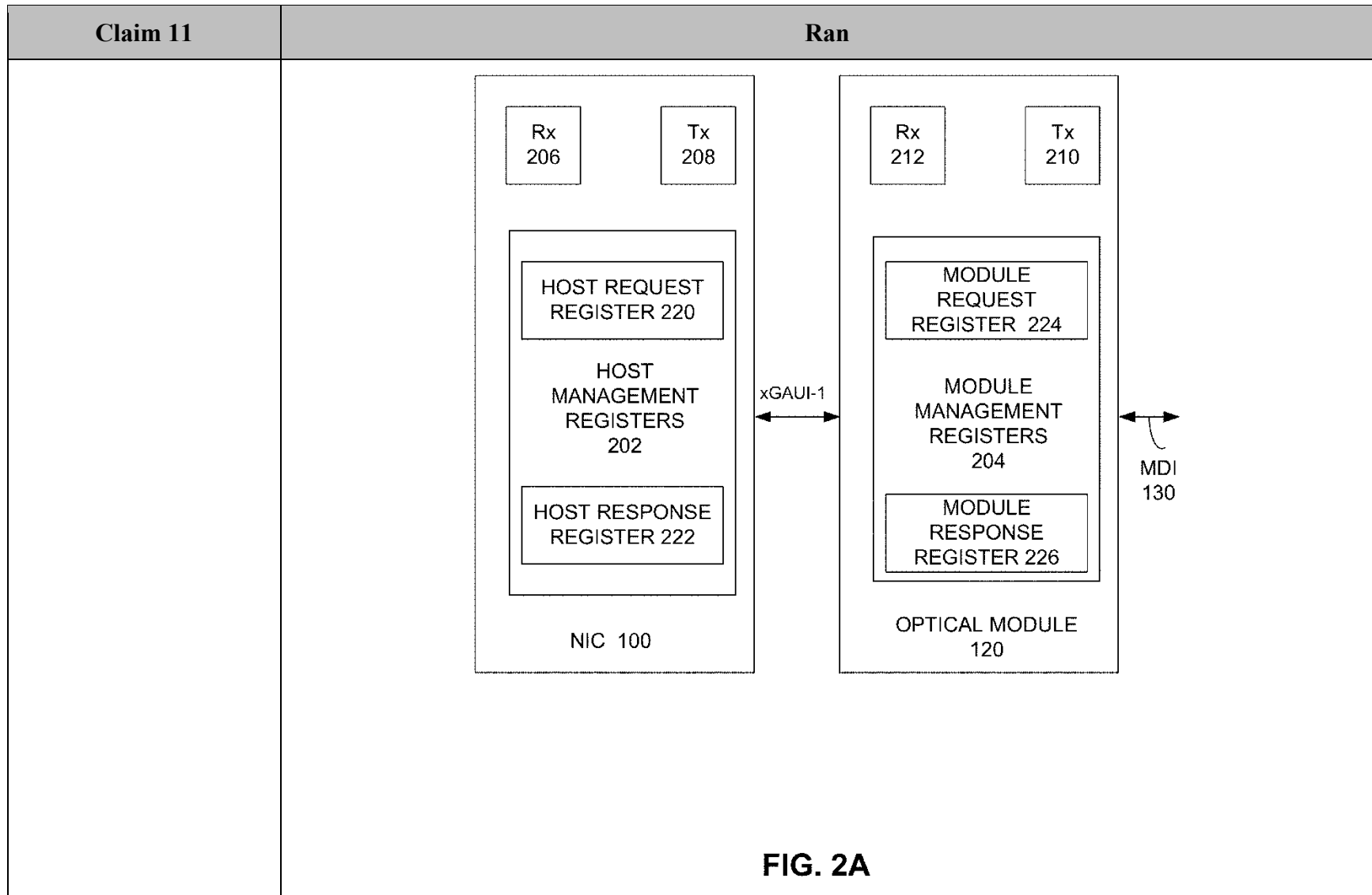


Exhibit C-3

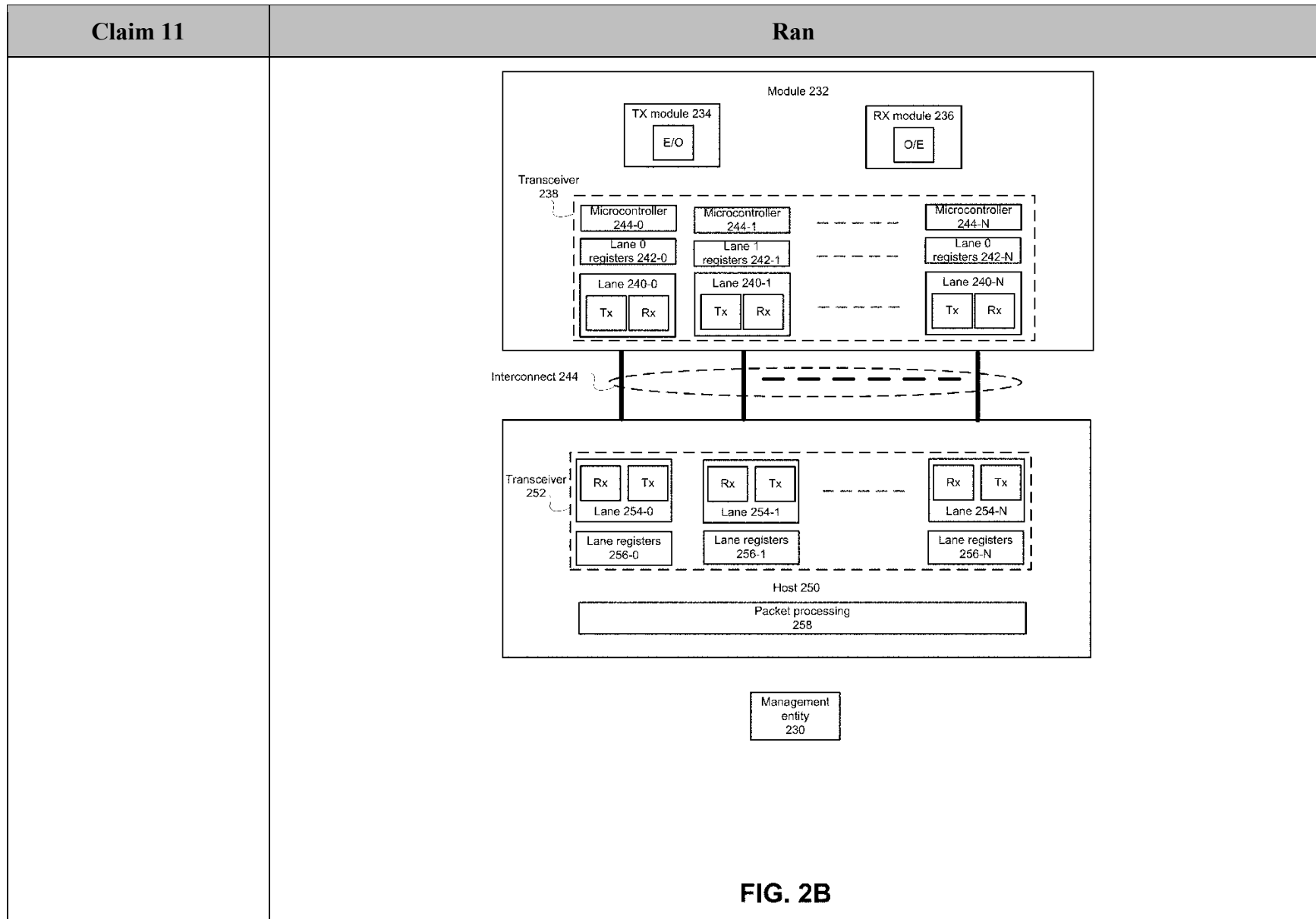


Exhibit C-3

Claim 11	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

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Claim 11	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
1	1	Preset3																													
1	0	Preset2																													
0	1	Preset1																													
0	0	Co-efficient Control																													
Bit 9	Bit 8	Description																													
1	1	PAM4 with precoding																													
1	0	PAM4																													
0	1	Reserved																													
0	0	PAM2																													

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Claim 11	Ran
	To the extent that this preamble is not disclosed, either explicitly or inherently, by Ran, this preamble is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
11[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4.

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Claim 11	Ran
	“Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause

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Claim 11	Ran
	136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8. “The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8.

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Claim 11	Ran
	“For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8. “The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to

Exhibit C-3

Claim 11	Ran
	enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-

Exhibit C-3

Claim 11	Ran
	0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The

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Claim 11	Ran
	parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10. “A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not

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Claim 11	Ran
	require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-

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Claim 11	Ran
	to-module interface. The FFE 550 includes a pre-cursor tap c(−2), a pre-cursor tap c(−1), a cursor tap c(0), and a post-cursor tap c(1). The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

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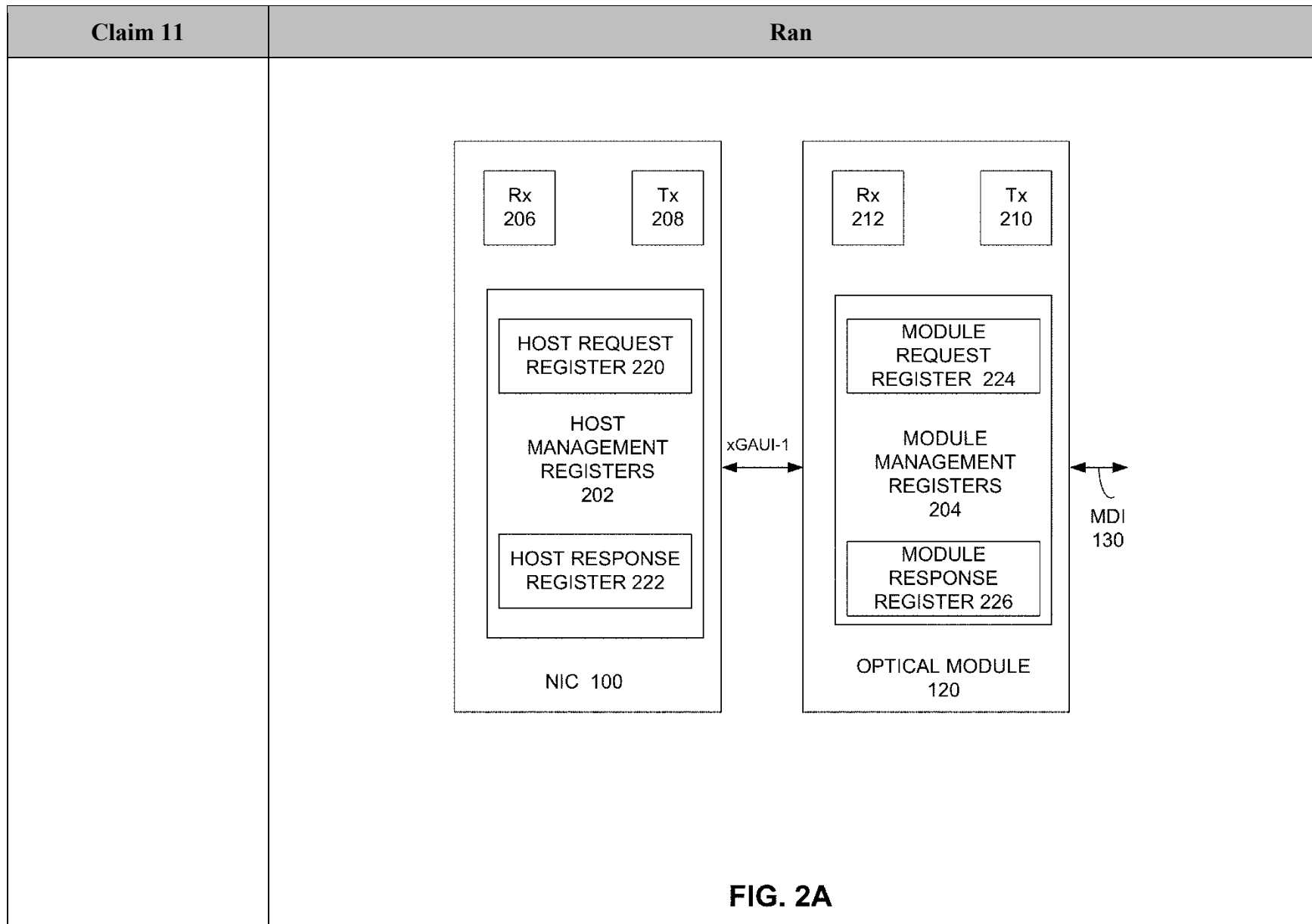


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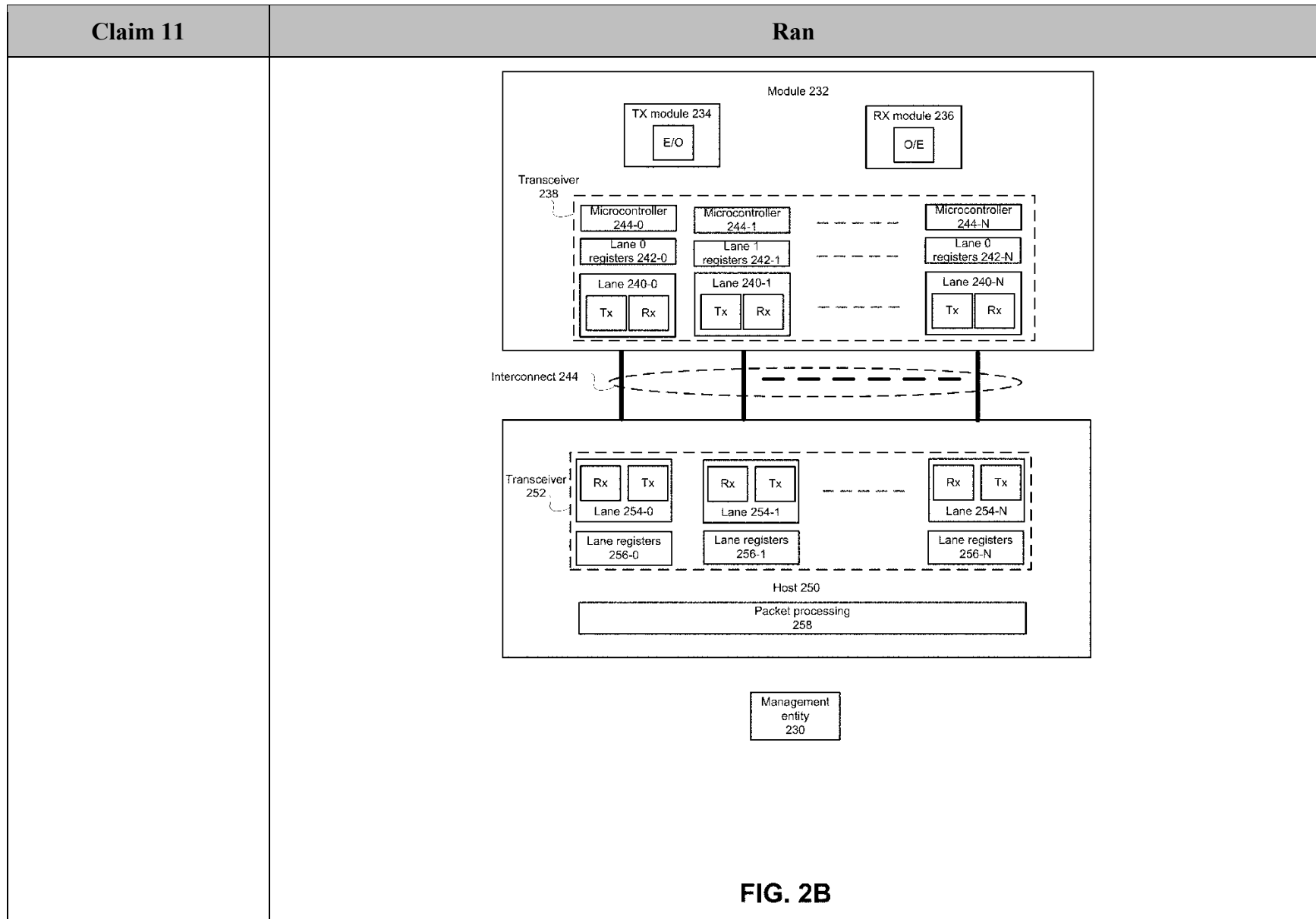


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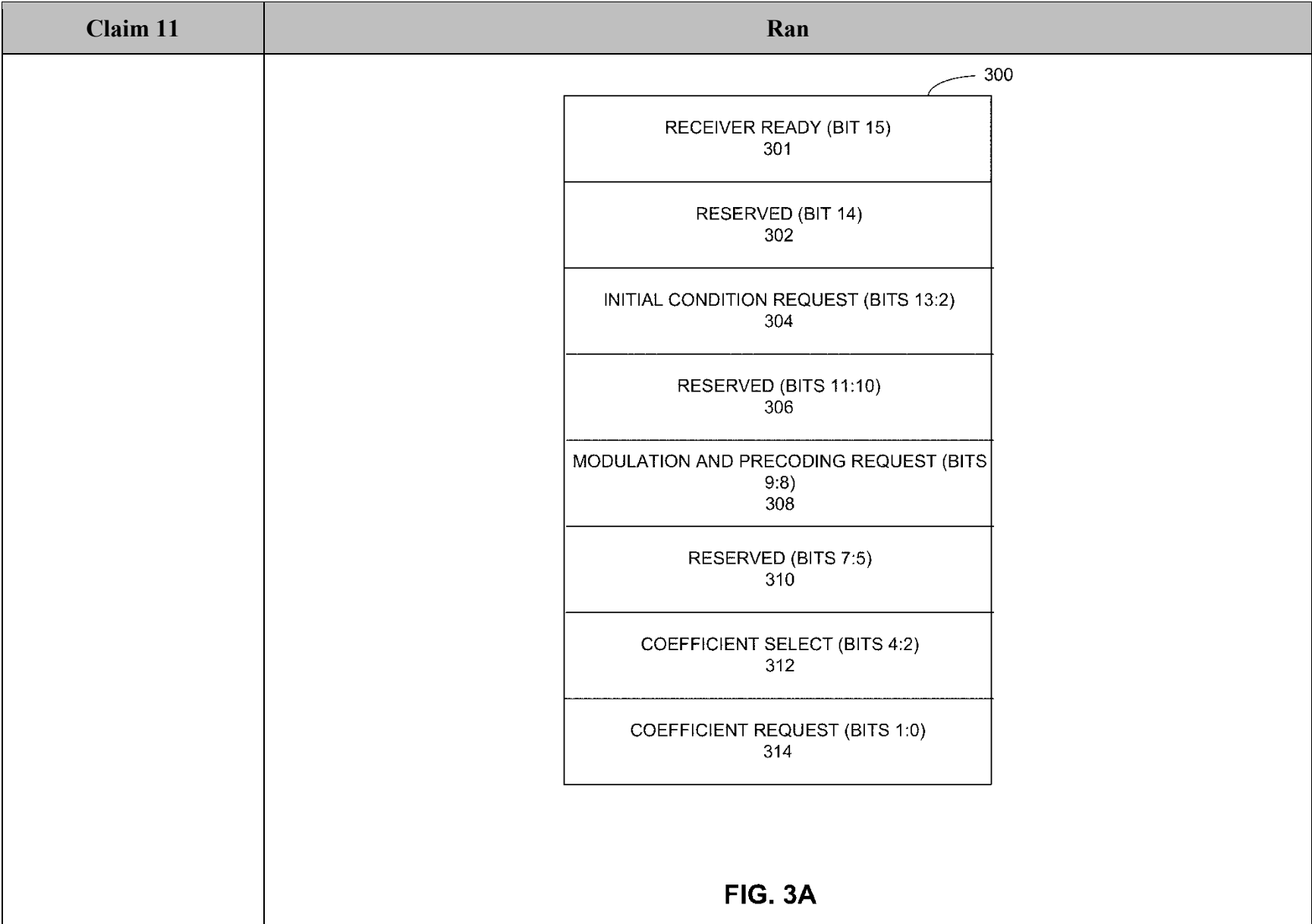


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	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
1	1	Preset3																													
1	0	Preset2																													
0	1	Preset1																													
0	0	Co-efficient Control																													
Bit 9	Bit 8	Description																													
1	1	PAM4 with precoding																													
1	0	PAM4																													
0	1	Reserved																													
0	0	PAM2																													

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	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
11[b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic,	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host.” Ran, 1:34-41; Ran Provisional at 2. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules

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Claim 11	Ran
	will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4. “Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily

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	fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause 136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “FIG. 2A illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface (AUI) Chip-to-Module (C2M) to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUI) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. In addition, the system can be used for C2C intercommunications.” Ran, 5:4-14; Ran Provisional at 7. “Host management registers 202 in the network interface controller 100 include a host request register 220 and a host response register 222. Module management registers 224 in the optical

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	module 120 include a module request register 224 and a module response register 226. The host management registers 202 and module management registers 204 are used at least in connection with two-way communications to perform timing recovery and equalization for a single-lane xGAUI-1 electrical link between the network interface controller 100 and the optical module 120 or other electrical interconnect module device.” Ran, 5:15-25; Ran Provisional at 7. “The request registers, host request register 220 and module request register 224, will be described in conjunction with FIGS. 3A-3E. The response registers, host response register 222 and module response register 226, will be described in conjunction with FIGS. 4A and 4B.” Ran, 5:34-38; Ran Provisional at 7-8. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8.

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Claim 11	Ran
	“The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8. “The host request register 220 can be written-to by the management entity. Writing this register has the effect of conveying the request message from module request register 224 of optical module 120 to the network interface controller 100 via host request register 220, which may change the equalization setting of one or more equalizer taps as requested. A response message can be generated by writing to host response register 222.” Ran, 6:5-12; Ran Provisional at 7-8. “For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8.

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Claim 11	Ran
	“The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog

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Claim 11	Ran
	converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Module 232 can be communicatively coupled to host 250 by an interconnect 244. Interconnect 244 can be electrical signal conductors that couple pins or holes of lane 240-0 to 240-N of a pluggable module 232 to holes or pins of lanes 254-0 to 254-N of host 250. Host 250 can transmit or receive signals in electrical format to or from module 232. In some examples, module 232 provides optical communications to and from any optical medium for host 250.” Ran, 7:60-67; Ran Provisional at 7-8.

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Claim 11	Ran
	“Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10.

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Claim 11	Ran
	“A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of –1. With a three bit

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	coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “The management entity may use the indication of “receiver ready” bit set to ‘1’ to permit transmission of real data (as opposed to training data) from the host transmitter to the module for transmission to a remote station (link partner). If the indication of “receiver ready” bit is not set to ‘1’, return to block 600 and the

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Claim 11	Ran
	receiver can continue to tune any transmitter equalizer settings for the same lane. For example, the “receiver ready” bit can be set to ‘1’ if a sufficiently low bit error rate (BER) is detected by the receiver.” Ran, 12:41-50; Ran Provisional at 12-13. “For example, equalization coefficients selected for a communications link between blades or other devices may need to be modified after the communications link is established to handle variations in operating conditions, for example, temperature and humidity that may cause an increase in bit errors over the communications link.” Ran, 15:45-50; Ran Provisional at 12-13. “FIG. 8 depicts a network interface. Various embodiments can use the network interface or be used by the network interface. Network interface 800 can use transceiver 802, processors 804, transmit queue 806, receive queue 808, memory 810, and bus interface 812, and DMA engine 852. Transceiver 802 can be capable of receiving and transmitting packets in conformance with the applicable protocols such as Ethernet as described in IEEE 802.3, although other protocols may be used. Transceiver 802 can receive and transmit packets from and to a network via a network medium (not depicted). Transceiver 802 can include PHY circuitry 814 and media access control (MAC) circuitry 816. PHY circuitry 814 can include encoding and decoding circuitry (not shown) to encode and decode data packets according to applicable physical layer specifications or standards. MAC circuitry 816 can be configured to assemble data to be transmitted into packets, that include destination and source addresses along with network control information and error detection hash values. Processors 804 can be any a combination of a: processor, core, graphics processing unit (GPU), field programmable gate array (FPGA), application specific integrated circuit (ASIC), or other programmable hardware device that allow programming of network interface 800. For example, processors 804 can provide for identification of a resource to use to perform a workload and generation of a bitstream for execution on the selected resource. For example, a “smart network interface” can provide packet processing capabilities in the network interface using processors 804.” Ran, 15:51-16:12; Ran Provisional at 12-14. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive

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Claim 11	Ran
	signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

Exhibit C-3

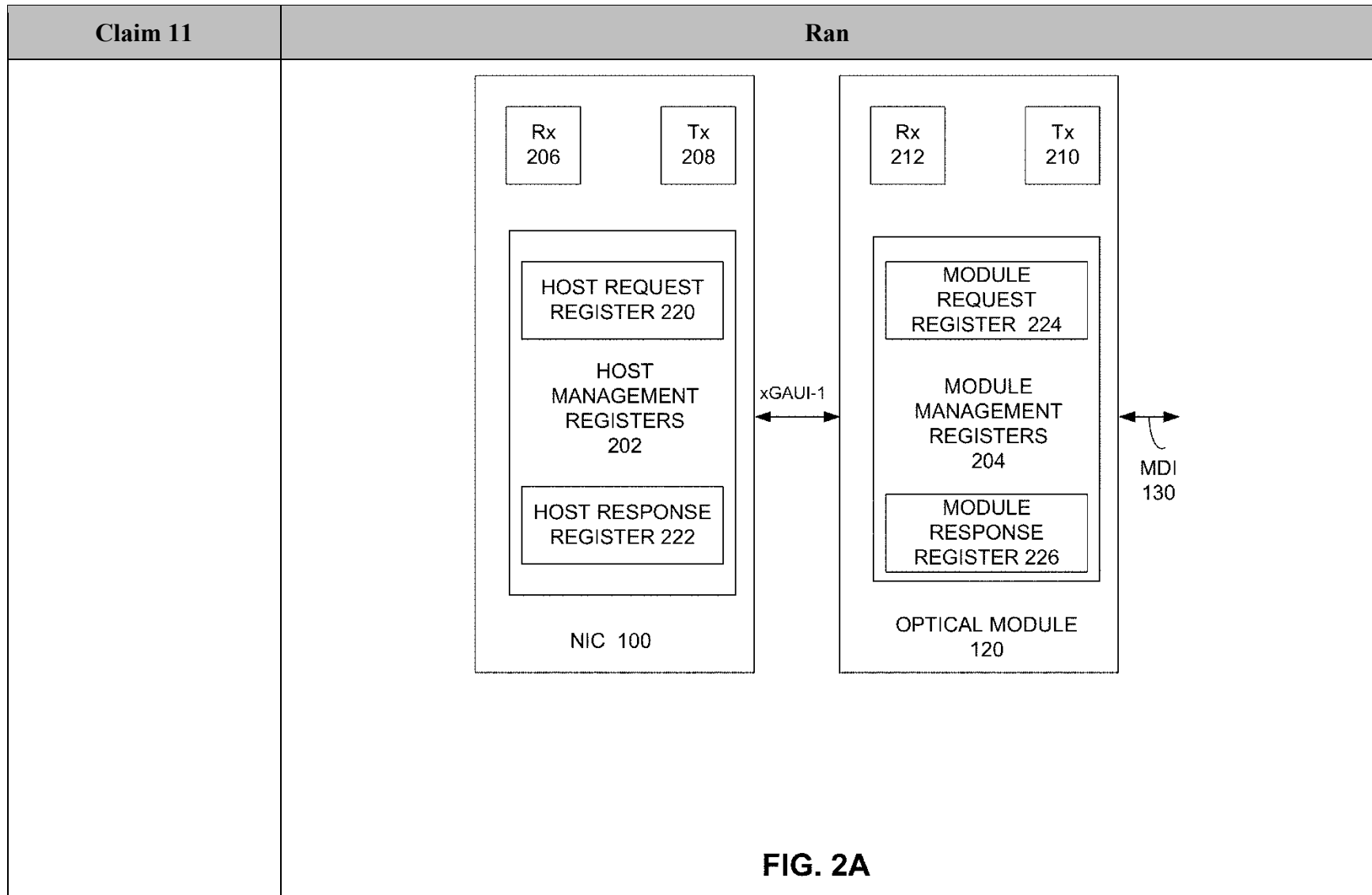


Exhibit C-3

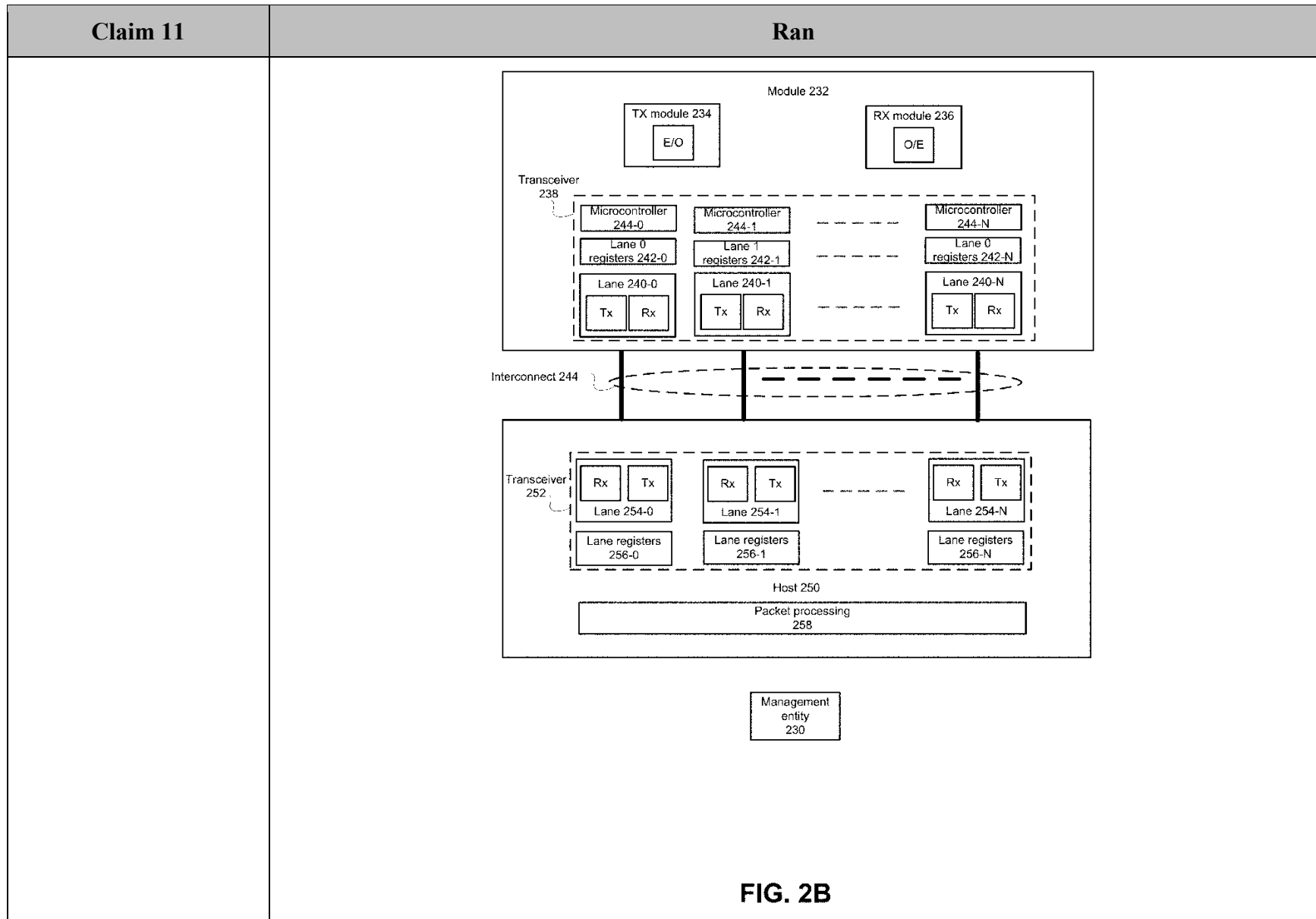


Exhibit C-3

Claim 11	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

Exhibit C-3

Claim 11	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
1	1	Preset3																													
1	0	Preset2																													
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0	1	Reserved																													
0	0	PAM2																													

Exhibit C-3

Claim 11	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
11[c] the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4.

Exhibit C-3

Claim 11	Ran
	“Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause

Exhibit C-3

Claim 11	Ran
	136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8. “The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8.

Exhibit C-3

Claim 11	Ran
	“For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8. “The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to

Exhibit C-3

Claim 11	Ran
	enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-

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Claim 11	Ran
	0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The

Exhibit C-3

Claim 11	Ran
	parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10. “A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not

Exhibit C-3

Claim 11	Ran
	require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-

Exhibit C-3

Claim 11	Ran
	to-module interface. The FFE 550 includes a pre-cursor tap c(−2), a pre-cursor tap c(−1), a cursor tap c(0), and a post-cursor tap c(1). The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

Exhibit C-3

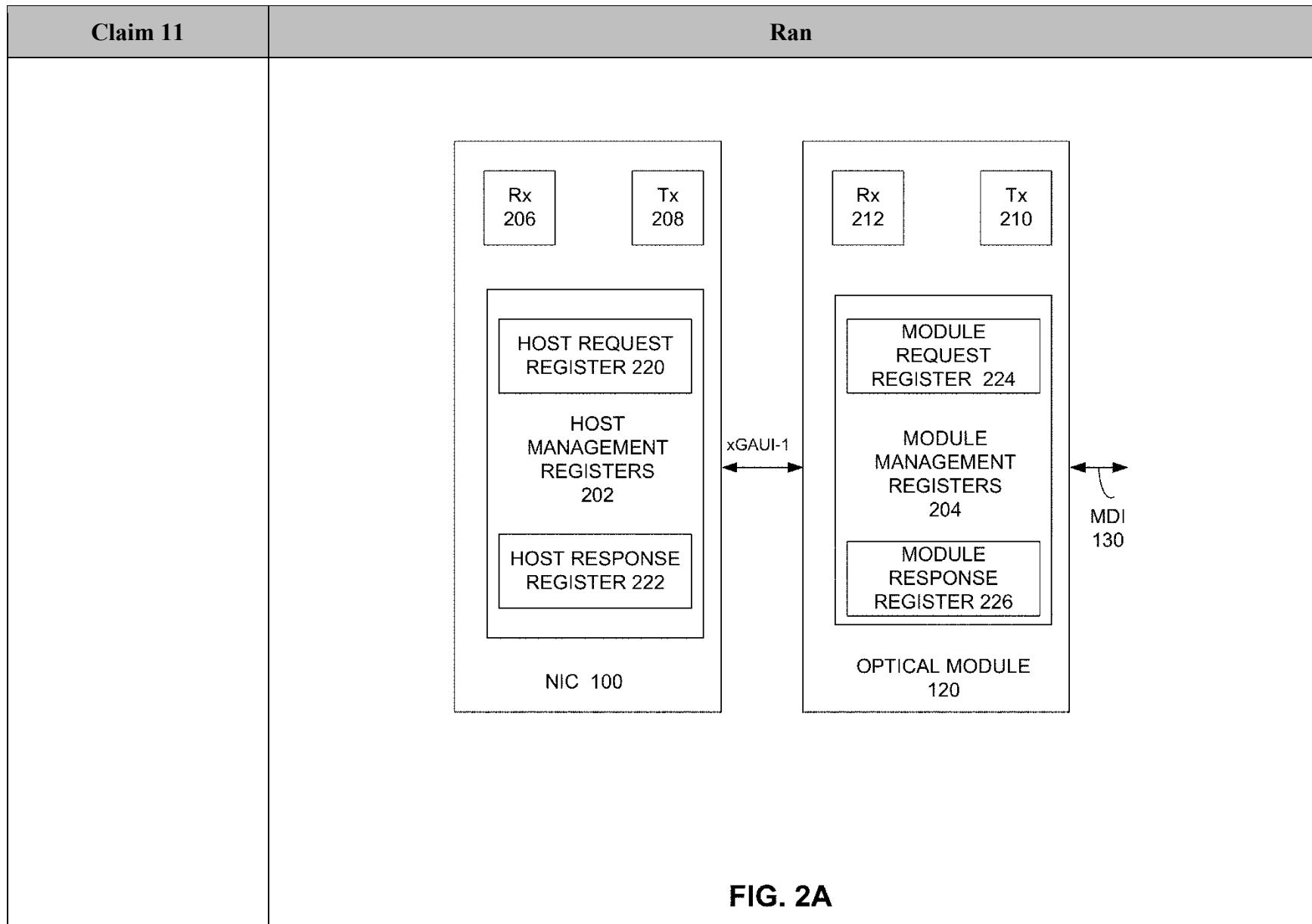


Exhibit C-3

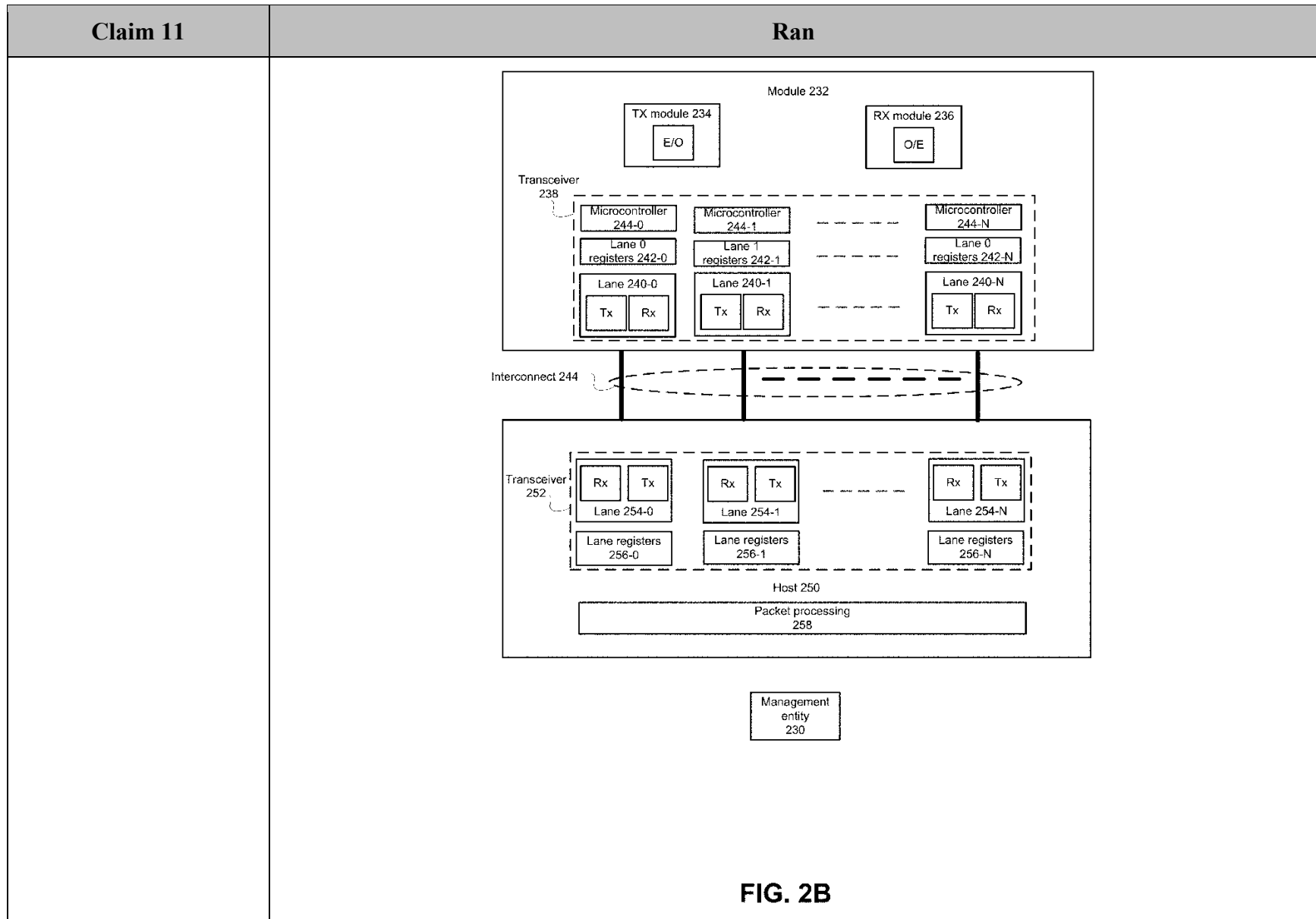


Exhibit C-3

Claim 11	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

Exhibit C-3

Claim 11	Ran																														
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Exhibit C-3

Claim 11	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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L. DEPENDENT CLAIM 12

Claim 12	Ran
12. The communications link of claim 11, wherein the performance characteristic is an error signal energy.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 12	Ran
	“The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-curser tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “The management entity may use the indication of “receiver ready” bit set to ‘1’ to permit transmission of real data (as opposed to training data) from the host transmitter to the module for transmission to a remote

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Claim 12	Ran
	station (link partner). If the indication of “receiver ready” bit is not set to ‘1’, return to block 600 and the receiver can continue to tune any transmitter equalizer settings for the same lane. For example, the “receiver ready” bit can be set to ‘1’ if a sufficiently low bit error rate (BER) is detected by the receiver.” Ran, 12:41-50; Ran Provisional at 12-13. “For example, equalization coefficients selected for a communications link between blades or other devices may need to be modified after the communications link is established to handle variations in operating conditions, for example, temperature and humidity that may cause an increase in bit errors over the communications link.” Ran, 15:45-50; Ran Provisional at 12-13. “FIG. 8 depicts a network interface. Various embodiments can use the network interface or be used by the network interface. Network interface 800 can use transceiver 802, processors 804, transmit queue 806, receive queue 808, memory 810, and bus interface 812, and DMA engine 852. Transceiver 802 can be capable of receiving and transmitting packets in conformance with the applicable protocols such as Ethernet as described in IEEE 802.3, although other protocols may be used. Transceiver 802 can receive and transmit packets from and to a network via a network medium (not depicted). Transceiver 802 can include PHY circuitry 814 and media access control (MAC) circuitry 816. PHY circuitry 814 can include encoding and decoding circuitry (not shown) to encode and decode data packets according to applicable physical layer specifications or standards. MAC circuitry 816 can be configured to assemble data to be transmitted into packets, that include destination and source addresses along with network control information and error detection hash values. Processors 804 can be any a combination of a: processor, core, graphics processing unit (GPU), field programmable gate array (FPGA), application specific integrated circuit (ASIC), or other programmable hardware device that allow programming of network interface 800. For example, processors 804 can provide for identification of a resource to use to perform a workload and generation of a bitstream for execution on the selected resource. For example, a “smart network interface” can provide packet processing capabilities in the network interface using processors 804.” Ran, 15:51-16:12; Ran Provisional at 12-14. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the

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Claim 12	Ran
	communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55; Ran Provisional at 16-18. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems

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Claim 12	Ran
	and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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M. DEPENDENT CLAIM 13

Claim 13	Ran
13. The communications link of claim 11, wherein the performance characteristic is a bit error rate.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 13	Ran
	“The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “The management entity may use the indication of “receiver ready” bit set to ‘1’ to permit transmission of real data (as opposed to training data) from the host transmitter to the module for transmission to a remote

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Claim 13	Ran
	station (link partner). If the indication of “receiver ready” bit is not set to ‘1’, return to block 600 and the receiver can continue to tune any transmitter equalizer settings for the same lane. For example, the “receiver ready” bit can be set to ‘1’ if a sufficiently low bit error rate (BER) is detected by the receiver.” Ran, 12:41-50; Ran Provisional at 12-13. “For example, equalization coefficients selected for a communications link between blades or other devices may need to be modified after the communications link is established to handle variations in operating conditions, for example, temperature and humidity that may cause an increase in bit errors over the communications link.” Ran, 15:45-50; Ran Provisional at 12-13. “FIG. 8 depicts a network interface. Various embodiments can use the network interface or be used by the network interface. Network interface 800 can use transceiver 802, processors 804, transmit queue 806, receive queue 808, memory 810, and bus interface 812, and DMA engine 852. Transceiver 802 can be capable of receiving and transmitting packets in conformance with the applicable protocols such as Ethernet as described in IEEE 802.3, although other protocols may be used. Transceiver 802 can receive and transmit packets from and to a network via a network medium (not depicted). Transceiver 802 can include PHY circuitry 814 and media access control (MAC) circuitry 816. PHY circuitry 814 can include encoding and decoding circuitry (not shown) to encode and decode data packets according to applicable physical layer specifications or standards. MAC circuitry 816 can be configured to assemble data to be transmitted into packets, that include destination and source addresses along with network control information and error detection hash values. Processors 804 can be any a combination of a: processor, core, graphics processing unit (GPU), field programmable gate array (FPGA), application specific integrated circuit (ASIC), or other programmable hardware device that allow programming of network interface 800. For example, processors 804 can provide for identification of a resource to use to perform a workload and generation of a bitstream for execution on the selected resource. For example, a “smart network interface” can provide packet processing capabilities in the network interface using processors 804.” Ran, 15:51-16:12; Ran Provisional at 12-14. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the

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Claim 13	Ran
	communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55; Ran Provisional at 16-18. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems

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Claim 13	Ran
	and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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N. DEPENDENT CLAIM 14

Claim 14	Ran
14. The communications link of claim 11, wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 14	Ran
	“The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over

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Claim 14	Ran
	the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of

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Claim 14	Ran
	registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two-bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10.

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Claim 14	Ran
	“FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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O. DEPENDENT CLAIM 15

Claim 15	Ran
15. The communications link of claim 14, wherein the controller saves updated coefficient values in one of the registers.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 15	Ran
	“The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over

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Claim 15	Ran
	the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of

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Claim 15	Ran
	registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two-bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10.

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Claim 15	Ran
	“FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

Exhibit C-3

P. INDEPENDENT CLAIM 16

Claim 16	Ran
16[pre] A pluggable module transceiver including:	To the extent the preamble is limiting, Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host.” Ran, 1:34-41; Ran Provisional at 2. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is

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Claim 16	Ran
	established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “FIG. 2A illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface (AUI) Chip-to-Module (C2M) to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUI) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. In addition, the system can be used for C2C intercommunications.” Ran, 5:4-14; Ran Provisional at 7. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used

Exhibit C-3

Claim 16	Ran
	to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8.

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Claim 16	Ran
	“FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “FIG. 10 depicts an example of a data center. Various embodiments can be used in or with the data center of FIG. 10 to adjust transmitter equalizer settings for any electrical or optical signal transmitter. As shown in FIG. 10, data center 1000 may include an optical fabric 1012. Optical fabric 1012 may generally include a combination of optical signaling media (such as optical cabling) and optical switching infrastructure via which any particular sled in data center 1000 can send signals to (and receive signals from) the other sleds in data center 1000. The signaling connectivity that optical fabric 1012 provides to any given sled may include connectivity both to other sleds in a same rack and sleds in other racks. Data center 1000 includes four racks 1002A to 1002D and racks 1002A to 1002D house respective pairs of sleds 1004A-1 and 1004A-2, 1004B-1 and 1004B-2, 1004C-1 and 1004C-2, and 1004D-1 and 1004D-2. Thus, in this example, data center 1000 includes a total of eight sleds. Optical fabric 1012 can provide sled signaling connectivity with one or more of the seven other sleds. For example, via optical fabric 1012, sled 1004A-1 in rack 1002A may possess signaling connectivity with sled 1004A-2 in rack 1002A, as well as the six other sleds 1004B-1, 1004B-2, 1004C-1, 1004C-2, 1004D-1, and 1004D-2 that are distributed among the other racks 1002B, 1002C, and 1002D of data center 1000. The embodiments are not limited to this example. For example, fabric 1012 can provide optical and/or electrical signaling.” Ran, 16:64-17:23; Ran Provisional at 14, 16. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive

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Claim 16	Ran
	signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55; Ran Provisional at 16-18. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; ; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; ; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; ; Ran Provisional at 16-18.

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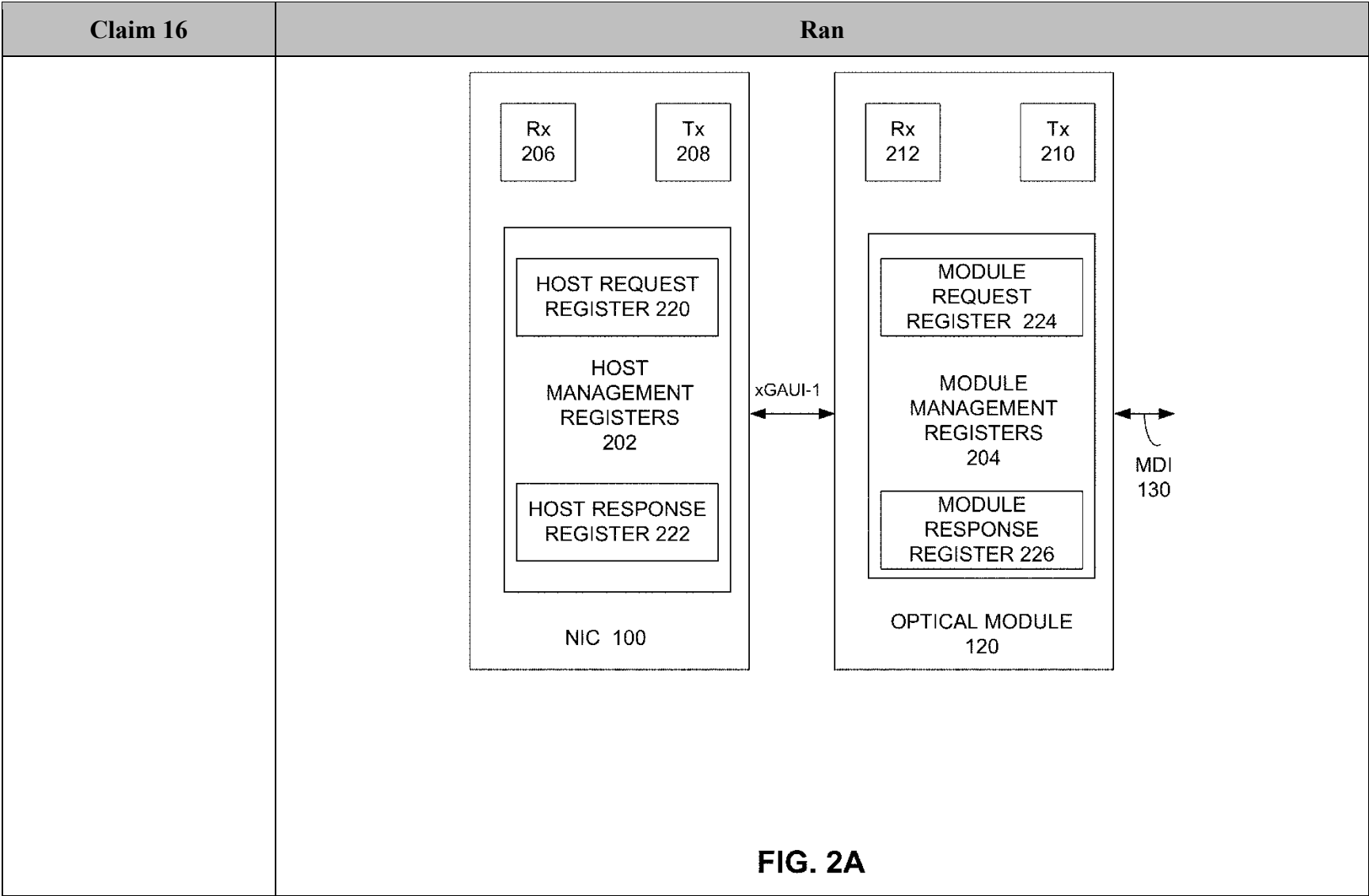


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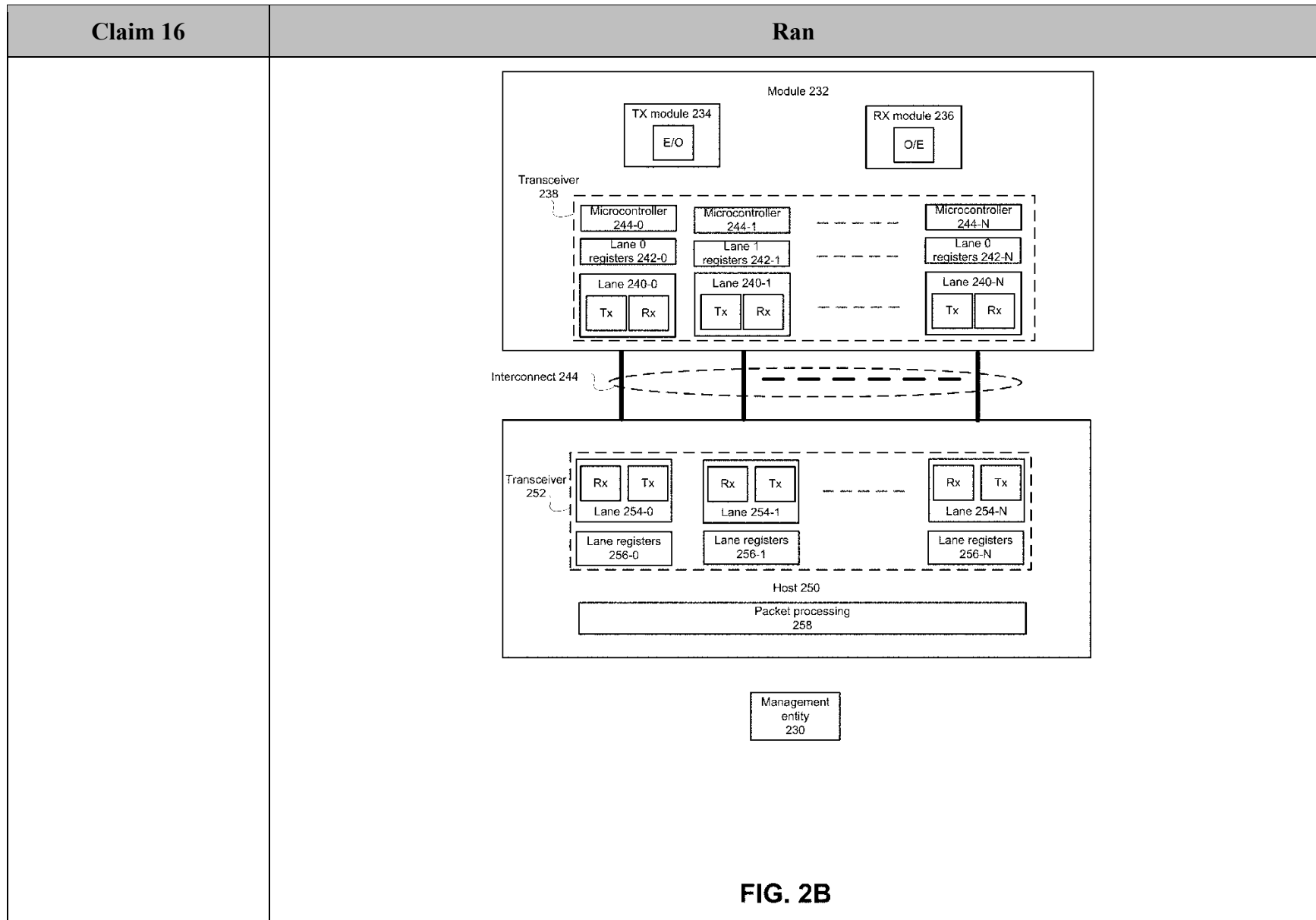


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Claim 16	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

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Claim 16	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
1	1	Preset3																													
1	0	Preset2																													
0	1	Preset1																													
0	0	Co-efficient Control																													
Bit 9	Bit 8	Description																													
1	1	PAM4 with precoding																													
1	0	PAM4																													
0	1	Reserved																													
0	0	PAM2																													

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Claim 16	Ran
	To the extent that this preamble is not disclosed, either explicitly or inherently, by Ran, this preamble is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
16[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to a port transceiver; and	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4.

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Claim 16	Ran
	“Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause

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Claim 16	Ran
	136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8. “The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8.

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Claim 16	Ran
	“For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8. “The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to

Exhibit C-3

Claim 16	Ran
	enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-

Exhibit C-3

Claim 16	Ran
	0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The

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Claim 16	Ran
	parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10. “A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not

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Claim 16	Ran
	require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-

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Claim 16	Ran
	to-module interface. The FFE 550 includes a pre-cursor tap c(−2), a pre-cursor tap c(−1), a cursor tap c(0), and a post-cursor tap c(1). The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

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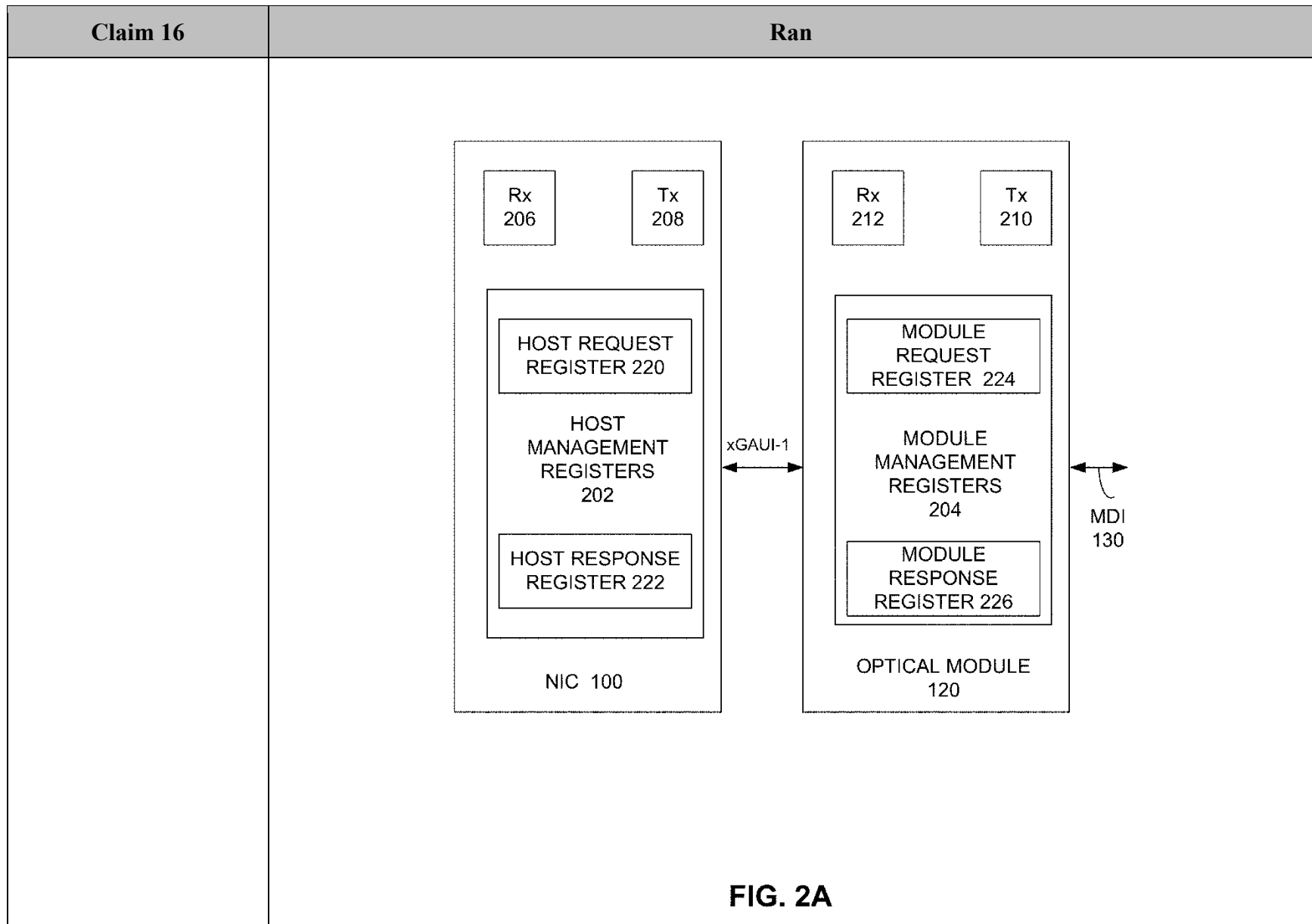


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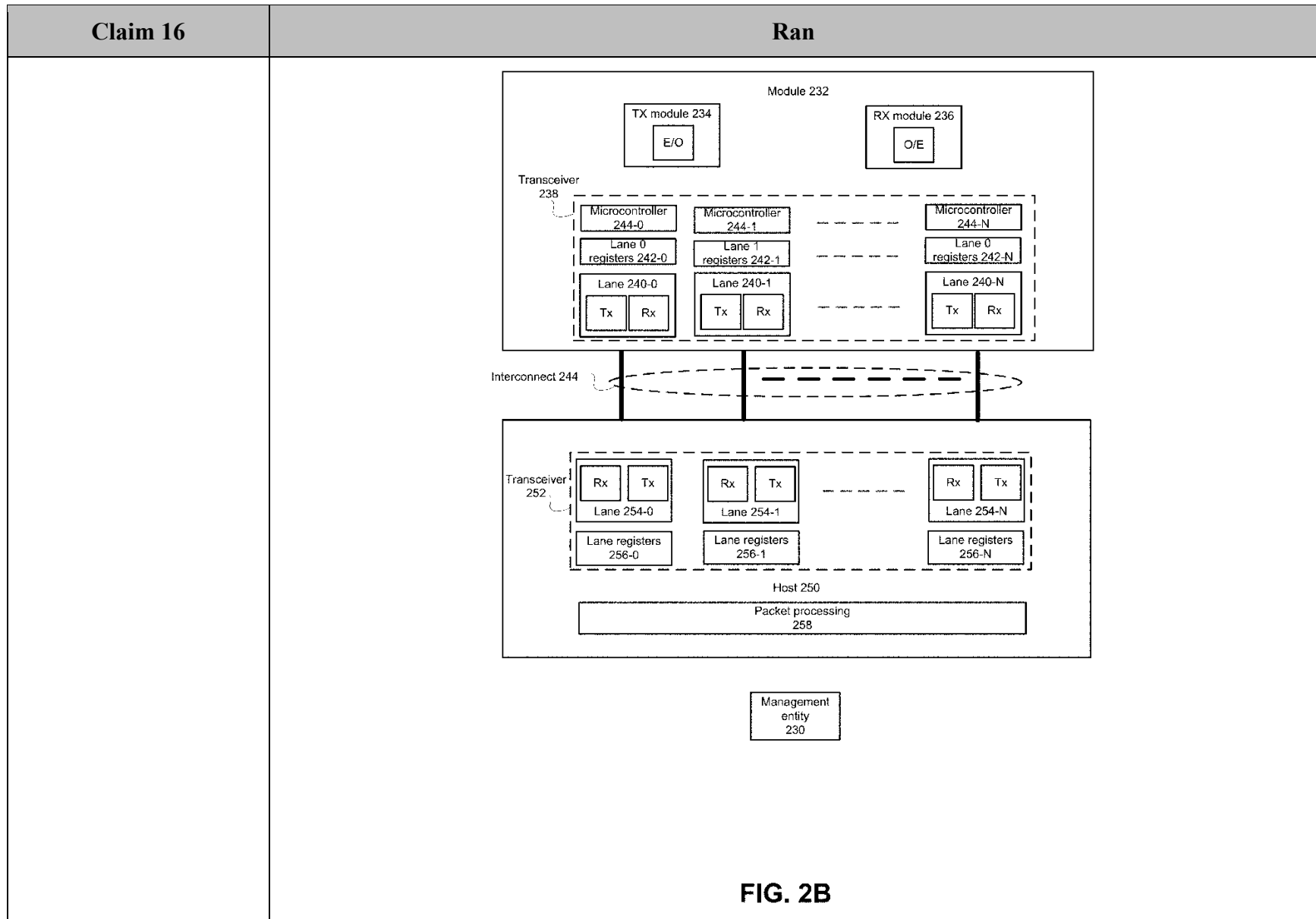


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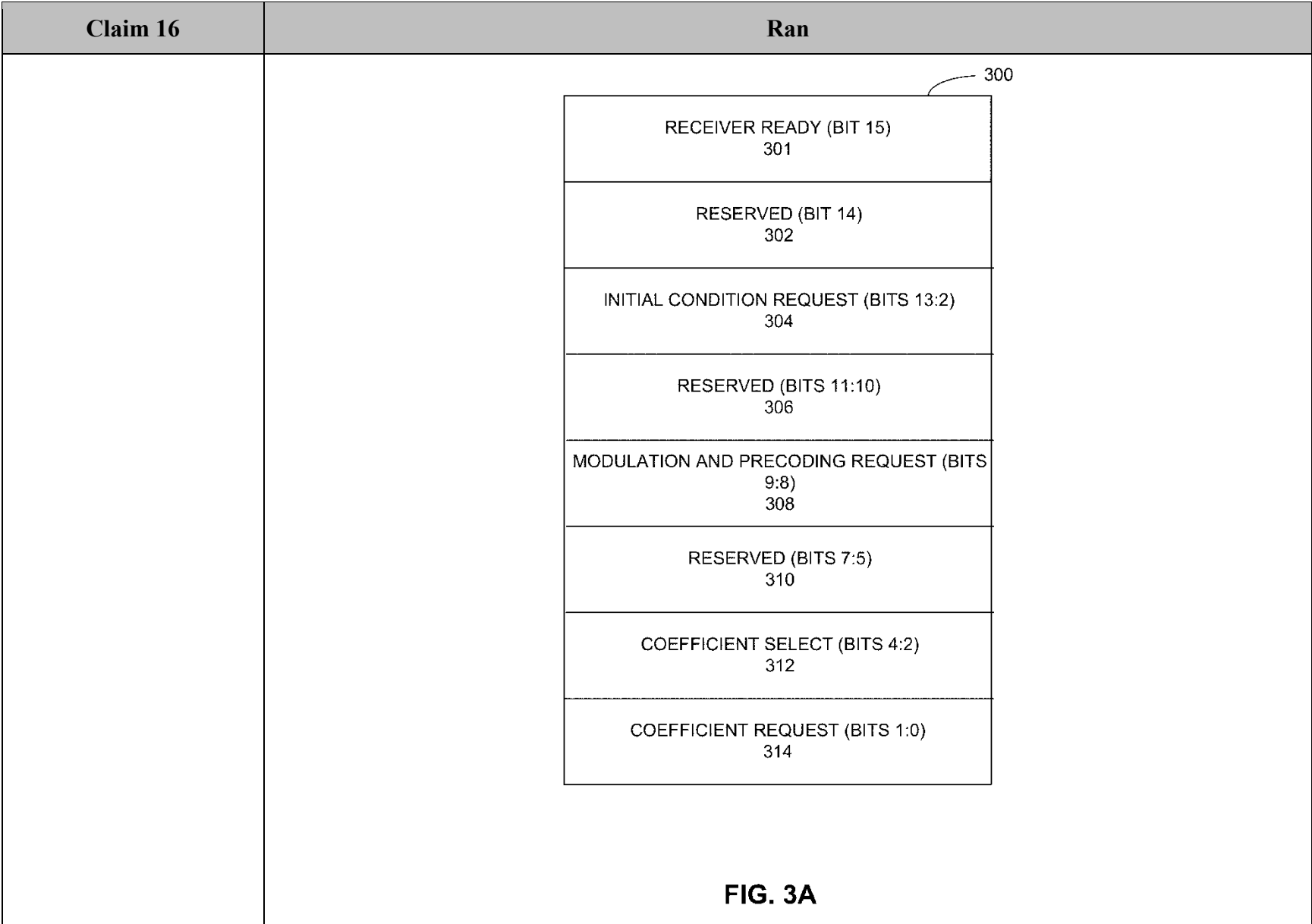


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Claim 16	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
1	1	Preset3																													
1	0	Preset2																													
0	1	Preset1																													
0	0	Co-efficient Control																													
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1	1	PAM4 with precoding																													
1	0	PAM4																													
0	1	Reserved																													
0	0	PAM2																													

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	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
16[b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model,	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host.” Ran, 1:34-41; Ran Provisional at 2. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules

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	will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4. “Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily

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Claim 16	Ran
	fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause 136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “FIG. 2A illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface (AUI) Chip-to-Module (C2M) to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUI) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. In addition, the system can be used for C2C intercommunications.” Ran, 5:4-14; Ran Provisional at 7. “Host management registers 202 in the network interface controller 100 include a host request register 220 and a host response register 222. Module management registers 224 in the optical

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	module 120 include a module request register 224 and a module response register 226. The host management registers 202 and module management registers 204 are used at least in connection with two-way communications to perform timing recovery and equalization for a single-lane xGAUI-1 electrical link between the network interface controller 100 and the optical module 120 or other electrical interconnect module device.” Ran, 5:15-25; Ran Provisional at 7. “The request registers, host request register 220 and module request register 224, will be described in conjunction with FIGS. 3A-3E. The response registers, host response register 222 and module response register 226, will be described in conjunction with FIGS. 4A and 4B.” Ran, 5:34-38; Ran Provisional at 7-8. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8.

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Claim 16	Ran
	“The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8. “The host request register 220 can be written-to by the management entity. Writing this register has the effect of conveying the request message from module request register 224 of optical module 120 to the network interface controller 100 via host request register 220, which may change the equalization setting of one or more equalizer taps as requested. A response message can be generated by writing to host response register 222.” Ran, 6:5-12; Ran Provisional at 7-8. “For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8.

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Claim 16	Ran
	“The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog

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Claim 16	Ran
	converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Module 232 can be communicatively coupled to host 250 by an interconnect 244. Interconnect 244 can be electrical signal conductors that couple pins or holes of lane 240-0 to 240-N of a pluggable module 232 to holes or pins of lanes 254-0 to 254-N of host 250. Host 250 can transmit or receive signals in electrical format to or from module 232. In some examples, module 232 provides optical communications to and from any optical medium for host 250.” Ran, 7:60-67; Ran Provisional at 7-8.

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Claim 16	Ran
	“Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10.

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Claim 16	Ran
	“A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of –1. With a three bit

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	coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive

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	signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

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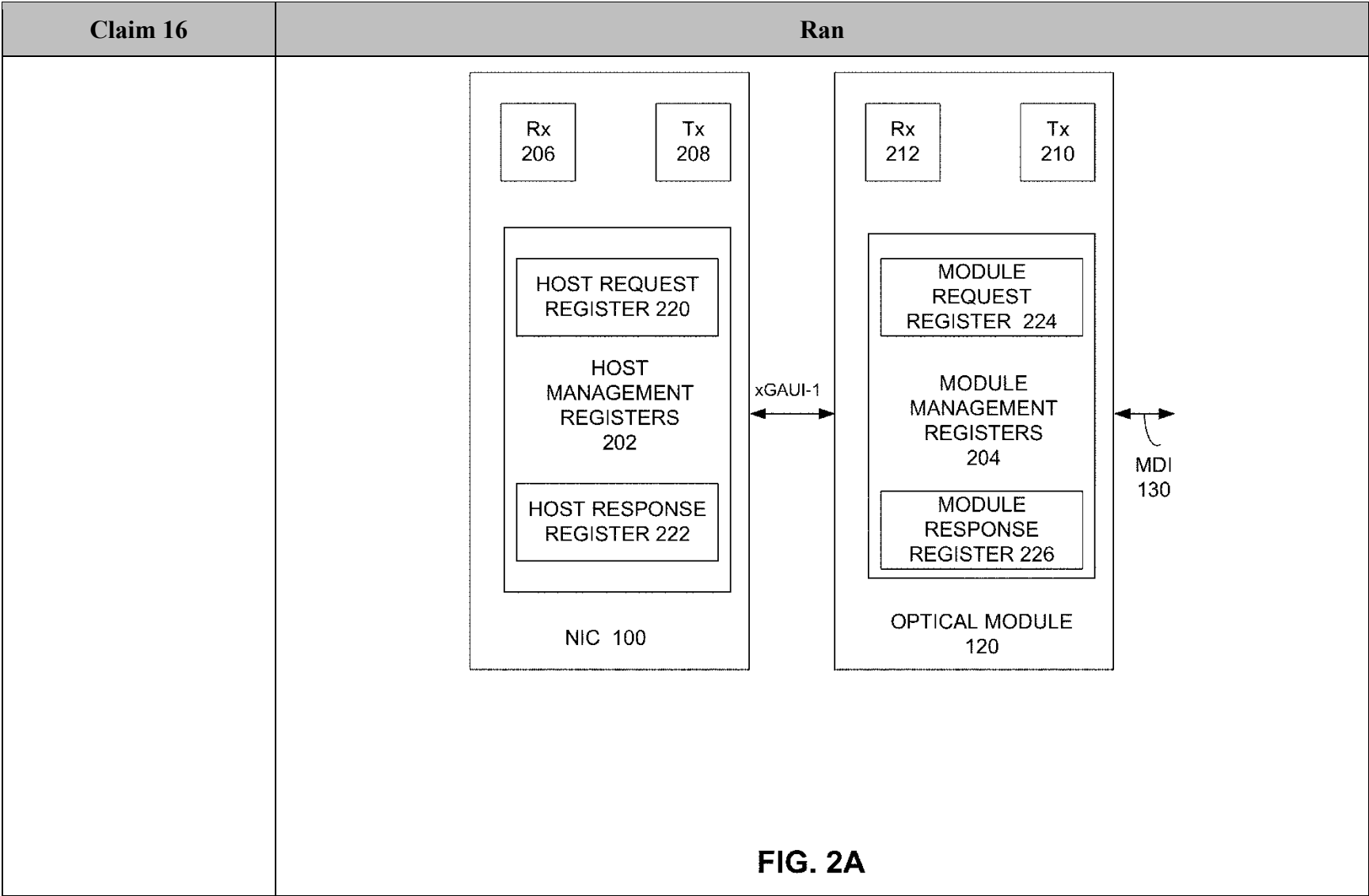


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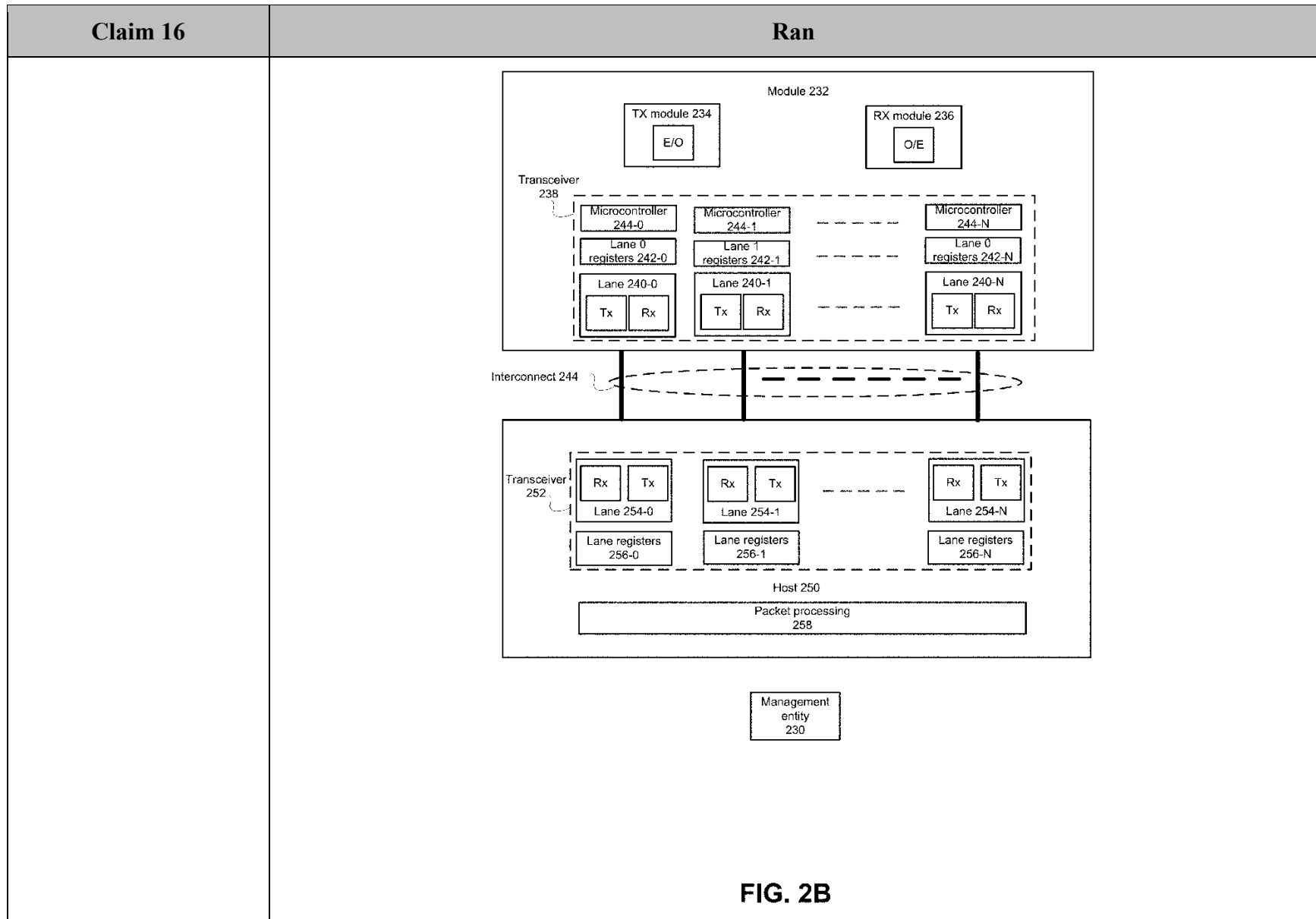


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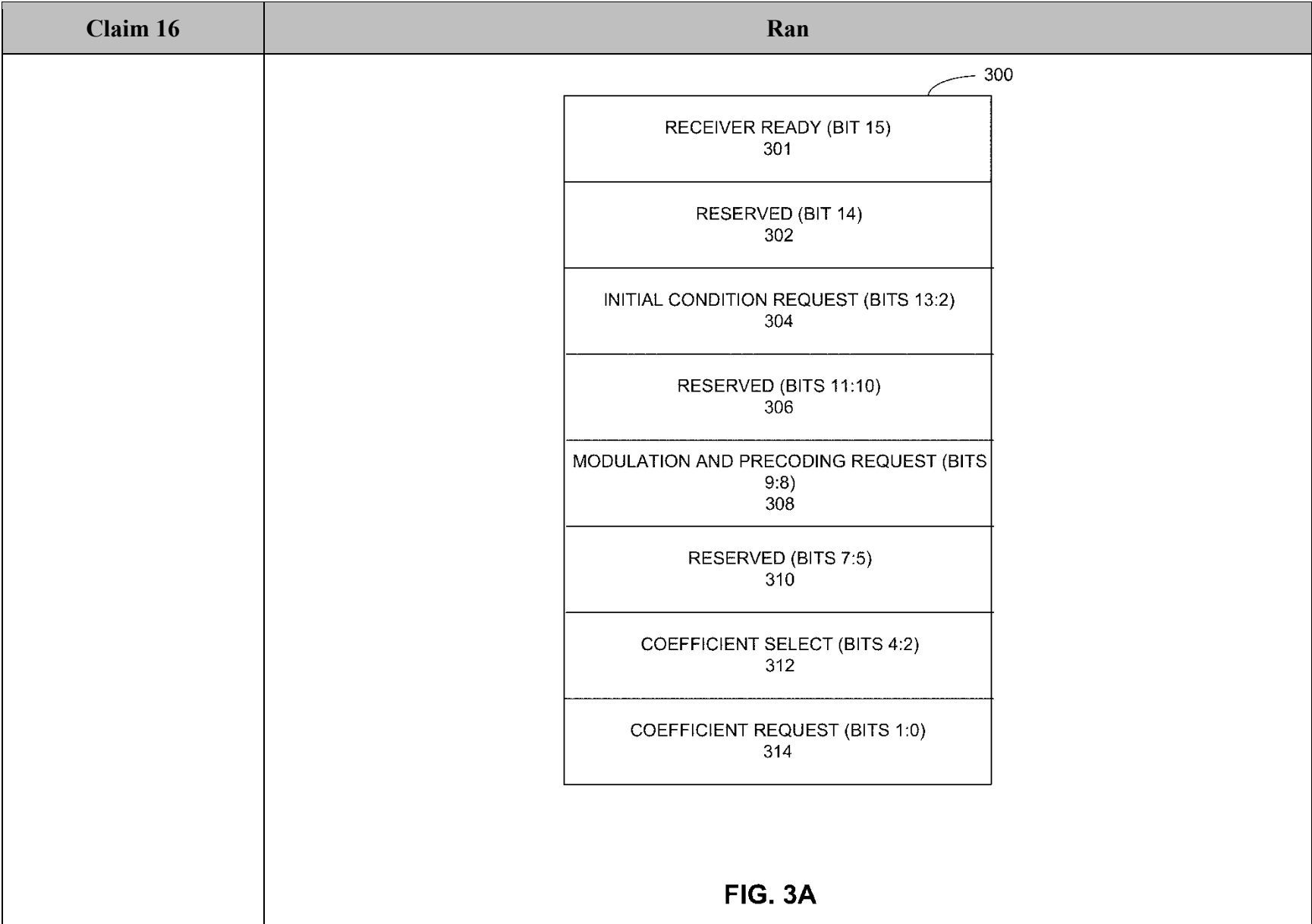


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Claim 16	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
Bit 13	Bit 12	Description																													
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Exhibit C-3

Claim 16	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
16[c] the controller using one of the registers to set initial coefficient values for the one or more transmit filters.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “The C2C versions include specified transmit equalization using a 3-tap feed-forward equalizer (FFE) with 2 degrees of freedom whereby two taps are controllable and the third tap is set as a function of the other two. The tap settings are controlled with standardized management registers, which may be programmed to fixed settings, or optionally managed with a request-response procedure that can be performed by a management entity (accessing both receive and transmit sides). These registers and procedure are specified in sections 83D.3.1.1, 83D.3.3.2, and 83D.5 of the Ethernet standard (IEEE Std 802.3-2018). However, the registers specified in the C2C AUIs are limited to 3-tap FFE with a small number of settings, which is too short and too coarse for equalization of a 100 Gb/s per lane AUI. As the data rate is increased above 50 Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings.” Ran, 2:40-59; Ran Provisional at 4.

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Claim 16	Ran
	“Ethernet over backplane and over copper cable assemblies use link startup protocols (specified in clause 72 of IEEE 802.3-2015 and in Clause 136 of IEEE Std 802.3cd-2018) that enable tuning transmit equalization using request and response messages. These protocols operate in-band before the link is established and do not require a common management entity to access registers on both transmit and receive sides. The request (control field) and response (status field) messages in clause 136 are described in Table 136-9 and Table 136-10 of IEEE Std 802.3cd-2018, respectively. A link startup protocol as in clause 136 requires logic on both ends to encode and decode request and response messages. This logic may not be desirable in a module implementation. Also, because this protocol operates in-band, it would not enable continuous adaptation after the link is established.” Ran, 2:66-3:13; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5. “A station management entity (STA) can monitor for messages in registers and read or write request and response message among registers when the request ID is toggled. The request ID bit can be toggled whenever a new request is generated and the management entity can read a source register to copy the content to a destination register. The management entity can access both the host application specific integrated circuit (ASIC) (e.g., MAC, PCS, FEC, or PMA) and the module during start-up and/or after start-up and during operation. According to some embodiments, continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions (such as temperature and humidity). However, the content of these registers is different from those of section 83D.5 and instead can be based on the message structure of the startup protocol of clause 136 of IEEE Std 802.3cd-2018, more specifically subclause

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Claim 16	Ran
	136.8.11.1.2 (Control and status fields). The message structure of the startup protocol enables changing one coefficient at a time, independent of a change to another coefficient, with a directed change request and arbitrarily fine steps.” Ran, 3:29-50; Ran Provisional at 4-5. “Module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller, or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (e.g., FIG. 3A). In an embodiment, module request register 224 includes a coefficient select field and a coefficient request field and may also include a modulation and precoding request field and an initial condition request field.” Ran, 5:39-49; Ran Provisional at 7-8. “The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120 (or vice versa).” Ran, 5:50-54; Ran Provisional at 7-8. “The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated.” Ran, 5:55-61; Ran Provisional at 7-8. “The module request register 224 may also include a three-bit lane identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (FIG. 3A). The lane identifier field in the module request register 224 can be used to indicate the specific lane (out of several lanes) that the request applies to, in a module that has multi-lane attachment unit interface, such as a 2-lane 200 Gbps AUI (200GAUI-2). If a lane identifier is used, the host response register 222 may also include a corresponding lane identifier echo field.” Ran, 5:62-6:4; Ran Provisional at 7-8.

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Claim 16	Ran
	“For NIC 100 to communicate with optical module 120, module response register 226 can be written-to by the management entity to copy content of fields of host response register 222 to module response register 226. Writing to module response register 226 has the effect of conveying the response message to the optical module 120 and completing the request-response transaction. The optical module 120 may then generate further requests if needed or signal that there are no further requests using the receiver ready field in the module request register 224.” Ran, 6:13-22; Ran Provisional at 7-8. “The “receiver ready” bit is set in module request register 224 when the receiver 212 in the optical module 120 does not have further requests from the transmitter 208 in the network interface controller (e.g., host) 100. The management entity may use this indication to start sending data from the network interface controller 100 to the optical module 120 for transmission to a remote station (link partner). The management entity may continue monitoring the host management registers 202 and module management registers 204 as described in conjunction with the flowgraph shown in FIG. 6A, to enable continuous or periodic adaptation of equalizer settings used to transmit signals over an operational link between the network interface controller 100 and the optical module 120.” Ran, 6:23-36; Ran Provisional at 7-8. “The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to

Exhibit C-3

Claim 16	Ran
	enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-

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Claim 16	Ran
	0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The

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Claim 16	Ran
	parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “A single bit “receiver ready” field 301 can be included in bit position 15 to indicate to a management entity that the equalization tuning is complete for one or all lanes and that data may be reliably transmitted from the host to the receive module on one or more lanes.” Ran, 9:60-64; Ran Provisional at 8-10. “A single bit “request ID” field can be included in part of a reserved bit to indicate to a management entity that a new request is available. The request ID bit can be toggled whenever a new request is generated. The management entity can respond by the toggling of request ID by copying a content of a register to a destination register.” Ran, 9:65-10:3; Ran Provisional at 8-10. “A reserved bit can be used to indicate an amount to decrement or increment a coefficient.” Ran, 10:4-5; Ran Provisional at 8-10. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two- bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not

Exhibit C-3

Claim 16	Ran
	require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10. “FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-

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Claim 16	Ran
	to-module interface. The FFE 550 includes a pre-cursor tap c(−2), a pre-cursor tap c(−1), a cursor tap c(0), and a post-cursor tap c(1). The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18.

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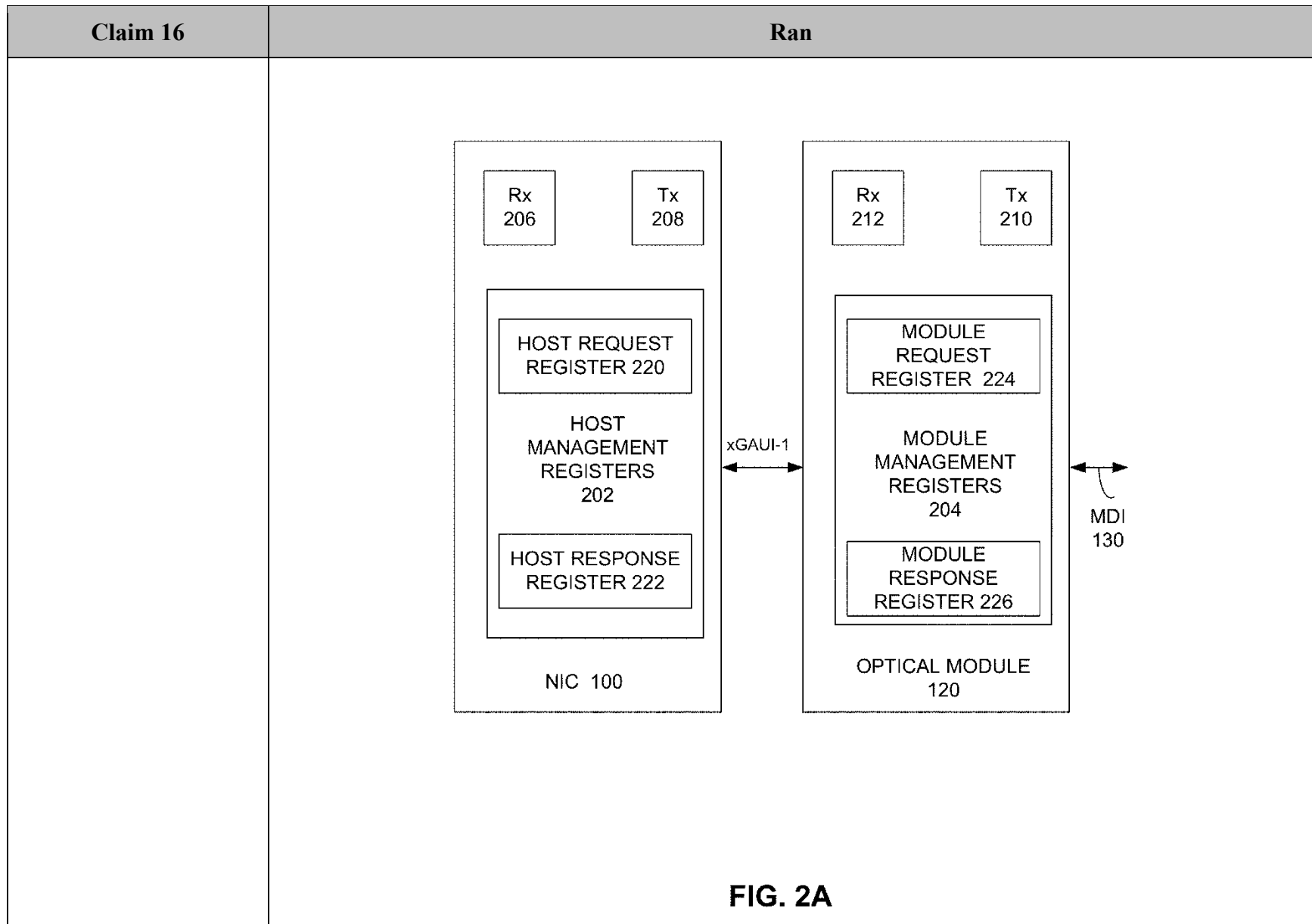


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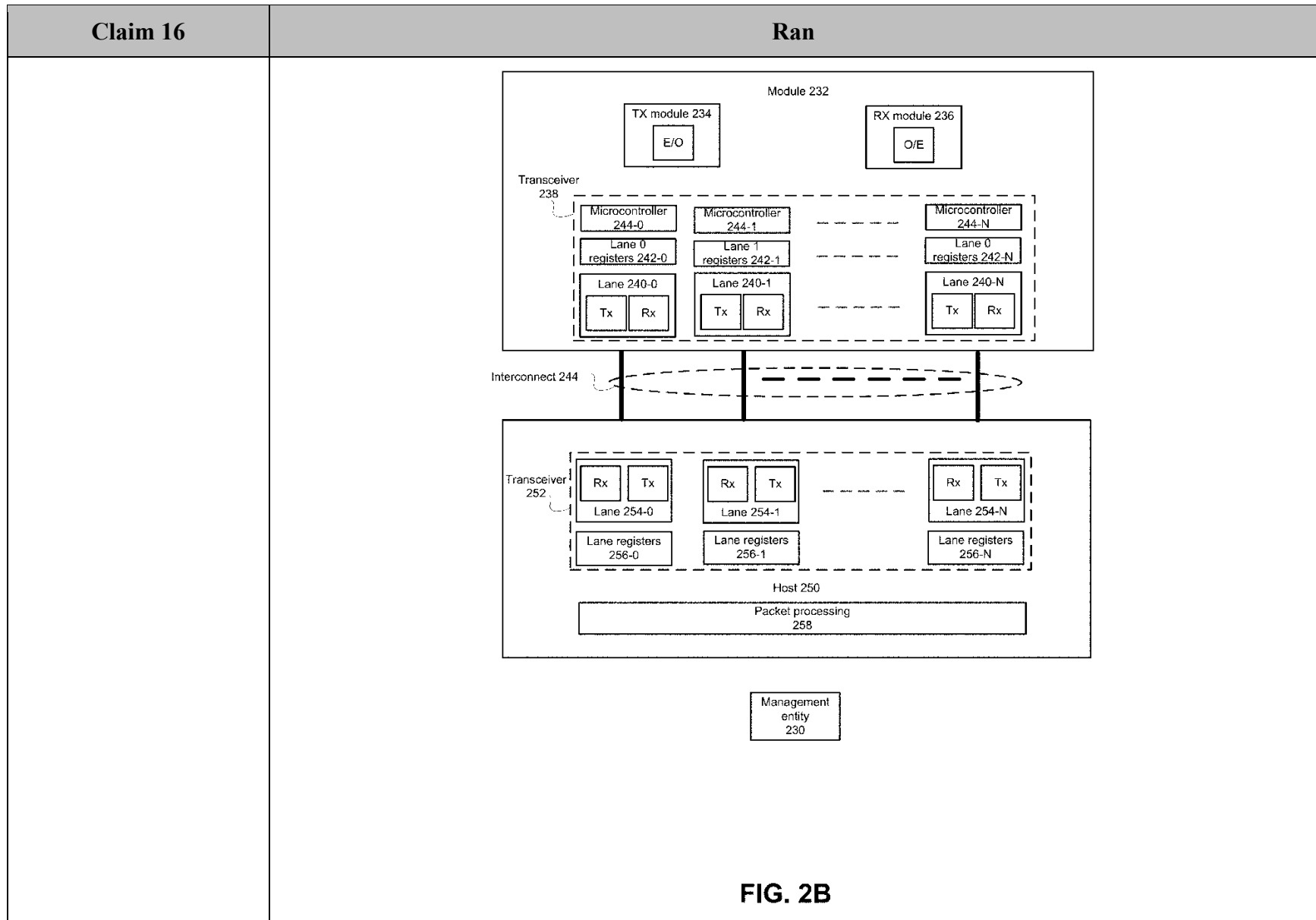


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Claim 16	Ran
	300 RECEIVER READY (BIT 15) 301 RESERVED (BIT 14) 302 INITIAL CONDITION REQUEST (BITS 13:2) 304 RESERVED (BITS 11:10) 306 MODULATION AND PRECODING REQUEST (BITS 9:8) 308 RESERVED (BITS 7:5) 310 COEFFICIENT SELECT (BITS 4:2) 312 COEFFICIENT REQUEST (BITS 1:0) 314 FIG. 3A

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Claim 16	Ran																														
	<table><tr><th>Bit 13</th><th>Bit 12</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>Preset3</td></tr><tr><td>1</td><td>0</td><td>Preset2</td></tr><tr><td>0</td><td>1</td><td>Preset1</td></tr><tr><td>0</td><td>0</td><td>Co-efficient Control</td></tr></table> FIG. 3B <table><tr><th>Bit 9</th><th>Bit 8</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>PAM4 with precoding</td></tr><tr><td>1</td><td>0</td><td>PAM4</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>0</td><td>PAM2</td></tr></table> FIG. 3C	Bit 13	Bit 12	Description	1	1	Preset3	1	0	Preset2	0	1	Preset1	0	0	Co-efficient Control	Bit 9	Bit 8	Description	1	1	PAM4 with precoding	1	0	PAM4	0	1	Reserved	0	0	PAM2
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Claim 16	Ran
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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Q. DEPENDENT CLAIM 17

Claim 17	Ran
17. The pluggable module transceiver of claim 16, wherein the port transceiver determines a performance characteristic for each register.	Ran discloses and/or renders obvious this limitation. Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 17	Ran
	“The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “In an embodiment, there may be four additional registers, two module management registers in the optical module 120 and two host management registers in the network interface controller 100 to enable control of transmitter equalization in the optical module 120 by host or NIC 100. The four additional registers can have similar fields to the fields as those used in host management registers 220, 222 and module management registers 224, 226. Copying of content of registers can be made in a similar manner as that for optical module 120 to control transmitter settings of NIC 100.” Ran, 6:52-62; Ran Provisional at 7-8. “FIG. 2B depicts an example system for communicatively coupling a chip to a module. The system can provide a chip-to-module (C2M) communications. The system can be used in a network interface, host computing platform, switch, router, interconnect, fabric, rack, server, or any computing or communications device. For example, an optical transceiver module can be connected to an interface with multiple electrical links. The system provides for multiple lanes of transmit-receive pairs that can be used to transmit or receive electrical signals between the module and the device. A lane can transmit and/or receive a signal. A transmitter of a lane can use an equalizer implemented in an analog circuit to generate an electrical signal for transmission. The equalizer can have one or more current sources that are used to create a signal whereby weights of current sources can be adjusted to change signal characteristics. Equalizer settings can be modified to change weights of current sources. For example, a digital-to-analog converter (DAC) can be used to create signal in the digital domain and output the result in an analog format.” Ran, 6:63-7:15; Ran Provisional at 7-8. “Various embodiments use any of the message structures of the startup protocol (or PMD control function) specified in subclause 136.8.11 of IEEE Std 802.3cd-2018, but instead of passing messages over

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Claim 17	Ran
	the physical medium, use a set of registers is used as a 2-way communication channel. A set of four management registers are defined for each lane of the xAUI C2C or C2M.” Ran, 7:16-22; Ran Provisional at 7-8. “Transceiver 238 can be used for electrical signal transmission and receipt between module 232 and host network interface device 250. Transceiver 238 can provide multiple transmit and receive lanes for electrical signal communication between module 232 and host device 250. For example, lanes 240-0 to 240-N can provide transmit and receive circuitry for coupling with receive and transmit circuitry of lanes 254-0 to 254-N of host device 250. Lane registers 242-0 to 242-N can act as registers for lanes 240-0 to 240-N. According to some embodiments, transceiver 238 can write to any of lane registers 242-0 to 242-N to communicate with a lane partner in host 250 or communicate with management entity 230. For example, any parameter described with respect to the parameters of FIG. 3A-3E can be written in any of lane registers 242-0 to 242-N. In other examples, any parameter described with respect to the parameters of FIGS. 4A and 4B can be written in any of lane registers 242-0 to 242-N. For example, lane registers 242-0 to 242-N can represent one or multiple registers for a lane. In some examples, some lanes may share use of a register instead of a register being allocated to every lane. A register can be a region of memory, in some examples. In some examples, any address or register defined by the SFP standard or other form factor standards can be used for a register.” Ran, 7:36-59; Ran Provisional at 7-8. “Management entity 230 manages operations at least of analog transmit and receive circuitry of lanes 240-0 to 240-N and lanes 254-0 to 254-N. For example, any of registers 242-0 to 242-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 240-0 to 240-N. Likewise, any of registers 256-0 to 256-N can be used to receive or transmit lane-specific operating commands or feedback for any of lanes 254-0 to 254-N. For example, one or more of microcontrollers 244-0 to 244-N can write one or more parameters to any of lane registers 242-0 to 242-N. For example, a single microcontroller can manage equalizer settings of several lanes. The one or more parameters can cause a transmit device in any of lanes 254-0 to 254-N to adjust its equalizer setting for a specific tap, whether to increase or decrease the coefficient value of an equalizer tap. In some embodiments, the settings of a tap can be adjusted independent of adjustment of settings of another tap. In response, a microcontroller associated with any of lanes 254-0 to 254-N can write a response to any of

Exhibit C-3

Claim 17	Ran
	registers 256-0 to 256-N. The response can indicate that the equalizer setting was applied or not applied.” Ran, 8:22-43; Ran Provisional at 7-8. “FIG. 3A depicts an embodiment of a control field structure in a request register 300. Register 300 can be used as one of two registers in a two-way communication channel on at least one lane of an AUI Chip-to-Chip (C2C) or Chip-to-Module (C2M). Any field or parameter of the control field structure in the request register 300 may be written in host request register 220 and module request register 224 shown in FIG. 2A, host response register 222 and module response register 226 of FIG. 2A (e.g., when NIC 100 tunes a transmitter equalizer setting of optical module 120), or registers of any system of FIG. 2B or 2C. The parameters can be set to convey actions to take by a transmitter device. In some examples, a management entity can access a register that stores one or more of the parameters and copy one or more of the parameters to a destination register.” Ran, 9:45-59; Ran Provisional at 8-9. “In the embodiment shown, the request register 300 is a sixteen-bit register. There are three reserved one or two-bit fields 302, 306, 310. A two-bit initial condition request field 304 is used to select one of three predefined transmitter equalizer configurations (“presets”). If one of the presets is not selected, that is, the binary value of the initial condition request field 304 is ‘00’, coefficient select field 312 and coefficient request field 314 are used to update the transmitter equalizer configuration.” Ran, 10:6-14; Ran Provisional at 8-10. “FIG. 3B illustrates a mapping of binary bit values in the initial condition request field 304 of request register 300. Modulation and precoding request field 308 can be a two-bit field that is used to request that a link partner transmitter transmit one of three training pattern formats. The training patterns may use Pulse Amplitude Modulation (PAM) that has two distinct levels (PAM-2) to encode two bits of data or PAM-4 that has four distinct levels to encode two bits of data. Initial training uses PAM-2 which does not require a high signal quality. When quality is sufficiently high, training switches to PAM-4 which is used for data transmission after training is complete. FIG. 3C illustrates an example of mapping of bit values in the modulation and precoding request field 308.” Ran, 10:15-29; Ran Provisional at 8-10.

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Claim 17	Ran
	“FIG. 3D illustrates a mapping of bit values in the coefficient select field 312 for four coefficients. The coefficient select field 312 can be used to identify a coefficient that is the target of a coefficient request. The value of the coefficient select field 312 can be the two's complement encoding of a coefficient index. For example, binary value 111 can correspond to a coefficient index of -1. With a three bit coefficient select field 312, 8 coefficients may be defined to improve the accuracy of the transmitter equalization. In an embodiment the 3-bit coefficient select field 312 may be extended to 4 or more bits, to enable more than 8 coefficients to improve the accuracy of the receiver equalization.” Ran, 10:29-40; Ran Provisional at 8-10. “FIG. 3E illustrates a mapping of bit values in the coefficient request field 314. The coefficient request field 314 is used to change the value of the coefficient specified by the coefficient select bits in the coefficient select field 312. A coefficient may be changed by incrementing or decrementing its value or by setting it to “No equalization”. The “No equalization” value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.” Ran, 10:41-47; Ran Provisional at 8-10. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

Exhibit C-3

R. DEPENDENT CLAIM 18

Claim 18	Ran
18. The pluggable module transceiver of claim 17, wherein the performance characteristic is an error signal energy.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 18	Ran
	“The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “The management entity may use the indication of “receiver ready” bit set to ‘1’ to permit transmission of real data (as opposed to training data) from the host transmitter to the module for transmission to a remote

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Claim 18	Ran
	station (link partner). If the indication of “receiver ready” bit is not set to ‘1’, return to block 600 and the receiver can continue to tune any transmitter equalizer settings for the same lane. For example, the “receiver ready” bit can be set to ‘1’ if a sufficiently low bit error rate (BER) is detected by the receiver.” Ran, 12:41-50; Ran Provisional at 12-13. “For example, equalization coefficients selected for a communications link between blades or other devices may need to be modified after the communications link is established to handle variations in operating conditions, for example, temperature and humidity that may cause an increase in bit errors over the communications link.” Ran, 15:45-50; Ran Provisional at 12-13. “FIG. 8 depicts a network interface. Various embodiments can use the network interface or be used by the network interface. Network interface 800 can use transceiver 802, processors 804, transmit queue 806, receive queue 808, memory 810, and bus interface 812, and DMA engine 852. Transceiver 802 can be capable of receiving and transmitting packets in conformance with the applicable protocols such as Ethernet as described in IEEE 802.3, although other protocols may be used. Transceiver 802 can receive and transmit packets from and to a network via a network medium (not depicted). Transceiver 802 can include PHY circuitry 814 and media access control (MAC) circuitry 816. PHY circuitry 814 can include encoding and decoding circuitry (not shown) to encode and decode data packets according to applicable physical layer specifications or standards. MAC circuitry 816 can be configured to assemble data to be transmitted into packets, that include destination and source addresses along with network control information and error detection hash values. Processors 804 can be any a combination of a: processor, core, graphics processing unit (GPU), field programmable gate array (FPGA), application specific integrated circuit (ASIC), or other programmable hardware device that allow programming of network interface 800. For example, processors 804 can provide for identification of a resource to use to perform a workload and generation of a bitstream for execution on the selected resource. For example, a “smart network interface” can provide packet processing capabilities in the network interface using processors 804.” Ran, 15:51-16:12; Ran Provisional at 12-14. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the

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Claim 18	Ran
	communications link; and a management entity, wherein: the receiver in the first device is to receive signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55; Ran Provisional at 16-18. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems

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Claim 18	Ran
	and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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S. DEPENDENT CLAIM 19

Claim 19	Ran
19. The pluggable module transceiver of claim 17, wherein the performance characteristic is a bit error rate.	Ran discloses and/or renders obvious this limitation. “Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical or electrical communication module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity.” Ran, Abstract; Ran Provisional at 22. “Previous technologies up to 50GAUI-n were separated to chip-to-module (C2M) and chip-to-chip (C2C). The C2M versions do not explicitly specify transmit equalization in the host but specify an “open eye” at the receive module with a very simple equalizer at the receive side. This typically requires some transmit equalization. Transmit equalization is implementation specific and may be tuned by the host board manufacturer, based on the board characteristics, to optimize the eye opening. Fixed equalization as done in existing C2M AUIs may not work well in 100 Gb/s per lane, as the variations between modules will likely require different equalization settings, and variable operating conditions will have a higher effect on circuits and boards.” Ran, 2:26-39; Ran Provisional at 4. “Various embodiments provide for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver. In some embodiments, equalizer settings can be adjusted per-lane at least for C2C or C2M connections. Request and response registers are accessible to a management entity to enable changing one equalization coefficient at a time, with a directed change request and arbitrarily fine steps. Various embodiments provide for request and response registers accessible to a management entity, as in the C2C AUIs (as specified in 83D.5 from IEEE 802.3-2018, as well as other future standards and derivatives thereof) and C2M AUIs. Various embodiments can be used in connection with IEEE P802.3ck for 100 Gbp/s, 200 Gbp/s, 400 Gbp/s and other speeds as well as future standards and derivatives thereof.” Ran, 3:14-28; Ran Provisional at 4-5.

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Claim 19	Ran
	“The contents of host request register 220 are set in an implementation-dependent way, and the requests to tune the transmit equalizer so that when “receiver ready” is set to 1, the receiver 212 in the optical module 120 receiver can operate at a sufficiently low bit error ratio (BER). The contents of register host response register 222 are set by the network interface controller 100 according to whether the request is accepted or not.” Ran, 6:37-44; Ran Provisional at 7-8. “The continuous or periodic equalization after the link is established may allow a greater distance between a network interface controller 100 and an optical module 102 in a host-to-module 100 Gb/s per lane channel and also reduce the power requirement for optical modules to tune the transmitter equalizer to allow more optical modules per panel in a network switch.” Ran, 6:45-51; Ran Provisional at 7-8. “FIG. 5A depicts an example of equalizer. The transmitter equalizer 500 includes a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-cursor tap $c(1)$. In an illustrative embodiment, filter tap settings identifies one of four possible tap values for the pre-cursor tap $c(-1)$ using two bits and one of six possible tap values for the post-cursor tap $c(1)$. The cursor tap $c(0)$ coefficient may be calculated based on the values of the other two tap coefficients, $c(-1)$ and $c(1)$, such that the equation: $c(0)-c(1)-c(-1)-1$, is satisfied. The filter tap settings may be modified by incrementing or decrementing the filter tap settings.” Ran, 11:45-55; Ran Provisional at 11. “FIG. 5B depicts a functional model of a structure of a four-tap feed-forward equalizer (FFE) 550 in a transmitter. An FFE 550 is implemented in each communication lane interface of a chip-to-chip or chip-to-module interface. The FFE 550 includes a pre-cursor tap $c(-2)$, a pre-cursor tap $c(-1)$, a cursor tap $c(0)$, and a post-curser tap $c(1)$. The filter tap settings may be modified by incrementing or decrementing the filter tap settings. A coefficient of any tap may be modified independent of coefficient of another tap or taps.” Ran, 11:56-65; Ran Provisional at 11. “The management entity may use the indication of “receiver ready” bit set to ‘1’ to permit transmission of real data (as opposed to training data) from the host transmitter to the module for transmission to a remote station (link partner). If the indication of “receiver ready” bit is not set to ‘1’, return to block 600 and the

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Claim 19	Ran
	receiver can continue to tune any transmitter equalizer settings for the same lane. For example, the “receiver ready” bit can be set to ‘1’ if a sufficiently low bit error rate (BER) is detected by the receiver.” Ran, 12:41-50; Ran Provisional at 12-13. “For example, equalization coefficients selected for a communications link between blades or other devices may need to be modified after the communications link is established to handle variations in operating conditions, for example, temperature and humidity that may cause an increase in bit errors over the communications link.” Ran, 15:45-50; Ran Provisional at 12-13. “FIG. 8 depicts a network interface. Various embodiments can use the network interface or be used by the network interface. Network interface 800 can use transceiver 802, processors 804, transmit queue 806, receive queue 808, memory 810, and bus interface 812, and DMA engine 852. Transceiver 802 can be capable of receiving and transmitting packets in conformance with the applicable protocols such as Ethernet as described in IEEE 802.3, although other protocols may be used. Transceiver 802 can receive and transmit packets from and to a network via a network medium (not depicted). Transceiver 802 can include PHY circuitry 814 and media access control (MAC) circuitry 816. PHY circuitry 814 can include encoding and decoding circuitry (not shown) to encode and decode data packets according to applicable physical layer specifications or standards. MAC circuitry 816 can be configured to assemble data to be transmitted into packets, that include destination and source addresses along with network control information and error detection hash values. Processors 804 can be any a combination of a: processor, core, graphics processing unit (GPU), field programmable gate array (FPGA), application specific integrated circuit (ASIC), or other programmable hardware device that allow programming of network interface 800. For example, processors 804 can provide for identification of a resource to use to perform a workload and generation of a bitstream for execution on the selected resource. For example, a “smart network interface” can provide packet processing capabilities in the network interface using processors 804.” Ran, 15:51-16:12; Ran Provisional at 12-14. “Example 1 includes a device-to-device connection apparatus comprising: a first device comprising a receiver for a lane of a communications link; a second device comprising a transmitter for the lane of the communications link; and a management entity, wherein: the receiver in the first device is to receive

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Claim 19	Ran
	signals from the transmitter of the second device, the first device including a plurality of management registers, the second device including a plurality of management registers, and in response to detection of toggling of a request identifier bit, the management entity is to communicate equalization settings from the receiver to the transmitter by a copy of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.” Ran, 19:40-55; Ran Provisional at 16-18. “Example 2 includes any example, wherein the management entity is to communicate equalization settings from the receiver to the transmitter during link operation.” Ran, 19:55-57; Ran Provisional at 16-18. “Example 5 includes any example, wherein a set of four registers are defined for the lane to communicate equalizer settings and receive feedback on the use or non-use of the settings.” Ran, 20:1-4; Ran Provisional at 16-18. “Example 7 includes any example, wherein the first device comprises an electrical signal communications device.” Ran, 20:7-8; Ran Provisional at 16-18. “Example 8 includes any example, wherein the management entity is to reconfigure equalization for the communications link after the communications link is established.” Ran, 20:9-11; Ran Provisional at 16-18. To the extent that this limitation is not disclosed, either explicitly or inherently, by Ran, this limitation is obvious to a person of ordinary skill in the art based on (1) Ran alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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The Ran Provisional provides the below written disclosure under 35 U.S.C. §112 for at least Ran’s Claim 1. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1380-81 (Fed. Cir. 2015). The disclosures below showing such a disclosure are exemplary only, and Respondents reserve the right to rely on additional support in the Ran reference.

Claim 1	Ran Provisional
1. A device-to-device connection apparatus comprising:	• Selection of equalization coefficients to configure a communications link between a receiver in a host system and a transmitter in an optical module is performed by a management entity with access to management registers in the receiver and transmitter. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established to handle varying operating conditions such as temperature and humidity. Ran Provisional at 22 (Abstract). • Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host. Ran Provisional at 2. • As the data rate is increased above 50Gb/s, for example to 100 Gb/s per lane, fixed equalization as performed in a 50 Gb/s per lane chip-to-module Attachment Unit Interface may not work well in a 100 Gb/s per lane chip-to-module Attachment Unit Interface, because variations between modules may require different equalization settings. In addition, a Chip-to-Chip Attachment Unit Interface is limited to 3-tap FFE with a small number of settings that are not sufficient for equalization of a 100 Gb/s per lane Attachment Unit Interface (AUi). Ran Provisional at 4. • Fig. 2 illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface(AUi) Chip-to-Module to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUi) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. Ran Provisional at 7.

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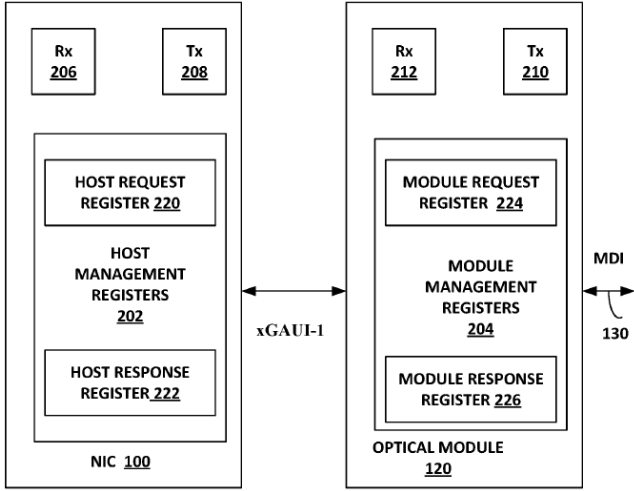
	 FIG. 2
a first device comprising a receiver for a lane of a communications link;	- Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host. Ran Provisional at 2. - Fig. 2 illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface(AUi) Chip-to-Module to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AU<i>i</i>) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. Ran Provisional at 7. - Host management registers 202 in the network interface controller 100 include a host request register 220 and a host response register 222. Module management registers 224 in the optical module 120 include a module request register 224 and a module response register 224. The host management registers 202 and module management registers 224 are used as a two-way

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communications channel to perform timing recovery and equalization for a single-lane xGAUI-1 electrical link between the network interface controller 100 and the optical module 120. Ran Provisional at 7.

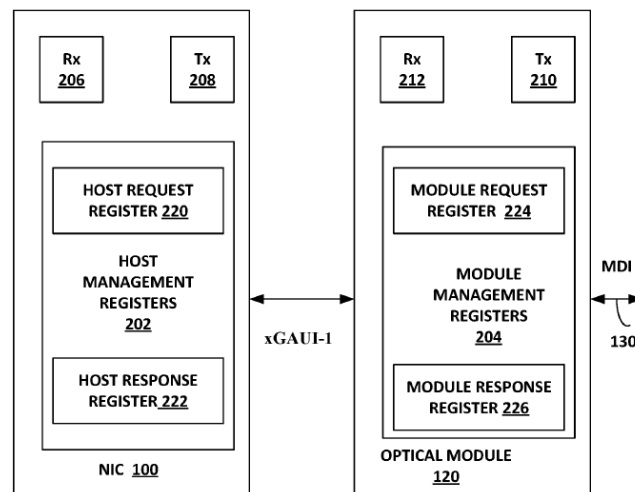


FIG. 2

a second device comprising a transmitter for the lane of the communications link; and

- Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host. Ran Provisional at 2.
- Fig. 2 illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface(AUi) Chip-to-Module to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AU)i Chip-to-Module forms a single link between

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	the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. Ran Provisional at 7. Host management registers 202 in the network interface controller 100 include a host request register 220 and a host response register 222. Module management registers 224 in the optical module 120 include a module request register 224 and a module response register 224. The host management registers 202 and module management registers 224 are used as a two-way communications channel to perform timing recovery and equalization for a single-lane xGAUI-1 electrical link between the network interface controller 100 and the optical module 120. Ran Provisional at 7. FIG. 2
a management entity, wherein:	Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver

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	equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host. Ran Provisional at 2. • Fig. 2 illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface(AUi) Chip-to-Module to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUi) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. Ran Provisional at 7. • Host management registers 202 in the network interface controller 100 include a host request register 220 and a host response register 222. Module management registers 224 in the optical module 120 include a module request register 224 and a module response register 224. The host management registers 202 and module management registers 224 are used as a two-way communications channel to perform timing recovery and equalization for a single-lane xGAUI-1 electrical link between the network interface controller 100 and the optical module 120. Ran Provisional at 7.
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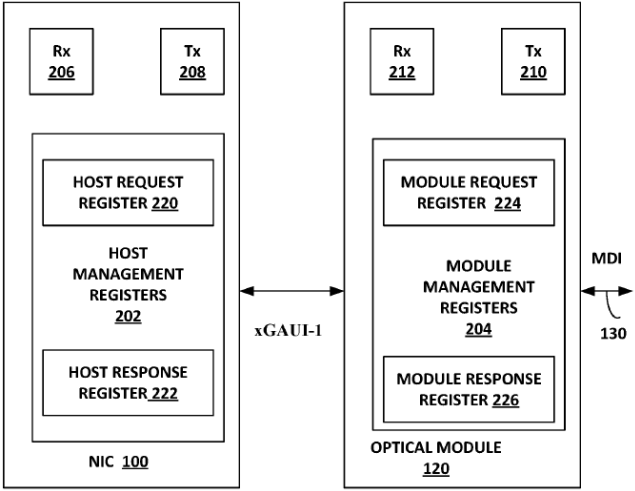
	 FIG. 2
the receiver in the first device is to receive signals from the transmitter of the second device,	- Serial communication between a transmitter and a receiver at very high data rates requires equalization to mitigate frequency dependent signal attenuation. Equalization can be applied at the transmitter (Tx) and/or at the receiver (Rx). Typically, a combination of transmitter and receiver equalization is used. At current rates of 50 Gb/s per lane, equalization is typically implemented in a receiver in the optical module and in a transmitter in the host. Ran Provisional at 2. - Fig. 2 illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface(AUi) Chip-to-Module to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUi) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. Ran Provisional at 7. - Host management registers 202 in the network interface controller 100 include a host request register 220 and a host response register 222. Module management registers 224 in the optical module 120 include a module request register 224 and a module response register 224. The host management registers 202 and module management registers 224 are used as a two-way

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communications channel to perform timing recovery and equalization for a single-lane xGAUI-1 electrical link between the network interface controller 100 and the optical module 120. Ran Provisional at 7.

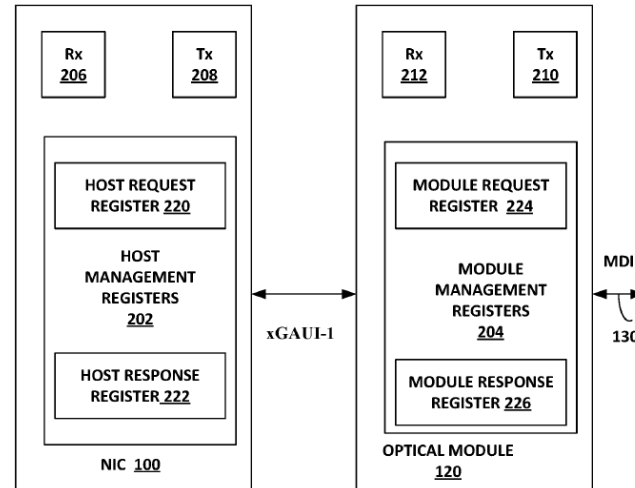


FIG. 2

the first device includes a plurality of management registers,

- Fig. 2 illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface(AUi) Chip-to-Module to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUi) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. Ran Provisional at 7.
- Host management registers 202 in the network interface controller 100 include a host request register 220 and a host response register 222. Module management registers 224 in the optical

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module 120 include a module request register 224 and a module response register 224. The host management registers 202 and module management registers 224 are used as a two-way communications channel to perform timing recovery and equalization for a single-lane xGAUI-1 electrical link between the network interface controller 100 and the optical module 120. Ran Provisional at 7.

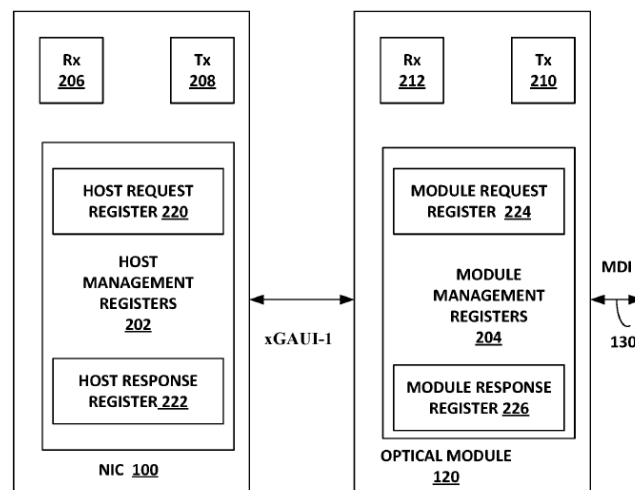


FIG. 2

the second device includes a plurality of management registers, and

- Fig. 2 illustrates a set of management registers in a network interface controller 100 and an optical module 120 for one lane of a multi-lane Attachment Unit Interface(AUi) Chip-to-Module to enable control of equalization in the receiver in the optical module 120 by the network interface controller 100. The multi-lane Attachment Unit Interface (AUi) Chip-to-Module forms a single link between the network interface controller 100 and an optical module 120 by transferring data in parallel over multiple lanes. Ran Provisional at 7.

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- Host management registers 202 in the network interface controller 100 include a host request register 220 and a host response register 222. Module management registers 224 in the optical module 120 include a module request register 224 and a module response register 224. The host management registers 202 and module management registers 224 are used as a two-way communications channel to perform timing recovery and equalization for a single-lane xGAUI-1 electrical link between the network interface controller 100 and the optical module 120. Ran Provisional at 7.

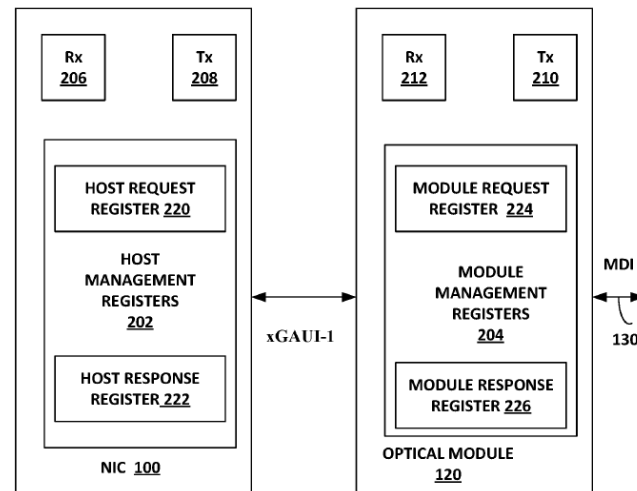


FIG. 2

in response to detection of toggling of a request identifier bit, the management entity is to communicate

- Returning to Fig. 2, module request register 224 is a read-only register that can only be read by a host management entity. The host management entity may be in a device driver in an operating system, logic in a network interface controller or logic in a media access controller. Module request register 224 may include some or all of the fields described in conjunction with request register 300 (Fig. 3). Ran Provisional at 10.

Exhibit C-3

equalization settings from the receiver to the transmitter by a copy of content of a management register of the first device to a management register of the second device in order to select an equalizer tap coefficient of the transmitter independent of modification of another tap coefficient.	• The module request register 224 may also include a one-bit request identifier field which may be assigned to any of the currently reserved bits 306, 310, 302 in the request register 300 (Fig. 3). The request identifier bit in the module request register 224 is toggled (state changed from logical 0 to logical 1 or logical 1 to logical 0) whenever a new request is generated. Ran Provisional at 10. Ran Provisional at 10. • At block 600, a management entity reads module request register 224 in the optical module 120. Processing continues with block 602. Ran Provisional at 12. • At block 602, if the state of a request identifier bit in module request register 224 has toggled (that is, changed from logical 1 to logical 0 or from logical 0 to logical 1) since the last time module request register 224 was read, processing continues with block 604. If the request identifier bit in host request register 220 is the same as the last time host request register 220 was read, processing continues with block 600, to read host request register 220 again. Ran Provisional at 12. • At block 604, the management entity writes the value read from module request register 224 to host request register 220, processing continues with block 606. Ran Provisional at 12. • At block 606, the management entity reads host response register 222 in the host management registers 202. Processing continues with block 608. Ran Provisional at 12. • At block 608, if the state of a response identifier bit in the host response register 222 has toggled (that is, changed from logical 1 to logical 0 or from logical 0 to logical 1), processing continues with block 610. If the response identifier bit in host response register 222 is the same as the last time host response register 222 was read, processing continues with block 606, to read host response register 222 again. Ran Provisional at 12. • At block 610, the value read from host response register 222 is written to module response register 226, processing continues with block 612. Ran Provisional at 12. • Selection of equalization coefficients to configure a communications link between the network interface controller 100 and the optical module 120 may be performed by a management entity with access to host management registers 202 and module management registers 204. Continuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established. Ran Provisional at 13.
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Exhibit C-3

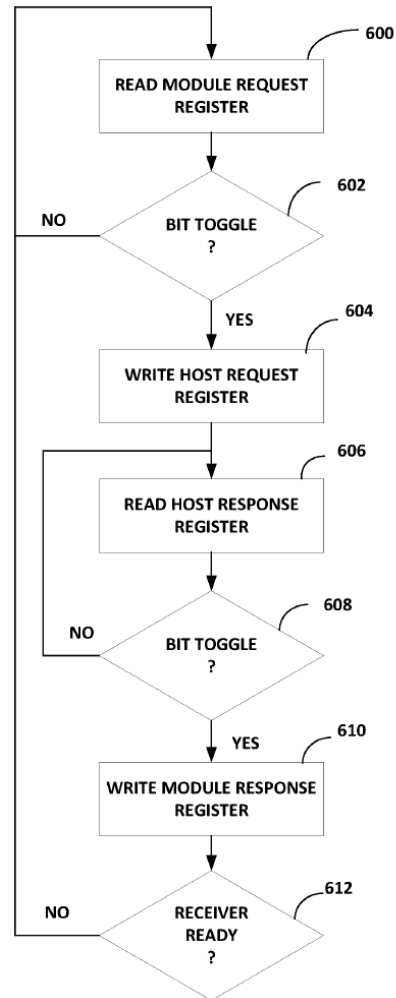


FIG. 6