

Exhibit C-11

Invalidity of U.S. Patent No. 11,032,111 (the “’111 Patent”) in View of David R. Stauffer *et al.*, HIGH SPEED SERDES DEVICES AND APPLICATIONS

HIGH SPEED SERDES DEVICES AND APPLICATIONS by David R. Stauffer *et al.* (“Stauffer”) was published in 2008 by Springer Science+Business Media LLC. Stauffer qualifies as prior art under at least 35 U.S.C. § 102(a)(1) (AIA).

The Administrative Law Judge has not yet construed the claims and therefore the meaning of the terms in the claims has yet to be resolved. The support identified here for limitations of the Asserted Claims of the ’111 Patent is responsive to Complainant’s apparent infringement contentions in its Complaint, which Respondents disagree with. As such, nothing in Respondents’ claim charts should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Respondents’ understanding of the proper scope of the Asserted Claims of the ’111 Patent.

All cross-references should be understood to include material that is cross-referenced within the cross-reference. Where a particular Figure is cited, the citation should be understood to encompass the caption and description of the Figure as well as any text relating to or describing the Figure. Conversely, where particular text referring to a Figure is cited, the citation should be understood to include the Figure as well. Respondents reserve the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Complainant’s infringement and/or domestic industry contentions, and/or information obtained during discovery as the case progresses.

To the extent Complainant alleges that Stauffer does not disclose any particular limitation of the Asserted Claims of the ’111 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the ’111 Patent to modify Stauffer and/or to combine the teachings of Stauffer with other prior art references, including but not limited to the prior art references cited in the Cover Pleading and the relevant section(s) of claim charts for other prior art references for the ’111 Patent in a manner that would have rendered the Asserted Claims invalid as obvious.

Because Complainant has yet to identify any limitation of the Asserted Claims of the ’111 Patent that it contends is not fully disclosed by Stauffer, either alone or in combination with other prior art cited by Respondents, Respondents expressly reserve the right to rebut any such contention, including by identifying additional obviousness combinations, if any such contention is made by Complainant. Respondents further reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Cover Pleading.

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A. INDEPENDENT CLAIM 1

Claim 1	Stauffer
1[pre] A SerDes communications method that comprises, in a transceiver:	To the extent the preamble is limiting, Stauffer discloses and/or renders obvious this limitation. “The interconnect between the transmitter and receiver device (known as the channel) acts as a filter at typical baud rates, and distorts the serial data signal to varying extents. Figure 1.9 illustrates this distortion: The input waveform is a clean digital signal, but the output waveform is significantly distorted. The illustrated frequency response function for the channel is characteristic of a low-pass filter. Signal distortion occurs because the signal baud rate is above the cut-off frequency for this filter.” Stauffer, 10. “Signal integrity concerns frequently dictate that the data signal be equalized at the transmitter and/or receiver in order to counter the effects of the channel and decode the signal properly. Many variations on filter architectures are possible, all of which accomplish this. Fig. 1.10 illustrates the addition of an equalizer at the transmitter with a transfer function that is roughly the inverse of the channel’s frequency response. This equalizer distorts the signal at the transmitter output such that the resulting signal at the receiver input is a clean waveform.” Stauffer, 10. “Most Serdes transmitter implementations include a FFE. The block diagram for a three-tap FFE is shown in Fig. 1.11. The serial data signal is delayed by several flip-flops which implement the taps for the filter. Each tap is multiplied by a tap weight value (also called a filter coefficient), and the results are summed and driven to the serial data output. FFE operation is described further in Sect. 3.2.1.” Stauffer, 10.

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	“The number of FFE taps on the filter, the spacing of these taps relative to the baud rate, and the granularity of these tap weight values vary based on implementation. The terminology preemphasis or deemphasis refer to the FFE architecture, and indicate whether the data signal amplitude is increased or decreased as compared to the nonemphasized value by the FFE tap. The terminology precursor taps and postcursor taps refer to whether the FFE filter taps operate on an advanced or delayed signal (respectively) relative to the $t = 0$ tap. Baud-spaced taps are defined as taps where the delay from one filter tap to the adjacent tap is one-bit time interval; fractional spacing of the taps is also possible.” Stauffer, 10. “The FFE tap weights are selected to generate a filter with the inverse transfer function of the channel transfer function. Various algorithms exist for determining optimal FFE coefficient values; some select filter coefficients to maximize signal amplitude at the receiver, while others optimize eye width (i.e., minimizing jitter). More complex algorithms may search for an optimal trade-off between amplitude and jitter in order to optimize a more complex parameter (such as projected BER). FFE tap weights are determined for many applications by design and coded as fixed values within system software, however, there are some applications where FFE tap weights are adjusted dynamically by the protocol based on signal characteristics at the receiver.” Stauffer, 10-11.

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	Typical Backplane Application Driver → PCB, connectors, cables → Receiver Input Bits → [Distorted] Output Waveform Frequency Response: Attenuation (dB) vs Frequency (Hz) from 10^3 to 10^{10} Hz. Fig. 1.9 Signal distortion for a typical channel application Driver with integrated FFE → PCB, connectors, cables → Receiver Preemphasis Example Using Integrated FFE → [Equalized] Waveform Fig. 1.10 Typical channel application with equalization at the transmitter

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Claim 1	Stauffer
	Fig. 1.11 Three-tap feed forward equalizer operation Fig. 1.12 Typical channel application with equalization at the receiver

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	Fig. 1.13 Receiver frequency response for peaking amplifier settings Fig. 1.14 Decision feedback equalizer architecture

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	To the extent that this preamble is not disclosed, either explicitly or inherently, by Stauffer, this preamble is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[a] selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;	Stauffer discloses and/or renders obvious this limitation. <i>See support provided above for claim 1[pre].</i> “Many of the TX slice parameter control registers are not effective immediately after being written. Application of register values to the analog circuits is controlled by writing the Apply Load bit in the Transmit Coefficient Control Register. This allows the FFE and power level configuration to be completely loaded in the individual registers and then simultaneously applied to the analog circuits. For the HSS EX10, the values loaded into the Transmit TapX Coefficient Registers, the Transmit Power Register, the Transmit Polarity Register, and the FFE Mode Select field of the Transmit Driver Mode Control Register are not applied to the analog circuits until the Apply Load bit is pulsed. The read-back value of these registers reflects the value being applied to the analog circuits. If these registers are written and then read before the Apply Load bit is pulsed, the old values are read. (The value of the Slow Slew Control field of the Transmit Driver Mode Control Register is applied to the analog circuits immediately, and is not gated by the Apply Load bit.)” Stauffer, 59.

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	“For cores which do not contain internal registers, filter coefficients may be set using input control pins. Sequencing updated values onto these pins is the responsibility of the chip designer.” Stauffer, 59. “FFE coefficient values are not intended to be changed dynamically while data is being transmitted (except as part of a speed negotiation or link optimization process). Significant changes to the TX slice configuration can cause loss of data at the receiver until such time as the receiver adapts to the new waveform characteristics.” Stauffer, 59. “Higher speed protocol standards sometimes support negotiation of transmitter FFE settings based on characteristics of the signal at the receiver. IEEE 802.3ap Backplane Ethernet is an example of such an application. Implementations of such applications must update FFE coefficients in response to a full duplex training protocol by reading and writing the corresponding registers.” Stauffer, 59. “The training protocol used for Backplane Ethernet is introduced in Sect. 5.3.5.1. Some cores provide register control signals to more easily implement the actions defined by this protocol, which include incrementing/decrementing coefficient values. Such features are not defined for the HSS EX10 core.” Stauffer, 59. “The tap ranges and resolutions for the HSS EX10 FFE circuit were described in Table 2.12, and this table is repeated in Table 3.1. In a nonequalized case, the main tap provides 100% of the driver output amplitude. As shown in the table, this limit corresponds to the maximum current that this tap can provide. Limits for other taps were chosen after empirical studies of equalization solutions for a variety of channel

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	design examples.” Stauffer, 109. Table 3.1 Transmitter FFE summary <table><tr><td><i>Tap coefficient #</i></td><td><i>0</i></td><td><i>1</i></td><td><i>2</i></td></tr><tr><td>Max current (mA)</td><td>7.5</td><td>30</td><td>15</td></tr><tr><td>Relative max (%)</td><td>25</td><td>100</td><td>50</td></tr><tr><td>DAC resolution (bits)</td><td>6</td><td>8</td><td>7</td></tr><tr><td>Tap allocation</td><td>Precursor</td><td>Main tap</td><td>Postcursor</td></tr></table> “Figure 3.9 illustrates a simplified generic FFE example. A simplified halfrate FFE architecture is shown in Fig. 3.9a, and is representative of the circuit in Fig. 3.8. This example explores a two-tap FFE case (i.e., FFE Mode Select set to “FFE2” in the Transmit Driver Mode Control Register as described in Table 2.6). The cursor and postcursor taps are set at +0.8 and – 0.2, respectively. Figure 3.9b illustrates the various signal waveforms and the resulting FFE output. The Serial Data or x(t) signal in Fig. 3.9b is the serial data input to the FFE circuit. The x(t–T) and –x(t–T) signals are noninverted and inverted polarities of the original signal delayed by one-bit time. Finally, the Tx OUT or y(t) signal is the Tx Output waveform, and can be expressed by the following mathematical summation: Tx Out = y(t) = 0.8 x(t) – 0.2 x(t – T), (3.1) where the signals y(t), x(t), and x(t–T) were defined above, and T is one-bit time (or 1 UI).” Stauffer, 109.	<i>Tap coefficient #</i>	<i>0</i>	<i>1</i>	<i>2</i>	Max current (mA)	7.5	30	15	Relative max (%)	25	100	50	DAC resolution (bits)	6	8	7	Tap allocation	Precursor	Main tap	Postcursor
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	a) b) Serial Data $x(t)$ $x(t-T)$ $-x(t-T)$ Tx OUT $y(t)$ where $T = 1$ bit time or UI Fig. 3.9 Example of feed forward equalizer operation “This example clearly illustrates how postcursor equalization affects the output waveform. Each time the input waveform transitions up or down, the instantaneous output increases in amplitude to a peak value of unity (the sum of $0.8 + 0.2$), producing a larger amplitude for one-bit time. The resulting waveform has

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	increased high frequency content, which compensates for the high frequency loss of the channel.” Stauffer, 110. “Figure 5.25 and 5.26 illustrate block diagrams of the datapath of the transmitter and receiver, respectively. These block diagrams show the relationship between the 8B/10B encoder/decoder, CRC generation/checking, and scrambling/descrambling functions. Scrambling is only relevant to 8GFC serial variants; lower baud rate serial variants are not scrambled. (The 10GFC variant is discussed later.)” Stauffer, 225. “Data words in the transmit datapath of the link layer shown in Fig. 5.25 are applied to the CRC generator, and the remainder is multiplexed onto the datapath at the end of the frame. Data is scrambled (for 8GFC only), and then multiplexed with Ordered Set primitives that are transmitted between frames or as SOF/EOF delimiters. Note that primitives are not scrambled and are not part of the CRC calculation. The physical layer 8B/10B encodes the data, and then uses an HSS core to transmit the data serially. Ordered Sets are aligned on word boundaries and defined such that only the first byte can be a Kxx.y control symbol (denoted prior to encoding in the figure by the Z bit) in the 8B/10B code.” Stauffer, 225. “Bytes (or the corresponding 8B/10B symbols) of each word are transmitted in the order of left to right. Symbols of the 8B/10B code are specified as 10-bit encoded values with bits labeled a through j. Bits within each symbol are transmitted serially in order starting with bit a and ending with bit j.” Stauffer, 225.

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	“The physical layer of the receive datapath shown in Fig. 5.26 deserializes the data and decodes the 8B/10B symbols. Primitives are processed directly in the link layer. Data is descrambled (for 8GFC only) and propagated to downstream logic. CRC is calculated for the unscrambled data and the result is compared to the transmitted value.” Stauffer, 225. “The CRC Generator polynomial used by Fibre Channel is the same as was defined in Sect. 4.2.3.3. The CRC calculation is performed in a manner that is equivalent to a serial CRC calculation using the following byte/bit order: The byte order is the same as the order in which bytes (or corresponding symbols) are transmitted. The bit order within each byte is least significant bit through most significant bit. The CRC remainder is calculated across all words of the frame between the Start Of Frame (SOF) delimiter and the CRC field.” Stauffer, 225.

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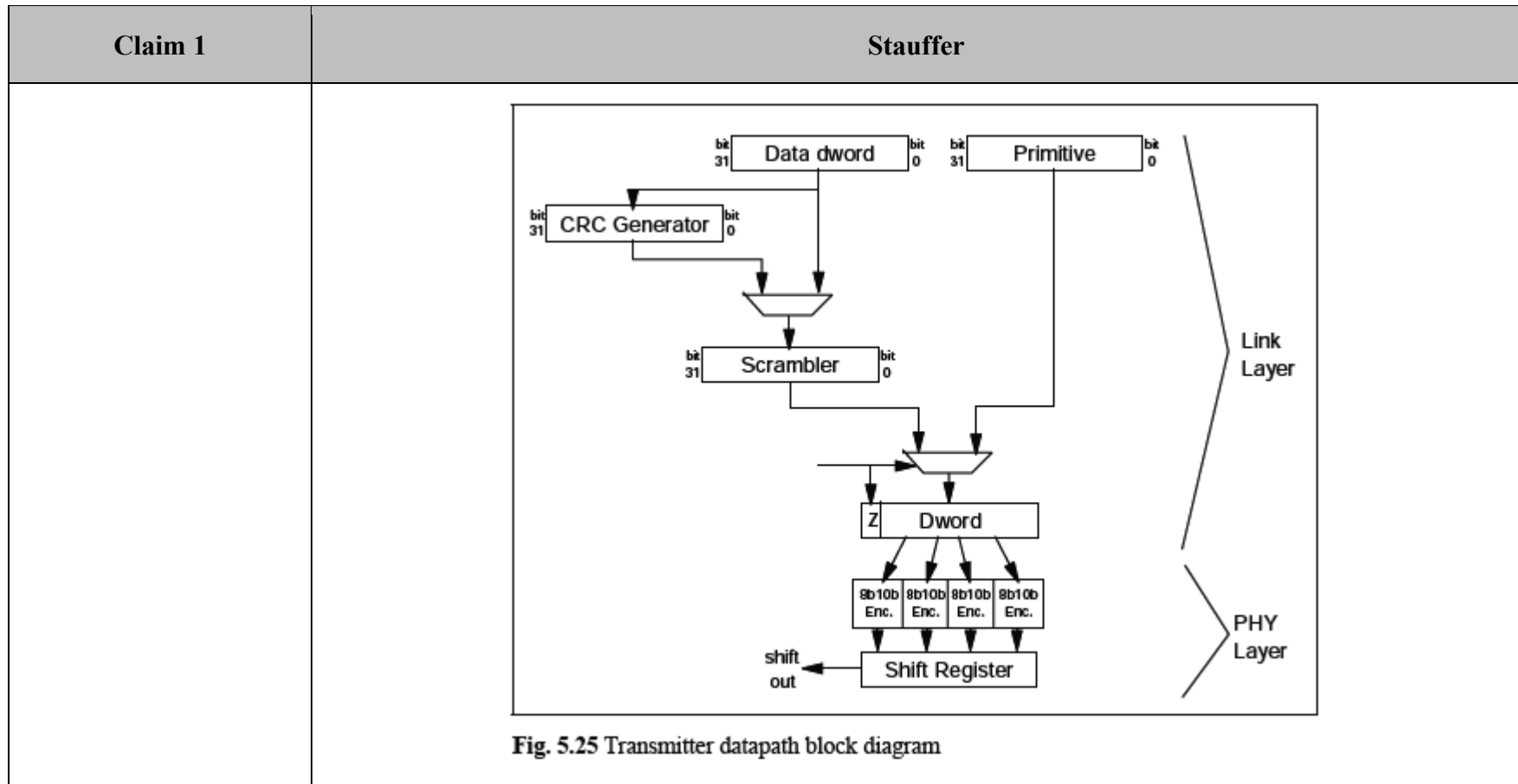


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	<pre> graph TD subgraph PHY_Layer [PHY Layer] SR[Shift Register] -- shift in --> SR SR --> D1[8b10b Dec.] SR --> D2[8b10b Dec.] SR --> D3[8b10b Dec.] SR --> D4[8b10b Dec.] D1 --> Dword[Z Dword] D2 --> Dword D3 --> Dword D4 --> Dword end subgraph Link_Layer [Link Layer] Dword --> Descrambler[Descrambler] Descrambler -- bit 31 to bit 0 --> CRC[CRC Generator] Descrambler -- bit 31 to bit 0 --> Data[Data dword] Descrambler -- bit 31 to bit 0 --> Primitive[Primitive] CRC -- bit 31 to bit 0 --> Compare[Dword Compare] end </pre> Fig. 5.26 Receiver datapath block diagram “The motivation for scrambling 8GFC serial variants is to avoid CDR biasing issues impacting the link jitter budget, as was discussed in Chap. 1. The 8GFC serial variants use a self-synchronizing scrambler with the following polynomial: $G(x) = x^{58} + x^{39} + 1.$ Stauffer, 227.

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	“The scrambler (and descrambler) are reset at the start of every frame to avoid any error propagation from one frame to the next. (Otherwise a received bit error at the end of one frame could corrupt the next frame as well.) By using a self-synchronizing scrambler, any variation in the content of the frame causes subsequent bytes to be scrambled differently. The SEQ_CNT field of the header is always guaranteed to change from frame to frame, even for a frame retransmission, and therefore the retransmitted frame is scrambled differently each time.” Stauffer, 227. “Note that the bit order for scrambling is not the same as the bit order defined for CRC calculation. Scrambling is performed equivalent to serially scrambling a bit stream consisting of each 32-bit word in the bit order of most significant bit to least significant bit. This convention simplifies implementation assuming a 32-bit datapath.” Stauffer, 227. “Fig. 7.16 illustrates two possible measurement points for characterization of transmitter devices. The transmitter devices to be tested are identified as the device under test (DUT) blocks.” Stauffer, 328. “One method of performing such measurements would be to connect test equipment directly to the output of a transmitter. The test equipment provides an ideal load for the transmitter, with no intervening channel to distort the signal. Some protocol standards do specify the transmitter output pin as a compliance point, and in such cases compliance measurements are performed directly at the transmitter output.” Stauffer, 328.

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	The diagram shows a lab setup for HSS characterization. A large box contains two main sections. On the left, a box labeled 'Pattern Recognition Equipment' is connected to a box labeled 'Clock Generation Pattern Generation Equipment'. This latter box is connected to a box labeled 'Clock Generation and MUXing' which is part of an 'Evaluation Board'. The 'Evaluation Board' also contains a box labeled 'HSS Test Chip'. A 'Host (personal computer)' is connected to the 'Evaluation Board' via a bidirectional arrow. The 'Host' is also connected to the 'Pattern Recognition Equipment' via a long arrow. Fig. 7.15 HSS characterization and qualification lab setup The diagram shows two test configurations for a transmitter. In the top configuration, a box labeled 'DUT' is connected to a box labeled 'Test Equipment'. To the right of the 'Test Equipment' box, text reads: 'Test Equipment measurements on transmitter output (ideal load)'. In the bottom configuration, a box labeled 'DUT' is connected to a box labeled 'Test Equipment' by a thick arrow. To the right of the 'Test Equipment' box, text reads: 'Test Equipment measurements at far end of a specified compliance channel'. Fig. 7.16 Lab characterization conditions for the transmitter

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	“Note, however, that in a real system the channel does distort the signal. This distortion, and associated signal integrity topics, are discussed in Chap. 8. HSS transmitters often contain an FFE circuit which is capable of altering the transmitted signal. The FFE emphasizes the transmitted signal to cancel the distortion effects of the channel, and thereby provide good signal quality at the receiver input. Measurements performed at the transmitter output must be performed using defined FFE settings, and provide no guidance as to the signal quality at the receiver.” Stauffer, 329. “An alternative used by many protocol standards is to define the characteristics of a compliance channel, and to perform transmitter characterization by measuring the transmitted signal at the far-end of this channel. This is also shown in Fig. 7.16, with the DUT driving a channel, and test equipment connected to the far-end of the channel. In this case, the FFE is expected to be set based on the channel characteristics to obtain the best possible signal quality at the test point.” Stauffer, 329. “HSS design teams perform characterization testing of their transmitter devices using both methods. Specifications for jitter and amplitude of the transmitter output require measurements directly at this point. Characterization of the FFE and model to hardware correlation of hardware to various signal integrity models requires measurements at the far-end of known channels. Furthermore, compliance testing for various protocol standards requires measurements be taken consistent with the test methods and conditions defined by the standards document.” Stauffer, 329. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the

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	Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[b] updating the initial pre-equalizer coefficient values during a training phase; and	Stauffer discloses and/or renders obvious this limitation. “Figure 5.25 and 5.26 illustrate block diagrams of the datapath of the transmitter and receiver, respectively. These block diagrams show the relationship between the 8B/10B encoder/decoder, CRC generation/checking, and scrambling/descrambling functions. Scrambling is only relevant to 8GFC serial variants; lower baud rate serial variants are not scrambled. (The 10GFC variant is discussed later.)” Stauffer, 225. “Data words in the transmit datapath of the link layer shown in Fig. 5.25 are applied to the CRC generator, and the remainder is multiplexed onto the datapath at the end of the frame. Data is scrambled (for 8GFC only), and then multiplexed with Ordered Set primitives that are transmitted between frames or as SOF/EOF delimiters. Note that primitives are not scrambled and are not part of the CRC calculation. The physical layer 8B/10B encodes the data, and then uses an HSS core to transmit the data serially. Ordered Sets are aligned on word boundaries and defined such that only the first byte can be a Kxx.y control symbol (denoted prior to encoding in the figure by the Z bit) in the 8B/10B code.” Stauffer, 225. “Bytes (or the corresponding 8B/10B symbols) of each word are transmitted in the order of left to right. Symbols of the 8B/10B code are specified as 10-bit encoded values with bits labeled a through j. Bits within each symbol are transmitted serially in order starting with bit a and ending with bit j.” Stauffer, 225.

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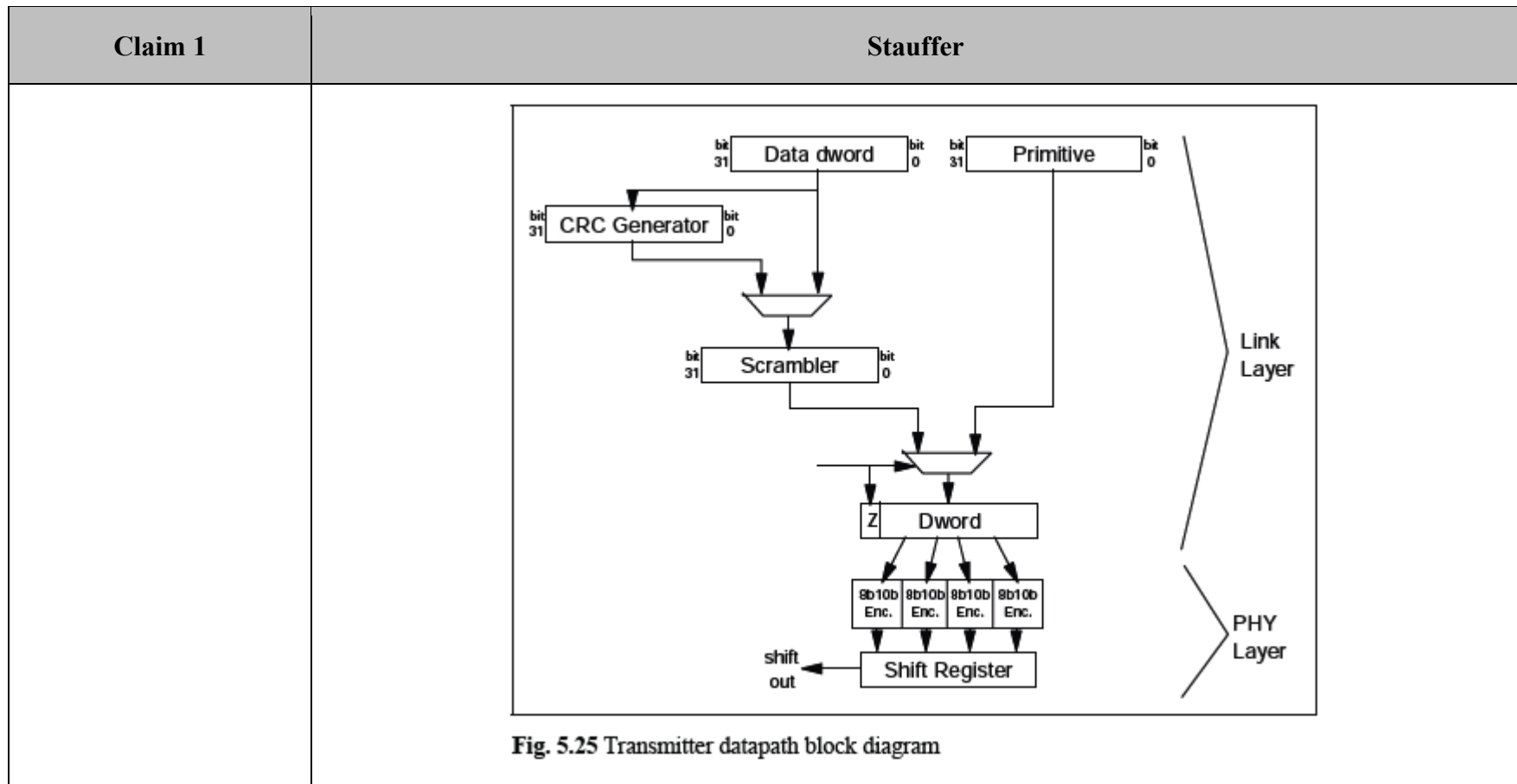


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	“The scrambler (and descrambler) are reset at the start of every frame to avoid any error propagation from one frame to the next. (Otherwise a received bit error at the end of one frame could corrupt the next frame as well.) By using a self-synchronizing scrambler, any variation in the content of the frame causes subsequent bytes to be scrambled differently. The SEQ_CNT field of the header is always guaranteed to change from frame to frame, even for a frame retransmission, and therefore the retransmitted frame is scrambled differently each time.” Stauffer, 227. “Note that the bit order for scrambling is not the same as the bit order defined for CRC calculation. Scrambling is performed equivalent to serially scrambling a bit stream consisting of each 32-bit word in the bit order of most significant bit to least significant bit. This convention simplifies implementation assuming a 32-bit datapath.” Stauffer, 227. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[c] using the updated pre-equalizer coefficient values to convey a transmit data stream.	Stauffer discloses and/or renders obvious this limitation. “Figure 5.25 and 5.26 illustrate block diagrams of the datapath of the transmitter and receiver, respectively. These block diagrams show the relationship between the 8B/10B encoder/decoder, CRC

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	generation/checking, and scrambling/descrambling functions. Scrambling is only relevant to 8GFC serial variants; lower baud rate serial variants are not scrambled. (The 10GFC variant is discussed later.)” Stauffer, 225. “Data words in the transmit datapath of the link layer shown in Fig. 5.25 are applied to the CRC generator, and the remainder is multiplexed onto the datapath at the end of the frame. Data is scrambled (for 8GFC only), and then multiplexed with Ordered Set primitives that are transmitted between frames or as SOF/EOF delimiters. Note that primitives are not scrambled and are not part of the CRC calculation. The physical layer 8B/10B encodes the data, and then uses an HSS core to transmit the data serially. Ordered Sets are aligned on word boundaries and defined such that only the first byte can be a Kxx.y control symbol (denoted prior to encoding in the figure by the Z bit) in the 8B/10B code.” Stauffer, 225. “Bytes (or the corresponding 8B/10B symbols) of each word are transmitted in the order of left to right. Symbols of the 8B/10B code are specified as 10-bit encoded values with bits labeled a through j. Bits within each symbol are transmitted serially in order starting with bit a and ending with bit j.” Stauffer, 225. “The physical layer of the receive datapath shown in Fig. 5.26 deserializes the data and decodes the 8B/10B symbols. Primitives are processed directly in the link layer. Data is descrambled (for 8GFC only) and propagated to downstream logic. CRC is calculated for the unscrambled data and the result is compared to the transmitted value.” Stauffer, 225.

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B. DEPENDENT CLAIM 2

Claim 2	Stauffer
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Claim 2	Stauffer
2. The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.	Stauffer discloses and/or renders obvious this limitation. <i>See support provided above for claim 1.</i> “The Serdes core requires an internal clock running at either the baud or halfbaud rate depending on the architecture of the driver and receiver stages. Rather than distribute a high-speed clock throughout the chip, a lower frequency reference clock is distributed within the chip, and a PLL is used in the Serdes to multiply this clock to the appropriate frequency. A given Serdes implementation may contain multiple instances of transmitter and/or receiver channels. In such cases, it is common for a single PLL in the core to generate clocks for all channels within the core.” Stauffer, 19. “The off-chip clock source often operates at an even lower frequency than the on-chip reference clock. An additional PLL may be used in the chip to multiply the frequency of the off-chip reference clock to meet the desired onchip reference clock frequency. Because the frequency of the on-chip reference clock is usually higher than the off-chip reference clock (but less than the internal clock in the Serdes core) the PLL which produces this clock is sometimes called an intermediate frequency (IF) PLL.” Stauffer, 19. “An example of clock distribution using such an IF PLL is shown in Fig. 1.19. An IF PLL is used to multiply the 200-MHz clock from an off-chip oscillator by four. The resulting 800-MHz reference clock is

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Claim 2	Stauffer
	distributed onchip into various Serdes cores. These Serdes cores each contain a PLL which additionally steps up the frequency of the 800-MHz reference clock to the desired baud rate.” Stauffer, 19. “The channel is defined as the electrical path between the transmitter and the receiver, including printed circuit board traces, vias, cables, connectors, decoupling capacitors, etc. The channel may traverse the printed circuit board between two chips on the same card, or may traverse a system backplane connecting two printed circuit boards.” Stauffer, 19. “At frequencies of interest, the printed circuit board is not a perfect connection. Major channel impairments include insertion loss, reflections, and crosstalk. Channel frequency response, including these impairments, is typically measured using a vector network analyzer (VNA), and captured in a Scattering Parameter matrix format (commonly called S-Parameters) as is described in “Channel Response” under Sect. 8.4.1.2 in Chap. 8. Each of these impairments impacts the BER of the link. Interface standards typically require link BER performance in the range of 10^{-12} to 10^{-15}.” Stauffer, 19. “The equalization scheme used by Serdes devices must compensate for the channel loss and other impairments in order to achieve the desired BER. A common figure of merit is based on the evaluation of the insertion loss of the channel at the Nyquist rate (two times the highest fundamental frequency of the signal). From this metric, a qualitative assessment as to the difficulty of signal propagation (and the necessary complexity of the equalization scheme) can be made.” Stauffer, 19-20.

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Claim 2	Stauffer
	“The XGXS PCS sublayer performs 8B/10B encoding and decoding of MAC frames. Each byte of data maps to a corresponding 10-bit symbol. In addition, the XGMII control characters in Table 5.12, with the exception of the Idle character, directly map to corresponding 10-bit symbols. This mapping is shown in Table 5.12 using the symbol nomenclature for 8B/10B codes. (The 8B/10B block code was described in Sect. 4.2.2.1.)” Stauffer, 207. “XGMII Idles are randomly converted to one of the following 10-bit codes: Sync (K28.5), Skip (K28.0), or Align (K28.3). A LFSR is used to randomly either generate Sync or Skip symbols. Align symbols are inserted at randomized intervals in the range of 16–31 symbols, with this interval also determined by a LFSR. The same symbol is transmitted on all lanes.” Stauffer, 207. “Align symbols are used by the receive PCS logic to perform deskew across all lanes of the interface such that the XGMII RXD[31:0] output is aligned to a common clock domain. The Align symbol is unique and does not otherwise occur in the protocol. Since it is transmitted on all lanes simultaneously, and is only transmitted every 16–31 symbols, the lanes can be deskewed by aligning the occurrence of this symbol.” Stauffer, 207. “Skip symbols are used by the receive PCS logic to adjust for frequency differences between the recovered receive clock and the local XGMII clock. Skip symbols are inserted or dropped as needed.” Stauffer, 207. “The Sequence symbol (K28.4) is used on lane 0, in conjunction with Dxx.y symbols on the other lanes, to

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Claim 2	Stauffer
	convey management information. Such information is inserted by the MAC layer between frames in place of Idles, and is conveyed through the XGXS accordingly.” Stauffer, 207. “The 10-Gb Serial Electrical Interface (XFI) was developed as part of the 10-Gigabit Small Form Factor Pluggable (XFP) Multi Source Agreement (MSA). This MSA was developed by a consortium of optics module vendors who agreed to source optics modules meeting the XFP requirements. The XFI is a 10-Gbps serial electrical interface for communications between the XFP module and a SONET framer chip, or an Ethernet PCS/PMA layer. The PCS and PMA sublayers defined in clauses 49 and 51, respectively, define the necessary functions to interface between XGMII and XFI, and are used with all 10-Gb Ethernet serial variants (including backplane applications using the PMD defined in clause 72). Although the XFI acronym does not appear anywhere in the IEEE 802.3 standard, for historical reasons implementations of clause 49 and 51 are commonly called XFI.” Stauffer, 207-08. “The XFI PCS encodes and serializes the XGMII transmit data (TXD/TXC signals) for transmission on XFI. Each XGMII lane is 64B/66B encoded, scrambled, serialized, and transmitted at a baud rate of 10.3125 Gbps. XFI serial data signals received by the XFI PCS are deserialized, descrambled, 64B/66B decoded, and then driven to the MAC or PHY on the XGMII receive data (RXD/RXC signals). XFI is a full duplex interface consisting of one transmit and one receive serial data signals.” Stauffer, 208. “An optional 16-bit bus is defined to interface between the PCS sublayer and the PMA sublayer. While this is the reference interface between the XFI PCS and the HSS core implementing the PMA sublayer as defined by clause 49, it does require data to be transferred on the parallel bus of the HSS core at 644.53 Mtransfers per second. Implementations may choose HSS core options which utilize more bits of parallel

Exhibit C-11

Claim 2	Stauffer
	data at a slower transfer rate. (Available IBM cores use a 32-bit interface.) The definition of this interface has significance for two reasons: • The 66-bit code word blocks produced by 64B/66B encoding of the XGMII data are not an integer multiple of the width of the parallel data bus on most HSS cores. Data must be steered from cycle to cycle by “gearbox” logic in order to map the 66-bit blocks onto the 16-bit (or 2-bit) parallel data bus of the HSS core. • 10GBASE-W Wide Area Network (WAN) variants are intended to interoperate with other network nodes on a SONET/SDH network. These variants define a WAN Interface Sublayer (WIS) in clause 50 which maps the Ethernet packets into a SONET SPE, and then wraps this data with SONET/SDH overhead bytes with the level of support defined in clause 50. WIS is sandwiched between the PCS and PMA sublayers for 10GBASE-W variants.” Stauffer, 208. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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C. DEPENDENT CLAIM 3

Claim 3	Stauffer
3. The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.	Stauffer discloses and/or renders obvious this limitation. “Parameters regarding “Input Differential Voltage” are informative specifications. The receiver must receive any signal generated by a compliant transmitter driven through a compliant channel. For CEI variants with receiver reference models using DFEs, the signal amplitude at the receiver may approach zero for higher spectral components of the data.” Stauffer, 196. “Jitter parameters are also informative specifications with respect to the receiver. The individual CEI clauses provide informative values for jitter at the receiver which may be used as a guideline. The requirement is that the receiver must receive any signal generated by a compliant transmitter and driven through a compliant channel.” Stauffer, 196. “All CEI variants include normative specifications for channel compliance. Channel compliance is determined by frequency domain analysis of the channel using the mathematical methods specified in the implementation agreement. This analysis is performed as follows: • A reference transmitter is assumed which incorporates certain assumptions regarding launch amplitude, jitter, equalizer capabilities, etc. • The channel response is measured and 4-port S-parameters are generated for the channel. • A reference receiver is assumed which incorporates certain assumptions regarding return loss, equalizer capabilities, etc. In some cases, more than one reference receiver is specified; the channel must work with all specified reference receivers. • Statistical signal integrity analysis is performed with the above components to determine the width and height of the virtual eye at the output of the receiver equalizer. If there exists a set of filter coefficients for the transmitter and the receiver which are legal, and which produce a virtual eye

Exhibit C-11

Claim 3	Stauffer
	that is of sufficient width and height for the target bit error rate (BER), then the channel is compliant.” Stauffer, 196. “The training frame is a fixed length frame containing the following fields: • Frame Marker. A four byte unique marker pattern denoting the start of the training frame. The marker pattern is “FFFF0000” hexadecimal. This marker is transmitted at 10.3125 Gbps. • Coefficient Update. A 16-bit coefficient update field which allows the PMD to request changes to the FFE coefficients being used by the PMD at the other end of the link. This 16-bit coefficient field is transmitted using Manchester coding at a baud rate which is one-eighth of the normal 10.3125 Gbps baud rate. Transmission of this 16-bit field is the equivalent of transmitting 16 bytes at 10.3125 Gbps. • Status Report. A 16-bit status field which indicates whether the PMD has finished its training process, as well as the status of any requested FFE coefficient updates. This 16-bit coefficient field is transmitted using Manchester coding at a baud rate which is one-eighth of the normal 10.3125 Gbps baud rate. Transmission of this 16-bit field is the equivalent of transmitting 16 bytes at 10.3125 Gbps. • Training Pattern. Pseudorandom data generated with the polynomial: $G(x) = 1 + x^9 + x^{11}$ This field is 512 bytes in length (4,094 bits PRBS bits followed by two zero bits), transmitted at 10.3125 Gbps.” Stauffer, 214. “The purpose of using low-speed Manchester encoding for the Coefficient Update and Status Report fields is to ensure reliable information is communicated even when the link performance is not optimized. These fields can be implemented by transmitting the parallel data byte “00000000” or “11111111” to represent a Manchester encoded “0” bit, and transmitting the parallel data byte “00001111” or “11110000” to represent a Manchester encoded “1” bit. (The byte pattern used to denote a Manchester encoded “0” or “1” is selected to ensure that a transition always occurs between bits.)” Stauffer, 214.

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Claim 3	Stauffer
	“The Coefficient Update field contains the following subfields: • Preset. Forces all FFE coefficients to be set to a state where equalization is turned off (i.e., coefficients for the main FFE tap is set to its maximum value, and coefficients for precursor and postcursor taps are set to zero). • Initialize. Forces FFE to be turned on and coefficients to be set to predefined initialization values. • Coefficient (+1) Update. Directs that the postcursor FFE coefficient shall be incremented, decremented, or held at current value. • Coefficient (0) Update. Directs that the main FFE coefficient shall be incremented, decremented, or held at current value. • Coefficient (-1) Update. Directs that the precursor FFE coefficient shall be incremented, decremented, or held at current value. Update requests to increment or decrement coefficients should only be sent if the received Status Report field corresponding to the coefficient indicates the coefficient is in not updated state. The Status Report field contains the following subfields: • Receiver Ready. Indicates that reporting node has finished training its receiver and is ready to receive data. • Coefficient (+1) Status. Reports that the postcursor FFE coefficient is not updated, is updated, is at maximum value, or is at minimum value. The PMD initially reports all coefficient status as not updated. After receiving a Coefficient Update request to update the coefficient, the PMD updates the coefficient and then reports either updated, maximum, or minimum status. After receiving a Coefficient Update request to hold the previous value, the PMD returns status to not updated. • Coefficient (0) Status. Reports that the main FFE coefficient is not updated, is updated, is at maximum value, or is at minimum value. Status transitions are similar to the description for the postcursor FFE coefficient. • Coefficient (-1) Status. Reports that the precursor FFE coefficient is not updated, is updated, is at maximum value, or is at minimum value. Status transitions are similar to the description for the postcursor FFE coefficient.” Stauffer, 214-15. “The coefficient status and coefficient update fields associated with each FFE coefficient operate according to a simple two-way handshake as described above. Each PMD assesses the quality of the received signal (through analysis of the training pattern), and then instructs its partner node to update FFE coefficients in an attempt to improve the quality of the signal.” Stauffer, 215.

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Claim 3	Stauffer
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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D. DEPENDENT CLAIM 4

Claim 4	Stauffer
4. The method of claim 1, wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.	Stauffer discloses and/or renders obvious this limitation. “Another consideration of Receiver Slice usage is the bit order in which bits of the parallel data bus are serially received. For the HSS EX10 core, the first bit received is always steered to bit 0 of the RXxD bus. The user must be cautious that this is consistent with the interface standard being implemented. If necessary the datapath connections to the RXxD inputs must be rearranged to obtain the desired bit order.” Stauffer, 70. “Receive data alignment may be adjusted through the use of the RXxDATASYNC control input, and may be independently adjusted on each receiver slice. When the RXxDATASYNC signal transitions from a “0” to a “1,” the deserializer within the receive logic ignores the most recent serial input and holds the contents of the deserializer for one-bit clock cycle. The RXxDATASYNC operation has the effect of changing the deserializer alignment by one-bit position.” Stauffer, 70. “The RXxDATASYNC operation also has the effect of stretching the corresponding RXxDCLK cycle. This behavior is dependent on the rate mode selected. In full-and half-rate modes, the RXxDCLK is stretched 2 UI after every RXxDATASYNC operation. In quarter-and eight-rate modes, the RXxDCLK is stretched 1 UI after every RXxDATASYNC operation. Because the cycle is always stretched, the minimum pulse width of the RXxDCLK signal is never reduced. Figure 2.9 illustrates the timing requirements for the RXxDATASYNC input.” Stauffer, 70.

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Claim 4	Stauffer															
	“In full-rate and half-rate modes the HSS EX10 receiver operates in one of three equalization modes; non-DFE, DFE3, or DFE5. In quarter-rate and eighth-rate modes only non-DFE mode is supported. In non-DFE mode, the received input signal is processed through the variable gain amplifier (VGA) then captured in the front end logic and deserialized. In DFE3 and DFE5 modes, the deserialized samples are processed using DFE algorithms that automatically adjust the receiver threshold to better compensate for severe pattern-dependent distortions in the channel. These modes are selected using by the DFE/non-DFE Mode Select bits in the Receive Configuration Mode Register as shown in Table 2.17.” Stauffer, 70. Table 2.17 DFE/non-DFE mode select <table><tr><th>Receiver mode</th><th colspan="2">DFE/non-DFE mode selector bits of “Receive Configuration Mode Register” for Port x</th></tr><tr><td>DFE5</td><td>0</td><td>0</td></tr><tr><td>DFE3</td><td>0</td><td>1</td></tr><tr><td>non-DFE</td><td>1</td><td>0</td></tr><tr><td>non-DFE (default)</td><td>1</td><td>1</td></tr></table> “DFE5 and DFE3 modes use 5 and 3 filter taps, respectively for feedback. A DFE-n mode makes decisions regarding whether a bit is “1” or “0” based on the history of the last n bits received. DFE5 provides maximum performance in terms of BER, while DFE3 may be used in cases where signal degradation is not as severe. The non-DFE mode uses a fixed threshold receiver for cases where signal degradation is small enough not to require further equalization. The VGA amplifier is used in all modes of operation.” Stauffer, 71. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation	Receiver mode	DFE/non-DFE mode selector bits of “Receive Configuration Mode Register” for Port x		DFE5	0	0	DFE3	0	1	non-DFE	1	0	non-DFE (default)	1	1
Receiver mode	DFE/non-DFE mode selector bits of “Receive Configuration Mode Register” for Port x															
DFE5	0	0														
DFE3	0	1														
non-DFE	1	0														
non-DFE (default)	1	1														

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Claim 4	Stauffer
	is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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E. DEPENDENT CLAIM 5

Claim 5	Stauffer
5. The method of claim 4, wherein the performance characteristic is an error signal energy.	Stauffer discloses and/or renders obvious this limitation. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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F. DEPENDENT CLAIM 6

Claim 6	Stauffer
6. The method of claim 4, wherein the performance characteristic is a bit error rate.	Stauffer discloses and/or renders obvious this limitation. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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G. DEPENDENT CLAIM 7

Claim 7	Stauffer
7. The method of claim 4, further comprising updating the selected register with the updated pre-equalizer coefficient values.	Stauffer discloses and/or renders obvious this limitation. “Many of the TX slice parameter control registers are not effective immediately after being written. Application of register values to the analog circuits is controlled by writing the Apply Load bit in the Transmit Coefficient Control Register. This allows the FFE and power level configuration to be completely loaded in the individual registers and then simultaneously applied to the analog circuits. For the HSS EX10, the values loaded into the Transmit TapX Coefficient Registers, the Transmit Power Register, the Transmit Polarity Register, and the FFE Mode Select field of the Transmit Driver Mode Control Register are not applied to the analog circuits until the Apply Load bit is pulsed. The read-back value of these registers reflects the value being applied to the analog circuits. If these registers are written and then read before the Apply Load bit is pulsed, the old values are read. (The value of the Slow Slew Control field of the Transmit Driver Mode Control Register is applied to the analog circuits immediately, and is not gated by the Apply Load bit.)” Stauffer, 59. “For cores which do not contain internal registers, filter coefficients may be set using input control pins. Sequencing updated values onto these pins is the responsibility of the chip designer.” Stauffer, 59. “FFE coefficient values are not intended to be changed dynamically while data is being transmitted (except as part of a speed negotiation or link optimization process). Significant changes to the TX slice configuration can cause loss of data at the receiver until such time as the receiver adapts to the new waveform characteristics.” Stauffer, 59.

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Claim 7	Stauffer
	“Higher speed protocol standards sometimes support negotiation of transmitter FFE settings based on characteristics of the signal at the receiver. IEEE 802.3ap Backplane Ethernet is an example of such an application. Implementations of such applications must update FFE coefficients in response to a full duplex training protocol by reading and writing the corresponding registers.” Stauffer, 59. “The training protocol used for Backplane Ethernet is introduced in Sect. 5.3.5.1. Some cores provide register control signals to more easily implement the actions defined by this protocol, which include incrementing/decrementing coefficient values. Such features are not defined for the HSS EX10 core.” Stauffer, 59. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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H. INDEPENDENT CLAIM 8

Claim 8	Stauffer
8[pre] A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:	To the extent the preamble is limiting, Stauffer discloses and/or renders obvious this limitation. “The XGXS PCS sublayer performs 8B/10B encoding and decoding of MAC frames. Each byte of data maps to a corresponding 10-bit symbol. In addition, the XGMII control characters in Table 5.12, with the exception of the Idle character, directly map to corresponding 10-bit symbols. This mapping is shown in Table 5.12 using the symbol nomenclature for 8B/10B codes. (The 8B/10B block code was described in Sect. 4.2.2.1.)” Stauffer, 207. “XGMII Idles are randomly converted to one of the following 10-bit codes: Sync (K28.5), Skip (K28.0), or Align (K28.3). A LFSR is used to randomly either generate Sync or Skip symbols. Align symbols are inserted at randomized intervals in the range of 16–31 symbols, with this interval also determined by a LFSR. The same symbol is transmitted on all lanes.” Stauffer, 207. “Align symbols are used by the receive PCS logic to perform deskew across all lanes of the interface such that the XGMII RXD[31:0] output is aligned to a common clock domain. The Align symbol is unique and does not otherwise occur in the protocol. Since it is transmitted on all lanes simultaneously, and is only transmitted every 16–31 symbols, the lanes can be deskewed by aligning the occurrence of this symbol.” Stauffer, 207.

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Claim 8	Stauffer
	“Skip symbols are used by the receive PCS logic to adjust for frequency differences between the recovered receive clock and the local XGMII clock. Skip symbols are inserted or dropped as needed.” Stauffer, 207. “The Sequence symbol (K28.4) is used on lane 0, in conjunction with Dxx.y symbols on the other lanes, to convey management information. Such information is inserted by the MAC layer between frames in place of Idles, and is conveyed through the XGXS accordingly.” Stauffer, 207. “The 10-Gb Serial Electrical Interface (XFI) was developed as part of the 10-Gigabit Small Form Factor Pluggable (XFP) Multi Source Agreement (MSA). This MSA was developed by a consortium of optics module vendors who agreed to source optics modules meeting the XFP requirements. The XFI is a 10-Gbps serial electrical interface for communications between the XFP module and a SONET framer chip, or an Ethernet PCS/PMA layer. The PCS and PMA sublayers defined in clauses 49 and 51, respectively, define the necessary functions to interface between XGMII and XFI, and are used with all 10-Gb Ethernet serial variants (including backplane applications using the PMD defined in clause 72). Although the XFI acronym does not appear anywhere in the IEEE 802.3 standard, for historical reasons implementations of clause 49 and 51 are commonly called XFI.” Stauffer, 207-08.

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Claim 8	Stauffer
	“The XFI PCS encodes and serializes the XGMII transmit data (TXD/TXC signals) for transmission on XFI. Each XGMII lane is 64B/66B encoded, scrambled, serialized, and transmitted at a baud rate of 10.3125 Gbps. XFI serial data signals received by the XFI PCS are deserialized, descrambled, 64B/66B decoded, and then driven to the MAC or PHY on the XGMII receive data (RXD/RXC signals). XFI is a full duplex interface consisting of one transmit and one receive serial data signals.” Stauffer, 208. “An optional 16-bit bus is defined to interface between the PCS sublayer and the PMA sublayer. While this is the reference interface between the XFI PCS and the HSS core implementing the PMA sublayer as defined by clause 49, it does require data to be transferred on the parallel bus of the HSS core at 644.53 Mtransfers per second. Implementations may choose HSS core options which utilize more bits of parallel data at a slower transfer rate. (Available IBM cores use a 32-bit interface.) The definition of this interface has significance for two reasons: • The 66-bit code word blocks produced by 64B/66B encoding of the XGMII data are not an integer multiple of the width of the parallel data bus on most HSS cores. Data must be steered from cycle to cycle by “gearbox” logic in order to map the 66-bit blocks onto the 16-bit (or 2-bit) parallel data bus of the HSS core. • 10GBASE-W Wide Area Network (WAN) variants are intended to interoperate with other network nodes on a SONET/SDH network. These variants define a WAN Interface Sublayer (WIS) in clause 50 which maps the Ethernet packets into a SONET SPE, and then wraps this data with SONET/SDH overhead bytes with the level of support defined in clause 50. WIS is sandwiched between the PCS and PMA sublayers for 10GBASE-W variants.” Stauffer, 208. To the extent that this preamble is not disclosed, either explicitly or inherently, by Stauffer, this preamble is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come

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Claim 8	Stauffer
	from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and	Stauffer discloses and/or renders obvious this limitation. “Conceptually, the input to the serializer transmit stage is an n-bit datapath which is serialized to a one-bit serial data signal for application to the FFE and Driver stages. Generally the value of n is a multiple of 8 or 10, and may be programmable on some implementations. Values of n which are multiples of 8 are useful for sending unencoded and/or scrambled data bytes; values of n which are multiples of 10 are useful for protocols which use 8B/10B coding, as discussed further in Sect. 4.2.2.1. (The 8B/10B encoder is generally implemented by logic outside the Serdes core.)” Stauffer, 9. “For simplicity, the block diagram in Fig. 1.8 illustrates the serializer feeding one-bit data into the transmit equalization block. Actual implementations may vary, and this datapath may be one or more bits wide. A wider datapath through the equalizer block results in a more complex design, but requires a lower operating frequency. Some implementations may initially multiplex the n-bit input to an m-bit datapath ($m < n$) prior to the equalizer, and perform the remainder of the serialization at the driver stage.” Stauffer, 9. “The serializer stage latches data on the n-bit input at the frequency of baud rate/n. The high-speed clock in the Serdes is divided down to generate a sample clock for the parallel data. Because the phase of this clock is determined by the internal state of the serializer, the Serdes channel generally provides this clock as an output for use by logic driving data to the transmit channel.” Stauffer, 9.

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Claim 8	Stauffer
	“Conceptually, the deserializer receive block performs the inverse function of the serializer block. Serial data is deserialized onto an n-bit databus of similar width to the serializer. A sample clock is generated by dividing down the internal high-speed clock, and this clock is supplied as an output for use by logic latching the parallel data. In a similar manner to the serializer, actual implementations may perform partial deserialization in a prior stage.” Stauffer, 9. “Many Serdes receivers also include a feature to assist with data alignment of the output. Most applications organize data into bytes or words (groups of bytes). For 8B/10B encoded applications, data is organized into 10-bit encoded symbols. The initialization of the clock divider in the deserializer is arbitrary, and the data received on the parallel data bus will have an arbitrary alignment that is unlikely to match the byte or symbol boundaries of the protocol. This can be corrected by downstream logic to steer data onto the appropriate byte, symbol, or word boundary. Alternatively, many Serdes receivers provide an input which forces the deserializer to “slip” one bit. Downstream logic detects that data is not aligned to the appropriate boundary, and repeatedly pulses the deserializer control until the data “slips” to the desired alignment.” Stauffer, 9-10. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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Claim 8	Stauffer
8[b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model,	Stauffer discloses and/or renders obvious this limitation. “Conceptually, the input to the serializer transmit stage is an n-bit datapath which is serialized to a one-bit serial data signal for application to the FFE and Driver stages. Generally the value of n is a multiple of 8 or 10, and may be programmable on some implementations. Values of n which are multiples of 8 are useful for sending unencoded and/or scrambled data bytes; values of n which are multiples of 10 are useful for protocols which use 8B/10B coding, as discussed further in Sect. 4.2.2.1. (The 8B/10B encoder is generally implemented by logic outside the Serdes core.)” Stauffer, 9. “For simplicity, the block diagram in Fig. 1.8 illustrates the serializer feeding one-bit data into the transmit equalization block. Actual implementations may vary, and this datapath may be one or more bits wide. A wider datapath through the equalizer block results in a more complex design, but requires a lower operating frequency. Some implementations may initially multiplex the n-bit input to an m-bit datapath ($m < n$) prior to the equalizer, and perform the remainder of the serialization at the driver stage.” Stauffer, 9. “The serializer stage latches data on the n-bit input at the frequency of baud rate/n. The high-speed clock in the Serdes is divided down to generate a sample clock for the parallel data. Because the phase of this clock is determined by the internal state of the serializer, the Serdes channel generally provides this clock as an output for use by logic driving data to the transmit channel.” Stauffer, 9. “Conceptually, the deserializer receive block performs the inverse function of the serializer block. Serial data is deserialized onto an n-bit databus of similar width to the serializer. A sample clock is generated by

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Claim 8	Stauffer
	dividing down the internal high-speed clock, and this clock is supplied as an output for use by logic latching the parallel data. In a similar manner to the serializer, actual implementations may perform partial deserialization in a prior stage.” Stauffer, 9. “Many Serdes receivers also include a feature to assist with data alignment of the output. Most applications organize data into bytes or words (groups of bytes). For 8B/10B encoded applications, data is organized into 10-bit encoded symbols. The initialization of the clock divider in the deserializer is arbitrary, and the data received on the parallel data bus will have an arbitrary alignment that is unlikely to match the byte or symbol boundaries of the protocol. This can be corrected by downstream logic to steer data onto the appropriate byte, symbol, or word boundary. Alternatively, many Serdes receivers provide an input which forces the deserializer to “slip” one bit. Downstream logic detects that data is not aligned to the appropriate boundary, and repeatedly pulses the deserializer control until the data “slips” to the desired alignment.” Stauffer, 9-10. “In this section, the functions of the transmitter slice of the HSS EX10 10-Gbps core are described. This core supports transmit bit rates as low as 8.5 Gbps and as high as 11.1 Gbps. Frequent references are made to the pin descriptions and register definitions found in Sect. 5.5.42.1. Although the HSS EX10 is only a tutorial example, the reader should compare the functions of the EX10 to real HSS cores with which the reader is familiar. Although implementations may vary, many similar functions will be found. In reading this chapter, the reader should acquire an understanding of the types of functions that may exist and some of the key features related to these functions.” Stauffer, 53. “A conceptual block diagram of the HSS EX10 transmitter is shown in Fig. 2.4. The parallel data input of the transmitter (TXxD[19:0]) has a 20-bit data width which may be programmed to capture 8, 10, 16, or 20

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Claim 8	Stauffer
	bits of user data (based on the setting of the Parallel Data Bus Width control bits in the Transmit Configuration Mode Register) on the rising edge of the word transmit clock (TXxDCLK). Other cores may support different data widths.” Stauffer, 53.

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Claim 8	Stauffer
	The diagram illustrates the transmitter architecture. TXxD[19:0] is input to a Mux. The output of this Mux goes to an 8/10/16/20-bit Data Capture Register. The output of the Data Capture Register goes to a Byte DataOut Register. The output of the Byte DataOut Register goes to an 8:1 Mux. The output of the 8:1 Mux goes to a Driver/equalizer. The output of the Driver/equalizer goes to TXxOP/TXxON and JTAG. The output of JTAG goes to TXxBSOUT. A Pseudo-random code generator outputs TXxPRBSEN to the 8:1 Mux. A PLL/Clock Divider (one per core) outputs 1.4 GHz to a Clock Divider. The Clock Divider outputs TXxDCLK to the Data Capture Register and TXxBSIN to the Mux. The PLL/Clock Divider also outputs TXxBSOUT. A Note indicates: PLL is shared across all ports. Control Registers are connected to HSSPRTADDR, HSSPRTDATAIN, and HSSPRTDATAOUT. Fig. 2.4 Transmitter concept diagram “The data in Fig. 2.4 is sampled and latched into a shift register synchronous with the high-speed transmit clock. The low order byte is synchronously loaded into a data out register that is clocked at one-eighth the bit rate, while the higher ordered bytes are synchronously shifted to lower byte positions. The 8 bits in the

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Claim 8	Stauffer
	data out register are transferred to the driver where they are further serialized and transmitted at up to 11.1 Gbps. The transferred eight-bit data byte is processed starting with the least significant bit (LSB) first, followed by the next higher significant bit, and so forth. The driver/equalizer multiplexes the 8-bit stream and creates a current-mode differential signal that is frequency equalized for the assumed media channel. The equalization is completely programmable but typically implements a finite impulse response (FIR) preemphasis filter using reduced current levels for longer run lengths. The core expects valid user data to be available on the parallel interface on each cycle.” Stauffer, 54. “In addition to the datapath, Fig. 2.4 also includes the PLL (actually located in the PLL slice), the PRBS generator (discussed later), and an interface for reading and writing control registers. Note that not all cores use control registers to implement slice control. Control signals can also be implemented as individual pins on the core and controlled by chip logic or by protocol cores. Which approach is used varies from one core family to the next, and is somewhat based upon the required number of control and status signals. Using internal registers in the core is a more efficient solution when an excessive number of control and status signals are needed.” Stauffer, 54. “Many of the TX slice parameter control registers are not effective immediately after being written. Application of register values to the analog circuits is controlled by writing the Apply Load bit in the Transmit Coefficient Control Register. This allows the FFE and power level configuration to be completely loaded in the individual registers and then simultaneously applied to the analog circuits. For the HSS EX10, the values loaded into the Transmit TapX Coefficient Registers, the Transmit Power Register, the Transmit Polarity Register, and the FFE Mode Select field of the Transmit Driver Mode Control Register are not applied to the analog circuits until the Apply Load bit is pulsed. The read-back value of these registers reflects the value being applied to the analog circuits. If these registers are written and then read before the Apply Load bit is pulsed, the old values are read. (The value of the Slow Slew Control field of the Transmit Driver Mode Control Register is applied to the analog circuits immediately, and is not gated

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Claim 8	Stauffer
	by the Apply Load bit.)” Stauffer, 59. “For cores which do not contain internal registers, filter coefficients may be set using input control pins. Sequencing updated values onto these pins is the responsibility of the chip designer” Stauffer, 59. “FFE coefficient values are not intended to be changed dynamically while data is being transmitted (except as part of a speed negotiation or link optimization process). Significant changes to the TX slice configuration can cause loss of data at the receiver until such time as the receiver adapts to the new waveform characteristics.” Stauffer, 59. “Higher speed protocol standards sometimes support negotiation of transmitter FFE settings based on characteristics of the signal at the receiver. IEEE 802.3ap Backplane Ethernet is an example of such an application. Implementations of such applications must update FFE coefficients in response to a full duplex training protocol by reading and writing the corresponding registers.” Stauffer, 59. “The training protocol used for Backplane Ethernet is introduced in Sect. 5.3.5.1. Some cores provide register control signals to more easily implement the actions defined by this protocol, which include incrementing/decrementing coefficient values. Such features are not defined for the HSS EX10 core.” Stauffer, 59.

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Claim 8	Stauffer
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[c] the controller using one of the registers to set initial coefficient values for the one or more transmit filters.	Stauffer discloses and/or renders obvious this limitation. “The interconnect between the transmitter and receiver device (known as the channel) acts as a filter at typical baud rates, and distorts the serial data signal to varying extents. Figure 1.9 illustrates this distortion: The input waveform is a clean digital signal, but the output waveform is significantly distorted. The illustrated frequency response function for the channel is characteristic of a low-pass filter. Signal distortion occurs because the signal baud rate is above the cut-off frequency for this filter.” Stauffer, 10. “Signal integrity concerns frequently dictate that the data signal be equalized at the transmitter and/or receiver in order to counter the effects of the channel and decode the signal properly. Many variations on filter architectures are possible, all of which accomplish this. Fig. 1.10 illustrates the addition of an equalizer at the transmitter with a transfer function that is roughly the inverse of the channel’s frequency response. This equalizer distorts the signal at the transmitter output such that the resulting signal at the receiver input is a clean waveform.” Stauffer, 10. “Most Serdes transmitter implementations include a FFE. The block diagram for a three-tap FFE is shown

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Claim 8	Stauffer
	in Fig. 1.11. The serial data signal is delayed by several flip-flops which implement the taps for the filter. Each tap is multiplied by a tap weight value (also called a filter coefficient), and the results are summed and driven to the serial data output. FFE operation is described further in Sect. 3.2.1.” Stauffer, 10. “The number of FFE taps on the filter, the spacing of these taps relative to the baud rate, and the granularity of these tap weight values vary based on implementation. The terminology preemphasis or deemphasis refer to the FFE architecture, and indicate whether the data signal amplitude is increased or decreased as compared to the nonemphasized value by the FFE tap. The terminology precursor taps and postcursor taps refer to whether the FFE filter taps operate on an advanced or delayed signal (respectively) relative to the $t = 0$ tap. Baud-spaced taps are defined as taps where the delay from one filter tap to the adjacent tap is one-bit time interval; fractional spacing of the taps is also possible.” Stauffer, 10. “The FFE tap weights are selected to generate a filter with the inverse transfer function of the channel transfer function. Various algorithms exist for determining optimal FFE coefficient values; some select filter coefficients to maximize signal amplitude at the receiver, while others optimize eye width (i.e., minimizing jitter). More complex algorithms may search for an optimal trade-off between amplitude and jitter in order to optimize a more complex parameter (such as projected BER). FFE tap weights are determined for many applications by design and coded as fixed values within system software, however, there are some applications where FFE tap weights are adjusted dynamically by the protocol based on signal characteristics at the receiver.” Stauffer, 10-11.

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Claim 8	Stauffer
	Typical Backplane Application Fig. 1.9 Signal distortion for a typical channel application Fig. 1.10 Typical channel application with equalization at the transmitter

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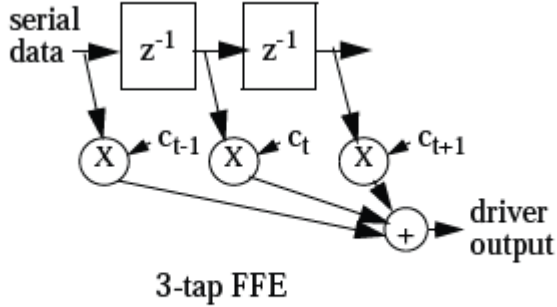
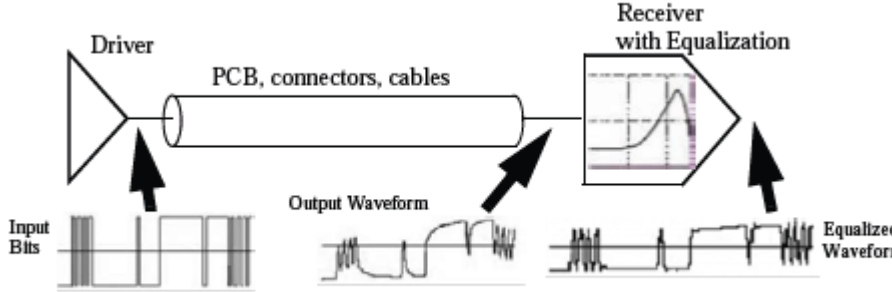
Claim 8	Stauffer
	 3-tap FFE Fig. 1.11 Three-tap feed forward equalizer operation  Fig. 1.12 Typical channel application with equalization at the receiver

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Claim 8	Stauffer
	Fig. 1.13 Receiver frequency response for peaking amplifier settings Fig. 1.14 Decision feedback equalizer architecture

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Claim 8	Stauffer
	“In this section, the functions of the transmitter slice of the HSS EX10 10-Gbps core are described. This core supports transmit bit rates as low as 8.5 Gbps and as high as 11.1 Gbps. Frequent references are made to the pin descriptions and register definitions found in Sect. 5.5.42.1. Although the HSS EX10 is only a tutorial example, the reader should compare the functions of the EX10 to real HSS cores with which the reader is familiar. Although implementations may vary, many similar functions will be found. In reading this chapter, the reader should acquire an understanding of the types of functions that may exist and some of the key features related to these functions.” Stauffer, 53. “A conceptual block diagram of the HSS EX10 transmitter is shown in Fig. 2.4. The parallel data input of the transmitter (TXxD[19:0]) has a 20-bit data width which may be programmed to capture 8, 10, 16, or 20 bits of user data (based on the setting of the Parallel Data Bus Width control bits in the Transmit Configuration Mode Register) on the rising edge of the word transmit clock (TXxDCLK). Other cores may support different data widths.” Stauffer, 53.

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Claim 8	Stauffer
	The diagram illustrates the transmitter architecture. Data from TXxD[19:0] enters a Mux, which also receives TXxBSIN. The output of this Mux goes to an 8/10/16/20-bit Data Capture Register. The output of the Data Capture Register goes to a Byte DataOut Register, which is clocked by TXxDCLK. The Byte DataOut Register outputs 8 bits to an 8:1 Mux. The 8:1 Mux also receives input from a Pseudo-random code generator (TXxPRBSEN) and a PLL/Clock Divider. The output of the 8:1 Mux goes to a Driver/equalizer, which outputs TXxOP/TXxON. The Driver/equalizer also receives input from a JTAG block (TXxBSOUT). The PLL/Clock Divider (one per core) provides a 1.4 GHz clock to the 8:1 Mux and the Driver/equalizer. The PLL/Clock Divider also provides a clock to the Data Capture Register and the Byte DataOut Register. The PLL/Clock Divider is shared across all ports. The Control Registers receive HSSPRTADDR, HSSPRTDATAIN, and HSSPRTDATAOUT signals. A Wrapback signal is also shown. Fig. 2.4 Transmitter concept diagram “The data in Fig. 2.4 is sampled and latched into a shift register synchronous with the high-speed transmit clock. The low order byte is synchronously loaded into a data out register that is clocked at one-eighth the bit rate, while the higher ordered bytes are synchronously shifted to lower byte positions. The 8 bits in the

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Claim 8	Stauffer
	data out register are transferred to the driver where they are further serialized and transmitted at up to 11.1 Gbps. The transferred eight-bit data byte is processed starting with the least significant bit (LSB) first, followed by the next higher significant bit, and so forth. The driver/equalizer multiplexes the 8-bit stream and creates a current-mode differential signal that is frequency equalized for the assumed media channel. The equalization is completely programmable but typically implements a finite impulse response (FIR) preemphasis filter using reduced current levels for longer run lengths. The core expects valid user data to be available on the parallel interface on each cycle.” Stauffer, 54. “In addition to the datapath, Fig. 2.4 also includes the PLL (actually located in the PLL slice), the PRBS generator (discussed later), and an interface for reading and writing control registers. Note that not all cores use control registers to implement slice control. Control signals can also be implemented as individual pins on the core and controlled by chip logic or by protocol cores. Which approach is used varies from one core family to the next, and is somewhat based upon the required number of control and status signals. Using internal registers in the core is a more efficient solution when an excessive number of control and status signals are needed.” Stauffer, 54. “Many of the TX slice parameter control registers are not effective immediately after being written. Application of register values to the analog circuits is controlled by writing the Apply Load bit in the Transmit Coefficient Control Register. This allows the FFE and power level configuration to be completely loaded in the individual registers and then simultaneously applied to the analog circuits. For the HSS EX10, the values loaded into the Transmit TapX Coefficient Registers, the Transmit Power Register, the Transmit Polarity Register, and the FFE Mode Select field of the Transmit Driver Mode Control Register are not applied to the analog circuits until the Apply Load bit is pulsed. The read-back value of these registers reflects the value being applied to the analog circuits. If these registers are written and then read before the Apply Load bit is pulsed, the old values are read. (The value of the Slow Slew Control field of the Transmit Driver Mode Control Register is applied to the analog circuits immediately, and is not gated

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Claim 8	Stauffer
	by the Apply Load bit.)” Stauffer, 59. “For cores which do not contain internal registers, filter coefficients may be set using input control pins. Sequencing updated values onto these pins is the responsibility of the chip designer.” Stauffer, 59. “FFE coefficient values are not intended to be changed dynamically while data is being transmitted (except as part of a speed negotiation or link optimization process). Significant changes to the TX slice configuration can cause loss of data at the receiver until such time as the receiver adapts to the new waveform characteristics.” Stauffer, 59. “Higher speed protocol standards sometimes support negotiation of transmitter FFE settings based on characteristics of the signal at the receiver. IEEE 802.3ap Backplane Ethernet is an example of such an application. Implementations of such applications must update FFE coefficients in response to a full duplex training protocol by reading and writing the corresponding registers.” Stauffer, 59. “The training protocol used for Backplane Ethernet is introduced in Sect. 5.3.5.1. Some cores provide register control signals to more easily implement the actions defined by this protocol, which include incrementing/decrementing coefficient values. Such features are not defined for the HSS EX10 core.” Stauffer, 59.

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Claim 8	Stauffer
	To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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I. DEPENDENT CLAIM 9

Claim 9	Stauffer
9. The communications link of claim 8, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.	Stauffer discloses and/or renders obvious this limitation. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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J. DEPENDENT CLAIM 10

Claim 10	Stauffer
10. The communications link of claim 8, wherein at least some of the different channel models presume different types of receiver equalization.	Stauffer discloses and/or renders obvious this limitation. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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K. INDEPENDENT CLAIM 11

Claim 11	Stauffer
11[pre] A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:	To the extent the preamble is limiting, Stauffer discloses and/or renders obvious this limitation. “The XGXS PCS sublayer performs 8B/10B encoding and decoding of MAC frames. Each byte of data maps to a corresponding 10-bit symbol. In addition, the XGMII control characters in Table 5.12, with the exception of the Idle character, directly map to corresponding 10-bit symbols. This mapping is shown in Table 5.12 using the symbol nomenclature for 8B/10B codes. (The 8B/10B block code was described in Sect. 4.2.2.1.)” Stauffer, 207. “XGMII Idles are randomly converted to one of the following 10-bit codes: Sync (K28.5), Skip (K28.0), or Align (K28.3). A LFSR is used to randomly either generate Sync or Skip symbols. Align symbols are inserted at randomized intervals in the range of 16–31 symbols, with this interval also determined by a LFSR. The same symbol is transmitted on all lanes.” Stauffer, 207. “Align symbols are used by the receive PCS logic to perform deskew across all lanes of the interface such that the XGMII RXD[31:0] output is aligned to a common clock domain. The Align symbol is unique and does not otherwise occur in the protocol. Since it is transmitted on all lanes simultaneously, and is only transmitted every 16–31 symbols, the lanes can be deskewed by aligning the occurrence of this symbol.” Stauffer, 207.

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Claim 11	Stauffer
	“Skip symbols are used by the receive PCS logic to adjust for frequency differences between the recovered receive clock and the local XGMII clock. Skip symbols are inserted or dropped as needed.” Stauffer, 207. “The Sequence symbol (K28.4) is used on lane 0, in conjunction with Dxx.y symbols on the other lanes, to convey management information. Such information is inserted by the MAC layer between frames in place of Idles, and is conveyed through the XGXS accordingly.” Stauffer, 207. “The 10-Gb Serial Electrical Interface (XFI) was developed as part of the 10-Gigabit Small Form Factor Pluggable (XFP) Multi Source Agreement (MSA). This MSA was developed by a consortium of optics module vendors who agreed to source optics modules meeting the XFP requirements. The XFI is a 10-Gbps serial electrical interface for communications between the XFP module and a SONET framer chip, or an Ethernet PCS/PMA layer. The PCS and PMA sublayers defined in clauses 49 and 51, respectively, define the necessary functions to interface between XGMII and XFI, and are used with all 10-Gb Ethernet serial variants (including backplane applications using the PMD defined in clause 72). Although the XFI acronym does not appear anywhere in the IEEE 802.3 standard, for historical reasons implementations of clause 49 and 51 are commonly called XFI.” Stauffer, 207-08. “The XFI PCS encodes and serializes the XGMII transmit data (TXD/TXC signals) for transmission on XFI. Each XGMII lane is 64B/66B encoded, scrambled, serialized, and transmitted at a baud rate of 10.3125 Gbps. XFI serial data signals received by the XFI PCS are deserialized, descrambled, 64B/66B decoded, and then driven to the MAC or PHY on the XGMII receive data (RXD/RXC signals). XFI is a full duplex interface consisting of one transmit and one receive serial data signals.”

Exhibit C-11

Claim 11	Stauffer
	Stauffer, 208. “An optional 16-bit bus is defined to interface between the PCS sublayer and the PMA sublayer. While this is the reference interface between the XFI PCS and the HSS core implementing the PMA sublayer as defined by clause 49, it does require data to be transferred on the parallel bus of the HSS core at 644.53 Mtransfers per second. Implementations may choose HSS core options which utilize more bits of parallel data at a slower transfer rate. (Available IBM cores use a 32-bit interface.) The definition of this interface has significance for two reasons: • The 66-bit code word blocks produced by 64B/66B encoding of the XGMII data are not an integer multiple of the width of the parallel data bus on most HSS cores. Data must be steered from cycle to cycle by “gearbox” logic in order to map the 66-bit blocks onto the 16-bit (or 2-bit) parallel data bus of the HSS core. • 10GBASE-W Wide Area Network (WAN) variants are intended to interoperate with other network nodes on a SONET/SDH network. These variants define a WAN Interface Sublayer (WIS) in clause 50 which maps the Ethernet packets into a SONET SPE, and then wraps this data with SONET/SDH overhead bytes with the level of support defined in clause 50. WIS is sandwiched between the PCS and PMA sublayers for 10GBASE-W variants.” Stauffer, 208. “There are three significant features associated with Backplane Ethernet which are not used in other Ethernet variants. These features are: • Training protocol (defined in Clause 72 for 10GBASE-KR) • Autonegotiation (defined in Clause 73 for all Backplane Ethernet variants) • Forward error correction (FEC) (defined in Clause 74 for optional use with 10GBASE-KR)” Stauffer, 213. To the extent that this preamble is not disclosed, either explicitly or inherently, by Stauffer, this preamble is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the

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Claim 11	Stauffer
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11[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and	Stauffer discloses and/or renders obvious this limitation. “The XGXS PCS sublayer performs 8B/10B encoding and decoding of MAC frames. Each byte of data maps to a corresponding 10-bit symbol. In addition, the XGMII control characters in Table 5.12, with the exception of the Idle character, directly map to corresponding 10-bit symbols. This mapping is shown in Table 5.12 using the symbol nomenclature for 8B/10B codes. (The 8B/10B block code was described in Sect. 4.2.2.1.)” Stauffer, 207. “XGMII Idles are randomly converted to one of the following 10-bit codes: Sync (K28.5), Skip (K28.0), or Align (K28.3). A LFSR is used to randomly either generate Sync or Skip symbols. Align symbols are inserted at randomized intervals in the range of 16–31 symbols, with this interval also determined by a LFSR. The same symbol is transmitted on all lanes.” Stauffer, 207. “Align symbols are used by the receive PCS logic to perform deskew across all lanes of the interface such that the XGMII RXD[31:0] output is aligned to a common clock domain. The Align symbol is unique and does not otherwise occur in the protocol. Since it is transmitted on all lanes simultaneously, and is only transmitted every 16–31 symbols, the lanes can be deskewed by aligning the occurrence of this symbol.” Stauffer, 207.

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Claim 11	Stauffer
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Claim 11	Stauffer
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Claim 11	Stauffer
	Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
11[b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic,	Stauffer discloses and/or renders obvious this limitation. “Many of the TX slice parameter control registers are not effective immediately after being written. Application of register values to the analog circuits is controlled by writing the Apply Load bit in the Transmit Coefficient Control Register. This allows the FFE and power level configuration to be completely loaded in the individual registers and then simultaneously applied to the analog circuits. For the HSS EX10, the values loaded into the Transmit TapX Coefficient Registers, the Transmit Power Register, the Transmit Polarity Register, and the FFE Mode Select field of the Transmit Driver Mode Control Register are not applied to the analog circuits until the Apply Load bit is pulsed. The read-back value of these registers reflects the value being applied to the analog circuits. If these registers are written and then read before the Apply Load bit is pulsed, the old values are read. (The value of the Slow Slew Control field of the Transmit Driver Mode Control Register is applied to the analog circuits immediately, and is not gated by the Apply Load bit.)” Stauffer, 59. “For cores which do not contain internal registers, filter coefficients may be set using input control pins. Sequencing updated values onto these pins is the responsibility of the chip designer.” Stauffer, 59. “FFE coefficient values are not intended to be changed dynamically while data is being transmitted (except as part of a speed negotiation or link optimization process). Significant changes to the TX slice

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Claim 11	Stauffer
	configuration can cause loss of data at the receiver until such time as the receiver adapts to the new waveform characteristics.” Stauffer, 59. “Higher speed protocol standards sometimes support negotiation of transmitter FFE settings based on characteristics of the signal at the receiver. IEEE 802.3ap Backplane Ethernet is an example of such an application. Implementations of such applications must update FFE coefficients in response to a full duplex training protocol by reading and writing the corresponding registers.” Stauffer, 59. “The training protocol used for Backplane Ethernet is introduced in Sect. 5.3.5.1. Some cores provide register control signals to more easily implement the actions defined by this protocol, which include incrementing/decrementing coefficient values. Such features are not defined for the HSS EX10 core.” Stauffer, 59. “Note, however, that in a real system the channel does distort the signal. This distortion, and associated signal integrity topics, are discussed in Chap. 8. HSS transmitters often contain an FFE circuit which is capable of altering the transmitted signal. The FFE emphasizes the transmitted signal to cancel the distortion effects of the channel, and thereby provide good signal quality at the receiver input. Measurements performed at the transmitter output must be performed using defined FFE settings, and provide no guidance as to the signal quality at the receiver.” Stauffer, 329. “An alternative used by many protocol standards is to define the characteristics of a compliance channel, and to perform transmitter characterization by measuring the transmitted signal at the far-end of this

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	channel. This is also shown in Fig. 7.16, with the DUT driving a channel, and test equipment connected to the far-end of the channel. In this case, the FFE is expected to be set based on the channel characteristics to obtain the best possible signal quality at the test point.” Stauffer, 329. “HSS design teams perform characterization testing of their transmitter devices using both methods. Specifications for jitter and amplitude of the transmitter output require measurements directly at this point. Characterization of the FFE and model to hardware correlation of hardware to various signal integrity models requires measurements at the far-end of known channels. Furthermore, compliance testing for various protocol standards requires measurements be taken consistent with the test methods and conditions defined by the standards document.” Stauffer, 329. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
11[c] the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more	Stauffer discloses and/or renders obvious this limitation. “The interconnect between the transmitter and receiver device (known as the channel) acts as a filter at typical baud rates, and distorts the serial data signal to varying extents. Figure 1.9 illustrates this distortion: The input waveform is a clean digital signal, but the output waveform is significantly distorted. The

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transmit filters.	illustrated frequency response function for the channel is characteristic of a low-pass filter. Signal distortion occurs because the signal baud rate is above the cut-off frequency for this filter.” Stauffer, 10. “Signal integrity concerns frequently dictate that the data signal be equalized at the transmitter and/or receiver in order to counter the effects of the channel and decode the signal properly. Many variations on filter architectures are possible, all of which accomplish this. Fig. 1.10 illustrates the addition of an equalizer at the transmitter with a transfer function that is roughly the inverse of the channel’s frequency response. This equalizer distorts the signal at the transmitter output such that the resulting signal at the receiver input is a clean waveform.” Stauffer, 10. “Most Serdes transmitter implementations include a FFE. The block diagram for a three-tap FFE is shown in Fig. 1.11. The serial data signal is delayed by several flip-flops which implement the taps for the filter. Each tap is multiplied by a tap weight value (also called a filter coefficient), and the results are summed and driven to the serial data output. FFE operation is described further in Sect. 3.2.1.” Stauffer, 10. “The number of FFE taps on the filter, the spacing of these taps relative to the baud rate, and the granularity of these tap weight values vary based on implementation. The terminology preemphasis or deemphasis refer to the FFE architecture, and indicate whether the data signal amplitude is increased or decreased as compared to the nonemphasized value by the FFE tap. The terminology precursor taps and postcursor taps refer to whether the FFE filter taps operate on an advanced or delayed signal (respectively) relative to the $t = 0$ tap. Baud-spaced taps are defined as taps where the delay from one filter tap to the adjacent tap is one-bit time interval; fractional spacing of the taps is also possible.” Stauffer, 10.

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Claim 11	Stauffer
	“The FFE tap weights are selected to generate a filter with the inverse transfer function of the channel transfer function. Various algorithms exist for determining optimal FFE coefficient values; some select filter coefficients to maximize signal amplitude at the receiver, while others optimize eye width (i.e., minimizing jitter). More complex algorithms may search for an optimal trade-off between amplitude and jitter in order to optimize a more complex parameter (such as projected BER). FFE tap weights are determined for many applications by design and coded as fixed values within system software, however, there are some applications where FFE tap weights are adjusted dynamically by the protocol based on signal characteristics at the receiver.” Stauffer, 10-11. The diagram, titled 'Typical Backplane Application', illustrates the signal path from a Driver to a Receiver through a channel consisting of PCB, connectors, and cables. Below the channel, three plots are shown: 'Input Bits' (a square wave), a graph of 'Attenuation per meter' vs 'Frequency-Hz' (showing a low-pass filter response), and 'Output Waveform' (a distorted, rounded square wave). Fig. 1.9 Signal distortion for a typical channel application

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Claim 11	Stauffer
	Fig. 1.10 Typical channel application with equalization at the transmitter Fig. 1.11 Three-tap feed forward equalizer operation

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Claim 11	Stauffer
	Fig. 1.12 Typical channel application with equalization at the receiver Fig. 1.13 Receiver frequency response for peaking amplifier settings

Exhibit C-11

Claim 11	Stauffer
	Fig. 1.14 Decision feedback equalizer architecture “In this section, the functions of the transmitter slice of the HSS EX10 10-Gbps core are described. This core supports transmit bit rates as low as 8.5 Gbps and as high as 11.1 Gbps. Frequent references are made to the pin descriptions and register definitions found in Sect. 5.5.42.1. Although the HSS EX10 is only a tutorial example, the reader should compare the functions of the EX10 to real HSS cores with which the reader is familiar. Although implementations may vary, many similar functions will be found. In reading this chapter, the reader should acquire an understanding of the types of functions that may exist and some of the key features related to these functions.” Stauffer, 53. “A conceptual block diagram of the HSS EX10 transmitter is shown in Fig. 2.4. The parallel data input of the transmitter (TXxD[19:0]) has a 20-bit data width which may be programmed to capture 8, 10, 16, or 20 bits of user data (based on the setting of the Parallel Data Bus Width control bits in the Transmit Configuration Mode Register) on the rising edge of the word transmit clock (TXxDCLK). Other cores may support different data widths.” Stauffer, 53.

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Claim 11	Stauffer
	The diagram illustrates the transmitter architecture. It starts with a 20-bit data input TXxD[19:0] entering a multiplexer (Mux). The output of this Mux goes to an 8/10/16/20-bit Data Capture Register. The output of the register is sent to a Byte DataOut Register. The output of the Byte DataOut Register is then sent to an 8:1 Mux. The output of the 8:1 Mux goes to a Driver/equalizer. The output of the Driver/equalizer is TXxOP/TXxON. A feedback loop labeled 'Wrapback' goes from the output of the Driver/equalizer back to the input of the first Mux. Another feedback loop labeled 'TXxBSOUT' goes from the output of the Driver/equalizer to a JTAG block, which then outputs TXxBSOUT. A Pseudo-random code generator provides TXxPRBSEN to the 8:1 Mux. A PLL/Clock Divider (one per core) provides a 1.4 GHz clock to a Clock Divider, which then provides TXxDCLK to the Data Capture Register. The PLL/Clock Divider also provides a shared clock to the other components. Control Registers are connected to HSSPRTADDR, HSSPRTDATAIN, and HSSPRTDATAOUT. A note states: 'Note: PLL is shared across all ports.' Fig. 2.4 Transmitter concept diagram “The data in Fig. 2.4 is sampled and latched into a shift register synchronous with the high-speed transmit

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	clock. The low order byte is synchronously loaded into a data out register that is clocked at one-eighth the bit rate, while the higher ordered bytes are synchronously shifted to lower byte positions. The 8 bits in the data out register are transferred to the driver where they are further serialized and transmitted at up to 11.1 Gbps. The transferred eight-bit data byte is processed starting with the least significant bit (LSB) first, followed by the next higher significant bit, and so forth. The driver/equalizer multiplexes the 8-bit stream and creates a current-mode differential signal that is frequency equalized for the assumed media channel. The equalization is completely programmable but typically implements a finite impulse response (FIR) preemphasis filter using reduced current levels for longer run lengths. The core expects valid user data to be available on the parallel interface on each cycle.” Stauffer, 54. “In addition to the datapath, Fig. 2.4 also includes the PLL (actually located in the PLL slice), the PRBS generator (discussed later), and an interface for reading and writing control registers. Note that not all cores use control registers to implement slice control. Control signals can also be implemented as individual pins on the core and controlled by chip logic or by protocol cores. Which approach is used varies from one core family to the next, and is somewhat based upon the required number of control and status signals. Using internal registers in the core is a more efficient solution when an excessive number of control and status signals are needed.” Stauffer, 54.

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Claim 11	Stauffer															
	Table 2.13 Transmit driver modes <table><tr><th>Mode</th><th>FFE mode select bits of "Transmit Driver Mode Control Register" for Port x</th><th>FFE taps activated</th></tr><tr><td>FFE2</td><td>"00"</td><td>0, 1</td></tr><tr><td>FFE3</td><td>"01"</td><td>0, 1, 2</td></tr><tr><td>(Reserved)</td><td>"10"</td><td>(Indeterminate)</td></tr><tr><td>Hi-Z</td><td>"11"</td><td>None (see Sect. 2.2.4.1)</td></tr></table> “Many of the TX slice parameter control registers are not effective immediately after being written. Application of register values to the analog circuits is controlled by writing the Apply Load bit in the Transmit Coefficient Control Register. This allows the FFE and power level configuration to be completely loaded in the individual registers and then simultaneously applied to the analog circuits. For the HSS EX10, the values loaded into the Transmit TapX Coefficient Registers, the Transmit Power Register, the Transmit Polarity Register, and the FFE Mode Select field of the Transmit Driver Mode Control Register are not applied to the analog circuits until the Apply Load bit is pulsed. The read-back value of these registers reflects the value being applied to the analog circuits. If these registers are written and then read before the Apply Load bit is pulsed, the old values are read. (The value of the Slow Slew Control field of the Transmit Driver Mode Control Register is applied to the analog circuits immediately, and is not gated by the Apply Load bit.)” Stauffer, 59. “For cores which do not contain internal registers, filter coefficients may be set using input control pins. Sequencing updated values onto these pins is the responsibility of the chip designer” Stauffer, 59.	Mode	FFE mode select bits of "Transmit Driver Mode Control Register" for Port x	FFE taps activated	FFE2	"00"	0, 1	FFE3	"01"	0, 1, 2	(Reserved)	"10"	(Indeterminate)	Hi-Z	"11"	None (see Sect. 2.2.4.1)
Mode	FFE mode select bits of "Transmit Driver Mode Control Register" for Port x	FFE taps activated														
FFE2	"00"	0, 1														
FFE3	"01"	0, 1, 2														
(Reserved)	"10"	(Indeterminate)														
Hi-Z	"11"	None (see Sect. 2.2.4.1)														

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Claim 11	Stauffer
	“FFE coefficient values are not intended to be changed dynamically while data is being transmitted (except as part of a speed negotiation or link optimization process). Significant changes to the TX slice configuration can cause loss of data at the receiver until such time as the receiver adapts to the new waveform characteristics.” Stauffer, 59. “Higher speed protocol standards sometimes support negotiation of transmitter FFE settings based on characteristics of the signal at the receiver. IEEE 802.3ap Backplane Ethernet is an example of such an application. Implementations of such applications must update FFE coefficients in response to a full duplex training protocol by reading and writing the corresponding registers.” Stauffer, 59. “The training protocol used for Backplane Ethernet is introduced in Sect. 5.3.5.1. Some cores provide register control signals to more easily implement the actions defined by this protocol, which include incrementing/decrementing coefficient values. Such features are not defined for the HSS EX10 core.” Stauffer, 59. “Note, however, that in a real system the channel does distort the signal. This distortion, and associated signal integrity topics, are discussed in Chap. 8. HSS transmitters often contain an FFE circuit which is capable of altering the transmitted signal. The FFE emphasizes the transmitted signal to cancel the distortion effects of the channel, and thereby provide good signal quality at the receiver input. Measurements performed at the transmitter output must be performed using defined FFE settings, and provide no guidance as to the signal quality at the receiver.” Stauffer, 329. “An alternative used by many protocol standards is to define the characteristics of a compliance channel,

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Claim 11	Stauffer
	and to perform transmitter characterization by measuring the transmitted signal at the far-end of this channel. This is also shown in Fig. 7.16, with the DUT driving a channel, and test equipment connected to the far-end of the channel. In this case, the FFE is expected to be set based on the channel characteristics to obtain the best possible signal quality at the test point.” Stauffer, 329. “HSS design teams perform characterization testing of their transmitter devices using both methods. Specifications for jitter and amplitude of the transmitter output require measurements directly at this point. Characterization of the FFE and model to hardware correlation of hardware to various signal integrity models requires measurements at the far-end of known channels. Furthermore, compliance testing for various protocol standards requires measurements be taken consistent with the test methods and conditions defined by the standards document.” Stauffer, 329. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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L. DEPENDENT CLAIM 12

Claim 12	Stauffer
12. The communications link of claim 11, wherein the performance characteristic is an error signal energy.	Stauffer discloses and/or renders obvious this limitation. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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M. DEPENDENT CLAIM 13

Claim 13	Stauffer
13. The communications link of claim 11, wherein the performance characteristic is a bit error rate.	Stauffer discloses and/or renders obvious this limitation. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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N. DEPENDENT CLAIM 14

Claim 14	Stauffer
14. The communications link of claim 11, wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters.	Stauffer discloses and/or renders obvious this limitation. “The interconnect between the transmitter and receiver device (known as the channel) acts as a filter at typical baud rates, and distorts the serial data signal to varying extents. Figure 1.9 illustrates this distortion: The input waveform is a clean digital signal, but the output waveform is significantly distorted. The illustrated frequency response function for the channel is characteristic of a low-pass filter. Signal distortion occurs because the signal baud rate is above the cut-off frequency for this filter.” Stauffer, 10. “Signal integrity concerns frequently dictate that the data signal be equalized at the transmitter and/or receiver in order to counter the effects of the channel and decode the signal properly. Many variations on filter architectures are possible, all of which accomplish this. Fig. 1.10 illustrates the addition of an equalizer at the transmitter with a transfer function that is roughly the inverse of the channel’s frequency response. This equalizer distorts the signal at the transmitter output such that the resulting signal at the receiver input is a clean waveform.” Stauffer, 10. “Most Serdes transmitter implementations include a FFE. The block diagram for a three-tap FFE is shown in Fig. 1.11. The serial data signal is delayed by several flip-flops which implement the taps for the filter. Each tap is multiplied by a tap weight value (also called a filter coefficient), and the results are summed and driven to the serial data output. FFE operation is described further in Sect. 3.2.1.” Stauffer, 10.

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Claim 14	Stauffer
	“The number of FFE taps on the filter, the spacing of these taps relative to the baud rate, and the granularity of these tap weight values vary based on implementation. The terminology preemphasis or deemphasis refer to the FFE architecture, and indicate whether the data signal amplitude is increased or decreased as compared to the nonemphasized value by the FFE tap. The terminology precursor taps and postcursor taps refer to whether the FFE filter taps operate on an advanced or delayed signal (respectively) relative to the $t = 0$ tap. Baud-spaced taps are defined as taps where the delay from one filter tap to the adjacent tap is one-bit time interval; fractional spacing of the taps is also possible.” Stauffer, 10. “The FFE tap weights are selected to generate a filter with the inverse transfer function of the channel transfer function. Various algorithms exist for determining optimal FFE coefficient values; some select filter coefficients to maximize signal amplitude at the receiver, while others optimize eye width (i.e., minimizing jitter). More complex algorithms may search for an optimal trade-off between amplitude and jitter in order to optimize a more complex parameter (such as projected BER). FFE tap weights are determined for many applications by design and coded as fixed values within system software, however, there are some applications where FFE tap weights are adjusted dynamically by the protocol based on signal characteristics at the receiver.” Stauffer, 10-11.

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Claim 14	Stauffer
	Typical Backplane Application Driver PCB, connectors, cables Receiver Input Bits Output Waveform Attenuation per octave Frequency (Hz) Fig. 1.9 Signal distortion for a typical channel application Driver with integrated FFE PCB, connectors, cables Receiver Preemphasis Example Using Integrated FFE Equalized Waveform Fig. 1.10 Typical channel application with equalization at the transmitter

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Claim 14	Stauffer
	Fig. 1.11 Three-tap feed forward equalizer operation Fig. 1.12 Typical channel application with equalization at the receiver

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Claim 14

Stauffer

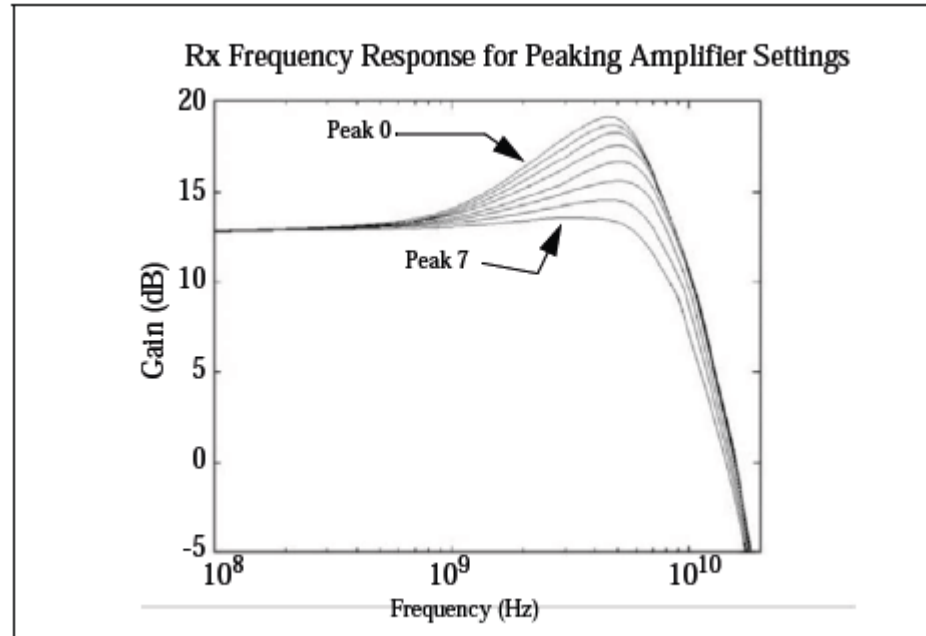


Fig. 1.13 Receiver frequency response for peaking amplifier settings

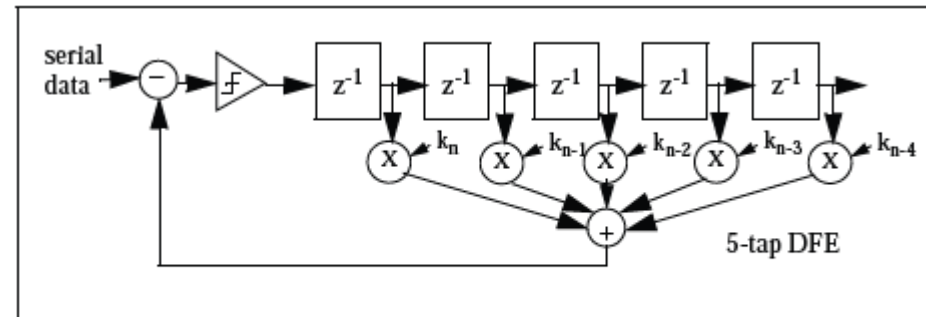


Fig. 1.14 Decision feedback equalizer architecture

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Claim 14	Stauffer
	“The HSS EX10 transmitter includes a feed forward equalization (FFE) to reduce inter-symbol interference (ISI) at the receiver. This pre-emphasis technique uses a FIR filter to compensate for the high frequency roll-off of the transmission channel. Control inputs are provided to allow adjustment of the river FFE filter coefficients on a per-port basis. The following equation describes the relationships of the FFE Coefficients. $H(Z) = K (C_0 z + 1 + C_1 z^0 + C_2 z^{-1})$ This Z-transform equation describes an FFE with three taps, including one pre and one post tap. Other cores may have FFEs with fewer or more taps.” Stauffer, 58. “The driver amplitude (K) is adjustable in the range of 0 – 1,320 (nominal) mV peak-to-peak differential using the Transmit Power Register described previously in this chapter. The relative weights and polarities of C0 to C2 are configured using the three Transmit TapX Coefficient Registers (X = 0, 1, 2), and the Transmit Polarity Register. The actual range of relative coefficient weights is defined in Table 2.12.” Stauffer, 58. “The resolution of the levels is also indicated in Table 2.12, with each tap having equal bit weighting. The driver circuit design enforces a constant driver output power for any combination of coefficients and polarities, provided the sum of coefficients C0 – C2 is 63 or higher (power decreases proportionally below this sum). As coefficients are initialized or updated, the logic calculates the appropriate internal amplitude (K) to maintain the overall output power at the level defined in the Transmit Power register.” Stauffer, 58.

Exhibit C-11

Claim 14	Stauffer																																			
	Table 2.12 Transmitter FFE summary <table><tr><td>Tap coefficient #</td><td>0</td><td>1</td><td>2</td></tr><tr><td>Max current (mA)</td><td>7.5</td><td>30</td><td>15</td></tr><tr><td>Relative max (%)</td><td>25</td><td>100</td><td>50</td></tr><tr><td>DAC resolution (bits)</td><td>6</td><td>8</td><td>7</td></tr><tr><td>Tap allocation</td><td>Precursor</td><td>Main tap</td><td>Postcursor</td></tr></table> Table 2.13 Transmit driver modes <table><tr><td>Mode</td><td>FFE mode select bits of "Transmit Driver Mode Control Register" for Port x</td><td>FFE taps activated</td></tr><tr><td>FFE2</td><td>"00"</td><td>0, 1</td></tr><tr><td>FFE3</td><td>"01"</td><td>0, 1, 2</td></tr><tr><td>(Reserved)</td><td>"10"</td><td>(Indeterminate)</td></tr><tr><td>Hi-Z</td><td>"11"</td><td>None (see Sect. 2.2.4.1)</td></tr></table> To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.	Tap coefficient #	0	1	2	Max current (mA)	7.5	30	15	Relative max (%)	25	100	50	DAC resolution (bits)	6	8	7	Tap allocation	Precursor	Main tap	Postcursor	Mode	FFE mode select bits of "Transmit Driver Mode Control Register" for Port x	FFE taps activated	FFE2	"00"	0, 1	FFE3	"01"	0, 1, 2	(Reserved)	"10"	(Indeterminate)	Hi-Z	"11"	None (see Sect. 2.2.4.1)
Tap coefficient #	0	1	2																																	
Max current (mA)	7.5	30	15																																	
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(Reserved)	"10"	(Indeterminate)																																		
Hi-Z	"11"	None (see Sect. 2.2.4.1)																																		

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O. DEPENDENT CLAIM 15

Claim 15	Stauffer
15. The communications link of claim 14, wherein the controller saves updated coefficient values in one of the registers.	Stauffer discloses and/or renders obvious this limitation. “The HSS EX10 transmitter includes a feed forward equalization (FFE) to reduce inter-symbol interference (ISI) at the receiver. This pre-emphasis technique uses a FIR filter to compensate for the high frequency roll-off of the transmission channel. Control inputs are provided to allow adjustment of the river FFE filter coefficients on a per-port basis. The following equation describes the relationships of the FFE Coefficients. $H(Z) = K (C0 z +1 + C1 z 0+ C2 z -1)$ This Z-transform equation describes an FFE with three taps, including one pre and one post tap. Other cores may have FFEs with fewer or more taps.” Stauffer, 58. “The driver amplitude (K) is adjustable in the range of 0 – 1,320 (nominal) mV peak-to-peak differential using the Transmit Power Register described previously in this chapter. The relative weights and polarities of C0 to C2 are configured using the three Transmit TapX Coefficient Registers (X = 0, 1, 2), and the Transmit Polarity Register. The actual range of relative coefficient weights is defined in Table 2.12.” Stauffer, 58. “The resolution of the levels is also indicated in Table 2.12, with each tap having equal bit weighting. The driver circuit design enforces a constant driver output power for any combination of coefficients and polarities, provided the sum of coefficients C0 – C2 is 63 or higher (power decreases proportionally below this sum). As coefficients are initialized or updated, the logic calculates the appropriate internal amplitude (K) to maintain the overall output power at the level defined in the Transmit Power register.” Stauffer, 58.

Exhibit C-11

Claim 15	Stauffer																																			
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(Reserved)	"10"	(Indeterminate)																																		
Hi-Z	"11"	None (see Sect. 2.2.4.1)																																		

Exhibit C-11

Claim 15	Stauffer
	before the Apply Load bit is pulsed, the old values are read. (The value of the Slow Slew Control field of the Transmit Driver Mode Control Register is applied to the analog circuits immediately, and is not gated by the Apply Load bit.)” Stauffer, 59. “For cores which do not contain internal registers, filter coefficients may be set using input control pins. Sequencing updated values onto these pins is the responsibility of the chip designer.” Stauffer, 59. “FFE coefficient values are not intended to be changed dynamically while data is being transmitted (except as part of a speed negotiation or link optimization process). Significant changes to the TX slice configuration can cause loss of data at the receiver until such time as the receiver adapts to the new waveform characteristics.” Stauffer, 59. “Higher speed protocol standards sometimes support negotiation of transmitter FFE settings based on characteristics of the signal at the receiver. IEEE 802.3ap Backplane Ethernet is an example of such an application. Implementations of such applications must update FFE coefficients in response to a full duplex training protocol by reading and writing the corresponding registers.” Stauffer, 59. “The training protocol used for Backplane Ethernet is introduced in Sect. 5.3.5.1. Some cores provide register control signals to more easily implement the actions defined by this protocol, which include incrementing/decrementing coefficient values. Such features are not defined for the HSS EX10 core.”

Exhibit C-11

Claim 15	Stauffer
	Stauffer, 59. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

Exhibit C-11

P. INDEPENDENT CLAIM 16

Claim 16	Stauffer
16[pre] A pluggable module transceiver including:	To the extent the preamble is limiting, Stauffer discloses and/or renders obvious this limitation. “The XGXS PCS sublayer performs 8B/10B encoding and decoding of MAC frames. Each byte of data maps to a corresponding 10-bit symbol. In addition, the XGMII control characters in Table 5.12, with the exception of the Idle character, directly map to corresponding 10-bit symbols. This mapping is shown in Table 5.12 using the symbol nomenclature for 8B/10B codes. (The 8B/10B block code was described in Sect. 4.2.2.1.)” Stauffer, 207. “XGMII Idles are randomly converted to one of the following 10-bit codes: Sync (K28.5), Skip (K28.0), or Align (K28.3). A LFSR is used to randomly either generate Sync or Skip symbols. Align symbols are inserted at randomized intervals in the range of 16–31 symbols, with this interval also determined by a LFSR. The same symbol is transmitted on all lanes.” Stauffer, 207. “Align symbols are used by the receive PCS logic to perform deskew across all lanes of the interface such that the XGMII RXD[31:0] output is aligned to a common clock domain. The Align symbol is unique and does not otherwise occur in the protocol. Since it is transmitted on all lanes simultaneously, and is only transmitted every 16–31 symbols, the lanes can be deskewed by aligning the occurrence of this symbol.” Stauffer, 207. “Skip symbols are used by the receive PCS logic to adjust for frequency differences between the recovered receive clock and the local XGMII clock. Skip symbols are inserted or dropped as needed.”

Exhibit C-11

Claim 16	Stauffer
	Stauffer, 207. “The Sequence symbol (K28.4) is used on lane 0, in conjunction with Dxx.y symbols on the other lanes, to convey management information. Such information is inserted by the MAC layer between frames in place of Idles, and is conveyed through the XGXS accordingly.” Stauffer, 207. “The 10-Gb Serial Electrical Interface (XFI) was developed as part of the 10-Gigabit Small Form Factor Pluggable (XFP) Multi Source Agreement (MSA). This MSA was developed by a consortium of optics module vendors who agreed to source optics modules meeting the XFP requirements. The XFI is a 10-Gbps serial electrical interface for communications between the XFP module and a SONET framer chip, or an Ethernet PCS/PMA layer. The PCS and PMA sublayers defined in clauses 49 and 51, respectively, define the necessary functions to interface between XGMII and XFI, and are used with all 10-Gb Ethernet serial variants (including backplane applications using the PMD defined in clause 72). Although the XFI acronym does not appear anywhere in the IEEE 802.3 standard, for historical reasons implementations of clause 49 and 51 are commonly called XFI.” Stauffer, 207-08. “The XFI PCS encodes and serializes the XGMII transmit data (TXD/TXC signals) for transmission on XFI. Each XGMII lane is 64B/66B encoded, scrambled, serialized, and transmitted at a baud rate of 10.3125 Gbps. XFI serial data signals received by the XFI PCS are deserialized, descrambled, 64B/66B decoded, and then driven to the MAC or PHY on the XGMII receive data (RXD/RXC signals). XFI is a full duplex interface consisting of one transmit and one receive serial data signals.” Stauffer, 208. “An optional 16-bit bus is defined to interface between the PCS sublayer and the PMA sublayer. While this

Exhibit C-11

Claim 16	Stauffer
	is the reference interface between the XFI PCS and the HSS core implementing the PMA sublayer as defined by clause 49, it does require data to be transferred on the parallel bus of the HSS core at 644.53 Mtransfers per second. Implementations may choose HSS core options which utilize more bits of parallel data at a slower transfer rate. (Available IBM cores use a 32-bit interface.) The definition of this interface has significance for two reasons: • The 66-bit code word blocks produced by 64B/66B encoding of the XGMII data are not an integer multiple of the width of the parallel data bus on most HSS cores. Data must be steered from cycle to cycle by “gearbox” logic in order to map the 66-bit blocks onto the 16-bit (or 2-bit) parallel data bus of the HSS core. • 10GBASE-W Wide Area Network (WAN) variants are intended to interoperate with other network nodes on a SONET/SDH network. These variants define a WAN Interface Sublayer (WIS) in clause 50 which maps the Ethernet packets into a SONET SPE, and then wraps this data with SONET/SDH overhead bytes with the level of support defined in clause 50. WIS is sandwiched between the PCS and PMA sublayers for 10GBASE-W variants.” Stauffer, 208. “There are three significant features associated with Backplane Ethernet which are not used in other Ethernet variants. These features are: • Training protocol (defined in Clause 72 for 10GBASE-KR) • Autonegotiation (defined in Clause 73 for all Backplane Ethernet variants) • Forward error correction (FEC) (defined in Clause 74 for optional use with 10GBASE-KR)” Stauffer, 213. To the extent that this preamble is not disclosed, either explicitly or inherently, by Stauffer, this preamble is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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Claim 16	Stauffer
16[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to a port transceiver; and	Stauffer discloses and/or renders obvious this limitation. “The XGXS PCS sublayer performs 8B/10B encoding and decoding of MAC frames. Each byte of data maps to a corresponding 10-bit symbol. In addition, the XGMII control characters in Table 5.12, with the exception of the Idle character, directly map to corresponding 10-bit symbols. This mapping is shown in Table 5.12 using the symbol nomenclature for 8B/10B codes. (The 8B/10B block code was described in Sect. 4.2.2.1.)” Stauffer, 207. “XGMII Idles are randomly converted to one of the following 10-bit codes: Sync (K28.5), Skip (K28.0), or Align (K28.3). A LFSR is used to randomly either generate Sync or Skip symbols. Align symbols are inserted at randomized intervals in the range of 16–31 symbols, with this interval also determined by a LFSR. The same symbol is transmitted on all lanes.” Stauffer, 207. “Align symbols are used by the receive PCS logic to perform deskew across all lanes of the interface such that the XGMII RXD[31:0] output is aligned to a common clock domain. The Align symbol is unique and does not otherwise occur in the protocol. Since it is transmitted on all lanes simultaneously, and is only transmitted every 16–31 symbols, the lanes can be deskewed by aligning the occurrence of this symbol.” Stauffer, 207. “Skip symbols are used by the receive PCS logic to adjust for frequency differences between the recovered receive clock and the local XGMII clock. Skip symbols are inserted or dropped as needed.” Stauffer, 207.

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Claim 16	Stauffer
	“The Sequence symbol (K28.4) is used on lane 0, in conjunction with Dxx.y symbols on the other lanes, to convey management information. Such information is inserted by the MAC layer between frames in place of Idles, and is conveyed through the XGXS accordingly.” Stauffer, 207. “The 10-Gb Serial Electrical Interface (XFI) was developed as part of the 10-Gigabit Small Form Factor Pluggable (XFP) Multi Source Agreement (MSA). This MSA was developed by a consortium of optics module vendors who agreed to source optics modules meeting the XFP requirements. The XFI is a 10-Gbps serial electrical interface for communications between the XFP module and a SONET framer chip, or an Ethernet PCS/PMA layer. The PCS and PMA sublayers defined in clauses 49 and 51, respectively, define the necessary functions to interface between XGMII and XFI, and are used with all 10-Gb Ethernet serial variants (including backplane applications using the PMD defined in clause 72). Although the XFI acronym does not appear anywhere in the IEEE 802.3 standard, for historical reasons implementations of clause 49 and 51 are commonly called XFI.” Stauffer, 207-08. “The XFI PCS encodes and serializes the XGMII transmit data (TXD/TXC signals) for transmission on XFI. Each XGMII lane is 64B/66B encoded, scrambled, serialized, and transmitted at a baud rate of 10.3125 Gbps. XFI serial data signals received by the XFI PCS are deserialized, descrambled, 64B/66B decoded, and then driven to the MAC or PHY on the XGMII receive data (RXD/RXC signals). XFI is a full duplex interface consisting of one transmit and one receive serial data signals.” Stauffer, 208. “An optional 16-bit bus is defined to interface between the PCS sublayer and the PMA sublayer. While this is the reference interface between the XFI PCS and the HSS core implementing the PMA sublayer as

Exhibit C-11

Claim 16	Stauffer
	defined by clause 49, it does require data to be transferred on the parallel bus of the HSS core at 644.53 Mtransfers per second. Implementations may choose HSS core options which utilize more bits of parallel data at a slower transfer rate. (Available IBM cores use a 32-bit interface.) The definition of this interface has significance for two reasons: • The 66-bit code word blocks produced by 64B/66B encoding of the XGMII data are not an integer multiple of the width of the parallel data bus on most HSS cores. Data must be steered from cycle to cycle by “gearbox” logic in order to map the 66-bit blocks onto the 16-bit (or 2-bit) parallel data bus of the HSS core. • 10GBASE-W Wide Area Network (WAN) variants are intended to interoperate with other network nodes on a SONET/SDH network. These variants define a WAN Interface Sublayer (WIS) in clause 50 which maps the Ethernet packets into a SONET SPE, and then wraps this data with SONET/SDH overhead bytes with the level of support defined in clause 50. WIS is sandwiched between the PCS and PMA sublayers for 10GBASE-W variants.” Stauffer, 208. “There are three significant features associated with Backplane Ethernet which are not used in other Ethernet variants. These features are: • Training protocol (defined in Clause 72 for 10GBASE-KR) • Autonegotiation (defined in Clause 73 for all Backplane Ethernet variants) • Forward error correction (FEC) (defined in Clause 74 for optional use with 10GBASE-KR)” Stauffer, 213. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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Claim 16	Stauffer
16[b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model,	Stauffer discloses and/or renders obvious this limitation. “Many of the TX slice parameter control registers are not effective immediately after being written. Application of register values to the analog circuits is controlled by writing the Apply Load bit in the Transmit Coefficient Control Register. This allows the FFE and power level configuration to be completely loaded in the individual registers and then simultaneously applied to the analog circuits. For the HSS EX10, the values loaded into the Transmit TapX Coefficient Registers, the Transmit Power Register, the Transmit Polarity Register, and the FFE Mode Select field of the Transmit Driver Mode Control Register are not applied to the analog circuits until the Apply Load bit is pulsed. The read-back value of these registers reflects the value being applied to the analog circuits. If these registers are written and then read before the Apply Load bit is pulsed, the old values are read. (The value of the Slow Slew Control field of the Transmit Driver Mode Control Register is applied to the analog circuits immediately, and is not gated by the Apply Load bit.)” Stauffer, 59. “For cores which do not contain internal registers, filter coefficients may be set using input control pins. Sequencing updated values onto these pins is the responsibility of the chip designer.” Stauffer, 59. “FFE coefficient values are not intended to be changed dynamically while data is being transmitted (except as part of a speed negotiation or link optimization process). Significant changes to the TX slice configuration can cause loss of data at the receiver until such time as the receiver adapts to the new waveform characteristics.” Stauffer, 59.

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Claim 16	Stauffer																				
	“Higher speed protocol standards sometimes support negotiation of transmitter FFE settings based on characteristics of the signal at the receiver. IEEE 802.3ap Backplane Ethernet is an example of such an application. Implementations of such applications must update FFE coefficients in response to a full duplex training protocol by reading and writing the corresponding registers.” Stauffer, 59. “The training protocol used for Backplane Ethernet is introduced in Sect. 5.3.5.1. Some cores provide register control signals to more easily implement the actions defined by this protocol, which include incrementing/decrementing coefficient values. Such features are not defined for the HSS EX10 core.” Stauffer, 59. “The tap ranges and resolutions for the HSS EX10 FFE circuit were described in Table 2.12, and this table is repeated in Table 3.1. In a nonequalized case, the main tap provides 100% of the driver output amplitude. As shown in the table, this limit corresponds to the maximum current that this tap can provide. Limits for other taps were chosen after empirical studies of equalization solutions for a variety of channel design examples.” Stauffer, 109. Table 3.1 Transmitter FFE summary <table><tr><th><i>Tap coefficient #</i></th><th><i>0</i></th><th><i>1</i></th><th><i>2</i></th></tr><tr><td>Max current (mA)</td><td>7.5</td><td>30</td><td>15</td></tr><tr><td>Relative max (%)</td><td>25</td><td>100</td><td>50</td></tr><tr><td>DAC resolution (bits)</td><td>6</td><td>8</td><td>7</td></tr><tr><td>Tap allocation</td><td>Precursor</td><td>Main tap</td><td>Postcursor</td></tr></table>	<i>Tap coefficient #</i>	<i>0</i>	<i>1</i>	<i>2</i>	Max current (mA)	7.5	30	15	Relative max (%)	25	100	50	DAC resolution (bits)	6	8	7	Tap allocation	Precursor	Main tap	Postcursor
<i>Tap coefficient #</i>	<i>0</i>	<i>1</i>	<i>2</i>																		
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Relative max (%)	25	100	50																		
DAC resolution (bits)	6	8	7																		
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Claim 16	Stauffer
	“Figure 3.9 illustrates a simplified generic FFE example. A simplified halfrate FFE architecture is shown in Fig. 3.9a, and is representative of the circuit in Fig. 3.8. This example explores a two-tap FFE case (i.e., FFE Mode Select set to “FFE2” in the Transmit Driver Mode Control Register as described in Table 2.6). The cursor and postcursor taps are set at +0.8 and – 0.2, respectively. Figure 3.9b illustrates the various signal waveforms and the resulting FFE output. The Serial Data or x(t) signal in Fig. 3.9b is the serial data input to the FFE circuit. The x(t–T) and –x(t–T) signals are noninverted and inverted polarities of the original signal delayed by one-bit time. Finally, the Tx OUT or y(t) signal is the Tx Output waveform, and can be expressed by the following mathematical summation: $Tx\ Out = y(t) = 0.8\ x(t) - 0.2\ x(t - T)$, (3.1) where the signals y(t), x(t), and x(t–T) were defined above, and T is one-bit time (or 1 UI).” Stauffer, 109. “There are three significant features associated with Backplane Ethernet which are not used in other Ethernet variants. These features are: • Training protocol (defined in Clause 72 for 10GBASE-KR) • Autonegotiation (defined in Clause 73 for all Backplane Ethernet variants) • Forward error correction (FEC) (defined in Clause 74 for optional use with 10GBASE-KR)” Stauffer, 213. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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Claim 16	Stauffer
16[c] the controller using one of the registers to set initial coefficient values for the one or more transmit filters.	Stauffer discloses and/or renders obvious this limitation. “Many of the TX slice parameter control registers are not effective immediately after being written. Application of register values to the analog circuits is controlled by writing the Apply Load bit in the Transmit Coefficient Control Register. This allows the FFE and power level configuration to be completely loaded in the individual registers and then simultaneously applied to the analog circuits. For the HSS EX10, the values loaded into the Transmit TapX Coefficient Registers, the Transmit Power Register, the Transmit Polarity Register, and the FFE Mode Select field of the Transmit Driver Mode Control Register are not applied to the analog circuits until the Apply Load bit is pulsed. The read-back value of these registers reflects the value being applied to the analog circuits. If these registers are written and then read before the Apply Load bit is pulsed, the old values are read. (The value of the Slow Slew Control field of the Transmit Driver Mode Control Register is applied to the analog circuits immediately, and is not gated by the Apply Load bit.)” Stauffer, 59. “For cores which do not contain internal registers, filter coefficients may be set using input control pins. Sequencing updated values onto these pins is the responsibility of the chip designer.” Stauffer, 59. “FFE coefficient values are not intended to be changed dynamically while data is being transmitted (except as part of a speed negotiation or link optimization process). Significant changes to the TX slice configuration can cause loss of data at the receiver until such time as the receiver adapts to the new waveform characteristics.” Stauffer, 59.

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Claim 16	Stauffer																				
	“Higher speed protocol standards sometimes support negotiation of transmitter FFE settings based on characteristics of the signal at the receiver. IEEE 802.3ap Backplane Ethernet is an example of such an application. Implementations of such applications must update FFE coefficients in response to a full duplex training protocol by reading and writing the corresponding registers.” Stauffer, 59. “The training protocol used for Backplane Ethernet is introduced in Sect. 5.3.5.1. Some cores provide register control signals to more easily implement the actions defined by this protocol, which include incrementing/decrementing coefficient values. Such features are not defined for the HSS EX10 core.” Stauffer, 59. “The tap ranges and resolutions for the HSS EX10 FFE circuit were described in Table 2.12, and this table is repeated in Table 3.1. In a nonequalized case, the main tap provides 100% of the driver output amplitude. As shown in the table, this limit corresponds to the maximum current that this tap can provide. Limits for other taps were chosen after empirical studies of equalization solutions for a variety of channel design examples.” Stauffer, 109. Table 3.1 Transmitter FFE summary <table><tr><td><i>Tap coefficient #</i></td><td><i>0</i></td><td><i>1</i></td><td><i>2</i></td></tr><tr><td>Max current (mA)</td><td>7.5</td><td>30</td><td>15</td></tr><tr><td>Relative max (%)</td><td>25</td><td>100</td><td>50</td></tr><tr><td>DAC resolution (bits)</td><td>6</td><td>8</td><td>7</td></tr><tr><td>Tap allocation</td><td>Precursor</td><td>Main tap</td><td>Postcursor</td></tr></table>	<i>Tap coefficient #</i>	<i>0</i>	<i>1</i>	<i>2</i>	Max current (mA)	7.5	30	15	Relative max (%)	25	100	50	DAC resolution (bits)	6	8	7	Tap allocation	Precursor	Main tap	Postcursor
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Exhibit C-11

Claim 16	Stauffer
	“Figure 3.9 illustrates a simplified generic FFE example. A simplified halfrate FFE architecture is shown in Fig. 3.9a, and is representative of the circuit in Fig. 3.8. This example explores a two-tap FFE case (i.e., FFE Mode Select set to “FFE2” in the Transmit Driver Mode Control Register as described in Table 2.6). The cursor and postcursor taps are set at +0.8 and – 0.2, respectively. Figure 3.9b illustrates the various signal waveforms and the resulting FFE output. The Serial Data or $x(t)$ signal in Fig. 3.9b is the serial data input to the FFE circuit. The $x(t-T)$ and $-x(t-T)$ signals are noninverted and inverted polarities of the original signal delayed by one-bit time. Finally, the Tx OUT or $y(t)$ signal is the Tx Output waveform, and can be expressed by the following mathematical summation: $Tx\ Out = y(t) = 0.8\ x(t) - 0.2\ x(t - T)$, (3.1) where the signals $y(t)$, $x(t)$, and $x(t-T)$ were defined above, and T is one-bit time (or 1 UI).” Stauffer, 109. “There are three significant features associated with Backplane Ethernet which are not used in other Ethernet variants. These features are: • Training protocol (defined in Clause 72 for 10GBASE-KR) • Autonegotiation (defined in Clause 73 for all Backplane Ethernet variants) • Forward error correction (FEC) (defined in Clause 74 for optional use with 10GBASE-KR)” Stauffer, 213. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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Q. DEPENDENT CLAIM 17

Claim 17	Stauffer
17. The pluggable module transceiver of claim 16, wherein the port transceiver determines a performance characteristic for each register.	Stauffer discloses and/or renders obvious this limitation. “The HSS EX10 transmitter includes a feed forward equalization (FFE) to reduce inter-symbol interference (ISI) at the receiver. This pre-emphasis technique uses a FIR filter to compensate for the high frequency roll-off of the transmission channel. Control inputs are provided to allow adjustment of the river FFE filter coefficients on a per-port basis. The following equation describes the relationships of the FFE Coefficients. $H(Z) = K (C0 z +1 + C1 z 0+ C2 z -1)$ This Z-transform equation describes an FFE with three taps, including one pre and one post tap. Other cores may have FFEs with fewer or more taps.” Stauffer, 58. “The driver amplitude (K) is adjustable in the range of 0 – 1,320 (nominal) mV peak-to-peak differential using the Transmit Power Register described previously in this chapter. The relative weights and polarities of C0 to C2 are configured using the three Transmit TapX Coefficient Registers (X = 0, 1, 2), and the Transmit Polarity Register. The actual range of relative coefficient weights is defined in Table 2.12.” Stauffer, 58. “The resolution of the levels is also indicated in Table 2.12, with each tap having equal bit weighting. The driver circuit design enforces a constant driver output power for any combination of coefficients and polarities, provided the sum of coefficients C0 – C2 is 63 or higher (power decreases proportionally below this sum). As coefficients are initialized or updated, the logic calculates the appropriate internal amplitude (K) to maintain the overall output power at the level defined in the Transmit Power register.” Stauffer, 58.

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Claim 17	Stauffer																																			
	Table 2.12 Transmitter FFE summary <table><tr><td>Tap coefficient #</td><td>0</td><td>1</td><td>2</td></tr><tr><td>Max current (mA)</td><td>7.5</td><td>30</td><td>15</td></tr><tr><td>Relative max (%)</td><td>25</td><td>100</td><td>50</td></tr><tr><td>DAC resolution (bits)</td><td>6</td><td>8</td><td>7</td></tr><tr><td>Tap allocation</td><td>Precursor</td><td>Main tap</td><td>Postcursor</td></tr></table> Table 2.13 Transmit driver modes <table><tr><td>Mode</td><td>FFE mode select bits of "Transmit Driver Mode Control Register" for Port x</td><td>FFE taps activated</td></tr><tr><td>FFE2</td><td>"00"</td><td>0, 1</td></tr><tr><td>FFE3</td><td>"01"</td><td>0, 1, 2</td></tr><tr><td>(Reserved)</td><td>"10"</td><td>(Indeterminate)</td></tr><tr><td>Hi-Z</td><td>"11"</td><td>None (see Sect. 2.2.4.1)</td></tr></table> “The XGXS PCS sublayer performs 8B/10B encoding and decoding of MAC frames. Each byte of data maps to a corresponding 10-bit symbol. In addition, the XGMII control characters in Table 5.12, with the exception of the Idle character, directly map to corresponding 10-bit symbols. This mapping is shown in Table 5.12 using the symbol nomenclature for 8B/10B codes. (The 8B/10B block code was described in Sect. 4.2.2.1.)” Stauffer, 207.	Tap coefficient #	0	1	2	Max current (mA)	7.5	30	15	Relative max (%)	25	100	50	DAC resolution (bits)	6	8	7	Tap allocation	Precursor	Main tap	Postcursor	Mode	FFE mode select bits of "Transmit Driver Mode Control Register" for Port x	FFE taps activated	FFE2	"00"	0, 1	FFE3	"01"	0, 1, 2	(Reserved)	"10"	(Indeterminate)	Hi-Z	"11"	None (see Sect. 2.2.4.1)
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Claim 17	Stauffer
	“XGMII Idles are randomly converted to one of the following 10-bit codes: Sync (K28.5), Skip (K28.0), or Align (K28.3). A LFSR is used to randomly either generate Sync or Skip symbols. Align symbols are inserted at randomized intervals in the range of 16–31 symbols, with this interval also determined by a LFSR. The same symbol is transmitted on all lanes.” Stauffer, 207. “Align symbols are used by the receive PCS logic to perform deskew across all lanes of the interface such that the XGMII RXD[31:0] output is aligned to a common clock domain. The Align symbol is unique and does not otherwise occur in the protocol. Since it is transmitted on all lanes simultaneously, and is only transmitted every 16–31 symbols, the lanes can be deskewed by aligning the occurrence of this symbol.” Stauffer, 207. “Skip symbols are used by the receive PCS logic to adjust for frequency differences between the recovered receive clock and the local XGMII clock. Skip symbols are inserted or dropped as needed.” Stauffer, 207. “The Sequence symbol (K28.4) is used on lane 0, in conjunction with Dxx.y symbols on the other lanes, to convey management information. Such information is inserted by the MAC layer between frames in place of Idles, and is conveyed through the XGXS accordingly.” Stauffer, 207. “The 10-Gb Serial Electrical Interface (XFI) was developed as part of the 10-Gigabit Small Form Factor Pluggable (XFP) Multi Source Agreement (MSA). This MSA was developed by a consortium of optics module vendors who agreed to source optics modules meeting the XFP requirements. The XFI is a 10-Gbps serial electrical interface for communications between the XFP module and a SONET framer chip, or

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Claim 17	Stauffer
	an Ethernet PCS/PMA layer. The PCS and PMA sublayers defined in clauses 49 and 51, respectively, define the necessary functions to interface between XGMII and XFI, and are used with all 10-Gb Ethernet serial variants (including backplane applications using the PMD defined in clause 72). Although the XFI acronym does not appear anywhere in the IEEE 802.3 standard, for historical reasons implementations of clause 49 and 51 are commonly called XFI.” Stauffer, 207-08. “The XFI PCS encodes and serializes the XGMII transmit data (TXD/TXC signals) for transmission on XFI. Each XGMII lane is 64B/66B encoded, scrambled, serialized, and transmitted at a baud rate of 10.3125 Gbps. XFI serial data signals received by the XFI PCS are deserialized, descrambled, 64B/66B decoded, and then driven to the MAC or PHY on the XGMII receive data (RXD/RXC signals). XFI is a full duplex interface consisting of one transmit and one receive serial data signals.” Stauffer, 208. “An optional 16-bit bus is defined to interface between the PCS sublayer and the PMA sublayer. While this is the reference interface between the XFI PCS and the HSS core implementing the PMA sublayer as defined by clause 49, it does require data to be transferred on the parallel bus of the HSS core at 644.53 Mtransfers per second. Implementations may choose HSS core options which utilize more bits of parallel data at a slower transfer rate. (Available IBM cores use a 32-bit interface.) The definition of this interface has significance for two reasons: • The 66-bit code word blocks produced by 64B/66B encoding of the XGMII data are not an integer multiple of the width of the parallel data bus on most HSS cores. Data must be steered from cycle to cycle by “gearbox” logic in order to map the 66-bit blocks onto the 16-bit (or 2-bit) parallel data bus of the HSS core. • 10GBASE-W Wide Area Network (WAN) variants are intended to interoperate with other network nodes on a SONET/SDH network. These variants define a WAN Interface Sublayer (WIS) in clause 50 which maps the Ethernet packets into a SONET SPE, and then wraps this data with SONET/SDH overhead bytes with the level of support defined in clause 50. WIS is sandwiched between the PCS and PMA sublayers for 10GBASE-W variants.”

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Claim 17	Stauffer
	Stauffer, 208. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

Exhibit C-11

R. DEPENDENT CLAIM 18

Claim 18	Stauffer
18. The pluggable module transceiver of claim 17, wherein the performance characteristic is an error signal energy.	Stauffer discloses and/or renders obvious this limitation. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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S. DEPENDENT CLAIM 19

Claim 19	Stauffer
19. The pluggable module transceiver of claim 17, wherein the performance characteristic is a bit error rate.	Stauffer discloses and/or renders obvious this limitation. “The XGXS PCS sublayer performs 8B/10B encoding and decoding of MAC frames. Each byte of data maps to a corresponding 10-bit symbol. In addition, the XGMII control characters in Table 5.12, with the exception of the Idle character, directly map to corresponding 10-bit symbols. This mapping is shown in Table 5.12 using the symbol nomenclature for 8B/10B codes. (The 8B/10B block code was described in Sect. 4.2.2.1.)” Stauffer, 207. “XGMII Idles are randomly converted to one of the following 10-bit codes: Sync (K28.5), Skip (K28.0), or Align (K28.3). A LFSR is used to randomly either generate Sync or Skip symbols. Align symbols are inserted at randomized intervals in the range of 16–31 symbols, with this interval also determined by a LFSR. The same symbol is transmitted on all lanes.” Stauffer, 207. “Align symbols are used by the receive PCS logic to perform deskew across all lanes of the interface such that the XGMII RXD[31:0] output is aligned to a common clock domain. The Align symbol is unique and does not otherwise occur in the protocol. Since it is transmitted on all lanes simultaneously, and is only transmitted every 16–31 symbols, the lanes can be deskewed by aligning the occurrence of this symbol.” Stauffer, 207. “Skip symbols are used by the receive PCS logic to adjust for frequency differences between the recovered receive clock and the local XGMII clock. Skip symbols are inserted or dropped as needed.”

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Claim 19	Stauffer
	Stauffer, 207. “The Sequence symbol (K28.4) is used on lane 0, in conjunction with Dxx.y symbols on the other lanes, to convey management information. Such information is inserted by the MAC layer between frames in place of Idles, and is conveyed through the XGXS accordingly.” Stauffer, 207. “The 10-Gb Serial Electrical Interface (XFI) was developed as part of the 10-Gigabit Small Form Factor Pluggable (XFP) Multi Source Agreement (MSA). This MSA was developed by a consortium of optics module vendors who agreed to source optics modules meeting the XFP requirements. The XFI is a 10-Gbps serial electrical interface for communications between the XFP module and a SONET framer chip, or an Ethernet PCS/PMA layer. The PCS and PMA sublayers defined in clauses 49 and 51, respectively, define the necessary functions to interface between XGMII and XFI, and are used with all 10-Gb Ethernet serial variants (including backplane applications using the PMD defined in clause 72). Although the XFI acronym does not appear anywhere in the IEEE 802.3 standard, for historical reasons implementations of clause 49 and 51 are commonly called XFI.” Stauffer, 207-08. “The XFI PCS encodes and serializes the XGMII transmit data (TXD/TXC signals) for transmission on XFI. Each XGMII lane is 64B/66B encoded, scrambled, serialized, and transmitted at a baud rate of 10.3125 Gbps. XFI serial data signals received by the XFI PCS are deserialized, descrambled, 64B/66B decoded, and then driven to the MAC or PHY on the XGMII receive data (RXD/RXC signals). XFI is a full duplex interface consisting of one transmit and one receive serial data signals.” Stauffer, 208. “An optional 16-bit bus is defined to interface between the PCS sublayer and the PMA sublayer. While this

Exhibit C-11

Claim 19	Stauffer
	is the reference interface between the XFI PCS and the HSS core implementing the PMA sublayer as defined by clause 49, it does require data to be transferred on the parallel bus of the HSS core at 644.53 Mtransfers per second. Implementations may choose HSS core options which utilize more bits of parallel data at a slower transfer rate. (Available IBM cores use a 32-bit interface.) The definition of this interface has significance for two reasons: • The 66-bit code word blocks produced by 64B/66B encoding of the XGMII data are not an integer multiple of the width of the parallel data bus on most HSS cores. Data must be steered from cycle to cycle by “gearbox” logic in order to map the 66-bit blocks onto the 16-bit (or 2-bit) parallel data bus of the HSS core. • 10GBASE-W Wide Area Network (WAN) variants are intended to interoperate with other network nodes on a SONET/SDH network. These variants define a WAN Interface Sublayer (WIS) in clause 50 which maps the Ethernet packets into a SONET SPE, and then wraps this data with SONET/SDH overhead bytes with the level of support defined in clause 50. WIS is sandwiched between the PCS and PMA sublayers for 10GBASE-W variants.” Stauffer, 208. To the extent that this limitation is not disclosed, either explicitly or inherently, by Stauffer, this limitation is obvious to a person of ordinary skill in the art based on (1) Stauffer alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.