

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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BOE Technology Group Co., Ltd.,  
Petitioner,

v.

Paneltouch Technologies LLC,  
Patent Owner.

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U.S. Patent No. 9,250,758  
Original Issue Date: February 2, 2016  
Title: DISPLAY DEVICE WITH TOUCH PANEL

Case No. IPR2025-01245

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**DECLARATION OF DR. VIVEK SUBRAMANIAN**

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**CHALLENGED CLAIM LISTING**

| <b>Claim</b> | <b>Limitation No.</b> | <b>Limitation</b>                                                                                                                                                                                                                                                                                                                                                                                               |
|--------------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1            | [1-PRE]               | A display device with a touch panel comprising:                                                                                                                                                                                                                                                                                                                                                                 |
|              | [1-A]                 | the touch panel including a first substrate having a detection area to detect a coordinate and an outside area in which at least one external terminal is formed, a plurality of first lines to detect the coordinate in the detection area, a plurality of second lines to detect the coordinate in the detection area, each of the plurality of first lines traversing each of the plurality of second lines; |
|              | [1-B]                 | an organic emitting display panel under the touch panel; and                                                                                                                                                                                                                                                                                                                                                    |
|              | [1-C]                 | a circular polarizing plate arranged at a side of the touch panel opposite to the organic emitting display panel;<br>wherein the organic emitting display panel, the touch panel, and the circular polarizing plate are arranged in this order.                                                                                                                                                                 |
| 2            | 2                     | A display device with a touch panel according to claim 1, wherein each of the plurality of second lines and the plurality of first lines is made of metal; and<br><br>wherein each of the plurality of first lines is black in color.                                                                                                                                                                           |
| 3            | 3                     | A display device with a touch panel according to claim 2, wherein the touch panel includes a plurality of wiring groups;<br><br>wherein each of plurality of wiring groups has some of the first lines; and<br><br>wherein some of the first lines in each of plurality of wiring groups are bonded with each other.                                                                                            |
| 4            | 4                     | A display device with a touch panel according to claim 3, wherein a transparent conductive film overlays the plurality of the first lines, and wherein the transparent conductive film is electrically connected to the plurality of the first lines.                                                                                                                                                           |

| <b>Claim</b> | <b>Limitation No.</b> | <b>Limitation</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------------|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5            | 5                     | A display device with a touch panel according to claim 3, wherein a transparent conductive film underlays the plurality of the first lines, and wherein the transparent conductive film is electrically connected to the plurality of the first lines.                                                                                                                                                                                                                                                                                                                  |
| 6            | 6                     | A display device with a touch panel according to claim 2, wherein a transparent conductive film overlays the plurality of the second lines; and wherein the transparent conductive film is electrically connected to the plurality of the second lines.                                                                                                                                                                                                                                                                                                                 |
| 7            | 7                     | A display device with a touch panel according to claim 2, wherein a transparent conductive film underlays the plurality of the second lines, and wherein the transparent conductive film is electrically connected to the plurality of the second lines.                                                                                                                                                                                                                                                                                                                |
| 8            | 8                     | A display device with a touch panel according to claim 1, wherein the touch panel is a resistance-film-type touch panel.                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 9            | 9                     | <p>A display device with a touch panel according to claim 1, further including:</p> <ul style="list-style-type: none"> <li>a first adhesive layer between the touch panel and the organic emitting display panel; and</li> <li>a second adhesive layer between the touch panel and the circular polarizing plate;</li> </ul> <p>wherein the touch panel and the organic emitting display panel are fixed with each other by the first adhesive layer, and the touch panel and the circular polarizing plate are fixed with each other by the second adhesive layer.</p> |

## I. INTRODUCTION

I, Dr. Vivek Subramanian, declare as follows:

1. I have been retained by counsel for BOE Technology Group Co., Ltd., (“BOE”) in the above-captioned *inter partes* review as an independent consultant to offer opinions regarding the validity of the challenged claims in U.S. Patent No. 9,250,758 (the “’758 Patent”).

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration – supplemented with my own knowledge and experience in the field. Should new materials, analyses, or opinions be introduced subsequent to the filing of this Declaration, I reserve the right to provide supplementary Declarations to the extent necessary to address any such newly introduced items.

3. If requested, I am prepared to explain in a deposition or at a trial before the Patent Trial and Appeal Board (the “Board”) the technology disclosed in the ’758 Patent, including the state of the art around 2009, the earliest alleged priority date of the ’758 Patent. Similarly, I am prepared to explain the technology disclosed in the prior art references cited herein. This may include, among other things, background information on the fields of display devices and touch panels.

## II. QUALIFICATIONS

4. My qualifications to testify as an expert in display devices and touch

panels are set forth in my *curriculum vitae*, attached as Appendix A. I have decades of experience as an engineer, scientist, and consultant in the display devices and touch panel fields. I am currently a Professor of Electrical and Microengineering at Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland and director of the micromanufacturing science and engineering research center. I moved to EPFL in 2018. I was previously a professor at the University of California, Berkeley for almost 20 years, and am still maintaining an adjunct professorship appointment there while I graduate my remaining PhD students. I also previously served as a founding technical advisor for Kovio, Inc. which developed thin film transistor technology for various applications, including RFID tags and displays.

5. I received a Ph.D. in electrical engineering from Stanford University in 1998. I received my MS in electrical engineering from Stanford in 1996, and my BS in electrical engineering from Louisiana State University, Baton Rouge, in 1994. My PhD thesis was specifically focused on the development of technology for displays. During my PhD, I was the recipient of an Eastman Kodak fellowship. As part of this award, I worked closely with Kodak on their OLED technology.

6. After completing my Ph.D., I held multiple jobs simultaneously. First, I was a founder and member of technical staff of Matrix Semiconductor (“Matrix”), which developed high density memory. We founded Matrix in 1997,

and I maintained a full-time role through 2000, at which point I transitioned to an advisory role. Matrix was acquired by Sandisk in 2005, at which point my affiliation with Matrix ended. Between 1998 and 2000, I was also a visiting research engineer at the University of California, Berkeley, where I performed research on high-performance transistors and process technology. In that same period, I was also a consulting assistant professor at Stanford University, where I performed research on 3D integration of transistors, among other topics. In 2000, I was offered a professorship at Berkeley, and moved there full time. I received tenure in 2005, and became a full professor in 2011. In 2018, I was awarded with a Chancellor's professorship. In 2018, I also accepted a position at EPFL, and between 2018 and 2020, I maintained dual appointments at Berkeley and EPFL while I completed my move.

7. My professional career has been focused heavily on semiconductor and display technology, and I have been actively involved in the development of process technology for displays and touch screens for a large part of my professional career, both in academia and in industry. I have specifically been involved in the development of thin film transistor technology for displays, development of materials and processes for OLEDs, and development of printing technology for display fabrication. I have also worked specifically on touch screen technology; as an example, I taught the main electrical engineering course at

Berkeley that dealt with touch screens, and introduced a touch screen lab into the curriculum. At EPFL, I have continued in this vein, and continue to teach the main course on large area and flexible electronics, which includes extensive teaching on displays.

8. I have authored or co-authored more than 200 publications in journals and major international conference proceedings, many of which are specifically related to displays, touch screens, and the associated thin film technologies.

9. My *curriculum vitae* contains further details regarding my experience, education, publications, and other qualifications that qualify me to render expert opinions in connection with this proceeding.

### **III. COMPENSATION**

10. I am being compensated for my work in this matter at an hourly rate of \$700 for consulting services.

11. My compensation is not contingent upon the opinions I render or the outcome of this proceeding.

### **IV. MATERIALS CONSIDERED**

12. In preparing this declaration, I reviewed and considered the following materials, along with any others referenced in the body of my declaration:

- The '758 Patent (Ex. 1001) and its file history (Ex. 1002).
- U.S. Patent Publication No. 2008/0303798 A1 ("**Nakamura**") (Ex.

1004)

- U.S. Patent Publication No. 2008/0246741 A1 (“**Hinata ’741**”) (Ex. 1005)
- U.S. Patent No. 9,639,229, which is related to the ’758 Patent, and its file history (excerpted as Ex. 1006)
- Japanese Patent No. JP-A-2002-342014 (“**Takaya**”) (Ex. 1007)
- U.S. Patent No. 8,803,836, which is related to the ’758 Patent, and its file history (excerpted as Ex. 1008)
- U.S. Patent Publication No. 2009/0096763 A1 (“**Hinata ’763**”) (Ex. 1009)

13. I may use these documents and information, or other information obtained during the course of this proceeding, as well as representative charts, graphs, schematics and diagrams, animations, and models based on those documents and information, to support and to explain my testimony.

14. My opinions are based in part on a review and analysis of the above-mentioned documents and materials. I have also drawn on my education, experience, and knowledge of basic engineering and scientific principles in forming my opinions.

## V. UNDERSTANDING OF THE LAW

### A. Legal Standards

15. I am not an attorney, but I have been informed of several legal principles, which I have employed in forming my opinions in this declaration. I have been informed and understand that each patent claim is considered separately

for purposes of validity and that a dependent claim that depends from another claim includes all of the limitations of the claim it depends from.

16. ***Claim Construction.*** I have been informed and understand that the claims of the challenged patents in this proceeding are to be construed using the same claim construction standard applied in district court. I have been informed and understand the claim construction analysis begins with the ordinary meaning of a claim term, and there is a presumption that the term carries its plain and ordinary meaning to persons of ordinary skill in the art as of the effective filing date of the patent. I have also been informed and understand that the most important sources for determining the meaning of a claim term are the claims, the specification, and the prosecution history of the patent at issue, which collectively is called “intrinsic evidence.” I have been further informed and understand that the meaning of a claim term may also be guided by “extrinsic evidence,” such as contemporaneous dictionaries and treatises.

17. **Burden of Proof.** I have been informed and understand that the petitioner in an *inter partes* review bears the burden of establishing invalidity by “a preponderance of the evidence.” I have been further informed and understand that, to prove an assertion by “a preponderance of the evidence,” the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

18. **Obviousness.** I have been informed and understand that a patent claim is invalid if it would have been obvious to a person of ordinary skill in the art at the time of the claimed invention. I have been further informed and understand that a claimed invention is not patentable if differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. I have been informed and understand that factors relevant to the determination of obviousness include the scope and content of the prior art, the level of ordinary skill in the art at the time of the invention, differences between the claimed invention and the prior art, and “secondary considerations” or objective indicia of non-obviousness.

19. I have been informed that a single reference alone can render a patent claim obvious, if any differences between the reference and the claim would have been known or obvious to a person of ordinary skill in the art (“POSITA”) at the

time of the invention. That is, if the POSITA could have adapted the reference to meet the claims of the patent by applying known concepts to achieve expected results, then the patent claims are rendered obvious by that reference.

20. I have been informed and understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have been further informed and understand that when a patent claim simply arranges old elements with each performing the same function it had been known to perform and yields no more than one of ordinary skill would expect from such an arrangement, the combination is obvious.

21. I have been informed and understand that a patent claim composed of several limitations is not obvious merely because each limitation was independently known in the prior art. Hindsight reasoning is not an appropriate basis for combining references to form an obviousness combination. I have been further informed and understand that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references.

22. I have been informed that various “secondary considerations” (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations must be considered as part of an obviousness analysis. I have been informed that even

strong evidence of secondary considerations may not be sufficient to rebut a strong showing of obviousness. I have been informed that the patentee bears the burden of showing the existence and effect of secondary considerations of non-obviousness, after which the burden of coming forward with rebuttal evidence shifts to the party arguing obviousness. I have been informed that the following secondary considerations may indicate non-obviousness:

- Copying: evidence that others, including the accused infringer, copied the patented invention.
- Long-standing problem or need: evidence of a persistent problem or need in the art that was resolved by the patented invention.
- Prior failure: evidence that others have tried and failed to solve the problem or failed to provide the need resolved by the claimed invention.
- Commercial acquiescence of competitors: the willingness of industry to license the patent at issue.
- Skepticism: evidence that those of ordinary skill in the art were skeptical as to the merits of the invention.
- Praise: evidence of praise directed to an invention by others in the field.
- Unexpected results: evidence that those of ordinary skill in the art were surprised by the capabilities of the claimed invention.

23. I have also been informed that the near-simultaneous invention by others can be evidence that a claimed invention is obvious. I have further been informed and understand that the patentee bears the burden of showing a “nexus”

between the claimed invention and the evidence proffered on secondary considerations (*e.g.*, proof of commercial success of a product that practices the claimed invention is not enough; there must be evidence that the commercial success resulted, at least in part, from the claimed invention).

**B. Priority Date**

24. I have been informed and understand that a U.S. patent may claim “priority” to the filing date of one or more earlier filed applications. I have been informed that the priority date, also called the “effective filing date,” is the earliest filing date to which a claim is entitled and that such date is relevant for determining what qualifies as prior art. I understand that a claim must have written description support in the application(s) to which it claims priority to be entitled to an earlier effective filing date. I have been informed that the priority date determination is done on a claim-by-claim basis and that claims in the same patent may have different priority dates.

**C. Level of Skill in the Art**

25. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art may have for combining references.

26. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art is also a person of ordinary creativity.

27. The challenged patent pertains generally to the fields of displays and touch panels. A person of ordinary skill in the art (“POSITA”) at the time of the alleged invention would have had at least a Bachelor’s degree in electrical engineering, or a similar discipline, along with 2-3 years of display and touch panel technology experience. Relevant experience can substitute for education and *vice versa*. I was at all relevant times at least a POSITA in the art relevant to the challenged patents.

## **VI. SUMMARY OF OPINIONS**

28. I have been asked to compare various prior art references to Claims 1-9 of the ’758 Patent (the “Challenged Claims”). In my opinion, the Challenged Claims are all unpatentable as obvious – based on these prior art references, combined with the knowledge of a POSITA.

29. My substantive analysis in Section X provides examples of why these

prior art references render the Challenged Claims unpatentable. I reserve the right to cite and rely on additional portions of these references in any future declarations or depositions.

## **VII. TECHNOLOGY BACKGROUND**

30. Before considering the '758 Patent in detail, some background on the technology of the '758 Patent should be considered.

31. Display devices having touch panels were well established by September 2009, building on the decades-old understanding of basic detection principles. The concept of using wired detection areas in one or more substrates to detect the coordinates where a user touches a touch screen was already well in place. The same is true of the display device and touch screen structures that were used to implement the concept.

32. For example, as I discuss in the following section, the '758 patent itself admits that detection methods ranging from light-based and electric characteristic-based concepts were all well known. Ex. 1001, 1:22-52, Figs. 20-21. This included extensive art relating to both resistive and capacitive sensing methods. *Id.* The '758 patent also repeatedly admits that the exact touch panel structure it claims had already been disclosed in Nakamura. *Id.*, 2:57-59, 4:57-60, 6:40-52.

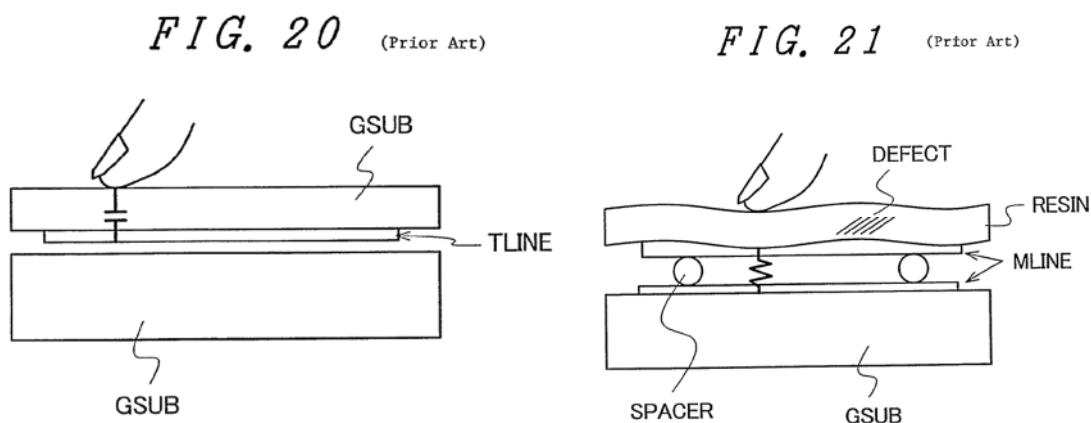
33. Thus, it was a crowded art by 2009, where the concepts employed in

the field were well understood, predictable, and routinely mixed and matched as needed to achieve a POSITA's design goals. The '758 patent itself admits that the particularities of such detection techniques—such as the exact structure its claimed display device and its touch panel—were all known and available for designers to choose from, as discussed throughout this Declaration. For example, I discuss the well-known practice of adhering display device components to each other using physically separate adhesion layers in Section X.B below.

### **VIII. THE '758 PATENT**

34. U.S. Patent No. 9,250,758 (“the '758 Patent” or “the Challenged Patent”) is entitled “Display Device With Touch Panel.” The '758 Patent claims priority to U.S. application 12/649,414, which was filed on December 30, 2009, and foreign application JP 2009-004874, which was filed on January 13, 2009. For purposes of this declaration, because I have been informed that the '758 Patent cannot rely on its foreign priority claim to overcome the prior art discussed in this Declaration, I have been instructed to use December 30, 2009 as the priority date of the '758 Patent. My opinions in this declaration were formed from the perspective of a POSITA as of December 30, 2009, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art. However, I also note that, if a January 13, 2009 priority date was instead employed for the '758 Patent, my opinions would not materially differ.

35. Display devices with touch panels were part of a crowded art by 2009. The art routinely utilized and adapted well understood and predictable detection methods in various structures. This understanding is reflected in the '758 Patent itself, as it admits that a wide variety of detection methods had already been “adopted by a conventional display device with a touch panel,” including light-based and electric characteristic-based detection methods. Ex. 1001, 1:22-31. The '758 Patent also admits that well-known prior art electric characteristic-based detection methods included both resistive detection, which works by detecting pressure applied to a touch panel, as well as capacitive sensing detection, which works by creating an electric field above the surface of the touch panel and detecting changes in the electric field caused by objects like a finger. *Id.*, 1:29-31. The '758 Patent provides example prior art capacitive and resistive sensing touch panel figures in its Figs. 20 and 21, respectively. *Id.*, 1:32-52, Figs. 20-21:



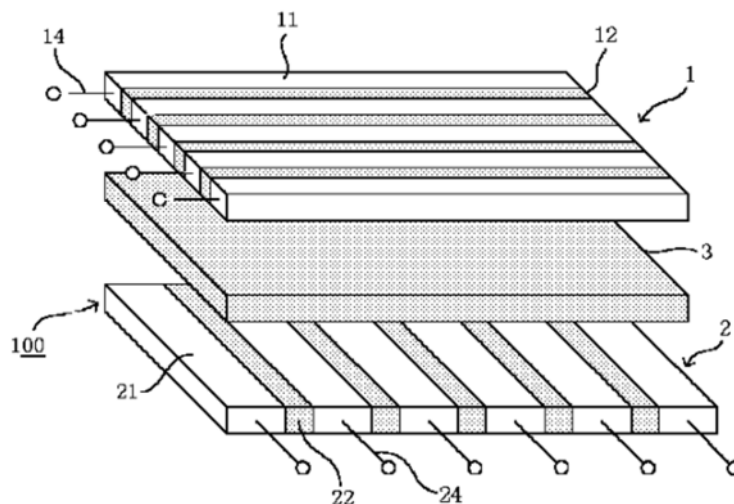
36. After its background discussion of resistive and capacitive sensing

touch panels, the rest of the '758 Patent focuses entirely on resistive sensing touch panels.

**A. Problem Addressed by the '758 Patent and the Alleged Invention**

37. As I have just discussed, the '758 Patent admits that touch panels, including resistive sensing touch panels, were already well-known. Despite this, the patent criticizes Japanese Patent No. JP-A-2002-342014 to Takaya ("Takaya"), which it says teaches a resistive sensing touch panel "in which a transparent electrode is formed into stripe-shaped electrodes and these stripe-shaped transparent electrodes are made [to] intersect with each other thus arranging intersecting portions in a matrix array." Ex. 1001, 1:53-59. While the '758 Patent does not provide precise citations or explain exactly what portion of Takaya's configuration it criticizes, it appears to take issue with the way electrodes 14 and electrodes 24 intersect with each other as shown in, *e.g.*, Fig. 1. Ex. 1007 (Takaya), Fig. 1:

【図 1】



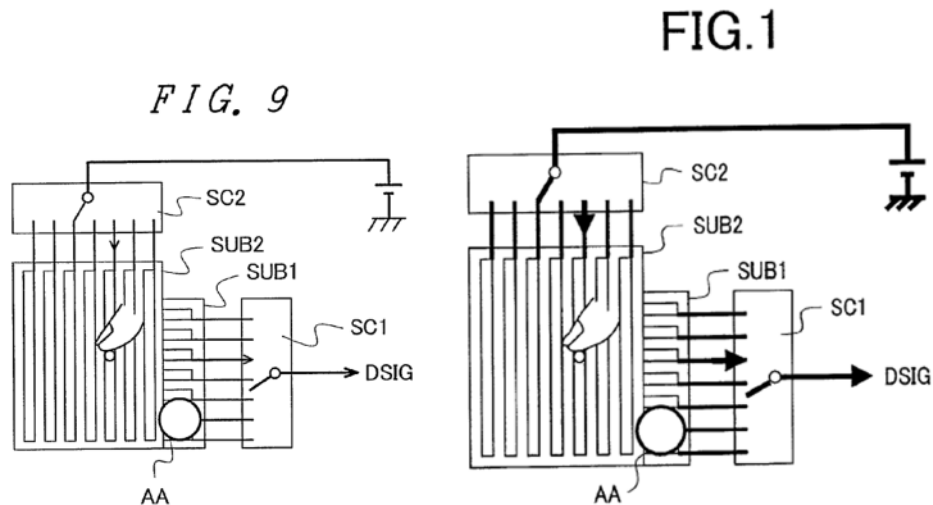
38. According to the '758 Patent, this “stripe-shaped” approach is undesirable due to its alleged inability to increase detection accuracy, which it says occurs due to the tradeoff between the need to decrease electrode line width and the corresponding increase in resistance this is said to cause. Ex. 1001, 1:63-2:2. The '758 Patent also criticizes Takaya because it is allegedly “difficult to decrease a gap between the transparent electrodes,” and for having contact positions that “are detected one-dimensionally,” which means that detection is “performed twice along an X axis and a Y axis.” *Id.*, 2:2-56.

39. Interestingly, after discussing these alleged issues in Takaya, the '758 Patent does not even claim to present a new solution to them. Rather, the patent states that the “applicants of the present application” had already “proposed a touch panel which adopts [a] new detection structure (Japanese Patent Application

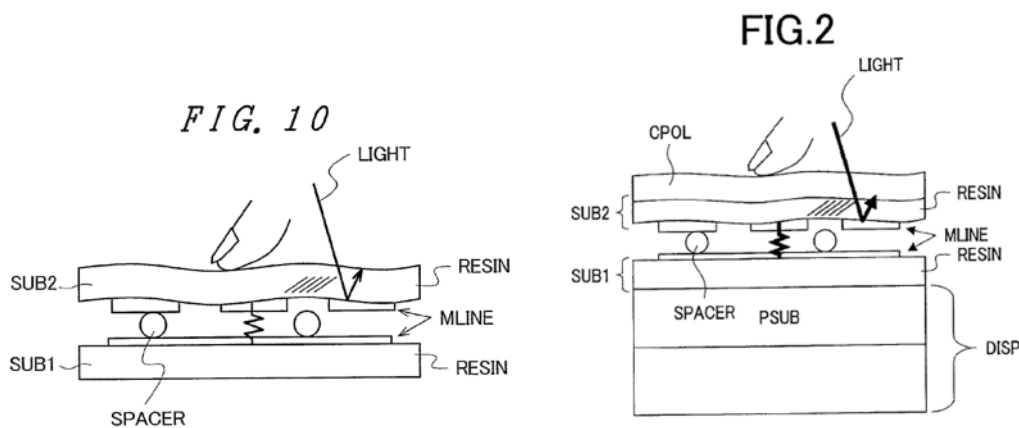
2007-149884)” that addresses these issues. *Id.*, 2:57-59. The ’758 Patent notes that it expressly adopts the structure already disclose presented in this prior application. *Id.*

40. This Japanese application that the ’758 Patent “adopts” is the foreign priority application for the Nakamura reference discussed throughout this Declaration. See Ex. 1004, [0001] (“The present application claims priority from Japanese application JP2007-149884 filed on Jun. 6, 2007, the content of which is hereby incorporated by reference into this application”), (30) (priority claim to same application).

41. The ’758 Patent reiterates several times that the details of the touch panel it discloses and claims, touch panel 10, is the same as the touch panel already described in Japanese Patent Application 2007-149884, *i.e.*, Nakamura. Ex. 1001, 4:57-59. This is also seen in comparing the ’758 Patent’s figures with Nakamura’s. For example, the preferred embodiment of the ’758 Patent’s touch panel is shown in its Fig. 9, which the ’758 Patent expressly states is copied from Nakamura: “FIG. 9 is a schematic plan view of the touch panel of this mode which adopts the touch panel described in” Nakamura. Ex. 1001 (’758 patent), 6:45-52, Fig. 9 (below left); Ex. 1004 (Nakamura), Fig. 1 (same figure, below right):



42. As another example, the figure comparison below shows how Nakamura had also already disclosed essentially the same cross-sectional view of the '758 Patent Fig. 10 embodiment, in greater detail than what is presented in the '758 Patent figure. Ex. 1001 ('758 patent), Fig. 10 (below left); Ex. 1004 (Nakamura), Fig. 1 (same figure with additional detail, below right):

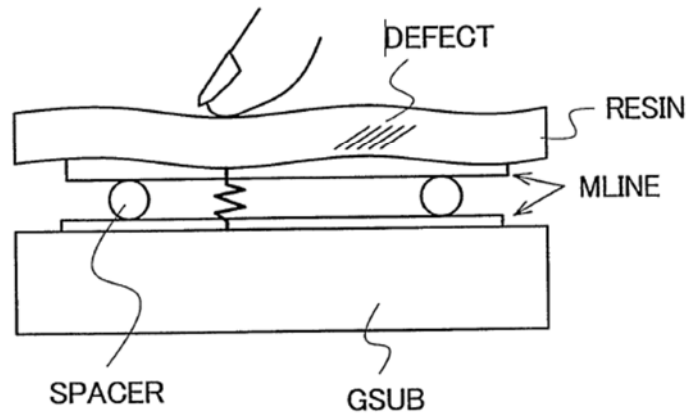


43. The '758 Patent thus admits that the exact “new detection structure” it presents to solve the alleged problems presented by Takaya had already been

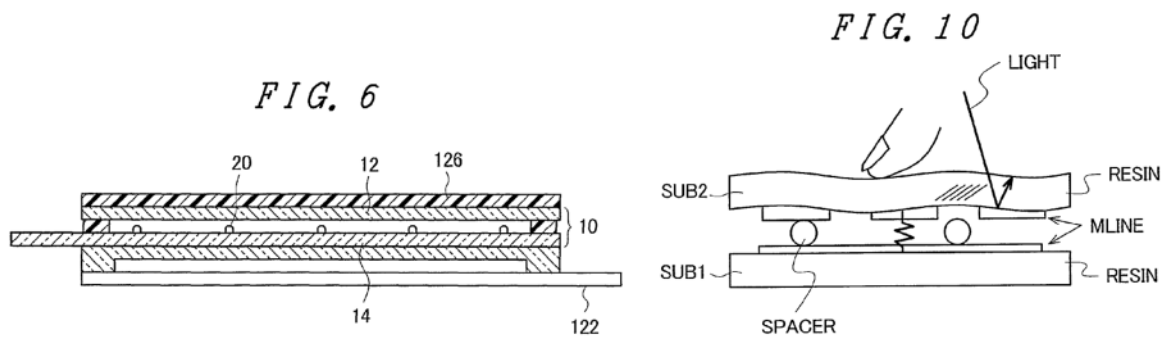
disclosed in Nakamura.

44. Without referencing any particular prior art, the '758 Patent states that “according to such a related art, since a plurality of lines are formed on a touch panel and hence, when a user moves a pen on an operation surface in a sliding manner, the user feels the surface unevenness.” Ex. 1001, 2:57-3:3. The '758 Patent complains that this “related art” prevents the user from experiencing an “excellent touch feeling.” *Id.* It then states that this “excellent touch feeling” is achieved by adding “a resin film which is adhered to the first substrate on a side opposite to the second substrate.” *Id.*, 3:14-16. It further states that, “[a]ccording to the present invention, the resin film is adhered to the touch panel, the uneven[n]ess attributed to the first electrode is absorbed and hence, the touch panel can give a user excellent touch feeling.” *Id.*, 3:16-19.

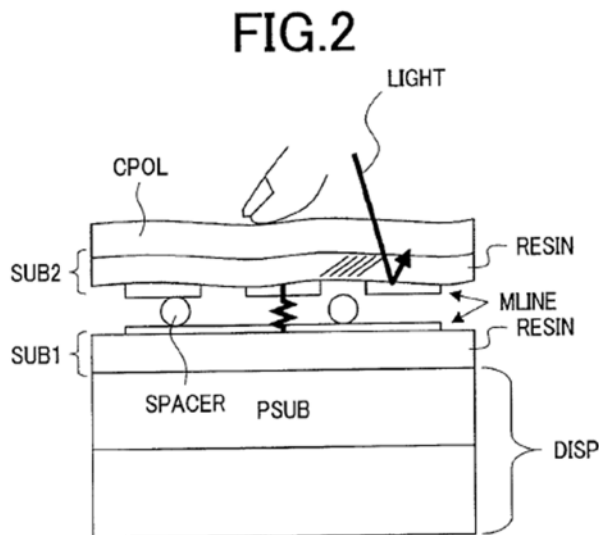
45. It appears that the '758 Patent is suggesting that in prior art systems, such as in the exemplary, “conventional” resistive sensing touch panel it shows in Fig. 21, the user would touch only a resin film, and so could feel the defects in the resin film. Ex. 1001, Fig. 21:

*FIG. 21* (Prior Art)

46. Apparently, the '758 Patent addresses this issue in “conventional” resistive sensing touch panels by having a touch panel that combines a resin film and a substrate, as in the touch panels of Figs. 6 and 10. Ex. 1001, Figs. 6, 10:



47. However, this distinction over “conventional” touch panels is not a distinction over Nakamura, which the '758 Patent admits had already disclosed this very same arrangement in its Fig. 2. Ex. 1004, Fig. 2:



48. The '758 Patent moves Nakamura's circular polarizing plate CPOL from its Fig. 10 embodiment to circular polarizing plate 126 in its Fig. 6 embodiment, without explaining why, but maintaining exactly the same arrangement as Nakamura's Fig. 2 in a differently styled figure. Ex. 1001, 5:52-63. *Compare* Ex. 1004 (Nakamura) Fig. 2 (circular polarizing plate CPOL arranged over touch panel comprising substrates SUB1 and SUB2, itself arranged over display panel DISP) with Ex. 1001 ('758 patent) Fig. 6 (circular polarizing plate 126 arranged over touch panel 10 comprising substrates 12 and 14, itself arranged over display panel 122). The '758 Patent's unexplained transference of the CPOL from one figure to another does not alter the fact that it still relies on the same touch panel structure already disclosed in Nakamura.

49. Thus, whatever advancement in "touch feeling" the '758 Patent is

referencing, that “advancement” had already been taught by Nakamura.

50. Indeed, the '758 Patent attributes its “excellent touch feeling” to “a resin film which is adhered to the first substrate on a side opposite to the second substrate,” which is precisely the resin film already disclosed in Nakamura’s Fig. 2. Ex. 1001, 3:14-16. The '758 Patent not only admits that such resin films were already disclosed in Nakamura, but even that they were already well-known in “conventional resistance-film-type panel[s].” Ex. 1001, 1:40-52, 6:45-52, Figs. 9, 21.

51. Further, looking beyond the '758 Patent specification’s statement that this resin film is the only alleged advancement over an unidentified “related art,” none of the claims in the '758 Patent recite such a concept. In fact, no claim even recites the word “resin” at all. Dependent claims 7 and 12-15 recite “a transparent conductive film” that overlays or underlays certain detection lines, but these claims do not relate to the allegedly novel resin film, but instead a “transparent electrode TLINE” that the '758 Patent itself admits was well disclosed by both “conventional” touch panels and Nakamura. Ex. 1001, 1:30-57, 8:51-9:15, 9:47-10:17, Figs. 12-13, 16-19, 20-21; *see also* Ex. 1004, [0007]-[0008], [0081]-[0089], [0098]-[0110], Figs. 4-5, 8-11, 13-14 (same disclosures in Nakamura). Similarly, while dependent claim 8 refers to a “resistance-film-type touch panel,” which is nothing more than a statement that the touch panel is a resistive sensing one, which

is again an admittedly “conventional” concept also taught by Nakamura. Ex. 1001, 1:29-59, Figs. 20-21; *see also* Ex. 1004, [0006]-[0008], [0068], [0080], Figs. 13-14.

52. The concepts the ’758 Patent does claim, such as substrate detection areas, display panels, and polarizing plates, are all concepts that the ’758 Patent’s specification itself expressly admits were already disclosed by the touch panel structure of Nakamura.

53. In other words, because the ’758 Patent itself admits that Nakamura had already taught the claimed touch panel structure, the claims are admittedly disclosed by Nakamura. This disclosure is confirmed throughout this Declaration.

**B. Prosecution History of the ’758 Patent**

54. The ’758 Patent was prosecuted in the United States as Application No. 14/451,769, and stems from foreign application JP 2009-004874 and U.S. application 12/649,414.

55. Despite the fact the ’758 Patent admits that Nakamura had already disclosed the touch panel structure it claims, the patent owner did not disclose Nakamura to the examiner in an information disclosure statement (“IDS”) during prosecution. *See generally* Ex. 1002.

56. During prosecution, the pending claims were subject to an obviousness-type double patenting rejection over the ’758 Patent’s parent patent,

U.S. Patent No. 8,803,836 (“the ’836 patent”). Ex. 1002, 5/6/2015 Office Action.

The patent owner responded by filing a terminal disclaimer, and the claims were then allowed. *Id.*, 8/4/2015 Response and Terminal Disclaimer; 9/28/2015 Notice of Allowance.

### C. Claim Construction

57. In my opinion, the claims of the ’758 Patent can be interpreted according to their ordinary meanings without construction for the purpose of this IPR.

58. While I do not believe that any claim construction is necessary here, I would like to make clear that, in my opinion, Claim 1 does **not** require a touch panel with first and second detection lines on “one and only one substrate.” For one thing, Claim 1 does not state that both sets of detection lines are adhered to the first substrate. Because Claim 1 is a “comprising” claim, it should cover touch panels that include additional substrates beyond the claimed first substrate.

59. The ’758 Patent family’s prosecution history further supports that this belief is correct. For example, during prosecution of the ’758 Patent parent ’836 Patent (during which Nakamura also was **not** disclosed by the patent owner in an IDS), the examiner initially rejected the pending claims over prior art including U.S. Patent Publication No. 2009/0096763 A1 (“Hinata ’763”). Ex. 1008 (’836

Patent File History), 12/12/2013 Office Action, pp. 3-8.

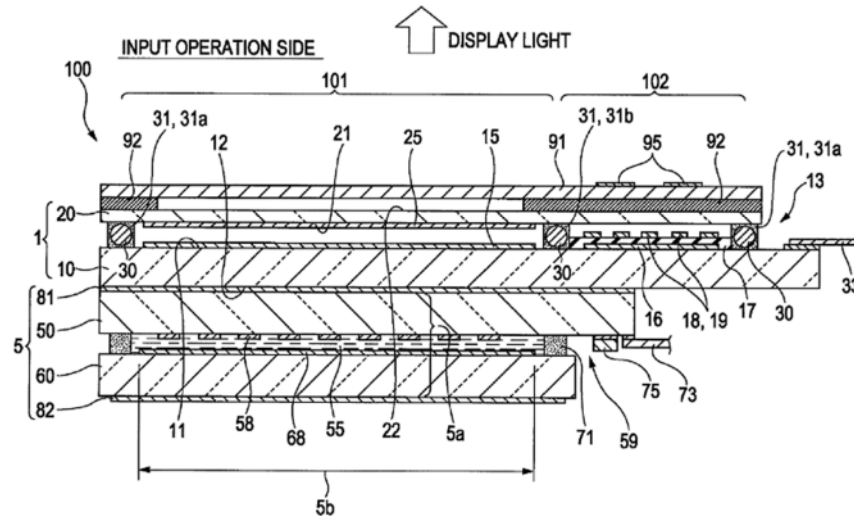
60. The patent owner added new independent Claim 8 to the '836 Patent, which is similar to '758 Patent Claim 1, and argued that Hinata '763 did not disclose “an organic luminescence electric device panel, wherein the organic luminescence electric device panel is adhered to the touch panel, and a circular polarizing plate is adhered to the touch panel at a side opposite to the organic luminescence organic electric device panel.” *Id.*, 3/11/2014 Amendment, pp. 3-4, 8-9.

61. The examiner allowed the claims over Hinata '763 after these amendments. *Id.*, 4/16/2015 Notice of Allowance.

62. The examiner thus maintained that Hinata '763 disclosed an '836 Patent claim element that—like '758 patent Claim 1 Element [1-A]—recites only a single “first substrate,” but two separate sets of detection lines (“first lines” and “second lines”). *Id.*, pp. 3-4. The examiner did so even though, like every embodiment in the '836 Patent's (and the '758 Patent's) specification embodiments, Hinata '763's touch panel discloses two separate substrates, each of which has its own set of detection lines. *See* Ex. 1009 (Hinata '763) Fig. 2 (depicting first electrode 15 formed on first substrate 10 opposite second electrode

25 formed on second substrate 20):

FIG. 2



*See also, e.g.,* Ex. 1001, 6:45-7:14, Figs. 9-10 (two-substrate structure in '758 patent).

63. The '836 Patent file history thus demonstrates an understanding between the patent owner and the examiner that the plain and ordinary meaning of its Claim 8 covers embodiments that contain two substrates, with the claimed “plurality of first lines” on a first substrate and the claimed “plurality of second lines” on a second substrate. This applies equally to '758 patent Claim 1 Element

[1-A].

64. The prosecution the '758 Patent's child '229 Patent further confirms this understanding. There, the examiner applied Hinata '763 against a version of pending Claim 1 that recited two substrates. Ex. 1006 ('229 Patent File History), 3/14/2016 Office Action, pp. 4-8. The patent then owner amended '229 Patent Claim 1 to, like '758 Patent Claim 1, recite only a single substrate. *Id.*, 6/14/2016 Amendment, pp. 2. After this amendment, the examiner continued to apply Hinata's two-substrate embodiment. *Id.*, 8/2/2016 Office Action, pp. 3-7.

65. Prosecution history aside, it is important that '758 Patent Claim 1 is satisfied by two-substrate embodiments. This is because every embodiment in the '758 Patent specification is, like Hinata, a two-substrate embodiment. *See, e.g.*, Ex. 1001, 6:45-7:14, Figs. 9-10 (two-substrate structure in '758 patent).

## **IX. THE PRIOR ART REFERENCES**

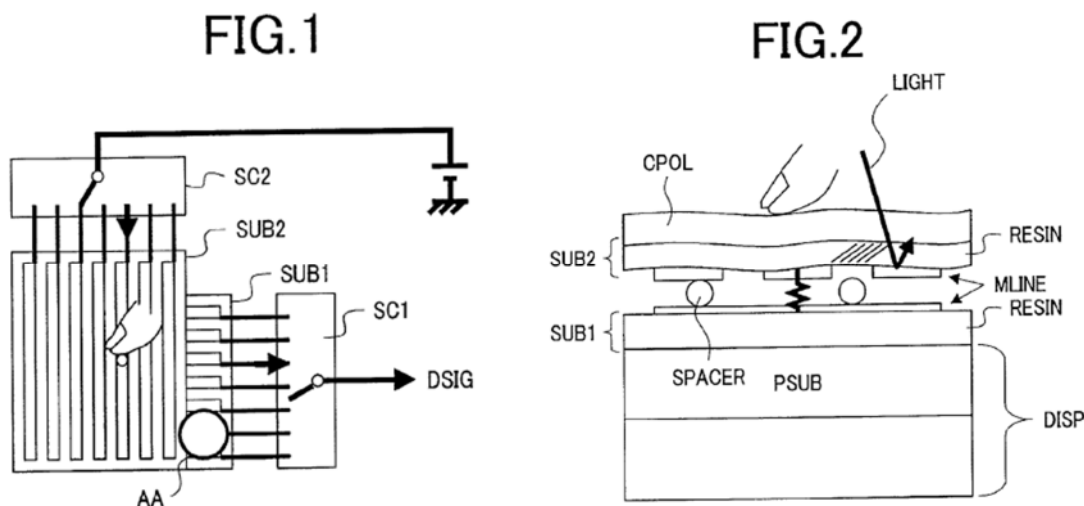
### **A. Nakamura**

66. Nakamura is titled "Display Device With Touch Panel," was published on December 11, 2008, filed on June 6, 2008, and claims priority to an application filed on June 6, 2007. Ex. 1004, (54), (43), (22), (30).

67. Nakamura relates to display devices that include touch panels that have particular structures. Ex. 1004, Abstract. Importantly, as I have just discussed, the '758 Patent admits several times that the exact touch panel structure

it claims had already been disclosed in Nakamura. Ex. 1001, 2:57-59, 4:57-60, 6:45-52.

68. Nakamura's Figs. 1 and 2 show schematic diagram and cross-sectional diagram views, respectively, of its preferred embodiment. Ex. 1004, Figs. 1-2:



See also Ex. 1001, Figs. 9-10 (substantially similar disclosure in '758 patent, with less detail in Fig. 10).

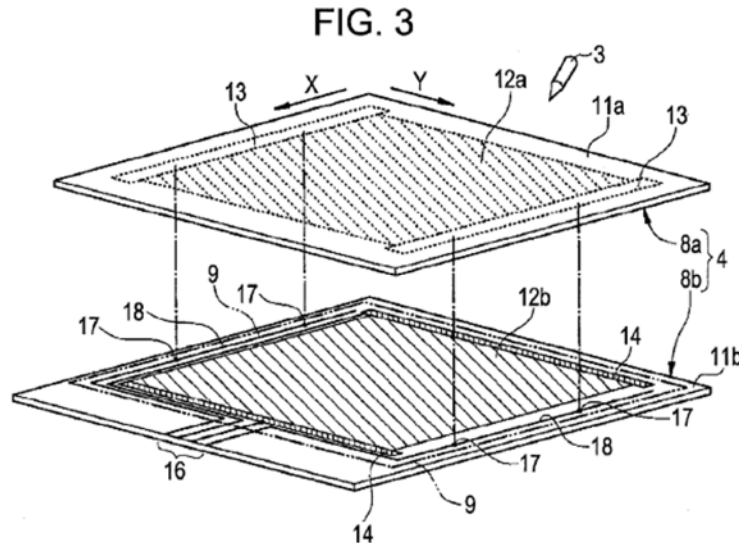
69. Nakamura's Figs. 1-2 show that its touch panel comprises two oppositely facing substrates, each arranged "so that their respective metal wirings face each other and that directions along which the respective metal wirings extend are made to intersect," a display panel, and a circularly polarizing plate CPOL. Ex. 1004, [0050]-[0055], Figs. 1-2; see also Ex. 1001, 6:45-7:14, Figs. 9-10 (substantially similar disclosure in '758 patent).

70. I discuss additional details regarding Nakamura's touch panels, which again are substantially similar to those of the '758 Patent, in the claim analysis section below.

**B. Hinata '741**

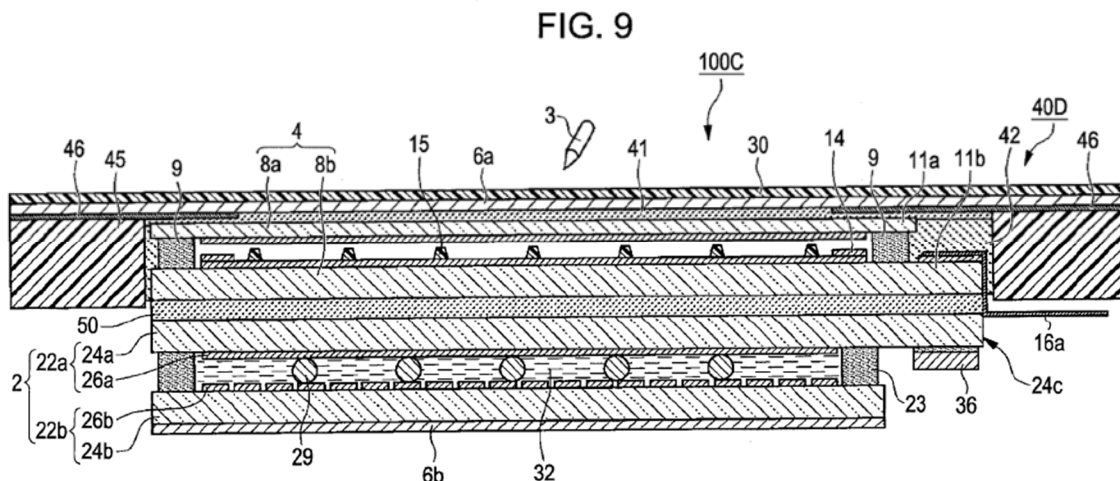
71. Hinata '741 is titled "Input Device, and Electro-Optical Device," was published on October 9, 2008, filed on March 7, 2008, and claims priority to applications filed on April 5, 2007. Ex. 1005, (54), (43), (22), (30).

72. Hinata '741 relates to input devices having displays and touch panels. *See, e.g.*, Ex. 1005, [0002]-[0006]. Hinata '741's Fig. 3 shows an exploded perspective view of one such touch panel. *Id.*, [0061], [0086], Fig. 3:



73. Hinata '741 teaches that the structure its touch panel can comprise can take on a number of embodiments, and that there are many different ways that its various components can be adhered together. *See, e.g.*, Ex. 1005, [0008]-[0009],

[0019]-[0022], [0030], [0048]-[0052], [0083], [0095]. Hinata '741's Fig. 9 shows one such embodiment. Ex. 1005, Fig. 9:



74. Hinata '741's Fig. 9 shows that this embodiment of its device uses a physically separate adhesive layer 41 that is located between the polarizing plate 6a and the touch panel 4. Ex. 1005, [0170]-[0178], Fig. 9. Similarly, the device uses a second physically separate adhesive layer 50 that is located between the display panel 2 and the touch panel 4. *Id.*

75. I note that display panel 2 is described as an LCD panel in these paragraphs. However, Hinata '741 notes elsewhere than an organic EL panel can be used rather than an LCD panel in any of its embodiments. *Id.*, [0029], [0056].

### **C. Motivation to Combine Nakamura and Hinata '741**

76. A POSITA would have found it obvious to combine Nakamura and Hinata '741 for many reasons.

77. For one thing, Nakamura and Hinata '741 are in the same field,

display device touch panels. Beyond that, both Nakamura and Hinata '741 disclose adhering a polarizing plate to one side of a touch panel as well as adhering an OLED display panel to the other side of the touch panel. *See, e.g.*, Ex. 1004 (Nakamura), [0055], Fig. 2; Ex. 1005 (Hinata '741), [0029], [0056], [0083], [0095], [0099], [0101], [0115]-[0116], [0147]-[0148], [0165]-[0168], [0170]-[0178], Fig. 9.

78. Additionally, both Nakamura and Hinata '741 are implemented in standard display panels using standard electrical principles. *See, e.g.*, Ex. 1004 (Nakamura), Abstract, [0002]-[0009], Figs. 13-14; Ex. 1005 (Hinata '741), [0005]-[0006], [0029], [0056]. Both Nakamura and Hinata '741 can be integrated into a variety of different devices, including cellular phones and televisions, and can comprise many different display types, including LCDs and OLEDs. Ex. 1004 (Nakamura), [0055], [0078], Fig. 12; Ex. 1005 (Hinata '741), [0029], [0056], [0279]. Further, both Nakamura and Hinata '741 disclose touch panels that detect touches using opposing surfaces, each having detection electrodes arranged along an x-y coordinate axis. *See, e.g.*, Ex. 1004 (Nakamura), [0003], [0051]-[0054], [0079], [0093], Figs. 1-2, 6; Ex. 1005 (Hinata '741), [0085]-[0087], [0104]-[0107], [0171], Figs. 3, 9. In view of this, a POSITA could have predictably and successfully combined Nakamura and Hinata '741 without undue experimentation.

79. I provide additional details regarding why a POSITA would have been

motivated to combine Nakamura and Hinata '741 to arrive at the relevant claim in Section X.B.1 below. For example, there I discuss how a POSITA would have been inspired to fix Nakamura's touch panel and organic emitting display panel with each other, and to fix Nakamura's touch panel and circular polarizing plate with each other, using physically separate adhesion layers in order to facilitate good adhesion between the layers over the large areas associated with typical displays / touch panels, using processes that were easy to implement and commonly used in the manufacture of the same.

## **X. INVALIDITY ANALYSIS**

80. As explained in detail in my analysis below, it is my conclusion and opinion that the Challenged Claims of the '758 Patent are invalid.

### **A. Ground 1 – Claims 1-8 Are Obvious Over Nakamura**

81. In my opinion, Nakamura renders Claims 1-8 of the '758 Patent obvious.

#### **1. Independent Claim 1**

82. In my opinion, Nakamura discloses and renders obvious Claim 1 of the '758 Patent.

##### **a) [1-PRE]**

83. In the event the Claim 1 preamble is found to be limiting, Nakamura discloses and renders obvious “[a] display device with a touch panel.”

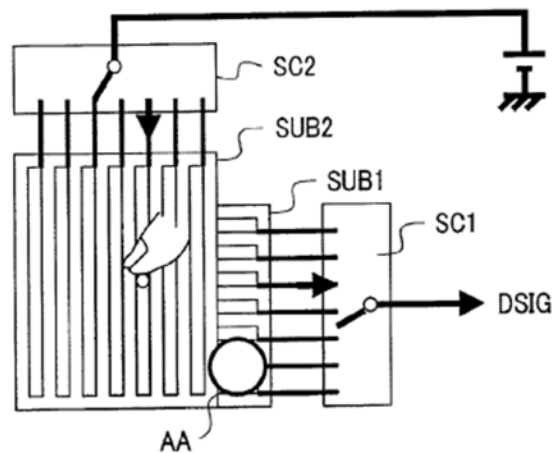
84. Nakamura repeatedly expressly discloses the exact verbiage of the preamble: a “display device with [a] touch panel.” *See, e.g.*, Ex. 1004, (54) (Title: “DISPLAY DEVICE WITH TOUCH PANEL”), Abstract, [0003], [0026], [0036], [0055].

**b) Element [1-A]**

85. Nakamura discloses and renders obvious this element of Claim 1: “the touch panel including a first substrate having a detection area to detect a coordinate and an outside area in which at least one external terminal is formed, a plurality of first lines to detect the coordinate in the detection area, a plurality of second lines to detect the coordinate in the detection area, each of the plurality of first lines traversing each of the plurality of second lines.”

86. Nakamura's Fig. 1 shows that its touch panel includes first substrate SUB1 and second substrate SUB2, and that both substrates include a detection area configured to detect a coordinate, as well as an outside area in which at least one external terminal is formed. Ex. 1004, [0051] (touch panel includes "a first peripheral circuit SC1, a second peripheral circuit SC2, a power supply, and a detection signal output terminal"), [0052], [0053] ("second peripheral circuit SC2 is connected to the second substrate SUB2, and selects the metal wiring line by line to input a voltage thereto from the power supply"), [0054] ("first peripheral circuit SC1 is connected to the first substrate SUB1, and selects the metal wiring line by line to detect a voltage therefrom"), Fig. 1:

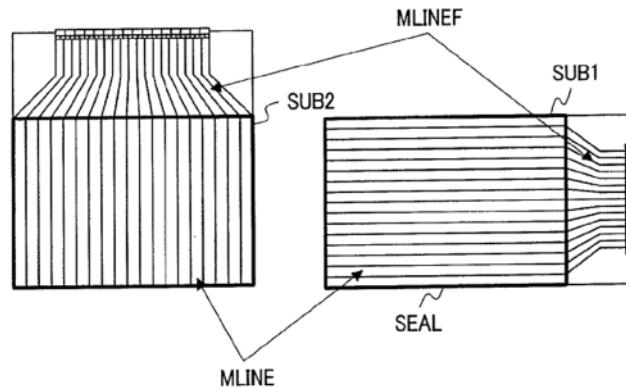
FIG. 1



87. I note that either of Nakamura's substrates SUB1 and SUB2 can be the "first substrate" claimed in Claim 1, which is the only substrate expressly recited in the claim. To prevent confusion, I will refer to the bottom substrate SUB1 as the exemplary claimed "first substrate" for the remainder of this claim. However, I expressly note that, in the alternative, the top substrate SUB1 can also be the claimed "first substrate" for this claim.

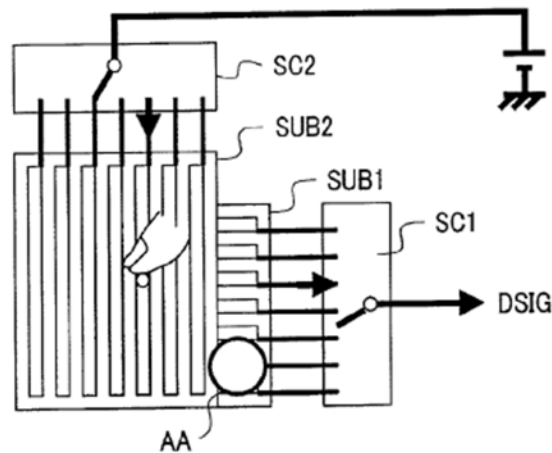
88. Nakamura goes on to discuss the detection areas and outside areas of its substrates in which at least one external terminal is formed several additional times. *See, e.g.*, Ex. 1004, [0079], [0083] (discussing the "detection area"), [0102] (same), [0105] (same), [0108] (same) [0095]-[0097] (discussing the "external terminals" and area "outside the detection area," including "the external terminals and wirings MLINEF extending up to the external terminals"), [0111], Fig. 7 (showing MLINE wiring in detection areas and MLINEF wiring connecting to external terminals in outside areas):

FIG. 7



89. As discussed throughout Nakamura's disclosure, its first substrate (*i.e.*, bottom substrate SUB1, or, in the alternative, top substrate SUB2) includes a plurality of first lines to detect a coordinate in the detection area, and its second substrate includes a plurality of second lines to detect the coordinate in the detection area. *See, e.g.*, Ex. 1004, [0003], [0079] ("The coordinate detection is performed on the metal wiring"), [0053] ("second peripheral circuit SC2 is connected to the second substrate SUB2, and selects the metal wiring line by line to input a voltage thereto from the power supply"), [0054] ("first peripheral circuit SC1 is connected to the first substrate SUB1, and selects the metal wiring line by line to detect a voltage therefrom"), [0111] ("In a case where the metal wiring is used as a wiring for the coordinate detection as in Wiring Layout Modes 1 to 9..."), Fig. 1:

FIG. 1



90. Nakamura's Figs. 1-2 additionally show that its first and second substrates "are arranged so that their respective metal wirings face each other and that directions along which the respective metal wirings extend are made to intersect," *i.e.*, its substrates are arranged so that each of the plurality of first lines traverse each of the plurality of second lines. Ex. 1004, [0052], Figs. 1-2:

FIG. 1

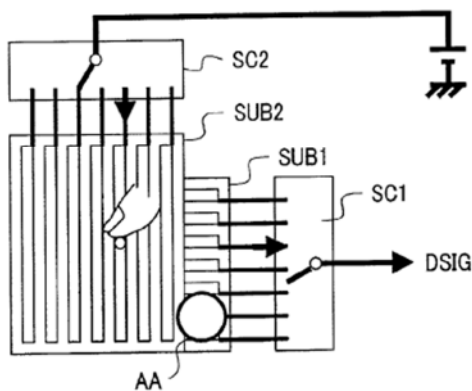
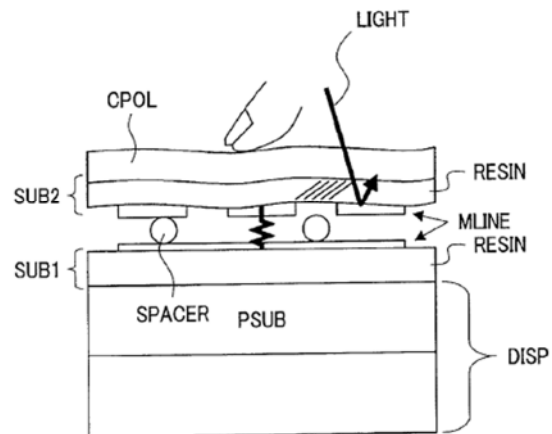
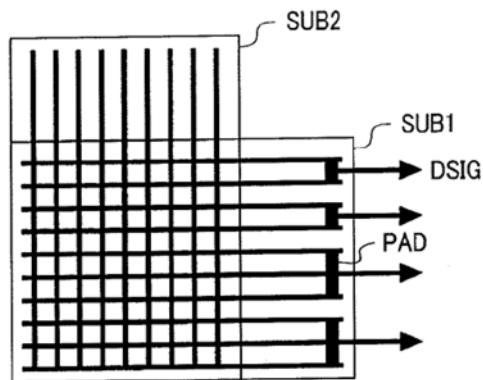


FIG. 2



See also [0093], Fig. 6:

FIG.6



91. I note that the disclosure of this concept in the '758 Patent is substantially similar to this disclosure in Nakamura, to the extent that the '758 Patent expressly “adopts” Nakamura in discussing it. *See, e.g.*, Ex. 1001, 6:45-7:14, Figs. 9-10 (two-substrate structure in '758 patent).

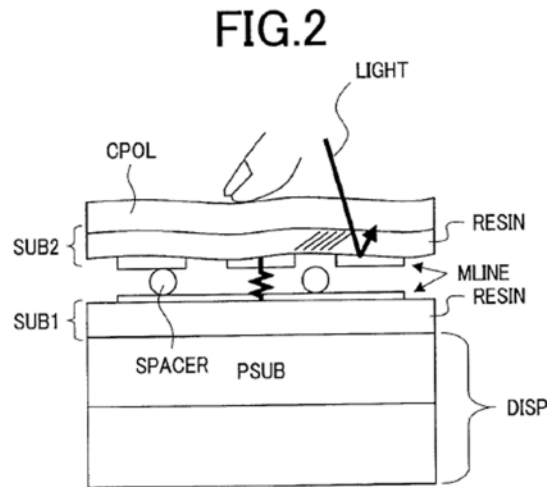
92. For at least these reasons, Nakamura discloses and renders obvious a touch panel that includes a first substrate having a detection area to detect a coordinate and an outside area in which at least one external terminal is formed, a plurality of first lines to detect the coordinate in the detection area, a plurality of second lines to detect the coordinate in the detection area, each of the plurality of

first lines traversing each of the plurality of second lines.

**c) Element [1-B]**

93. Nakamura discloses and renders obvious this element of Claim 1: “an organic emitting display panel under the touch panel.”

94. Nakamura’s Fig. 2 shows that “the touch panel of FIG. 1 is bonded to a surface of a display panel,” and the “display device with the touch panel includes a display panel substrate PSUB composing a display device DISP, the first substrate SUB1, the second substrate SUB2, a spacer SPACER, and a circularly polarizing plate CPOL.” Ex. 1004, [0055], Fig. 2:



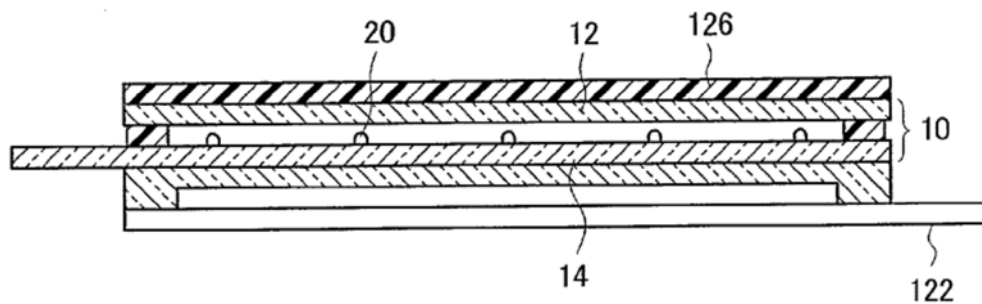
95. Nakamura explains that “[t]he display panel substrate PSUB” constitutes “a display-surface-side substrate similar to a counter substrate of a liquid crystal display device and a sealing substrate of a top emission organic EL display device.” Ex. 1004, [0055]. Nakamura’s “top emission organic EL display device” panel is “an organic emitting display panel.” Specifically, a POSITA would have known that EL is an acronym for electroluminescent, and indeed, therefore, an organic emitting display panel is an organic electroluminescent display device. The use of the phrase “top emission” in Nakamura further confirms this understanding, since it makes clear that the display is an emissive element, again exactly as is an organic “emitting” display panel.

96. OLEDs like Nakamura’s organic EL display were well-known display devices in 2009. POSITAs at the time understood that the selection of one type of well-known display device, such as a liquid crystal display or OLED display, was an obvious and routine one that they could implement as they chose based on the design needs of their system.

97. Nakamura also explains that “[t]he first substrate SUB1 is adhered onto the display panel substrate PSUB.” Ex. 1004, [0055]. In other words, as Nakamura’s Fig. 2 shows, the organic emitting display panel (*i.e.*, the organic EL display device) is located under the touch panel (*i.e.*, under the first substrate portion of the touch panel). *Id.*, Fig. 2.

98. I note that the disclosure of this concept in the '758 Patent is substantially similar to this disclosure in Nakamura. See Ex. 1001, 5:52-63, Fig. 6 (showing same arrangement of “circular polarizing plate” 126, “touch panel” 10 comprising substrates 12 and 14, and “organic EL display panel” 122):

*FIG. 6*



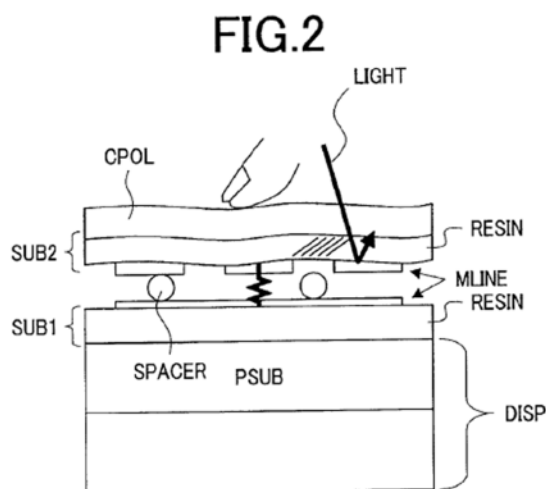
99. As confirmation of this, during the prosecution of the '758 Patent's child '229 Patent, the examiner expressly applied Nakamura against similar claim language. Ex. 1006 ('229 File History), 8/2/2016 Office Action, pp. 7-8. The examiner also stated that Nakamura discloses an “organic EL display, predetermined layer of resin, touch panel, and circular polarizing plate and polarizing circular plates [that] adheres to touch panel,” and a “touch panel with circular polarized plates bonded to resin with organic EL display.” *Id.* The patent owner did not dispute that Nakamura disclosed these concepts, and instead amended the claims. *Id.*, 11/1/2016 Response.

100. For at least these reasons, Nakamura discloses and renders obvious an organic emitting display panel under the touch panel.

**d) Element [1-C]**

101. Nakamura discloses and renders obvious this element of Claim 1: “a circular polarizing plate arranged at a side of the touch panel opposite to the organic emitting display panel,” and “the organic emitting display panel, the touch panel, and the circular polarizing plate are arranged in this order.”

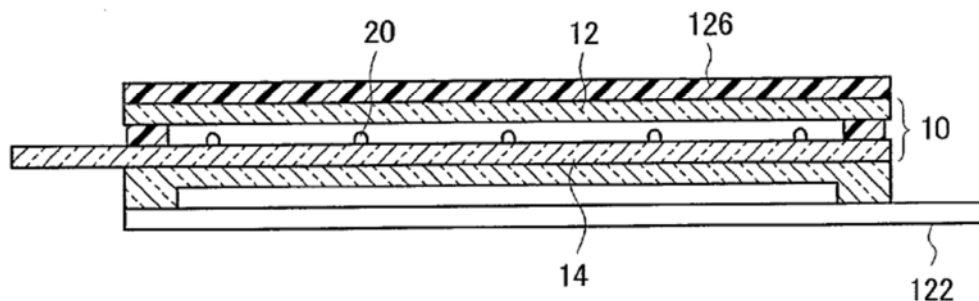
102. As I discussed for the previous limitation, Nakamura’s Fig. 2 shows that “the touch panel of FIG. 1 is bonded to a surface of a display panel,” and the “display device with the touch panel includes a display panel substrate PSUB composing a display device DISP, the first substrate SUB1, the second substrate SUB2, a spacer SPACER, and a circularly polarizing plate CPOL.” Ex. 1004, [0055], Fig. 2:



103. Nakamura's Fig. 2 also shows that "[t]he circularly polarizing plate CPOL is fixed onto the second substrate SUB2," and so is arranged at a side of the touch panel opposite to the organic emitting display panel (the "top emission organic EL display device") located in the display panel substrate PSUB. Ex. 1004, [0055], Fig. 2. As also shown, "[t]he circularly polarizing plate CPOL is fixed onto the second substrate SUB2," such that the organic emitting display panel (the "top emission organic EL display device") the touch panel, and the circular polarizing plate are arranged "in this order." *Id.*

104. I note that the disclosure of this concept in the '758 Patent is substantially similar to this disclosure in Nakamura. See Ex. 1001, 5:52-63, Fig. 6 (showing same arrangement of "circular polarizing plate" 126, "touch panel" 10 comprising substrates 12 and 14, and "organic EL display panel" 122):

*FIG. 6*



105. As confirmation of this, during the prosecution of the '758 Patent's child '229 Patent, the examiner expressly applied Nakamura against similar claim language. Ex. 1006 ('229 File History), 8/2/2016 Office Action, pp. 7-8. The examiner also stated that Nakamura discloses a “circular polarizer [that] adheres to touch panel,” which the examiner stated was well known to a POSITA, an “organic EL display, predetermined layer of resin, touch panel, and circular polarizing plate and polarizing circular plates [that] adheres to touch panel please see figure 2,” and a “touch panel with circular polarized plates bonded to resin with organic EL display.” *Id.* The patent owner did not dispute that Nakamura disclosed these concepts, and instead amended the claims. *Id.*, 11/1/2016 Response.

106. For at least these reasons, Nakamura discloses and renders obvious a circular polarizing plate arranged at a side of the touch panel opposite to the organic emitting display panel, and that the organic emitting display panel, the touch panel, and the circular polarizing plate are arranged in this order.

## **2. Dependent Claim 2**

107. Claim 2 of the '758 Patent depends from Claim 1. Claim 1 is disclosed and rendered obvious by Nakamura, for at least the reasons discussed above.

108. Claim 2 further recites: “each of the plurality of second lines and the plurality of first lines is made of metal” and “each of the plurality of first lines is

black in color.” Nakamura discloses and renders obvious this additional limitation.

109. I note that the disclosure of this concept in the '758 Patent is the same as in Nakamura. *See* Ex. 1001, 6:45-67, 7:45-48, 8:34-37.

110. Nakamura expressly states that the first lines and second lines on its substrates are “configured of metal.” Ex. 1004, [0052] (“The first substrate SUB1 and the second substrate SUB2 are arranged so that their respective metal wirings face each other and that directions along which the respective metal wirings extend are made to intersect”), [0053] (“The second peripheral circuit SC2 is connected to the second substrate SUB2, and selects the metal wiring line by line to input a voltage thereto from the power supply”), [0054] (“The first peripheral circuit SC1 is connected to the first substrate SUB1, and selects the metal wiring line by line to detect a voltage therefrom”), [0066] (“Possible materials of the metal wiring include an opaque metal film made of aluminum (Al), carbon (C), nonferrous metal such as copper (Cu), stainless steel (SUS), or iron (Fe)”; *see also* [0028], [0032], [0050]-[0053], [0055]-[0065], [0067]-[0069], [0071]-[0111]).

111. Nakamura also goes on to explain that any of its lines, including the first lines, may be “black in color.” Ex. 1004, [0078] (“By changing the color of the above-mentioned metal wiring into black, it is possible to raise a contrast of a display such as a liquid crystal equipped with a touch panel”).

112. As confirmation of this, during the prosecution of the '758 Patent's

child '229 Patent, the examiner expressly applied Nakamura against similar claim language. Ex. 1006 ('229 File History), 8/2/2016 Office Action, p. 9. The patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

113. For at least these reasons, Nakamura discloses and renders obvious that each of the plurality of second lines and the plurality of first lines is made of metal and that each of the plurality of first lines is black in color.

### **3. Dependent Claim 3**

114. Claim 3 of the '758 Patent depends from Claim 2. Claim 2 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

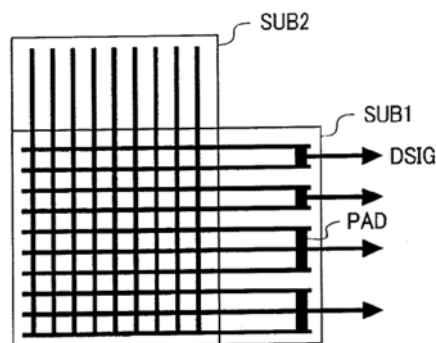
115. Claim 3 further recites: “the touch panel includes a plurality of wiring groups,” “each of plurality of wiring groups has some of the first lines,” and that “some of the first lines in each of plurality of wiring groups are bonded with each other.” Nakamura discloses and renders obvious this additional limitation.

116. I note that the disclosure of this concept in the '758 Patent is the same as in Nakamura. *See* Ex. 1001, 9:17-26, Fig. 14.

117. Nakamura's Fig. 6 shows that the metal wiring on its substrates, which are called MLINEs, can be combined with each other to form wiring groups (*i.e.*, bonded with each other), that each of the wiring groups can comprise some of

the first lines, and that some of the first lines in each plurality of wiring groups can be bonded with each other. Ex. 1004, [0091] (“a terminal PAD for combining a plurality of metal wirings MLINE is provided in order to detect voltages of the plurality of metal wirings MLINE simultaneously, and a detection signal is output from each terminal PAD”), [0092] (“If the coordinate detection high in definition is unnecessary, the plurality of metal wirings MLINE are combined, to thereby enhance a recognition rate”), Fig. 6:

FIG.6



118. As Nakamura explains, “[t]his [Fig. 6 wiring] mode can be applied to the stripe-shaped metal wirings according to Wiring Layout Modes 1 and 2.” Ex. 1004, [0093]. Wiring Layout Mode 1 is the preferred embodiment shown in Figs. 1-3. *Id.*, [0050]-[0080].

119. I note that Fig. 6 only depicts the metal wiring on the bottom substrate SUB1 combined into a group. While that is sufficient to show that Nakamura

discloses this claim element, a POSITA also would have understood that this teaching regarding grouping the metal wirings applies equally to both of Nakamura's substrates, at least because both substrates use the same metal wirings MLINE to detect the coordinates of a touch. *See* Ex. 1004, [0051], [0056]-[0057], [0079], Figs. 1-2, 7. The choice of which substrates and electrodes to use for the application of voltage and which to use for sensing of the voltage could be equally made for each substrate. Similarly, the choice of grouping could be applied to the voltage application wiring and/or the sensing wiring without concern. For at least these reasons, therefore, a POSITA would have understood that this teaching regarding grouping the metal wirings applies equally to both of Nakamura's substrates.

120. This was confirmed during the prosecution of the '758 Patent's child '229 Patent, when the examiner expressly applied Nakamura against similar claim language. Ex. 1006 ('229 File History), 8/2/2016 Office Action, p. 8. The examiner also stated that "figures 16-21 suggest[] different wiring patterns are in groups and banded [sic] by being printed on the different films." *Id.* The patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

121. For at least these reasons, Nakamura discloses and renders obvious that the touch panel includes a plurality of wiring groups, each of plurality of

wiring groups has some of the first lines, and that some of the first lines in each of plurality of wiring groups are bonded with each other.

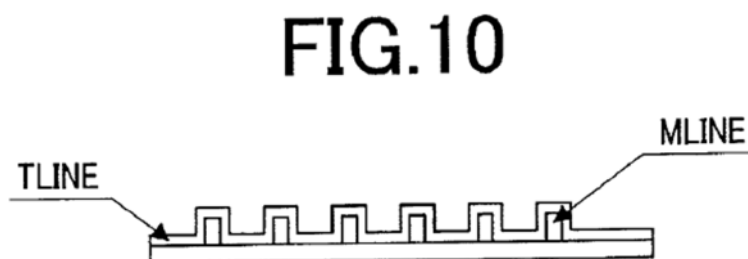
#### 4. Dependent Claim 4

122. Claim 4 of the '758 Patent depends from Claim 3. Claim 3 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

123. Claim 4 further recites: “a transparent conductive film overlays the plurality of the first lines” and “the transparent conductive film is electrically connected to the plurality of the first lines.” Nakamura discloses and renders obvious this additional limitation.

124. I note that the disclosure of this concept in the '758 Patent is the same as in Nakamura. See Ex. 1001, 9:63-10:3, Fig. 18.

125. Nakamura's Fig. 10 shows “that a transparent wiring (electrode) TLINE that covers the entirety of the detection area is located above the metal wiring MLINE.” Ex. 1004, [0105], Fig. 10:



126. Nakamura explains throughout its disclosure that transparent wiring

TLINE is a transparent conductive film that is electrically connected to the metal lines MLINE. *See, e.g.*, Ex. 1004, [0007]-[0008], [0102], [0105]. And as shown in Fig. 10, TLINE overlays the MLINEs.

127. As Nakamura explains, “[t]his [Fig. 10 wiring] mode can be applied to the stripe-shaped metal wirings according to Wiring Layout Modes 1 to 5.” Ex. 1004, [0106]. Wiring Layout Mode 1 is the preferred embodiment shown in Figs. 1-3. *Id.*, [0050]-[0080].

128. As confirmation of this, during the prosecution of the ’758 Patent’s child ’229 Patent, the examiner expressly applied Nakamura against identical claim language. Ex. 1006 (’229 File History), 8/2/2016 Office Action, pp. 10-11. The patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

129. Nakamura’s teachings regarding Fig. 10 apply to both the first lines and second lines for several reasons. At the threshold, Nakamura’s discussion of Fig. 10 does not limit which lines its teachings apply to. Additionally, as I have previously discussed, the disclosure of this concept in the ’758 Patent is the same as in Nakamura. Further, as I have also discussed, Nakamura was applied against identical claim language during the prosecution of a related patent. Moreover, the metal lines MLINE on both of Nakamura’s substrates are used for coordinate detection, such that both could benefit from transparent conductive film overlays.

Ex. 1004, [0079]. And as I discussed above in Section X.A.3, either substrate could be used for voltage application or sensing, at least because the assignment of substrates is arbitrary and a POSITA would have recognized that either substrate could serve as the voltage application or voltage sensing substrate.

130. For at least these reasons, Nakamura discloses and renders obvious that a transparent conductive film overlays the plurality of the first lines and the transparent conductive film is electrically connected to the plurality of the first lines.

#### **5. Dependent Claim 5**

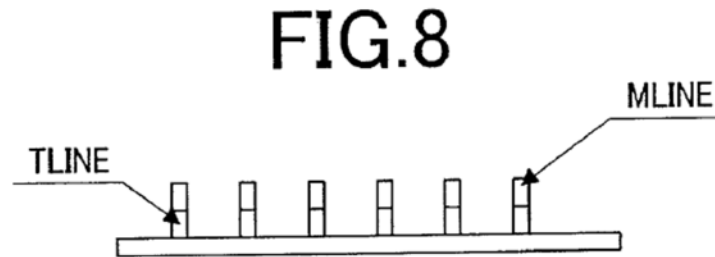
131. Claim 5 of the '758 Patent depends from Claim 3. Claim 3 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

132. Claim 5 further recites: “a transparent conductive film underlays the plurality of the first lines” and “the transparent conductive film is electrically connected to the plurality of the first lines.” Nakamura discloses and renders obvious this additional limitation. This is the case in several embodiments.

133. I note that the disclosure of this concept in the '758 Patent is the same as in Nakamura. See Ex. 1001, 9:47-62, Figs. 16-17.

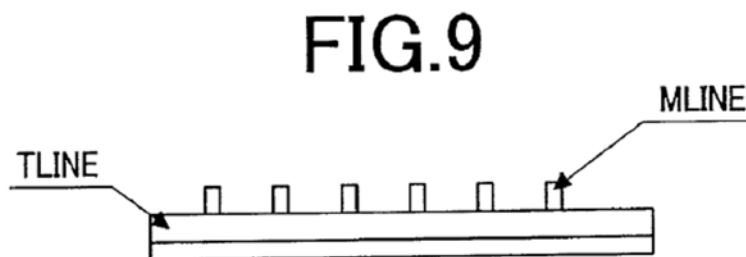
134. A first embodiment is shown in Fig. 8, about which Nakamura discloses “that a stripe-shaped transparent wiring TLINE having the same pattern

as that of the metal wiring MLINE is located under the metal wiring MLINE.” Ex. 1004, [0099], Fig. 8:



135. Nakamura explains throughout its disclosure that the transparent wiring TLINE is a transparent conductive film that is electrically connected to the metal lines . *See, e.g.*, Ex. 1004, [0007]-[0008], [0099], [0102], [0105]. And as applied to and shown in Fig. 8, a collection of TLINEs underlays and connects to the plurality of MLINEs.

136. A second embodiment is shown in Fig. 9, about which Nakamura discloses “that a transparent wiring (electrode) TLINE that covers the entirety of the detection area is located under the metal wiring MLINE.” Ex. 1004, [0102], Fig. 9:



137. Here again, TLINE underlays the MLINEs.

138. Nakamura explains throughout its disclosure that the wirings shown in all of Figs. 8-9 “can be applied to the stripe-shaped metal wirings according to Wiring Layout Modes 1 to 5.” Ex. 1004, [0100], [0103]. Wiring Layout Mode 1 is the preferred embodiment shown in Figs. 1-3. *Id.*, [0050]-[0080].

139. As confirmation of this, during the prosecution of the ’758 Patent’s child ’229 Patent, the examiner expressly applied Nakamura against identical claim language. Ex. 1006 (’229 File History), 8/2/2016 Office Action, p. 11. The patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

140. Nakamura’s teachings regarding Figs. 8 and 9 apply to both the first lines and second lines for several reasons. At the threshold, Nakamura’s discussion of Figs. 8 and 9 does not limit which lines its teachings apply to. Additionally, as I have previously discussed, the disclosure of this concept in the ’758 Patent is the same as in Nakamura. Further, as I have also discussed, Nakamura was applied against identical claim language during the prosecution of a related patent. Moreover, the metal lines MLINE on both of Nakamura’s substrates are used for coordinate detection, such that both could benefit from transparent conductive film overlays. Ex. 1004, [0079]. As I discussed above in Section X.A.3, either substrate could be used for voltage application or sensing, at least because the assignment of substrates is arbitrary and a POSITA would have

recognized that either substrate could serve as either the voltage application or voltage sensing substrate. The choice of which lines to use for voltage application or sensing could thus also be made between the two sets of lines without issue, since the assignment of substrates is simply a matter of choice. Under these circumstances, at a minimum, a POSITA would have found it obvious to apply Nakamura's Fig. 8 and 9 concepts to its first lines in addition to its second lines.

141. For at least these reasons, Nakamura discloses and renders obvious that a transparent conductive film underlays the plurality of the first lines and the transparent conductive film is electrically connected to the plurality of the first lines.

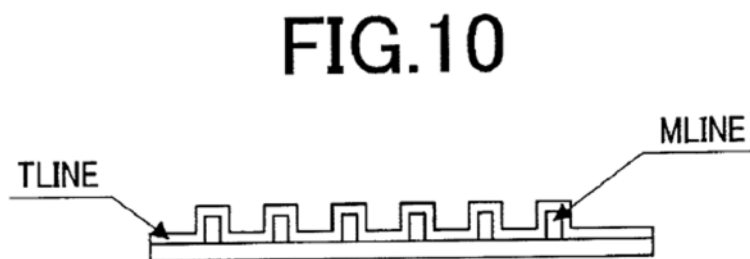
## **6. Dependent Claim 6**

142. Claim 6 of the '758 Patent depends from Claim 2. Claim 2 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

143. Claim 6 further recites: "a transparent conductive film overlays the plurality of the second lines" and "the transparent conductive film is electrically connected to the plurality of the second lines." Nakamura discloses and renders obvious this additional limitation.

144. I note that the disclosure of this concept in the '758 Patent is the same as in Nakamura. See Ex. 1001, 9:63-10:3, Fig. 18.

145. Nakamura's Fig. 10 shows "that a transparent wiring (electrode) TLINE that covers the entirety of the detection area is located above the metal wiring MLINE." Ex. 1004, [0105], Fig. 10:



146. Nakamura explains throughout its disclosure that the transparent wiring TLINE is a transparent conductive film that is electrically connected to the metal lines. *See, e.g.*, Ex. 1004, [0007]-[0008], [0102], [0105]. And as shown in Fig. 10, TLINE overlaps the MLINEs.

147. As Nakamura explains, "[t]his [Fig. 10 wiring] mode can be applied to the stripe-shaped metal wirings according to Wiring Layout Modes 1 to 5." Ex. 1004, [0106]. Wiring Layout Mode 1 is the preferred embodiment shown in Figs. 1-3. *Id.*, [0050]-[0080].

148. As confirmation of this, during the prosecution of the '758 Patent's child '229 Patent, the examiner expressly applied Nakamura against similar claim language. Ex. 1006 ('229 File History), 8/2/2016 Office Action, p. 10. The patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

149. For at least these reasons, Nakamura discloses and renders obvious that a transparent conductive film overlays the plurality of the second lines and the transparent conductive film is electrically connected to the plurality of the second lines.

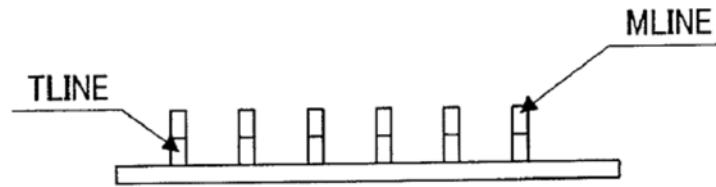
## **7. Dependent Claim 7**

150. Claim 7 of the '758 Patent depends from Claim 2. Claim 2 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

151. Claim 7 further recites: “a transparent conductive film underlays the plurality of the second lines” and “the transparent conductive film is electrically connected to the plurality of the second lines.” Nakamura discloses and renders obvious this additional limitation. This is the case in several embodiments.

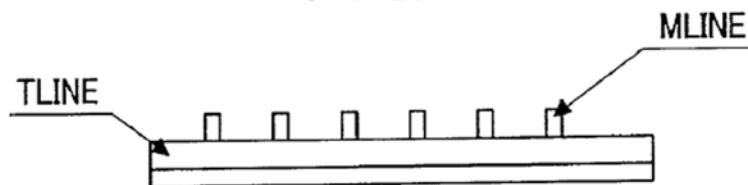
152. I note that the disclosure of this concept in the '758 Patent is the same as in Nakamura. *See* Ex. 1001, 9:47-62, Figs. 16-17.

153. A first embodiment is shown in Fig. 8, about which Nakamura discloses “that a stripe-shaped transparent wiring TLINE having the same pattern as that of the metal wiring MLINE is located under the metal wiring MLINE.” Ex. 1004, [0099], Fig. 8:

**FIG.8**

154. Nakamura explains throughout its disclosure that the transparent wiring TLINE is a transparent conductive film that is electrically connected to the metal lines. *See, e.g.*, Ex. 1004, [0007]-[0008], [0102], [0105]. And as applied to and shown in Fig. 8, a collection of TLINEs underlays and connects to the plurality of MLINEs.

155. A second embodiment is shown in Fig. 9, about which Nakamura discloses “that a transparent wiring (electrode) TLINE that covers the entirety of the detection area is located under the metal wiring MLINE.” Ex. 1004, [0102], Fig. 9:

**FIG.9**

156. Here again, TLINE underlays the MLINEs.

157. As Nakamura explains, the wirings shown in all of Figs. 8-9 “can be

applied to the stripe-shaped metal wirings according to Wiring Layout Modes 1 to 5.” Ex. 1004, [0100], [0103]. Wiring Layout Mode 1 is the preferred embodiment shown in Figs. 1-3. *Id.*, [0050]-[0080].

158. As confirmation of this, during the prosecution of the ’758 Patent’s child ’229 Patent, the examiner expressly applied Nakamura against identical claim language. Ex. 1006 (’229 File History), 8/2/2016 Office Action, p. 11. The patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

159. For at least these reasons, Nakamura discloses and renders obvious that a transparent conductive film underlays the plurality of the second lines and the transparent conductive film is electrically connected to the plurality of the second lines.

## **8. Dependent Claim 8**

160. Claim 8 of the ’758 Patent depends from Claim 1. Claim 1 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

161. Claim 8 further recites: “the touch panel is a resistance-film-type touch panel.” Nakamura discloses and renders obvious this additional limitation.

162. I note that the disclosure of this concept in the ’758 Patent is the same as in Nakamura. *See* Ex. 1001, 1:22-2:15, 7:54-67, 8:44-50, Figs. 10, 21.

163. Nakamura explains in detail that resistive sensing touch panels (which it refers to as “resistive film systems”) were so well-known that they were “conventional” in the art, as reflected in Nakamura’s depiction of one such touch panel in its “prior art” Fig. 14, and discussion of the prior art “resistive film system” of Takaya. Ex. 1004, [0005]-[0009], Fig. 14.

164. Following this discussion, Nakamura expressly states that it too discloses a resistive sensing system, but one that overcomes the alleged drawbacks of Takaya. *Id.*, [0010]-[0011]; *see also* [0068], [0080], Fig. 2.

165. For at least these reasons, Nakamura discloses and renders obvious that the touch panel is a resistance-film-type touch panel.

**B. Ground 2 – Nakamura, As Well as Nakamura in Combination with Hinata ’741, Renders Claim 9 Obvious**

166. In my opinion, Nakamura renders Claim 9 of the ’758 Patent obvious, both alone and in combination with Hinata ’741.

**1. Dependent Claim 9**

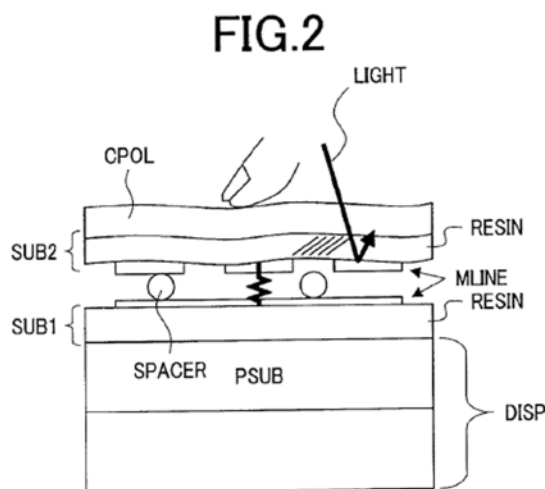
167. Claim 9 of the ’758 Patent depends from Claim 1. Nakamura discloses and renders obvious Claim 1 for at least the reasons I discussed above for that claim. *See* Section X.A.1.

168. Claim 9 further recites: “a first adhesive layer between the touch panel and the organic emitting display panel” and “a second adhesive layer between the touch panel and the circular polarizing plate,” “wherein the touch

panel and the organic emitting display panel are fixed with each other by the first adhesive layer, and the touch panel and the circular polarizing plate are fixed with each other by the second adhesive layer.”

169. Nakamura renders this additional limitation obvious, both alone and in combination with Hinata '741.

170. As I discussed for Claim 1 above, Nakamura's Fig. 2 shows an embodiment that includes an organic emitting display panel (the “top emission organic EL display device”), a touch panel, and a circular polarizing plate, and that they are arranged in that order. See Section X.A.1; Ex. 1004, [0055], Fig. 2:



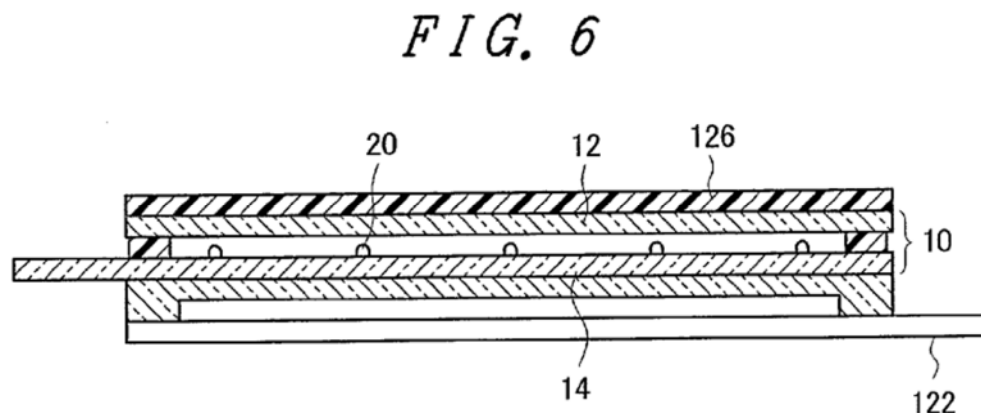
171. Additionally, Nakamura states both that the touch panel's first substrate SUB1 can be “adhered onto the display panel substrate PSUB” and also that it can be “fixed onto the display panel substrate PSUB,” with the PSUB comprising “a sealing substrate of a top emission organic EL display device.” Ex.

1004, [0055]. The point in Nakamura's display where the first substrate SUB1 is adhered onto and fixed onto the display panel substrate PSUB, this discloses and renders obvious the claimed "first adhesive layer" between the organic emitting display panel and the touch panel, which adheres and fixes them with each other. A POSITA would recognize that the material at that point is necessarily a physical layer and, since Nakamura clearly indicates that it is adhered therein, it would, at a minimum, be obvious for this adhesion to constitute an adhesive layer. I note that there is no requirement in the claim at issue, nor would a POSITA interpret it to require, that the material of the adhesive layer be a different material or be formed in an entirely different process than the layer sequentially below it.

172. Nakamura similarly explains that "[t]he circularly polarizing plate CPOL is fixed onto the second substrate SUB2." Ex. 1004, [0055]. The point in Nakamura's display where the CPOL is fixed onto the second substrate SUB2 discloses and renders obvious the claimed "second adhesive layer" between the touch panel and the circular polarizing plate, which fixes them with each other. As Nakamura clearly indicates that the polarizing plate is fixed onto the second substrate SUB2, a POSITA would recognize that this fixing would involve a physical layer and that, at a minimum, it would be obvious to fix the polarizing plate onto the second substrate SUB2 by adhering it, thus constituting an adhesive layer. I again note that there is no requirement in the claim at issue, nor would a

POSITA interpret it to require, that the material of the adhesive layer be a different material or be formed in an entirely different process than the layer sequentially below it.

173. It does not appear that this claim element requires physically separate adhesive layers. Indeed, I note that the disclosure of this concept in the '758 Patent is the substantially similar to this discussion in Nakamura. See Ex. 1001, 5:52-63, Fig. 6 (showing same arrangement of “circular polarizing plate” 126, “touch panel” 10 comprising substrates 12 and 14, and “organic EL display panel” 122):



174. Similar to Nakamura’s disclosure, the '758 Patent specification states only that “the touch panel 10 is adhered to a display screen of the display panel 122, and a resin film 126 is adhered to the touch panel 10.” Ex. 1001, 5:58-60. The '758 Patent specification does not recite, or depict in its Figures, physically separate adhesive layers, and instead states only that the components are “adhered” to each other. *Id.* Consistent with the fact that the '758 Patent specification does

not even recite physically separate adhesive layers, it also does not provide any discussion of what form such an adhesive layer would take, and of course does not allege that such a concept was novel or nonobvious. This means that, if this claim element were interpreted to require physically separate adhesive “layers,” there is no written description in the ’758 Patent specification that could support such a read of the claim.

175. This understanding was confirmed during the prosecution of the ’758 Patent’s child ’229 patent, when the examiner expressly applied Nakamura against claim language relating to these same components being “adhered” together. Ex. 1006 (’229 File History), 8/2/2016 Office Action, pp. 7-8. When doing so, the examiner additionally stated that Nakamura discloses a “circular polarizer [that] adheres to touch panel”—which the examiner remarked was well known to a POSITA—an “organic EL display, predetermined layer of resin, touch panel, and circular polarizing plate and polarizing circular plates [that] adheres to touch panel please see figure 2,” and a “touch panel with circular polarized plates bonded to resin with organic EL display.” *Id.* The patent owner did not dispute that Nakamura disclosed these concepts, and instead amended the claims. *Id.*, 11/1/2016 Response.

176. In view of these considerations and Nakamura’s express disclosures that the components are “adhered” and “fixed” together in the claimed

arrangement, a POSITA would have additionally considered it obvious for Nakamura's display components to have been adhered together using a separate "first adhesive layer" and "second adhesive layer."

177. In 2009, there were only a few ways to adhere touch panel components together. These included using a physically separate adhesive layer, as well as using the interfacing surfaces of one or both of the materials being adhered as the adhesive layer. It would have been a routine design choice to select any one of these ways in order to accommodate the needs of a particular touch panel. The most common-sense way of doing so would have been using a physically separate adhesive layer. In particular, for touch panel applications such as displays with touch-panels integrated on them, it was particularly beneficial to use a physically separate adhesive layer in order to first allow for complete fabrication of the display (even in a different factory or location, for example), and then adhering the touch panel on top using such a separate adhesive layer. In 2009, there were a number of common methods of forming adhesives, including coating and laminate and deposited adhesives, and the selection of any of these methods would have been an obvious, routine design choice. Deposition of adhesives was well-known in the semiconductor and display industries, and would have been straightforward to implement using equipment and processes that were well-known and common in the same, and enable easy adhesion of layers even in the large

areas associated with many touch-integrated displays. Indeed, the use of laminated or deposited adhesion films was common in the industry and eliminated concerns with process integration and contamination when the surfaces of the layers being joined are themselves adhered without a separate adhesive layer. The benefits of using a physically separate adhesive layer include allowing for a greater strength of adhesion in situations where the surface of a layer has low adhesion. A POSITA thus would have been particularly motivated to implement Nakamura using physically separate adhesive layers when employing its touch panel in such applications.

178. For at least these reasons, a POSITA would have considered it obvious to fix Nakamura's touch panel and organic emitting display panel with each other using a physically separate first adhesive layer and to fix Nakamura's touch panel and circular polarizing plate with each other using a using a physically separate second adhesive layer in view of Nakamura alone.

179. A POSITA also would have found it obvious to adhere Nakamura's touch panel, organic emitting display panel, and circular polarizing plate to each other using physically separate adhesive layers in view of Nakamura combined with Hinata '741.

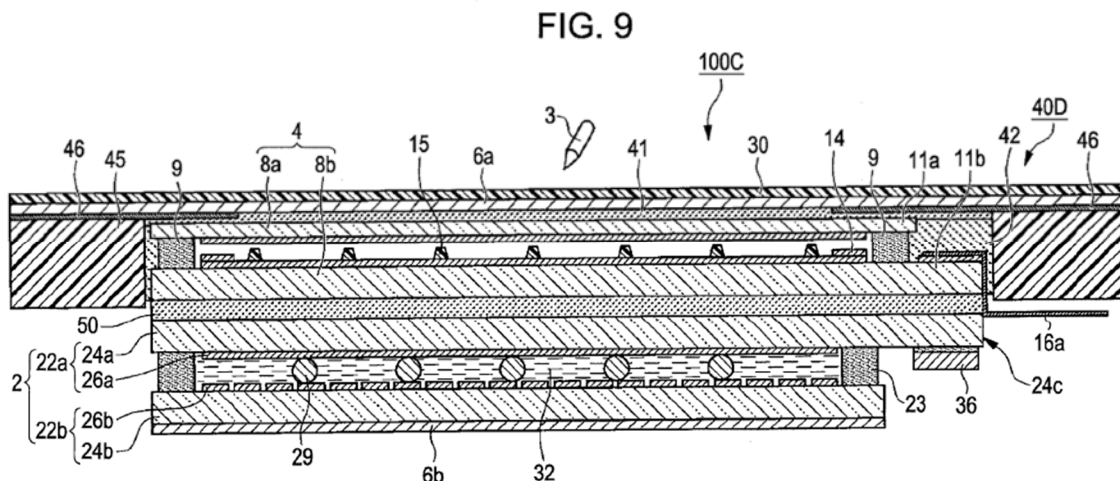
180. A POSITA would have been motivated to combine Nakamura and Hinata '741 for at least the reasons that I discussed in Section IX.C above, as well

as the reasons I discuss in the following paragraphs.

181. Hinata '741 teaches a number of touch panel embodiments that can take of a variety of structures, and these discussions include a number of different ways that each of its various components can be adhered together. *See, e.g.*, Ex. 1005, [0008]-[0009], [0019]-[0022] (discussing using “[a]n adhesive”), [0030] (discussing “optically adher[ing]”), [0048]-[0052] (discussing “vacuum thermal-welding method” of adhesion), [0083], [0095] (“various adhesive compounds, such as acrylic adhesive compounds, rubber-based adhesive compounds, and silicon based adhesive compounds, may be used”). Each of these discussions alone provides greater detail than anything in the '758 Patent does.

182. Hinata '741's varied disclosure of these concepts includes embodiments that expressly include a physically separate adhesive layer 41 between the polarizing plate 6a and the touch panel 4. *Id.*; *see also* Figs. 5, 9 (applying the above adhering teachings to adhesive layer 41). Similarly, Hinata '741 includes embodiments that expressly include a second physically separate adhesive layer 50 between the display panel 2 and the touch panel 4. *Id.*; *see also* Figs. 7A, 8, 9, 18 (applying the above adhering teachings to adhesive layer 50). Putting these concepts together, Hinata '741's Fig. 9 embodiment discloses both of the adhesive layers recited in '758 patent Claim 9 in a single embodiment, *i.e.*, first adhesive layer 41 between polarizing plate 6a and touch panel 4, and second

adhesive layer 50 between display panel 2 and touch panel 4. This is readily seen in Hinata '741's Fig. 9 itself. *Id.*, Fig. 9:



183. I note that display panel 2 is described as an LCD panel in the above paragraphs. However, Hinata '741 expressly explains elsewhere than an organic EL panel can be used rather than an LCD panel in any of its embodiments. *Id.*, [0029], [0056].

184. A POSITA would have been motivated to apply Hinata '741's physically separate adhesive layers to the touch panel, organic emitting display panel, and circular polarizing plate that Nakamura explains are adhered to each other for the same reasons discussed above in relation to the benefits of using an adhesive layer—namely, ease of implementation, applicability to large area systems such as displays with touch screens, the use of common equipment and processes, and the potential for a greater strength of adhesion.

185. For at least these reasons, a POSITA would have found it obvious to

adhere Nakamura's touch panel, organic emitting display panel, and circular polarizing plate to each other using physically separate adhesive layers in view of Nakamura alone, and also as taught by Hinata '741.

## **XI. SECONDARY CONSIDERATIONS**

186. I am not aware of secondary considerations of non-obviousness that bear on the challenged claims. If I am made aware in the future of arguments of any secondary consideration, I expressly reserve the right to assess those arguments when they arise in order to form opinions regarding their correctness or incorrectness.

## **XII. CONCLUSION**

187. It is my conclusion and opinion that Claims 1-9 of the '758 Patent are invalid.

I declare under penalty of perjury that the foregoing is true and correct.

Executed this 3rd day of July, 2025 in Morges, Switzerland.

Vivek Subramanian

Dr. Vivek Subramanian

# Appendix A

## Vivek Subramanian

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### @ Virtual Mailbox

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Austin, TX 78701, USA

### Education

3 / 96 - 6 / 98

**Ph.D. in Electrical Engineering, Stanford University**  
*Stanford, California*

Honors earned: Graduate Fellowship, Eastman Kodak Company

9 / 94 - 3 / 96

**MS in Electrical Engineering, Stanford University**  
*Stanford, California*

8 / 90 - 5 / 94

**BS in Electrical Engineering, Louisiana State University**  
*Baton Rouge, Louisiana*

Honors earned: Summa cum laude, College Honors, Outstanding Senior, Junior and Sophomore, Honors College

### Professional Experience

2018 - present

**École polytechnique fédérale de Lausanne**  
*Switzerland*

**8/18 – present: Professor of Microengineering**

2000 - present

**Department of Electrical Engineering & Computer Sciences, University of California**  
*Berkeley, CA*

**7/18 – present: Chancellor's Professor**

**7/11 – present: Professor**

**7/05 – 7/11: Associate Professor**

**7/00-7/05: Assistant Professor**

Research, teaching and service in EECS Department

#### Honors Earned:

2015 IEEE Kiyo Tomiyasu Award  
Best in session and best in track awards, 2013 IMAPS Microelectronics Conference  
Outstanding paper award, 2012 IMAPS Microelectronics Conference  
2008 Printed Electronics Champion, Printed Electronics USA Conference, November 2008  
Outstanding Teaching Award, EECS Department, UC Berkeley, 2005  
Best paper award, 2004 IEEE Device Research Conference  
Nominated to MIT's Technology Review top 100 young innovators list (TR100), 2002  
National Science Foundation Young Investigator (CAREER) Award, FY2002,  
Nominated to National Academy of Engineering's *Frontiers of Engineering*, 2002  
Winner of 2002 Paul Rappaport Award for best paper in an IEEE EDS Journal

2009 - present

**Adjunct Professor, Sunchon National University**  
*Sunchon, Korea*

**2013 to date: Adjunct Professor, BK21 Program**

**2009-2013: Adjunct Professor and Principal Investigator, WCU Program**

*Initiated, managed, and contributed to large multinational research program focused on printed electronics, including displays, energy devices, and RFID*

2000 - present

**Independent Consultant**  
*Orinda, CA*

Consultant to the semiconductor industry and its associated fields in the following areas:

Memory technology and design, Silicon Process Technology  
Display / Imager and Flexible Electronics Technology, RFID Technology  
Intellectual Property Consulting  
Technology Evaluation / Venture Capital due diligence

|               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2014- present | <b>Founder and CTO, Locix Inc.</b><br><i>San Bruno, CA</i><br><i>Senior leadership role in venture-funded startup company working on wireless networking</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 2004 – 2013   | <b>Founding Scientific Advisor, Kovio, Inc.</b><br><i>Sunnyvale, CA</i><br><i>Scientific advising to printed electronics startup company</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 2008 - 2011   | <b>Chief Technical Advisor, QuSwami, Inc.</b><br><i>San Francisco, CA</i><br><i>Scientific advising to energy conversion device startup company</i><br>Served as CTO from July 2010-June 2011                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1998 - 2000   | <b>Consulting Assistant Professor, Electrical Engineering Department, Stanford University.</b><br><i>Stanford, CA</i><br>Advisory role for research group of Prof. Krishna C. Saraswat                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 1998-2000     | <b>Visiting Research Engineer, Electrical Engineering Department, University of California.</b><br><i>Berkeley, CA</i><br>Research into 25nm MOSFET technologies for giga-scale integration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1998 - 2000   | <b>Founder, Matrix Semiconductor, Inc.</b><br><i>Santa Clara, CA</i><br>Co-founder and technical advisor of startup company working on high-density memory technology<br><b>Honors Earned:</b><br>Nominated to Scientific American's SA50 List for Visionary Technology<br>Finalist for 2003 World Technology Award for Information Technology Hardware<br>Winner, 2005 EDN Innovation Award                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 1998          | <b>Co-instructor, Electrical Engineering Department, Stanford University.</b><br><i>Stanford, CA</i><br>Co-teaching of EE311, Advanced Integrated Circuit Fabrication Processes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 1997          | <b>Intern, Advanced Product Research and Development Laboratory, Motorola Inc.</b><br><i>Austin, TX</i><br>Research into process development issues affecting SiGe SEMFET devices                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1996          | <b>Head Teaching Assistant EE410: IC Fabrication Laboratory, Stanford University</b><br><i>Stanford, CA</i><br>Coordination and instruction of EE410, graduate level laboratory course.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1994-1998     | <b>Research Assistant, Electrical Engineering, Stanford University</b><br><i>Stanford, CA</i><br>Research into crystallization of amorphous Si and SiGe films using low thermal budget processes.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|               | <b>Professional Affiliations and Activities</b><br>Technical Program Committee, IEEE Electronic Components and Technology Conference, 2014 to 2016<br>Chair, Scientific Advisory Board, iPACK, Royal Institute of Technology (KTH), Sweden, 2011 to 2016<br>Tampere Institute of Technology Faculty Search Committee, Finland, 2013<br>University of Oulu Faculty Search Committee, Finland, 2013<br>Served as external thesis committee member for several universities world-wide, including University of Cape Town (South Africa), Tampere Institute of Technology (Finland), Technical University of Eindhoven (Netherlands), Indian Institute of Science (India), Indian Institute of Technology (India), 2009 to date<br>Associate Editor, IEEE Journal of Display Technology, 2008 to date<br>Technical Program Chair, Large Area, Organic, and Printed Electronics Conference, 2012-2013<br>Scientific Committee, Large Area, Organic, and Printed Electronics Conference, 2009-2011<br>Scientific Committee, International Conference on Printed and Flexible Electronics, 2009-2013<br>IEEE Electron Devices Society Organic Electronics Committee, 2003 - 2005<br>Executive Committee, International Electron Device Meeting, 2003 to 2009<br>Technical Program Committee, International Electron Device Meeting, 2001-2002<br>Technical Program Committee member, Device Research Conference, 2000-2002<br>Technical Program Committee member, VLSI-TSA Conference, 2005<br>Member, Institute of Electrical and Electronic Engineers |

**List of cases worked on by Vivek Subramanian**

***Completed***

- Lexar Media v. Pretec Electronics Corp., et al (N.D. Cal., Case No. 00-CV-4770 MJJ, deposition) – retained by Pretec Electronics Corp, PNY Electronics, Memorex
- Motorola, Inc. v. Analog Devices, Inc., Civil Action No. 1:03-CV-0131 – retained by Analog Devices
- *Sandisk Corporation vs. Micron*, Case No. CV-01-3855 CW – retained by Micron
- In the Matter of CERTAIN NAND FLASH MEMORY CIRCUITS AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-526, deposition and trial) – retained by STMicroelectronics
- In the Matter of CERTAIN NAND FLASH MEMORY DEVICES AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-553, deposition and trial) – retained by Hynix
- In the Matter of CERTAIN NOR AND NAND FLASH MEMORY DEVICES AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-560, deposition and trial) – retained by STMicroelectronics
- STMicroelectronics, Inc. v. SanDisk Corporation (E.D. Texas, Civil Action No. 4:05-CV-45, deposition) – retained by STMicroelectronics
- Sandisk Corporation v. Memorex Products, Inc. et al, CV 01-4063 – retained by Memorex.
- Seagate Technology LLC et al v. STEC, Inc., Case No. 5:08-CV-01950 JW (HRL) – retained by STEC.
- In the Matter of CERTAIN NAND FLASH MEMORY DEVICES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-592) – retained by Hynix
- In the Matter of CERTAIN FLASH MEMORY CONTROLLERS, DRIVES, MEMORY CARDS, AND MEDIA PLAYERS AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-619, deposition and trial) – retained by Phison Electronics, Silicon Motion, Kingston, and Apacer
- Harari and Mehrotra v. Hollmer and Cleveland (Board of Patent Appeals and Interferences, Interference# 105,606, deposition) – retained by Spansion

- In the Matter of CERTAIN SEMICONDUCTOR INTEGRATED CIRCUITS USING TUNGSTEN METALLIZATION AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-648) – retained by STMicroelectronics
- In the Matter of CERTAIN SEMICONDUCTOR CHIPS HAVING SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY CONTROLLERS AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-661, deposition and trial) – retained by NVidia
- Fast memory erase, LLC. v. Spansion, Inc. et al, Civil Action No. 3:08-CV-00977-M, retained by Spansion
- In the Matter of CERTAIN MOBILE TELEPHONES AND WIRELESS COMMUNICATIONS DEVICES FEATURING DIGITAL CAMERAS AND COMPONENTS THEREOF (ITC, Investigation No. 337-TA-663, deposition and trial) – retained by LG Electronics and Samsung Electronics
- In the Matter of CERTAIN MLC FLASH MEMORY DEVICES AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-683, deposition and trial) – retained by Samsung
- In the Matter of CERTAIN MOBILE TELEPHONES WIRELESS COMMUNICATION DEVICES FEATURING DIGITAL CAMERAS, AND COMPONENTS THEREOF (ITC, Investigation No. 337-TA-703, deposition and trial) – retained by Apple
- Vizio, Inc. v. L Electronics, Inc., et al, In the United States District Court For The District of Maryland, Civil action No. 1:09-CV-1481 (BEL), deposition – retained by LG
- In the Matter of CERTAIN ELECTRONIC DEVICES, INCLUDING MOBILE PHONES, PORTABLE MUSIC PLAYERS, AND COMPUTERS (ITC, Investigation No. 337-TA-701, deposition and trial) – retained by Apple
- Nokia v. Apple, 09-CV-791 and v09-CV-1002 – retained by Apple
- SanDisk Corporation v. Phison Electronics Corp., et al, In the United States District Court For The Western District of Wisconsin, Civil action No. 07-C-0605-C and 07-C-0607-C, deposition – retained by Phison Electronics Corp., Silicon Motion, Skymedi, and Kingston
- Microchip Technology Inc v. LSI Corporation and Agere Systems Inc., Case No. 2:11-cv-01326-DGC, retained by Microchip
- In the Matter of CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS, MEDIA PLAYERS AND CAMERAS (ITC, Investigation No. 337-TA-709, deposition and trial) – retained by Freescale Semiconductor, Inc.

- In the Matter of CERTAIN SEMICONDUCTOR PRODUCTS MADE BY ADVANCED LITHOGRAPHY TECHNIQUES AND PRODUCTS CONTAINING SAME, (ITC, Investigation No. 337-TA-729) – retained by Samsung
- In the Matter of CERTAIN MOBILE DEVICES AND RELATED SOFTWARE (ITC, Investigation No. 337-TA-750, deposition and trial) – retained by Apple, Inc.
- In the Matter of CERTAIN SEMICONDUCTOR CHIPS AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-753) – retained by NVidia
- In the Matter of CERTAIN MOBILE TELEPHONES AND MODEMS (ITC, Investigation No. 337-TA-758) – retained by LG.
- In the Matter of CERTAIN VIDEO GAME SYSTEMS AND WIRELESS CONTROLLERS AND COMPONENTS THEREOF (ITC, Investigation No. 337-TA-770, deposition and trial) – retained by Nintendo
- In the Matter of CERTAIN RANDOM ACCESS MEMORY DEVICES AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-595 ) retained by Renesas
- In the Matter of CERTAIN MICROPROCESSORS, COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-781, deposition and trial) – retained by Intel
- In the Matter of CERTAIN DIGITAL TELEVISIONS CONTAINING INTEGRATED CIRCUIT DEVICES AND COMPONENTS THEREOF (ITC, Investigation No. 337-TA-806, deposition) – retained by Renesas
- In the Matter of CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS (ITC, Investigation No. 337-TA-786, deposition and trial) – retained by Freescale
- In the Matter of CERTAIN SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES AND PRODUCTS CONTAINING SAME (ITC Investigation No. 337-TA-840) – retained by Microchip.
- In the Matter of CERTAIN DYNAMIC RANDOM ACCESS MEMORY AND NAND FLASH MEMORY DEVICES AND PRODUCTS CONTAINING THE SAME (ITC, Investigation No. 337-TA-803, deposition) – retained by Hynix
- AVM Technologies LLC v. Intel Corporation, Civil Action No. 10-610-RK – retained by Intel
- Round Rock Research LLC v. Dell Inc., No. 11-CV-976-RGA – retained by Dell

- Solid State Storage Solutions, Inc. v. STEC, Inc., OCZ Technology, Inc. Corsair Memory, Texas Memory Systems, Inc. PNY Technologies, Inc., Patriot Memory LLC, Fusion-IO, Inc., Other World Computing, Inc., and Mushkin, Inc., Civil Action No 2:11-CV-391, retained by Corsair, PNY, and Fusion-IO.
- Grail Semiconductor, Inc., v. Renesas Electronics America, Inc., Case No. C 11-03847, retained by Renesas.
- In The Matter of Certain Wireless Consumer Electronics Devices and Components Thereof (ITC, Inv. No. 337-TA-853), retained by Amazon.com, Acer, Barnes & Noble, Garmin, HTC, Huawei, Kyocera, LG, Nintendo, Novatel, Samsung, and ZTE.
- Invensas Corporation v Renesas Electronics Corporation, Civil Action No. 11-448-GMS-CJB, retained by Renesas (deposition)
- In the Matter of Certain Non-volatile Memory Chips and Products Containing Same (ITC, Inv. No. 337-TA-916), retained by Macronix (deposition)
- Sandisk Corporation v. PNY Technologies, Inc., Case No. 1-11-CV-205928, retained by PNY (deposition)
- *TPK Touch Solutions, Inc. v. Wintek Electro-Optics Corporation, et al.*, 3:13-cv-02218-NC (N.D. Cal.), and associated issues in front of the patent board, retained by Wintek (deposition)
- GSI Technology, Inv. V. Cypress Semiconductor Corporation, IPR2014-00121 and associated issues in front of the patent board, retained by Cypress (deposition)
- Grail Semiconductor, Inc. v Mitsubishi, Case No. 1-07-CV-098590, retained by Mitsubishi
- AVM Technologies, LLC v. Intel Corporation, C.A. No. 15-33-RGA, retained by Intel (deposition and testimony)
- Intellectual Ventures LLV v. Toshiba, C.A. No. 13-453-SLR-SRF, retained by Toshiba (deposition and testimony)
- In the Matter of CERTAIN MEMORY MODEULS AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME, US ITC 337-TA-1023, retained by Hynix (deposition and testimony)
- In the Matter of CERTAIN INTEGRATED CIRCUITS WITH VOLTAGE REGULATORS AND PRODIUCTS CONTAINING THE SAME, US ITC 337-TA-1024, retained by Intel (deposition)

- Technology Properties Ltd, LLC v. LG et al, Case No. 3:12-cv-03880-VC, retained by defendants.
- Longitude Licensing Ltd. V Apple, Case 3:14-CV-04275-EDL, retained by Apple.
- KAIST IP v. Samsung et al, 2:16-cv-01314-JRG-RSP – retained by Samsung (deposition and trial).
- Toshiba Corporation v Lone Star Silicon Innovations LLC, IPR – retained by Toshiba
- Samsung Electronics Co Ltd. Vs PROMOS Technologies Inc, IPRs – retained by Samsung (deposition)
- Samsung Electronics Co. Ltd vs. UUSI LLC d/b/a Narton, IPRs – retained by Samsung (deposition)
- Carl Zeiss AG and ASML v Nikon, 2:17-cv-03221 RGK – retained by ASML and Zeiss (deposition and trial testimony)
- In the matter of CERTAIN MEMORY MODULES AND COMPONENTS THEREOF (ITC, Inv. No. 337-TA-1089), retained by SK Hynix (deposition and trial testimony)
- In the Matter of CERTAIN SOLID STATE STORAGE DRIVES, STACKED ELECTRONICS COMPONENTS, AND PRODUCTS CONTAINING SAME, US ITC 337-TA-1097, retained by Samsung and Hynix (deposition)
- In the Matter of CERTAIN INFOTAINMENT SYSTEMS, COMPONENTS THEREOF, AND AUTOMOBILES CONTAINING THE SAME, US ITC 337-TA-1119, retained by Renesas, Denso, Pioneer, Panasonic, Socionext, and Toyota (deposition and trial testimony)
- In the Matter of CERTAIN MOVABLE BARRIER OPERATOR SYSTEMS AND COMPONENTS THEREOF, US ITC 337-TA-1118, retained by Chamberlain (deposition and trial testimony)
- Fereydun Tabaian and Ahmad Ashrafzadeh v Intel Corporation, 3:18-cv-326-HZ., retained by Intel

*Active*

- Innovative Memory Systems, Inc. v. Micron Tech, Inc 14-cv-01480 and associated IPRs, retained by Micron (deposition)
- Kingston Technology Company v. Polaris Innovations Ltd, IPRs – retained by Kingston (deposition)

- Intel Corporation v. Tela Innovations, 18-cv-02848-WHO, retained by Intel (deposition)
- VLSI Technology LLC v. Intel Corporation, 1:18-cv-00966-CFC, retained by Intel
- X2Y Attenuators LLC v. Intel Corporation, Case No. 3:18-cv-1394-HZ, retained by Intel (deposition)
- In the Matter of CERTAIN TOUCH-CONTROLLED MOBILE DEVICES, COMPUTERS, AND COMPONENTS THEREOF, US ITC 337-TA-1162, retained by Samsung et al

## **List of Patents, Publications and Presentations**

### **Patents**

1. "Systems and methods for coarse and fine time of flight estimates for precise radio frequency localization in the presence of multiple communication paths", Seth, M., Kong, L., Ylamurto, T., Subramanian, V., US Patent 10,470,156
2. "Methods and apparatus for monitoring wound healing using impedance spectroscopy", Maharbiz, M., Subramanian, V., Arias, A.C., Swisher, S., Liao, A., Lin, M., Pavinatto, F., Khan, Y., Cohen, D., Leeftang, E., Roy, S., Harrison, M., Young, D., US Patent 10,463,293.
3. "Systems and methods for using radio frequency signals and sensors to monitor environments", T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,156,852.
4. "Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 10,104,508.
5. "Systems and methods for providing wireless asymmetric network architectures of wireless devices with power management features", V. Subramanian, E. Alon, V. Pavate, US Patent 10,028,220.
6. "Random delay generation for thin-film transistor based circuits", V Subramanian, M Mao, Z Wang, US Patent 9,985,664
7. "Systems and methods for determining locations of wireless sensor nodes in a network architecture having mesh-based features for localization", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,846,220
8. "Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,763,054
9. "Through silicon vias and thermocompression bonding using inkjet-printed nanoparticles", V. Subramanian and J. Sadie, US Patent 9,717,145
10. "Systems and methods for providing wireless asymmetric network architectures of wireless devices with anti-collision features", V. Subramanian, E. Alon, V. Pavate, US Patent 9,706,489
11. "Systems and methods for determining locations of wireless sensor nodes in an asymmetric network architecture", V. Subramanian, E. Alon, V. Pavate, US Patent 9,529,076
12. "Systems and methods for providing wireless sensor networks with an asymmetric network architecture", V. Subramanian, E. Alon, V. Pavate, US Patent 9,380,531
13. "Transparent metal oxide nanoparticle compositions, methods of manufacture thereof and articles comprising the same", V. Subramanian, S. K. Volkman, US Patent 9,343,202
14. "Three-dimensional nonvolatile memory and method of fabrication", M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 9,214,243
15. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 9,171,857
16. "Print compatible designs and layout schemes for printed electronics", Z. Wang, V. Subramanian, L. Cleveland, US Patent 9,155,202
17. "Wireless devices including printed integrated circuitry and methods for manufacturing and using the same", P. Smith, C. Choi, V. Pavate, J. M. Cleeves, V. Subramanian, R. Young, V. Biviano, US Patent 9,004,366.
18. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. Kouznetsov, US Patent, 8,981,457.
19. "High reliability surveillance and/or identification tag/devices and methods of making and using the same", V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, J. M. Cleeves, US Patent, 8,933,806.
20. "Surveillance devices with multiple capacitors", P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Moles, US Patent, 8,912,890.
21. "Pillar-shaped nonvolatile memory and method of fabrication", M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 8,897,056
22. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,853,765

23. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,823,076
24. "Random delay generation for thin-film transistor based circuits", V. Subramanian, M. Mao, Z. Wang, US Patent 8,810,298
25. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8,503,215
26. "Process-variation tolerant series-connected NMOS and PMOS diodes, and standard cells, tags, and sensors containing the same", V. Subramanian, P. Smith, US Patent 8,471,308
27. "Printed compatible designs and layout schemes for printed electronics", Z. Wang, V. Subramanian, L. Cleveland, US Patent 8,383,952
28. "Method for making surveillance devices with multiple capacitors", P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Molesa, US Patent 8,296,943
29. "High reliability surveillance and/or identification tag/devices and methods of making and using the same", V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,264,359
30. "High reliability surveillance and/or identification tag/devices and methods of making and using the same", V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,227,320
31. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8,208,282
32. "Reliable tag deactivation", J. M. Cleeves, V. Subramanian, US Patent 8,138,921
33. "Combined static and dynamic frequency divider chains using thin film transistors", V. Subramanian, US Patent 8,085,068
34. "Process-variation tolerant diode, standard cells including the same, tags and sensors containing the same, and methods for manufacturing the same", V. Subramanian, P. Smith, US Patent 7,932,537
35. "Three terminal nonvolatile memory Device with vertical gated diode", T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. G. Kouznetsov, US Patent 7,825,455
36. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7,816,189
37. "Multi-mode tags and methods of making and using the same", P. Smith, J. M. Cleeves, V. Pavate, V. Subramanian, US Patent 7,750,792
38. "Method of manufacturing complementary diodes", V. Subramanian, P. Smith, US Patent 7,528,017
39. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7,319,053
40. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7,265,000
41. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7,160,761
42. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7,157,314
43. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. Petti, I. Kouznetsov, M. G. Johnson, P. M. Farmwald, B. Herner, US Patent 7,129,538
44. "Patterning three dimensional structures", C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleeves, V. Subramanian, US Patent 7,071,565
45. "Monolithic three dimensional array of charge storage devices containing a planarized layer", T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. J. Petti, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, and B. Herner, US Patent 6,881,994
46. "Thermal processing for three dimensional circuits", V. Subramanian, J. M. Cleeves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6,770,939

47. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. G. Johnson, T. H. Lee, V. Subramanian, and P. M. Farnwald, US Patent 6780711
48. "Multigate semiconductor device with vertical channel current and method of fabrication", J. M. Cleaves and V. Subramanian, US Patent 6677204
49. "Thermal processing for three dimensional circuits", V. Subramanian, J. M. Cleaves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6624011
50. "Multigate semiconductor device with vertical channel current and method of fabrication", J. M. Cleaves and V. Subramanian, US Patent 6580124
51. "Patterning three dimensional structures", C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleaves, and V. Subramanian, US Patent 6627530
52. "Low cost three-dimensional memory array", M. Johnson, T. Lee, V. Subramanian, P. Farnwald, J. Knall, US Patent 6515888
53. "Integrated circuit structure including three-dimensional memory array", M. Johnson, T. Lee, V. Subramanian, P. M. Farnwald, J. M. Cleaves, US Patent 6385074.
54. "FINFET transistor structures having double gate channel extending vertically from a substrate and methods of manufacture", C. Hu, T.-J. King, V. Subramanian, L. Chang, X. Huang, Y.-K. Choi, J. T. Kedzierski, N. Lindert, J. Bokor, W.-C. Lee, US Patent 6413802
55. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farnwald, and J. M. Cleaves, US Patent 6185122.
56. "Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farnwald, and J. M. Cleaves, US Patent 6034882.
57. "Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farnwald, and J. M. Cleaves, US Patent 6351406.
58. "Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farnwald, and J. M. Cleaves, US Patent 6483736.

#### **Invited Magazine Articles, Books, Chapters, and Monographs**

1. Chapter in "Inkjet Technology for Digital Fabrication", Editors: Ian M. Hutchings, Graham D. Martin, Wiley, ISBN: 978-0470681985
2. Chapter in "Applications of Organic and Printed Electronics: A Technology-Enabled Revolution (Integrated Circuits and Systems)", Editor: E. Cantatore, ISB: 978-1-461-43159-6
3. Chapter in "Inkjet-based Micromanufacturing", Editors: Korvink, Smith, Shin, Wiley, ISBN: 978-3-527-31904-6
4. Chapter in "Organic Electronics II. More Materials and Applications", Editor: H. Klauk, Wiley, ISBN: 978-3-527-32647-1
5. Chapter in "Transparent Electronics: From Synthesis to Applications", Editors: A. Facchetti and T. Marks, Wiley, ISBN: 978-0-470-99077-3, 2010.
6. Chapter in "The chemistry of inkjet inks", Editor: S. Magdassi, World Scientific Publishing Company, ISBN: 978-9812818218, 2009
7. Chapter in "Organic Field-Effect Transistors", Editors: Z. Bao, and J. Locklin, CRC Press, ISBN: 978-0849380808, 2007
8. "Developments in printed RFID", V. Subramanian, Pira Publishing, UK, 2006.
9. "3D Chips: Future Possibilities", V. Subramanian, Silicon India, Feb 2003, pp. 24-25

#### **Invited Conference Presentations**

1. *Invited*, "High-Speed, High-Resolution Printing of Inorganic Devices", Vivek Subramanian and William J. Scheideler, 2018 Fall Materials Research Society Meeting, Boston, MA, Nov 25-30, 2018.
2. *Invited*, "Materials, Process, and Device Innovations for High-Performance Printed Electronics", PRINSE'18 – The 5<sup>th</sup> Printed Intelligence Industry Seminar on Manufacturing Solutions for Customer Needs and Vision to the Future, Oulu, Finland, Jan 31-Feb 1, 2018.

3. *Invited*, "Highly scaled gravure printed organic transistors for high-performance printed organic electronics", High-frequency printed and direct-written organic-hybrid integrated circuits (HEROIC) Workshop, Milan, Italy, Nov 8-10, 2017.
4. *Keynote*, "Printed Electronics: Innovations in Materials, Processes, and Devices", Association of International Metallizers, Coaters, and Laminators (AIMCAL) R2R Conference USA 2017, Tampa, FL, Oct-15-18, 2017.
5. *Invited*, "High-performance gravure printed organic transistors", 2017 European Materials Research Society Meeting, Strasbourg, France, May 22-26, 2017
6. *Invited*, "Printed Electronics: Innovations in Materials, Processes, and Devices", 2017 International Thin Film Transistor Conference (ITC 2017), Austin, TX, February 23-24, 2017.
7. *Invited*, "High-speed Printing of Transistors: From Inks to Devices", 2016 International Society of Coating Science and Technology Symposium (ISCST), Pittsburgh, PA, September 18-21, 2016.
8. *Keynote*, "Printed Electronics: Innovations in Materials, Processes, and Devices", 2016 Canadian Printable Flexible Wearable electronics Symposium (CPES2016), April 19-20, Oakville, Canada
9. *Keynote*, "Printed Electronics: Innovations in Materials, Processes, and Device", 2016 Society of Vacuum Coaters Techcon, Indianapolis, IN, May 10-13, 2016.
10. *Invited*, Subramanian, Vivek, Chung, Seungjun, Grau, Gerd and Scheideler, William J., "71-2: Invited Paper: Printed Transistors and MEMS for Large-Area Electronics", 2016 Society for Information Display Symposium, San Francisco, May 20-27, 2016.
11. *Keynote*, "Printed Electronics: Innovations in Materials, Processes, and Devices", 31<sup>st</sup> Philippine Chemistry Congress, Iloilo, Philippines, April 13-15, 2016.
12. *Keynote*, "Advanced Processes, Materials, and Devices for Emerging Printed Electronics Applications", 3<sup>rd</sup> Swiss Conference on Printed Electronics and Functional Materials, Neuchatel, Switzerland, Oct 1-2, 2015.
13. *Invited*, "High-performance printed organic transistors: Materials, processes, and devices", V. Subramanian, G. Grau, H. Kang, and R. Kitsomboonloha, 2015 American Chemical Society National Meeting and Exposition, Boston, MA, Aug 17<sup>th</sup>, 2015.
14. *Invited*, Subramanian, Vivek, Jaewon Jang, William Scheideler, and Sarah Swisher, "39.1: Invited Paper: Printed Inorganic Transistors Based on Transparent Oxides." In SID Symposium Digest of Technical Papers, vol. 46, no. 1, pp. 587-590. 2015.
15. *Plenary*, "Printed Electronics: Advanced Technologies Enabling New Applications", 2015 Flexible and Printed Electronics Conference, Monterey, CA, February 23-26, 2015.
16. *Invited*, "High-resolution gravure printing of organic thin film transistors for high-performance printed electronic systems", V. Subramanian, R. Kitsomboonloha, J. Cen, H. Kang, G. Grau, and W. J. Scheideler, Materials Research Society Fall Meeting, Boston, MA, Dec 3, 2014.
17. *Invited*, "Advanced printed electronics technologies for novel ubiquitous human interactive systems", 2014 CMOS Emerging Technologies Research Symposium, Grenoble, France, July 6-8, 2014.
18. *Invited*, "Printed Electronics: A pathway to functionally-rich systems", 64<sup>th</sup> annual IEEE Electronic Components and Technology Conference, Orlando, FL, May 27, 2014.
19. *Invited*, "Printed Electronics: The Confluence of Printing and Semiconductors", Canadian Printed Electronics Symposium, Montreal, Canada, April 9, 2013.
20. *Invited*, "Modeling, scaling, and integration of gravure printing for fast switching Organic FETs", V. Subramanian, S. J. S. Morris, H. Kang, Materials Research Society Fall 2012 Meeting, Boston, MA, Nov 25-30, 2012
21. *Invited*, "Printed Nanoparticles as routes to high-performance printed conductors: Synthesis, Printing Processes, and Device Applications", V. Subramanian, H. Kang, R. Kitsomboonloha, and S. K. Volkman, The 2012 International Conference on Flexible and Printed Electronics ICFPE2012, Tokyo, Japan, September 6th - 8th, 2012
22. *Invited*, "Advanced Printing Processes for High-Performance Printed Transistors", V. Subramanian, Flextech Workshop on Printing Electronics - Ink and Substrate Interactions, Kalamazoo, MI, August 1-2, 2012
23. *Invited*, "High-performance Printed Transistors: Materials, Processes, and Devices", V. Subramanian, 2nd CPEM International Symposium "Organic Semiconductors and Printed Electronics", Gyeonggi, South Korea, May 10th, 2012.

24. *Invited* “Highly-Scaled Gravure and Inkjet Printed Organic Transistors: Tools, Processes, and Devices”, Hongki Kang & Vivek Subramanian, 2012 Flextech Flexible Electronics and Display Conference, Phoenix, AZ, Feb 5-9, 2012.
25. *Plenary* “Nanomaterials for printed electronics: synthesis, design, and applications”, V. Subramanian, International Conference on Nano Science and Nano Technology, Sunchon, Korea, November 11<sup>th</sup>, 2011.
26. *Invited* “Advances in scaling of printed transistors”, V. Subramanian, International Seminar on Printed Electronics, Seoul, Korea, June 8<sup>th</sup>, 2011.
27. *Invited* “High-Performance Fully Printed Transistors: Materials, Processes, and Device Characteristics”, V. Subramanian, H. Tseng, R. Kitsomboonloha, and A. de la Fuente Vornbrock, 2011 Electrochemical Society Meeting, Montreal, Canada, May 2011
28. *Invited* “From Droplets to Devices: Printed Transistor Processes, Integration, and Characteristics”, Vivek Subramanian, Daniel Soltman, Huai-Yuan Tseng, Rungrot Kitsomboonloha and Alejandro de la Fuente Vornbrock, Materials Research Society Spring Meeting, San Francisco, CA, April 2011
29. *Keynote* “Printed electronics: Innovations in tools, materials, devices, and applications”, V. Subramanian, 2011 Korea Printed Electronics Association (KoPeA) meeting, Seoul, Korea, March 2011
30. *Keynote* “Printed RF tags and sensors: the confluence of printing and semiconductors”, V. Subramanian, F. Liao, and H-Y. Tseng, The European Microwave Integrated Circuits Conference 2010, Paris, France, September 2010.
31. *Invited* “Droplet-on-demand direct patterning of active materials: materials, modeling, and integration”, V. Subramanian, The 2010 IEEE Lithography Workshop, Kuai, Hawaii, November 2010
32. *Plenary* “Printed electronics: where are we, and where are we going”, V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.
33. *Keynote* “Printed RFID: Technology Trends and Outlook”, V. Subramanian, IEEE International Conference on RFID 2010, Orlando, Florida, April 2010.
34. *Invited* “Mechanistic studies on sintering of nanoparticles for formation of solution-processed thin films”, 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.
35. *Invited* “Printed Electronics: the confluence of printing and semiconductors”, Vivek Subramanian, 2009 International Conference on Flexible and Printing Electronics, Jeju Island, Korea, Nov 2009.
36. *Invited* “Organic Transistor Vapor and Biosensors – Technology Status and Implementation Issues”, Vivek Subramanian, Frank Liao, Lakshmi Jagannathan, Electrochemical Society Meeting, Vienna, Austria, October 2009.
37. *Invited* “Printed transistors for low-cost electronics: the confluence of printing and printable electronic materials”, Vivek Subramanian, Alejandro de la Fuente Vornbrock, Steven Moles, Daniel Soltman, Huai-Yuan Tseng, and Steven K. Volkman, SPIE Optics + Photonics, August 2-6, 2009, San Diego, CA
38. *Invited* “Printed Zinc Oxide Based Electronics: Materials, Devices, and Outlook”, V. Subramanian, S. K. Volkman, and D. R. Redinger, LOPE-C, June 23-25, 2009, Frankfurt, Germany
39. *Invited* “Printed Devices for Low-Cost Electronics: Technology Status and Outlook”, V. Subramanian, PETEC Inaugural Event, March 17, 2009, Durham, United Kingdom
40. *invited* “Printed Electronic Tags and Sensors for Smart Packaging Applications”, Vivek Subramanian, Josephine Chang, Lakshmi Jagannathan, Frank Liao, Steve Moles, David Redinger, Daniel Soltman, Huai-Yuan Tseng, Steve Volkman, Shong Yin, 2009 Flexible Electronics and Display Conference, Phoenix, AZ, Feb 2-5, 2009.
41. *invited* “Electronic Nose Sensors for Consumer Packaging”, V. Subramanian, IDTechEx Printed Electronics USA, San Jose, CA, Dec 2-5, 2008.
42. *invited* “Solution-Processed Transparent Transistors for Low-Cost, Flexible Displays”, V. Subramanian, S. K. Volkman, and D. R. Redinger, LEOS 2008: The 21<sup>st</sup> Annual Meeting of the IEEE Lasers and Electro-Optics Society, Newport Beach, CA, 9-13 November, 2008.
43. *invited* “Organic chemical and biosensors for smart packages”, V. Subramanian, IDTechEx Printed Electronics Asia, Tokyo, Japan, Oct 8-9, 2008.
44. *invited* “Printed Electronics for Low-Cost Tags, Displays, and Sensors”, V. Subramanian, 1<sup>st</sup> International Conference on R2R Printed Electronics, Seoul, Korea, April 30-May 2, 2008.

45. *invited* "Printed organic RFID tags: technology, roadmaps, and challenges", V. Subramanian, 1<sup>st</sup> Plastic Electronics Asia Conference and Showcase, Seoul, Korea, June 24-26, 2008
46. *invited* "Power supply considerations and solutions for printed electronic tags and sensors", V. Subramanian, IDTechEx Printed Electronics Europe, Dresden, Germany, April 8-9, 2008
47. *invited* "Printed Chemical and Biosensors: Technology, Design and Challenges", GOSPEL Workshop on Plastic Chemical Sensors, Dresden, Germany, April 9, 2008
48. *Plenary* "Printed Electronics For Low-Cost Electronic Systems: Technology Status and Application Development", Vivek Subramanian, Josephine B. Chang, Alejandro de la Fuente Vornbrock, Daniel C. Huang, Lakshmi Jagannathan, Frank Liao, Brian Mattis, Steven Moles, David R. Redinger, Daniel Soltman, Steven K. Volkman, Qintao Zhang, 38<sup>th</sup> European Solid State Device Research Conference, Edinburgh, Scotland, September 15-19, 2008
49. *invited* "Printed Organic Transistors for Low-cost Tags, Displays, and Sensors: Technology, Modeling and Challenges", Vivek Subramanian, Alejandro de la Fuente Vornbrock, Huai-Yuan Tseng and Shong Yin, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008.
50. *invited* "Printed Electronics for Low-Cost Tags and Sensors", Vivek Subramanian, Sixth Annual Workshop on Microelectronics and Electron Devices, April 18, 2008.
51. *invited* "Printed organic RF tags, chemical sensors and biosensors", Vivek Subramanian, International Symposium for Flexible Electronics and Display, Hsinchu, Taiwan, Nov 18, 2007.
52. *invited* "Printed Tags and Sensors for RFID: Opportunities and Challenges", Vivek Subramanian, Printed Electronics USA 2007, San Francisco, CA, Nov 14, 2007.
53. *invited* "Printed RFID Tags: Materials, Processes, and Devices", Vivek Subramanian, Daniel Soltman, Daniel Huang, Steven Moles, 2007 AiChE Annual Meeting, Salt Lake City, UT, Nov. 8, 2007.
54. *invited* "Printed organic RFID tags: technology, roadmaps, and challenges", Vivek Subramanian, 3<sup>rd</sup> Global Plastic Electronics Conference and Showcase, Frankfurt, Germany, Oct 30, 2007.
55. *invited* "Printed organic transistors: technology, characteristics, and modeling", Vivek Subramanian, Alejandro de la Fuente Vornbrock, Daniel Soltman, Huai-Yuan Tseng, and Steve Moles, 212<sup>th</sup> meeting of the Electrochemical Society, Washington, DC, Oct 8, 2007.
56. *invited* "Printed electronic tags and sensors - device, materials, and circuit issues", Vivek Subramanian, 2007 Organic Electronics Conference and Exhibition, Frankfurt, Germany, Sept 25, 2007.
57. *invited* "Inkjet printing of transistors, diodes, and passive components for smart tags", Vivek Subramanian, Innovations in Inkjet: 3<sup>rd</sup> DPI Inkjet Workshop, Eindhoven Institute of Technology, Netherlands, June 28-29, 2007.
58. *invited* "Printed organic transistors", A. de la Fuente and V. Subramanian, Industry Forum on Printed Electronics, Chicago, IL, April 23-24, 2007
59. *invited* "From Materials to Circuits: Implications of printed materials on printed RFID", V. Subramanian, 2007 Pira printed RFID conference, Frankfurt, Germany, June 4-6, 2007.
60. *keynote* "Droplet on demand lithography: An enabling technology for low-cost electronics", V. Subramanian, A. de la Fuente Vornbrock, S. Moles, D. Redinger, Q. Zhang, and S. K. Volkman, SPIE Advanced lithography, 27<sup>th</sup> February, 2007
61. *invited* "Printed RFID tags: performance needs and technology trends", V. Subramanian, 2007 IDTechEx Smart labels USA, Boston, MA, February 20-23, 2007.
62. *keynote* "Printed Organic Transistors for low-cost tagging and sensing applications", V. Subramanian, J. Chang, A. de la Fuente Vornbrock, S. Moles, D. Soltman, and Q. Zhang. 6<sup>th</sup> International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, Tokyo, January 15<sup>th</sup>-18<sup>th</sup>, 2007.
63. *invited* "Nano Inks for Printed RFID", V. Subramanian, Pira Nanoscale Inks and Pigment Technologies Conference, Chicago, IL, Sept 27-28, 2006.
64. *invited* "Toward Printed RFID: Materials, Processes, and Devices", V. Subramanian, 5<sup>th</sup> Annual Printed Electronics and Displays Conference and Trade Fair, Las Vegas, Oct 11-13, 2006.
65. *invited* "Inkjetted Organic Transistors for Smart Tagging Applications", Vivek Subramanian, Jean M. J. Frechet, Steven Moles, Josephine Chang, Amanda R. Murphy, Alejandro de la Fuente Vornbrock, Steven Volkman, 2006 AiChE Annual Meeting, Nov 17<sup>th</sup>, 2006

66. *invited focal paper* "All-printed electronics: Materials, Devices, and Circuit Implications", V. Subramanian, J. Chang, S. Molesa, D. Redinger, and S. Volkman, Digital Fabrication 2006, Denver, CO, Sept 17-22, 2006.
67. *invited* "Printed transistors and passive components for low-cost electronics applications", V. Subramanian, J. B. Chang, S. E. Molesa, S. K. Volkman, and D. R. Redinger, International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA) April, 2006, pp. 68-9.
68. *invited* "Advanced printed materials and devices for RFID applications", V. Subramanian, IDTechEx Printed Electronics Europe, April 19-21, 2006.
69. *invited* "Printed Electronic Nose Vapor Sensors for Consumer Product Monitoring", V. Subramanian, J. Lee, V. Liu, S. Molesa, IEEE International Solid State Circuits Conference, Paper 15.3, February, 2006.
70. *invited* "Nanotechnology in Printed Electronics: Nanoparticles, Nanorods, and Nanowhy", V. Subramanian, Pira Pack Electronics Conference, January 25-26, 2006.
71. *invited* "All-printed RFID Tags: Materials, Devices, and Circuit Implications", Vivek Subramanian, Paul C. Chang, Daniel Huang, Josephine B. Lee, Steven E. Molesa, David R. Redinger, and Steven K. Volkman, VLSI Design, 2006, Hyderabad India, Jan 2006.
72. *invited* "Printed organic transistors: materials and technology", Vivek Subramanian, Pacificchem 2005: American Chemical Society Pacific Basin meeting, December 15-20, 2005, Honolulu, HI,
73. *invited* "Low-cost arrayed gas sensors for environmental monitoring", Vivek Subramanian, Josephine Lee and Vincent Liu, Materials Research Society Fall Symposium, Paper S2.1, Boston, MA, December 2005.
74. *invited* "Prospects for All-printed RFID: Materials, Devices, Circuits", V. Subramanian, International Workshop on Radio Frequency Identification (RFID) and Wirelss Sensors, 11-13 November, 2005, Kanpur, India.
75. *invited* "Printed electronics for low-cost tagging applications", V. Subramanian, 2005 International Symposium on Flexible Electronics and Display, Hsinchu, Taiwan, October 2005.
76. *invited* "Printed electronic nose gas sensors", Vivek Subramanian, Plastic Electronics 2005, Frankfurt, Germany, Oct 4-5, 2005
77. *invited* "Uses of nanotechnology in printed electronics", Vivek Subramanian, Printed Electronics 205, Pira International, Thistle Marble Arch, London, UK, Sept 14-15, 2005
78. *invited* "Printed organic transistors for low-cost RFID applications", Vivek Subramanian, Proceedings of SPIE-The International Society for Optical Engineering vol. 5940, (594013/1-594013/9), pp. 170-178, 2005.
79. *invited* "Advanced printed materials and devices for ultra-low-cost RFID", Vivek Subramanian, Printed RFID: Achieving low cost tags through printed electronics – Pira International, Gatwick, Surrey, UK, May 10-11, 2005.
80. *Plenary session invited talk* "Printed Organic Transistors for Ultra-low-cost RFID Applications", Vivek Subramanian, Paul C. Chang, Josephine B. Lee, Steven E. Molesa, and Steven K. Volkman, Polytronic 2004: 4th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, Portland, Oregon, USA, 12 September 2004.
81. *invited* "Materials, Device, and Circuits Issues for low-cost printed RFID", V. Subramanian, 2<sup>nd</sup> Cintelliq Organic Semiconductor Conference, 2004 (OSC-2004), Cambridge, England, October 2004.
82. *invited* "All-printed flexible organic thin film transistors: Current status and outlook for the future", V. Subramanian, J. M. J. Fréchet, P. C. Chang, D. C. Huang, J. B. Lee, F. Liao, B. A. Mattis, S. Molesa, A. R. Murphy, D. R. Redinger, and S. K. Volkman, 206<sup>th</sup> meeting of the Electrochemical Society, Honolulu, HI, October 2004.
83. *invited* "Nanoscale organic transistors: towards gain in molecular devices", V. Subramanian, P. C. Chang, J. B. Lee, T. Le, A. Murphy, J. M. J. Frechet, and A. Liddle, 2004 IEEE Nanoscale Devices and Systems Integration Conference, Miami, FL, 2004.
84. *invited* "Towards Printed Low-Cost RFID Tags: Device, Materials and Circuit Technologies", V. Subramanian, 2nd Advanced Technology Workshop on Printing an Intelligent Future: Printed Organic and Molecular Electronic Technologies, Boston, MA, March 16-19, 2003.
85. *invited* "Prospects for organic semiconductor based devices and circuits: applications, performance, and reliability considerations", V. Subramanian, 2002 Topical Research Conference on Reliability, Oct 2002.
86. *invited* "FinFET - quasi-planar double-gate MOSFET", S. H. Tang, L. Chang, N. Lindert, Y-K. Choi, W-C. Lee, X. Huang, V. Subramanian, J. Bokor, T-J. King, C. Hu, 20001 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 118-119, 437, 2001.

87. *invited* "3-D ICs with Multiple Si Layers: Performance Analysis, and Technology", K. Saraswat, K. Banerjee, A. Joshi, P. Kalavade, S. Souri, and V. Subramanian, *presented at The Fifth International Symposium on Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues*, 197th meeting of the Electrochemical Society, Toronto, Ontario, Canada, May 14-18, 2000.
88. *invited* "Novel 3-D Structures", K. C. Saraswat, S. J. Souri, V. Subramanian, A. R. Joshi, and A. W. Wang, 1999 IEEE International SOI Conference Proceedings, pp. 54-55.
89. *invited* "Seeding Technology for High Performance TFTs", K. C. Saraswat and V. Subramanian, Proceedings of the Electronic Display Forum 98, ELAJ/SEMI, Yokohama, April 1998, pp. 2.7-2.15.
90. *invited* "A Low-Temperature Polycrystalline Si TFT Technology for Large-Area AMLCD Drivers", K. C. Saraswat, V. Subramanian, and S. Jurichich, Polycrystalline Thin Films III - Structure, Texture, Properties, and Applications, MRS Symposium Proceedings pp 439-449, 1997.
91. *invited* "A low temperature polycrystalline SiGe CMOS TFT technology for large area AMLCD drivers", K. C. Saraswat, S. Jurichich, T.-J. King, V. Subramanian, and A. Wang, Proceedings of Thin Film Transistor Technologies III, ECS Symposium, 1996, pp. 186-196.

#### Journal Papers

1. *invited* William Scheideler and Vivek Subramanian, "Printed flexible and transparent electronics: enhancing low-temperature processed metal oxides with 0D and 1D nanomaterials", 2019 Nanotechnology 30 272001
2. R. Kumar, K. M. Johnson, N. X. Williams, V. Subramanian, "Scaling Printable Zn-Ag<sub>2</sub>O Batteries for Integrated Electronics", Adv. Energy Mater. 2019, 1803645.
3. William J. Scheideler, Matthew W. McPhail, Rajan Kumar, Jeremy Smith, and Vivek Subramanian, "Scalable, High-Performance Printed InOx Transistors Enabled by Ultraviolet-Annealed Printed High-k AlOx Gate Dielectrics", ACS Applied Materials & Interfaces 2018 10 (43), 37277-37286.
4. J. Smith, S. Chung, J. Jang, C. Biao, V. Subramanian, "Solution-processed complementary resistive switching arrays for associative memory", IEEE Transactions on Electron Devices 64 (10), pp 4310, 2017
5. A. Zeumault, V. Subramanian, "Use of high-k encapsulation to improve mobility in trap-limited metal oxide semiconductors", physica status solidi (b) 254 (10), 1700124, 2017
6. A. Zeumault, W. Scheideler, V. Subramanian, "Electrostatic tuning of spray-deposited ZnO for controlled mobility enhancement", Advanced Functional materials, 27 (30), pp. 1701021, 2017
7. W. J. Scheideler, R. Kumar, A. R. Zeumault, V. Subramanian, "Low-Temperature-Processed Printed Metal Oxide Transistors Based on Pure Aqueous Inks", Advanced Functional Materials 2017, 1606062.
8. Jaewon Jang, Vivek Subramanian, "Effect of electrode material on resistive switching memory behavior of solution-processed resistive switches: Realization of robust multi-level cells", Thin Solid Films, Volume 625, Pages 87-92, 1 March 2017.
9. S. Chung, M. A. U. Karim, H. J. Kwon, W. Scheideler and V. Subramanian, "A High-Speed Inkjet-Printed Microelectromechanical Relay With a Mechanically Enhanced Double-Clamped Channel-Beam," Journal of Microelectromechanical Systems, vol. 26, no. 1, pp. 95-101, Feb. 2017.
10. G. Grau, E. J. Frazier, and V. Subramanian, "Printed unmanned aerial vehicles using paper-based electroactive polymer actuators and organic ion gel transistors", Nature Microsystems & Nanoengineering, vol 2, pp. 16032, 2016
11. *invited* Gerd Grau, Jialiang Cen, Hongki Kang, Rungrot Kitsomboonloha, William J Scheideler, and Vivek Subramanian "Gravure-printed electronics: recent progress in tooling development, understanding of printing physics, and realization of printed devices", IOP Journal of Flexible and Printed Electronics, vol. 1, No. 2, pp. 023002, 2016
12. Scheideler, William J., Jeremy Smith, Igal Deckman, Seungjun Chung, Ana Claudia Arias, and Vivek Subramanian. "A robust, gravure-printed, silver nanowire/metal oxide hybrid electrode for high-throughput patterned transparent conductors." Journal of Materials Chemistry C 4, no. 15 (2016): 3248-3255.
13. Karim, Muhammed Ahsan Ul, Seungjun Chung, Elad Alon, and Vivek Subramanian. "Fully Inkjet-Printed Stress-Tolerant Microelectromechanical Reed Relays for Large-Area Electronics." Advanced Electronic Materials (2016).
14. Khan, Yasser, Felipe J. Pavinatto, Monica C. Lin, Amy Liao, Sarah L. Swisher, Kaylee Mann, Vivek Subramanian, Michel M. Maharbiz, and Ana C. Arias. "Bioelectronic Interfaces: Inkjet-Printed Flexible Gold Electrode Arrays for Bioelectronic Interfaces (Adv. Funct. Mater. 7/2016)." Advanced Functional Materials 26, no. 7 (2016): 981-981.

15. Jang, Jaewon, Seungjun Chung, Hongki Kang, and Vivek Subramanian. "P-type CuO and Cu<sub>2</sub>O transistors derived from a Sol–Gel Copper (II) acetate monohydrate precursor." *Thin Solid Films* (2016).
16. Grau, Gerd, and Vivek Subramanian. "Fully High-Speed Gravure Printed, Low-Variability, High-Performance Organic Polymer Transistors with Sub-5 V Operation." *Advanced Electronic Materials* (2016).
17. Zeumault, Andre, and Vivek Subramanian. "Mobility Enhancement in Solution-Processed Transparent Conductive Oxide TFTs due to Electron Donation from Traps in High-k Gate Dielectrics." *Advanced Functional Materials* (2016).
18. Zeumault, Andre, William Scheideler, Gerd Grau, Jeremy Smith, and Vivek Subramanian. "Patterning of Solution-Processed, Indium-Free Oxide TFTs by Selective Spray Pyrolysis." *Advanced Electronic Materials* (2015).
19. Jang, Jaewon, Hongki Kang, Himamshu C. Nallan Chakravarthula, and Vivek Subramanian. "Fully Inkjet-Printed Transparent Oxide Thin Film Transistors Using a Fugitive Wettability Switch." *Advanced Electronic Materials* 1, no. 7 (2015).
20. Grau, Gerd, Rungrot Kitsomboonloha, Hongki Kang, and Vivek Subramanian. "High performance printed organic transistors using a novel scanned thermal annealing technology." *Organic Electronics* 20 (2015): 150-157.
21. Zeumault, Andre, and Vivek Subramanian. "Improved Technique for Quantifying the Bias-Dependent Mobility of Metal-Oxide Thin-Film Transistors." *Electron Devices, IEEE Transactions on* 62, no. 3 (2015): 855-861.
22. Swisher, Sarah L., Steven K. Volkman, and Vivek Subramanian. "Tailoring Indium Oxide Nanocrystal Synthesis Conditions for Air-Stable High-Performance Solution-Processed Thin-Film Transistors." *ACS applied materials & interfaces* 7, no. 19 (2015): 10069-10075.
23. Koo, Hyunmo, Wookyu Lee, Yunchang Choi, Junfeng Sun, Jina Bak, Jinsoo Noh, Vivek Subramanian, Yasuo Azuma, Yutaka Majima, and Gyoujin Cho. "Scalability of carbon-nanotube-based thin film transistors for flexible electronic devices manufactured using an all roll-to-roll gravure printing system." *Scientific reports* 5 (2015).
24. "Perpendicular Magnetization Switching via Current induced Spin-Orbit Torques on Flexible Substrate", O.J. Lee, L. You, J. Jang, V. Subramanian, S. Sahahuddin, *Bulletin of the American Physical Society* 60, 2015.
25. "High-Performance Inkjet-Printed Four-Terminal Microelectromechanical Relays and Inverters", Seungjun Chung, Muhammed Ahsan Ul Karim, Hyuk-Jun Kwon, and Vivek Subramanian, *Nano Letters*, 15 (5), pp 3261–3266, 2015.
26. *Invited* Subramanian, Vivek, Jialiang Cen, Alejandro de la Fuente Vornbrock, Gerd Grau, Hongki Kang, Rungrot Kitsomboonloha, Daniel Soltman, and Huai-Yuan Tseng. "High-Speed Printing of Transistors: From Inks to Devices." *Proceedings of the IEEE* 103, no. 4 (2015): 567-582.
27. Scheideler, William J., Jaewon Jang, Muhammed Ahsan Ul Karim, Rungrot Kitsomboonloha, Andre Zeumault, and Vivek Subramanian. "Gravure-Printed Sol–Gels on Flexible Glass: A Scalable Route to Additively Patterned Transparent Conductors." *ACS applied materials & interfaces* 7, no. 23 (2015): 12679-12687.
28. Lee, OukJae, Long You, Jaewon Jang, Vivek Subramanian, and Sayeef Salahuddin. "Flexible spin-orbit torque devices." *Applied Physics Letters* 107, no. 25 (2015): 252401.
29. Kitsomboonloha, Rungrot, Hongki Kang, Gerd Grau, William Scheideler, and Vivek Subramanian. "MHz-Range Fully Printed High-Performance Thin-Film Transistors by Using High-Resolution Gravure-Printed Lines." *Advanced Electronic Materials* 1, no. 12 (2015).
30. Swisher, Sarah L., Monica C. Lin, Amy Liao, Elisabeth J. Leeftang, Yasser Khan, Felipe J. Pavinatto, Kaylee Mann et al. "Impedance sensing device enables early detection of pressure ulcers in vivo." *Nature communications* 6 (2015).
31. "A Stencil Printed, High Energy Density Silver Oxide Battery Using a Novel Photopolymerizable Poly(acrylic acid) Separator", K. Braam and V. Subramanian, *Advanced Materials*, Vol. 27, 689-694, 2015
32. "Megahertz-class printed high mobility organic thin-film transistors and inverters on plastic using attoliter-scale high-speed gravure-printed sub-5µm gate electrodes", H. Kang, R. Kitsomboonloha, K. Ulmer, L. Stecker, G. Grau, J. Jang, V. Subramanian, *Organic Electronics*, vol. 15, 3639-3647, 2014.
33. "Exploitation of the coffee-ring effect to realize mechanically enhanced inkjet-printed microelectromechanical relays with U-bar-shaped cantilevers", S Chung, MAU Karim, M Spencer, HJ Kwon, CP Grigoropoulos, E Alon, V. Subramanian, *Applied Physics Letters* 105 (26), 261901, 2014.
34. "Printed Transistors on Paper: Towards Smart Consumer Product Packaging", G. Grau, R. Kitsomboonloha, S. L. Swisher, H. Kang, and V. Subramanian, *Advanced Functional Materials*, Vol. 24, 5067-5074, 2014.

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#### Conference Presentations

1. R. Kumar, E. Kedzie, B. D. McCloskey, and V. Subramanian, "Characterizing Zn Corrosion in Printed Zn-Air batteries Via Operando Dens, XRD, and XAS", Electrochemical Conference on Energy and the Environment: Bioelectrochemistry and Energy Storage, MA2019-04 July 21-26, 2019, Glasgow, Scotland
2. Carlos Biao, Matt McPhail, Vivek Subramanian and Oscar Dubon, "Comprehensive Multifactorial Studies on the Degradation of Perovskite Solar Cells in Operation", 2019 Spring Materials Research Society Meeting, Phoenix, AZ, April 22-26, 2019.
3. Rajan Kumar, Jessica E. Nichols, Bryan D. McCloskey, and Vivek Subramanian, "Low-Temperature-Processing of Printed Cathodes for Aqueous Metal-Air Batteries", ECS AiMES 2018 Meeting, September 30, 2018 - October 4, 2018, Cancun, Mexico
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5. "Inkjet-printed MEM relays for active solar cell routing", S Patel, WJ Scheideler, MAU Karim, V Subramanian, Micro Electro Mechanical Systems (MEMS), 2018 IEEE, 616-619
6. "Back-channel engineering of ultrathin printed indium oxide transistors for carbon dioxide sensing", Y. Kobayashi, W. Scheideler, V. Subramanian, 2017 Materials Research Society Fall Meeting, Boston, MA, Nov 28, 2017.

7. "Morphological Control of Gravure Printed Perovskite Films", M. McPhail and V. Subramanian, 2017 Materials Research Society Fall meeting, Boston, MA, Nov 29, 2017.
8. "Improving high-speed nanomaterial printing with sub-process-decoupled gravure printer design", W. Scheideler, V. Subramanian, ASME 2017 Conference on Smart Materials, Adaptive Structures, and Intelligent Systems, Snowbird, UT, Sept 18-20, 2017
9. "Development of a printed cathode and catalyst layer for printed zinc-air batteries, R. Kumar, N. Williams, and V. Subramanian, 232<sup>nd</sup> ECS Meeting, National Harbor, MD, Oct 1-5, 2017.
10. "UV-annealing-enhanced stability in high-performance printed InOx transistors, W. Scheideler, V. Subramanian, 2017 IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Toyama, Japan, Feb 28-Mar 2, 2017.
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15. "High-resolution gravure printed lines: proximity effects and design rules", G. Grau, W. J. Scheideler, V. Subramanian, SPIE Organic Photonics+ Electronics (pp. 95690B-95690B). International Society for Optics and Photonics, 2015
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29. "Simulation and Experimental Characterization of Cell Filling During Highly-Scaled Gravure Printing for Printed Electronics Applications", A. Cen, R. Kitsomboonloha, and V. Subramanian, 2013 Fall Meeting of the Materials Research Society, Boston, Ma, Dec 1-6, 2013.
30. **Best paper award** "Droplet-on-demand Inkjet-Filled TSVs as a pathway to cost-efficient chip stacking", J. Sadie, N. Quack, M. Wu, and V. Subramanian, IMAPS 2013 - 46<sup>th</sup> International Symposium on Microelectronics, Orlando, FL, Sept 30 – Oct 3, 2013.
31. "Through silicon vias and thermocompression bonding using inkjet-printed gold nanoparticles for heterogeneous MEMS Integration", N. Quack, J. Sadie, V. Subramanian, and M. C. Wu, The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, Barcelona, Spain, June 16-20, 2013.
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34. "High Performance Solution-Processed Thin-Film Transistors Based on In<sub>2</sub>O<sub>3</sub> Nanocrystals: Investigating Effects of Annealing Conditions and Gate Dielectric", Sarah L. Swisher, Steve Volkman, and Vivek Subramanian, 2013 Large Area, Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, June 11-13, 2013.
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