

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE Technology Group Co., Ltd.,
Petitioner,

v.

Paneltouch Technologies LLC,
Patent Owner.

U.S. Patent No. 8,803,836
Original Issue Date: August 12, 2014
Title: DISPLAY DEVICE WITH TOUCH PANEL

Case No. IPR2025-01246

DECLARATION OF DR. VIVEK SUBRAMANIAN

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CHALLENGED CLAIM LISTING

Claim	Limitation No.	Limitation
1	[1-PRE]	A display device with a touch panel comprising:
	[1-A]	the touch panel which includes a first substrate, and a second substrate arranged to face the first substrate in an opposed manner, wherein:
	[1-B]	the first substrate and the second substrate each include a detection area configured to detect a coordinate and an outside area in which external terminals are formed,
	[1-C]	the first substrate includes a plurality of first lines each configured to detect a coordinate, the second substrate includes a plurality of second lines in the detection area which face the first substrate,
	[1-D]	each of the plurality of first lines and the plurality of second lines are configured of metal, each of the plurality of first lines is black in color,
	[1-E]	a polarizing plate is arranged on the first substrate at a side opposite to the second substrate,
	[1-F]	the first substrate includes a plurality of wiring groups, each of the plurality of wiring groups include at least two first lines of the plurality of first lines, and the at least two first lines of each of the plurality of wiring groups are combined with each other.
2	2	The display device with a touch panel according to claim 1, wherein the polarizing plate comprises a linear polarizing plate.
3	3	The display device with a touch panel according to claim 1, wherein the polarizing plate comprises a circular polarizing plate.

Claim	Limitation No.	Limitation
4	4	The display device with a touch panel according to claim 1, wherein the second lines comprise a second electrode each configured to detect a coordinate.
5	5	The display device with a touch panel according to claim 1, wherein a transparent electrode connects to the second lines.
6	6	A display device with a touch panel according to claim 1, wherein the at least two first lines of each of the plurality of wiring groups are combined with each other by a pad member.
7	7	A display device with a touch panel according to claim 1, wherein a transparent conductive film overlaps the plurality of the second lines in plan view, and wherein the transparent conductive film is electrically connected to the plurality of the second lines.
8	[8-PRE]	A display device with a touch panel comprising:
	[8-A]	the touch panel including a first substrate having a detection area to detect a coordinate and an outside area in which external terminals are formed, a plurality of first lines to detect the coordinate in the detection area, a plurality of second lines to detect the coordinate in the detection area, each of the plurality of first lines traversing each of the plurality of second lines;
	[8-B]	an organic luminescence electric device panel which is adhered to the touch panel; and
	[8-C]	a circular polarizing plate which is adhered to the touch panel at a side opposite to the organic luminescence electric device panel.
9	9	A display device with a touch panel according to claim 8, wherein each of the plurality of first lines and the plurality of second lines is made of metal, and wherein each of the plurality of first lines is black in color.

Claim	Limitation No.	Limitation
10	10	A display device with a touch panel according to claim 9, wherein the touch panel includes a plurality of wiring groups, wherein each of plurality of wiring groups includes at least first two lines of the plurality of first lines, and wherein the at least two first lines in each of plurality of wiring groups are combined with each other.
11	11	A display device with a touch panel according to claim 10, wherein the at least two first lines of each of the plurality of wiring groups are combined with each other by a pad member.
12	12	A display device with a touch panel according to claim 9, wherein a transparent conductive film overlays the plurality of the second lines, and wherein the transparent conductive film is electrically connected to the plurality of the second lines.
13	13	A display device with a touch panel according to claim 10, wherein a transparent conductive film overlays the plurality of the first lines, and wherein the transparent conductive film is electrically connected to the plurality of the first lines.
14	14	A display device with a touch panel according to claim 9, wherein a transparent conductive film underlays the plurality of the second lines, and wherein the transparent conductive film is electrically connected to the plurality of the second lines.
15	15	A display device with a touch panel according to claim 10, wherein a transparent conductive film underlays the plurality of the first lines, and wherein the transparent conductive film is electrically connected to the plurality of first lines.

I. INTRODUCTION

I, Dr. Vivek Subramanian, declare as follows:

1. I have been retained by counsel for BOE Technology Group Co., Ltd., (“BOE”) in the above-captioned *inter partes* review as an independent consultant to offer opinions regarding the validity of the challenged claims in U.S. Patent No. 8,803,836 (the “’836 Patent”).

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration – supplemented with my own knowledge and experience in the field. Should new materials, analyses, or opinions be introduced subsequent to the filing of this Declaration, I reserve the right to provide supplementary Declarations to the extent necessary to address any such newly introduced items.

3. If requested, I am prepared to explain in a deposition or at a trial before the Patent Trial and Appeal Board (the “Board”) the technology disclosed in the ’836 Patent, including the state of the art around 2009, the earliest alleged priority date of the ’836 Patent. Similarly, I am prepared to explain the technology disclosed in the prior art references cited herein. This may include, among other things, background information on the fields of display devices and touch panels.

II. QUALIFICATIONS

4. My qualifications to testify as an expert in display devices and touch

panels are set forth in my *curriculum vitae*, attached as Appendix A. I have decades of experience as an engineer, scientist, and consultant in the display devices and touch panel fields. I am currently a Professor of Electrical and Microengineering at Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland and director of the micromanufacturing science and engineering research center. I moved to EPFL in 2018. I was previously a professor at the University of California, Berkeley for almost 20 years, and am still maintaining an adjunct professorship appointment there while I graduate my remaining PhD students. I also previously served as a founding technical advisor for Kovio, Inc. which developed thin film transistor technology for various applications, including RFID tags and displays.

5. I received a Ph.D. in electrical engineering from Stanford University in 1998. I received my MS in electrical engineering from Stanford in 1996, and my BS in electrical engineering from Louisiana State University, Baton Rouge, in 1994. My PhD thesis was specifically focused on the development of technology for displays. During my PhD, I was the recipient of an Eastman Kodak fellowship. As part of this award, I worked closely with Kodak on their OLED technology.

6. After completing my Ph.D., I held multiple jobs simultaneously. First, I was a founder and member of technical staff of Matrix Semiconductor (“Matrix”), which developed high density memory. We founded Matrix in 1997,

and I maintained a full-time role through 2000, at which point I transitioned to an advisory role. Matrix was acquired by Sandisk in 2005, at which point my affiliation with Matrix ended. Between 1998 and 2000, I was also a visiting research engineer at the University of California, Berkeley, where I performed research on high-performance transistors and process technology. In that same period, I was also a consulting assistant professor at Stanford University, where I performed research on 3D integration of transistors, among other topics. In 2000, I was offered a professorship at Berkeley, and moved there full time. I received tenure in 2005, and became a full professor in 2011. In 2018, I was awarded with a Chancellor's professorship. In 2018, I also accepted a position at EPFL, and between 2018 and 2020, I maintained dual appointments at Berkeley and EPFL while I completed my move.

7. My professional career has been focused heavily on semiconductor and display technology, and I have been actively involved in the development of process technology for displays and touch screens for a large part of my professional career, both in academia and in industry. I have specifically been involved in the development of thin film transistor technology for displays, development of materials and processes for OLEDs, and development of printing technology for display fabrication. I have also worked specifically on touch screen technology; as an example, I taught the main electrical engineering course at

Berkeley that dealt with touch screens, and introduced a touch screen lab into the curriculum. At EPFL, I have continued in this vein, and continue to teach the main course on large area and flexible electronics, which includes extensive teaching on displays.

8. I have authored or co-authored more than 200 publications in journals and major international conference proceedings, many of which are specifically related to displays, touch screens, and the associated thin film technologies.

9. My *curriculum vitae* contains further details regarding my experience, education, publications, and other qualifications that qualify me to render expert opinions in connection with this proceeding.

III. COMPENSATION

10. I am being compensated for my work in this matter at an hourly rate of \$700 for consulting services.

11. My compensation is not contingent upon the opinions I render or the outcome of this proceeding.

IV. MATERIALS CONSIDERED

12. In preparing this declaration, I reviewed and considered the following materials, along with any others referenced in the body of my declaration:

- The '836 Patent (Ex. 1001) and its file history (Ex. 1002).
- U.S. Patent Publication No. 2008/0303798 A1 (“**Nakamura**”) (Ex.

1004)

- U.S. Patent Publication No. 2008/0266273 A1 (“**Slobodin**”) (Ex. 1005)
- U.S. Patent No. 9,639,229, which is related to the ’836 Patent, and its file history (excerpted as Ex. 1006)
- Japanese Patent No. JP-A-2002-342014 (“**Takaya**”) (Ex. 1007)
- U.S. Patent Publication No. 2009/0096763 A1 (“**Hinata**”) (Ex. 1008)
- U.S. Patent Publication No. 2010/0013785 A1 (“**Murai**”) (Ex. 1009)

13. I may use these documents and information, or other information obtained during the course of this proceeding, as well as representative charts, graphs, schematics and diagrams, animations, and models based on those documents and information, to support and to explain my testimony.

14. My opinions are based in part on a review and analysis of the above-mentioned documents and materials. I have also drawn on my education, experience, and knowledge of basic engineering and scientific principles in forming my opinions.

V. UNDERSTANDING OF THE LAW

A. Legal Standards

15. I am not an attorney, but I have been informed of several legal principles, which I have employed in forming my opinions in this declaration. I have been informed and understand that each patent claim is considered separately for purposes of validity and that a dependent claim that depends from another

claim includes all of the limitations of the claim it depends from.

16. ***Claim Construction.*** I have been informed and understand that the claims of the challenged patents in this proceeding are to be construed using the same claim construction standard applied in district court. I have been informed and understand the claim construction analysis begins with the ordinary meaning of a claim term, and there is a presumption that the term carries its plain and ordinary meaning to persons of ordinary skill in the art as of the effective filing date of the patent. I have also been informed and understand that the most important sources for determining the meaning of a claim term are the claims, the specification, and the prosecution history of the patent at issue, which collectively is called “intrinsic evidence.” I have been further informed and understand that the meaning of a claim term may also be guided by “extrinsic evidence,” such as contemporaneous dictionaries and treatises.

17. ***Burden of Proof.*** I have been informed and understand that the petitioner in an *inter partes* review bears the burden of establishing invalidity by “a preponderance of the evidence.” I have been further informed and understand that, to prove an assertion by “a preponderance of the evidence,” the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

18. ***Obviousness.*** I have been informed and understand that a patent

claim is invalid if it would have been obvious to a person of ordinary skill in the art at the time of the claimed invention. I have been further informed and understand that a claimed invention is not patentable if differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. I have been informed and understand that factors relevant to the determination of obviousness include the scope and content of the prior art, the level of ordinary skill in the art at the time of the invention, differences between the claimed invention and the prior art, and “secondary considerations” or objective indicia of non-obviousness.

19. I have been informed that a single reference alone can render a patent claim obvious, if any differences between the reference and the claim would have been known or obvious to a person of ordinary skill in the art (“POSITA”) at the time of the invention. That is, if the POSITA could have adapted the reference to meet the claims of the patent by applying known concepts to achieve expected results, then the patent claims are rendered obvious by that reference.

20. I have been informed and understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have been further informed and understand that when a patent claim simply arranges old elements with each performing the same

function it had been known to perform and yields no more than one of ordinary skill would expect from such an arrangement, the combination is obvious.

21. I have been informed and understand that a patent claim composed of several limitations is not obvious merely because each limitation was independently known in the prior art. Hindsight reasoning is not an appropriate basis for combining references to form an obviousness combination. I have been further informed and understand that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references.

22. I have been informed that various “secondary considerations” (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations must be considered as part of an obviousness analysis. I have been informed that even strong evidence of secondary considerations may not be sufficient to rebut a strong showing of obviousness. I have been informed that the patentee bears the burden of showing the existence and effect of secondary considerations of non-obviousness, after which the burden of coming forward with rebuttal evidence shifts to the party arguing obviousness. I have been informed that the following secondary considerations may indicate non-obviousness:

- Copying: evidence that others, including the accused infringer,

copied the patented invention.

- Long-standing problem or need: evidence of a persistent problem or need in the art that was resolved by the patented invention.
- Prior failure: evidence that others have tried and failed to solve the problem or failed to provide the need resolved by the claimed invention.
- Commercial acquiescence of competitors: the willingness of industry to license the patent at issue.
- Skepticism: evidence that those of ordinary skill in the art were skeptical as to the merits of the invention.
- Praise: evidence of praise directed to an invention by others in the field.
- Unexpected results: evidence that those of ordinary skill in the art were surprised by the capabilities of the claimed invention.

23. I have also been informed that the near-simultaneous invention by others can be evidence that a claimed invention is obvious. I have further been informed and understand that the patentee bears the burden of showing a “nexus” between the claimed invention and the evidence proffered on secondary considerations (*e.g.*, proof of commercial success of a product that practices the claimed invention is not enough; there must be evidence that the commercial success resulted, at least in part, from the claimed invention).

B. Priority Date

24. I have been informed and understand that a U.S. patent may claim “priority” to the filing date of one or more earlier filed applications. I have been

informed that the priority date, also called the “effective filing date,” is the earliest filing date to which a claim is entitled and that such date is relevant for determining what qualifies as prior art. I understand that a claim must have written description support in the application(s) to which it claims priority to be entitled to an earlier effective filing date. I have been informed that the priority date determination is done on a claim-by-claim basis and that claims in the same patent may have different priority dates.

C. Level of Skill in the Art

25. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art may have for combining references.

26. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art is also a person of ordinary creativity.

27. The challenged patent pertains generally to the fields of displays and

touch panels. A person of ordinary skill in the art (“POSITA”) at the time of the alleged invention would have had at least a Bachelor’s degree in electrical engineering, or a similar discipline, along with 2-3 years of display and touch panel technology experience. Relevant experience can substitute for education and *vice versa*. I was at all relevant times at least a POSITA in the art relevant to the challenged patents.

VI. SUMMARY OF OPINIONS

28. I have been asked to compare various prior art references to Claims 1-15 of the ’836 Patent (the “Challenged Claims”). In my opinion, the Challenged Claims are all unpatentable as obvious – based on these prior art references, combined with the knowledge of a POSITA.

29. My substantive analysis in Section X provides examples of why these prior art references render the Challenged Claims unpatentable. I reserve the right to cite and rely on additional portions of these references in any future declarations or depositions.

VII. TECHNOLOGY BACKGROUND

30. Before considering the ’836 Patent in detail, some background on the technology of the ’836 Patent should be considered.

31. Display devices having touch panels were well established by September 2009, building on the decades-old understanding of basic detection

principles. The concept of using wired detection areas in one or more substrates to detect the coordinates where a user touches a touch screen was already well in place. The same is true of the display device and touch screen structures that were used to implement the concept.

32. For example, as I discuss in the following section, the '836 patent itself admits that detection methods ranging from light-based and electric characteristic-based concepts were all well known. Ex. 1001, 1:20-50, Figs. 20-21. This included extensive art relating to both resistive and capacitive sensing methods. *Id.* The '836 patent also repeatedly admits that the exact touch panel structure it claims had already been disclosed in Nakamura. *Id.*, 2:57-59, 4:57-60, 6:40-52.

33. Thus, it was a crowded art by 2009, where the concepts employed in the field were well understood, predictable, and routinely mixed and matched as needed to achieve a POSITA's design goals. The '836 patent itself admits that the particularities of such detection techniques—such as the exact structure its claimed display device and its touch panel—were all known and available for designers to choose from, as discussed throughout this Declaration. For example, I discuss the well-known practice of grouping detection wiring on touch panel substrates in Section X.A.1.g below. I further discuss the similarly well-known decision of whether to use a linear polarizing plate or a circular polarizing plate, in Section

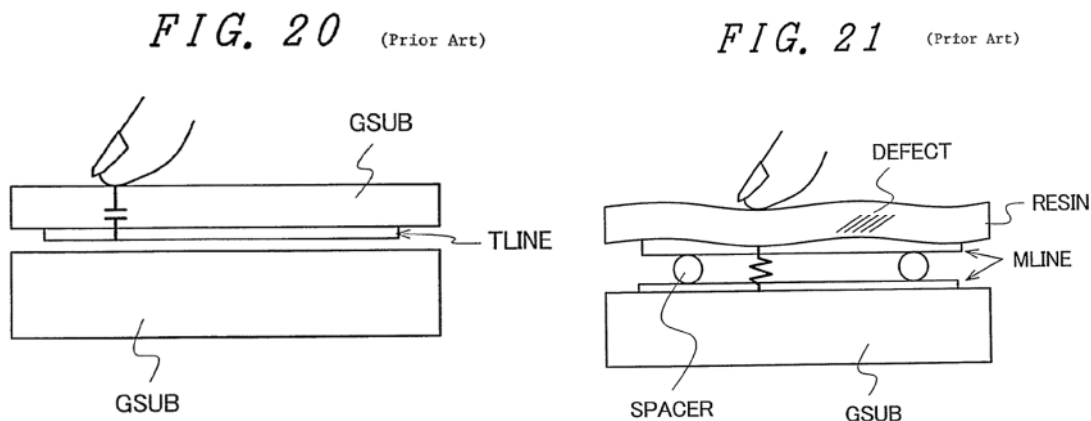
X.B below.

VIII. THE '836 PATENT

34. U.S. Patent No. 8,803,836 (“the ’836 Patent” or “the Challenged Patent”) is entitled “Display Device With Touch Panel.” The ’836 patent claims priority to U.S. application 12/649,414, which was filed on December 30, 2009, and foreign application JP 2009-004874, which was filed on January 13, 2009. For purposes of this declaration, because I have been informed that the ’836 Patent cannot rely on its foreign priority claim to overcome the prior art discussed in this Declaration, I have been instructed to use December 30, 2009 as the priority date of the ’836 Patent. My opinions in this declaration were formed from the perspective of a POSITA as of December 30, 2009, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art. However, I also note that, if a January 13, 2009 priority date was instead employed for the ’836 Patent, my opinions would not materially differ.

35. Display devices with touch panels were part of a crowded art by 2009. The art routinely utilized and adapted well understood and predictable detection methods in various structures. This understanding is reflected in the ’836 Patent itself, as it admits that a wide variety of detection methods had already been “adopted by a conventional display device with a touch panel,” including light-based and electric characteristic-based detection methods. Ex. 1001, 1:20-29. The

'836 Patent also admits that well-known prior art electric characteristic-based detection methods included both resistive detection, which works by detecting pressure applied to a touch panel, as well as capacitive sensing detection, which works by creating an electric field above the surface of the touch panel and detecting changes in the electric field caused by objects like a finger. *Id.*, 1:27-29. The '836 Patent provides example prior art capacitive and resistive sensing touch panel figures in its Figs. 20 and 21, respectively. *Id.*, 1:30-50, Figs. 20-21:

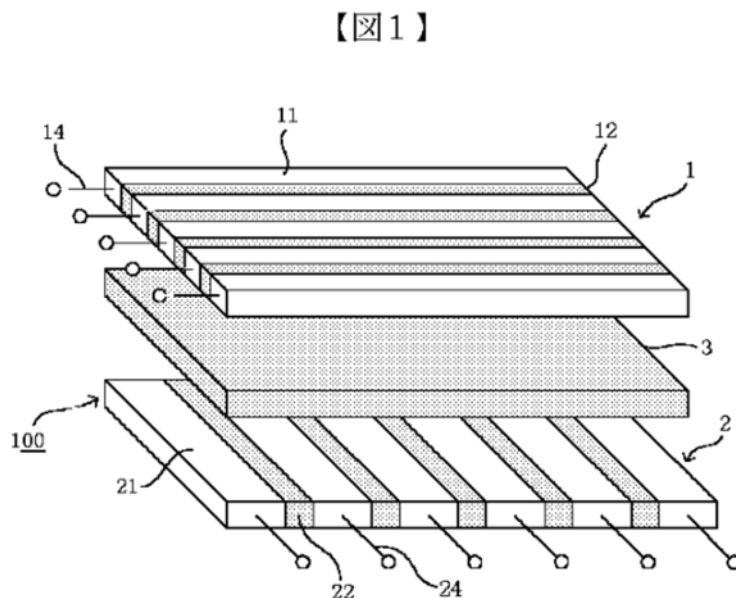


36. After its background discussion of resistive and capacitive sensing touch panels, the rest of the '836 Patent focuses entirely on resistive sensing touch panels.

A. Problem Addressed by the '836 Patent and the Alleged Invention

37. As I have just discussed, the '836 Patent admits that touch panels, including resistive sensing touch panels, were already well-known. Despite this, the patent criticizes Japanese Patent No. JP-A-2002-342014 to Takaya ("Takaya"),

which it says teaches a resistive sensing touch panel “in which a transparent electrode is formed into stripe-shaped electrodes and these stripe-shaped transparent electrodes are made [to] intersect with each other thus arranging intersecting portions in a matrix array.” Ex. 1001, 1:51-57. While the ’836 Patent does not provide precise citations or explain exactly what portion of Takaya’s configuration it criticizes, it appears to take issue with the way electrodes 14 and electrodes 24 intersect with each other as shown in, *e.g.*, Fig. 1. Ex. 1007 (Takaya), Fig. 1:



38. According to the ’836 Patent, this “stripe-shaped” approach is undesirable due to its alleged inability to increase detection accuracy, which it says occurs due to the tradeoff between the need to decrease electrode line width and the corresponding increase in resistance this is said to cause. Ex. 1001, 1:61-67.

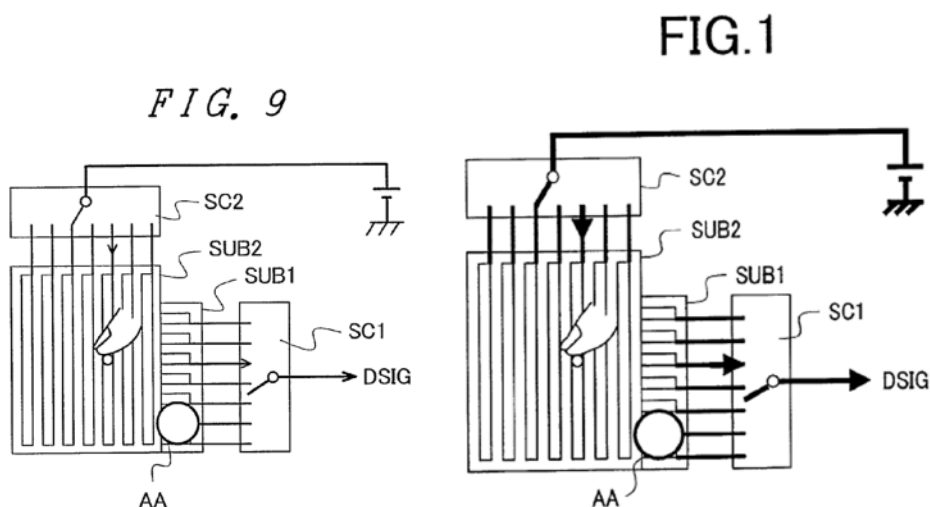
The '836 Patent also criticizes Takaya because it is allegedly “difficult to decrease a gap between the transparent electrodes,” and for having contact positions that “are detected one-dimensionally,” which means that detection is “performed twice along an X axis and a Y axis.” *Id.*, 1:67-2:56.

39. Interestingly, after discussing these alleged issues in Takaya, the '836 Patent does not even claim to present a new solution to them. Rather, the patent states that the “applicants of the present application” had already “proposed a touch panel which adopts [a] new detection structure (Japanese Patent Application 2007-149884)” that addresses these issues. *Id.*, 2:57-59. The '836 Patent notes that it expressly adopts the structure already disclosed presented in this prior application. *Id.*

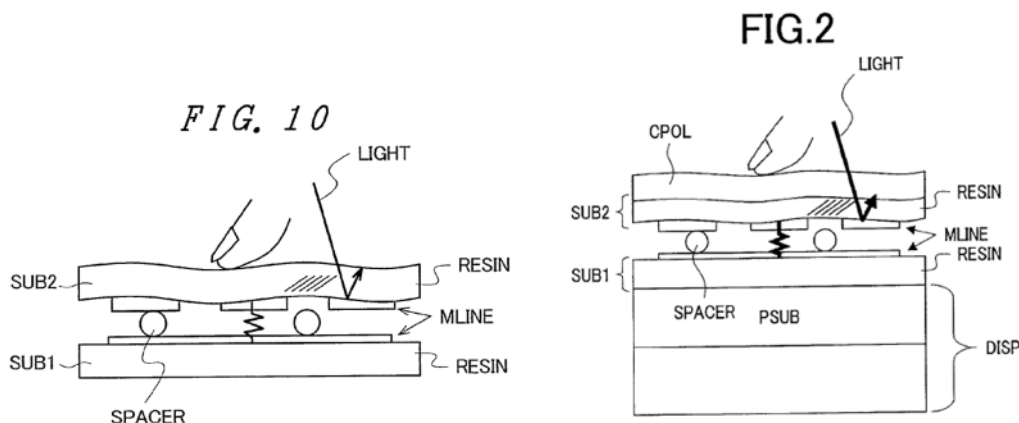
40. This Japanese application that the '836 Patent “adopts” is the foreign priority application for the Nakamura reference discussed throughout this Declaration. See Ex. 1004, [0001] (“The present application claims priority from Japanese application JP2007-149884 filed on Jun. 6, 2007, the content of which is hereby incorporated by reference into this application”), (30) (priority claim to same application).

41. The '836 Patent reiterates several times that the details of the touch panel it discloses and claims, touch panel 10, is the same as the touch panel already described in Japanese Patent Application 2007-149884, *i.e.*, Nakamura. Ex. 1001,

4:57-59. This is also seen in comparing the '836 Patent's figures with Nakamura's. For example, the preferred embodiment of the '836 Patent's touch panel is shown in its Fig. 9, which the '836 Patent expressly states is copied from Nakamura: "FIG. 9 is a schematic plan view of the touch panel of this mode which adopts the touch panel described in" Nakamura. Ex. 1001 ('836 patent), 6:45-52, Fig. 9 (below left); Ex. 1004 (Nakamura), Fig. 1 (same figure, below right):



42. As another example, the figure comparison below shows how Nakamura had also already disclosed essentially the same cross-sectional view of the '836 Patent Fig. 10 embodiment, in greater detail than what is presented in the '836 Patent figure. Ex. 1001 ('836 patent), Fig. 10 (below left); Ex. 1004 (Nakamura), Fig. 1 (same figure with additional detail, below right):

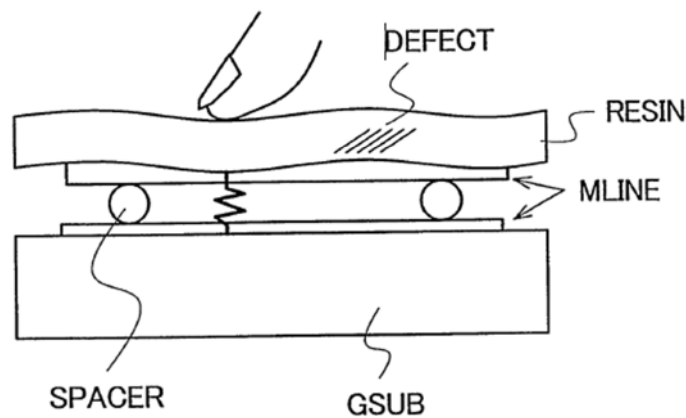


43. The '836 Patent thus admits that the exact “new detection structure” it presents to solve the alleged problems presented by Takaya had already been disclosed in Nakamura.

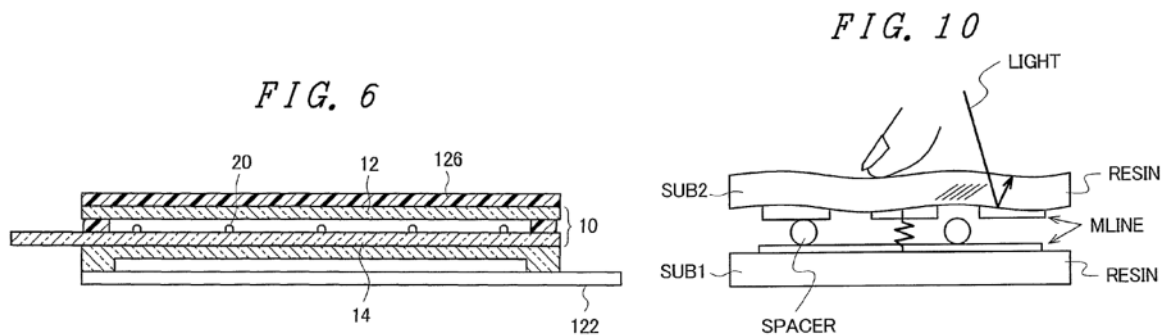
44. Without referencing any particular prior art, the '836 Patent states that “according to such a related art, since a plurality of lines are formed on a touch panel and hence, when a user moves a pen on an operation surface in a sliding manner, the user feels the surface unevenness.” Ex. 1001, 2:57-3:3. The '836 Patent complains that this “related art” prevents the user from experiencing an “excellent touch feeling.” *Id.* It then states that this “excellent touch feeling” is achieved by adding “a resin film which is adhered to the first substrate on a side opposite to the second substrate.” *Id.*, 3:14-16. It further states that, “[a]ccording to the present invention, the resin film is adhered to the touch panel, the unevenness attributed to the first electrode is absorbed and hence, the touch panel can give a user excellent touch feeling.” *Id.*, 3:16-19.

45. It appears that the '836 Patent is suggesting that in prior art systems, such as in the exemplary, "conventional" resistive sensing touch panel it shows in Fig. 21, the user would touch only a resin film, and so could feel the defects in the resin film. Ex. 1001, Fig. 21:

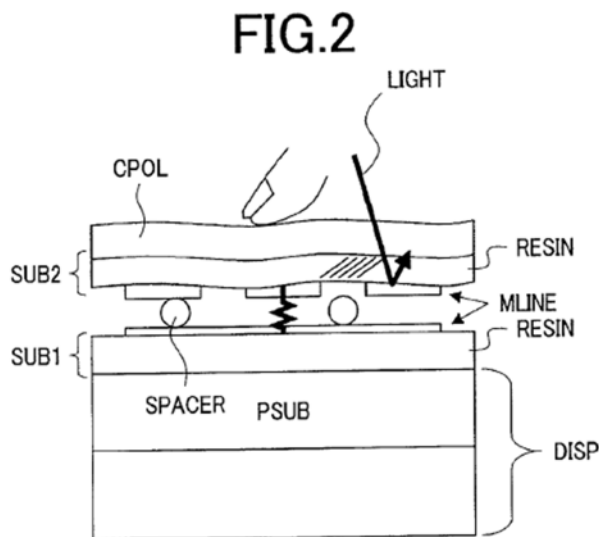
FIG. 21 (Prior Art)



46. Apparently, the '836 Patent addresses this issue in "conventional" resistive sensing touch panels by having a touch panel that combines a resin film and a substrate, as in the touch panels of Figs. 6 and 10. Ex. 1001, Figs. 6, 10:



47. However, this distinction over “conventional” touch panels is not a distinction over Nakamura, which the '836 Patent admits had already disclosed this very same arrangement in its Fig. 2. Ex. 1004, Fig. 2:



48. The '836 Patent moves Nakamura's circular polarizing plate CPOL from its Fig. 10 embodiment to circular polarizing plate 126 in its Fig. 6 embodiment, without explaining why, but maintaining exactly the same arrangement as Nakamura's Fig. 2 in a differently styled figure. Ex. 1001, 5:52-63. *Compare* Ex. 1004 (Nakamura) Fig. 2 (circular polarizing plate CPOL arranged over touch panel comprising substrates SUB1 and SUB2, itself arranged over display panel DISP) with Ex. 1001 ('836 patent) Fig. 6 (circular polarizing plate 126 arranged over touch panel 10 comprising substrates 12 and 14, itself arranged over display panel 122). The '836 Patent's unexplained transference of the

CPOL from one figure to another does not alter the fact that it still relies on the same touch panel structure already disclosed in Nakamura.

49. Thus, whatever advancement in “touch feeling” the ’836 Patent is referencing, that “advancement” had already been taught by Nakamura.

50. Indeed, the ’836 Patent attributes its “excellent touch feeling” to “a resin film which is adhered to the first substrate on a side opposite to the second substrate,” which is precisely the resin film already disclosed in Nakamura’s Fig. 2. Ex. 1001, 3:14-16. The ’836 Patent not only admits that such resin films were already disclosed in Nakamura, but even that they were already well-known in “conventional resistance-film-type panel[s].” Ex. 1001, 1:38-50, 6:45-52, Figs. 9, 21.

51. Further, looking beyond the ’836 Patent specification’s statement that this resin film is the only alleged advancement over an unidentified “related art,” none of the claims in the ’836 Patent recite such a concept. In fact, no claim even recites the word “resin” at all. Dependent claims 7 and 12-15 recite “a transparent conductive film” that overlays or underlays certain detection lines, but these claims do not relate to the allegedly novel resin film, but instead a “transparent electrode TLIN” that the ’836 Patent itself admits was well disclosed by both “conventional” touch panels and Nakamura. Ex. 1001, 1:30-57, 8:51-9:15, 9:47-10:17, Figs. 12-13, 16-19, 20-21; *see also* Ex. 1004, [0007]-[0008], [0081]-[0089],

[0098]-[0110], Figs. 4-5, 8-11, 13-14 (same disclosures in Nakamura).

52. The concepts the '836 Patent does claim, such as substrate detection areas, display panels, and polarizing plates, are all concepts that the '836 Patent's specification itself expressly admits were already disclosed by the touch panel structure of Nakamura.

53. In other words, because the '836 Patent itself admits that Nakamura had already taught the claimed touch panel structure, the claims are admittedly disclosed by Nakamura. This disclosure is confirmed throughout this Declaration.

B. Prosecution History of the '836 Patent

54. The '836 Patent was prosecuted in the United States as Application No. 13/966,857, and stems from foreign application JP 2009-004874 and U.S. application 12/649,414.

55. Despite the fact the '836 Patent admits that Nakamura had already disclosed the touch panel structure it claims, the patent owner did not disclose Nakamura to the examiner in an information disclosure statement ("IDS") during prosecution. *See generally* Ex. 1002.

56. During prosecution, the examiner rejected the pending claims over prior art including U.S. Patent Publication No. 2009/0096763 A1 ("Hinata"). *Id.*, 12/12/2013 Office Action, pp. 3-8.

57. The patent owner responded by amending pending Claim 1 to add

limitations relating to detection lines on the first and second substrates and arguing that Hinata did not disclose them. *Id.*, 3/11/2014 Amendment, pp. 2, 7-8.

58. The patent owner also newly added independent Claim 8, arguing that Hinata did not disclose “an organic luminescence electric device panel, wherein the organic luminescence electric device panel is adhered to the touch panel, and a circular polarizing plate is adhered to the touch panel at a side opposite to the organic luminescence organic electric device panel.” *Id.*, pp. 3-4, 8-9.

59. After these amendments, the examiner allowed the claims over Hinata. *Id.*, 4/16/2015 Notice of Allowance.

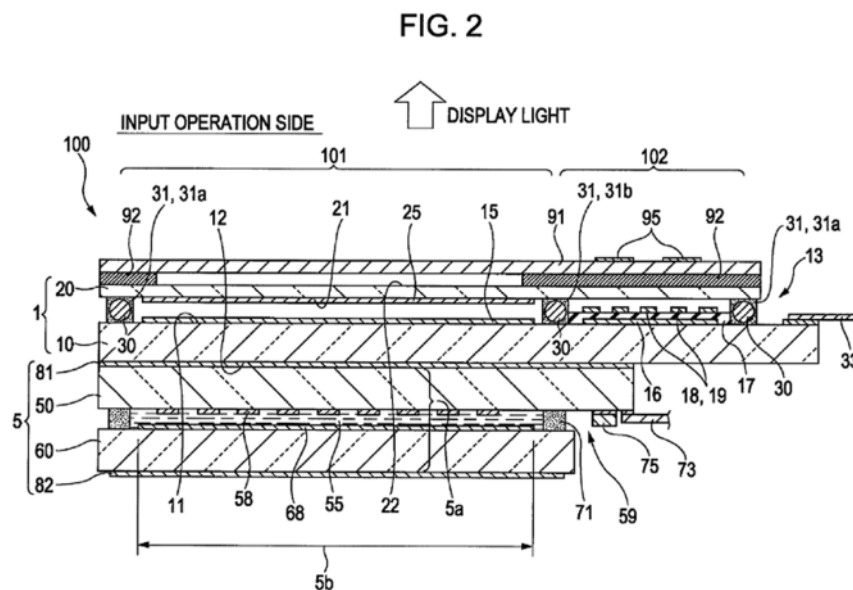
C. Claim Construction

60. In my opinion, the claims of the '836 Patent can be interpreted according to their ordinary meanings without construction for the purpose of this IPR.

61. While I do not believe that any claim construction is necessary here, I would like to make clear that, in my opinion, Claim 8 does **not** require a touch panel with first and second detection lines on “one and only one substrate.” For one thing, Claim 8 does not state that both sets of detection lines are adhered to the first substrate. Because Claim 8 is a “comprising” claim, it should cover touch panels that include additional substrates beyond the claimed first substrate.

62. The '836 Patent family's prosecution history further supports that this belief is correct. For example, as I discussed above, after the pending claims of the '836 Patent were rejected over Hinata, the patent owner added Claim 8 and argued against Hinata for other reasons. Ex. 1002 ('836 Patent File History), 12/12/2013 Office Action, pp. 3-8; 3/11/2014 Amendment, pp. 2-4, 7-9.

63. After Claim 8 was introduced in its issued form, the examiner maintained that Hinata disclosed Element [8-A], which recites only a single “first substrate,” but two separate sets of detection lines (“first lines” and “second lines”). *Id.*, 4/16/2015 Notice of Allowance, pp. 3-4. The examiner did so even though, like every embodiment in the '836 Patent's specification, Hinata's touch panel discloses two separate substrates, each of which has its own set of detection lines. *See* Ex. 1008 (Hinata) Fig. 2 (depicting first electrode 15 formed on first substrate 10 opposite second electrode 25 formed on second substrate 20):



See also, e.g., Ex. 1001, 6:45-7:14, Figs. 9-10 (two-substrate structure in '836 patent).

64. This demonstrates an understanding between the patent owner and the examiner that the plain and ordinary meaning of Claim 8 covers embodiments that contain two substrates, with the claimed “plurality of first lines” on a first substrate and the claimed “plurality of second lines” on a second substrate.

65. The prosecution the ’836 Patent’s child ’229 Patent further confirms this understanding. There, the examiner applied Hinata against a version of pending ’229 Patent Claim 1 that, at first, expressly recited two substrates. Ex. 1006 (’229 Patent File History), 3/14/2016 Office Action, pp. 4-8. The patent owner then amended ’229 Patent Claim 1 to, like ’836 patent Claim 8, recite only a single substrate. *Id.*, 6/14/2016 Amendment, pp. 2. After this amendment, the examiner continued to apply Hinata’s two-substrate embodiment. *Id.*, 8/2/2016 Office Action, pp. 3-7.

66. Prosecution history aside, it is important that ’836 patent Claim 8 is satisfied by two-substrate embodiments. This is because every embodiment in the ’836 Patent specification is, like Hinata, a two-substrate embodiment. *See, e.g.*, Ex. 1001, 6:45-7:14, Figs. 9-10 (two-substrate structure in ’836 patent).

IX. THE PRIOR ART REFERENCES

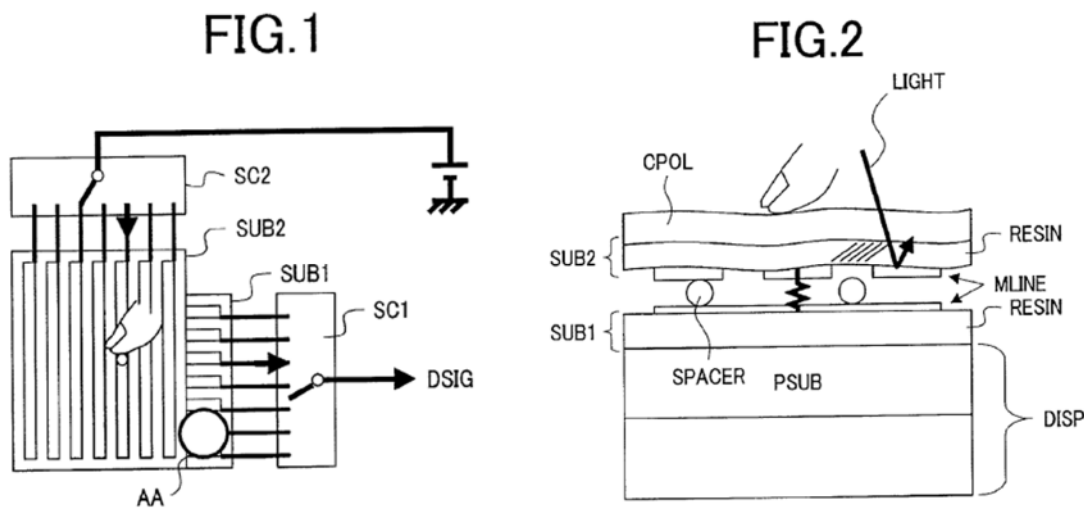
A. Nakamura

67. Nakamura is titled “Display Device With Touch Panel,” was published on December 11, 2008, filed on June 6, 2008, and claims priority to an

application filed on June 6, 2007. Ex. 1004, (54), (43), (22), (30).

68. Nakamura relates to display devices that include touch panels that have particular structures. Ex. 1004, Abstract. Importantly, as I have just discussed, the '836 Patent admits several times that the exact touch panel structure it claims had already been disclosed in Nakamura. Ex. 1001, 2:57-59, 4:57-60, 6:45-52.

69. Nakamura's Figs. 1 and 2 show schematic diagram and cross-sectional diagram views, respectively, of its preferred embodiment. Ex. 1004, Figs. 1-2:



See also Ex. 1001, Figs. 9-10 (substantially similar disclosure in '836 patent, with less detail in Fig. 10).

70. Nakamura's Figs. 1-2 show that its touch panel comprises two oppositely facing substrates, each arranged "so that their respective metal wirings

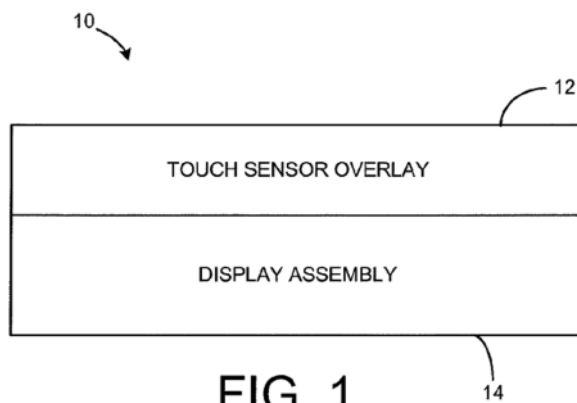
face each other and that directions along which the respective metal wirings extend are made to intersect,” a display panel, and a circularly polarizing plate CPOL. Ex. 1004, [0050]-[0055], Figs. 1-2; *see also* Ex. 1001, 6:45-7:14, Figs. 9-10 (substantially similar disclosure in '836 patent).

71. I discuss additional details regarding Nakamura's touch panels, which again are substantially similar to those of the '836 Patent, in the claim analysis section below.

B. Slobodin

72. Slobodin is titled “Interactive Display System,” was published on October 30, 2008, filed on April 24, 2008, and claims priority to an application filed on April 24, 2007. Ex. 1005, (54), (43), (22), (30).

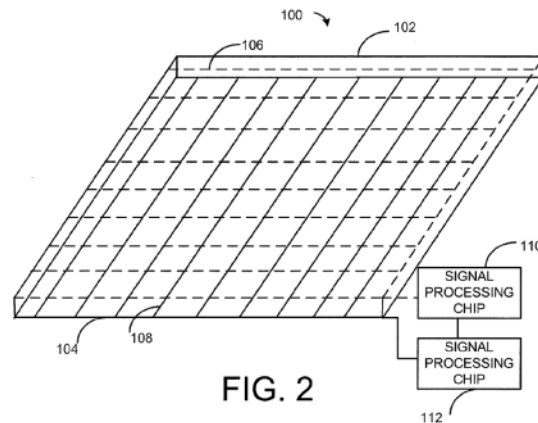
73. Slobodin relates to “[a]n interactive display system including a touch sensor overlay,” “a display assembly and an optical layer interposed the touch sensor overlay and the display assembly.” Ex. 1005, Abstract, Fig. 1:



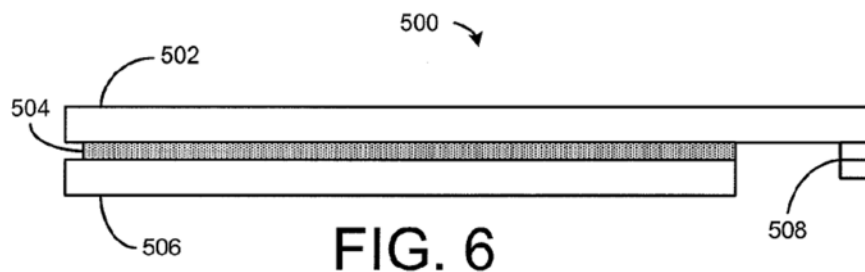
74. Slobodin explains that its interactive display system can be integrated

into a variety of different devices, including cellular phones and televisions, and that its display assembly can comprise many different types of displays, including LCDs and OLEDs. Ex. 1005, [0024]-[0025].

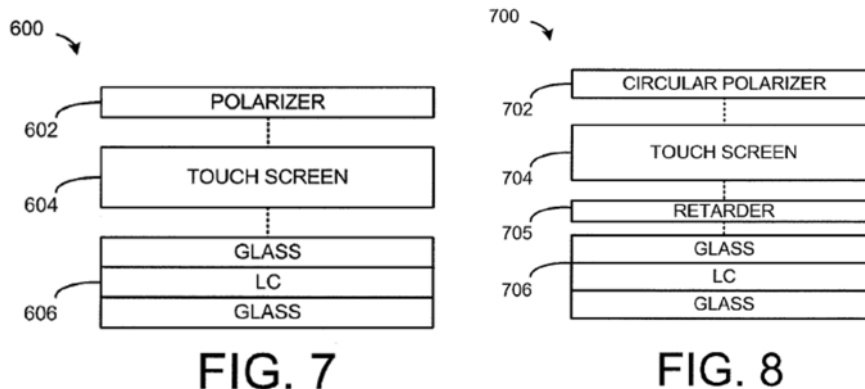
75. An embodiment of Slobodin's touch sensor overlay is shown in Fig. 2. As Fig. 2 shows, the touch sensor overlay includes opposing surfaces 102 and 104, each of which as detection electrodes arranged along an x-y coordinate axis. Ex. 1005, [0026]-[0031], Fig. 2:



76. Slobodin's touch panels may be adhered to an OLED display assembly, which forms an interactive display system. Ex. 1005, [0041], [0043], Fig. 6:



77. Slobodin includes a meaningful discussion of the pros and cons of using a linear polarizer versus a circular polarizer on the outer surface of the touch sensor (*i.e.*, located opposite the display panel) to reduce surface reflections. Ex. 1005, [0005], [0009]-[0010], [0050]-[0052], Figs. 7-8:



78. I examine this topic in detail in Section X.B.1 below

C. Motivation to Combine Nakamura and Slobodin

79. A POSITA would have found it obvious to combine Nakamura and Slobodin for many reasons.

80. For one thing, Nakamura and Slobodin are in the same field, display device touch panels. Beyond that, both Nakamura and Slobodin use polarizers on the outer surface of their touch panels to achieve the same thing, reducing surface reflections. *See, e.g.*, Ex. 1004 (Nakamura), Abstract, [0002]-[0009], [0029], [0055], [0061], Fig. 2; Ex. 1005 (Slobodin), Abstract, [0003]-[0010], Figs. 7-8.

81. Additionally, both Nakamura and Slobodin are implemented in standard display panels and both use standard electrical and optical principles.

See, e.g., Ex. 1004 (Nakamura), Abstract, [0002]-[0009], Figs. 13-14; Ex. 1005 (Slobodin), Abstract, [0003]-[0010]. Both Nakamura and Slobodin can be integrated into a variety of different devices, including cellular phones and televisions, and can comprise many different display types, including LCDs and OLEDs. Ex. 1004 (Nakamura), [0055], [0078], Fig. 12; Ex. 1005 (Slobodin), [0024]-[0025]. Further, both Nakamura and Slobodin disclose touch panels that detect touches using opposing surfaces, one surface having detection electrodes arranged along an x coordinate axis, and the other surface having detection electrodes arranged along an intersection y coordinate axis. *See, e.g.*, Ex. 1004 (Nakamura), [0003], [0051]-[0054], [0079], [0093], Figs. 1-2, 6; Ex. 1005 (Slobodin), [0026]-[0031], Fig. 2. In view of this, a POSITA could have predictably and successfully combined Nakamura and Slobodin without undue experimentation.

82. I provide additional details regarding why a POSITA would have been motivated to combine Nakamura and Slobodin to arrive at the relevant claim in Section X.B.1 below. For example, there I discuss how a POSITA would have been inspired to replace Nakamura's circular polarizer with Slobodin's linear polarizer in touch sensor applications involving birefringent materials, which is a situation where the optical performance improvements provided by circular polarizers are limited. By doing so, they would be able to take advantage of linear

polarizers' simpler and less expensive nature.

X. INVALIDITY ANALYSIS

83. As explained in detail in my analysis below, it is my conclusion and opinion that the Challenged Claims of the '836 Patent are invalid.

A. Ground 1 – Claims 1 and 3-15 Are Obvious Over Nakamura

84. In my opinion, Nakamura renders Claims 1 and 3-15 of the '836 Patent obvious.

1. Independent Claim 1

85. In my opinion, Nakamura discloses and renders obvious Claim 1 of the '836 Patent.

a) [1-PRE]

86. In the event the Claim 1 preamble is found to be limiting, Nakamura discloses and renders obvious “[a] display device with a touch panel.”

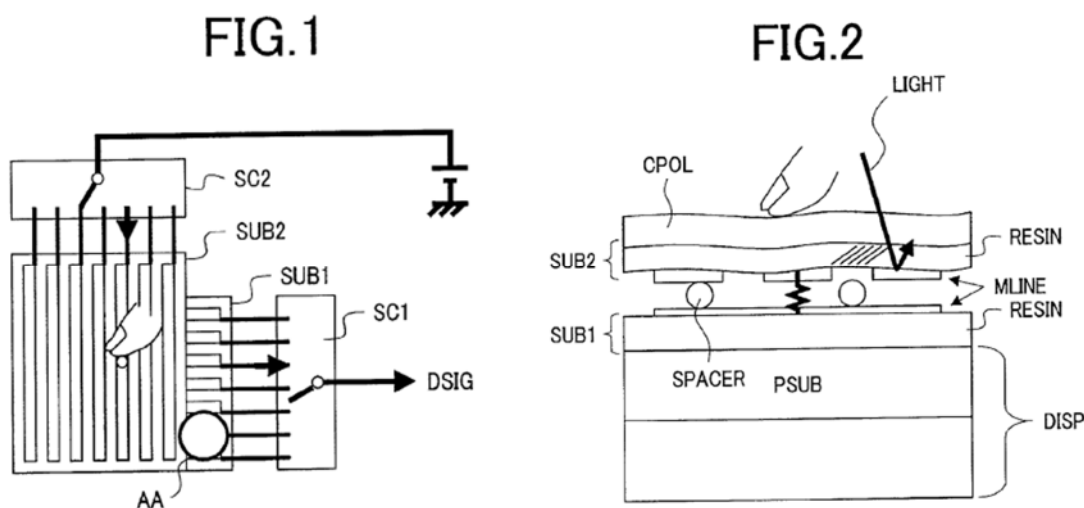
87. Nakamura repeatedly expressly discloses the exact verbiage of the preamble: a “display device with [a] touch panel.” *See, e.g.*, Ex. 1004, (54) (Title: “DISPLAY DEVICE WITH TOUCH PANEL”), Abstract, [0003], [0026], [0036], [0055].

b) Element [1-A]

88. Nakamura discloses and renders obvious this element of Claim 1: “the touch panel which includes a first substrate, and a second substrate arranged

to face the first substrate in an opposed manner.”

89. Nakamura’s Figs. 1-2 show how its touch panel includes “[t]he first substrate SUB1 and the second substrate SUB2,” and how these substrates “are arranged so that their respective metal wirings face each other and that directions along which the respective metal wirings extend are made to intersect.” Ex. 1004, [0052], Figs. 1-2:



90. I will refer to the substrate this Nakamura embodiment labels as the SUB2 as the “top” substrate, because it is located above the substrate labeled SUB1 for the rest of the Claim 1 group. For similar reasons, I will refer to SUB1 as the “bottom” substrate for the rest of this claim group.

91. Nakamura’s substrates are arranged so that each “face[s]” the other substrate “in an opposed manner.” *See, e.g.*, Ex. 1004, Abstract (“a touch panel including a pair of substrates provided with electrodes on opposing surfaces

thereof”), [0026] (same); *see also* [0030], [0058], [0082], [0086].

92. I note that the disclosure of this concept in the ’836 Patent is substantially similar to this disclosure in Nakamura, to the extent that the ’836 Patent expressly “adopts” Nakamura in discussing it. *See* Ex. 1001, 6:45-67, Figs. 9-10.

93. For at least these reasons, Nakamura discloses and renders obvious a touch panel that includes a first substrate, and a second substrate arranged to face the first substrate in an opposed manner.

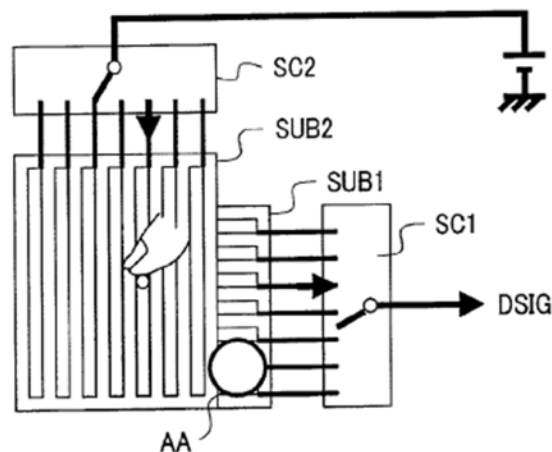
c) Element [1-B]

94. Nakamura discloses and renders obvious this element of Claim 1: “the first substrate and the second substrate each include a detection area configured to detect a coordinate and an outside area in which external terminals are formed.”

95. Nakamura’s Fig. 1 shows that the top substrate SUB2 and bottom substrate SUB1 in its touch panel both include a detection area that is configured to detect a coordinate, as well as an outside area in which external terminals are formed. Ex. 1004, [0051] (touch panel includes “a first peripheral circuit SC1, a second peripheral circuit SC2, a power supply, and a detection signal output terminal”), [0053] (“second peripheral circuit SC2 is connected to the second substrate SUB2, and selects the metal wiring line by line to input a voltage thereto

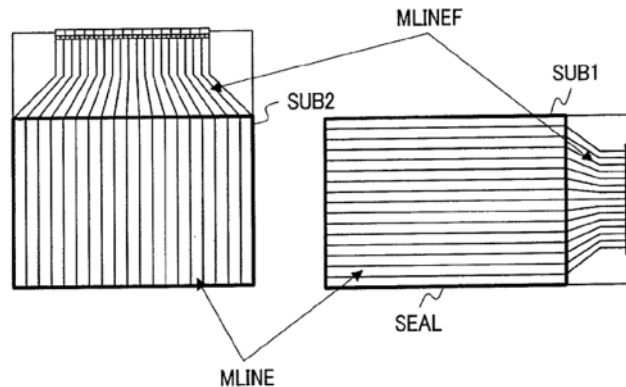
from the power supply”), [0054] (“first peripheral circuit SC1 is connected to the first substrate SUB1, and selects the metal wiring line by line to detect a voltage therefrom”), Fig. 1:

FIG. 1



96. Nakamura goes on to discuss the detection areas and outside areas of its substrates many more times. *See, e.g.*, Ex. 1004, [0079], [0083] (discussing the “detection area”), [0102] (same), [0105] (same), [0108] (same) [0095]-[0097] (discussing the “external terminals” and area “outside the detection area”), [0111], Fig. 7 (showing MLINE wiring in detection areas and MLINEF wiring in outside areas):

FIG. 7



97. I note that the disclosure of this concept in the '836 Patent is substantially similar to this disclosure in Nakamura, to the extent that the '836 Patent expressly “adopts” Nakamura in discussing it. See Ex. 1001, 6:45-52, 7:1-7, 9:28-46, Figs. 9, 15.

98. For at least these reasons, Nakamura discloses and renders obvious first substrates and second substrates that include both a detection area configured to detect a coordinate and an outside area in which external terminals are formed.

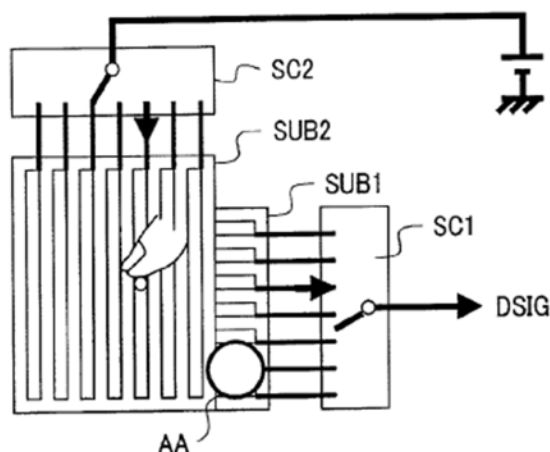
d) Element [1-C]

99. Nakamura discloses and renders obvious this element of Claim 1: “the first substrate includes a plurality of first lines each configured to detect a coordinate” and “the second substrate includes a plurality of second lines in the detection area which face the first substrate.”

100. Nakamura’s Fig. 1 shows that the top substrate SUB2 and the bottom

substrate SUB1 in its touch panel both include a plurality of lines that are configured to detect a coordinate, and also that the lines on each substrate “face” the other substrate. Ex. 1004, Fig. 1:

FIG. 1



101. Since the apparatus of Fig. 1 of Nakamura is a touch sensor, the lines are configured to detect a coordinate. Nakamura goes on to expressly state that “[t]he first substrate SUB1 and the second substrate SUB2 are flexible wiring substrates” that “are arranged so that their respective metal wirings face each other and that directions along which the respective metal wirings extend are made to intersect.” Ex. 1004, [0052]; *see also* [0051], [0053]-[0054], [0058], Figs. 2, 6-7.

102. I note that the disclosure of this concept in the '836 Patent is substantially similar to this disclosure in Nakamura, to the extent that the '836 Patent expressly “adopts” Nakamura in discussing it. *See* Ex. 1001, 6:45-7:7, Fig.

9.

103. For at least these reasons, Nakamura discloses and renders obvious a first substrate that includes a plurality of first lines each configured to detect a coordinate and a second substrate that includes a plurality of second lines in the detection area which face the first substrate.

e) Element [1-D]

104. Nakamura discloses and renders obvious this element of Claim 1: “each of the plurality of first lines and the plurality of second lines are configured of metal” and “each of the plurality of first lines is black in color.”

105. Nakamura expressly states that the first lines and second lines on its substrates are “configured of metal.” Ex. 1004, [0052] (“The first substrate SUB1 and the second substrate SUB2 are arranged so that their respective metal wirings face each other and that directions along which the respective metal wirings extend are made to intersect”), [0053] (“The second peripheral circuit SC2 is connected to the second substrate SUB2, and selects the metal wiring line by line to input a voltage thereto from the power supply”), [0054] (“The first peripheral circuit SC1 is connected to the first substrate SUB1, and selects the metal wiring line by line to detect a voltage therefrom”), [0066] (“Possible materials of the metal wiring include an opaque metal film made of aluminum (Al), carbon (C), nonferrous metal such as copper (Cu), stainless steel (SUS), or iron (Fe)”); *see also* [0028],

[0032], [0050]-[0053], [0055]-[0065], [0067]-[0069], [0071]-[0111].

106. Nakamura also goes on to explain that any of its lines, including the first lines, may be “black in color.” Ex. 1004, [0078] (“By changing the color of the above-mentioned metal wiring into black, it is possible to raise a contrast of a display such as a liquid crystal equipped with a touch panel”).

107. I note that the disclosure of this concept in the ’836 Patent is substantially similar to this disclosure in Nakamura, to the extent that the ’836 Patent expressly “adopts” Nakamura in discussing it. *See* Ex. 1001, 6:45-67, 7:45-48, 8:34-37.

108. As confirmation of this, during the prosecution of the ’836 Patent’s child ’229 Patent, the examiner expressly applied Nakamura against similar claim language. Ex. 1006 (’229 File History), 8/2/2016 Office Action, p. 9. The patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

109. For at least these reasons, Nakamura discloses and renders obvious that each of the plurality of first lines and the plurality of second lines are configured of metal and that each of the plurality of first lines is black in color.

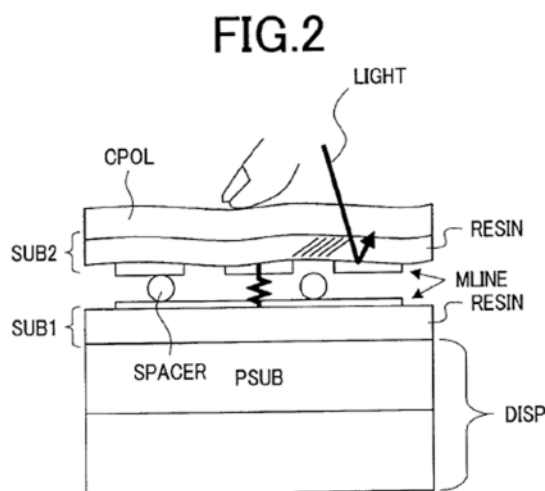
f) Element [1-E]

110. Nakamura discloses and renders obvious this element of Claim 1: “a polarizing plate is arranged on the first substrate at a side opposite to the second

substrate.”

111. Nakamura explains that “one of substrates may be provided with a polarizing plate on an outside thereof,” which can suppress ambient light reflection.” Ex. 1004, [0029]; *see also* [0061]. In other words, Nakamura is explaining that a polarizing plate can be arranged on either of its substrates, which of course includes an arrangement on the first substrate at a side opposite the second substrate.

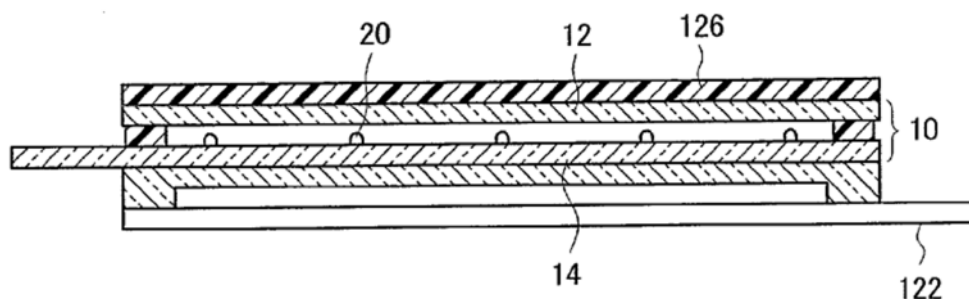
112. An embodiment of just such a polarizing plate is shown in Nakamura’s Fig. 2, with the polarizing plate taking the form of a circular polarizing plate. Specifically, Nakamura’s display device includes a “circularly polarizing plate CPOL” that “is fixed onto” the top substrate SUB2. Ex. 1004, [0055], Fig. 2:



113. I note that the disclosure of this concept in the '836 Patent is

substantially similar to this disclosure in Nakamura, to the extent that the '836 Patent expressly “adopts” Nakamura in discussing it. See Ex. 1001, 4:37-60, 5:52-63, Fig. 6 (depicting circular polarizing plate 126 fixed onto substrate 12, at a side opposite substrate 14).

FIG. 6



114. I note that Nakamura’s circularly polarizing plate is fixed onto the top substrate SUB2, which is labeled the “second substrate” in Nakamura’s Fig. 2 embodiment. Regardless, Nakamura’s top substrate SUB2 can be, and is, the “first substrate” recited in '836 Patent Claim 1. The “second” label in Nakamura’s Fig. 2 and “first” language in Claim 1 are merely numerical identifiers. Nothing about Claim 1 requires that the substrate the polarizing plate is “arranged on” be literally labeled the “first” substrate verbatim.

115. As confirmation of this, during the prosecution of the '836 Patent’s child '229 Patent, the examiner repeatedly stated that the “first and second labels” that carried over into its pending claims “are very arbitrary.” Ex. 1006 ('229 File

History), 3/14/2016 Office Action, pp. 7-8; 8/2/2016 Office Action, pp. 8-9. The patent owner did not dispute these statements.

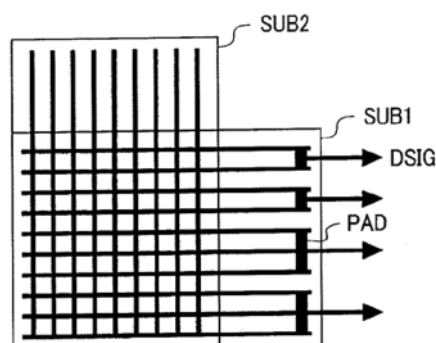
116. For at least these reasons, Nakamura discloses and renders obvious a polarizing plate that is arranged on the first substrate at a side opposite to the second substrate, both generally as well as in the form of a circular polarizing plate.

g) Element [1-F]

117. Nakamura discloses and renders obvious this element of Claim 1: “the first substrate includes a plurality of wiring groups,” “each of the plurality of wiring groups include at least two first lines of the plurality of first lines,” and “the at least two first lines of each of the plurality of wiring groups are combined with each other.”

118. Nakamura’s Fig. 6 shows that the metal wiring on its substrates, which are called MLINEs, can be combined with each other to form wiring groups. Ex. 1004, [0091] (“a terminal PAD for combining a plurality of metal wirings MLINE is provided in order to detect voltages of the plurality of metal wirings MLINE simultaneously, and a detection signal is output from each terminal PAD”), [0092] (“If the coordinate detection high in definition is unnecessary, the plurality of metal wirings MLINE are combined, to thereby enhance a recognition rate”), Fig. 6:

FIG.6



119. As Nakamura explains, “[t]his [Fig. 6 wiring] mode can be applied to the stripe-shaped metal wirings according to Wiring Layout Modes 1 and 2.” Ex. 1004, [0093]. Wiring Layout Mode 1 is the preferred embodiment shown in Figs. 1-3. *Id.*, [0050]-[0080].

120. I note that Fig. 6 only depicts the metal wiring on the bottom substrate SUB1 combined into a group. However, a POSITA would have considered it obvious to apply Nakamura’s wiring grouping teachings to the “top” substrate SUB2 (*i.e.*, the “first substrate” of Claim 1) for at least two independent reasons.

121. One reason relates to Nakamura’s explanation that, in its Fig. 2 embodiment, the top substrate SUB2 connects to a circuit that “selects the metal wiring line by line to input a voltage thereto from the power supply,” while the bottom substrate SUB1 connects to a circuit that “selects the metal wiring line by line to detect a voltage therefrom.” Ex. 1004, [0053]-[0054]. Significantly,

Nakamura does not say there is any special reason why the bottom substrate needs to be the detection substrate. Nor does the '836 Patent. This is consistent with a POSITA's understanding that there is no reason why the positions of Nakamura's two Fig. 2 substrates could not simply be reversed, and that it in fact would have been obvious to do so. This is particularly the case because both of Nakamura's substrates use the same metal wirings, and the wirings in both of its substrates are used for the same purpose, detecting the x-y coordinates of a touch. *See, e.g.*, Ex. 1004, [0051], [0056]-[0057], [0079], Fig. 7. While in the embodiment of Fig. 6, the detection voltage is applied to the wiring of the top substrate SUB2 and the detection signal is read on the wiring on the bottom substrate SUB1, it would have been obvious to a POSITA that this could have been reversed. *Id.* With Nakamura's substrates reversed, the detection substrate would simply be the top substrate, and all of Nakamura's wiring grouping teachings for Fig. 6 then directly apply to it, disclosing this limitation. *Id.*

122. A second reason is that, even if the top substrate in Nakamura's Fig. 2 embodiment remains the input substrate rather than the detection substrate, a POSITA still would have considered it obvious to apply Nakamura's wiring grouping teachings for Fig. 6 to the top substrate. It was well-understood that grouping the wiring on any substrate will reduce the resolution of the touch detection that substrate is responsible for. Nakamura's Fig. 6, and so the '836

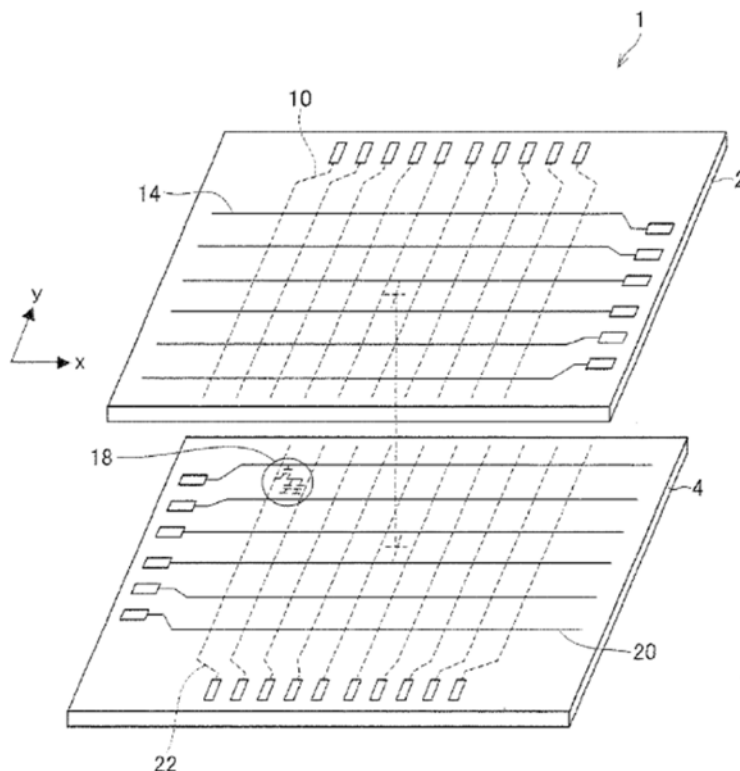
Patent's identical Fig. 14, accepts that very reduction by grouping the wiring on the "bottom" substrate, which reduces the touch resolution in the y-axis direction.

This means that the locations of touches in that direction are detected at are less precise than they would have been if the wires were not grouped. The '836 Patent does not discuss or acknowledge this loss whatsoever, but this necessary consequence of Fig. 14 shows it is willing to accept it. And the '836 Patent's failure to acknowledge this loss does not put any limitation on how much loss would or would not be acceptable.

123. Because Nakamura (and the '836 Patent) do not explain that any particular touch resolution is required, and expressly limit touch resolution for the "bottom" substrate in the Fig. 6 embodiment without qualification or discussion of its downsides, there is no reason why the wiring of the top substrate cannot be similarly grouped. A POSITA would have recognized that grouping in this manner reduces the complexity of wiring provided to the display, since less external wiring is now needed. Additionally, by having less externally-addressed lines, the overall scanning speed can be increased, as schematically illustrated by the rotary switches SC1 and SC2 in Fig. 1. In other words, resolution can be traded off for reduced wiring complexity and faster scanning. In fact, Nakamura expressly discusses how it would be appropriate to make these adjustments in view of this very same tradeoff. Ex., 1004, [0092] ("If the coordinate detection high in definition is

unnecessary, the plurality of metal wirings MLINE are combined, to thereby enhance a recognition rate”). Thus, a POSITA would have considered it obvious to apply Nakamura’s wiring grouping teachings for Fig. 6 to the top substrate in applications where high resolution is not required.

124. Prior art references that discuss this concept, which the ’836 Patent does not even acknowledge, confirm this. For example, U.S. Patent Publication No. 2010/0013785 A1 to Murai (“Murai”) (Ex. 1009) relates to a touch panel for a display that includes two sets of intersecting metal wires formed on a substrate for use in X-Y coordinate touch detection. Ex. 1009, [0146]-[0150]. Metal wires 14 are arranged in the X direction and metal wires 10 are arranged in the Y direction. *Id.*, [0146]-[0150], Fig. 2:



125. Murai Fig. 2 shows one possible arrangement, where each wire is connected to a different terminal. Ex. 1009, Fig. 2. However, Murai explains that this is only one disclosed arrangement. One metal wire “does not necessarily correspond to one terminal,” and “[a]lternatively, several metal wires [] can be connected to one terminal.” *Id.*, [0150]. Murai teaches that the decision of whether to group these wires or not depends on the same consideration that I have just discussed, the desired resolution. When less wires are connected to a given terminal, “the higher the detected resolution of a contact position” becomes. *Id.* “Therefore, a relation of connection of the metal wires 10 and the metal wires 14 to terminals can be freely set within an acceptable range of desired resolution of

coordinate detection.” *Id.*

126. The examination of this tradeoff in Murai confirms a POSITA’s understanding that the decision of whether or not to group detection wiring on a particular touch panel substrate is an obvious one. It also confirms that the decision depends on the resolution needed for a particular application.

Accordingly, a POSITA would have readily applied this concept to either of Nakamura’s two substrates in applications where a high resolution is not required.

127. As confirmation of the flexibility of Nakamura’s wiring grouping teachings, during the prosecution of the ’836 Patent’s child ’229 Patent, the examiner repeatedly stated that the “first and second labels” that carried over into its pending claims “are very arbitrary.” Ex. 1006 (’229 File History), 3/14/2016 Office Action, pp. 7-8; 8/2/2016 Office Action, pp. 8-9. *Id.* The examiner expressly applied these statements to claim language involving the “pluralit[ies] of wiring groups.” *Id.* The patent owner did not dispute these statements.

128. I note that the disclosure of this concept in the ’836 Patent is substantially similar to this disclosure in Nakamura. *See* Ex. 1001, 9:17-26, Fig. 14.

129. As confirmation of this, during the prosecution of the ’836 Patent’s child ’229 Patent, the examiner expressly applied Nakamura against similar claim language. Ex. 1006 (’229 File History), 8/2/2016 Office Action, p. 8. The

examiner also stated that “figures 16-21 suggest[] different wiring patterns are in groups and banded by being printed on the different films.” *Id.* Patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

130. For at least these reasons, Nakamura discloses and renders obvious a first substrate that includes a plurality of wiring groups, each of which includes at least two first lines of the plurality of first lines, and that the at least two first lines of each of the plurality of wiring groups are combined with each other.

2. Dependent Claim 3

131. Claim 3 of the '836 Patent depends from Claim 1. Claim 1 is disclosed and rendered obvious by Nakamura, for at least the reasons discussed above.

132. Claim 3 further recites: “the polarizing plate comprises a circular polarizing plate.” Nakamura discloses and renders obvious this additional limitation.

133. As I discussed for Claim 1 in Section X.A.1.f above, Nakamura expressly states that the polarizing plate CPOL in its Fig. 2 embodiment is a “circularly polarizing plate.” Ex. 1004, [0055].

3. Dependent Claims 4 and 5

134. Claims 4 and 5 of the '835 Patent depend from Claim 1. Claim 1 is

disclosed and rendered obvious by Nakamura, for at least the reasons discussed above.

135. Claim 4 further recites: “the second lines comprise a second electrode each configured to detect a coordinate.”

136. Claim 5 further recites: “a transparent electrode connects to the second lines.”

137. Nakamura discloses and renders obvious both of these additional limitations. This is the case in several embodiments.

138. I note that the disclosure of this concept in the '836 Patent is the same as in Nakamura. *See* Ex. 1001, 9:47-10:3, Figs. 16-18.

139. A first embodiment is shown in Fig. 8, about which Nakamura discloses “that a stripe-shaped transparent wiring TLINE having the same pattern as that of the metal wiring MLINE is located under the metal wiring MLINE.” Ex. 1004, [0099], Fig. 8:

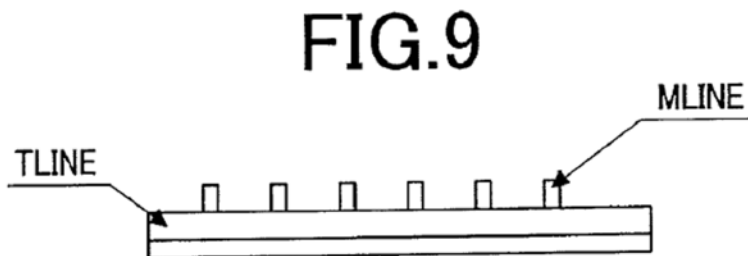


140. Nakamura explains throughout its disclosure both that transparent wiring TLINE is a transparent electrode that is configured to detect coordinates,

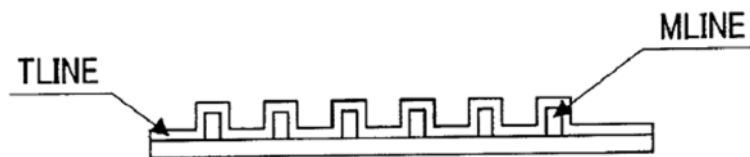
and also that the metal wiring MLINEs (which are also electrodes used to detect coordinates), comprise the first and second lines on both the first and second substrates. *See, e.g.*, Ex. 1004, [0007]-[0008], [0056]-[0057], [0079], [0091]-[0092], [0095], [0099], [0102], [0105], [0108], [0111]. And as applied to and shown in Fig. 8, a collection of TLINEs connects to the plurality of MLINEs.

141. In other words, Nakamura discloses both second lines comprising electrodes configured to detect a coordinate (*i.e.*, the MLINEs) and also transparent electrodes that connect to the second lines (*i.e.*, the TLINE).

142. A second embodiment is shown in Fig. 9, about which Nakamura discloses “that a transparent wiring (electrode) TLINE that covers the entirety of the detection area is located under the metal wiring MLINE.” Ex. 1004, [0102], Fig. 9:



143. A third embodiment is shown in Fig. 10, about which Nakamura discloses “that a transparent wiring (electrode) TLINE that covers the entirety of the detection area is located above the metal wiring MLINE.” Ex. 1004, [0105], Fig. 10:

FIG.10

144. As Nakamura explains, the wirings shown in all of Figs. 8-10 “can be applied to the stripe-shaped metal wirings according to Wiring Layout Modes 1 to 5.” Ex. 1004, [0100], [0103], [0106]. Wiring Layout Mode 1 is the preferred embodiment shown in Figs. 1-3. *Id.*, [0050]-[0080].

145. Nakamura’s teachings regarding Figs. 8-10 apply to both the lines on the “top” substrate (*i.e.*, the “first substrate” of ’836 patent Claim 1) and also the lines on the “bottom” substrate (*i.e.*, the “second substrate” of ’836 patent Claim 1), for several reasons. At the threshold, Nakamura’s discussions of Figs. 8-10 do not limit which substrate or lines their teachings apply to. Additionally, as I have previously discussed, the disclosure of this concept in the ’836 Patent is the same as in Nakamura. Moreover, the metal lines MLINE on both of Nakamura’s substrates are used for coordinate detection, such that both could benefit from transparent conductive film overlays and/or underlays. Ex. 1004, [0079]. As discussed above in Section X.A.1.g, it would have been obvious to a POSITA that either of Nakamura’s substrates could serve as the “top” or “bottom” substrate. As such, the transparent conductive film could be applied to either the top or bottom

substrate. Under these circumstances, at a minimum, a POSITA would have found it obvious to apply Nakamura's Fig. 8-10 concepts to the lines on its "bottom" substrate in addition to those on its "top" substrate.

146. For at least these reasons, Nakamura discloses and renders obvious that the second lines comprise a second electrode each configured to detect a coordinate, and that a transparent electrode connects to the second lines.

4. Dependent Claim 6

147. Claim 6 of the '836 Patent depends from Claim 1. Claim 1 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

148. Claim 6 further recites: "the at least two first lines of each of the plurality of wiring groups are combined with each other by a pad member."

Nakamura discloses and renders obvious this additional limitation.

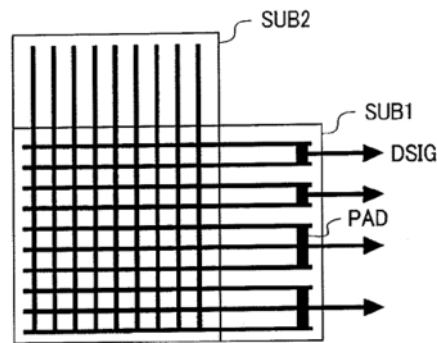
149. I note that the disclosure of this concept in the '836 Patent is the same as in Nakamura. *See* Ex. 1001, 9:17-26, Fig. 14.

150. As I discussed for Claim 1 above, Nakamura teaches—in a disclosure identical to that of the '836 Patent—that the metal wirings on its bottom substrate can be combined with each other to form wiring groups, as shown in Fig. 6. *See* Section X.A.1.g; Ex. 1004, [0050]-[0080], [0091]-[0093], Figs. 1-2, 6-7. There, I also explained multiple reasons why a POSITA would have considered it obvious

to apply this teaching to the top substrate. *Id.*

151. Nakamura's Fig. 6 also shows that lines of these wiring groups can be combined with each other by a pad member. Ex. 1004, [0091] ("a terminal PAD for combining a plurality of metal wirings MLINE is provided in order to detect voltages of the plurality of metal wirings MLINE simultaneously, and a detection signal is output from each terminal PAD"), Fig. 6:

FIG.6



152. Because this pad member is applied to the wiring groups, a POSITA would have considered it obvious to apply it to grouped wiring on the top substrate for the same reasons I discussed for Claim 1 in Section X.A.1.g above.

153. For at least these reasons, Nakamura discloses and renders obvious that the at least two first lines of each of the plurality of wiring groups are combined with each other by a pad member.

5. Dependent Claim 7

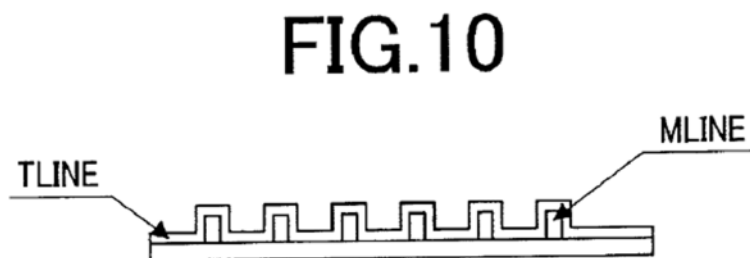
154. Claim 7 of the '836 Patent depends from Claim 1. Claim 1 is

disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above for Claim 1.

155. Claim 7 further recites: “a transparent conductive film overlaps the plurality of the second lines in plan view” and “the transparent conductive film is electrically connected to the plurality of the second lines.” Nakamura discloses and renders obvious this additional limitation.

156. I note that the disclosure of this concept in the '836 Patent is the same as in Nakamura. See Ex. 1001, 9:63:10-3, Fig. 18.

157. Nakamura's Fig. 10 shows “that a transparent wiring (electrode) TLINE that covers the entirety of the detection area is located above the metal wiring MLINE.” Ex. 1004, [0105], Fig. 10:



158. Nakamura explains throughout its disclosure that the transparent wiring TLINE is a transparent conductive film that is electrically connected to the metal lines. See, e.g., Ex. 1004, [0007]-[0008], [0102], [0105]. And as shown in Fig. 10, TLINE overlaps the MLINES.

159. As Nakamura explains, “[t]his [Fig. 10 wiring] mode can be applied

to the stripe-shaped metal wirings according to Wiring Layout Modes 1 to 5.” Ex. 1004, [0106]. Wiring Layout Mode 1 is the preferred embodiment shown in Figs. 1-3. *Id.*, [0050]-[0080].

160. As confirmation of this, during the prosecution of the '836 Patent's child '229 Patent, the examiner expressly applied Nakamura against similar claim language. Ex. 1006 ('229 File History), 8/2/2016 Office Action, p. 10. The patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

161. Nakamura's teachings regarding Fig. 10 apply to both the lines on the “top” substrate (*i.e.*, the “first substrate” of '836 patent Claim 1) and also the lines on the “bottom” substrate (*i.e.*, the “second substrate” of '836 patent Claim 1), for several reasons. At the threshold, Nakamura's discussion of Fig. 10 does not limit which substrate or lines its teaching apply to. Additionally, as I have previously discussed, the disclosure of this concept in the '836 Patent is the same as in Nakamura. And as I have also discussed, Nakamura was applied against similar claim language during related prosecution. Moreover, the metal lines MLINE on both of Nakamura's substrates are used for coordinate detection, such that both could benefit from transparent conductive film overlays and/or underlays. Ex. 1004, [0079]. As discussed above in Section X.A.1.g, it would have been obvious to a POSITA that either of Nakamura's substrates could serve as the “top” or

“bottom” substrate. As such, the transparent conductive film could be applied to either the top or bottom substrate. Under these circumstances, at a minimum, a POSITA would have found it obvious to apply Nakamura’s Fig. 10 concept to the lines on its “bottom” substrate in addition to those on its “top” substrate.

162. For at least these reasons, Nakamura discloses and renders obvious that a transparent conductive film overlaps the plurality of the second lines in plan view and the transparent conductive film is electrically connected to the plurality of the second lines.

6. Independent Claim 8

163. In my opinion, Nakamura discloses and renders obvious Claim 8 of the ’836 Patent.

a) [8-PRE]

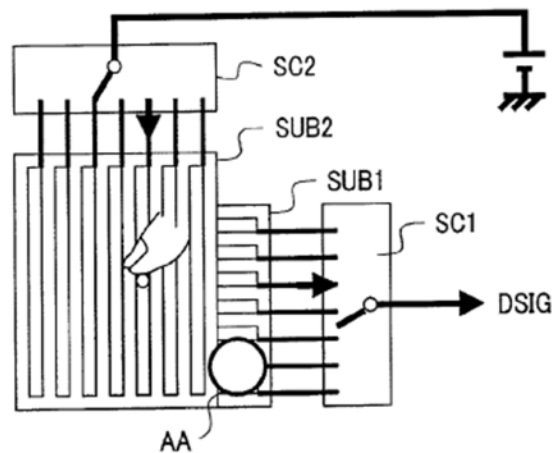
164. The preamble of Claim 8 is the same as the preamble of Claim 1. Thus, to the extent it is found to be limiting, Nakamura discloses and renders obvious the preamble of Claim 8 for the same reasons discussed above for the preamble of Claim 1. *See* Section X.A.1.a.

b) Element [8-A]

165. Nakamura discloses and renders obvious this element of Claim 8: “the touch panel including a first substrate having a detection area to detect a coordinate and an outside area in which external terminals are formed, a plurality

of first lines to detect the coordinate in the detection area, a plurality of second lines to detect the coordinate in the detection area, each of the plurality of first lines traversing each of the plurality of second lines.”

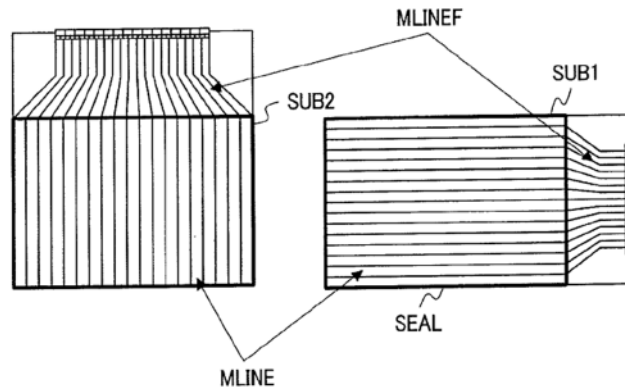
166. Nakamura's Fig. 1 shows that its touch panel includes first substrate SUB1 and second substrate SUB2, and that both substrates include a detection area configured to detect a coordinate, as well as an outside area in which external terminals are formed. Ex. 1004, [0051] (touch panel includes "a first peripheral circuit SC1, a second peripheral circuit SC2, a power supply, and a detection signal output terminal"), [0052], [0053] ("second peripheral circuit SC2 is connected to the second substrate SUB2, and selects the metal wiring line by line to input a voltage thereto from the power supply"), [0054] ("first peripheral circuit SC1 is connected to the first substrate SUB1, and selects the metal wiring line by line to detect a voltage therefrom"), Fig. 1:

FIG. 1

167. I note that either of Nakamura's substrates SUB1 and SUB2 can be the "first substrate" claimed in Claim 8, which is the only substrate expressly recited in the claim. To prevent confusion, I will refer to the bottom substrate SUB1 as the exemplary claimed "first substrate" for the remainder of this claim. However, I expressly note that, in the alternative, the top substrate SUB1 can also be the claimed "first substrate" for this claim.

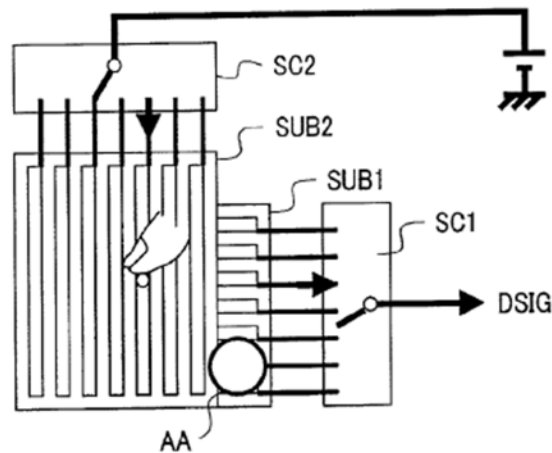
168. Nakamura goes on to discuss the detection areas and outside areas of its substrates in which external terminals are formed several additional times. *See, e.g.*, Ex. 1004, [0079], [0083] (discussing the "detection area"), [0102] (same), [0105] (same), [0108] (same) [0095]-[0097] (discussing the "external terminals" and area "outside the detection area," including "the external terminals and wirings MLINEF extending up to the external terminals"), [0111], Fig. 7 (showing MLINE wiring in detection areas and MLINEF wiring connecting to external terminals in outside areas):

FIG. 7



169. As discussed throughout Nakamura's disclosure, its first substrate (*i.e.*, bottom substrate SUB1, or, in the alternative, top substrate SUB2) includes a plurality of first lines to detect a coordinate in the detection area, and its second substrate includes a plurality of second lines to detect the coordinate in the detection area. *See, e.g.*, Ex. 1004, [0003], [0079] ("The coordinate detection is performed on the metal wiring"), [0053] ("second peripheral circuit SC2 is connected to the second substrate SUB2, and selects the metal wiring line by line to input a voltage thereto from the power supply"), [0054] ("first peripheral circuit SC1 is connected to the first substrate SUB1, and selects the metal wiring line by line to detect a voltage therefrom"), [0111] ("In a case where the metal wiring is used as a wiring for the coordinate detection as in Wiring Layout Modes 1 to 9..."), Fig. 1:

FIG. 1



170. Nakamura's Figs. 1-2 additionally show that its first and second substrates "are arranged so that their respective metal wirings face each other and that directions along which the respective metal wirings extend are made to intersect," *i.e.*, its substrates are arranged so that each of the plurality of first lines traverse each of the plurality of second lines. Ex. 1004, [0052], Figs. 1-2:

FIG. 1

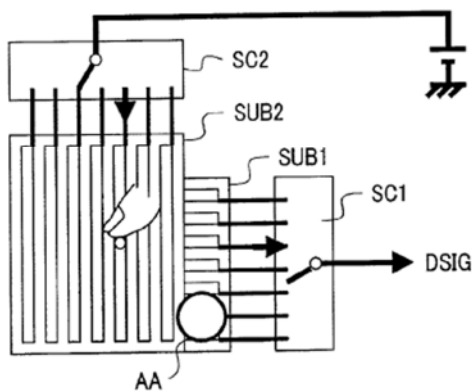
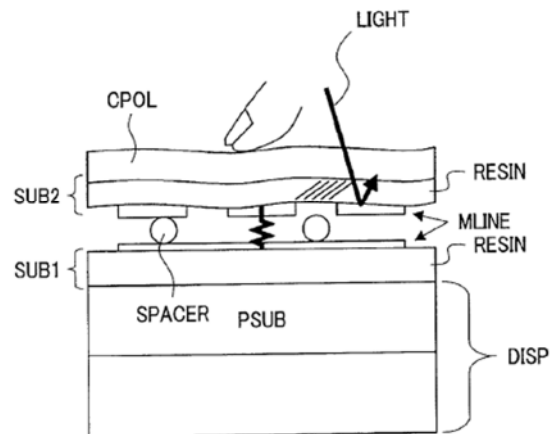
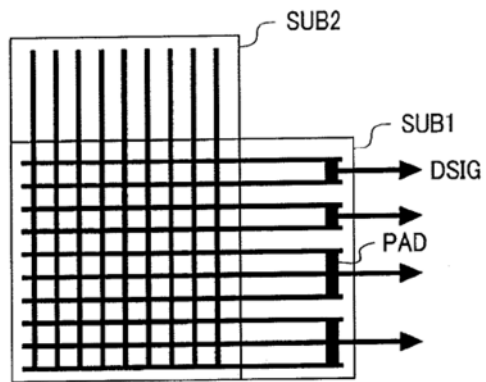


FIG. 2



See also [0093], Fig. 6:

FIG.6



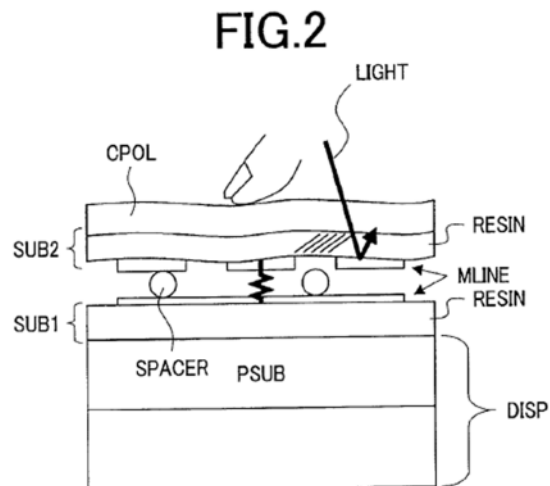
171. I note that the disclosure of this concept in the '836 Patent is substantially similar to this disclosure in Nakamura, to the extent that the '836 Patent expressly “adopts” Nakamura in discussing it. *See, e.g.*, Ex. 1001, 6:45-7:14, Figs. 9-10 (two-substrate structure in '836 patent).

172. For at least these reasons, Nakamura discloses and renders obvious a touch panel that includes a first substrate having a detection area to detect a coordinate and an outside area in which external terminals are formed, a plurality of first lines to detect the coordinate in the detection area, a plurality of second lines to detect the coordinate in the detection area, each of the plurality of first lines traversing each of the plurality of second lines.

c) Element [8-B]

173. Nakamura discloses and renders obvious this element of Claim 8: “an organic luminescence electric device panel which is adhered to the touch panel.”

174. Nakamura’s Fig. 2 shows that “the touch panel of FIG. 1 is bonded to a surface of a display panel,” and the “display device with the touch panel includes a display panel substrate PSUB composing a display device DISP, the first substrate SUB1, the second substrate SUB2, a spacer SPACER, and a circularly polarizing plate CPOL.” Ex. 1004, [0055], Fig. 2:

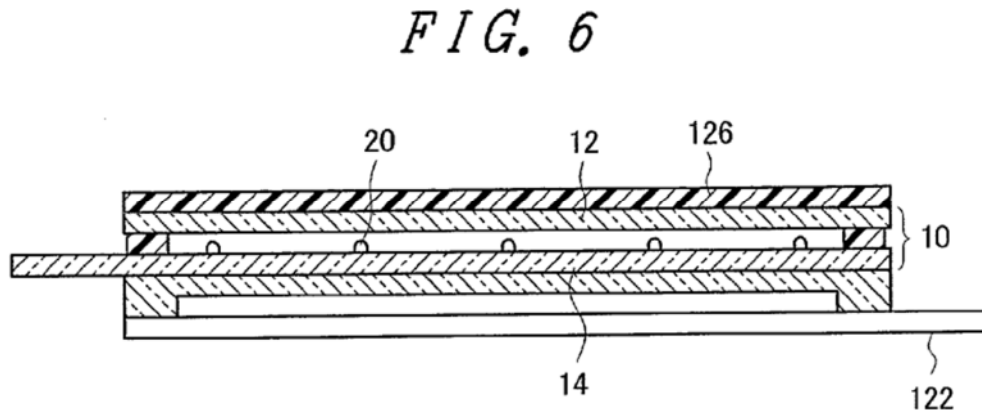


175. Nakamura explains that “[t]he display panel substrate PSUB” constitutes “a display-surface-side substrate similar to a counter substrate of a liquid crystal display device and a sealing substrate of a top emission organic EL display device.” Ex. 1004, [0055]. Nakamura’s “top emission organic EL display device” panel is “an organic luminescence electric device panel.” Specifically, a POSITA would know that EL is an acronym for electroluminescent, and indeed, therefore, an organic emitting display panel is an organic electroluminescent display device. The use of the phrase “top emission” in Nakamura further confirms this understanding, since it makes clear that the display is an emissive element, again exactly as is an organic “emitting” display panel.

176. OLEDs like Nakamura's organic EL display were well-known display devices in 2009. POSITAs at the time understood that the selection of one type of well-known display device, such as a liquid crystal display or OLED display, was an obvious and routine one that they could implement as they chose based on the design needs of their system.

177. Nakamura also explains that "[t]he first substrate SUB1 is adhered onto the display panel substrate PSUB." Ex. 1004, [0055].

178. I note that the disclosure of this concept in the '836 Patent is substantially similar to this disclosure in Nakamura. See Ex. 1001, 5:52-63, Fig. 6 (showing same arrangement of "circular polarizing plate" 126, "touch panel" 10 comprising substrates 12 and 14, and "organic EL display panel" 122):



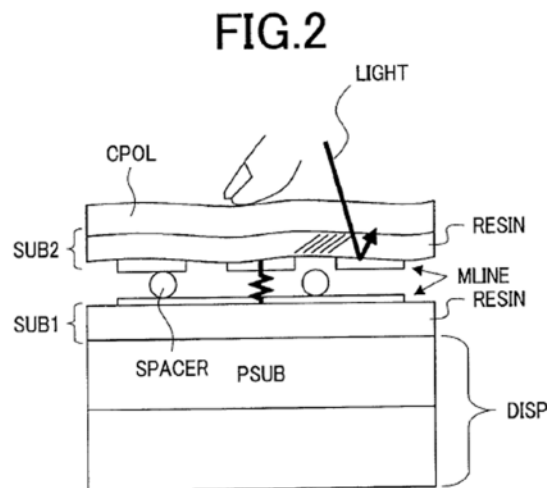
179. As confirmation of this, during the prosecution of the '836 Patent's child '229 Patent, the examiner expressly applied Nakamura against similar claim language. Ex. 1006 ('229 File History), 8/2/2016 Office Action, pp. 7-8. The examiner also stated that Nakamura discloses an “organic EL display, predetermined layer of resin, touch panel, and circular polarizing plate and polarizing circular plates [that] adheres to touch panel,” and a “touch panel with circular polarized plates bonded to resin with organic EL display.” *Id.* The patent owner did not dispute that Nakamura disclosed these concepts, and instead amended the claims. *Id.*, 11/1/2016 Response.

180. For at least these reasons, Nakamura discloses and renders obvious an organic luminescence electric device panel which is adhered to the touch panel.

d) Element [8-C]

181. Nakamura discloses and renders obvious this element of Claim 8: “a circular polarizing plate which is adhered to the touch panel at a side opposite to the organic luminescence electric device panel.”

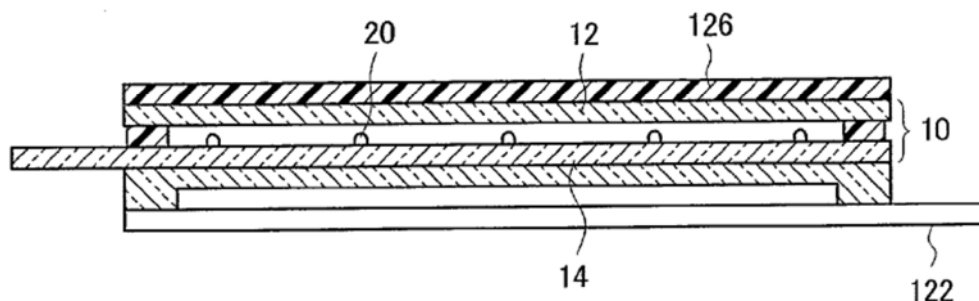
182. As I discussed for the previous limitation, Nakamura's Fig. 2 shows that "the touch panel of FIG. 1 is bonded to a surface of a display panel," and the "display device with the touch panel includes a display panel substrate PSUB composing a display device DISP, the first substrate SUB1, the second substrate SUB2, a spacer SPACER, and a circularly polarizing plate CPOL." Ex. 1004, [0055], Fig. 2:



183. Nakamura also explains that “[t]he circularly polarizing plate CPOL is fixed onto the second substrate SUB2.” Ex. 1004, [0055]. A POSITA would have understood that this statement that the CPOL is fixed onto the substrate means it is adhered to the touch panel, or at a minimum that it would have been obvious to fix the CPOL to the touch panel by adhering. They would have understood that, in 2009, adhering was one of a few obvious ways to fix display device components together, and that the selection of any such ways would have been an obvious design choice. This is particularly the case because Nakamura mentions adhering the substrate in this same paragraph. *Id.*; Ex. 1004, [0055].

184. Nakamura’s Fig. 2 also shows that its circularly polarizing plate CPOL is adhered to the touch panel at a side opposite to the organic luminescence electric device panel, and that the “top emission organic EL display device” located in the display panel substrate PSUB. Ex. 1004, [0055], Fig. 2.

185. I note that the disclosure of this concept in the ’836 Patent is substantially similar to this disclosure in Nakamura. *See* Ex. 1001, 5:52-63, Fig. 6 (showing same arrangement of “circular polarizing plate” 126, “touch panel” 10 comprising substrates 12 and 14, and “organic EL display panel” 122):

FIG. 6

186. As confirmation of this, during the prosecution of the '836 Patent's child '229 Patent, the examiner expressly applied Nakamura against similar claim language. Ex. 1006 ('229 File History), 8/2/2016 Office Action, pp. 7-8. The examiner also stated that Nakamura discloses a "circular polarizer [that] adheres to touch panel," which the examiner stated was well known to a POSITA, an "organic EL display, predetermined layer of resin, touch panel, and circular polarizing plate and polarizing circular plates [that] adheres to touch panel please see figure 2," and a "touch panel with circular polarized plates bonded to resin with organic EL display." *Id.* The patent owner did not dispute that Nakamura disclosed these concepts, and instead amended the claims. *Id.*, 11/1/2016 Response.

187. For at least these reasons, Nakamura discloses and renders obvious a circular polarizing plate which is adhered to the touch panel at a side opposite to the organic luminescence electric device panel.

7. Dependent Claim 9

188. Claim 9 of the '836 Patent depends from Claim 8. Claim 8 is disclosed and rendered obvious by Nakamura, for at least the reasons discussed above.

189. The additional limitation of Claim 9 is identical to that of Claim 1 Element [1-D]. Thus, Nakamura discloses and renders obvious the additional limitation of Claim 9 for the same reasons I discussed above for Claim 1 Element [1-D]. *See* Section X.A.1.e.

8. Dependent Claim 10

190. Claim 10 of the '836 Patent depends from Claim 8. Claim 8 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

191. The additional limitation of Claim 10 is a broader version of Claim 1 Element [1-F]. While Element [1-F] requires the plurality of wiring groups to be on the first substrate, Claim 10 allows the wiring groups to be anywhere on the touch panel, including on either of substrates SUB1 or SUB2.

192. Thus, regardless of which substrate is labeled the “first substrate” in Nakamura, Nakamura discloses and renders obvious Claim 10 for at least the same reasons I discussed above for Claim 1 Element [1-F]. *See* Section X.A.1.g.

9. Dependent Claim 11

193. Claim 11 of the '836 Patent depends from Claim 10. Claim 8 is

disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

194. The additional limitation of Claim 11 is a broader version of Claim 6. While Claim 6 requires the plurality of wiring groups to be on the first substrate, via Claim 1, Claim 11 allows the wiring groups to be anywhere on the touch panel, including on either of substrates SUB1 or SUB2.

195. Thus, regardless of which substrate is labeled the “first substrate” in Nakamura, Nakamura discloses and renders obvious Claim 11 for at least the same reasons I discussed above for Claim 6. *See* Section X.A.4.

10. Dependent Claim 12

196. Claim 12 of the '836 Patent depends from Claim 9. Claim 9 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

197. The additional limitation of Claim 12 is a broader version of Claim 7.

198. When Claim 7 applies the transparent conductive film to the plurality of the second lines, these second lines are required to be on the second substrate, due to Claim 1. Claim 12, however, allows the transparent conductive film to be anywhere on the touch panel, including on either of substrates SUB1 or SUB2.

199. Another difference between Claims 12 and 7 is that Claim 12 says the “transparent conductive film **overlays** the plurality of the second lines” while

Claim 7 says the film “**overlaps**” the second lines. This is not a substantive difference.

200. Thus, Nakamura discloses and renders obvious Claim 12 for at least the same reasons I discussed above for Claim 7. *See* Section X.A.5.

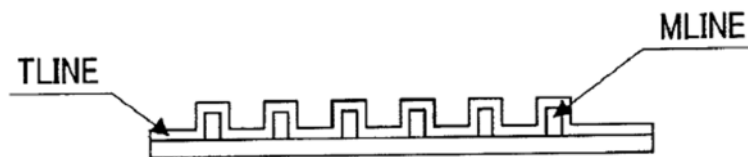
11. Dependent Claim 13

201. Claim 13 of the '836 Patent depends from Claim 10. Claim 10 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

202. Claim 13 further recites: “a transparent conductive film overlays the plurality of the first lines” and “the transparent conductive film is electrically connected to the plurality of the first lines.” Nakamura discloses and renders obvious this additional limitation.

203. I note that the disclosure of this concept in the '836 Patent is the same as in Nakamura. *See* Ex. 1001, 9:63:10-3, Fig. 18.

204. Nakamura's Fig. 10 shows “that a transparent wiring (electrode) TLINE that covers the entirety of the detection area is located above the metal wiring MLINE.” Ex. 1004, [0105], Fig. 10:

FIG. 10

205. Nakamura explains throughout its disclosure that transparent wiring TLINE is a transparent conductive film that is electrically connected to the metal lines MLINE. *See, e.g.*, Ex. 1004, [0007]-[0008], [0102], [0105]. And as shown in Fig. 10, TLINE overlays the MLINEs.

206. As Nakamura explains, “[t]his [Fig. 10 wiring] mode can be applied to the stripe-shaped metal wirings according to Wiring Layout Modes 1 to 5.” Ex. 1004, [0106]. Wiring Layout Mode 1 is the preferred embodiment shown in Figs. 1-3. *Id.*, [0050]-[0080].

207. As confirmation of this, during the prosecution of the ’836 Patent’s child ’229 Patent, the examiner expressly applied Nakamura against identical claim language. Ex. 1006 (’229 File History), 8/2/2016 Office Action, pp. 10-11. The patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

208. Nakamura’s teachings regarding Fig. 10 apply to both the first lines and second lines for several reasons. At the threshold, Nakamura’s discussion of Fig. 10 does not limit which lines its teachings apply to. Additionally, as I have

previously discussed, the disclosure of this concept in the '836 Patent is the same as in Nakamura. Further, as I have also discussed, Nakamura was applied against identical claim language during the prosecution of a related patent. Moreover, the metal lines MLINE on both of Nakamura's substrates are used for coordinate detection, such that both could benefit from transparent conductive film overlays. Ex. 1004, [0079]. As discussed above in Section X.A.1.g, it would have been obvious to a POSITA that either of Nakamura's substrates could serve as the "top" or "bottom" substrate. As such, a POSITA would have recognized that the lines used for application of voltage and those used for detection could be placed on either substrate without concern. Under these circumstances, at a minimum, a POSITA would have found it obvious to apply Nakamura's Fig. 8 and 9 concepts to its first lines in addition to its second lines.

209. For at least these reasons, Nakamura discloses and renders obvious that a transparent conductive film overlays the plurality of the first lines and the transparent conductive film is electrically connected to the plurality of the first lines.

12. Dependent Claim 14

210. Claim 14 of the '836 Patent depends from Claim 9. Claim 9 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

211. Claim 14 further recites: “a transparent conductive film underlays the plurality of the second lines” and “the transparent conductive film is electrically connected to the plurality of the second lines.” Nakamura discloses and renders obvious this additional limitation. This is the case in several embodiments.

212. I note that the disclosure of this concept in the '836 Patent is the same as in Nakamura. *See* Ex. 1001, 9:47-62, Figs. 16-17.

213. A first embodiment is shown in Fig. 8, about which Nakamura discloses “that a stripe-shaped transparent wiring TLINE having the same pattern as that of the metal wiring MLINE is located under the metal wiring MLINE.” Ex. 1004, [0099], Fig. 8:

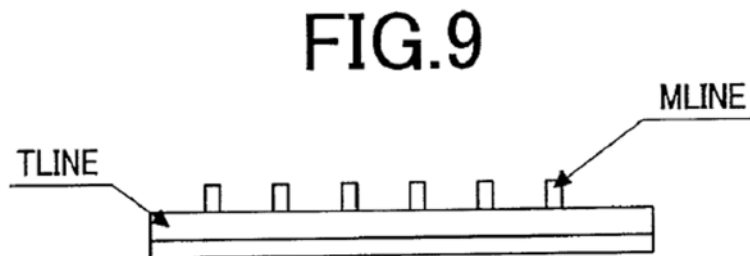


214. Nakamura explains throughout its disclosure that the transparent wiring TLINE is a transparent conductive film that is electrically connected to the metal lines. *See, e.g.*, Ex. 1004, [0007]-[0008], [0102], [0105]. And as applied to and shown in Fig. 8, a collection of TLINEs underlays and connects to the plurality of MLINEs.

215. A second embodiment is shown in Fig. 9, about which Nakamura

discloses “that a transparent wiring (electrode) TLINE that covers the entirety of the detection area is located under the metal wiring MLINE.” Ex. 1004, [0102],

Fig. 9:



216. Here again, TLINE underlays the MLINEs.

217. As Nakamura explains, the wirings shown in all of Figs. 8-9 “can be applied to the stripe-shaped metal wirings according to Wiring Layout Modes 1 to 5.” Ex. 1004, [0100], [0103]. Wiring Layout Mode 1 is the preferred embodiment shown in Figs. 1-3. *Id.*, [0050]-[0080].

218. As confirmation of this, during the prosecution of the '836 Patent's child '229 Patent, the examiner expressly applied Nakamura against identical claim language. Ex. 1006 ('229 File History), 8/2/2016 Office Action, p. 11. The patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

219. For at least these reasons, Nakamura discloses and renders obvious that a transparent conductive film underlays the plurality of the second lines and

the transparent conductive film is electrically connected to the plurality of the second lines.

13. Dependent Claim 15

220. Claim 15 of the '836 Patent depends from Claim 10. Claim 10 is disclosed and rendered obvious by Nakamura, for at least the reasons I discussed above.

221. Claim 15 further recites: “a transparent conductive [sic] film underlays the plurality of the first lines” and “the transparent conductive film is electrically connected to the plurality of first line.” Nakamura discloses and renders obvious this additional limitation. This is the case in several embodiments.

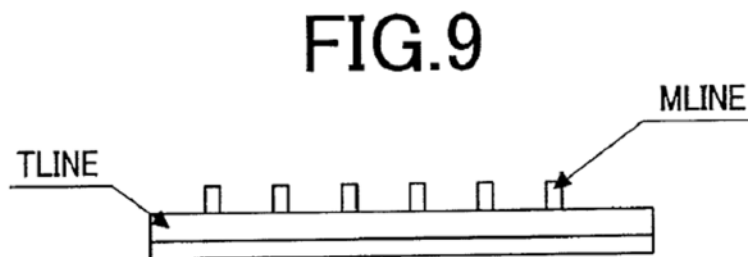
222. I note that the disclosure of this concept in the '836 Patent is the same as in Nakamura. See Ex. 1001, 9:47-62, Figs. 16-17.

223. A first embodiment is shown in Fig. 8, about which Nakamura discloses “that a stripe-shaped transparent wiring TLINE having the same pattern as that of the metal wiring MLINE is located under the metal wiring MLINE.” Ex. 1004, [0099], Fig. 8:



224. Nakamura explains throughout its disclosure that the transparent wiring TLINE is a transparent conductive film that is electrically connected to the metal lines. *See, e.g.*, Ex. 1004, [0007]-[0008], [0099], [0102], [0105]. And as applied to and shown in Fig. 8, a collection of TLINEs underlays and connects to the plurality of MLINEs.

225. A second embodiment is shown in Fig. 9, about which Nakamura discloses “that a transparent wiring (electrode) TLINE that covers the entirety of the detection area is located under the metal wiring MLINE.” Ex. 1004, [0102], Fig. 9:



226. Here again, TLINE underlays the MLINEs.

227. Nakamura explains throughout its disclosure that the wirings shown in all of Figs. 8-9 “can be applied to the stripe-shaped metal wirings according to Wiring Layout Modes 1 to 5.” Ex. 1004, [0100], [0103]. Wiring Layout Mode 1 is the preferred embodiment shown in Figs. 1-3. *Id.*, [0050]-[0080].

228. As confirmation of this, during the prosecution of the '836 Patent's child '229 Patent, the examiner expressly applied Nakamura against identical claim

language. Ex. 1006 ('229 File History), 8/2/2016 Office Action, p. 11. The patent owner did not dispute that Nakamura disclosed this concept, and instead amended the claims. *Id.*, 11/1/2016 Response.

229. Nakamura's teachings regarding Figs. 8 and 9 apply to both the first lines and second lines for several reasons. At the threshold, Nakamura's discussion of Figs. 8 and 9 does not limit which lines its teachings apply to. Additionally, as I have previously discussed, the disclosure of this concept in the '836 Patent is the same as in Nakamura. Further, as I have also discussed, Nakamura was applied against identical claim language during the prosecution of a related patent. Moreover, the metal lines MLINE on both of Nakamura's substrates are used for coordinate detection, such that both could benefit from transparent conductive film overlays. Ex. 1004, [0079]. As discussed above in Section X.A.1.g, it would have been obvious to a POSITA that either of Nakamura's substrates could serve as the "top" or "bottom" substrate. As such, a POSITA would have recognized that the lines used for application of voltage and those used for detection could be placed on either substrate without concern. Under these circumstances, at a minimum, a POSITA would have found it obvious to apply Nakamura's Fig. 8 and 9 concepts to its first lines in addition to its second lines.

230. For at least these reasons, Nakamura discloses and renders obvious

that a transparent conductive film underlays the plurality of the first lines and the transparent conductive film is electrically connected to the plurality of the first lines.

B. Ground 2 – Nakamura, As Well as Nakamura in Combination with Slobodin, Renders Claim 2 Obvious

231. In my opinion, Nakamura renders Claim 2 of the '836 Patent obvious, both alone and in combination with Slobodin.

1. Dependent Claim 2

232. Claim 2 of the '836 Patent depends from Claim 1. Nakamura discloses and renders obvious Claim 1 for at least the reasons I discussed above for that claim. *See* Section X.A.1.

233. Claim 2 further recites: “the polarizing plate comprises a linear polarizing plate.” Nakamura renders this additional limitation obvious, both alone and in combination with Slobodin.

234. At the outset, it is important to understand a few things points regarding the '836 Patent's discussion of polarizing plates (or lack thereof). For one thing, the '836 Patent does not claim to have invented the concept of a polarizing plate of any type or allege that it was novel or nonobvious. Nor does the '836 Patent describe the structure or operation of a any sort of polarizing plate, much less linear or circular polarizing plates specifically. This lack of discussion is reflected in the claims. '836 Patent independent Claim 1 just recites a

“polarizing plate,” meaning that it can comprise both the “linear polarizing plate” of dependent Claim 2 and the “circular polarizing plate” of dependent Claim 3.

This generalized claiming, combined with a lack of any explanation in the specification about the nature of polarizing plates, demonstrates the obviousness of both types of plates.

235. As I discussed for Claim 1 in Section X.A.1.f above, Nakamura discloses both the use of a polarizing plate generally, and also the use of a circular polarizing plate specifically in its Fig. 2 embodiment.

236. In view of this disclosure, at a minimum, a POSITA would have considered it obvious for Nakamura to use a linear polarizing plate generally, as well as to substitute the circular polarizing plate of Nakamura’s Fig. 2 embodiment with a linear polarizing plate. They also would have considered this selection or substitution obvious because linear and circular polarizers are the two most common polarizers. A POSITA would have found it obvious to use either type of polarizing in Nakamura, depending on the needs of the application and design choices.

237. For example, a POSITA would have been motivated to select a linear polarizer for use in Nakamura and also to replace the circular polarizer in Nakamura’s Fig. 2 embodiment with a linear polarizer in applications where linear polarizers adequately suppress ambient light. By doing so, they would have been

able to save on both costs and valuable space in their touch panel.

238. This understanding is confirmed by Nakamura's general statement that the "polarizing plate" it utilizes is included to "suppress ambient light reflection." Ex. 1004, [0029], [0061]. Importantly, Nakamura does not state how much reflection necessarily needs to be suppressed, and it also does not state that a circular polarizer is required to sufficiently suppress reflection. *Id.* In view of this disclosure, a POSITA would have understood Nakamura to be explaining that a linear polarizer could have sufficiently suppressed reflection in various applications.

239. Another reason why POSITA would have found it obvious to choose a linear polarizing plate for use in Nakamura occurs in applications of Nakamura that use an LCD display, which Nakamura discloses. Ex. 1004, [0055], [0078]. '836 Patent Claim 2 is not limited to any particular type of display, and it was common in 2009 to use linear polarizing plates in conjunction with LCD displays.

240. While a POSITA would have found it obvious to select a linear polarizer or replace the circular polarizer in Nakamura's Fig. 2 embodiment with a linear polarizer based on Nakamura alone for at least these reasons, they also would have found it obvious to modify Nakamura's polarizer in view of Slobodin.

241. A POSITA would have been motivated to combine Nakamura and Slobodin for at least the reasons that I discussed in Section IX.C above, as well as

the reasons I discuss in the following paragraphs.

242. Slobodin elaborates on the concept that a “polarizing material may be incorporated onto the outer surface of the touch sensor to help control the surface reflections from the touch sensor.” Ex. 1005, [0009]. In some systems, “a linear polarizer may be applied to the outer surface of the touch sensor with its pass axis aligned with the output polarizer of the underlying display.” *Id.* “The linear polarizer may absorb over 50% of the light incident on the touch sensor, reducing the surface reflections by the same amount, while passing almost all of the light emitted by the underlying display.” *Id.*

243. But in other systems, Slobodin explains, designers may choose to have light incident on the surface of the touch sensor both “linearly polarized and then rotated to circular polarization, absorbing over 50% of the incident light.” *Id.* This “circularly polarized incident light that passes into the touch sensor may partially reflect off of the various surface interfaces in the touch sensor and display.” *Id.* Because circularly polarized light changes orientation when it reflects, “the reflected light may be absorbed in the circular polarizer on the reflected path, substantially eliminating internal touch sensor reflections.” *Id.*

244. But Slobodin goes on to explain that, “in touch sensors that incorporate birefringent materials, such as polyethylene terephthalate (PET), the opportunity to improve the optical performance of the display may be limited.”

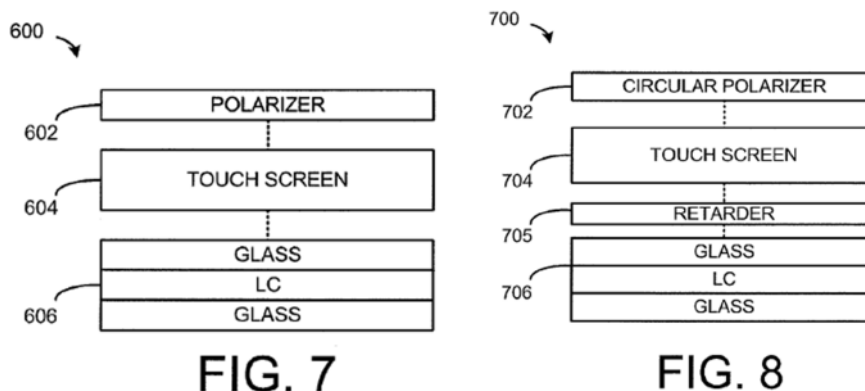
Id., [0010].

245. A birefringent material is one that exhibits different refractive indices for light polarized in different directions. This means that when light passes through a birefringent material, it effectively splits into two rays, each with a different speed and polarization. This phenomenon is also known as double refraction.

246. Slobodin goes on to also discuss how this limitation on optical performance in birefringent materials “may be even more pronounced if a touch sensor polarizer is attached to the outer surface of the touch sensor.” Ex. 1005, [0010]. In this situation, even when a circular polarizer is used, the birefringent layers pollute the linearly polarized light emitted from the underlying display and some of the desired light may be absorbed by the polarizer on the outer surface of the touch sensor, reducing image uniformity. *Id.* Additionally, “incident light that is controlled by the circular polarizer is similarly polluted, reducing the effectiveness of the incident light control normally afforded by the circular polarizer.” *Id.*

247. Consistent with its discussion of how linear polarizers may be preferable in certain situations, while circular polarizers may be preferable in others, Slobodin discloses two display system embodiments. Each embodiment utilizes one such type of polarizer in detail: a linear polarizer in Fig. 7 and a

circular polarizer in Fig. 8. *See* Ex. 1005, [0050]-[0052], Figs. 7-8:



248. I note that Slobodin’s Fig. 7 polarizer is labeled as simply a “polarizer.” However, in view of Slobodin’s extension discussion of the differences between linear and circular polarizers and Fig. 8’s disclosure of a circular polarizer, a POSITA would have understood that Fig. 7’s polarizer is a linear polarizer. Ex. 1005, [0009]-[0010], [0050]-[0052], Figs. 7-8.

249. To summarize, Slobodin teaches that, in certain touch sensors, including those incorporating birefringent materials, the benefits that circular polarizers often provide cannot fully be taken advantage of. And because Nakamura states only that the “polarizing plate” it utilizes needs to “suppress ambient light reflection,” without requiring a particular amount of suppression or type of polarizer, a POSITA would have understood this to mean that a linear polarizer could have sufficiently suppressed reflection in certain situations. Ex. 1004, [0029], [0061]. For example, in applications of Nakamura that included birefringent materials, a POSITA would have been motivated to use a simpler and

less expensive linear polarizer. Indeed, Slobodin teaches exactly that. Ex. 1005, [0009]-[0010] (explaining that a “linear polarizer may absorb over 50% of the light incident on the touch sensor,” which cannot be meaningfully improved on when birefringent materials are used), [0023] (explaining how Slobodin’s teachings may improve performance by “reducing reflectance within the system, simplifying manufacturing and/or reducing manufacturing costs while retaining the advantages of prior touch sensors”).

250. For at least these reasons, a POSITA would have found it obvious to select a linear polarizer for use in Nakamura and also to replace the circular polarizer in Nakamura’s Fig. 2 embodiment with a linear polarizer like the one taught by Slobodin.

XI. SECONDARY CONSIDERATIONS

251. I am not aware of secondary considerations of non-obviousness that bear on the challenged claims. If I am made aware in the future of arguments of any secondary consideration, I expressly reserve the right to assess those arguments when they arise in order to form opinions regarding their correctness or incorrectness.

XII. CONCLUSION

252. It is my conclusion and opinion that Claims 1-15 of the ’836 Patent are invalid.

I declare under penalty of perjury that the foregoing is true and correct.

Executed this 3rd day of July, 2025 in Morges, Switzerland.

Vivek Subramanian

Dr. Vivek Subramanian

Appendix A

Vivek Subramanian

@ Berkeley:

513 Sutardja Dai Hall
University of California
Berkeley, CA 94720-1770, USA
Ph: +1 (510) 643-4535
Email: viveks@eecs.berkeley.edu

@ EPFL

Rue de la Maladière 71
CH-2000 Neuchâtel, Switzerland
Ph: +41 21 695 42 65
Email: vivek.subramanian@epfl.ch

@ Virtual Mailbox

700 Lavaca #1400-91298
Austin, TX 78701, USA

Education

3 / 96 - 6 / 98

Ph.D. in Electrical Engineering, Stanford University Stanford, California

Honors earned: Graduate Fellowship, Eastman Kodak Company

9 / 94 - 3 / 96

MS in Electrical Engineering, Stanford University Stanford, California

8 / 90 - 5 / 94

BS in Electrical Engineering, Louisiana State University Baton Rouge, Louisiana

Honors earned: Summa cum laude, College Honors, Outstanding Senior, Junior and Sophomore, Honors College

Professional Experience

2018 - present

École polytechnique fédérale de Lausanne Switzerland

8/18 – present: Professor of Microengineering

2000 - present

Department of Electrical Engineering & Computer Sciences, University of California Berkeley, CA

7/18 – present: Chancellor's Professor

7/11 – present: Professor

7/05 – 7/11: Associate Professor

7/00-7/05: Assistant Professor

Research, teaching and service in EECS Department

Honors Earned:

2015 IEEE Kiyo Tomiyasu Award
Best in session and best in track awards, 2013 IMAPS Microelectronics Conference
Outstanding paper award, 2012 IMAPS Microelectronics Conference
2008 Printed Electronics Champion, Printed Electronics USA Conference, November 2008
Outstanding Teaching Award, EECS Department, UC Berkeley, 2005
Best paper award, 2004 IEEE Device Research Conference
Nominated to MIT's Technology Review top 100 young innovators list (TR100), 2002
National Science Foundation Young Investigator (CAREER) Award, FY2002,
Nominated to National Academy of Engineering's *Frontiers of Engineering*, 2002
Winner of 2002 Paul Rappaport Award for best paper in an IEEE EDS Journal

2009 - present

Adjunct Professor, Sunchon National University

Sunchon, Korea

2013 to date: Adjunct Professor, BK21 Program

2009-2013: Adjunct Professor and Principal Investigator, WCU Program

Initiated, managed, and contributed to large multinational research program focused on printed electronics, including displays, energy devices, and RFID

2000 - present

Independent Consultant

Orinda, CA

Consultant to the semiconductor industry and its associated fields in the following areas:

Memory technology and design, Silicon Process Technology
Display / Imager and Flexible Electronics Technology, RFID Technology
Intellectual Property Consulting
Technology Evaluation / Venture Capital due diligence

2014- present	Founder and CTO, Locix Inc. <i>San Bruno, CA</i> <i>Senior leadership role in venture-funded startup company working on wireless networking</i>
2004 – 2013	Founding Scientific Advisor, Kovio, Inc. <i>Sunnyvale, CA</i> <i>Scientific advising to printed electronics startup company</i>
2008 - 2011	Chief Technical Advisor, QuSwami, Inc. <i>San Francisco, CA</i> <i>Scientific advising to energy conversion device startup company</i> Served as CTO from July 2010-June 2011
1998 - 2000	Consulting Assistant Professor, Electrical Engineering Department, Stanford University. <i>Stanford, CA</i> Advisory role for research group of Prof. Krishna C. Saraswat
1998-2000	Visiting Research Engineer, Electrical Engineering Department, University of California. <i>Berkeley, CA</i> Research into 25nm MOSFET technologies for giga-scale integration
1998 - 2000	Founder, Matrix Semiconductor, Inc. <i>Santa Clara, CA</i> Co-founder and technical advisor of startup company working on high-density memory technology Honors Earned: Nominated to Scientific American's SA50 List for Visionary Technology Finalist for 2003 World Technology Award for Information Technology Hardware Winner, 2005 EDN Innovation Award
1998	Co-instructor, Electrical Engineering Department, Stanford University. <i>Stanford, CA</i> Co-teaching of EE311, Advanced Integrated Circuit Fabrication Processes
1997	Intern, Advanced Product Research and Development Laboratory, Motorola Inc. <i>Austin, TX</i> Research into process development issues affecting SiGe SEMFET devices
1996	Head Teaching Assistant EE410: IC Fabrication Laboratory, Stanford University <i>Stanford, CA</i> Coordination and instruction of EE410, graduate level laboratory course.
1994-1998	Research Assistant, Electrical Engineering, Stanford University <i>Stanford, CA</i> Research into crystallization of amorphous Si and SiGe films using low thermal budget processes.
	Professional Affiliations and Activities Technical Program Committee, IEEE Electronic Components and Technology Conference, 2014 to 2016 Chair, Scientific Advisory Board, iPACK, Royal Institute of Technology (KTH), Sweden, 2011 to 2016 Tampere Institute of Technology Faculty Search Committee, Finland, 2013 University of Oulu Faculty Search Committee, Finland, 2013 Served as external thesis committee member for several universities world-wide, including University of Cape Town (South Africa), Tampere Institute of Technology (Finland), Technical University of Eindhoven (Netherlands), Indian Institute of Science (India), Indian Institute of Technology (India), 2009 to date Associate Editor, IEEE Journal of Display Technology, 2008 to date Technical Program Chair, Large Area, Organic, and Printed Electronics Conference, 2012-2013 Scientific Committee, Large Area, Organic, and Printed Electronics Conference, 2009-2011 Scientific Committee, International Conference on Printed and Flexible Electronics, 2009-2013 IEEE Electron Devices Society Organic Electronics Committee, 2003 - 2005 Executive Committee, International Electron Device Meeting, 2003 to 2009 Technical Program Committee, International Electron Device Meeting, 2001-2002 Technical Program Committee member, Device Research Conference, 2000-2002 Technical Program Committee member, VLSI-TSA Conference, 2005 Member, Institute of Electrical and Electronic Engineers

List of cases worked on by Vivek Subramanian

Completed

- Lexar Media v. Pretec Electronics Corp., et al (N.D. Cal., Case No. 00-CV-4770 MJJ, deposition) – retained by Pretec Electronics Corp, PNY Electronics, Memorex
- Motorola, Inc. v. Analog Devices, Inc., Civil Action No. 1:03-CV-0131 – retained by Analog Devices
- *Sandisk Corporation vs. Micron*, Case No. CV-01-3855 CW – retained by Micron
- In the Matter of CERTAIN NAND FLASH MEMORY CIRCUITS AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-526, deposition and trial) – retained by STMicroelectronics
- In the Matter of CERTAIN NAND FLASH MEMORY DEVICES AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-553, deposition and trial) – retained by Hynix
- In the Matter of CERTAIN NOR AND NAND FLASH MEMORY DEVICES AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-560, deposition and trial) – retained by STMicroelectronics
- STMicroelectronics, Inc. v. SanDisk Corporation (E.D. Texas, Civil Action No. 4:05-CV-45, deposition) – retained by STMicroelectronics
- Sandisk Corporation v. Memorex Products, Inc. et al, CV 01-4063 – retained by Memorex.
- Seagate Technology LLC et al v. STEC, Inc., Case No. 5:08-CV-01950 JW (HRL) – retained by STEC.
- In the Matter of CERTAIN NAND FLASH MEMORY DEVICES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-592) – retained by Hynix
- In the Matter of CERTAIN FLASH MEMORY CONTROLLERS, DRIVES, MEMORY CARDS, AND MEDIA PLAYERS AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-619, deposition and trial) – retained by Phison Electronics, Silicon Motion, Kingston, and Apacer
- Harari and Mehrotra v. Hollmer and Cleveland (Board of Patent Appeals and Interferences, Interference# 105,606, deposition) – retained by Spansion

- In the Matter of CERTAIN SEMICONDUCTOR INTEGRATED CIRCUITS USING TUNGSTEN METALLIZATION AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-648) – retained by STMicroelectronics
- In the Matter of CERTAIN SEMICONDUCTOR CHIPS HAVING SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY CONTROLLERS AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-661, deposition and trial) – retained by NVidia
- Fast memory erase, LLC. v. Spansion, Inc. et al, Civil Action No. 3:08-CV-00977-M, retained by Spansion
- In the Matter of CERTAIN MOBILE TELEPHONES AND WIRELESS COMMUNICATIONS DEVICES FEATURING DIGITAL CAMERAS AND COMPONENTS THEREOF (ITC, Investigation No. 337-TA-663, deposition and trial) – retained by LG Electronics and Samsung Electronics
- In the Matter of CERTAIN MLC FLASH MEMORY DEVICES AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-683, deposition and trial) – retained by Samsung
- In the Matter of CERTAIN MOBILE TELEPHONES WIRELESS COMMUNICATION DEVICES FEATURING DIGITAL CAMERAS, AND COMPONENTS THEREOF (ITC, Investigation No. 337-TA-703, deposition and trial) – retained by Apple
- Vizio, Inc. v. L Electronics, Inc., et al, In the Unites States District Court For The District of Maryland, Civil action No. 1:09-CV-1481 (BEL), deposition – retained by LG
- In the Matter of CERTAIN ELECTRONIC DEVICES, INCLUDING MOBILE PHONES, PORTABLE MUSIC PLAYERS, AND COMPUTERS (ITC, Investigation No. 337-TA-701, deposition and trial) – retained by Apple
- Nokia v. Apple, 09-CV-791 and v09-CV-1002 – retained by Apple
- SanDisk Corporation v. Phison Electronics Corp., et al, In the United States District Court For The Western District of Wisconsin, Civil action No. 07-C-0605-C and 07-C-0607-C, deposition – retained by Phison Electronics Corp., Silicon Motion, Skymedi, and Kingston
- Microchip Technology Inc v. LSI Corporation and Agere Systems Inc., Case No. 2:11-cv-01326-DGC, retained by Microchip
- In the Matter of CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS, MEDIA PLAYERS AND CAMERAS (ITC, Investigation No. 337-TA-709, deposition and trial) – retained by Freescale Semiconductor, Inc.

- In the Matter of CERTAIN SEMICONDUCTOR PRODUCTS MADE BY ADVANCED LITHOGRAPHY TECHNIQUES AND PRODUCTS CONTAINING SAME, (ITC, Investigation No. 337-TA-729) – retained by Samsung
- In the Matter of CERTAIN MOBILE DEVICES AND RELATED SOFTWARE (ITC, Investigation No. 337-TA-750, deposition and trial) – retained by Apple, Inc.
- In the Matter of CERTAIN SEMICONDUCTOR CHIPS AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-753) – retained by NVidia
- In the Matter of CERTAIN MOBILE TELEPHONES AND MODEMS (ITC, Investigation No. 337-TA-758) – retained by LG.
- In the Matter of CERTAIN VIDEO GAME SYSTEMS AND WIRELESS CONTROLLERS AND COMPONENTS THEREOF (ITC, Investigation No. 337-TA-770, deposition and trial) – retained by Nintendo
- In the Matter of CERTAIN RANDOM ACCESS MEMORY DEVICES AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-595) retained by Renesas
- In the Matter of CERTAIN MICROPROCESSORS, COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME (ITC, Investigation No. 337-TA-781, deposition and trial) – retained by Intel
- In the Matter of CERTAIN DIGITAL TELEVISIONS CONTAINING INTEGRATED CIRCUIT DEVICES AND COMPONENTS THEREOF (ITC, Investigation No. 337-TA-806, deposition) – retained by Renesas
- In the Matter of CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS (ITC, Investigation No. 337-TA-786, deposition and trial) – retained by Freescale
- In the Matter of CERTAIN SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES AND PRODUCTS CONTAINING SAME (ITC Investigation No. 337-TA-840) – retained by Microchip.
- In the Matter of CERTAIN DYNAMIC RANDOM ACCESS MEMORY AND NAND FLASH MEMORY DEVICES AND PRODUCTS CONTAINING THE SAME (ITC, Investigation No. 337-TA-803, deposition) – retained by Hynix
- AVM Technologies LLC v. Intel Corporation, Civil Action No. 10-610-RK – retained by Intel
- Round Rock Research LLC v. Dell Inc., No. 11-CV-976-RGA – retained by Dell

- Solid State Storage Solutions, Inc. v. STEC, Inc., OCZ Technology, Inc. Corsair Memory, Texas Memory Systems, Inc. PNY Technologies, Inc., Patriot Memory LLC, Fusion-IO, Inc., Other World Computing, Inc., and Mushkin, Inc., Civil Action No 2:11-CV-391, retained by Corsair, PNY, and Fusion-IO.
- Grail Semiconductor, Inc., v. Renesas Electronics America, Inc., Case No. C 11-03847, retained by Renesas.
- In The Matter of Certain Wireless Consumer Electronics Devices and Components Thereof (ITC, Inv. No. 337-TA-853), retained by Amazon.com, Acer, Barnes & Noble, Garmin, HTC, Huawei, Kyocera, LG, Nintendo, Novatel, Samsung, and ZTE.
- Invensas Corporation v Renesas Electronics Corporation, Civil Action No. 11-448-GMS-CJB, retained by Renesas (deposition)
- In the Matter of Certain Non-volatile Memory Chips and Products Containing Same (ITC, Inv. No. 337-TA-916), retained by Macronix (deposition)
- Sandisk Corporation v. PNY Technologies, Inc., Case No. 1-11-CV-205928, retained by PNY (deposition)
- *TPK Touch Solutions, Inc. v. Wintek Electro-Optics Corporation, et al.*, 3:13-cv-02218-NC (N.D. Cal.), and associated issues in front of the patent board, retained by Wintek (deposition)
- GSI Technology, Inv. V. Cypress Semiconductor Corporation, IPR2014-00121 and associated issues in front of the patent board, retained by Cypress (deposition)
- Grail Semiconductor, Inc. v Mitsubishi, Case No. 1-07-CV-098590, retained by Mitsubishi
- AVM Technologies, LLC v. Intel Corporation, C.A. No. 15-33-RGA, retained by Intel (deposition and testimony)
- Intellectual Ventures LLV v. Toshiba, C.A. No. 13-453-SLR-SRF, retained by Toshiba (deposition and testimony)
- In the Matter of CERTAIN MEMORY MODEULS AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME, US ITC 337-TA-1023, retained by Hynix (deposition and testimony)
- In the Matter of CERTAIN INTEGRATED CIRCUITS WITH VOLTAGE REGULATORS AND PRODIUCTS CONTAINING THE SAME, US ITC 337-TA-1024, retained by Intel (deposition)

- Technology Properties Ltd, LLC v. LG et al, Case No. 3:12-cv-03880-VC, retained by defendants.
- Longitude Licensing Ltd. V Apple, Case 3:14-CV-04275-EDL, retained by Apple.
- KAIST IP v. Samsung et al, 2:16-cv-01314-JRG-RSP – retained by Samsung (deposition and trial).
- Toshiba Corporation v Lone Star Silicon Innovations LLC, IPR – retained by Toshiba
- Samsung Electronics Co Ltd. Vs PROMOS Technologies Inc, IPRs – retained by Samsung (deposition)
- Samsung Electronics Co. Ltd vs. UUSI LLC d/b/a Narton, IPRs – retained by Samsung (deposition)
- Carl Zeiss AG and ASML v Nikon, 2:17-cv-03221 RGK – retained by ASML and Zeiss (deposition and trial testimony)
- In the matter of CERTAIN MEMORY MODULES AND COMPONENTS THEREOF (ITC, Inv. No. 337-TA-1089), retained by SK Hynix (deposition and trial testimony)
- In the Matter of CERTAIN SOLID STATE STORAGE DRIVES, STACKED ELECTRONICS COMPONENTS, AND PRODUCTS CONTAINING SAME, US ITC 337-TA-1097, retained by Samsung and Hynix (deposition)
- In the Matter of CERTAIN INFOTAINMENT SYSTEMS, COMPONENTS THEREOF, AND AUTOMOBILES CONTAINING THE SAME, US ITC 337-TA-1119, retained by Renesas, Denso, Pioneer, Panasonic, Socionext, and Toyota (deposition and trial testimony)
- In the Matter of CERTAIN MOVABLE BARRIER OPERATOR SYSTEMS AND COMPONENTS THEREOF, US ITC 337-TA-1118, retained by Chamberlain (deposition and trial testimony)
- Fereydun Tabaian and Ahmad Ashrafzadeh v Intel Corporation, 3:18-cv-326-HZ., retained by Intel

Active

- Innovative Memory Systems, Inc. v. Micron Tech, In.c 14-cv-01480 and associated IPRs, retained by Micron (deposition)
- Kingston Technology Company v. Polaris Innovations Ltd, IPRs – retained by Kingston (deposition)

- Intel Corporation v. Tela Innovations, 18-cv-02848-WHO, retained by Intel (deposition)
- VLSI Technology LLC v. Intel Corporation, 1:18-cv-00966-CFC, retained by Intel
- X2Y Attenuators LLC v. Intel Corporation, Case No. 3:18-cv-1394-HZ, retained by Intel (deposition)
- In the Matter of CERTAIN TOUCH-CONTROLLED MOBILE DEVICES, COMPUTERS, AND COMPONENTS THEREOF, US ITC 337-TA-1162, retained by Samsung et al

List of Patents, Publications and Presentations

Patents

1. "Systems and methods for coarse and fine time of flight estimates for precise radio frequency localization in the presence of multiple communication paths", Seth, M., Kong, L., Ylamurto, T., Subramanian, V., US Patent 10,470,156
2. "Methods and apparatus for monitoring wound healing using impedance spectroscopy", Maharbiz, M., Subramanian, V., Arias, A.C., Swisher, S., Liao, A., Lin, M., Pavinatto, F., Khan, Y., Cohen, D., Leeftang, E., Roy, S., Harrison, M., Young, D., US Patent 10,463,293.
3. "Systems and methods for using radio frequency signals and sensors to monitor environments", T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,156,852.
4. "Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 10,104,508.
5. "Systems and methods for providing wireless asymmetric network architectures of wireless devices with power management features", V. Subramanian, E. Alon, V. Pavate, US Patent 10,028,220.
6. "Random delay generation for thin-film transistor based circuits", V Subramanian, M Mao, Z Wang, US Patent 9,985,664
7. "Systems and methods for determining locations of wireless sensor nodes in a network architecture having mesh-based features for localization", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,846,220
8. "Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features", L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,763,054
9. "Through silicon vias and thermocompression bonding using inkjet-printed nanoparticles", V. Subramanian and J. Sadie, US Patent 9,717,145
10. "Systems and methods for providing wireless asymmetric network architectures of wireless devices with anti-collision features", V. Subramanian, E. Alon, V. Pavate, US Patent 9,706,489
11. "Systems and methods for determining locations of wireless sensor nodes in an asymmetric network architecture", V. Subramanian, E. Alon, V. Pavate, US Patent 9,529,076
12. "Systems and methods for providing wireless sensor networks with an asymmetric network architecture", V. Subramanian, E. Alon, V. Pavate, US Patent 9,380,531
13. "Transparent metal oxide nanoparticle compositions, methods of manufacture thereof and articles comprising the same", V. Subramanian, S. K. Volkman, US Patent 9,343,202
14. "Three-dimensional nonvolatile memory and method of fabrication", M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 9,214,243
15. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 9,171,857
16. "Print compatible designs and layout schemes for printed electronics", Z. Wang, V. Subramanian, L. Cleveland, US Patent 9,155,202
17. "Wireless devices including printed integrated circuitry and methods for manufacturing and using the same", P. Smith, C. Choi, V. Pavate, J. M. Cleeves, V. Subramanian, R. Young, V. Biviano, US Patent 9,004,366.
18. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. Kouznetsov, US Patent, 8,981,457.
19. "High reliability surveillance and/or identification tag/devices and methods of making and using the same", V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, J. M. Cleeves, US Patent, 8,933,806.
20. "Surveillance devices with multiple capacitors", P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Molesa, US Patent, 8,912,890.
21. "Pillar-shaped nonvolatile memory and method of fabrication", M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 8,897,056
22. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,853,765

23. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,823,076
24. "Random delay generation for thin-film transistor based circuits", V. Subramanian, M. Mao, Z. Wang, US Patent 8,810,298
25. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8,503,215
26. "Process-variation tolerant series-connected NMOS and PMOS diodes, and standard cells, tags, and sensors containing the same", V. Subramanian, P. Smith, US Patent 8,471,308
27. "Printed compatible designs and layout schemes for printed electronics", Z. Wang, V. Subramanian, L. Cleveland, US Patent 8,383,952
28. "Method for making surveillance devices with multiple capacitors", P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Molesa, US Patent 8,296,943
29. "High reliability surveillance and/or identification tag/devices and methods of making and using the same", V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,264,359
30. "High reliability surveillance and/or identification tag/devices and methods of making and using the same", V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,227,320
31. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8,208,282
32. "Reliable tag deactivation", J. M. Cleeves, V. Subramanian, US Patent 8,138,921
33. "Combined static and dynamic frequency divider chains using thin film transistors", V. Subramanian, US Patent 8,085,068
34. "Process-variation tolerant diode, standard cells including the same, tags and sensors containing the same, and methods for manufacturing the same", V. Subramanian, P. Smith, US Patent 7,932,537
35. "Three terminal nonvolatile memory Device with vertical gated diode", T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. G. Kouznetsov, US Patent 7,825,455
36. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7,816,189
37. "Multi-mode tags and methods of making and using the same", P. Smith, J. M. Cleeves, V. Pavate, V. Subramanian, US Patent 7,750,792
38. "Method of manufacturing complementary diodes", V. Subramanian, P. Smith, US Patent 7,528,017
39. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7,319,053
40. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7,265,000
41. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7,160,761
42. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7,157,314
43. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. Petti, I. Kouznetsov, M. G. Johnson, P. M. Farmwald, B. Herner, US Patent 7,129,538
44. "Patterning three dimensional structures", C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleeves, V. Subramanian, US Patent 7,071,565
45. "Monolithic three dimensional array of charge storage devices containing a planarized layer", T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. J. Petti, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, and B. Herner, US Patent 6,881,994
46. "Thermal processing for three dimensional circuits", V. Subramanian, J. M. Cleeves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6,770,939

47. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. G. Johnson, T. H. Lee, V. Subramanian, and P. M. Farnwald, US Patent 6780711
48. "Multigate semiconductor device with vertical channel current and method of fabrication", J. M. Cleaves and V. Subramanian, US Patent 6677204
49. "Thermal processing for three dimensional circuits", V. Subramanian, J. M. Cleaves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6624011
50. "Multigate semiconductor device with vertical channel current and method of fabrication", J. M. Cleaves and V. Subramanian, US Patent 6580124
51. "Patterning three dimensional structures", C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleaves, and V. Subramanian, US Patent 6627530
52. "Low cost three-dimensional memory array", M. Johnson, T. Lee, V. Subramanian, P. Farnwald, J. Knall, US Patent 6515888
53. "Integrated circuit structure including three-dimensional memory array", M. Johnson, T. Lee, V. Subramanian, P. M. Farnwald, J. M. Cleaves, US Patent 6385074.
54. "FINFET transistor structures having double gate channel extending vertically from a substrate and methods of manufacture", C. Hu, T.-J. King, V. Subramanian, L. Chang, X. Huang, Y.-K. Choi, J. T. Kedzierski, N. Lindert, J. Bokor, W.-C. Lee, US Patent 6413802
55. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farnwald, and J. M. Cleaves, US Patent 6185122.
56. "Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farnwald, and J. M. Cleaves, US Patent 6034882.
57. "Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farnwald, and J. M. Cleaves, US Patent 6351406.
58. "Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farnwald, and J. M. Cleaves, US Patent 6483736.

Invited Magazine Articles, Books, Chapters, and Monographs

1. Chapter in "Inkjet Technology for Digital Fabrication", Editors: Ian M. Hutchings, Graham D. Martin, Wiley, ISBN: 978-0470681985
2. Chapter in "Applications of Organic and Printed Electronics: A Technology-Enabled Revolution (Integrated Circuits and Systems)", Editor: E. Cantatore, ISB: 978-1-461-43159-6
3. Chapter in "Inkjet-based Micromanufacturing", Editors: Korvink, Smith, Shin, Wiley, ISBN: 978-3-527-31904-6
4. Chapter in "Organic Electronics II. More Materials and Applications", Editor: H. Klauk, Wiley, ISBN: 978-3-527-32647-1
5. Chapter in "Transparent Electronics: From Synthesis to Applications", Editors: A. Facchetti and T. Marks, Wiley, ISBN: 978-0-470-99077-3, 2010.
6. Chapter in "The chemistry of inkjet inks", Editor: S. Magdassi, World Scientific Publishing Company, ISBN: 978-9812818218, 2009
7. Chapter in "Organic Field-Effect Transistors", Editors: Z. Bao, and J. Locklin, CRC Press, ISBN: 978-0849380808, 2007
8. "Developments in printed RFID", V. Subramanian, Pira Publishing, UK, 2006.
9. "3D Chips: Future Possibilities", V. Subramanian, Silicon India, Feb 2003, pp. 24-25

Invited Conference Presentations

1. *Invited*, "High-Speed, High-Resolution Printing of Inorganic Devices", Vivek Subramanian and William J. Scheideler, 2018 Fall Materials Research Society Meeting, Boston, MA, Nov 25-30, 2018.
2. *Invited*, "Materials, Process, and Device Innovations for High-Performance Printed Electronics", PRINSE'18 – The 5th Printed Intelligence Industry Seminar on Manufacturing Solutions for Customer Needs and Vision to the Future, Oulu, Finland, Jan 31-Feb 1, 2018.

3. *Invited*, "Highly scaled gravure printed organic transistors for high-performance printed organic electronics", High-frequency printed and direct-written organic-hybrid integrated circuits (HEROIC) Workshop, Milan, Italy, Nov 8-10, 2017.
4. *Keynote*, "Printed Electronics: Innovations in Materials, Processes, and Devices", Association of International Metallizers, Coaters, and Laminators (AIMCAL) R2R Conference USA 2017, Tampa, FL, Oct-15-18, 2017.
5. *Invited*, "High-performance gravure printed organic transistors", 2017 European Materials Research Society Meeting, Strasbourg, France, May 22-26, 2017
6. *Invited*, "Printed Electronics: Innovations in Materials, Processes, and Devices", 2017 International Thin Film Transistor Conference (ITC 2017), Austin, TX, February 23-24, 2017.
7. *Invited*, "High-speed Printing of Transistors: From Inks to Devices", 2016 International Society of Coating Science and Technology Symposium (ISCST), Pittsburgh, PA, September 18-21, 2016.
8. *Keynote*, "Printed Electronics: Innovations in Materials, Processes, and Devices", 2016 Canadian Printable Flexible Wearable electronics Symposium (CPES2016), April 19-20, Oakville, Canada
9. *Keynote*, "Printed Electronics: Innovations in Materials, Processes, and Device", 2016 Society of Vacuum Coaters Techcon, Indianapolis, IN, May 10-13, 2016.
10. *Invited*, Subramanian, Vivek, Chung, Seungjun, Grau, Gerd and Scheideler, William J., "71-2: Invited Paper: Printed Transistors and MEMS for Large-Area Electronics", 2016 Society for Information Display Symposium, San Francisco, May 20-27, 2016.
11. *Keynote*, "Printed Electronics: Innovations in Materials, Processes, and Devices", 31st Philippine Chemistry Congress, Iloilo, Philippines, April 13-15, 2016.
12. *Keynote*, "Advanced Processes, Materials, and Devices for Emerging Printed Electronics Applications", 3rd Swiss Conference on Printed Electronics and Functional Materials, Neuchatel, Switzerland, Oct 1-2, 2015.
13. *Invited*, "High-performance printed organic transistors: Materials, processes, and devices", V. Subramanian, G. Grau, H. Kang, and R. Kitsomboonloha, 2015 American Chemical Society National Meeting and Exposition, Boston, MA, Aug 17th, 2015.
14. *Invited*, Subramanian, Vivek, Jaewon Jang, William Scheideler, and Sarah Swisher, "39.1: Invited Paper: Printed Inorganic Transistors Based on Transparent Oxides." In SID Symposium Digest of Technical Papers, vol. 46, no. 1, pp. 587-590. 2015.
15. *Plenary*, "Printed Electronics: Advanced Technologies Enabling New Applications", 2015 Flexible and Printed Electronics Conference, Monterey, CA, February 23-26, 2015.
16. *Invited*, "High-resolution gravure printing of organic thin film transistors for high-performance printed electronic systems", V. Subramanian, R. Kitsomboonloha, J. Cen, H. Kang, G. Grau, and W. J. Scheideler, Materials Research Society Fall Meeting, Boston, MA, Dec 3, 2014.
17. *Invited*, "Advanced printed electronics technologies for novel ubiquitous human interactive systems", 2014 CMOS Emerging Technologies Research Symposium, Grenoble, France, July 6-8, 2014.
18. *Invited*, "Printed Electronics: A pathway to functionally-rich systems", 64th annual IEEE Electronic Components and Technology Conference, Orlando, FL, May 27, 2014.
19. *Invited*, "Printed Electronics: The Confluence of Printing and Semiconductors", Canadian Printed Electronics Symposium, Montreal, Canada, April 9, 2013.
20. *Invited*, "Modeling, scaling, and integration of gravure printing for fast switching Organic FETs", V. Subramanian, S. J. S. Morris, H. Kang, Materials Research Society Fall 2012 Meeting, Boston, MA, Nov 25-30, 2012
21. *Invited*, "Printed Nanoparticles as routes to high-performance printed conductors: Synthesis, Printing Processes, and Device Applications", V. Subramanian, H. Kang, R. Kitsomboonloha, and S. K. Volkman, The 2012 International Conference on Flexible and Printed Electronics ICFPE2012, Tokyo, Japan, September 6th - 8th, 2012
22. *Invited*, "Advanced Printing Processes for High-Performance Printed Transistors", V. Subramanian, Flextech Workshop on Printing Electronics - Ink and Substrate Interactions, Kalamazoo, MI, August 1-2, 2012
23. *Invited*, "High-performance Printed Transistors: Materials, Processes, and Devices", V. Subramanian, 2nd CPEM International Symposium "Organic Semiconductors and Printed Electronics", Gyeonggi, South Korea, May 10th, 2012.

24. *Invited* “Highly-Scaled Gravure and Inkjet Printed Organic Transistors: Tools, Processes, and Devices”, Hongki Kang & Vivek Subramanian, 2012 Flextech Flexible Electronics and Display Conference, Phoenix, AZ, Feb 5-9, 2012.
25. *Plenary* “Nanomaterials for printed electronics: synthesis, design, and applications”, V. Subramanian, International Conference on Nano Science and Nano Technology, Sunchon, Korea, November 11th, 2011.
26. *Invited* “Advances in scaling of printed transistors”, V. Subramanian, International Seminar on Printed Electronics, Seoul, Korea, June 8th, 2011.
27. *Invited* “High-Performance Fully Printed Transistors: Materials, Processes, and Device Characteristics”, V. Subramanian, H. Tseng, R. Kitsomboonloha, and A. de la Fuente Vornbrock, 2011 Electrochemical Society Meeting, Montreal, Canada, May 2011
28. *Invited* “From Droplets to Devices: Printed Transistor Processes, Integration, and Characteristics”, Vivek Subramanian, Daniel Soltman, Huai-Yuan Tseng, Rungrot Kitsomboonloha and Alejandro de la Fuente Vornbrock, Materials Research Society Spring Meeting, San Francisco, CA, April 2011
29. *Keynote* “Printed electronics: Innovations in tools, materials, devices, and applications”, V. Subramanian, 2011 Korea Printed Electronics Association (KoPeA) meeting, Seoul, Korea, March 2011
30. *Keynote* “Printed RF tags and sensors: the confluence of printing and semiconductors”, V. Subramanian, F. Liao, and H-Y. Tseng, The European Microwave Integrated Circuits Conference 2010, Paris, France, September 2010.
31. *Invited* “Droplet-on-demand direct patterning of active materials: materials, modeling, and integration”, V. Subramanian, The 2010 IEEE Lithography Workshop, Kuai, Hawaii, November 2010
32. *Plenary* “Printed electronics: where are we, and where are we going”, V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.
33. *Keynote* “Printed RFID: Technology Trends and Outlook”, V. Subramanian, IEEE International Conference on RFID 2010, Orlando, Florida, April 2010.
34. *Invited* “Mechanistic studies on sintering of nanoparticles for formation of solution-processed thin films”, 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.
35. *Invited* “Printed Electronics: the confluence of printing and semiconductors”, Vivek Subramanian, 2009 International Conference on Flexible and Printing Electronics, Jeju Island, Korea, Nov 2009.
36. *Invited* “Organic Transistor Vapor and Biosensors – Technology Status and Implementation Issues”, Vivek Subramanian, Frank Liao, Lakshmi Jagannathan, Electrochemical Society Meeting, Vienna, Austria, October 2009.
37. *Invited* “Printed transistors for low-cost electronics: the confluence of printing and printable electronic materials”, Vivek Subramanian, Alejandro de la Fuente Vornbrock, Steven Moles, Daniel Soltman, Huai-Yuan Tseng, and Steven K. Volkman, SPIE Optics + Photonics, August 2-6, 2009, San Diego, CA
38. *Invited* “Printed Zinc Oxide Based Electronics: Materials, Devices, and Outlook”, V. Subramanian, S. K. Volkman, and D. R. Redinger, LOPE-C, June 23-25, 2009, Frankfurt, Germany
39. *Invited* “Printed Devices for Low-Cost Electronics: Technology Status and Outlook”, V. Subramanian, PETEC Inaugural Event, March 17, 2009, Durham, United Kingdom
40. *invited* “Printed Electronic Tags and Sensors for Smart Packaging Applications”, Vivek Subramanian, Josephine Chang, Lakshmi Jagannathan, Frank Liao, Steve Moles, David Redinger, Daniel Soltman, Huai-Yuan Tseng, Steve Volkman, Shong Yin, 2009 Flexible Electronics and Display Conference, Phoenix, AZ, Feb 2-5, 2009.
41. *invited* “Electronic Nose Sensors for Consumer Packaging”, V. Subramanian, IDTechEx Printed Electronics USA, San Jose, CA, Dec 2-5, 2008.
42. *invited* “Solution-Processed Transparent Transistors for Low-Cost, Flexible Displays”, V. Subramanian, S. K. Volkman, and D. R. Redinger, LEOS 2008: The 21st Annual Meeting of the IEEE Lasers and Electro-Optics Society, Newport Beach, CA, 9-13 November, 2008.
43. *invited* “Organic chemical and biosensors for smart packages”, V. Subramanian, IDTechEx Printed Electronics Asia, Tokyo, Japan, Oct 8-9, 2008.
44. *invited* “Printed Electronics for Low-Cost Tags, Displays, and Sensors”, V. Subramanian, 1st International Conference on R2R Printed Electronics, Seoul, Korea, April 30-May 2, 2008.

45. *invited* "Printed organic RFID tags: technology, roadmaps, and challenges", V. Subramanian, 1st Plastic Electronics Asia Conference and Showcase, Seoul, Korea, June 24-26, 2008
46. *invited* "Power supply considerations and solutions for printed electronic tags and sensors", V. Subramanian, IDTechEx Printed Electronics Europe, Dresden, Germany, April 8-9, 2008
47. *invited* "Printed Chemical and Biosensors: Technology, Design and Challenges", GOSPEL Workshop on Plastic Chemical Sensors, Dresden, Germany, April 9, 2008
48. *Plenary* "Printed Electronics For Low-Cost Electronic Systems: Technology Status and Application Development", Vivek Subramanian, Josephine B. Chang, Alejandro de la Fuente Vornbrock, Daniel C. Huang, Lakshmi Jagannathan, Frank Liao, Brian Mattis, Steven Moles, David R. Redinger, Daniel Soltman, Steven K. Volkman, Qintao Zhang, 38th European Solid State Device Research Conference, Edinburgh, Scotland, September 15-19, 2008
49. *invited* "Printed Organic Transistors for Low-cost Tags, Displays, and Sensors: Technology, Modeling and Challenges", Vivek Subramanian, Alejandro de la Fuente Vornbrock, Huai-Yuan Tseng and Shong Yin, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008.
50. *invited* "Printed Electronics for Low-Cost Tags and Sensors", Vivek Subramanian, Sixth Annual Workshop on Microelectronics and Electron Devices, April 18, 2008.
51. *invited* "Printed organic RF tags, chemical sensors and biosensors", Vivek Subramanian, International Symposium for Flexible Electronics and Display, Hsinchu, Taiwan, Nov 18, 2007.
52. *invited* "Printed Tags and Sensors for RFID: Opportunities and Challenges", Vivek Subramanian, Printed Electronics USA 2007, San Francisco, CA, Nov 14, 2007.
53. *invited* "Printed RFID Tags: Materials, Processes, and Devices", Vivek Subramanian, Daniel Soltman, Daniel Huang, Steven Moles, 2007 AiChE Annual Meeting, Salt Lake City, UT, Nov. 8, 2007.
54. *invited* "Printed organic RFID tags: technology, roadmaps, and challenges", Vivek Subramanian, 3rd Global Plastic Electronics Conference and Showcase, Frankfurt, Germany, Oct 30, 2007.
55. *invited* "Printed organic transistors: technology, characteristics, and modeling", Vivek Subramanian, Alejandro de la Fuente Vornbrock, Daniel Soltman, Huai-Yuan Tseng, and Steve Moles, 212th meeting of the Electrochemical Society, Washington, DC, Oct 8, 2007.
56. *invited* "Printed electronic tags and sensors - device, materials, and circuit issues", Vivek Subramanian, 2007 Organic Electronics Conference and Exhibition, Frankfurt, Germany, Sept 25, 2007.
57. *invited* "Inkjet printing of transistors, diodes, and passive components for smart tags", Vivek Subramanian, Innovations in Inkjet: 3rd DPI Inkjet Workshop, Eindhoven Institute of Technology, Netherlands, June 28-29, 2007.
58. *invited* "Printed organic transistors", A. de la Fuente and V. Subramanian, Industry Forum on Printed Electronics, Chicago, IL, April 23-24, 2007
59. *invited* "From Materials to Circuits: Implications of printed materials on printed RFID", V. Subramanian, 2007 Pira printed RFID conference, Frankfurt, Germany, June 4-6, 2007.
60. *keynote* "Droplet on demand lithography: An enabling technology for low-cost electronics", V. Subramanian, A. de la Fuente Vornbrock, S. Moles, D. Redinger, Q. Zhang, and S. K. Volkman, SPIE Advanced lithography, 27th February, 2007
61. *invited* "Printed RFID tags: performance needs and technology trends", V. Subramanian, 2007 IDTechEx Smart labels USA, Boston, MA, February 20-23, 2007.
62. *keynote* "Printed Organic Transistors for low-cost tagging and sensing applications", V. Subramanian, J. Chang, A. de la Fuente Vornbrock, S. Moles, D. Soltman, and Q. Zhang. 6th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, Tokyo, January 15th-18th, 2007.
63. *invited* "Nano Inks for Printed RFID", V. Subramanian, Pira Nanoscale Inks and Pigment Technologies Conference, Chicago, IL, Sept 27-28, 2006.
64. *invited* "Toward Printed RFID: Materials, Processes, and Devices", V. Subramanian, 5th Annual Printed Electronics and Displays Conference and Trade Fair, Las Vegas, Oct 11-13, 2006.
65. *invited* "Inkjetted Organic Transistors for Smart Tagging Applications", Vivek Subramanian, Jean M. J. Frechet, Steven Moles, Josephine Chang, Amanda R. Murphy, Alejandro de la Fuente Vornbrock, Steven Volkman, 2006 AiChE Annual Meeting, Nov 17th, 2006

66. *invited focal paper* "All-printed electronics: Materials, Devices, and Circuit Implications", V. Subramanian, J. Chang, S. Molesa, D. Redinger, and S. Volkman, Digital Fabrication 2006, Denver, CO, Sept 17-22, 2006.
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2. Carlos Biao, Matt McPhail, Vivek Subramanian and Oscar Dubon, "Comprehensive Multifactorial Studies on the Degradation of Perovskite Solar Cells in Operation", 2019 Spring Materials Research Society Meeting, Phoenix, AZ, April 22-26, 2019.
3. Rajan Kumar, Jessica E. Nichols, Bryan D. McCloskey, and Vivek Subramanian, "Low-Temperature-Processing of Printed Cathodes for Aqueous Metal-Air Batteries", ECS AiMES 2018 Meeting, September 30, 2018 - October 4, 2018, Cancun, Mexico
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8. "Improving high-speed nanomaterial printing with sub-process-decoupled gravure printer design", W. Scheideler, V. Subramanian, ASME 2017 Conference on Smart Materials, Adaptive Structures, and Intelligent Systems, Snowbird, UT, Sept 18-20, 2017
9. "Development of a printed cathode and catalyst layer for printed zinc-air batteries, R. Kumar, N. Williams, and V. Subramanian, 232nd ECS Meeting, National Harbor, MD, Oct 1-5, 2017.
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38. "Experimental study of the residue film in direct gravure printing of electronics", Rungrot Kitsomboonloha, Umut Ceyhan, SJS Morris, Vivek Subramanian, 65th Annual Meeting of the APS Division of Fluid Dynamics, Volume 57, Number 17, San Diego, California, November 18–20, 2012
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