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Lochtefeld

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(54) **SEMICONDUCTOR DIODES FABRICATED BY ASPECT RATIO TRAPPING WITH COALESCED FILMS**

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(52) **U.S. Cl.** **257/103**; 257/86; 257/94; 257/431; 257/461

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See application file for complete search history.

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(57) **ABSTRACT**

A photonic device comprises a substrate and a dielectric material including two or more openings that expose a portion of the substrate, the two or more openings each having an aspect ratio of at least 1. A bottom diode material comprising a compound semiconductor material that is lattice mismatched to the substrate occupies the two or more openings and is coalesced above the two or more openings to form the bottom diode region. The device further includes a top diode material and an active diode region between the top and bottom diode materials.

20 Claims, 20 Drawing Sheets

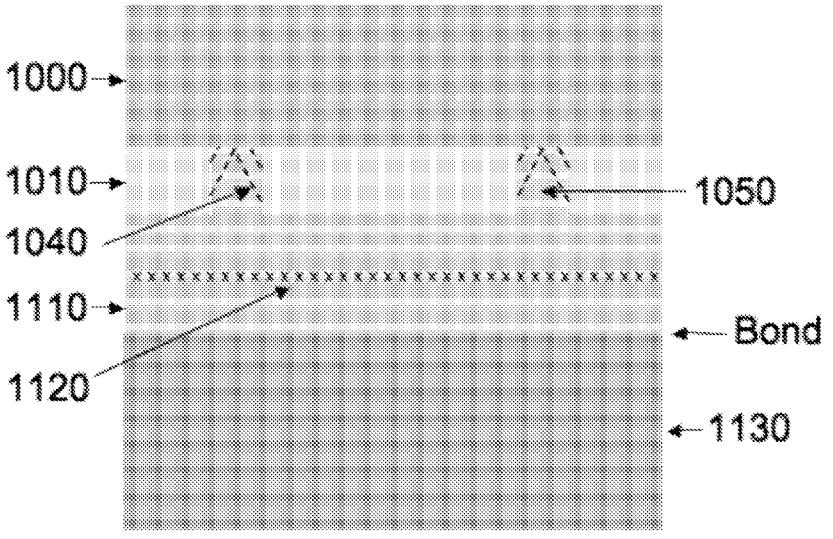

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FIGURE 1

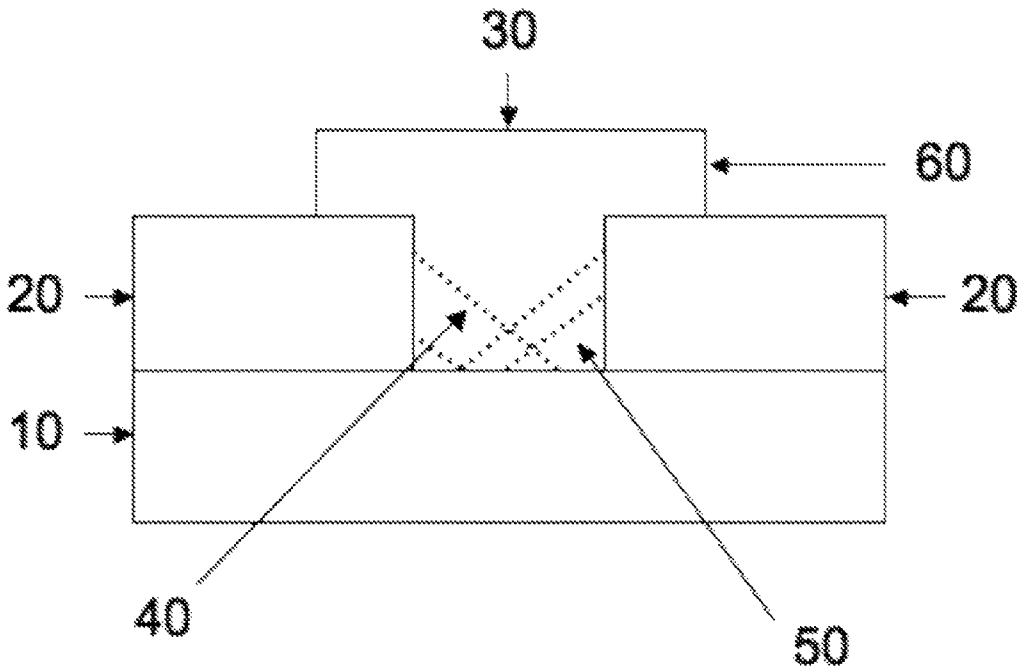


FIGURE 2

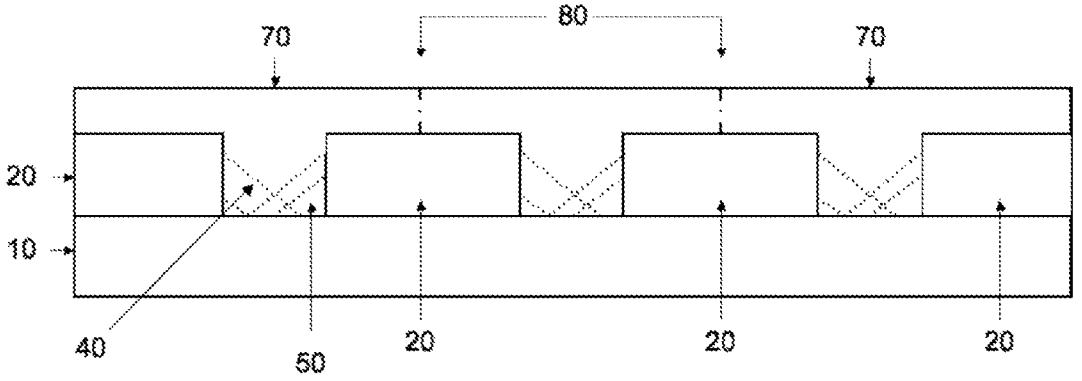


FIGURE 3

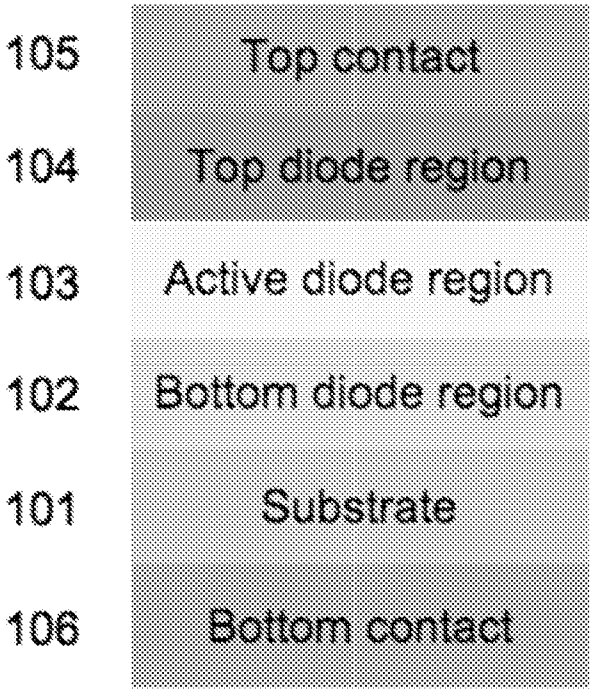


FIGURE 4

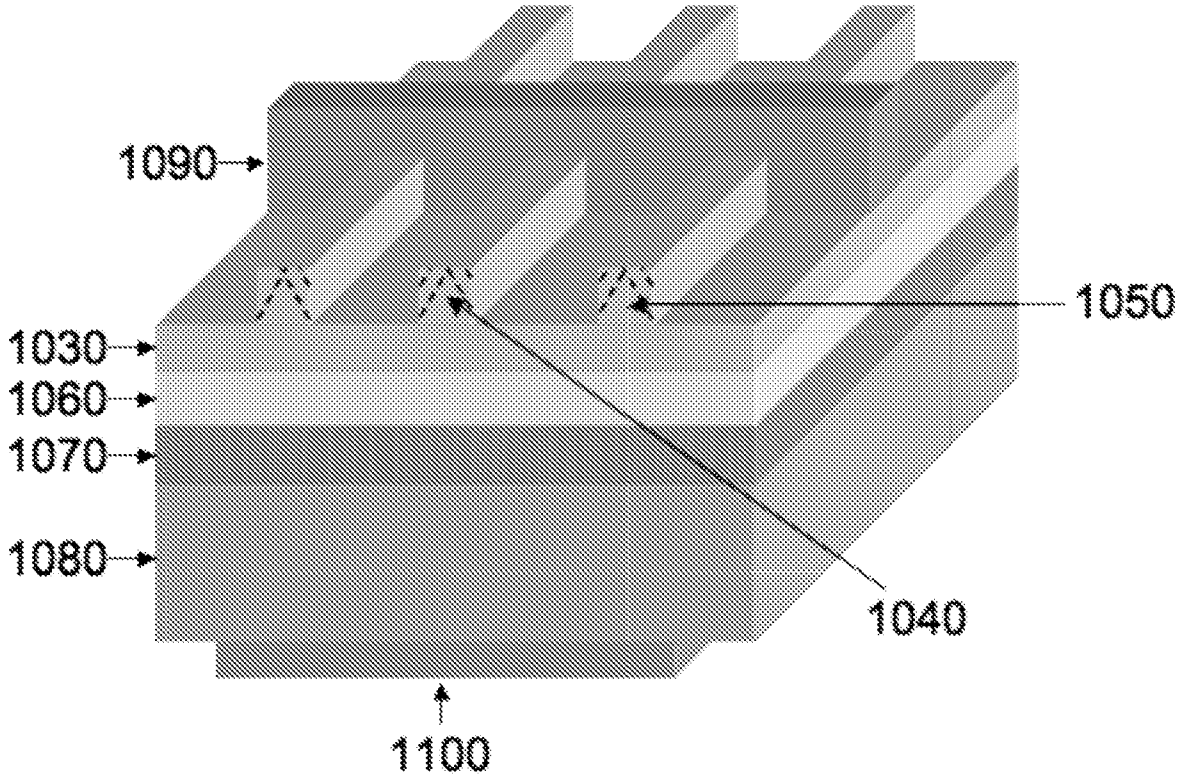


FIGURE 5

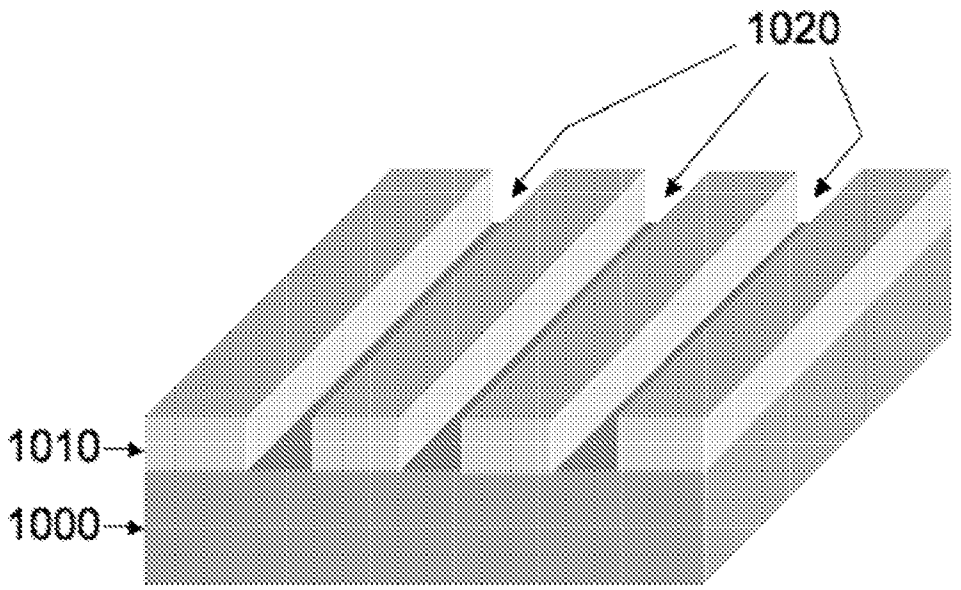


FIGURE 6

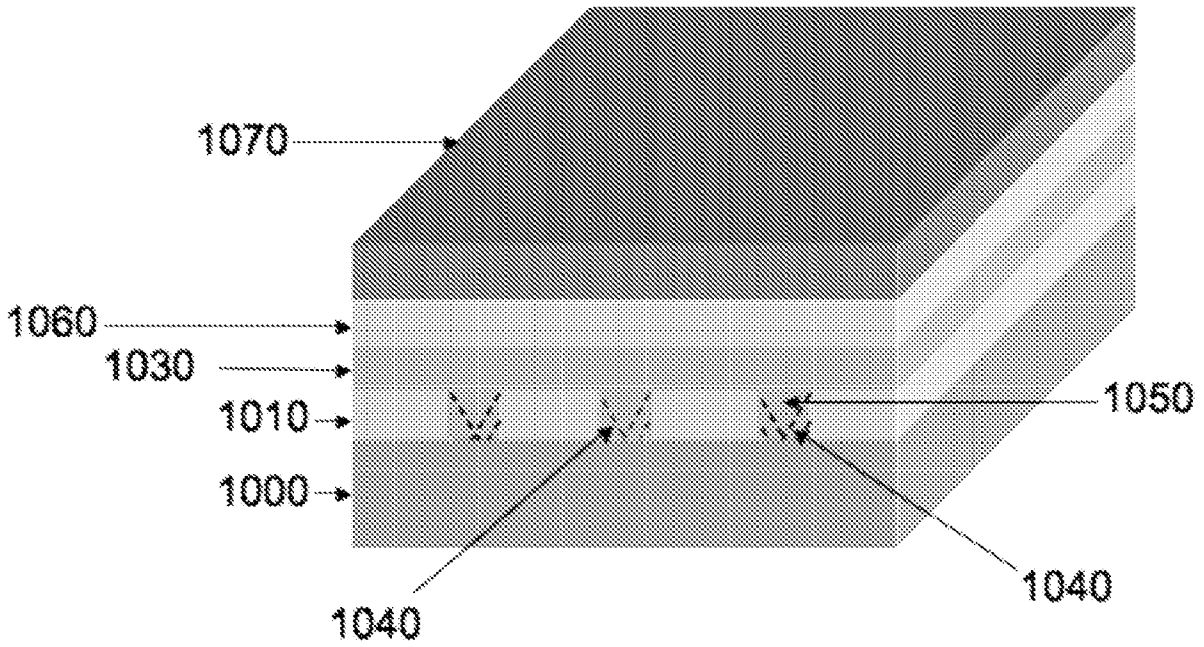


FIGURE 7

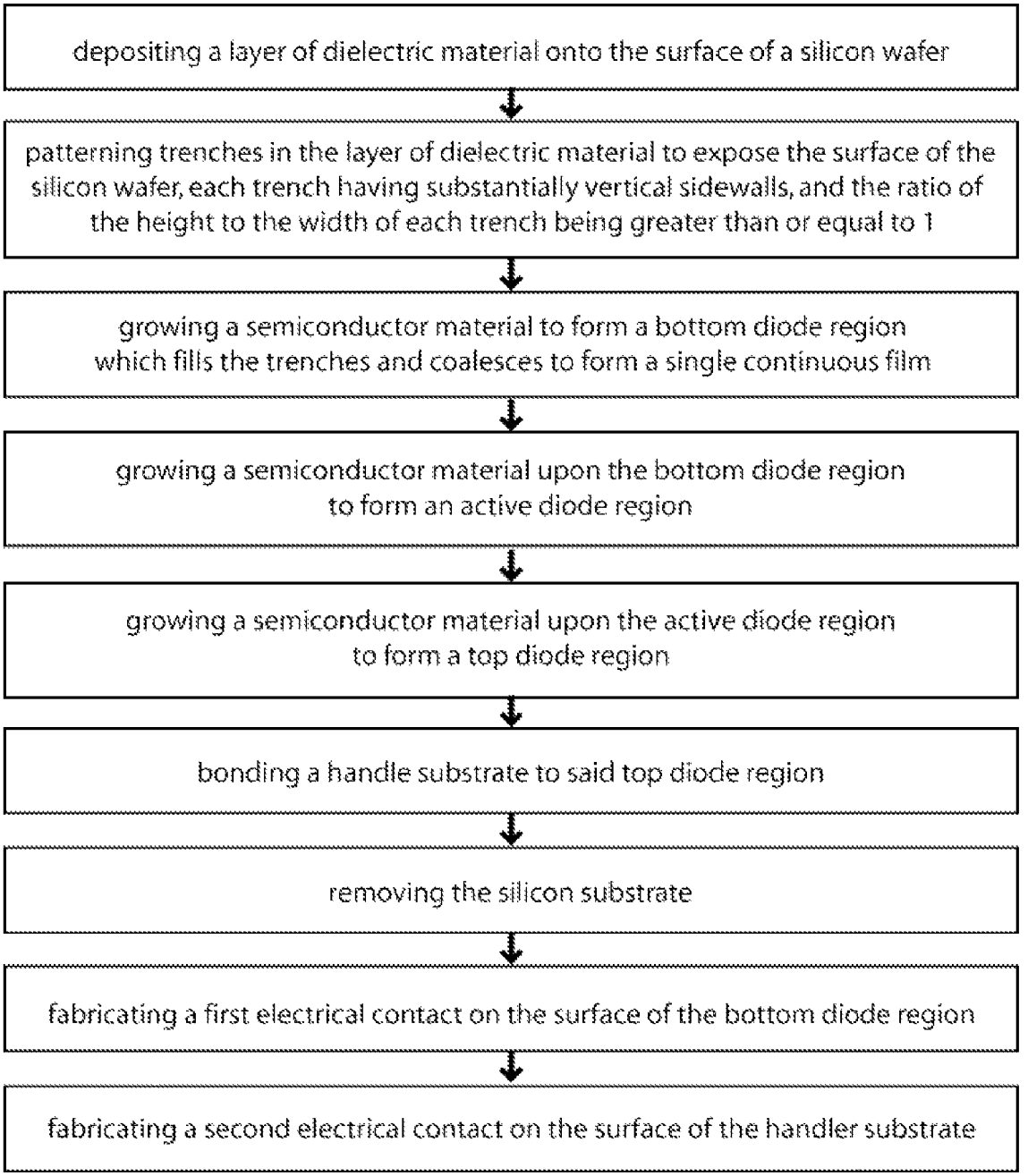

depositing a layer of dielectric material onto the surface of a silicon wafer
patterning trenches in the layer of dielectric material to expose the surface of the silicon wafer, each trench having substantially vertical sidewalls, and the ratio of the height to the width of each trench being greater than or equal to 1
growing a semiconductor material to form a bottom diode region which fills the trenches and coalesces to form a single continuous film
growing a semiconductor material upon the bottom diode region to form an active diode region
growing a semiconductor material upon the active diode region to form a top diode region
bonding a handle substrate to said top diode region
removing the silicon substrate
fabricating a first electrical contact on the surface of the bottom diode region
fabricating a second electrical contact on the surface of the handler substrate

FIGURE 8

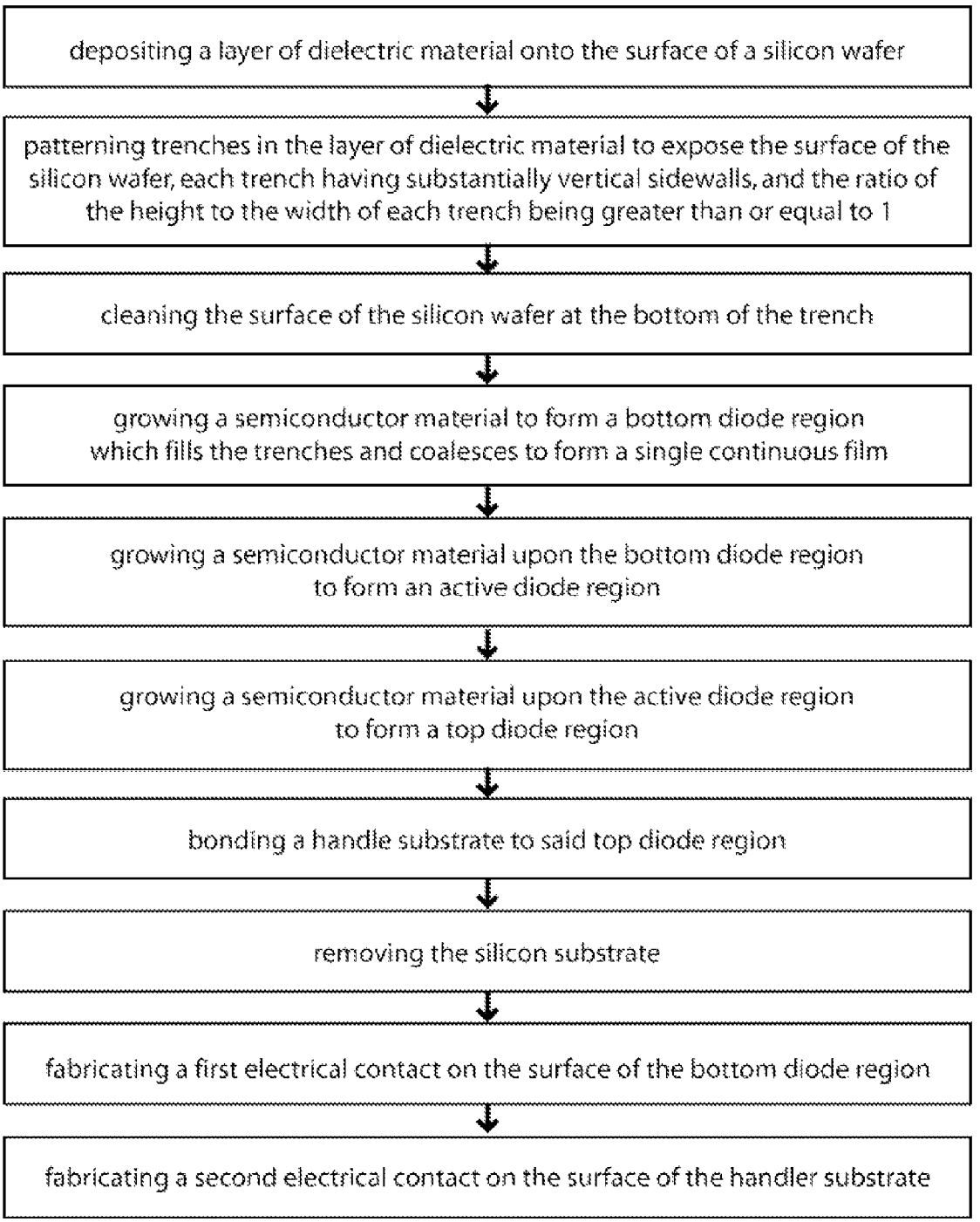

depositing a layer of dielectric material onto the surface of a silicon wafer
patterning trenches in the layer of dielectric material to expose the surface of the silicon wafer, each trench having substantially vertical sidewalls, and the ratio of the height to the width of each trench being greater than or equal to 1
cleaning the surface of the silicon wafer at the bottom of the trench
growing a semiconductor material to form a bottom diode region which fills the trenches and coalesces to form a single continuous film
growing a semiconductor material upon the bottom diode region to form an active diode region
growing a semiconductor material upon the active diode region to form a top diode region
bonding a handle substrate to said top diode region
removing the silicon substrate
fabricating a first electrical contact on the surface of the bottom diode region
fabricating a second electrical contact on the surface of the handler substrate

FIGURE 9

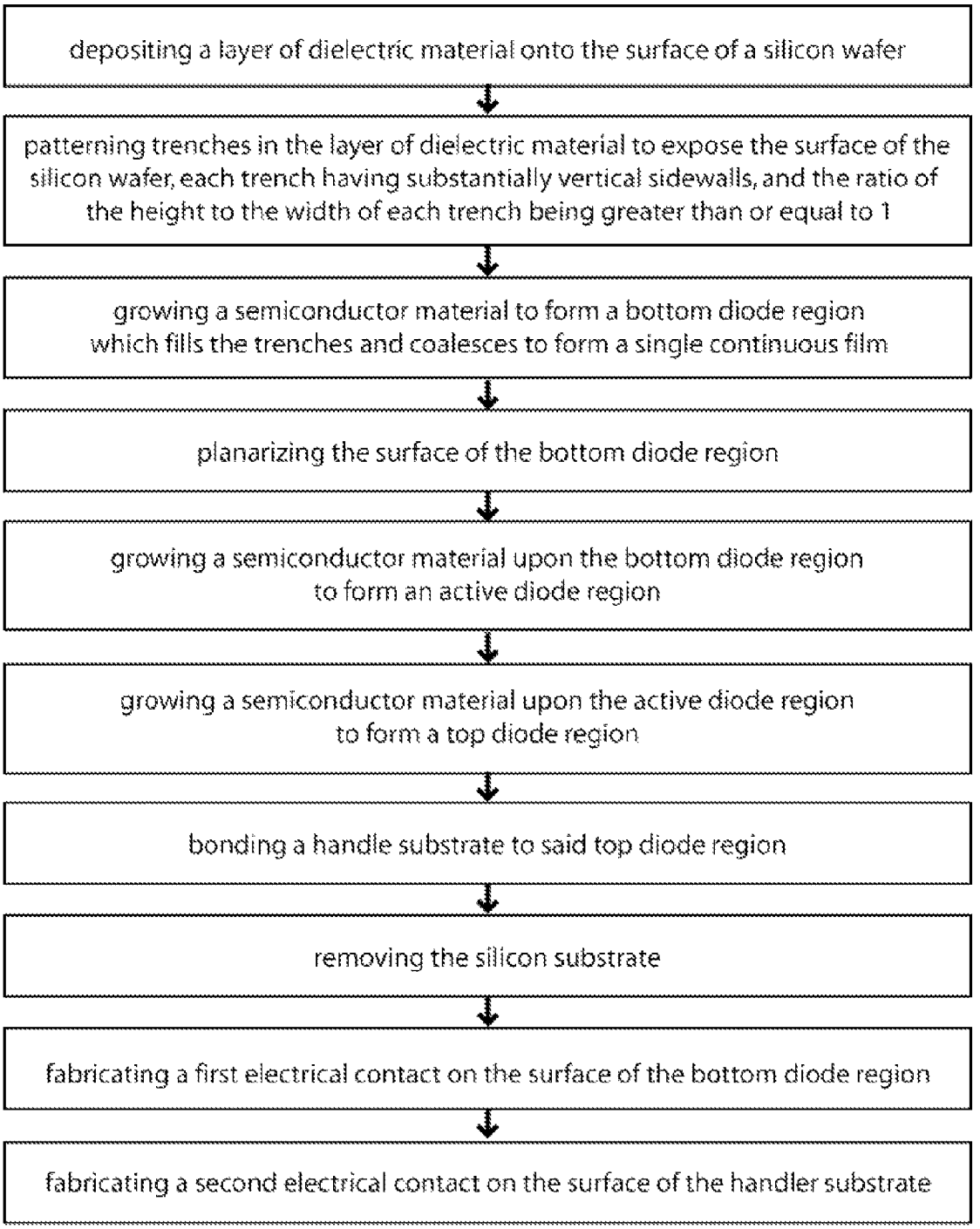

depositing a layer of dielectric material onto the surface of a silicon wafer
patterning trenches in the layer of dielectric material to expose the surface of the silicon wafer, each trench having substantially vertical sidewalls, and the ratio of the height to the width of each trench being greater than or equal to 1
growing a semiconductor material to form a bottom diode region which fills the trenches and coalesces to form a single continuous film
planarizing the surface of the bottom diode region
growing a semiconductor material upon the bottom diode region to form an active diode region
growing a semiconductor material upon the active diode region to form a top diode region
bonding a handle substrate to said top diode region
removing the silicon substrate
fabricating a first electrical contact on the surface of the bottom diode region
fabricating a second electrical contact on the surface of the handler substrate

FIGURE 10

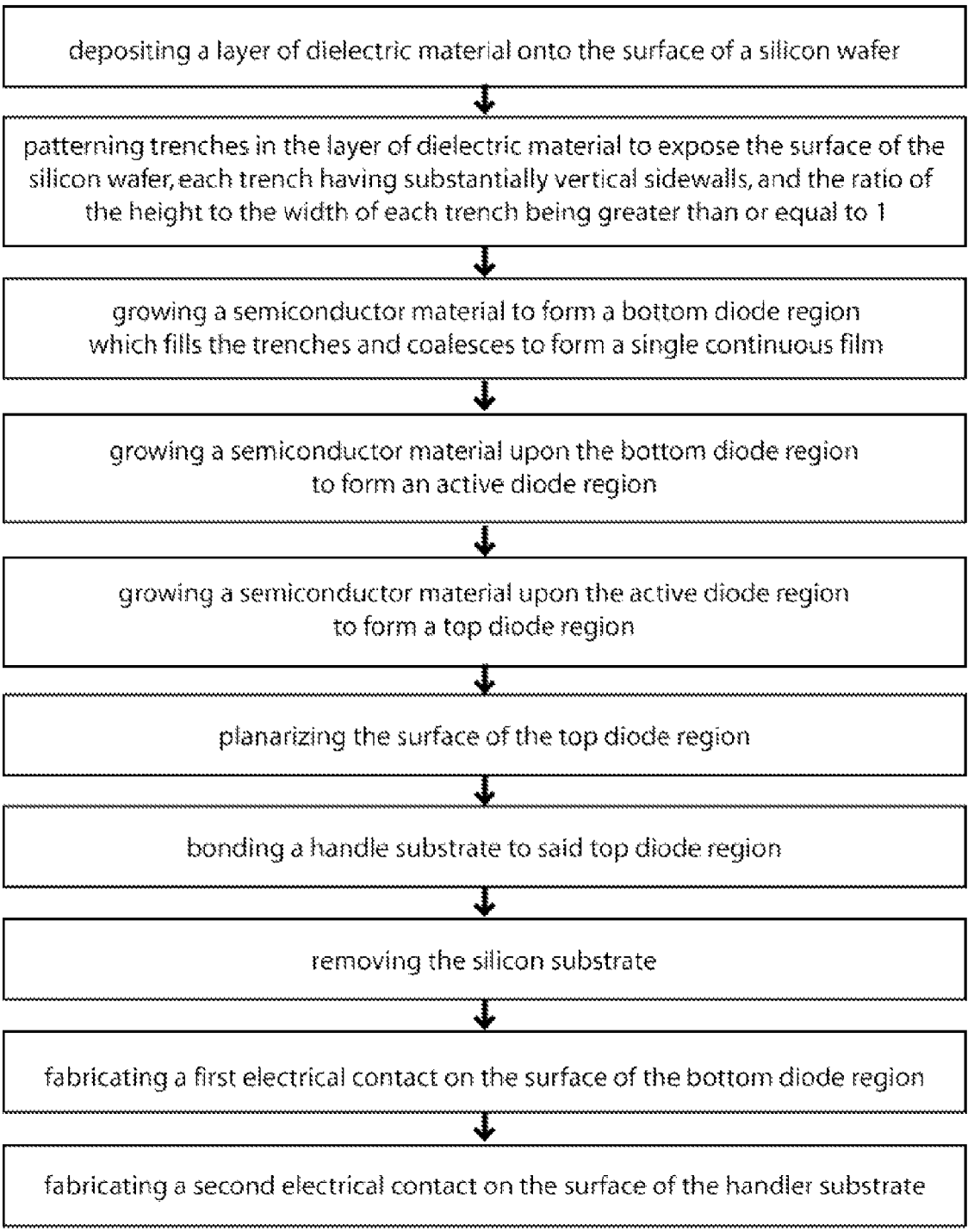

depositing a layer of dielectric material onto the surface of a silicon wafer
patterning trenches in the layer of dielectric material to expose the surface of the silicon wafer, each trench having substantially vertical sidewalls, and the ratio of the height to the width of each trench being greater than or equal to 1
growing a semiconductor material to form a bottom diode region which fills the trenches and coalesces to form a single continuous film
growing a semiconductor material upon the bottom diode region to form an active diode region
growing a semiconductor material upon the active diode region to form a top diode region
planarizing the surface of the top diode region
bonding a handle substrate to said top diode region
removing the silicon substrate
fabricating a first electrical contact on the surface of the bottom diode region
fabricating a second electrical contact on the surface of the handler substrate

FIGURE 11

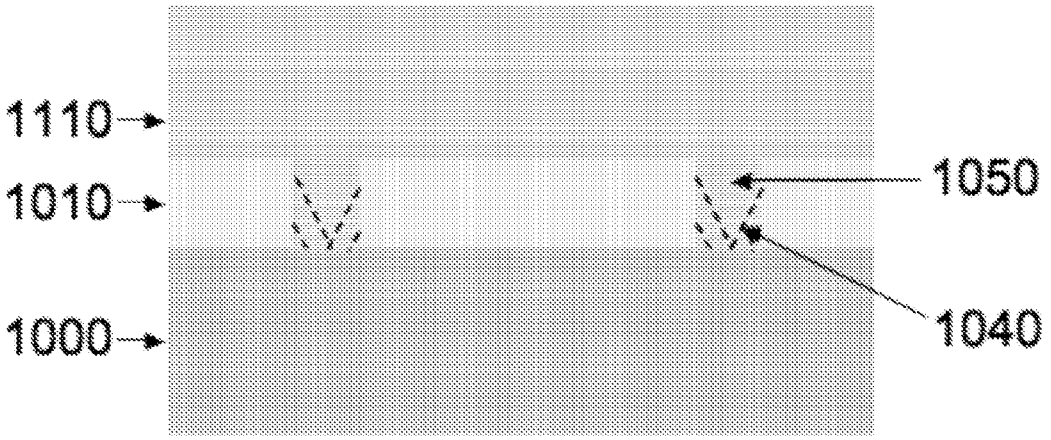


FIGURE 12

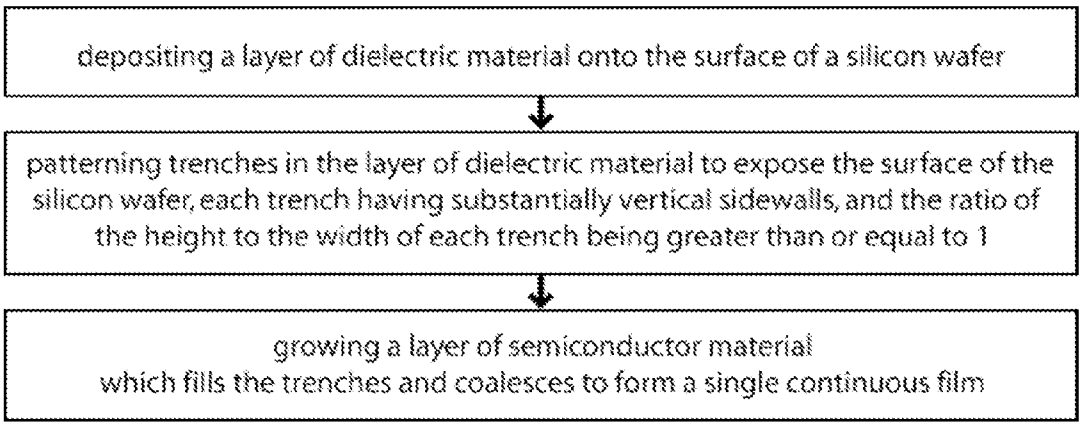


FIGURE 13

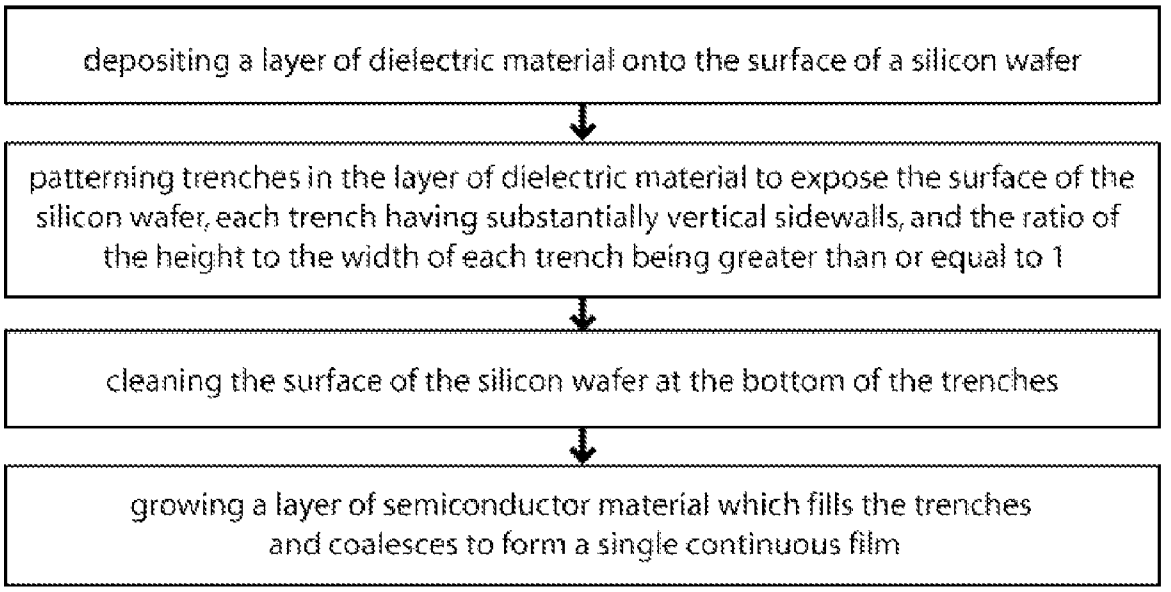


FIGURE 14

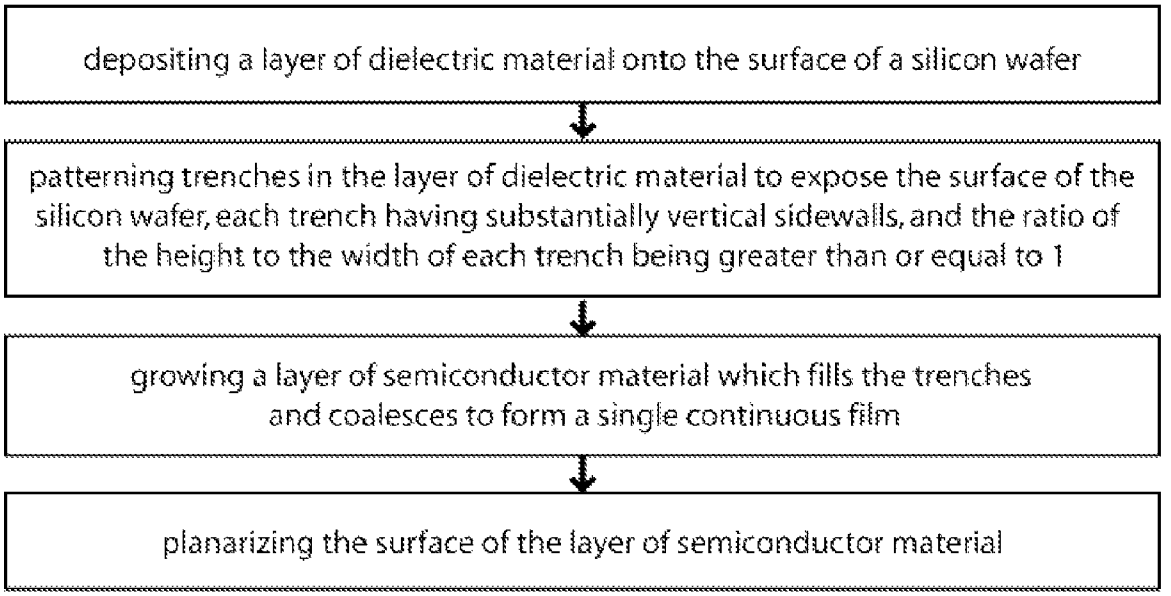


FIGURE 15

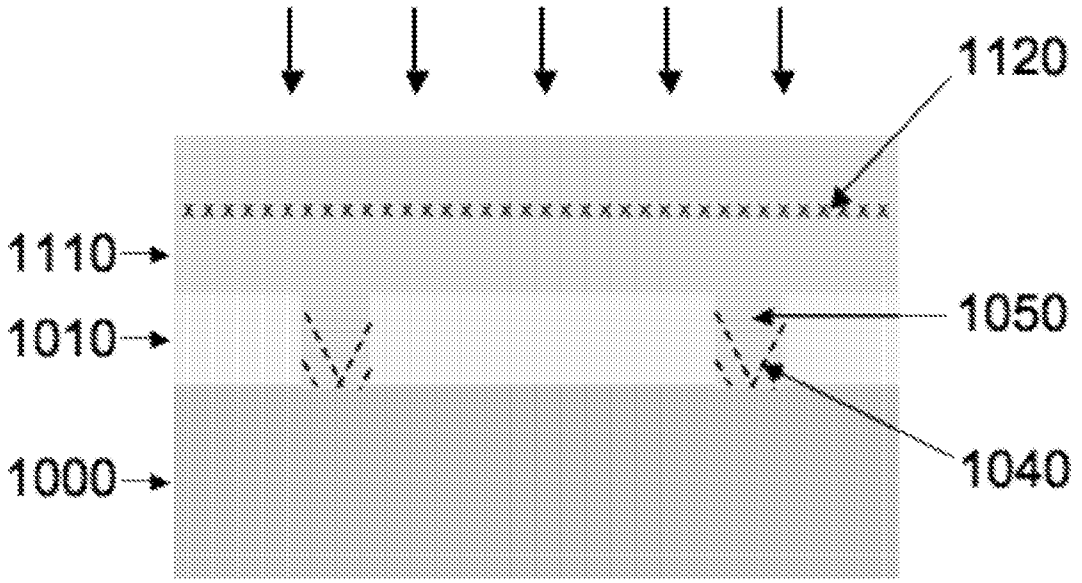


FIGURE 16

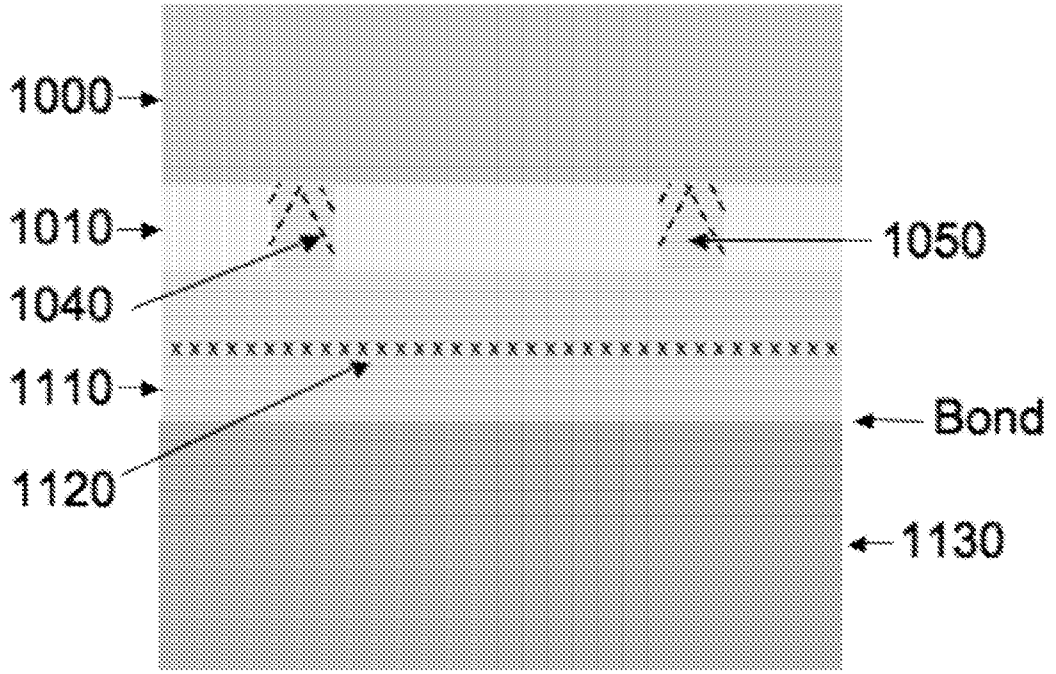


FIGURE 17

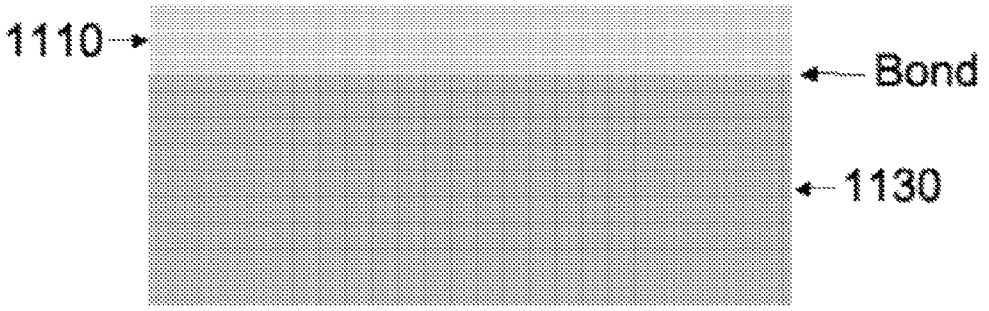


FIGURE 18

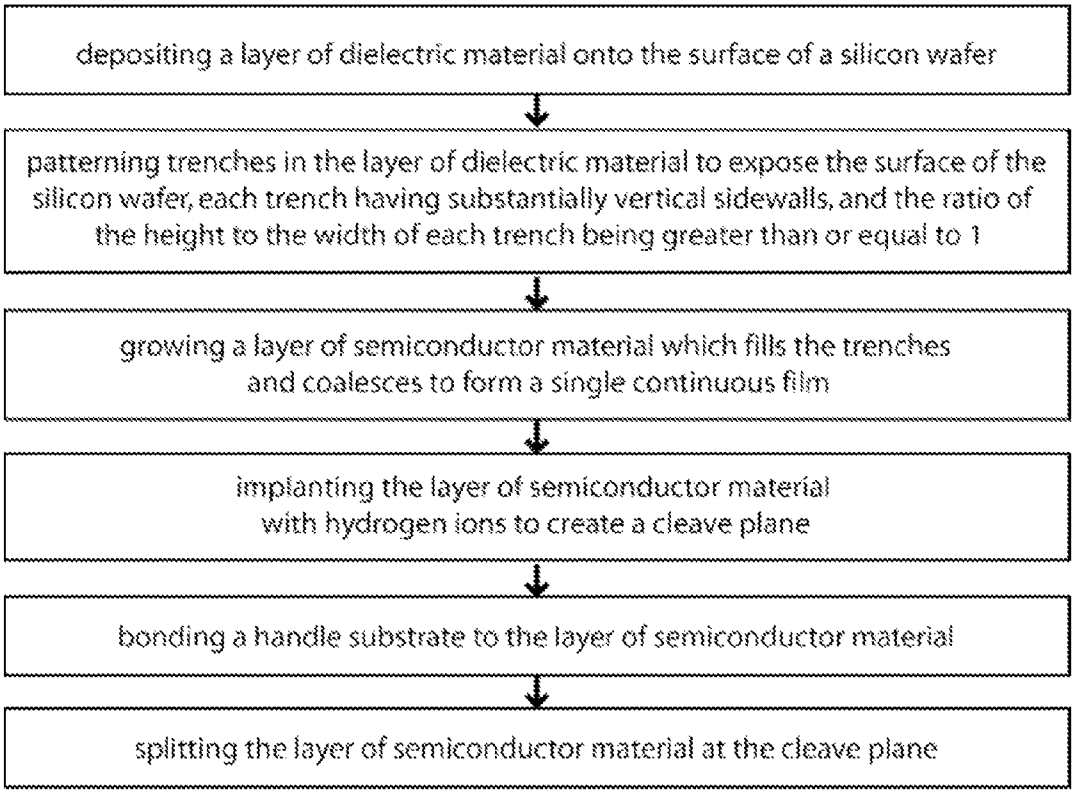


FIGURE 19

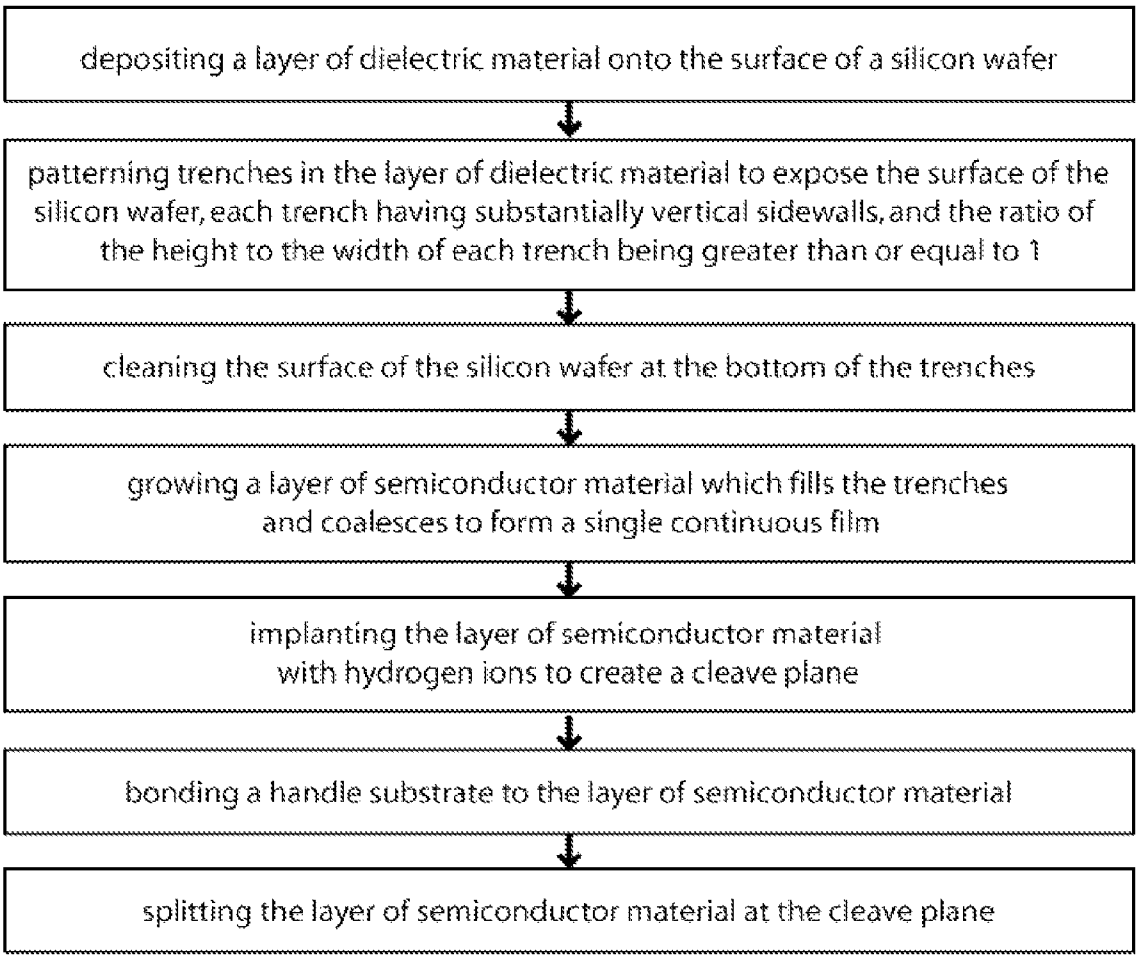

depositing a layer of dielectric material onto the surface of a silicon wafer
patterning trenches in the layer of dielectric material to expose the surface of the silicon wafer, each trench having substantially vertical sidewalls, and the ratio of the height to the width of each trench being greater than or equal to 1
cleaning the surface of the silicon wafer at the bottom of the trenches
growing a layer of semiconductor material which fills the trenches and coalesces to form a single continuous film
implanting the layer of semiconductor material with hydrogen ions to create a cleave plane
bonding a handle substrate to the layer of semiconductor material
splitting the layer of semiconductor material at the cleave plane

FIGURE 20

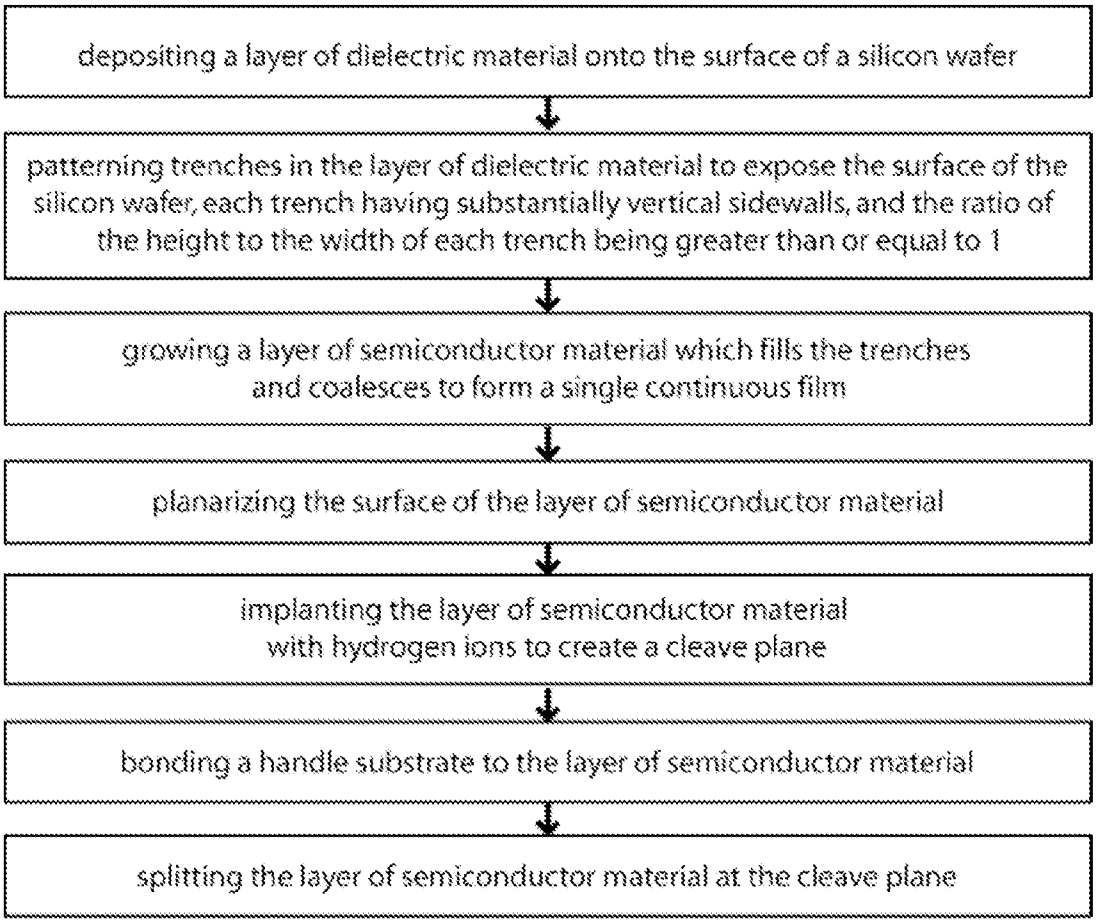


FIGURE 21

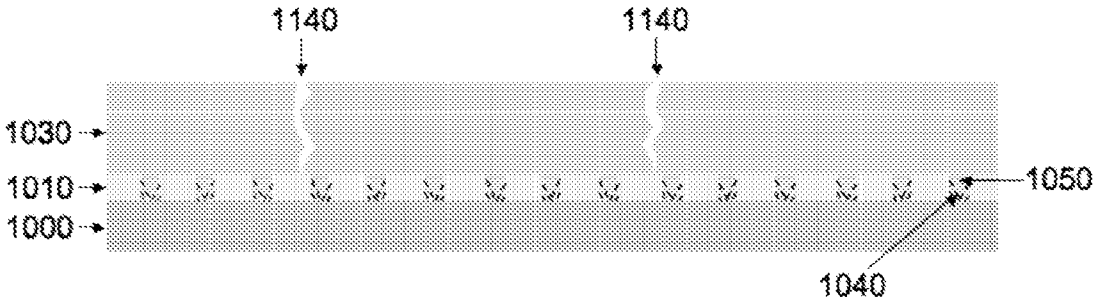


FIGURE 22

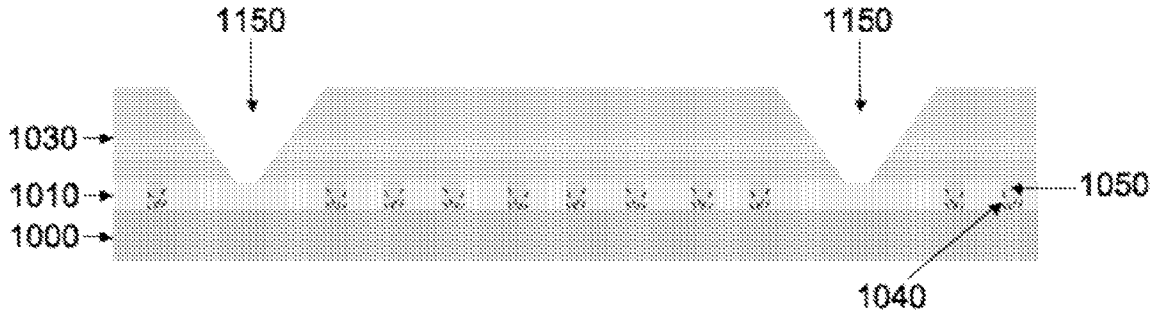


FIGURE 23

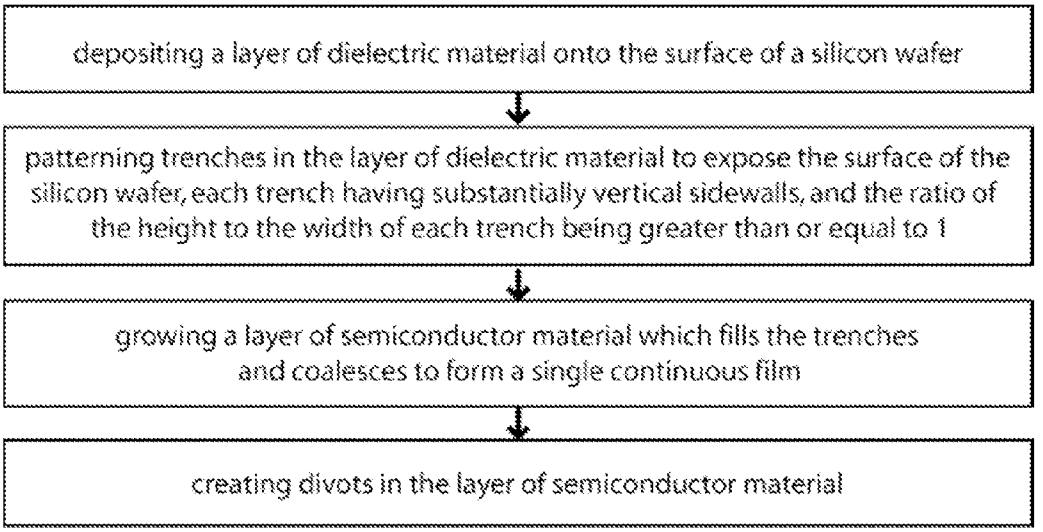


FIGURE 23A

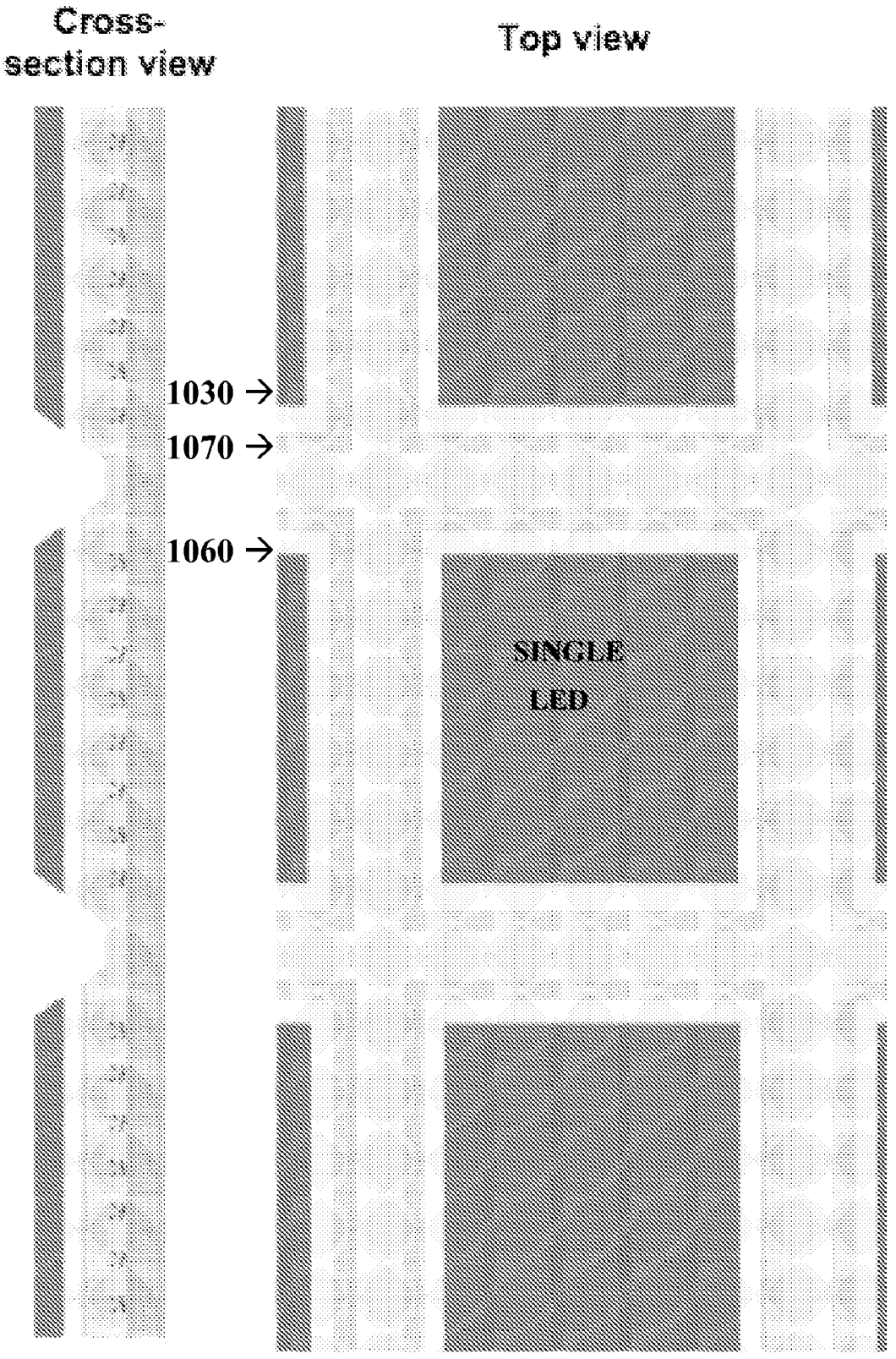


FIGURE 23B

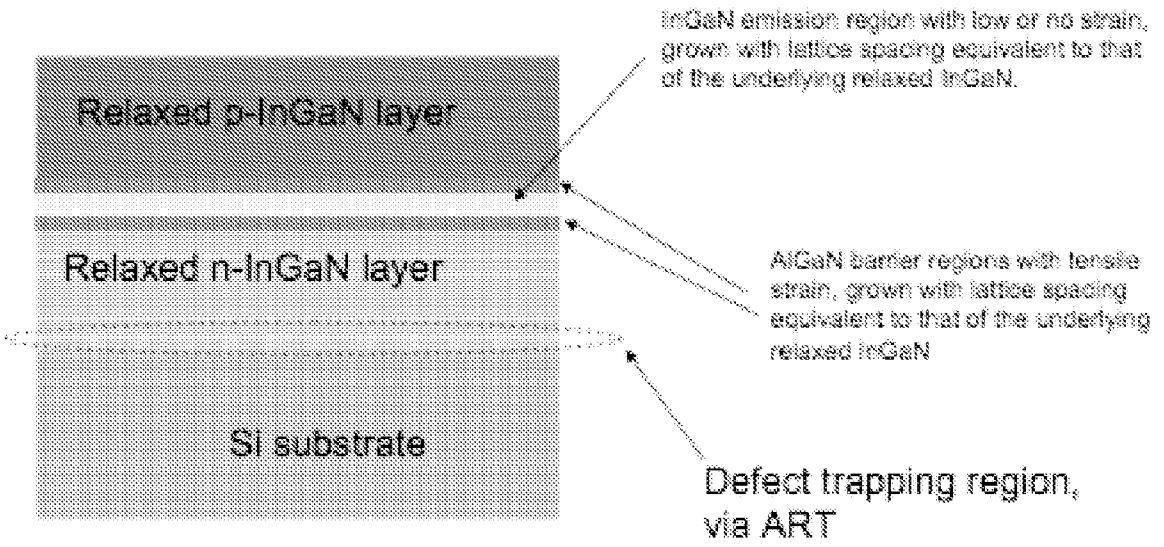

InGaN emission region with low or no strain, grown with lattice spacing equivalent to that of the underlying relaxed InGaN.
Relaxed p-InGaN layer
Relaxed n-InGaN layer
AlGaN barrier regions with tensile strain, grown with lattice spacing equivalent to that of the underlying relaxed InGaN
Si substrate
Defect trapping region, via ART

FIGURE 24

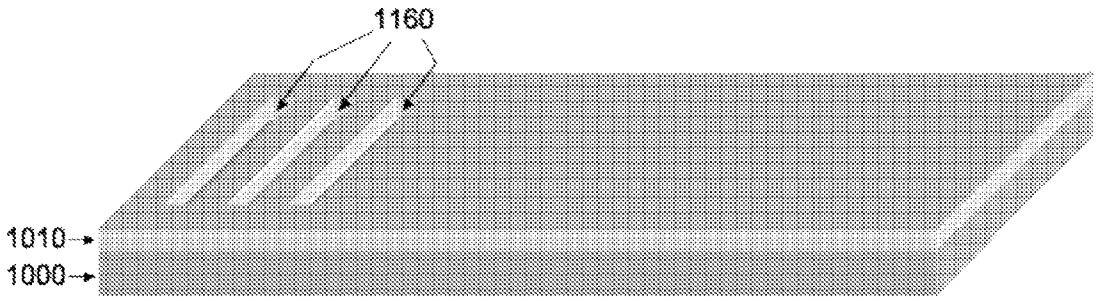


FIGURE 25

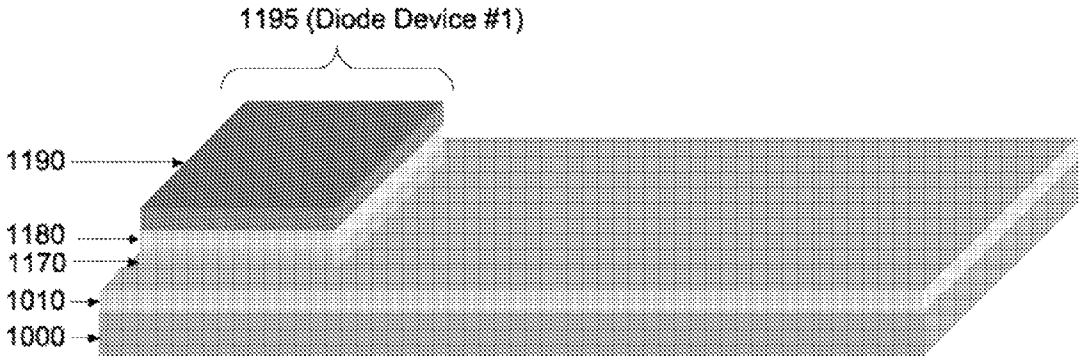


FIGURE 26

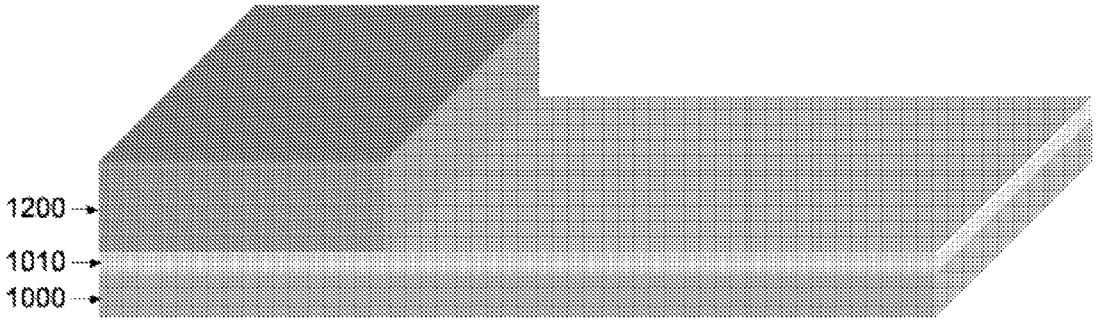


FIGURE 27

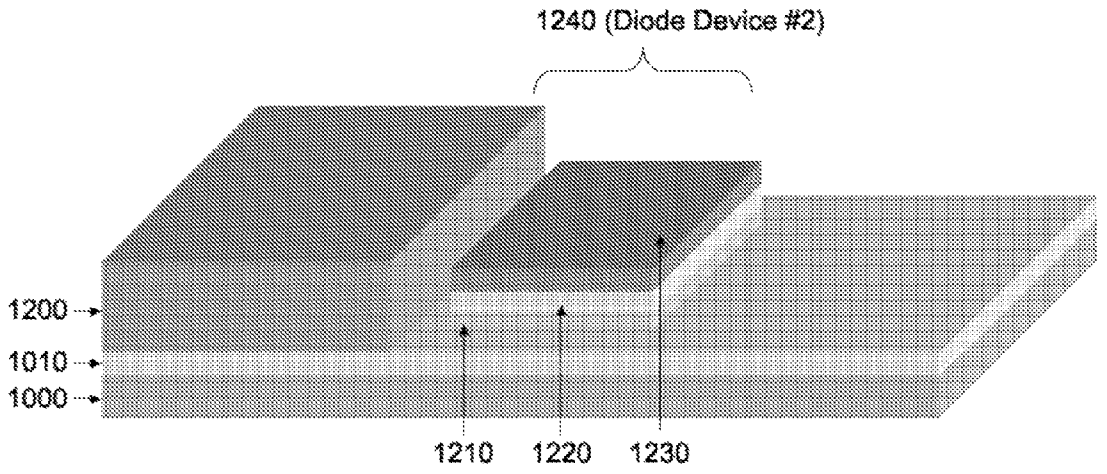


FIGURE 28

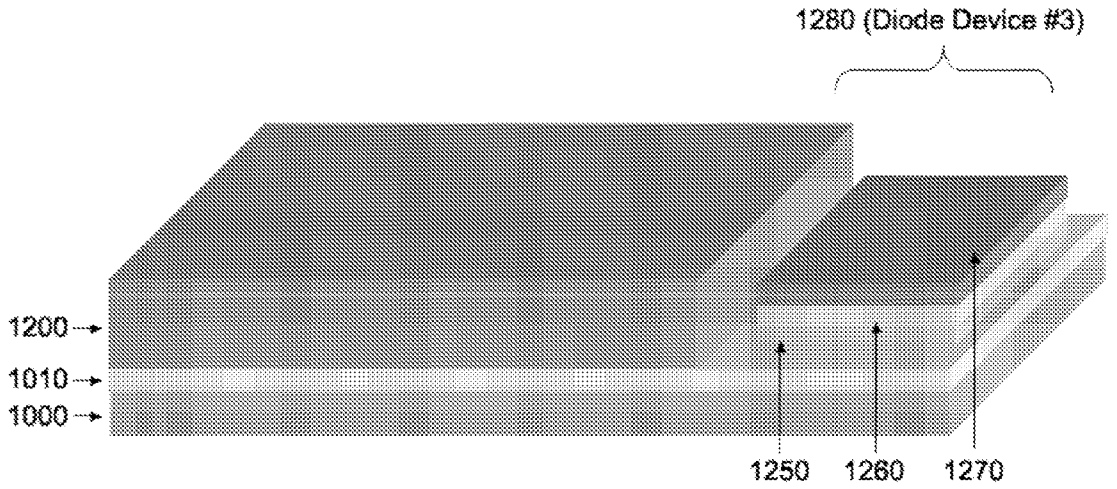


FIGURE 29

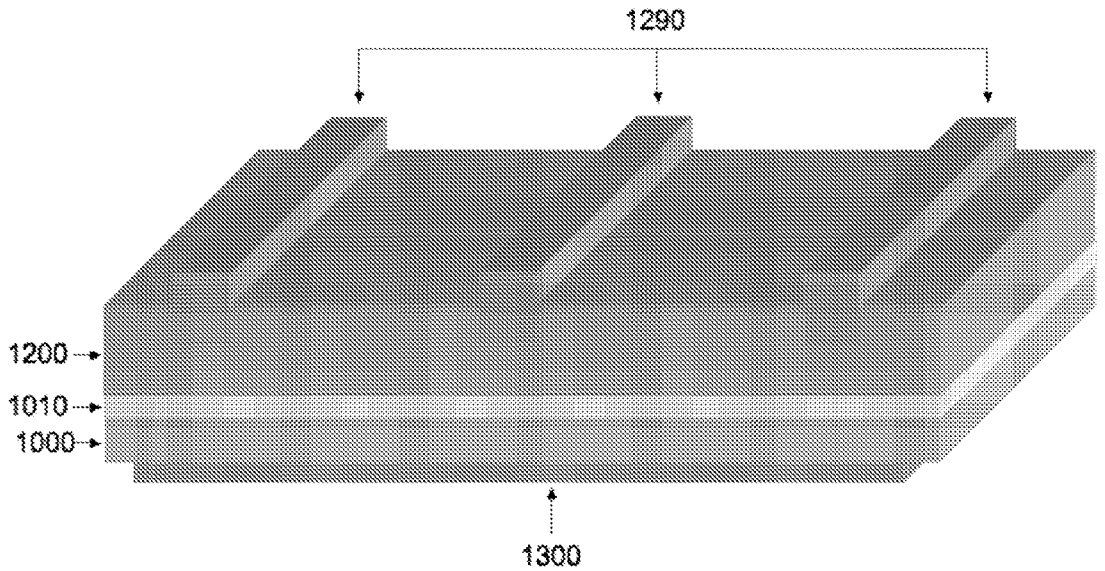
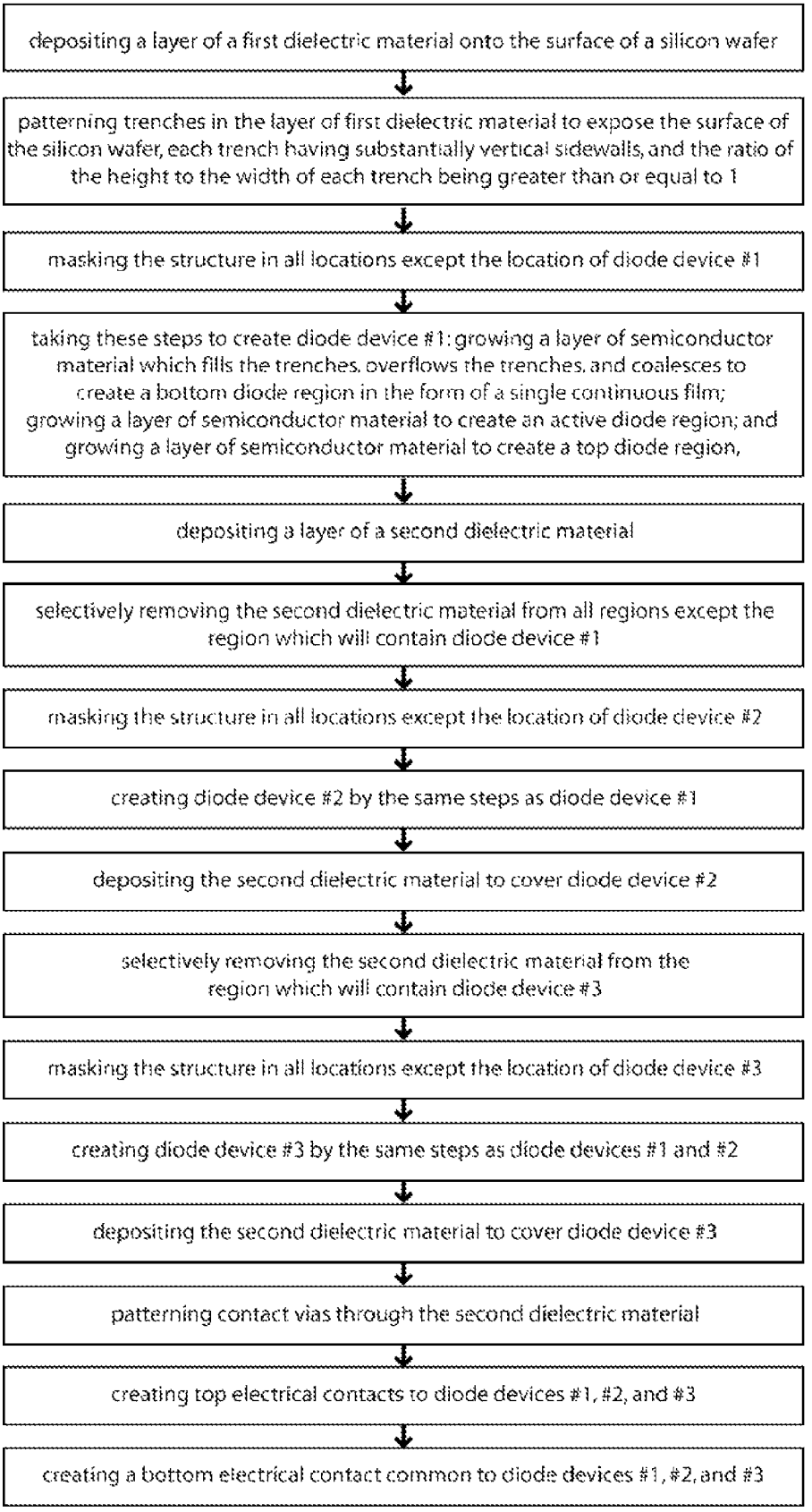


FIGURE 30


depositing a layer of a first dielectric material onto the surface of a silicon wafer
patterning trenches in the layer of first dielectric material to expose the surface of the silicon wafer, each trench having substantially vertical sidewalls, and the ratio of the height to the width of each trench being greater than or equal to 1
masking the structure in all locations except the location of diode device #1
taking these steps to create diode device #1: growing a layer of semiconductor material which fills the trenches, overflows the trenches, and coalesces to create a bottom diode region in the form of a single continuous film; growing a layer of semiconductor material to create an active diode region; and growing a layer of semiconductor material to create a top diode region,
depositing a layer of a second dielectric material
selectively removing the second dielectric material from all regions except the region which will contain diode device #1
masking the structure in all locations except the location of diode device #2
creating diode device #2 by the same steps as diode device #1
depositing the second dielectric material to cover diode device #2
selectively removing the second dielectric material from the region which will contain diode device #3
masking the structure in all locations except the location of diode device #3
creating diode device #3 by the same steps as diode devices #1 and #2
depositing the second dielectric material to cover diode device #3
patterning contact vias through the second dielectric material
creating top electrical contacts to diode devices #1, #2, and #3
creating a bottom electrical contact common to diode devices #1, #2, and #3

SEMICONDUCTOR DIODES FABRICATED BY ASPECT RATIO TRAPPING WITH COALESCED FILMS

This application claims the benefit of U.S. Provisional Patent Application Ser. No. 61/143,602, filed on Jan. 9, 2009, entitled "Semiconductor Diodes Fabricated by Aspect Ratio Trapping with Coalesced Films," which application is hereby incorporated herein by reference.

CROSS-REFERENCE TO RELATED APPLICATIONS

This application relates to the following and commonly assigned patent application Ser. No. 12/684,797, filed on Jan. 8, 2010, entitled "Diode-Based Devices and Methods for Making the Same," which application is hereby incorporated herein by reference.

TECHNICAL FIELD

The present invention relates generally to semiconductor diodes made from compound semiconductors or other lattice-mismatched semiconductors on silicon wafers, as well as methods of fabricating such semiconductor diodes, and more particularly to photonic applications such as light emitting diodes (LEDs), lasers, photovoltaics, and other optoelectronic uses.

BACKGROUND

U.S. patent application Ser. No. 12/100,131 filed on Apr. 9, 2008 claims priority to U.S. Provisional Patent Application No. 60/922,533 filed on Apr. 9, 2007, which are hereby incorporated by reference in their entirety.

This section provides background information and introduces information related to various aspects of the disclosures that are described and/or claimed below. These background statements are not admissions of prior art.

The majority of chip manufacturing takes advantage of silicon processing on high-quality, large-area, low-cost silicon wafers. Commercial manufacturers of devices made from compound semiconductors such as gallium arsenide and indium phosphide generally have been unable to take advantage of silicon wafers. They typically build light emitting diodes (LEDs), multi junction solar cells, and other compound semiconductor devices on small, expensive wafers made of materials such as sapphire, germanium, gallium arsenide, or silicon carbide.

The challenge of making compound semiconductor devices on inexpensive substrates has widespread economic implications. Compound semiconductors are an important component of our communications infrastructure because they can emit and detect light. They are the materials in the lasers that transmit signals through optical fibers, the sensors that receive those signals, the amplifiers in cellular telephones, the amplifiers in cell phone base stations, and the circuits that transmit and receive microwave signals.

Light-emitting diodes typically consist of gallium nitride films deposited onto sapphire or silicon carbide wafers. These exotic substrates contribute to the high cost of LEDs. A sapphire wafer 4 inches in diameter typically costs around $130, and a 2-inch silicon carbide wafer can cost about $2000. By contrast, an 8-inch silicon wafer, which provides four times as much surface area as a 4-inch wafer and 16 times as much surface area as a 2-inch wafer, typically costs less than $100.

High-efficiency multi junction solar cells typically contain layers such as germanium, gallium arsenide, and indium gallium phosphide deposited onto germanium wafers. As is the case with wafers for LEDs, germanium wafers similarly are smaller and significantly more expensive than silicon wafers.

The ability to create compound semiconductor devices on silicon wafers would facilitate market growth in several key industries.

Two key technical barriers have inhibited the practical fabrication of compound semiconductor devices on silicon wafers: the mismatch of lattice constants and the mismatch of thermal expansion coefficients.

Lattice Mismatch: In a crystal, the atoms sit in a regular periodic array known as a lattice. The distance between the atoms, known as the "lattice constant," is typically a few ångstroms (1 ångstrom=10^{-10} meter). Silicon has a smaller lattice constant than compound semiconductors. When compound semiconductors grow on silicon, crystalline imperfections known as misfit dislocations appear at the interface. The misfit dislocations create other crystalline defects known as threading dislocations, which propagate upward from the interface. Threading dislocations diminish the performance and the reliability of compound semiconductor devices such as lasers, solar cells, light-emitting diodes, etc.

Thermal Contraction Mismatch: Compound semiconductors typically grow at high temperatures, which can exceed 1000° C. When the wafer cools, the compound semiconductor film may contract more than the silicon wafer. As a result, the wafer may bow in a concave manner, stressing and ultimately cracking the film.

Until recently, the most promising previous efforts to grow high-quality compound semiconductors onto silicon substrates have relied on three approaches: graded buffer layers, wafer bonding, or selective growth on mesas. None of these approaches has achieved commercial success.

In graded buffer layers, the composition of the material changes gradually from substantially pure silicon to a compound semiconductor. Since the lattice constant also changes gradually, crystalline defects are less likely to form at the interface. Unfortunately, the graded buffer layers have to be relatively thick (about ten microns for a 4% lattice mismatch). The thick buffer layer increases both the costs and the likelihood of cracking.

Wafer bonding involves growing devices on expensive substrates, then lifting off the devices and bonding them to a silicon wafer. This approach rules out modern silicon processing as a route to cost reduction. Furthermore, bonding typically requires temperatures above 300° C. When the materials cool, the compound semiconductors may crack because they contract more than the silicon wafer.

Selective growth on a mesa exploits the mobility of some dislocations. The strategy is to deposit compound semiconductors in small regions (10 to 100 microns in length), thereby providing a short path where mobile dislocations can glide to the edge of the region and remove themselves from the device. However, structures created by this technique typically have a high density of threading dislocations (more than 100 million per square centimeter). This technique can't remove immobile dislocations, which predominate when the lattice mismatch exceeds 2%.

Aspect Ratio Trapping (J. S. Park et al., APL 90, 052113 (2007, hereby incorporated by reference) is a recently developed technology that makes it possible to deposit high-quality compound semiconductors, germanium or other lattice-mismatched materials on silicon wafers. FIG. **1** illustrates the principle of Aspect Ratio Trapping. We deposit a thin film of dielectric material (**20**) such as silicon dioxide (SiO2) or

silicon nitride (SiNx) onto a silicon wafer (**10**). Those of ordinary skill in the art can select a variety of dielectric materials such as SiOxNy, and silicates or oxides of materials such as Hf or Zr.

We etch a trench in the dielectric material, then deposit a non-lattice-matched semiconductor (**30**) such as germanium or a compound semiconductor in the trench. The threading dislocations (**40**), shown as dotted lines, propagate upward, typically at approximately a 45 degree angle from the interface, then intersect the sidewalls of the trench, where they terminate. Threading dislocations (**40**) do not propagate down the length of the trench because they propagate in a direction perpendicular to the faceted growth face of the crystal—the facets guide the dislocations to the sidewalls, where the dislocations terminate. We refer to the region in the trench where the sidewalls trap threading dislocations as the "trapping region" (**50**). The upper region of the non-lattice-matched semiconductor (**30**), above the trapping region (**50**), is a relatively defect-free region (**60**).

ART addresses the issue of cracking caused from mismatch of thermal expansion coefficients for these reasons: (1) the stresses are small because the epitaxial layers are thin; (2) the material can elastically accommodate the stresses arising from thermal expansion mismatch because dimensions of the ART openings are small; and (3) the SiO2 pedestals, which are more compliant than the semiconductor materials, may deform to accommodate the stress.

Continuous high-quality films of high-quality III-V semiconductors or other non-lattice-matched materials may be provided on silicon wafers using Aspect Ratio Trapping as shown in FIG. **2**. This technique is similar to the technique illustrated in FIG. **1**, except that we continue to grow the non-lattice-matched semiconductor until the growth fronts from adjacent trenches coalesce to form a single continuous film (**70**). Additional defects, which we call "coalescence defects" (**80**), form at some of the "coalescence regions" where the growth fronts meet. However, the defect density is much lower than the defect density of a non-lattice-matched semiconductor grown directly on a silicon wafer.

SUMMARY OF THE INVENTION

In one aspect, the present disclosure is directed to a photonic device comprising a substrate, a dielectric material including two or more openings that expose a portion of the substrate, the two or more openings each having an aspect ratio of at least 1, a bottom diode material comprising a compound semiconductor material that is lattice mismatched to the substrate, and wherein the compound semiconductor material occupies the two or more openings and is coalesced above the two or more openings to form the bottom diode region, a top diode material, and an active diode region between the top and bottom diode materials.

In another embodiment, the present disclosure is directed to a photonic device comprising a substrate and a photonic diode comprising a first region proximate a top surface of the substrate, a second region proximate the first region, and an active region between the first and second regions, wherein the second diode region includes a surface adjacent the active photonic diode region, the surface being generally parallel to the substrate top surface, and the second diode region includes at least one defect-trapping region spaced apart from the active photonic diode region, the defect trapping region including a surface that extends away from the substrate top surface.

In another embodiment, the present disclosure is directed to a method of making a photonic device, the method comprising depositing a layer of a dielectric material onto a substrate, patterning two or more openings in the dielectric material to expose portions of the surface of the substrate, the two or more openings having an aspect ratio of at least 1, forming a bottom diode region by growing a compound semiconductor material that is lattice mismatched to the substrate in the two or more openings and allowing the compound semiconductor material to fill in the two or more openings and coalesce above the two or more openings to form a continuous layer, forming an active diode region on the bottom diode region, and forming a top diode region on the active diode region.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. **1** illustrates the principle of Aspect Ratio Trapping, a method of depositing high-quality compound semiconductors or other non-lattice-matched semiconductors on silicon wafers;

FIG. **2** illustrates the technique for growing continuous films of high-quality compound semiconductors or other non-lattice-matched semiconductors on silicon wafers by Aspect Ratio Trapping;

FIG. **3** shows the generic structure of semiconductor diodes;

FIG. **4** shows a semiconductor diode according to a first embodiment;

FIGS. **5** and **6** show exemplary successive stages of construction for the first embodiment semiconductor diode;

FIG. **7** is a flowchart illustrating a method of fabrication according to the first embodiment;

FIGS. **8**, **9**, and **10** illustrate variations on the method illustrated in FIG. **7**;

FIG. **11** shows a donor wafer according to a second embodiment;

FIG. **12** is a flow chart illustrating a method of creating a second embodiment donor wafer;

FIGS. **13** and **14** show variations on the method illustrated in FIG. **12**;

FIGS. **15** through **17** illustrate various steps in the method of exploiting a donor wafer to create a gallium nitride substrate;

FIG. **18** is a flow chart illustrating the method illustrated in FIGS. **15** through **17**;

FIGS. **19** and **20** show variations on method illustrated in FIG. **18**;

FIG. **21** shows how cracks can appear in an epitaxially grown film;

FIG. **22** illustrates a method of reducing the thermally induced stresses in a coalesced film of semiconductor material grown on a silicon substrate by Aspect Ratio Trapping;

FIG. **23** is a flow chart illustrating the method shown in FIG. **22**;

FIG. **23**A illustrates exemplary intermediate results from an LED fabrication process;

FIG. **23**B shows an exemplary diode structure for another embodiment of an LED;

FIG. **24** through **28** illustrate steps in constructing a single chip containing a plurality of diode devices according to a third embodiment;

FIG. **29** shows a structure manufactured according to the third embodiment; and

FIG. **30** is a flow chart illustrating a method of creating a structure according to the third embodiment.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

Embodiments of the disclosure provide novel and useful architectures for semiconductor diodes made using coalesced films of compound semiconductors or other non-lattice-matched semiconductors deposited on silicon wafers by Aspect Ratio Trapping. The semiconductor diode is the fundamental building block of solar cells, light-emitting diodes, resonant tunneling diodes, semiconductor lasers, and other devices.

Aspects of the present disclosure include a reduction in the costs of solar cells, light-emitting diodes, and other compound semiconductor devices by creating them on high-quality, large-area, low-cost silicon wafers instead of smaller, more expensive substrates.

Other aspects of embodiments of the present disclosure provide for removal of the silicon wafer substrate from a semiconductor diode for devices in which the substrate can degrade performance, such as a light-emitting diode.

Still other aspects of embodiments of the present disclosure provide an economical way to fabricate a gallium nitride substrate; e.g., a high-quality film of gallium nitride on a thermally matched substrate such as polycrystalline aluminum nitride.

Other aspects of embodiments of the present disclosure provide less expensive donor wafers for creating gallium nitride films, which can then be transferred to other substrates such as aluminum nitride substrates.

Another aspect of the present disclosure is to mitigate thermally induced cracking in coalesced films grown by Aspect Ratio Trapping.

Yet other aspects of embodiments of the present disclosure provide more economical ways to create single chips containing a plurality of diode devices made from different semiconductor materials.

In the following description, exemplary diode structures are generally discussed in the context of a single diode; semiconductor engineers and others skilled in the art will understand that most applications require multiple diodes, typically integrated onto a single chip.

In general, semiconductor diodes disclosed in this document have the generic structure illustrated in FIG. **3**: a substrate (**101**), a bottom diode region (**102**), an active diode region (**103**), a top diode region (**104**), an electrical contact on the top of the device (**105**), and an electrical contact on the bottom of the device (**106**). Each of the diode regions (**102**, **103**, **104**) may be comprised of multiple layers.

The bottom diode region (**102**) and the top diode region (**104**) have opposite doping types. For example, if the bottom diode region (**102**) is predominantly n-type doped (with an electron donor such phosphorous, arsenic, or antimony), then the top diode region (**104**) will be predominantly p-type doped (with an electron acceptor such as boron or aluminum), and vice versa. Heavy doping in both the bottom diode region (**102**) and the top diode region (**104**) provides a low-resistance pathway for current to enter and leave the device. Typical doping levels of the top and bottom regions would be in the range of 10^{17}-10^{20} cm^{-3}. Typical doping levels of the active region would be below 10^{17} cm^{-3}. Note that the use of "top" and "bottom" for designating regions is a matter of convenience and in some frames of reference a top region can be located above a bottom region. For example, consider a diode formed above a substrate with its top region formed above its bottom region. If the diode is flip-chip bonded to a handle wafer and then the substrate is removed, the frame of reference for viewing the diode typically is flipped. In this case the top region will be viewed as being below the bottom region.

The substrate (**101**) is typically a silicon wafer, although in different embodiments a variety of other substrates including sapphire and silicon carbide, are suitable. At least some portion of the substrate (**101**) usually will have the same predominant doping type (either n or p) as the bottom diode region (**102**) to facilitate good electrical contact between the bottom diode region (**102**) and the substrate (**101**).

The detailed structure of the active diode region (**103**) may depend upon numerous factors, including the intended application. In one form, the active diode region (**103**) is formed by the junction of the top diode region (**102**) and the bottom diode region (**104**). In this case, it can be desirable to vary the doping of the top and bottom regions near the junction. In an LED, the active diode region (**103**) may contain many layers that include both doped layers and thin undoped quantum wells where electrons and holes can recombine and generate photons. In another example of a solar cell, the active diode region (**103**) may consist of a single layer of moderately n-doped or moderately p-doped semiconductor material to absorb incident photons and generate an electron-hole pair.

The materials used to form the diode regions are well known to those of skill in the art. Typical examples of useful semiconductor materials are: Group IV materials, such as Si, C, or Ge, or alloys of these such as SiC or SiGe; Group II-VI compounds (including binary, ternary, and quaternary forms), e.g., compounds formed from Group II materials such as Zn, Mg, Be or Cd and Group VI materials such as Te, Se or S, such as ZnSe, ZnSTe, or ZnMgSTe; and Group III-V compounds (including binary, ternary, and quaternary forms), e.g., compounds formed from Group III materials such as In, Al, or Ga and group V materials such as As, P, Sb or N, such as InP, GaAs, GaN, InAlAs, AlGaN, InAlGaAs, etc. Those of skill in the art understand how to select and process these materials based on desired properties such as bandgaps, lattice constants, doping levels, etc.

FIG. **4** shows an illustrative semiconductor diode embodiment. This diode architecture is suitable for devices in which the substrate can degrade performance. In a light-emitting diode, for example, a silicon substrate can absorb light generated within the device. In the embodiment illustrated in FIG. **4**, we have removed the silicon substrate.

FIG. **5** shows the results of the preliminary stages of construction. The foundation is a substrate (**1000**) such as a silicon wafer in which the surface preferably has a (111) crystal orientation, although other orientations are possible and in some embodiments other orientations such as (100) can be selected. The substrate (**1000**) can be either n-doped or p-doped, depending on the configuration of the diode-based device. The first step is to deposit a layer of dielectric material (**1010**) such as SiO2 or SiNx onto the silicon wafer (**1000**) by chemical vapor deposition (CVD) or another deposition technique. In devices where reflection of light from the dielectric layer creates a problem, silicon nitride can be preferable because its index of refraction is closer to that of common semiconductor materials. The thickness of the dielectric film is typically 200 to 400 nm, but it can be thicker or thinner.

Then we pattern openings for aspect ratio trapping, such as trenches (**1020**) with substantially vertical sidewalls in the layer of dielectric material (**1010**), thereby exposing the surface of the silicon wafer (**1000**) within the trenches. Two exemplary ways to pattern a trench (**1020**) are by conventional photolithography or by reactive ion etch techniques. As

would be recognized by one skilled in the art based on the disclosure herein, the trench could be another shaped opening such as a hole, recess or ring for example. The width of the trench (**1020**) should be equal to or less than the thickness of the dielectric material. This condition emerges from the principles of Aspect Ratio Trapping: the ratio of the height of the trench (**1020**) to the width of the trench (**1020**) should generally be greater than or equal to 1 in order to trap threading dislocations. Further details regarding this technique are disclosed in co-pending and commonly assigned U.S. patent application Ser. No. 11/436,198, and U.S. patent application Ser. No. 11/852,078, which are hereby incorporated in their entirety by reference). And in (Park et al., Appl. Phys. Lett. 90, 052113 [2007]), which is incorporated herein by reference.

In some cases, it may be advantageous to clean the surface of the silicon substrate (**1000**) at the bottom of the trenches (**1020**) to prepare for epitaxial growth of the bottom diode region. For one version of a suitable cleaning process, which includes an oxygen plasma etch, see Park et al., Appl. Phys. Lett. 90, 052113 [2007].

FIG. **6** illustrates the results of the next several steps. First we grow the bottom diode region (**1030**). The semiconductor material for the bottom diode region (**1030**) depends on the device. For a solar cell, the bottom diode region (**1030**) is, for example, indium gallium phosphide (InGaP). For a light-emitting diode, the bottom diode region (**1030**) is, for example, gallium nitride (GaN). We can also make the bottom diode region from many other semiconductor materials, including compound semiconductor materials, which have useful properties for devices such as lasers and resonant tunneling diodes. Exemplary semiconductor materials are described above.

It is possible to dope the bottom diode region (**1030**) in situ during epitaxial growth or to dope it ex situ by ion implantation. (As a general matter, it is generally preferable to dope the bottom diode regions, active diode regions, and top diode regions mentioned in this disclosure, and it is possible to dope them either in situ during epitaxial growth or ex situ by ion implantation.)

We refer to a portion of the bottom diode region (**1030**) in the trenches (**1020**) as the "trapping region" (**1050**) because it traps dislocations such as threading dislocations (**1040**), which originate at the interface between the bottom diode region (**1030**) and the substrate (**1000**) and propagate upward towards the side walls. FIG. **6** illustrates the threading dislocations (**1040**) as dashed lines. The portion of the bottom diode region (**1030**) which lies above the trapping region (**1050**) remains relatively free of defects. This low-defect region enables us to create high-quality compound semiconductor devices on high-quality, large-area, low-cost silicon wafers. For some materials, such as GaN, InN, AlN, or ternary or quarternary combinations of these, a dislocation density of e.g. less than or equal to $10^8/cm^2$ is low enough to be useful for device applications. For some other materials, such as GaAs and InP, a somewhat lower dislocation density is typically required to be useful for devices, e.g. less than or equal to $10^6/cm^2$.

We continue to grow the bottom diode region (**1030**) until a) the material overflows the trenches, and b) the material from adjacent trenches coalesce to form a single continuous film. It is typically desirable to planarize the bottom diode region (**1030**) by chemical mechanical processing or any other suitable technique before further fabrication. The next steps are to deposit the active diode region (**1060**) and the top diode region (**1070**). In most embodiments, the active diode region (**1060**) and the top diode region (**1070**) have the same or approximately the same lattice constants as the bottom diode region (**1030**).

FIG. **4** shows the results of the final steps. We bond a handle substrate (**1080**) to the top diode region (**1070**). In some embodiments, it may be preferable to planarize the top diode region (**1070**) in order to achieve a high-quality bond to the handle substrate (**1080**). In still other embodiments, it may be preferable to include an intermediate layer between the top diode region (**1070**) and the handle substrate (**1080**) to improve adhesion, minimize thermal mismatch, or the like. The handle substrate (**1080**) could be part of an LED packaging fixture. Bonding methods are well known, including those used in flip-chip bonding, where the top portion of an LED is bonded to a surface that is part of an LED package. The handle substrate (**1080**) may be conductive, or it may contain conductive elements which serve as contacts for the top diode region (**1070**). Then we remove the silicon substrate (**1000**) by standard techniques such as grinding, chemical etch-back, laser ablation, or some combination of those methods.

Finally, we add a first electrical contact (**1090**) to the bottom diode region (**1030**) and a second electrical contact (**1100**) to the handle substrate (**1080**). In various embodiments the material for the electrical contacts can be, for example, a strip of conductive metal such as copper, silver, or aluminum, or a layer of relatively transparent conductive oxide such as indium tin oxide. For light-emitting diodes, the bottom electrical contact (**1100**) should preferably be a highly reflective conductive material, such as silver, which will reflect the internally created light so it will exit the LED from another surface.

People skilled in the art of semiconductor diode manufacturing know many materials for and ways of adding electrical contacts. FIG. **4** shows one option for creating the first electrical contact (**1090**): we have removed the dielectric layer (**1010**) to expose the surface of the bottom diode region (**1030**). Here, the dielectric material (**1010**) is removed by standard techniques such as etching. In an LED, the trapping regions (**1050**) shown in FIG. **4** could effectively roughen the surface to reduce internal reflection of light, provided that their size and spacing were correct.

The following are examples of process parameters sufficient to form the bottom, active, and top diode regions according to embodiments in this disclosure. First, a substrate and a patterned dielectric layer as known in the art are provided. Exemplary process parameters for bottom, active, and top diode regions, for of a GaAs and AlGaAs-based LED, according to one embodiment are below.

A) Bottom diode region (e.g., **1030**): (e.g., 100 nm-500 nm thick layer of GaAs);
Pressure: 0.1 atm
Precursors: TMG (Trimethylgallium) and 20% AsH3 (Arsine), diluted in H2
Temperature: 720 C
N-type: dope with silicon
B) Active diode region (e.g., **1060**): AlGaAs layer for carrier confinement (15 nm thick)
Pressure: 0.1 atm
Precursors: TMG, TMA (Trimethylaluminium), and 20% arsine, diluted in H2
Temperature: 850 C
N-type: dope with silicon
GaAs Quantum well for emission (10 nm thick)
Pressure: 0.1 atm
Precursors: TMG and 20% arsine, diluted in H2
Temperature: 720 C

No doping
AlGaAs layer for carrier confinement (15 nm thick)
Pressure: 0.1 atm
Precursors: TMG, TMA (Trimethylaluminium), and 20% arsine, diluted in H2
Temperature: 850 C
P-type: dope with zinc
C) Top diode region (e.g., **1070**): (e.g., 100 nm-500 nm thick layer of GaAs)
Pressure: 0.1 atm
Precursors: TMG and 20% arsine, diluted in H2
Temperature: 720 C
P-type: dope with zinc

Exemplary prophetic process parameters of growth conditions (e.g., CVD) for bottom, active, and top diode regions, for a GaN and InGaN-based LED, according to the first embodiment 1 are below.

A) Bottom diode region (e.g., **1030**):
GaN low-temperature buffer (e.g., 30 nm thick)
Pressure: 100 Torr
Precursors: TMG and NH3, diluted in H2
Temperature: 530 C
N-type: dope with silicon
GaN hi-temperature buffer (e.g., 500 nm thick)
Pressure: 100 Torr
Precursors: TMG and NH3, diluted in H2
Temperature: 1030 C
N-type: dope with silicon
B) Active diode region (e.g., **1060**):
InGaN Quantum well layer for emission (e.g., 2 nm thick)
Pressure: 100 Torr
Precursors: TMG+TMI+NH3, diluted in N2
Temperature: 740 C
No doping
GaN barrier layer for carrier confinement (e.g., 15 nm thick)
Pressure: 100 Torr
Precursors: TMG and NH3, diluted in H2
Temperature: 860 C
N-type: dope with silicon
C) Top diode region (e.g., **1070**): GaN p-contact layer (e.g., 100 nm thick)
Pressure: 100 Torr
Precursors: TMG and NH3, diluted in H2
Temperature: 950 C
P-type: dope with magnesium

Embodiment No. 1, shown in FIG. **4**, includes a semiconductor diode made from compound semiconductors or other lattice-mismatched materials on a silicon wafer comprising these elements: a bottom diode region (**1030**), an active diode region (**1060**), a top diode region (**1070**), a handle substrate (**1080**), a first electrical contact (**1090**), a second electrical contact (**1100**), and a trapping region (**1050**) where threading dislocations terminate.

The bottom diode region (**1030**), the active diode region (**1060**), and the top diode region (**1070**) will have low defect densities (typically less than or equal to 5×10^7 per square centimeter) as a result of growing the bottom diode region (**1030**) as a coalesced film by Aspect Ratio Trapping.

Turning now to FIG. **7**, which illustrates a method of fabricating a device according to the first embodiment. The method includes: depositing a layer of dielectric material (**1010**) onto the surface of a silicon wafer (**1000**), patterning trenches (**1020**) in the layer of dielectric material (**1010**) to expose the surface of the silicon wafer (**1000**), each trench (**1020**) having substantially vertical sidewalls, and the ratio of the height to the width of each trench (**1020**) being greater than or equal to 1, growing a semiconductor material to form a bottom diode region (**1030**) which fills the trenches (**1020**) and coalesces to form a single continuous film, growing a semiconductor material upon the bottom diode region (**1030**) to form an active diode region (**1060**), growing a semiconductor material upon the active diode region (**1060**) to form a top diode region (**1070**), bonding a handle substrate (**1080**) to the top diode region (**1070**), removing the silicon substrate (**1000**), removing the dielectric material (**1010**), fabricating a first electrical contact (**1090**) on the surface of the bottom diode region (**1030**), and fabricating a second electrical contact (**1100**) on the surface of the handle substrate (**1080**).

FIG. **8** summarizes a variation of the method illustrated in FIG. **7** in which we clean the surface of the silicon wafer at the bottom of the trenches before depositing the bottom diode region. FIG. **9** summarizes another variation in which we planarize the surface of the bottom diode region before growing the active diode region. FIG. **10** summarizes yet another variation in which we planarize the surface of the top diode region before bonding it to the handle substrate.

Another exemplary embodiment allows coalesced films deposited by Aspect Ratio Trapping to create gallium nitride substrates. In this document, as in the LED industry, the term "gallium nitride substrate" means a thin film as well known in the art of gallium nitride (GaN) grown onto, or bonded onto, a substrate made from a material other than GaN. LED manufacturers typically buy GaN substrates from materials suppliers, then deposit additional layers of GaN and other materials to create LEDs. A typical GaN substrate consists of a layer of GaN deposited on a wafer of sapphire (Al2O3) silicon carbide. The worldwide market for gallium nitride substrates currently is about $300 million per year.

Materials suppliers typically deposit GaN onto Al2O3 because these two materials have a reasonably good lattice match. However, GaN and Al2O3 have very different thermal expansion coefficients. When LED manufacturers heat the GaN/Al2O3 structure to deposit additional layers, the difference in thermal expansion coefficients causes the structure to bow. The bowing causes some portion of the Al2O3 wafer to lose contact with the susceptor, the substrate heater in the deposition chamber. As a result, the temperature of the Al2O3 wafer varies as a function of position. The inconsistent Al2O3 wafer temperature causes variations in layer composition and layer thickness. The practical consequence is that manufacturers have difficulty controlling the emission wavelength of the resulting LED.

An emerging technique for creating GaN substrates may solve or at least ameliorate this problem. The essence of this emerging technique is to extract a GaN thin film from a donor wafer and to bond that film to a substrate of aluminum nitride, which has a thermal expansion coefficient similar to that of GaN. The donor wafer is typically a wafer of single-crystal GaN. The conventional method of extracting the GaN thin film from the donor wafer involves ion implantation and exfoliation. The manufacturers implant hydrogen ions into the donor wafer to create a cleave plane, then split the donor wafer by annealing it or by applying mechanical pressure. This technique makes it possible to extract multiple thin films from a single donor wafer.

FIG. **11** illustrates a second embodiment that provides for a novel donor wafer which can be produced at lower cost than a donor wafer of single-crystal GaN. We begin with a substrate (**1000**) such as a silicon wafer in which the surface has a (111) crystal orientation. However, other orientations are possible and in some embodiments other orientations such as (100) can be selected. The substrate (**1000**) can be either n-doped or p-doped. Onto that substrate (**1000**), we deposit a

layer of dielectric material (**1010**). Next, we pattern trenches with substantially vertical sidewalls in the layer of dielectric material (**1010**), thereby exposing the surface of the silicon wafer (**1000**). In the stage of manufacture illustrated in FIG. **11**, the trenches have been filled with semiconductor material (**1100**) as described below. As before, to promote trapping of threading dislocations, the width of each trench should be less than or equal to the thickness of the dielectric material. Optionally, we might then clean the surface of the silicon substrate (**1000**) at the bottom of the trenches by the techniques described above.

The next step is to grow a layer of semiconductor material (such as GaN) (**1110**) until the material overflows the trenches and the material from adjacent trenches coalesce to form a single continuous film. Exemplary semiconductor materials are described above. The portion of the semiconductor material (**1110**) which fills the trenches serves as a trapping region (**1050**); it traps the threading dislocations (**1040**). The portion of the semiconductor material (**1110**) above the trapping regions (**1050**) grows substantially free of threading dislocations. Coalescence defects may appear at some of the locations where the growth fronts from adjacent trenches merge, but the density of coalescence defects is low enough (generally less than or equal to $5\times10^7/cm^2$) to allow the structure to be technologically useful.

FIG. **11** illustrates a novel donor wafer which can yield multiple thin films from the layer of semiconductor material (**1110**). For example, the illustrated embodiment could provide a source of multiple GaN films which could be separated by ion implantation and exfoliation, then bonded to aluminum nitride wafers. Aspect Ratio Trapping makes it possible to create high-quality GaN films for this donor wafer on an inexpensive silicon substrate.

The embodiment shown in FIG. **11**, is a donor wafer composed of these elements: a silicon wafer substrate (**1000**), a layer of dielectric material (**1010**) covering the silicon wafer substrate (**1000**), the layer of dielectric material (**1010**) containing trenches which expose the surface of the silicon wafer substrate (**1000**), the trenches having substantially vertical sidewalls, and the ratio of the height to the width of the trenches being greater than or equal to 1, a layer of semiconductor material (**1110**) which fills the trenches and overflows the trenches to create a single continuous film, and trapping regions (**1050**) within the trenches wherein threading dislocations (**1040**) intersect the sidewalls of the dielectric material and terminate.

FIG. **12** summarizes a method to fabricate the donor wafer shown in FIG. **11**. It includes these steps: depositing a layer of dielectric material (**1010**) onto the surface of a silicon wafer (**1000**), patterning trenches in the layer of dielectric material (**1010**) to expose the surface of the silicon wafer (**1000**), each trench having substantially vertical sidewalls, and the ratio of the height to the width of each trench being greater than or equal to 1, and growing a layer of semiconductor material (**1110**) such as GaN which fills the trenches and coalesces to form a single continuous film.

FIG. **13** summarizes a variation on the method illustrated in FIG. **12**, in which we clean the surface of the silicon wafer substrate (**1000**) at the bottom of the trenches before growing the semiconductor material (**1110**). FIG. **14** summarizes another variation in which we planarize the surface of the semiconductor material (**1110**).

Described next is a way of exploiting the donor wafer concept described above to create a GaN substrate, such as a high-quality GaN film bonded to an AlN wafer. More generally, it is a method of creating a layer of semiconductor material bonded to an arbitrary substrate material.

After we create the donor wafer (shown in FIG. **11**), FIG. **15** illustrates a next step: we implant the layer of semiconductor material (**1110**) with ions, such as, for example, hydrogen ions or a combination of hydrogen and helium ions, to create a cleave plane (**1120**). Next we bond the layer of semiconductor material (**1110**) by conventional techniques to a handle substrate (**1130**), as shown in FIG. **16**. If the semiconductor material (**1110**) is GaN, a generally preferred material for the handle substrate (**1130**) is a material with a similar thermal expansion coefficient, such as AlN.

The final step is to split the layer of semiconductor material (**1110**) at the cleave plane (**1120**) by annealing it or by applying mechanical pressure. The result is shown in FIG. **17**: a layer of semiconductor material (**1110**) bonded to a handle substrate (**1130**). This structure is especially useful when the defect density of the semiconductor material (**1110**) is low (e.g., less than or equal to $5\times10^7/cm^2$), when there is a mismatch of lattice constants between the semiconductor material (**1110**) and the handle substrate (**1130**), and/or there is a close match of thermal expansion coefficients between the semiconductor material (**1110**) and the handle substrate (**1130**). Again, for some materials, such as GaN, InN, MN, or ternary or quarternary combinations of these, a dislocation density of e.g. less than or equal to $10^8/cm^2$ is low enough to be useful for device applications. For some other materials, such as GaAs and InP, a somewhat lower dislocation density is typically required to be useful for devices, e.g. less than or equal to $10^6/cm^2$.

FIG. **18** summarizes the above described method to create a structure composed of a layer of semiconductor material bonded to a substrate comprising these steps: depositing a layer of dielectric material (**1010**) onto the surface of a silicon wafer (**1000**), patterning trenches in the layer of dielectric material (**1010**) to expose the surface of the silicon wafer (**1000**), each trench having substantially vertical sidewalls, and the ratio of the height to the width of each trench being greater than or equal to 1, growing a layer of semiconductor material (**1110**) which fills the trenches and coalesces to form a single continuous film, implanting the layer of semiconductor material (**1110**) with ions to create a cleave plane (**1120**), bonding a handle substrate (**1130**) to the layer of semiconductor material (**1110**), and splitting the layer of semiconductor of material (**1110**) at the cleave plane (**1120**).

FIG. **19** summarizes a variation of the method illustrated in FIG. **19**, in which we clean the surface of the silicon wafer (**1000**) at the bottom of the trenches before depositing the layer of semiconductor material (**1010**). FIG. **20** summarizes another variation of Method C in which we planarize the surface of the layer of semiconductor material (**1110**) before implanting it with ions.

In some embodiments, coalesced films grown by Aspect Ratio Trapping may be susceptible to cracking because the epitaxial materials typically have larger thermal expansion coefficients than the silicon wafer substrate. When the structure cools from the growth temperature, the film contracts more than the substrate. As FIG. **21** illustrates, tensile strain in the film can lead to cracks (**1140**). Cracks (**1140**) can impair the performance and the reliability of devices such as LEDs or solar cells.

FIG. **22** shows a novel solution: create divots (**1150**) in the layer of semiconductor material. It would be possible to create these divots by standard techniques, such as lithography, etching, or laser ablation. The divots (**1150**) effectively limit the area of the coalesced film. As a result, they reduce the thermally induced stresses in the semiconductor material. If the divots have the proper size and spacing, they will allow the semiconductor material to accommodate the thermal stress

elastically, without cracking. If the divots have the proper size and spacing, they will allow the semiconductor material to accommodate and largely reduce or eliminate wafer bow. FIG. **23** summarizes this method of reducing the thermally induced stresses in a coalesced film of semiconductor material grown on a silicon substrate by Aspect Ratio Trapping: depositing a layer of dielectric material (**1010**) onto the surface of a silicon wafer (**1000**), patterning trenches in the layer of dielectric material (**1010**) to expose the surface of the silicon wafer (**1000**), each trench having substantially vertical sidewalls, and the ratio of the height to the width of each trench being greater than or equal to 1, growing a layer of semiconductor material (**1030**) which fills the trenches and coalesces to form a single continuous film, and creating divots (**1150**) in the semiconductor material.

In one embodiment, exemplary first divots can extend along a first direction in parallel with a regular, irregular, prescribed, periodic or intermittent spacing, for example, between 0.1 um and 1.0 um. In this manner, the semiconductor material can be made into a plurality of strips or segments. Exemplary second divots similar to the first divots can extend in a second direction (e.g., perpendicular) to the first direction. In this manner, the semiconductor material can be made into a plurality of islands. If the first and second divot patterning was regular and equal, the resulting islands would be squares, however, other known shapes for such islands may be used. In one embodiment, the semiconductor material can include a lower diode region, an active diode region and an upper diode region.

An exemplary method of reducing the thermally induced stresses in coalesced films forming an LED grown on a silicon substrate by Aspect Ratio Trapping (ART) can include: depositing a layer of dielectric material (**1010**) onto the surface of a silicon wafer (**1000**), patterning trenches or holes in the layer of dielectric material (**1010**) to expose the surface of the silicon wafer (**1000**) with unpatterned lanes or sections between areas filled with patterned trenches or holes, each trench having substantially vertical sidewalls, and the ratio of the height to the width of each trench or hole being sufficient to create a trapping region, and successively growing a coalesced bottom diode region, an active diode region and a top diode region corresponding to the patterned areas within the lanes of unpatterned dielectric material (**1010**) by standard methods (e.g., MOCVD) to result in divots over the lanes of unpatterned dielectric material (**1010**).

FIG. **23**A illustrates exemplary results from these several steps. Separating (e.g., saw or cleave) individual LEDs corresponding to the divots in the semiconductor material and/or additional steps previously described with respect to the above described first embodiment can result in an alternative embodiment of a LED.

In one embodiment, divots in each lane can occupy 10-30% of a length or width dimension of a corresponding LED. Exemplary divots can include slanted sidewalls at a 45 degree angle to a top surface of an adjacent LED. Alternatively, sidewalls of divots can use a greater or smaller angle such as 30 degrees, 60 degrees, etc.

The active regions for LEDs in a III-N system can be grown over relaxed GaN. For example, such relaxed GaN can be c-plane bulk GaN wafer or substantially relaxed c-plane GaN epilayer grown over a substrate of sapphire or silicon carbide. However, for visible light emission, the emission region must contain a significant fraction of indium. Thus, the emission regions for visible light LEDs in a III-N system have one or more InGaN alloy layers. InGaN has a larger lattice constant than GaN. To avoid or reduce dislocations that accompany relaxation of strained epilayers, such InGaN films remain strained over the underlying GaN layer (e.g., as they are grown to have substantially the same lattice constant as the underlying GaN layer). Further, the c-plane III-N semiconductor materials are polar materials and the strain in the emission region leads to significant polarization fields (e.g., piezoelectric polarization), which can be deleterious to device performance. For example, device/emission efficiency can be degraded or the wavelength of emission can be shifted.)

FIG. **23**B shows an exemplary diode structure for another embodiment of an LED. In FIG. **23**B, at least a portion of a lower diode region close to the substrate comprises InGaN (instead of GaN). The InGaN lower diode region can be a relaxed layer with reduced or controlled defect densities formed using ART techniques. Such an InGaN lower diode region can be a platform for emission regions (e.g., LED emission regions) with significantly reduced strain. For example, further growth of subsequent layers for the active diode region (e.g., InGaN with low or no strain) and upper diode region result in emission regions with significantly reduced strain. As shown in FIG. **23**B, a lower diode region is relaxed N-type InGaN over and partially in a defect trapping region, an active diode region is subsequent layers of AlGaN barrier region (e.g., lattice spacing equal to the lower diode region), a reduced strain InGaN emission region and an AlGaN barrier region (e.g., lattice spacing equal to the emission region) In FIG. **23**B, the substrate can be a silicon substrate, and contacts to the upper/top and lower/bottom diode regions can be subsequently added (e.g., as described above).

Manufacturers of LEDs have created multi-chip solutions in which they mounted semiconductor chips made of different materials into a single package or module. This technique allows them to combine different colors to achieve white light.

Researchers developing high-efficiency solar cells have created multi-chip solutions in which they mounted semiconductor chips made of different materials into a single package or module. They were implementing a "split spectrum" approach in which they directed a portion of the solar spectrum onto a chip optimized for that portion of the spectrum.

In both of these cases, the costs of mounting and packaging multiple chips may be prohibitively high. We propose a single-chip solution, which has the potential to be much less expensive. For illustrative purposes, we will describe a single chip with three separate diodes.

FIG. **24** shows the first few steps. We deposit a layer of a first dielectric material (**1010**) onto a silicon substrate (**1000**). Then we pattern trenches (**1160**) with substantially vertical sidewalls in a first region of the layer of dielectric material (**1010**). Each trench exposes the surface of the silicon wafer (**1000**). The width of each trench should be equal to or less than the thickness of the dielectric material so that the trench can trap threading dislocations.

Optionally, we might then clean the surface of the silicon substrate (**1000**) at the bottom of the trenches (**1160**) by the techniques described above.

The next step is to mask the top surface of the structure in all locations except the location of diode device number **1** (**1195**). We then grow the bottom diode region (**1170**), a layer of semiconductor material which fills the trenches and coalesces to form a single continuous film, as shown in FIG. **25**. Exemplary semiconductor materials are described above. Misfit dislocations form at the interface between the bottom diode region (**1170**) and the silicon substrate (**1000**). Threading dislocations propagate upward at a 45 degree angle, intersect the sidewalls of the trenches, and terminate within a trapping region.

At this point, it might be useful to planarize the bottom diode region (**1170**).

Then we grow a layer of semiconductor material to form the active diode region (**1180**) and yet another layer of semiconductor material to form the top diode region (**1190**). Together, the bottom diode region (**1170**), the active diode region (**1180**), and the top diode region (**1190**) make up diode device number **1** (**1195**).

Next we deposit a layer of a second dielectric material (**1200**). For example, if the first dielectric material was SiO2, the second dielectric material might be SiNx. We selectively remove the second dielectric material (**1200**) by wet or dry etch from all regions except the region which contains diode device number **1**, leaving the structure shown in FIG. **26**.

Then we mask the structure in all locations except the location of diode device number **2** (**1240**). In the next steps, we create diode device number **2**, following the same steps by which we created diode device number **1**, thereby yielding the structure shown in FIG. **27**. As shown in the FIG. **27**, a bottom diode region (**1210**), an active diode region (**1220**), and a top diode region (**1230**) make up diode device number **2** (**1240**).

We deposit another layer of the second dielectric material (**1200**) to cover diode device number **2** (**1240**). Then we selectively remove this layer of the second dielectric material (**1200**) by wet or dry etch from the region which will contain diode device number **3** (**1280**).

Next we mask the structure in all locations except the location of diode device number **3** (**1280**) and create diode device number **3** (**1280**), following the same steps by which we created diode device number **1** (**1195**) and diode device number **2** (**1240**). The result is the structure shown in FIG. **28**. As shown in the FIG. **28**, a bottom diode region (**1250**), an active diode region (**1260**), and a top diode region (**1270**) make up diode device number **3** (**1280**).

Finally, we cover diode device number **3** (**1280**) with the second dielectric material (**1200**), pattern contact vias through the second dielectric material (**1200**), and deposit individual contacts (**1290**) on the top of each diode device. We also create a bottom electrical contact (**1300**) preferably but not necessarily common to all devices on the support substrate (**1000**).

The result is shown in FIG. **29**. The various diode devices can contain different sets of semiconductor materials for the top, active, and bottom diode regions. In each diode device, the bandgaps of the materials are tailored to emit light of the desired color (in an LED) or to absorb light of the desired frequency (in a solar cell). This embodiment represents a relatively inexpensive way to create multiple diode devices on a single chip.

In summary, a single chip containing a plurality of diode devices, comprising the following elements: a silicon wafer substrate (**1000**), a layer of a first dielectric material (**1010**) covering the silicon wafer substrate (**1000**), this layer of first dielectric material (**1010**) containing trenches (**1160**) which expose the surface of the silicon wafer substrate (**1000**), these trenches (**1160**) having substantially vertical sidewalls, and the ratio of the height to the width of these trenches (**1160**) being greater than or equal to 1, a plurality of diode devices (at least three devices **1995**, **1240**, **1280**), each of which comprises a layer of semiconductor material which fills trenches (**1160**) in one portion of the layer of first dielectric material (**1010**) and overflows the trenches (**1160**) to create a bottom diode region (**1170**, **210**, **1250**), a trapping region for trapping threading dislocations within the trenches (**1160**), an active diode region (**1180**, **1220**, **1260**), and a top diode region (**1190**, **1230**, **1270**), a layer of a second dielectric material (**1200**) covering the diode devices (**1995**, **1240**, **1280**), top electrical contacts (**1290**), and a bottom electrical contact (**1300**).

FIG. **30** summarizes a method of fabricating the structure shown in FIG. **29**. This method of fabricating a plurality of diode devices on a single chip includes these steps:

- depositing a layer of a first dielectric material (**1010**) onto the surface of a silicon wafer (**1000**),
- patterning trenches (**1160**) in the layer of first dielectric material (**1010**) to expose the surface of the silicon wafer (**1000**), each trench (**1160**) having substantially vertical sidewalls, and the ratio of the height to the width of each trench (**1160**) being greater than or equal to 1,
- masking the structure in all locations except the location of diode device No. **1** (**1195**),
- taking these steps to create diode device No. **1**: growing a layer of semiconductor material which fills the trenches, overflows the trenches, and coalesces to create a bottom diode region (**1170**) in the form of single continuous film; growing a layer of semiconductor material to create an active diode region (**1180**); and growing a layer of semiconductor material to create a top diode region (**1190**),
- depositing a layer of a second dielectric material (**1200**),
- selectively removing the second dielectric material (**1200**) from all regions except the region which contains diode device No. **1** (**1195**),
- masking the structure in all locations except the location of diode device No. **2** (**1240**),
- creating diode device No. **2** (**1240**) by the same steps as diode device No. **1** (**1195**),
- depositing the second dielectric material (**1200**) to cover diode device No. **2** (**1240**),
- selectively removing the second dielectric material (**1200**) from the region which will contain diode device No. **3** (**1280**),
- masking the structure in all locations except the location of diode device No. **3** (**1280**),
- creating diode device No. **3** (**1280**) by the same steps as diode device No. **1** (**1195**) and diode device No. **2** (**1240**),
- depositing the second dielectric material (**1200**) to cover diode device No. **3** (**1280**),
- patterning contact vias through the second dielectric material (**1200**),
- creating top electrical contacts (**1290**) to diode device No. **1**, diode device No. **2**, and diode device No. **3**, and
- creating a bottom electrical contact (**1300**) common to all three diode devices.

It would, of course, be possible to create any number of diode devices on a single chip, the only limitation being the amount of available space.

Embodiments of the application were described using trenches to provide trapping regions, however, alternative structural configurations of recesses with cross-sections functionally sufficient and intended to trap defects may be used herein as "trenches."

Embodiments of the application provide methods, structures or apparatus that may use and/or form by epitaxial growth or the like. For example, exemplary suitable epitaxial growth systems may be a single-wafer or multiple-wafer batch reactor. Various CVD techniques may be used. Suitable CVD systems commonly used for volume epitaxy in manufacturing applications include, for example, an Aixtron 2600 multi-wafer system available from Aixtron, based in Aachen, Germany; an EPI CENTURA single-wafer multi-chamber systems available from Applied Materials of Santa Clara,

Calif.; or EPSILON single-wafer epitaxial reactors available from ASM International based in Bilthoven, The Netherlands.

Any reference in this specification to "one embodiment," "an embodiment," "example embodiment," "another embodiment," "other embodiments," etc., means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of such phrases in various places in the specification are not necessarily all referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with any embodiment, it is submitted that it is within the purview of one skilled in the art to affect such feature, structure, or characteristic in connection with other ones of the embodiments. Furthermore, for ease of understanding, certain method procedures may have been delineated as separate procedures; however, these separately delineated procedures should not be construed as necessarily order dependent in their performance. That is, some procedures may be able to be performed in an alternative ordering, simultaneously, etc. In addition, exemplary diagrams illustrate various methods in accordance with embodiments of the present disclosure. Such exemplary method embodiments are described herein using and can be applied to corresponding apparatus embodiments, however, the method embodiments are not intended to be limited thereby.

Although few embodiments of the present invention have been illustrated and described, it would be appreciated by those skilled in the art that changes may be made in these embodiments without departing from the principles and spirit of the invention. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting on the invention described herein. Scope of the invention is thus indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein. As used in this disclosure, the term "preferably" is non-exclusive and means "preferably, but not limited to." Terms in the claims should be given their broadest interpretation consistent with the general inventive concept as set forth in this description. For example, the terms "coupled" and "connect" (and derivations thereof) are used to connote both direct and indirect connections/couplings. As another example, "having" and "including", derivatives thereof and similar transitional terms or phrases are used synonymously with "comprising" (i.e., all are considered "open ended" terms)—only the phrases "consisting of" and "consisting essentially of" should be considered as "close ended". Claims are not intended to be interpreted under 112 sixth paragraph unless the phrase "means for" and an associated function appear in a claim and the claim fails to recite sufficient structure to perform such function.

Advantageous embodiments could include a photonic device comprising a substrate, a dielectric material including two or more openings that expose a portion of the substrate, the two or more openings each having an aspect ratio of at least 1, a bottom diode material comprising a compound semiconductor material that is lattice mismatched to the substrate, and wherein the compound semiconductor material occupies the two or more openings and is coalesced above the two or more openings to form the bottom diode region, a top diode material, and an active diode region between the top and bottom diode materials. The substrate could be selected from the group consisting of silicon, sapphire, and silicon carbide. The substrate could be a single crystal silicon wafer. The single crystal silicon wafer could have a crystal orientation of (111) or (100). The active diode region could comprise a p-n junction formed by a junction of the top and bottom diode materials. The active diode region could comprise a material different from the top and bottom diode materials, and could form an intrinsic region of a p-i-n junction formed between the top and bottom diode materials. The active diode region could comprise multiple quantum wells formed between the top and bottom diode materials. The dielectric material could comprise a material selected from the group consisting essentially of silicon dioxide, silicon nitride, silicon oxynitride, oxides of hafnium, silicates of hafnium, oxides of zirconium, silicates of zirconium, and combinations thereof. The opening could be a trench or could be a hole having an aspect ratio of at least 1 in two perpendicular axes. The semiconductor material could comprise a Group III-V compound, a Group II-VI compound, or a Group IV alloy. The bottom diode material could include an n-type dopant and the top diode material could include a p-type dopant. The device could further include a contact formed over the top diode region. The contact could be a transparent conductor. The device could yet further include a second contact formed adjacent the substrate.

Another advantageous embodiment could include a photonic device having a substrate, and a photonic diode comprising a first region proximate a top surface of the substrate, a second region proximate the first region, and an active region between the first and second regions, wherein the second region includes a surface adjacent the active region, the surface being generally parallel to the substrate top surface, and the second region includes at least one defect-trapping region spaced apart from the active region, the defect trapping region including a surface that extends away from the substrate top surface. The surface of the first diode region could be bonded to a handle substrate. An intermediate layer could be bonded to the handle substrate between the first diode region and the handle substrate. The handle substrate could include a conductor electrically connected to the first diode region. The device could further include a contact connected to the handle substrate and in electrical communication with the first diode region.

Another advantageous embodiment includes a method of making a photonic device. The method could include depositing a layer of a dielectric material onto a substrate, patterning two or more openings in the dielectric material to expose portions of the surface of the substrate, the two or more openings having an aspect ratio of at least 1, forming a bottom diode region by growing a compound semiconductor material that is lattice mismatched to the substrate in the two or more openings and allowing the compound semiconductor material to fill in the two or more openings and coalesce above the two or more openings to form a continuous layer, forming an active diode region on the bottom diode region, and forming a top diode region on the active diode region. The method could further include bonding a handle wafer to the top diode region and removing the substrate.

Another advantageous embodiment could provide for a photonic device having a bottom diode region including two or more threading dislocation trapping regions and comprised of a compound semiconductor material, an active diode region, a top diode region, a handle substrate, a first electrical contact in communication with the handle substrate, and a second electrical contact in communication with the bottom diode region.

Yet another advantageous embodiment could provide for a method of making a photonic device comprising depositing a layer of a dielectric material onto a substrate, patterning two or more openings in the dielectric material to expose portions

of the surface of the substrate, the two or more openings having an aspect ratio of at least 1, forming a bottom diode region by growing a compound semiconductor material that is lattice mismatched to the substrate in the two or more openings and allowing the compound semiconductor material to fill in the two or more openings and coalesce above the two or more openings to form a continuous layer, forming an active diode region on the bottom diode region, forming a top diode region on the active diode region, bonding a handle wafer to the top diode region, removing the substrate, removing the dielectric material, contacting a first electrical contact with the handle substrate, and contacting a second electrical contact with the bottom diode region.

Still another advantageous embodiment includes a method of making a structure comprising a semiconductor material bonded to a substrate. The method could include depositing a layer of a dielectric material onto a substrate, patterning two or more openings in the dielectric material to expose portions of the surface of the substrate, the two or more openings having an aspect ratio of at least 1, growing a layer of a compound semiconductor material that is lattice mismatched to the substrate in the two or more openings and allowing the semiconductor material to fill in the two or more openings and coalesce above the two or more openings to form a continuous layer, implanting ions into the semiconductor material to create a cleavage plane, bonding a handle substrate to the semiconductor material, and cleaving the layer of semiconductor material at the cleavage plane.

In some aspect, advantageous embodiments could provide for a chip including a plurality of discrete photonic devices thereon. The chip could include a substrate, a first dielectric material layer covering the substrate and having a plurality of openings therein having an aspect ratio of at least 1, a plurality of discrete photonic devices, each discrete photonic device comprising (i) a layer of semiconductor material that is mismatched to the substrate that occupies at least two openings and is coalesced above the occupied openings to form a single bottom diode region, (ii) an active diode region, and (iii) a top diode region, a second layer of dielectric material covering the plurality of discrete photonic devices, at least one top electrical contact; and at least one bottom electrical contact.

Yet another advantageous method could provide for a method of making a chip including a plurality of discrete photonic devices thereon comprising depositing a layer of a dielectric material onto a substrate, patterning a first set of openings in the dielectric material to expose portions of the surface of the substrate, the first set of openings having an aspect ratio of at least 1, forming a first bottom diode region by growing a layer of a semiconductor material that is lattice mismatched to the substrate in the first set of openings and allowing the semiconductor material to fill in the first set of openings and coalesce above the first set of openings to form a continuous layer, forming a first active diode region on the first bottom diode region, forming a first top diode region on the first active diode region, growing a layer of dielectric material to cover the first bottom diode region, first active diode region, and first top diode region, patterning a second set of openings in the dielectric material to expose portions of the surface of the substrate, the second set of openings having an aspect ratio of at least 1, forming a second bottom diode region by growing a layer of a semiconductor material that is lattice mismatched to the substrate in the second set of openings and allowing the semiconductor material to fill in the second set of openings and coalesce above the second set of openings to form a continuous layer, forming a second active diode region on the second bottom diode region, forming a second top diode region on the second active diode region, and growing a layer of dielectric material to cover the second bottom diode region, second active diode region, and second top diode region. The method could further include contacting a first electrical contact with the substrate, contacting a second electrical contact with first top diode region, and contacting a third electrical contact with the second top diode region.

What is claimed is:

1. A photonic device comprising:

a substrate;

a dielectric material including a first set of at least two openings and a second set of at least two openings, each of the openings in the first set and the second set exposing a portion of the substrate and having an aspect ratio of at least 1;

a first diode comprising:

a first bottom diode material comprising a first semiconductor material that is lattice mismatched to the substrate, and wherein the first semiconductor material occupies the first set of at least two openings and is coalesced above the first set of at least two openings;

a first top diode material; and

a first active diode region between the first top diode material and the first bottom diode material; and

a second diode comprising:

a second bottom diode material comprising a second semiconductor material that is lattice mismatched to the substrate, and wherein the second semiconductor material occupies the second set of at least two openings and is coalesced above the second set of at least two openings;

a second top diode material; and

a second active diode region between the second top diode material and the second bottom diode material;

wherein at least one of (i) the second bottom diode material is different from the first bottom diode material, (ii) the second active diode region comprises a material different from a material of the first active diode region, (iii) the second top diode material is different from the first top diode material, or (iv) a combination thereof.

2. The photonic device of claim **1** wherein the substrate is selected from the group consisting of silicon, sapphire, and silicon carbide.

3. The photonic device of claim **1** wherein the substrate is a single crystal silicon wafer having a crystal orientation of (111) or (100).

4. The photonic device of claim **1** wherein the first active diode region comprises a p-n junction formed by a junction of the first top and first bottom diode materials.

5. The photonic device of claim **1** wherein the first active diode region comprises a material different from the first top and first bottom diode materials, and the first active diode region forms an intrinsic region of a p-i-n junction formed between the first top and first bottom diode materials.

6. The photonic device of claim **1** wherein the first active diode region comprises multiple quantum wells formed between the top and bottom diode materials.

7. The photonic device of claim **1** wherein the dielectric material comprises a material selected from the group consisting essentially of silicon dioxide, silicon nitride, silicon oxynitride, oxides of hafnium, silicates of hafnium, oxides of zirconium, silicates of zirconium, and combinations thereof.

8. The photonic device of claim **1** wherein each of the openings of the first set and second set opening is a hole having an aspect ratio of at least 1 in two perpendicular axes.

9. The photonic device of claim **1** wherein the first semiconductor material comprises a material selected from the

group consisting essentially of a Group III-V compound, a Group II-VI compound, a Group IV alloy, and combinations thereof.

10. The photonic device of claim **1** wherein the first bottom diode material includes an n-type dopant and the first top diode material includes a p-type dopant.

11. The photonic device of claim **1** further comprising a contact formed over the first top diode material.

12. The diode of claim **11**, further comprising a second contact formed adjacent the substrate.

13. A photonic device comprising:

a substrate; and

a photonic diode comprising a first region proximate a top surface of the substrate, a second region proximate the first region, and an active region between the first and second regions, wherein

the second region includes a surface adjacent the active region, the surface being generally parallel to the substrate top surface, and

the second region includes at least one defect-trapping region spaced apart from the active region, the defect trapping region being distally located from the substrate top surface, the first region being between the defect trapping region and the substrate top surface.

14. The photonic device of claim **13** wherein a surface of the first region is bonded to a handle substrate.

15. The photonic device of claim **14** wherein an intermediate layer is bonded to the handle substrate between the first region and the handle substrate.

16. The photonic device of claim **14** wherein the handle substrate includes a conductor electrically connected to the first region.

17. The photonic device of claim **14** further comprising a contact connected to the handle substrate and in electrical communication with the first region.

18. A photonic device comprising:

a substrate;

a dielectric material including a first set of at least two openings and a second set of at least two openings, each of the openings in the first set and the second set exposing a portion of the substrate and having an aspect ratio of at least 1;

a first diode comprising:

a first bottom diode material comprising a first semiconductor material that is lattice mismatched to the substrate, and wherein the first semiconductor material occupies the first set of at least two openings and is coalesced above the first set of at least two openings;

a first top diode material; and

a first active diode region between the first top diode material and the first bottom diode material; and

a second diode comprising:

a second bottom diode material comprising a second semiconductor material that is lattice mismatched to the substrate, and wherein the second semiconductor material occupies the second set of at least two openings and is coalesced above the second set of at least two openings;

a second top diode material; and

a second active diode region between the second top diode material and the second bottom diode material;

wherein the first diode and the second diode are adjacent but not in physical contact, and a separation region is between the first bottom diode material and the second bottom diode material.

19. The photonic device of claim **18**, wherein at least one of (i) the second bottom diode material is different from the first bottom diode material, (ii) the second active diode region comprises a material different from a material of the first active diode region, (iii) the second top diode material is different from the first top diode material, or (iv) a combination thereof.

20. The photonic device of claim **18**, wherein the separation region comprises a dielectric material.

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