

Petition for *Inter Partes* Review of USP 8,993,384

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re *Inter Partes* Review of:)
U.S. Patent No. 8,993,384)
Issued: Mar. 31, 2015)
Application No.: 13/913,511)
Filing Date: Jun. 9, 2013)

For: **Semiconductor Device And Fabrication Method Thereof**

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,993,384**

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Exhibit List

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1001	U.S. Patent No. 8,993,384 (“’384 patent”).
1002	Prosecution History of U.S. Patent No. 8,993,384.
1003	Declaration of Dr. Jack Lee, Ph.D.
1004	U.S. Patent No. 9,166,022 B2 (“Xu”).
1005	U.S. Patent 2012/0091538 A1 (“Lin”).
1006	U.S. Patent Pub. No. 2005/0148137 A1 (“Brask”).
1007	T. Ghani et al, <i>A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45 Nm Gate Length Strained Silicon CMOS Transistors</i> , IEEE International Electron Devices Meeting 2003, pp. 11.6.1-11.6.3 (2003).
1008	Excerpts from N. Collaert, <i>CMOS Nanoelectronics</i> (2012).
1009	A. Veloso et al., <i>Gate-Last vs. Gate-First Technology for aggressively scaled EOT Logic/RF CMOS</i> , Symposium on VLSI Technology – Digest of Technical Papers, pp. 34-35, (2011).
1010	M. Quirk and J. Serda, <i>Semiconductor Manufacturing Technology Instructor’s Manual</i> (2001) (archived Sep. 28, 2007).
1011	Excerpts from S. P. Muraka et al., <i>Interlayer Dielectrics for Semiconductor Technologies</i> (2003).
1012	Excerpts from D. Neaman, <i>Semiconductor Physics and Devices</i> (2012).
1013	D. Hisamoto et al., <i>Folded-channel MOSFET for deep-sub-tenth micron era</i> , International Electron Devices Meeting 1998 – Technical Digest, pp. 1032-1034, (1998).
1014	X. Huang et al., <i>Sub 50-nm FinFET: PMOS</i> , International Electron Devices Meeting 1999 – Technical Digest, pp. 67-70, (1999).
1015	D. Hisamoto et al., <i>FinFET – a self-aligned double-gate MOSFET scalable to 20 nm</i> , IEEE Transactions on Electron Devices, Vol. 47, No. 12, pp. 2320-2325 (2000).
1016	J. Markoff, <i>Intel Increases Transistor Speed by Building Upward</i> , New York Times (2011).

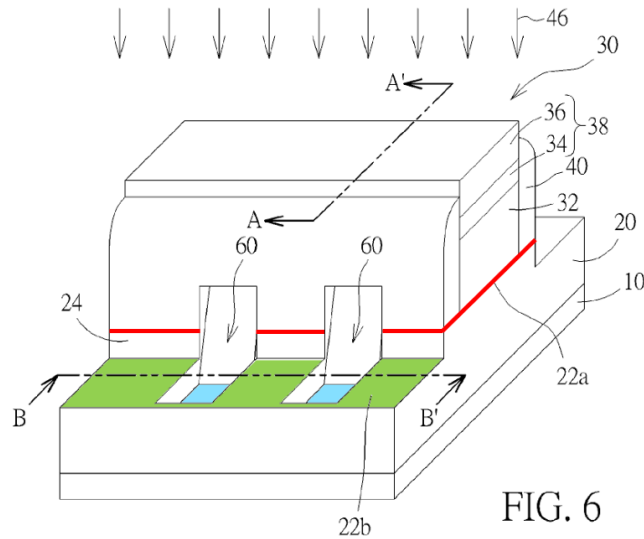
1017	Intel, <i>Intel's Revolutionary 22 nm Transistor Technology</i> (2011).
1018	A. Shimpi, <i>Intel Announces first 22nm 3D Tri-Gate Transistors, Shipping in 2H 2011</i> , AnandTech (2011) (archived May 18, 2011).
1019	K. Mistry et al., <i>A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging</i> , 2007 IEEE International Electron Devices Meeting, pp. 247-250, (2007)
1020	U.S. Patent No. 7,525,160 B2 (“Kavalieros”)
1021	S. Thompson et al., <i>Key Differences for Process-Induced Uniaxial vs. Substrate-Induced Biaxial Stressed Si and Ge Channel MOSFETs</i> , Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 221-224 (2004).
1022	C. Auth et al., <i>45nm High-k + Metal Gate Strain-Enhanced Transistors</i> , 2008 Symposium on VLSI Technology, pp. 128-129 (2008)
1023	S. Mayuzumi et al., <i>High-Performance Metal/High-k n- and p-MOSFETs With Top-Cut Dual Stress liners Using Gate-Last Damascene Process on (100) Substrates</i> , IEEE Transactions on Electron Devices, Vol. 56, No. 4, pp. 620-626, (2009)
1024	Excerpts from G. May and S. Sze, <i>Fundamentals of Semiconductor Fabrication</i> (2004).
1025	Excerpts from S. Wolf, <i>Microchip Manufacturing</i> , (2004).
1026	<i>Curriculum Vitae</i> of Dr. Jack Lee, Ph.D.
1027	Declaration of Stephen M. Bradley

I. Introduction

Taiwan Semiconductor Manufacturing Company Limited (“TSMC” or “Petitioner”) requests *inter partes* review of claims 1-9 (“Challenged Claims”) of U.S. Patent No. 8,993,384 (Ex. 1001, “’384 patent”).

The ’384 patent relates to semiconductor devices including a “fin structure” that “protrudes from the surface of the substrate.” Ex. 1001 at 1:53-55. The fin structure enables the formation of a “multi-gate MOSFET” (metal-oxide-semiconductor field effect transistor) such as a FinFET (fin field effect transistor). Ex. 1001 at 3:49-51, 1:13-14. As explained by TSMC’s expert Dr. Jack Lee, however, TSMC invented FinFETs in 1999—more than ten years before the ’384 patent’s effective filing date—and continued to innovate over many years to improve FinFET manufacturing and the resultant devices. *See* Ex. 1003 at ¶¶ 38, 40.

Specifically, the ’384 patent describes a fabrication method for FinFET transistors comprising forming “a fin structure, an isolation structure, a gate structure and an epitaxial structure.” Ex. 1001 at Abst. The ’384 patent claims methods for fabricating FinFETs where the “fin” is recessed and the “isolation structure” is etched. *Id.* at cl. 1. According to the ’384 patent, the depth of the recessed fin is deeper than that of the etched isolation structure. *Id.* This is shown in Figure 6 of the ’384 patent as annotated below, with the recesses shown in blue and the etched surface shown in green.



But before the '384 patent was filed, FinFET transistors fabricated by forming a fin structure, an isolation structure, a gate structure, and an epitaxial structure were already well-known. Ex. 1003 at ¶ 40. In fact, before the '384 patent was filed, TSMC had already filed patent applications describing FinFET transistors fabricated by recessing fins and etching isolation structures such that the depth of the recessed fins is “deeper” than the depth of the etched isolation structures—for example, in U.S. Patent No. 9,166,022 (Ex. 1004, “Xu”) and U.S. Patent Pub. No. 2012/0091538 (Ex. 1005, “Lin”) discussed in greater detail below.

This Petition therefore requests *inter partes* review of challenged claims 1-9 and demonstrates their unpatentability.

II. Identification of Challenges (37 C.F.R. § 42.104(b))

Under Rules 42.22(a)(1) and 42.104(b)(1)-(2), Petitioner challenges claims 1-9 (“Challenged Claims”) of the '384 patent and requests each Challenged Claim be

cancelled. The effective filing date of the Challenged Claims is no earlier than June 9, 2013.

A. Prior Art Patents and Printed Publications Relied Upon

Petitioner relies upon the following patents and printed publications:

1. U.S. Patent No. 9,166,022 (“Xu”), issued on October 20, 2015 and filed on November 2, 2010, is prior art to the ’384 patent under at least AIA 35 U.S.C. § 102(a)(2).
2. U.S. Patent Pub. No. 2012/0091538 (“Lin”), filed on October 13, 2010 and published on April 19, 2012, is prior art to the ’384 patent under at least AIA 35 U.S.C. §§ 102(a)(1) and 102(a)(2).
3. U.S. Patent Pub. No. 2005/0148137 (Ex. 1006, “Brask”), filed on December 30, 2003 and published on July 7, 2005, is prior art to the ’384 patent under at least AIA 35 U.S.C. §§ 102(a)(1) and 102(a)(2).

B. Grounds for Challenge

This Petition, supported by the declaration of Dr. Jack C. Lee (Ex. 1003), presents the following grounds of unpatentability:

Ground 1A: Claims 1-9 are obvious under 35 U.S.C. § 103 over Xu in view of the knowledge of a POSITA.

Ground 1B: Claims 4 and 9 are obvious under 35 U.S.C. § 103 over Xu in view Brask.

Ground 2A: Claims 1-3 and 5-8 are obvious under 35 U.S.C. § 103 over Lin in view of the knowledge of a POSITA.

Ground 2B: Claims 4 and 9 are obvious under 35 U.S.C. § 103 over Lin in view of Brask.

III. Background

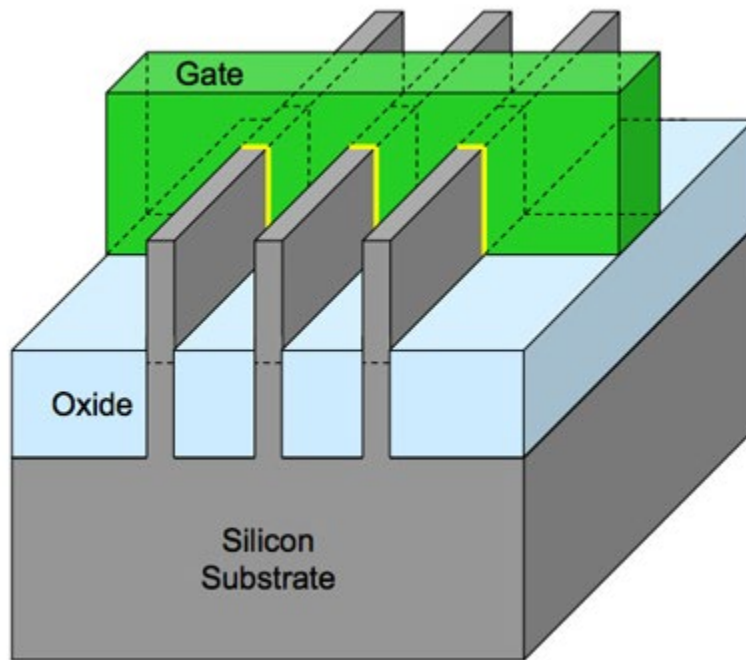
A. Technology Background

The '384 patent relates to semiconductor devices. Ex. 1003 at ¶ 34. Semiconductor devices are generally manufactured on silicon wafers and comprise billions of transistors. *Id.*

Transistors are the fundamental building blocks for semiconductor chips. *Id.* at ¶ 35. Each transistor operates as a switch that either allows or blocks the flow of electrical current. *Id.* By combining thousands, or even billions, of transistors together, circuit designers can implement electronic hardware like processors used in computers, mobile phones and other semiconductor devices. *Id.*

A typical transistor has three main components: a “source,” a “drain,” and a “gate.” *Id.* at ¶ 36. When the transistor is “off,” no current flows between the source and drain. *Id.* When a proper voltage is applied to the “gate,” the transistor is turned on, allowing current to flow through a “channel region” between the source and drain. *Id.*

Around 1999, Chenming Hu, who served as TSMC's CTO, introduced a new type of transistor that he called "FinFETs." Ex. 1003 at ¶ 38 (citing Ex. 1013, Ex. 1014, Ex. 1015). FinFETs are so named because the transistor channel is formed in a thin vertical "fin" of silicon protruding from the substrate. *Id.* Dr. Hu later received the National Medal of Technology and Innovation for his invention of FinFETs. *Id.* A representative FinFET structure is shown below:



Ex. 1017 at 7. As shown above, the gate overlays multiple surfaces of the fin, allowing for more effective control of the channel region between the source and drain. Ex. 1003 at ¶ 38. FinFET transistors on the wafer are separated by dielectric materials on the wafer. *Id.*

By 2004, it was already known that transistor performance is improved by introducing strain into the transistor channel by using epitaxial techniques. Ex. 1003 at ¶ 39. For example, silicon germanium (or “SiGe”) was commonly used in the source and drain regions to induce compressive strain, particularly for pMOS devices, thereby improving carrier mobility and drive current. *See id.* (citing Ex. 1007 at 978-980; Ex. 1019 at 247-250).

Thus, long before the priority date of the ’384 patent, FinFET transistors fabricated by forming fin structures, isolation structures, gate structures, and epitaxially formed source/drains were already well-known. Ex. 1003 at ¶ 40. In fact, by 2013, the priority date of the ’384 patent, Intel had already commercialized FinFET-based products with this architecture. *Id.* (citing Exs. 1016, 1017, 1018). TSMC, likewise, had developed and held numerous patents on FinFET transistors featuring these same fabrication elements, as discussed in greater detail below with respect to the Xu and Lin references. *Id.*

B. The ’384 Patent (Ex. 1001)

The ’384 patent is titled “Semiconductor Device and Fabrication Method Thereof.” The ’384 patent was filed on June 9, 2013 and the ’384 patent does not claim priority to any earlier date. It describes a method of fabricating FinFET transistors that include “a fin structure, an isolation structure, a gate structure and an epitaxial structure.” Ex. 1001 at Abst. The ’384 patent issued to United

Microelectronics Corp., a Taiwanese semiconductor manufacturer, but was subsequently assigned to Marlin Semiconductor, a non-practicing entity that is asserting other patents against TSMC and its customers.

Figures 1 through 3 of the '384 patent depict the fabrication of a conventional FinFET device, which was known by the priority date. As shown in Figure 3, the FinFET comprises “a plurality of fin structures 12” (light blue), a “gate structure” 30 (gold) formed over the fins 12, and “a spacer 40” (dark blue) formed “on the sidewalls of the gate structure 30.” *Id.* at 3:20-22, 5:4-8. Figure 3 also depicts “isolation structure 20” (magenta) formed on the substrate 10. *Id.* at 3:60-61.

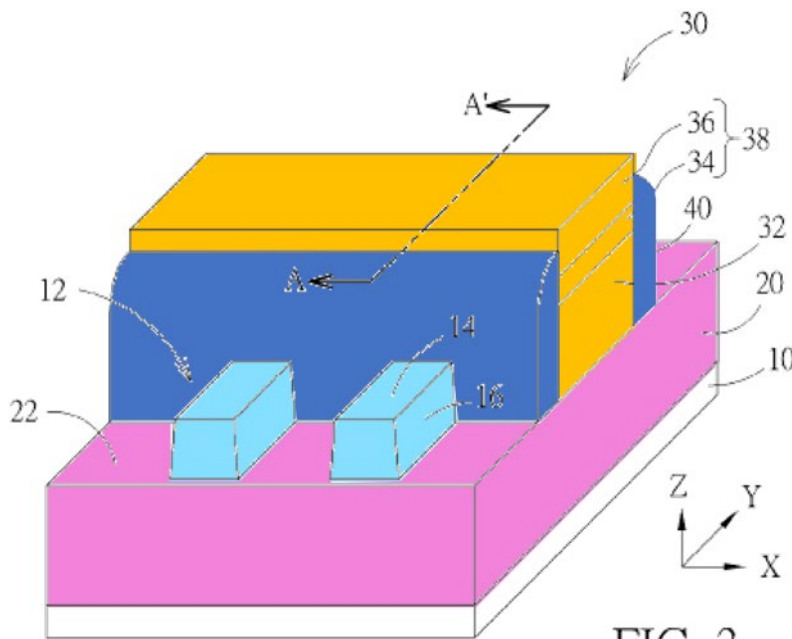


FIG. 3

After forming the gate structure 30, “a first etching process 42 ... may be carried out to selectively remove” the exposed portions of “isolation structure 20,” resulting in the structure shown in Figure 5. *Id.* at 5:26-37.

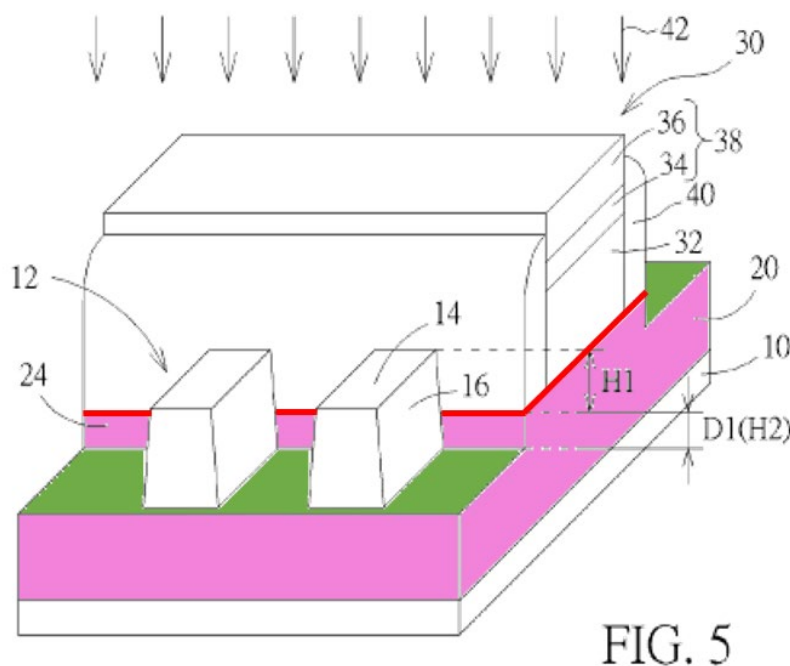


FIG. 5

Figure 5 illustrates that, due to the etching process, “[t]here is a height difference H2 between the first top surface 22a [red] and the second top surface 22b [green]” of the isolation structure (magenta) depicted as “D1” in Figure 5. *Id.* at 5:42-48.

In addition, the fin structures 12 are etched and “a recess 60 may be formed in each fin structure 12.” *Id.* at 5:56-60. An “epitaxial growth process” is then “carried out in order to grow an epitaxial structure 60 [*sic.* 66] in each corresponding recess 60.” *Id.* at 6:43-50. The recess is shown below in blue (Figure 6) and the epitaxial structures are shown below in purple (Figure 9).

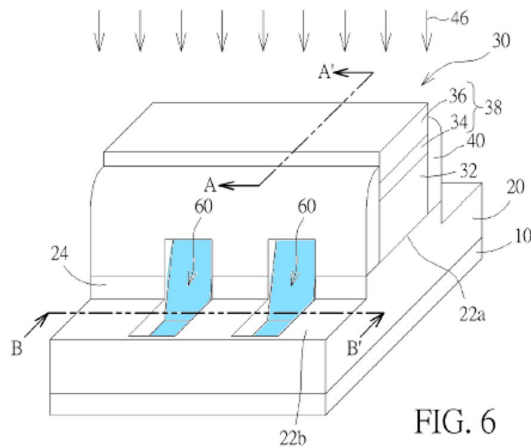


FIG. 6

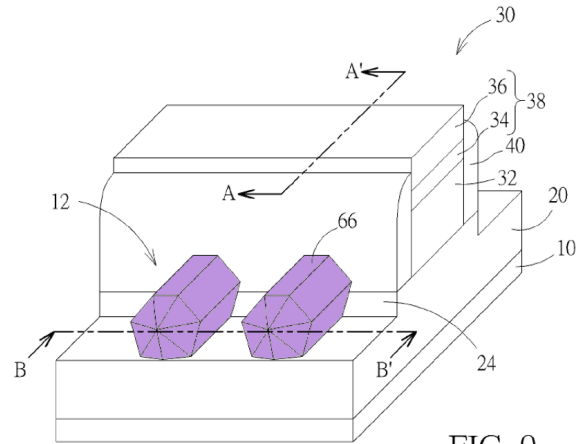


FIG. 9

C. Prosecution History

The Challenged Claims were allowed after one non-final rejection. Specifically, the Examiner rejected the pending claims based on U.S. Patent 7,525,160 to Kavalieros *et al.* (“Kavalieros”, Exhibit 1020). Ex. 1002 at 88. In response, the Applicant amended pending claim 11 (the only independent claim) to recite that the step of etching the isolation structure be performed “after the step of forming the gate structure.” *Id.* at 107. The claims were subsequently allowed, with the Examiner “agree[ing] with applicant’s arguments, with regard to the amended claim.” *Id.* at 118.

D. Person of Ordinary Skill in the Art

A POSITA would have had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as, for example, in integrated circuit device (or transistor) design and/or manufacturing, as of June 9,

2013. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for less formal education.

E. Claim Construction

The prior art relied on in this Petition discloses the subject matter of the challenged claims under any reasonable construction, including their plain meaning.¹

IV. Ground 1A: Claims 1-9 Are Obvious Over Xu In View Of The Knowledge Of A POSITA

A. Overview of Xu

Xu was filed on November 2, 2010 by TSMC. *See* Ex. 1004. Because Xu is in the same field (FinFETs) and reasonably pertinent to a problem the '384 patent purports to address (FinFET fabrication), Xu is analogous art. *See* Ex. 1001 at Abstr., 3:39-54; Ex. 1004 at Abstr.; Ex. 1003 at ¶ 54. Xu describes “a FinFET device and method for fabricating a FinFET device.” *Id.* at Abst. “FIGS. 2-6 provide various perspective views of a FinFET device 100, in portion or entirety, at various stages of fabrication according to the method 10 of FIG. 1.” *Id.* at 2:51-53. “The term FinFET device refers to any fin-based transistor.” *Id.* at 2:53-55.

¹ Petitioner reserves the right to argue alternative constructions in other proceedings, and where such a defense is available, that the claims are indefinite.

Figure 2 of Xu depicts a “fin structure 115A and 115B [blue] that extends from a substrate 110.” *Id.* at 3:9-12. Figure 2 also shows “[i]solation features 130” that can be “shallow trench isolation (STI) structures” (magenta) that “surround the fin structure 115A and 115B.” *Id.* at 3:54-58. The FinFET device also includes a “gate structure 150” (gold). *Id.* at 3:66-4:3.

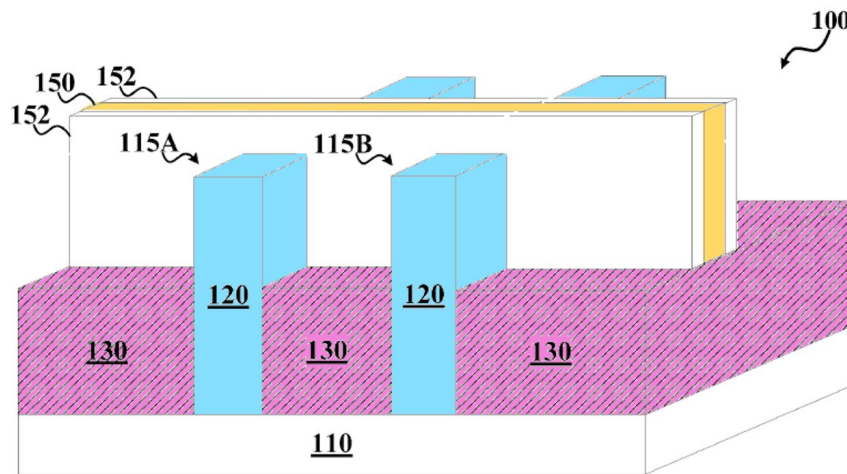


FIG. 2

After forming the gate structure, as shown in Figure 3, “a process is performed to recess the isolation features 130” using an “etching process.” *Id.* at 4:54-56. The “etching process selectively etches the isolation features 130.” *Id.* at 4:58-61. The process creates a height difference (or depth) between a top surface (red) under the gate and a top surface (green) to the sides of the gate as shown below. Ex. 1003 at ¶ 56.

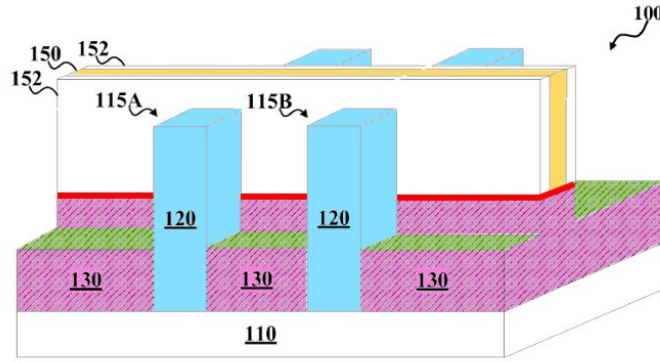


FIG. 3

Next, as shown in Figure 4, a “fin template 135” (purple) is formed by “merging the fins 120 together” via “epitaxially (epi) growing a semiconductor material on exposed portions of the fins 120 in the source and drain regions of the fin structure 115A and 115B.” Ex. 1004 at 5:1-15.

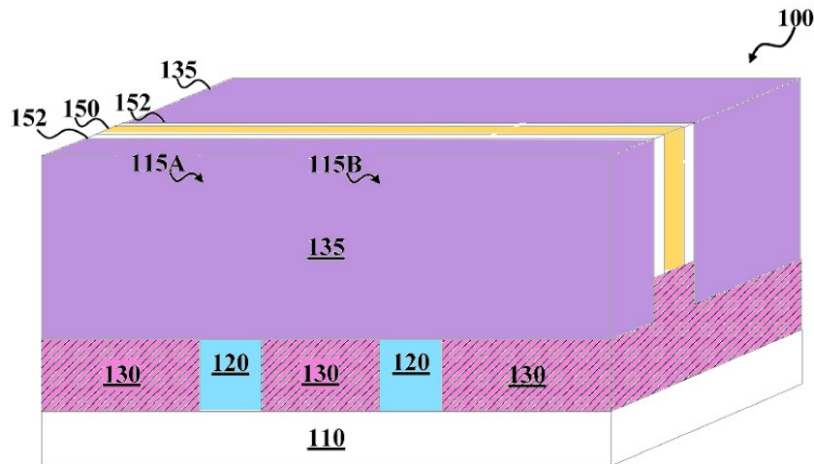


FIG. 4

The resulting fin template 135 (purple) and fins 120 (blue) are recessed in Figure 5 and, as shown in Figure 6, another “semiconductor material 160 [purple] is epitaxially grown over the fin template 135,” which “generates channel strain.” *Id.* at 5:34-35, 5:49-55.

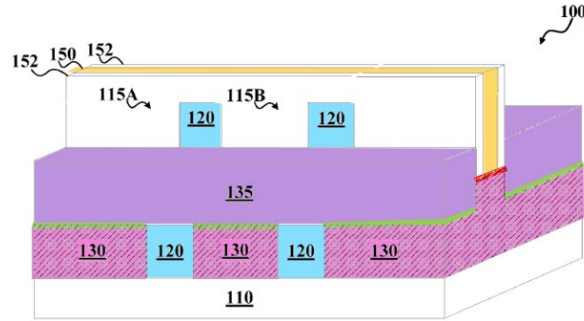


FIG. 5

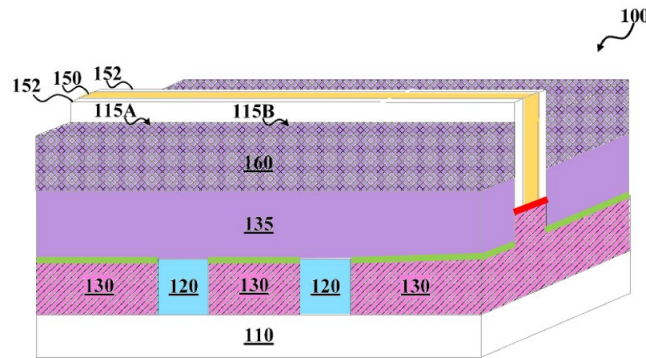


FIG. 6

Xu teaches that “[t]he semiconductor material 160 may be referred to as raised source and drain features of the source and drain regions of the fin structure 115A and 115B,” and that the “fin template 135 in the source and drain regions of the fin structures 115A and 115B may also be considered as part of the raised source and drain features.” *Id.* at 6:2-7.

Xu also discloses a second embodiment where “an etching process” removes portions “of the fin structures 215A and 215B,” resulting in recessed fins as shown below. *Id.* at 7:58-61, 10:34-36; Fig. 7 (“[c]ompletely remove the second material portion [230] from the source and drain regions of the first and second fin structure”).

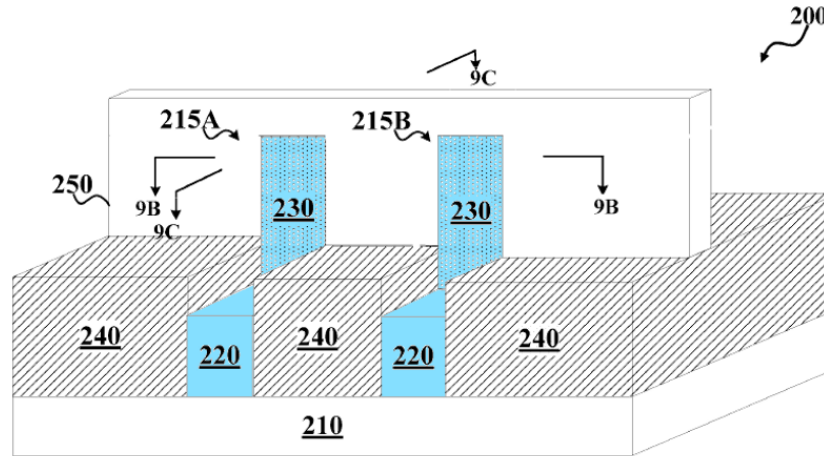


FIG. 9A

After that, the epitaxial materials (*i.e.*, the “fin template”) “may be formed by a process similar to that described above with reference to FIG. 5” (*i.e.*, the first embodiment discussed above) to fill the recesses. *Id.* at 11:2-4. Xu contemplates that a fabrication method can include both etching the isolation structure as well as recessing the fin structure. *See, e.g., id.* at 16:5-17:10 and claim 19.

B. Claim 1

1. 1[pre]: A fabrication method for a semiconductor device:

The preamble is not limiting. Regardless, Xu discloses and renders obvious a fabrication method for a semiconductor device. Ex. 1003 at ¶ 75. For example, Xu discloses “[a] FinFET device and method for fabricating a FinFET device,” which is a semiconductor device. *See, e.g.,* Ex. 1004 at Abst.; *id.*, 2:51-53 (“FIGS. 2-6 provide various perspective views of a FinFET device 100, in portion or entirety, at various stages of fabrication according to the method 10 of FIG.1.”). Figure 1, reproduced below, depicts a “flow chart of a method for fabricating a fin-like field

effect transistor (FinFET) device according to aspects of the present disclosure.” *Id.* at 1:49-51; Fig. 1.

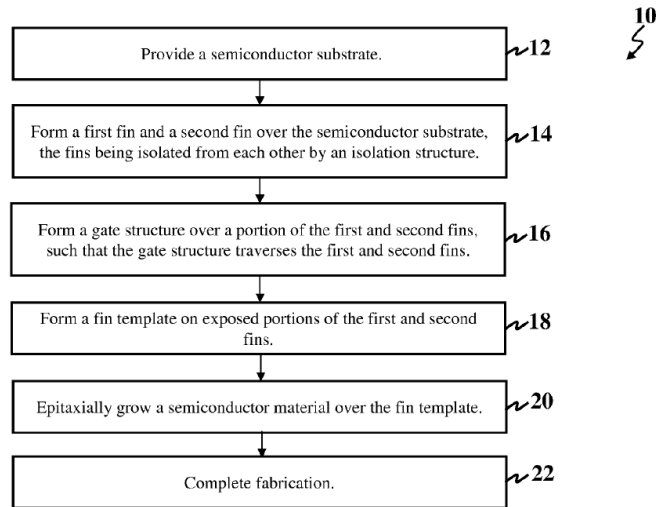


FIG. 1

Xu discloses a second fabrication method, illustrated in Figure 7, below, that includes a step 38 of forming a recess in the fin structure. *Id.* at Fig. 7.

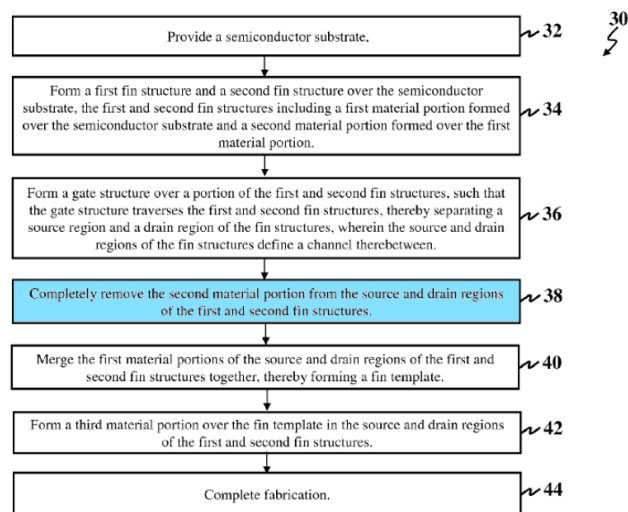


FIG. 7

Xu further discloses fabrication methods that incorporate the various steps of Figures 1 and Figures 7 together, including etching the isolation layer and forming

recesses in the fin structure, as discussed in greater detail below. *See* Ex. 1004 at 16:5-17:10 and claim 19.

2. 1[a]: forming a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 78. For example, the first step of Xu’s method is “[f]orm[ing] a first fin and a second fin over the semiconductor substrate, the fins being isolated from each other by an isolation structure.” Ex. 1004 at Fig. 1.

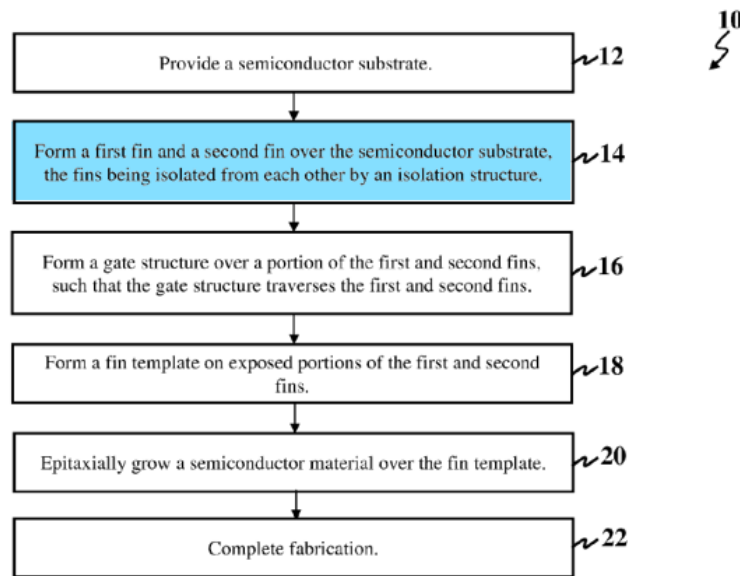


FIG. 1

Xu discloses that “FinFET device 100 includes fin structure 115A and 115B that extend from the substrate 110.” *Id.* at 3:9-10. Figure 2, for example, illustrates substrate 110 and fin structures 115A and 115B (annotated in blue) protruding from

the top surface of substrate 110 and comprising a top surface and two side surfaces.

Id. at Fig. 2.

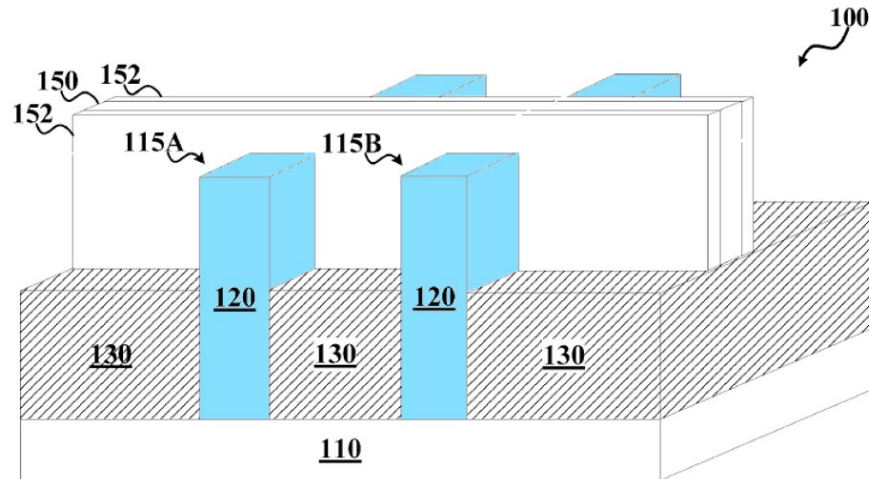


FIG. 2

3. 1[b]: forming an isolation structure to surround the fin structure;

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 80. For example, in the second step (14) of fabrication Xu Figure 1 specifies that the formed fins are “isolated from each other by an isolation structure.” Ex. 1004 at Fig. 1. The isolation structure is shown, for example, as isolation features 130 (magenta) in Figure 2 (below) and surround the fins structures 120 (blue). *Id.* at 3:54-58.

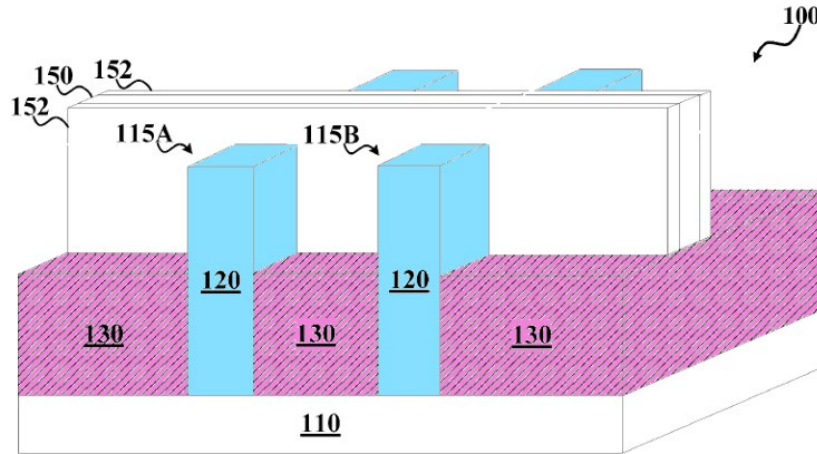


FIG. 2

According to Xu, “[i]solation features 130, such as shallow trench isolation (STI) structures, *surround the fin structures* 115A and 115B (in the depicted embodiment, the fins 120), isolating the fins 120 from each other and other not-illustrated integrated circuit devices.” *Id.* at 3:54-58 (emphasis added).

4. 1[c]: forming a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure, and covering a portion of the isolation structure;

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 82. For example, the third step (16) of Xu Figure 1 includes “[f]orm[ing] a gate structure over a portion of the first and second fins, such that the gate structure traverses the first and second fins.” Ex. 1004 at Fig. 1.

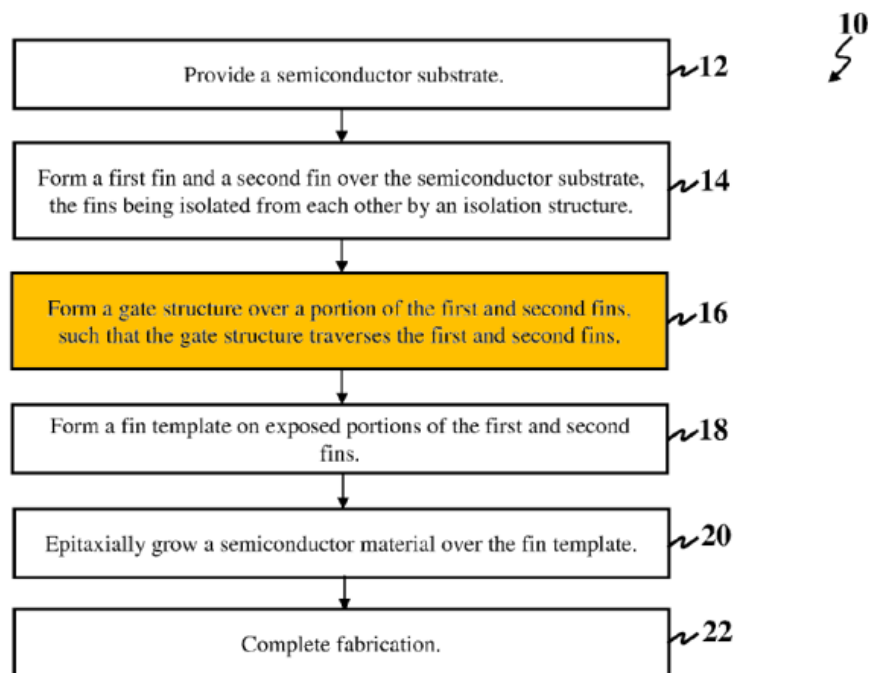


FIG. 1

Figure 2, for example, illustrates the gate structure 150 (gold) overlaying the top surface and two side surfaces of a portion of fins 120 (blue) and covering a portion of the isolation structure 130 (magenta). *Id.* at Fig. 2; *id.* at 3:66-4:1.

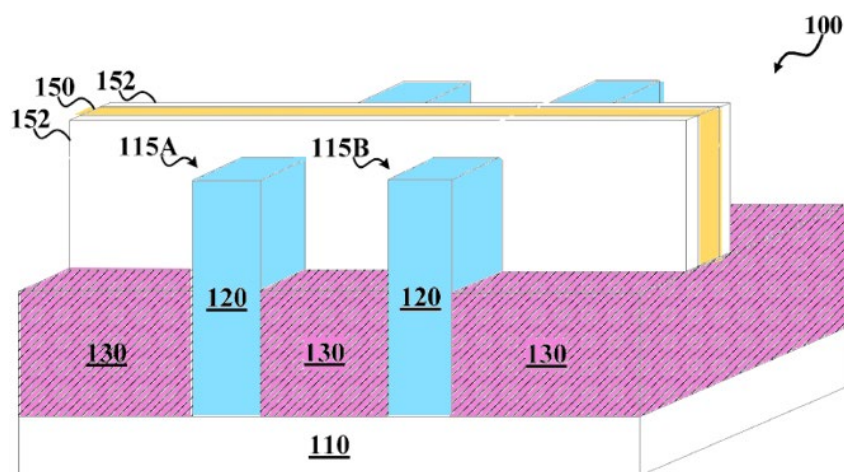


FIG. 2

5. **1[d]: after the step of forming the gate structure, etching the isolation structure exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth;**

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 84. For example, Xu discloses that “an etching process is applied to recess the isolation features 130” and, as shown in Figure 3, the top surface (green) of the isolation structure 130 (magenta) is etched down to a first depth. Ex. 1004 at 4:54-56.

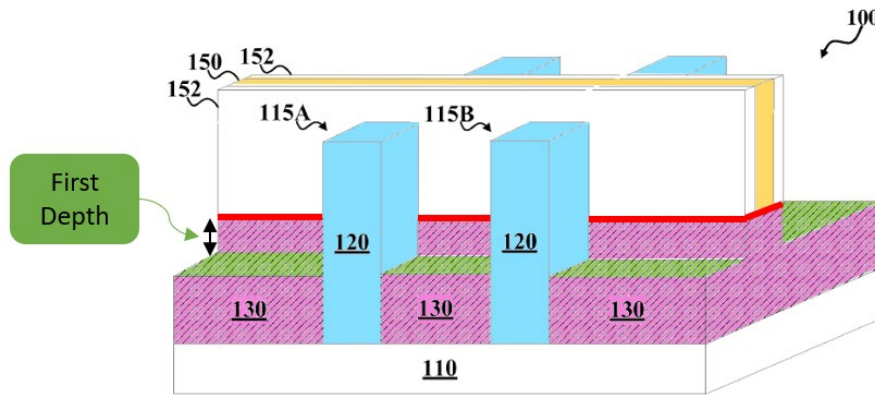


FIG. 3

The recessing step is performed after the step of forming the gate structure. Ex. 1004 at Figs. 2-3, 4:39-67. As shown in Figure 2 (below), the gate structure (gold) is first formed over an isolation structure 130 (magenta) that has not yet been etched. Ex. 1003 at ¶ 85. In the next step (Figure 3), the isolation structure 130 (magenta) is etched after the gate structure is formed, resulting in the exposed top surface (green) of the isolation structure 130 (magenta) etched down to a first depth.

Id.

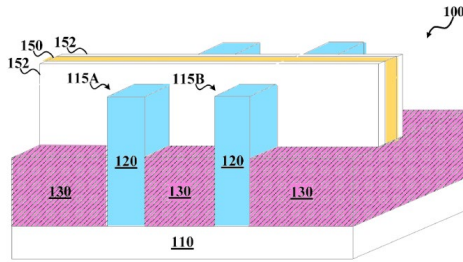


FIG. 2

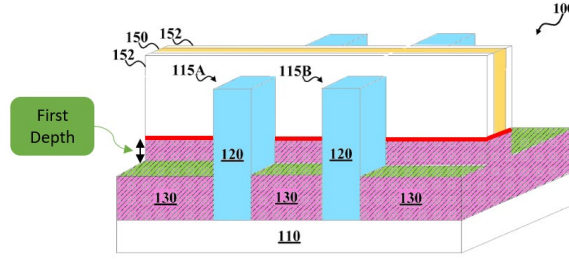


FIG. 3

Further, Xu explains that etching of the isolation structure is performed “selectively” so that it “avoid[s] etching the silicon nitride spacers 152.” Ex. 1004 at 4:58-61. Because the spacers are formed after the gate structure is formed (*id.* at 4:39-40), this further confirms that the isolation structures 130 are etched “after the step of forming the gate structure” as claimed. Ex. 1003 at ¶ 86.

6. 1[e]: forming a recess in the fin structure at a side of the gate structure; and

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 87. For example, Xu Figure 7 discloses removing material from a fin structure:

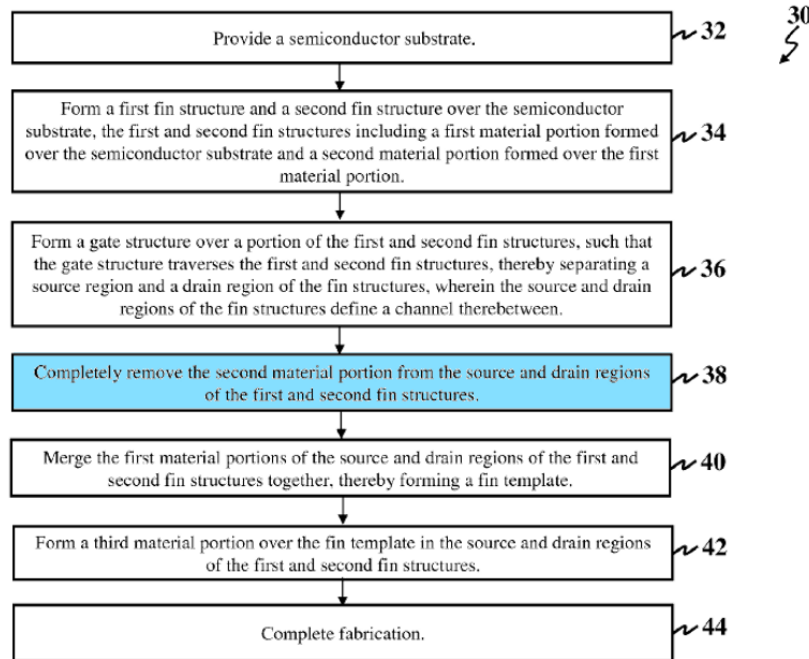


FIG. 7

Specifically, Xu discloses a second embodiment of the FinFET device 200 where the “fin structures 215A and 215B” have two portions 220 and 230 (as shown in Figure 8A) and **“an etching process completely removes the fin portions 230 from the source and drain regions of the fin structures 215A and 215B, exposing the fin portions 220”** (as shown in Figure 9A). Ex. 1004 at 7:58-61, 10:34-36; Fig. 7 (“[c]ompletely remove the second material portion [230] from the source and drain regions of the first and second fin structure”). The result of these steps is the creation of a recess in the fin structure at the side of the gate structures, as shown in Figures 8A and 9A.

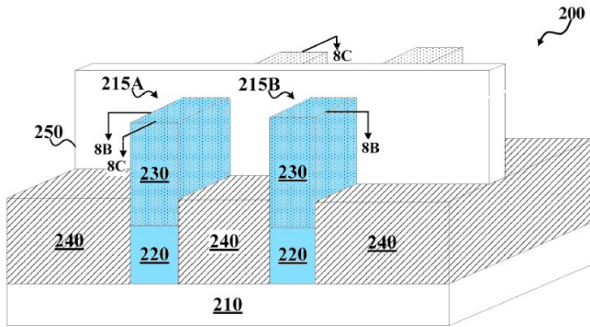


FIG. 8A

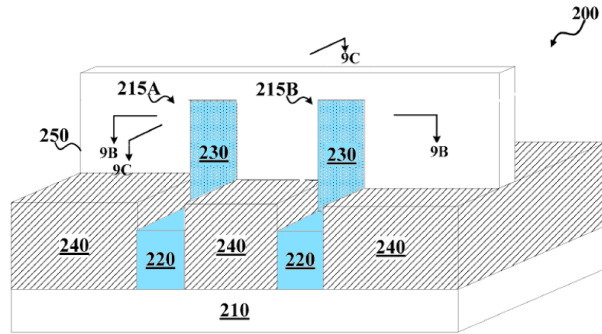


FIG. 9A

This etching process forms recesses in fin structures 215A, 215B at a side of the gate—*i.e.*, either the source or drain region. *Id.*; Ex. 1003 at ¶ 88.

It would have been obvious to a POSITA to combine the fin-recessing step with Xu's first embodiment. Ex. 1003 at ¶ 89. As Xu discloses, it was known in the art, and a POSITA would have understood, that "strained source/drain features [] enhance carrier mobility and improve device performance." Ex. 1004 at 1:28-29; Ex. 1003 at ¶ 89. Xu explains that forming recesses in the fin structure is beneficial in that it allows for optimization of this strain, specifically noting that "by controlling source and drain trench depth"—which is dictated by the depth of the recess—"strain for both PMOS and NMOS FinFET devices can be achieved and optimized" and "different types of strain can be achieved." Ex. 1004 at 15:56-66. "Accordingly, the trench depth can be tuned to independently optimize performance of each FinFET device in an integrated circuit device." *Id.* at 15:67-16:2. Thus, a POSITA would have understood and found obvious that recessing "fins 120" of Xu's first embodiment will result in "achiev[ing] and optimiz[ing]" strain. *Id.* at 15:56-60,

15:67-16:2; Ex. 1003 at ¶ 89. Xu therefore expressly recognizes an advantage or expected beneficial result that would have motivated a POSITA to combine the recessing of the fins of the second embodiment with Xu's first embodiment. Ex. 1003 at ¶ 89.

Moreover, after describing the subject matter illustrated in Figs. 1-16C, Xu summarizes the invention in a way that suggests combining steps of Xu's first embodiment with steps of Xu's second embodiment in a single embodiment. Ex. 1004 at 16:5-44, 16:45-17:10; Ex. 1003 at ¶ 91. As Xu explains, its "disclosure provides for **many** different embodiments." Ex. 1004 at 16:5-6 (emphasis added). For example, Xu discloses a method (Ex. 1004 at 16:7-26) that can include "etching back the isolation structure" as in Xu's first embodiment. Ex. 1004 at 16:17-19. Following this description, Xu provides alternative modifications to this method. *Id.* at 16:27-44. Specifically Xu discloses "[t]he method may include completely removing the second material portion from the source and drain regions of the fins before forming the fin template." *Id.* at 16:40-43. These techniques correspond to the fin-recessing steps described in Xu's second embodiment, as shown in Figures 7, 8A and 9A. Ex. 1003 at ¶ 91. *See also* Ex. 1004 at 16:45-17:10 (describing "another embodiment" that may include "etching back the isolation structure" and "removing a portion of the first and second fin structures before epitaxially growing the first semiconductor material" which may include "completely removing the

second material portion”). Xu’s express disclosure of using these steps together suggests and renders obvious the combination of the first and second embodiments. Ex. 1003 at ¶ 91. And, as the Federal Circuit has found, “[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.” *Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009). This is especially true where the reference itself suggests such a combination. Ex. 1003 at ¶ 91.

Additionally, a POSITA would have had a reasonable expectation of success in making this combination. Ex. 1003 at ¶ 92. Xu discloses exemplary etch processes which can be used to perform the step of recessing the fin. Ex. 1004 at 10:36-61; 13:44-55. A POSITA would have understood these to be conventional processes that could be applied to the fins of Xu’s first embodiment in order to control a recess depth. Ex. 1003 at ¶ 92.

Put differently, Xu’s first embodiment is a known fabrication method ready for improvement by applying the known technique from the second embodiment of forming a trench or recess in the fin, which yields the predictable result taught by Xu of “provid[ing] different starting substrates for forming the fin templates, such that different types of strain can be achieved.” Ex. 1004 at 15:64-16:2; Ex. 1003 at ¶ 94.

Claim 19 of Xu, dependent from independent claim 11, further reinforces the obviousness of such a combination. Ex. 1003 at ¶ 95. Like the portions of the specification described above, dependent Claim 19 sets forth a method that combines “completely removing the second material portion from the source and drain regions of the fins” (Ex. 1004 at 20:16-21) with “recessing the isolation structure by removing a portion of the isolation structure” (*id.* at 19:8-10, independent claim 11). Thus, Claim 19 of Xu explicitly recites a fabrication method that combines the step of “recessing the isolation structure by removing a portion of the isolation structure”—as disclosed in the first embodiment—with the step of removing materials from the source and drain regions of the fins to form recesses in the fin structures—as described in the second embodiment. Ex. 1004 at Claim 19; Ex. 1003 at ¶ 95. That Xu claims these steps together demonstrates that a POSITA would have found it obvious to combine the first embodiment with the fin-recessing of the second embodiment to arrive at the claimed method. Ex. 1003 at ¶ 95. Put simply, a POSITA reading Claim 19 would have “readily envisage[d] the combination of” Xu’s first and second embodiments and “it would have been obvious to that person that these two could be combined with a reasonable expectation of success.” *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1385 (Fed. Cir. 2015).

7. 1[f]: forming an epitaxial layer to fill up the recess,

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 96. As discussed above, a POSITA would have been motivated to combine Xu's first embodiment with the technique for recessing the "fins 120." *Id.*; *see supra* 1[e]. A POSITA would have been further motivated to form an epitaxial layer to fill up the recess when recessed fins of the second embodiment are combined with the first embodiment. Ex. 1003 at ¶ 96. For example, Xu notes that after the fins are recessed, fin template 280 "may be formed by a process similar to that described above with reference to FIG. 5" of Xu's first embodiment. Ex. 1004 at 11:2-4. In other words, after recessing the fins of Xu's first embodiment, Xu expressly recognizes that the same epitaxial growth process of the first embodiment is used to fill the recess with the "fin template" (purple). *Id.*; Ex. 1004.

As shown in Figure 10A, this epitaxially-grown layer 280 (purple) fills the recesses above fins 220 in the second embodiment where recesses are formed in the fins. Ex. 1004 at Fig. 10A; Ex. 1003 at ¶ 97.

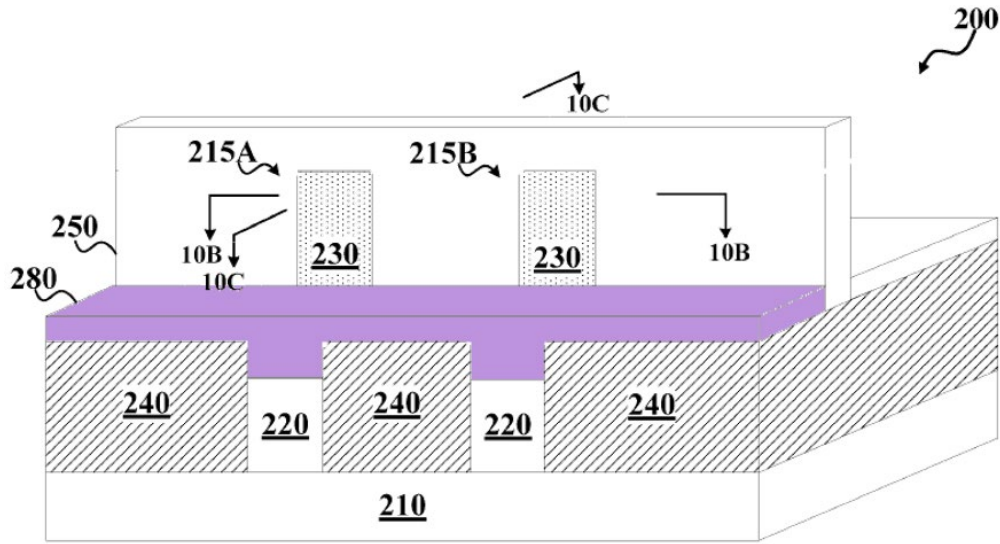


FIG. 10A

Figure 5 illustrates the corresponding epitaxial structure 135 for the first embodiment without a recess in the fin structure above fins 120. Ex. 1004 at Fig. 5; Ex. 1003 at ¶ 98.

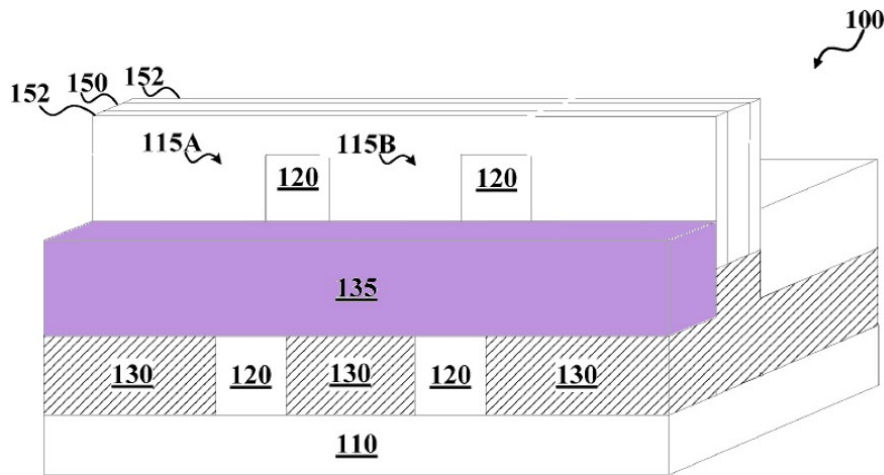
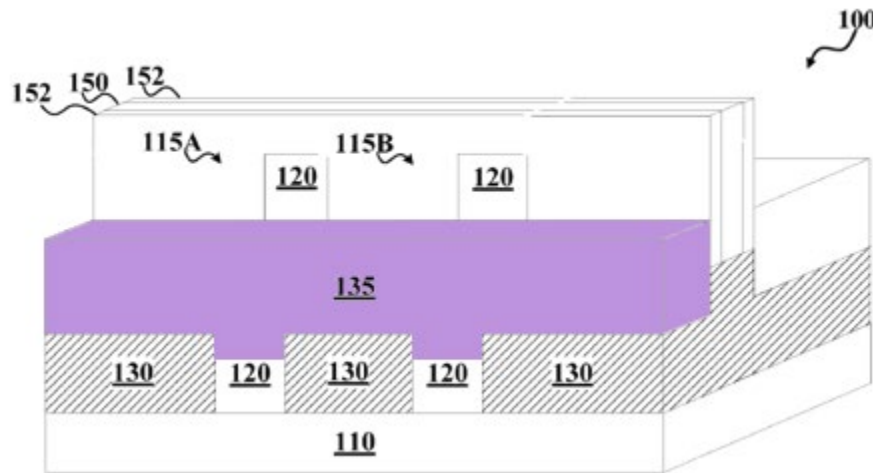


FIG. 5

Thus, when the fin-recesses of the second embodiment are formed in the first embodiment, a POSITA would have understood and found it obvious that an

epitaxial layer (purple) will “fill the recesses” because Xu teaches that, in both embodiments, the epitaxial layer is formed on the “exposed portions of the fins 120.” Ex. 1004 at 5:1-2 (first embodiment); 11:4-8 (second embodiment); Ex. 1003 at ¶ 99. This is shown in the modified figure below, showing the combination of the second embodiment’s recesses with the first embodiment. *Id.*



As discussed, fin template 280 of the second embodiment “may be formed by a process similar to that described above with reference to FIG. 5” of Xu’s first embodiment. Ex. 1004 at 11:2-4. Thus, fin template 135/280 is an epitaxial layer because it is formed by “epitaxially (epi) growing a semiconductor material on exposed portions of the fins 120 in the source and drain regions of the fin structures 115A and 115B.” *Id.* at 5:4-8. The fin template 135 “could be silicon germanium (SiGe) formed by a silicon germanium epitaxial deposition process.” *Id.* at 5:18-20.

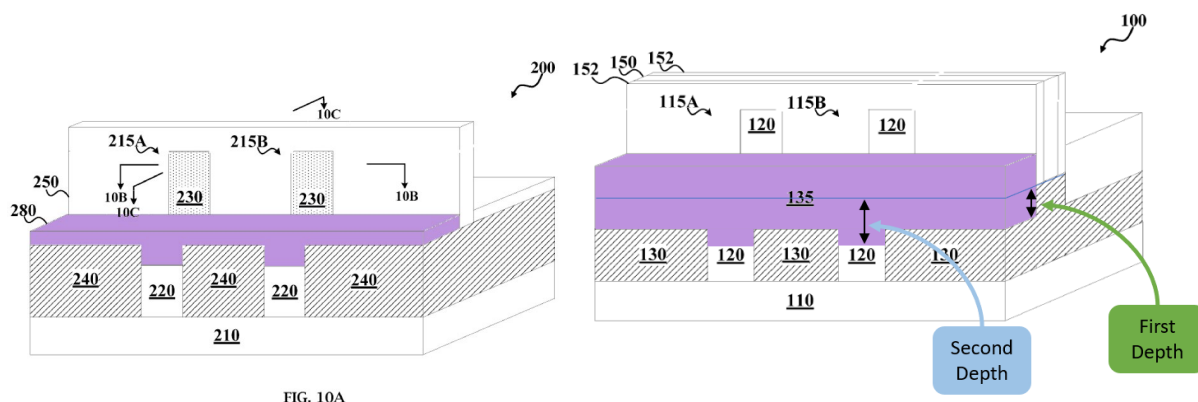
8. 1[g]: wherein a bottom surface of the recess has a second depth, and the second depth is deeper than the first depth.

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 101. For example, when recessed fins of the second embodiment are applied to the first embodiment of Xu as discussed above, the recesses form “trenches” that “extend[]” to an “exposed surface of the fin portion 220.” Ex. 1004 at 10:50-57. The bottoms of these trenches define the claimed “second depth” which extends to the recessed surface of the fin. Ex. 1003 at ¶ 101.

The “trench sidewalls” are defined by the “isolation features” (Ex. 1004 at 10:52-54), the top surfaces of which were previously etched to the claimed “first depth.” *See supra* cl. 1[d]. Because the top surfaces of the isolation features define the “first depth” and the bottom of the trench defines the “second depth,” the second depth is necessarily “deeper than the first depth” as claimed. Ex. 1003 at ¶ 102.

Figure 10A depicts the second embodiment of Xu, which shows the “second depth.” Ex. 1004 at Fig. 10A. Because the isolation structure is not shown to be etched, Figure 10A does not depict the “first depth.” Ex. 1003 at ¶ 103. A POSITA, however, would have understood that combining the recessed fins 220 of the second embodiment with the first embodiment’s etched isolation structures (as shown in

modified version of Figure 5 below), results in a structure where the second depth is deeper than the first depth.² *Id.*



Therefore, in the combined device, where the isolation structure has been etched to a first depth, the bottom of the trench has a second depth that is deeper than the “first depth” because the “first depth” terminates at the top surface of the adjacent isolation structures whose sidewalls form the trench. Ex. 1003 at ¶ 104.

C. Claim 2: The fabrication method according to claim 1, wherein the isolation structure is a shallow trench isolation structure.

As discussed above, Xu discloses and renders obvious the fabrication method according to claim 1. Xu further discloses and renders obvious the additional limitation of claim 2. Ex. 1003 at ¶ 105. For example, Xu discloses that isolation

² For visual comparison, the annotated figure extends with a blue line the plane of the top surface of the isolation structure below the gate, which serves as reference points for the first and second depths.

features 130 can be “shallow trench isolation (STI) structures, surround[ing] the fin structures 115A and 115B.” Ex. 1004 at 3:54-58; *see also id.* at 9:30-33 (same for isolation features 240 in second embodiment).

D. Claim 3: The fabrication method according to claim 1, wherein a step for etching the isolation structure comprises wet etching or dry etching.

As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 3. Ex. 1003 at ¶ 106. For example, Xu discloses that “an etching process is applied to recess the isolation features 130” and that the etching can be “a dry etching process, wet etching process, other etching process, or combinations thereof.” Ex. 1004 at 4:55-58.

E. Claim 4: The fabrication method according to claim 1, wherein the gate structure is a dummy gate structure.

As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 4. Ex. 1003 at ¶ 107. For example, Xu discloses that the gate structure 150 may be formed in a “gate last process.” Ex. 1004 at 4:13-14. A POSITA would have understood and found it obvious that a gate last process comprises forming a dummy gate structure as the “gate structure.” Ex. 1003 at ¶ 107.

Skilled artisans used “gate-last” and “RMG” interchangeably during the relevant timeframe. *See* Ex. 1009 at 34 (“gate-last (GL=RMG)”). Thus, a POSITA

would have understood and found obvious that Xu's "gate-last" and the '384 Patent's replacement metal gate ("RMG") processes patent refer to the same approach, wherein metal gate structures are formed last to replace dummy gates. Ex. 1003 at ¶ 109. The '384 patent admits that a RMG process includes forming a dummy gate structure and then "removing the [dummy] gate structure to leave a trench." Ex. 1003 at ¶ 109; Ex. 1001 at 7:21-27. The '384 Patent further admits that this "RMG process . . . [is] well-known to those skilled in the art" and therefore omits a detailed description of it. *Id.* at 7:31-34.

Formation of dummy gates was well-known in the art by 2013 as prerequisite to forming the final gate in gate-last processing. Ex. 1003 at ¶ 108 (citing Ex. 1008 at 16). This gate-last process has the advantage that the "final metal gate is not exposed to the high activation anneal for the junctions." Ex. 1008 at 16. "As a result, a better controlled work function for nMOS and pMOS can be achieved." *Id.*

Thus, a POSITA would have understood and found obvious that in the gate-last process in Xu, a dummy gate structure is formed at the step 16 of forming the gate structure in the Figure 1 fabrication method. Ex. 1003 at ¶ 110. The rest of the fabrication would be the same, with additional unclaimed steps at the end of the method for removing the dummy gate and forming the replacement metal gate. *Id.*

F. Claim 5: The fabrication method according to claim 1, wherein a step for forming the recess comprises wet etching or dry etching.

As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 5. Ex. 1003 at ¶ 111. For example, Xu discloses that the etching process that removes the fin portions 230 to form the claimed recess can be “a dry etching process, [or] wet etching process” Ex. 1004 at 10:34-38; *see also supra* discussion of claim limitation 1[e].

G. Claim 6: The fabrication method according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 6. Ex. 1003 at ¶ 112. For example, Xu discloses that the fin template 135 (an epitaxial structure as shown above for limitation 1.f), “could be silicon germanium (SiGe) formed by a silicon germanium epitaxial deposition process.” Ex. 1004 at 5:18-20; *see also* Xu at 11:14-16 (same for fin template 280 in the second embodiment).

Xu also discloses that the fin template could be silicon phosphide. Specifically, “the epi silicon fin template 135 may be doped with phosphorous (to form a Si:P epi layer). The doped epitaxial layer may have a gradient doping profile.” Ex. 1004 at 5:23-25. A POSITA would have understood this disclosure,

and specifically “Si:P”, to mean the epitaxial structure 135 can be silicon phosphide.

Ex. 1003 at ¶ 113.

H. Claim 7: The fabrication method according to claim 1, further comprising forming a spacer before etching the isolation structure, wherein the spacer is disposed on a sidewall of the gate structure.

As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 7. Ex. 1003 at ¶ 114. For example, Xu discloses “spacers 152 are disposed on the sidewalls of the gate structure 150, such as along the gate electrode.” Ex. 1004 at 4:39-40. And Figure 2 shows the spacers 152 (blue) formed on the sidewalls of the gate structure 150 before etching the isolation structure 130 as shown in Figure 3. *Id.* at Figs. 2-3. Although the figures for Xu’s second embodiment do not show the spacers, Xu discloses that they exist in the same manner as Figure 2. *Id.* at 10:11-14; Ex. 1003 at ¶ 114.

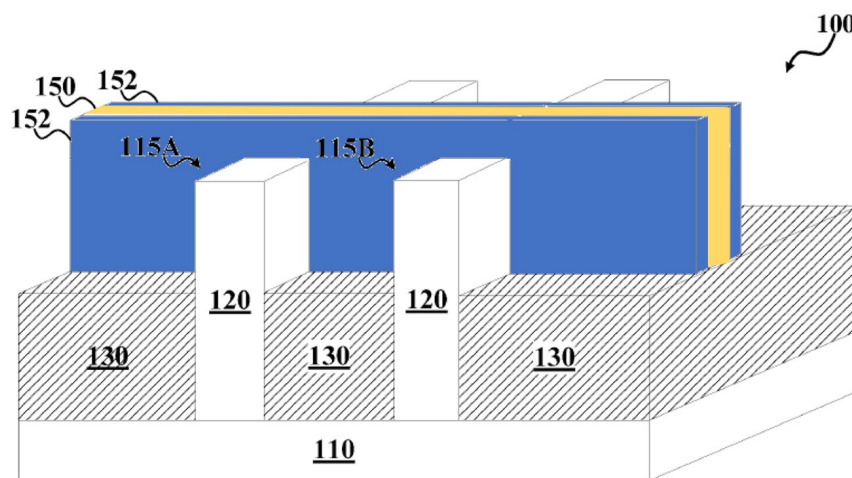


FIG. 2

I. Claim 8: The fabrication method according to claim 7, wherein a step for forming the spacer comprises: depositing a material layer to conformally cover the gate structure and the fin structure, and etching the material layer until the isolation structure is exposed.

As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 8. Ex. 1003 at ¶ 115. For example, Xu discloses that “spacers 152 may be formed by depositing a silicon nitride layer.” Ex. 1004 at 4:46-49.

A POSITA would have understood and found obvious that the deposited silicon nitride layer would conformally cover the gate structure and the fin structure as recited in claim 8. Ex. 1003 at ¶ 116. For example, a POSITA would have understood that, by the time of the effective filing date, materials like silicon nitride were typically deposited using conformal deposition techniques such as LPCVD (low-pressure chemical vapor deposition) or PECVD (plasma-enhanced CVD), which were well-known to coat all exposed topographies uniformly. *Id.* (citing Ex. 1025 describing CVD techniques for conformal deposition of silicon nitride). Here, the gate structure 150 and fin structure 115A/115B are formed before the spacers, and are exposed at this point of the fabrication method. *Id.* at ¶ 117. A POSITA therefore would have understood that the deposited SiN layer conformally coats both of these structures before being anisotropically etched to form spacers along the gate sidewalls and above the fin. *See id.* at ¶¶ 116-117 (citing Ex. 1025 and explaining

how the deposition of silicon nitride using traditional CVD techniques would result in a conformal coating of exposed surfaces).

To the extent Patent Owner argues the deposition in Xu is non-conformal, it would have been obvious to a POSITA to simply substitute one of these well-known conformal deposition processes into the method of Xu, yielding the predictable results of a conformal, uniform coating over all exposed topographies. *Id.* at ¶ 118. *See also KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007) (“the mere substitution of one element for another known in the field ... must do more than yield a predictable result” to be nonobvious).

Further, Xu discloses that the silicon nitride layer is dry etched to form the spacers as illustrated in Figure 2, above. Ex. 1004 at 4:46-49. A POSITA would have understood and found obvious that this etching constitutes etching the material layer until the isolation structure is exposed. Ex. 1003 at ¶ 119. For example, Figure 2 illustrates that the isolation layer is exposed after formation of the spacers 152. *Id.*; Ex. 1004 at Fig. 2. Additionally, spacers were well-known in the art and were used to isolate the gate structure from the source/drain regions of a transistor. Ex. 1003 at ¶ 119. Thus, the function of the well-known spacers dictates that it is disposed on the sidewalls of the gate structure and thus would be removed from other features, such as the isolation structures. *Id.*

J. Claim 9

1. 9[pre]: The fabrication method according to claim 1, further comprising:

As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu also renders obvious claim 9 in view of the knowledge of a POSITA, as detailed below. Ex. 1003 at ¶ 120.

2. 9[a]: depositing an interlayer dielectric to surround the gate structure;

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 121. For example, as detailed above for claim 4, a POSITA would have understood and found obvious that Xu's disclosure of a "gate-last" process (Ex. 1004 at 4:13-14) refers to the "well-known" replacement metal gate (or "RMG process"). *See supra* cl. 4; *see also* Ex. 1001 at 7:31-34; Ex. 1003 at ¶ 121. A POSITA would have understood that Xu's gate-last process includes depositing an interlayer dielectric to surround the gate structure. Ex. 1003 at ¶ 121.

The '384 patent expressly admits that "the RMG process" was "well-known to those skilled in the art" at the time of filing. Ex. 1001 at 7:31-34. The '384 patent further describes the steps that this "well-known" process entails. *Id.* at 7:24-29. These admissions relating to the RMG process, are "binding on the patentee" and bear on "whether th[e] patent's claims would have been obvious." *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1339 (Fed. Cir. 2020) ("Admissions in the specification regarding the prior art are binding on the patentee for purposes of

a later inquiry into obviousness.”); *Qualcomm Inc. v. Apple Inc. (Qualcomm I)*, 24 F.4th 1367, 1375 (Fed. Cir. 2022) (“We have held that ‘it is appropriate to rely on admissions in a patent’s specification when assessing whether that patent’s claims would have been obvious’ in an inter partes review proceeding.”); *Qualcomm Inc. v. Apple Inc. (Qualcomm II)*, No. 23-1208, 2025 WL 1174161 at *8 (Fed. Cir. Apr. 23, 2025) (“... an IPR petition may rely on AAPA for certain uses....”). Here, Applicant’s admissions are properly relied upon because they “indicate the general knowledge of a person of ordinary skill in the art.” *Qualcomm II*, 2025 WL 1174161 at *8. Specifically, Applicant’s admissions evidence that a POSITA would have understood Xu’s disclosure of a “gate last” process as disclosing the limitations set forth in claim 9 of the ’384 Patent. Ex. 1003 at ¶ 122.

Specifically, a POSITA would have understood that Xu’s “gate-last process” is the applicant admitted prior art “RMG process,” which a POSITA would have understood includes “depositing an interlayer dielectric *to surround the gate structure.*” Ex. 1001 at 7:24-34; *see, e.g., Koninklijke Philips N.V.*, 948 F.3d at 1339 (“Admissions in the specification regarding the prior art are binding on the patentee for purposes of a later inquiry into obviousness.”).

Further, Xu expressly recognizes that the FinFET device 100 “may include additional features,” such as “*interlayer-dielectrics*” that are formed “over the substrate 110.” Ex. 1004 at 6:44-53. Interlayer dielectrics (ILDs) were well-known

to a POSITA before 2013 and used for isolating electrically conducting and semiconducting features and films in transistors. Ex. 1003 at ¶ 124 (citing Ex. 1011 at v; Ex. 1010 at 27). A POSITA would have understood and found obvious that to isolate the “electrically conducting” gate, the interlayer dielectric would be deposited to surround the gate structure of Xu. Ex. 1003 at ¶ 124.

3. 9[b]: removing the gate structure to leave a trench;

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 125. For example, a POSITA would have understood that Xu’s “gate-last process” is the applicant admitted prior art “RMG process,” which a POSITA would have understood includes “removing the gate structure to leave a trench.” Ex. 1001 at 7:24-34; *see, e.g., Koninklijke Philips N.V.*, 948 F.3d at 1339.

Moreover, as discussed above for claim 4, a POSITA would have understood and found obvious that the “gate last process” of Xu uses a dummy gate as the initial gate structure, which is subsequently removed. Ex. 1003 at ¶ 126; Ex. 1008 at 16 (in a gate-last process “a dummy gate is patterned” and later “removed after source/drain silicidation and replaced by the final gate stack.”). A POSITA would further have understood that removing the gate structure 152 (gold) of Xu would leave a trench between the spacers 152. *See* Ex. 1004 at Fig. 2.

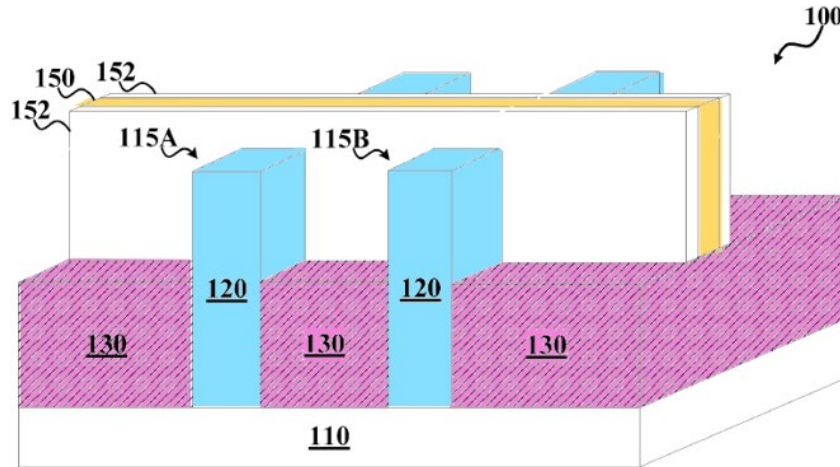


FIG. 2

4. 9[c]: forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench; and

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 127. For example, a POSITA would have understood that Xu’s “gate-last process” is the admitted prior art “RMG process,” which a POSITA would have understood includes “forming a gate dielectric layer to conformally cover the sidewalls and bottom of the trench.” Ex. 1001 at 7:27-28; *see, e.g., Koninklijke Philips N.V.*, 948 F.3d at 1339.

Moreover, Xu discloses that its “gate structure 150 may include a gate dielectric layer.” Ex. 1004 at 4:2-3. A POSITA would have understood and found obvious that the gate dielectric layer is deposited conformally to cover a sidewall and a bottom of the trench in a gate-last process. Ex. 1003 at ¶ 128; *see also* Ex. 1008 at 16 (describing that multi-gate FETs “require[] highly conformal deposition techniques for the gate electrode and dielectric”).

5. 9[d]: forming a conductive layer to fill up the trench.

Xu discloses and renders obvious this limitation. Ex. 1003 at ¶ 129. For example, a POSITA would have understood that Xu's "gate-last process" is the admitted prior art "RMG process," which a POSITA would have understood includes "forming a conductive layer to fill up the trench." Ex. 1001 at 7:28-29; *see, e.g., Koninklijke Philips N.V.*, 948 F.3d at 1339.

Further, Xu discloses that its "gate structure 150 may include . . . a gate electrode." Ex. 1004 at 4:2-3. A POSITA would have understood and found obvious that in Xu's "gate last process," that final gate structure would include this "gate electrode" because it is a conductive layer replacing the dummy gate. Ex. 1004 at 4:10-13 (gate electrode includes "polysilicon and/or a metal . . . or other conductive materials"); Ex. 1003 at 130. Without it, the transistor would not work. *Id.* In fact, it was well-known that the gate-last process forms a "replacement metal gate" that replaces the dummy gate and fills the trench left by the dummy gate. *See, e.g.,* Ex. 1009 at 34; Ex. 1003 at ¶ 130. After forming the replacement metal gate, the transistor would be as shown in Figure 6 of Xu, below, where the gate structure of FinFET 100 would fill the trench between spacers 152 left by removing the dummy gate (gold). Ex. 1004 at Fig. 6; Ex. 1003 at ¶ 130.

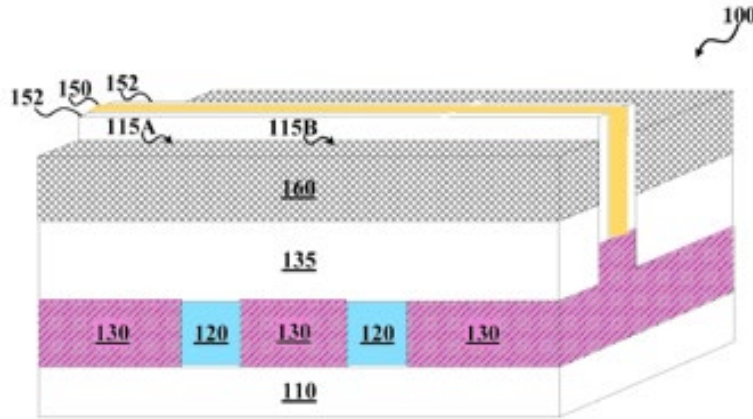


FIG. 6

V. Ground 1B: Claims 4 and 9 Are Obvious Over Xu in View of Brask

Additionally, claims 4 and 9 are rendered obvious by the combination of Xu and Brask. Brask discloses a common mechanism for following a “gate last” process, and, as explained below, a POSITA would have combined Xu and Brask because Xu suggests using a gate last process, and Brask provides details on how such a gate last process should be implemented.

A. Overview of Brask

Brask is titled “Nonplanar Transistors With Metal Gate Electrodes” and was filed on December 30, 2003 and published on July 7, 2005. *See* Ex. 1006. Because Brask is in the same field (FinFETs) and reasonably pertinent to a problem the ’384 patent purports to address (FinFET fabrication), Brask is analogous art. *See* Ex. 1001 at Abstr., 3:39-54; Ex. 1006 at ¶¶ [0015]-[0017], [0046]; Ex. 1003 at ¶ 69. Brask is directed to “semiconductor integrated circuit manufacture” and in particular, integrated circuits including “nonplanar transistors.” *Id.* at ¶ [0002].

Brask discloses such “nonplanar transistors” include transistors comprising semiconductor fins—*i.e.*, FinFETs. *Id.* at ¶ [0046]; Ex. 1003 at ¶ 69. Brask further discloses forming such transistors “utilizing a replacement gate technique.” Ex. 1006 at ¶ [0058]. An example of such a technique is depicted in Figures. 6G-6K of Brask. Ex. 1003 at ¶ 69. These figures depict the replacement gate process for an n-type transistor, but Brask also discloses further steps to form a replacement gate for a p-type transistor with respect to Figures 6L-6O. *Id.*

Figure 6G depicts a nonplanar transistor prior to the replacement gate process having source/drain regions 613 of a semiconductor body (*i.e.*, “fin”) (blue) separated by a sacrificial gate 604 (gold). Ex. 1006 at ¶ [0069]. An annealing process is carried out in Figure 6G to activate dopants within the source/drain regions. *Id.* The anneal process causes “dopants placed into the sacrificial gate electrode 604 to move from interstitial sites and substitute with atoms in the lattice of the sacrificial gate electrode 604.” *Id.* Next, in Figure 6H, a dielectric material (green) is “blanket deposited over the substrate” and then “planarized ... until the top surface of the dielectric film is planar with the sacrificial gate electrode.” Ex. 1006 at ¶ [0071].

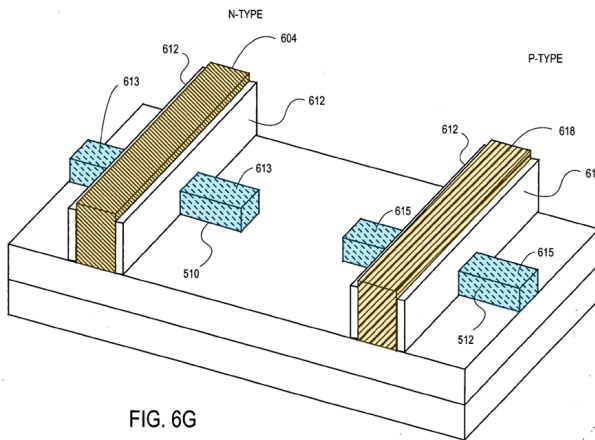


FIG. 6G

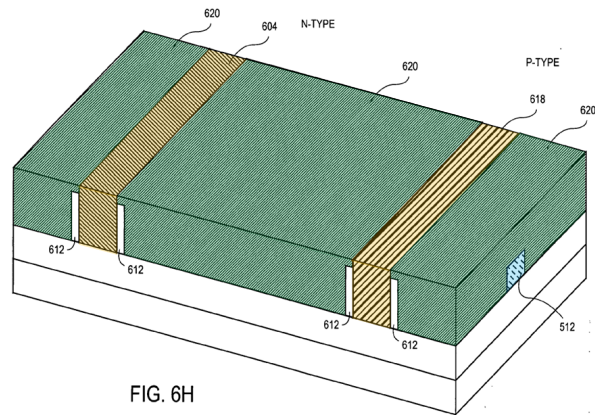


FIG. 6H

In Figure 6I, after forming the dielectric layer, the sacrificial gate is removed to form an opening for the gate electrode, exposing a channel of the fin (red). Ex. 1006 at ¶ [0072].

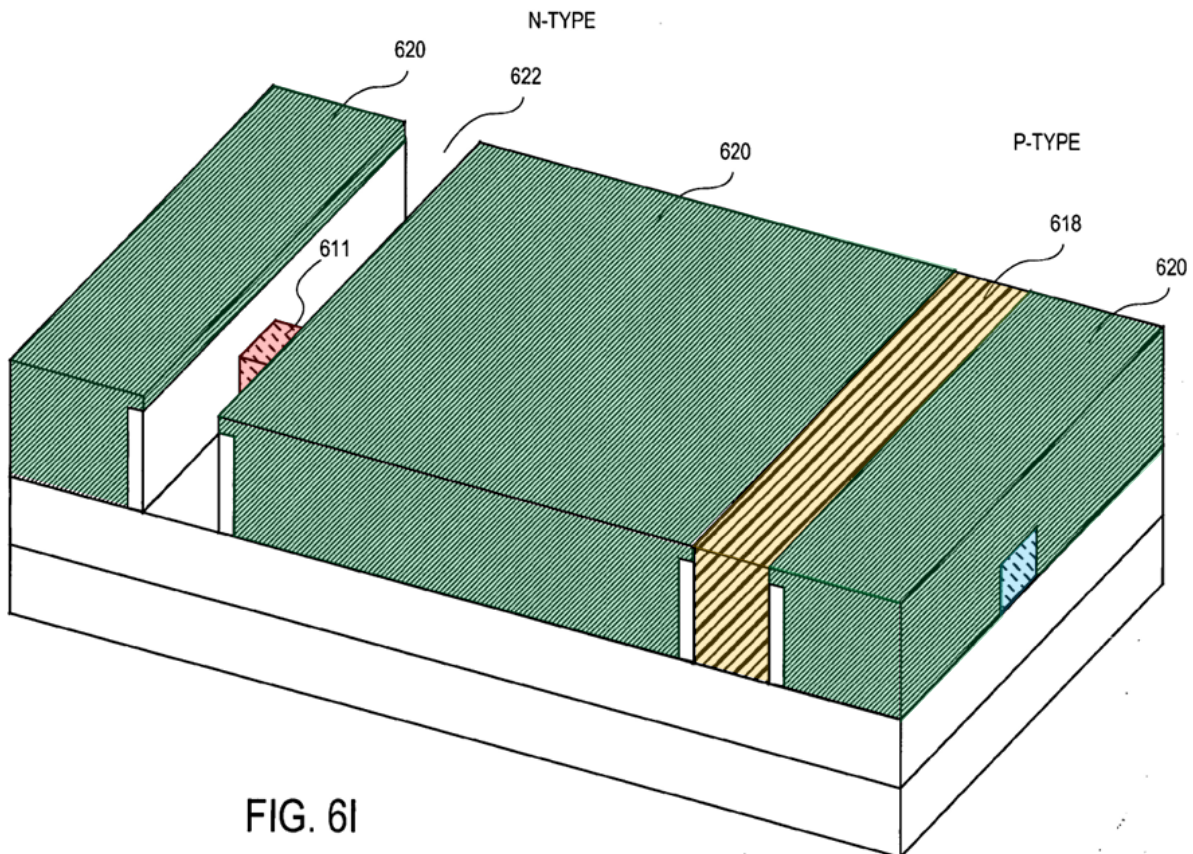
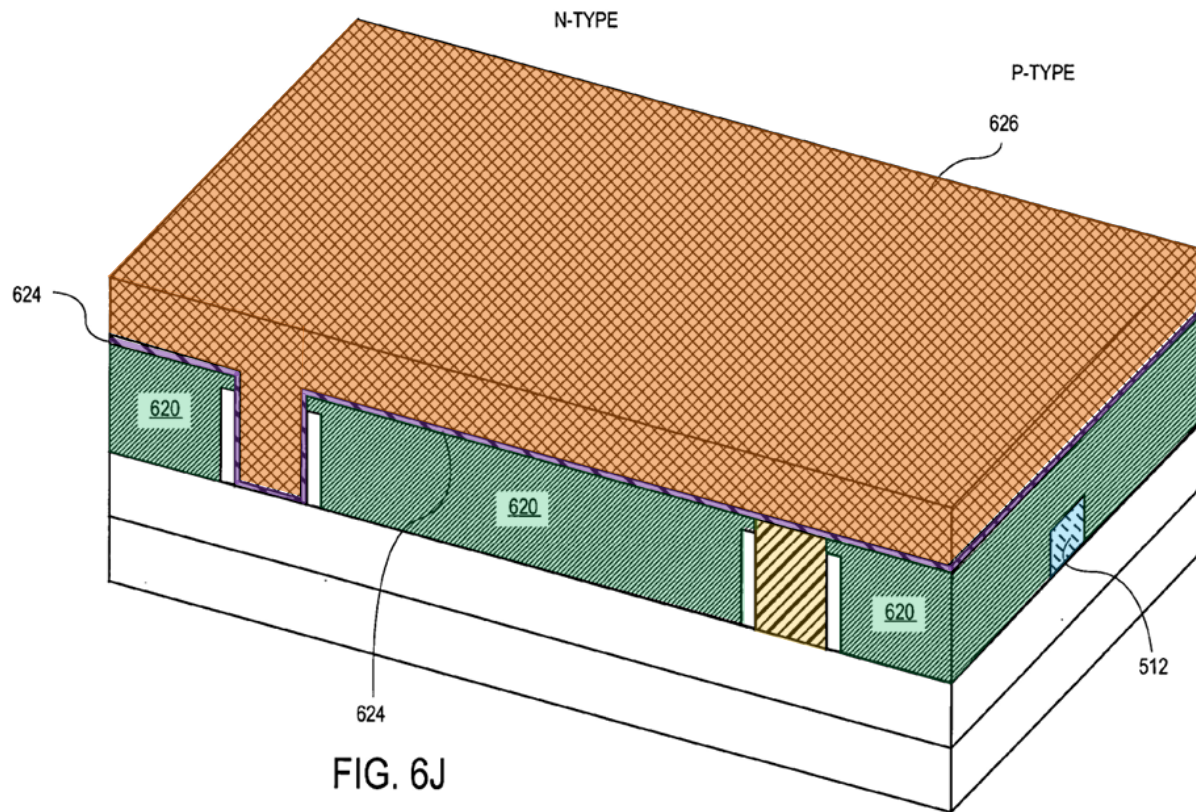
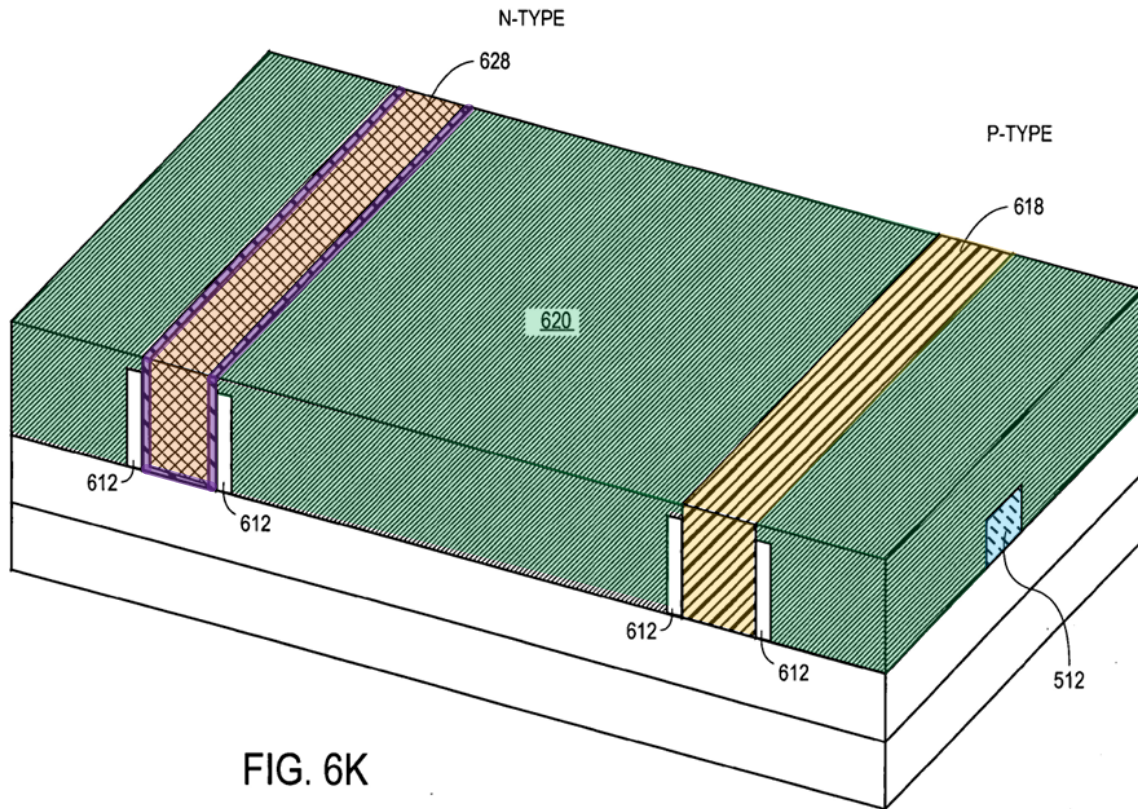


FIG. 6I

“Next, the gate dielectric layer [(purple)] and the gate electrode material [(orange)] for the ... device are formed in the openings 622 as shown in FIG. 6J.” *Id.* at ¶ [0074]. Brask discloses that a “conformal deposition process, such as CVD or ALD is used to deposit a high K gate dielectric layer.” *Id.*



The deposited gate dielectric layer and gate electrode material are then polished back or removed resulting in the gate structure shown in Fig. 6K. *Id.*



B. A POSITA would have been motivated to combine Xu with Brask.

As discussed above in Ground 1A, Xu discloses that the gate structure 150 may be formed in a “gate last process.” Ex. 1004 at 4:13-14. However, Xu does not explicitly disclose implementation details of the gate-last process. Ex. 1003 at ¶ 132. A POSITA therefore would have looked to established prior art, like Brask, for details on gate-last processing in FinFET structures. *Id.* Brask teaches fabricating a FinFET transistor with a gate-last process where a “sacrificial gate electrode” (*i.e.*, “dummy gate”) is first formed on the fins. Ex. 1006 at ¶ [0059]; *see id.* at ¶ [0047] (“semiconductor bodies *or fins* 510 and 512”) (emphasis added); Ex. 1003 at ¶ 132.

After source/drain regions of the transistor are formed, the sacrificial gate is removed to form an opening 622 exposing the channel region of the fin. Ex. 1006 at ¶ [0072]. The opening is then filled with a gate dielectric layer and gate electrode material which serve as a “gate dielectric layer” and “gate electrode,” respectively, of the final FinFET device. *Id.* at ¶ [0074]. A POSITA would have understood Brask’s process of forming a sacrificial gate (*i.e.*, “dummy gate”) first, and then removing the sacrificial gate (*i.e.*, “dummy gate”) and replacing it with a metal gate, is a “gate-last” process. Ex. 1003 at ¶ 132.

Xu explicitly motivates the use of a gate-last process by stating that its gate structure may be formed this way. Ex. 1004 at 4:13-14. A POSITA would have known the benefits of gate-last processes, which were well-known by the ’384 patent’s priority date. For example, as discussed above in Ground 1A, *supra*, a gate-last process has the advantage that the “final metal gate is not exposed to the high activation anneal for the junctions.” Ex. 1008 at 16. “As a result, a better controlled work function for nMOS and pMOS can be achieved.” *Id.* Brask expressly recognizes this advantage, disclosing that gate-last processing enables tuning of gate electrode work functions such that performance of the transistor may be “dramatically improved.” Ex. 1006 at ¶ [0058]. Brask’s therefore expressly teaches, suggests, or otherwise motivates a POSITA to combine the teachings of Xu with the

implementation details of Brask in order to achieve these advantages. Ex. 1003 at ¶ 133.

In the combination of Xu and Brask, a POSITA would recognize that the “gate structure 150” formed in step 16 of Figure 1 would be formed with a “gate-last process” (Ex. 1004 at 4:13-14) as taught by Brask, *e.g.*, by initially forming a “sacrificial gate electrode” over the fins (Ex. 1006 at ¶ [0059]). Xu’s process would then proceed through the source/drain formation. Ex. 1003 at ¶ 134.

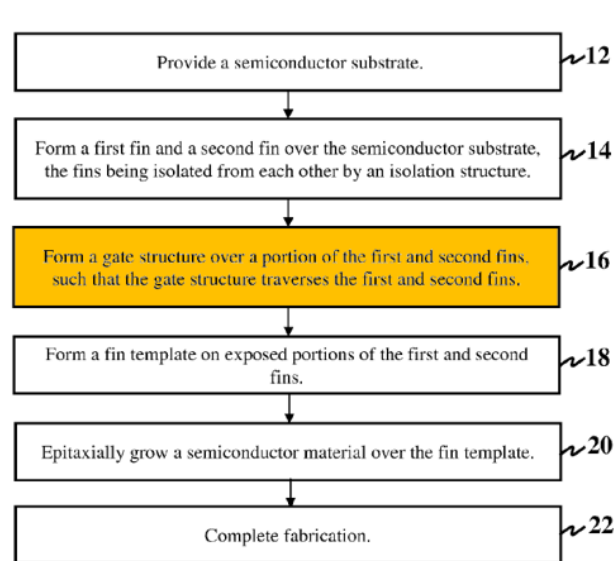


FIG. 1

After formation of the source and drain regions (*e.g.*, in Xu’s steps 18 and 20), an interlayer dielectric layer is formed. Ex. 1004 at 6:49-53; Ex. 1006 at ¶ [0071]. The dummy gate (*i.e.*, Brask’s sacrificial gate) is then removed to expose the fin, as taught by Brask. Ex. 1006 at ¶ [0072]. The gate dielectric and metal gate are subsequently formed in its place. *Id.* at ¶ [0074]. Notably, Xu and Brask teach

forming the operative metal gate structure using substantially the same process—including conformally depositing a gate dielectric layer (Ex. 1004 at 4:2-3; Ex. 1006 at ¶ [0074], Figure 6J) and then forming a metal gate to fill the trench (Ex. 1004 at 4:2-3, Figures 2-3; Ex. 1006 ¶ [0074], Fig. 6J). Ex. 1003 at ¶ 135. This obvious combination of Xu and Brask discloses all of the limitations of claims 4 and 9, as shown below, rendering those claims obvious to a POSITA.

C. Claim 4: The fabrication method according to claim 1, wherein the gate structure is a dummy gate structure.

As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu in view of Brask renders obvious claim 4. Ex. 1003 at ¶ 136.

Xu contemplates using a “gate-last process,” such as the process taught by Brask. Ex. 1004 at 4:13-14. When Xu is combined with Brask as discussed above, the fabrication method will include depositing a “sacrificial gate electrode.” Ex. 1006 at ¶ [0060]. A POSITA would have recognized that the “sacrificial gate electrode” is a “dummy gate structure” because it is not an operative gate and will subsequently be replaced. Ex. 1003 at ¶ 137.

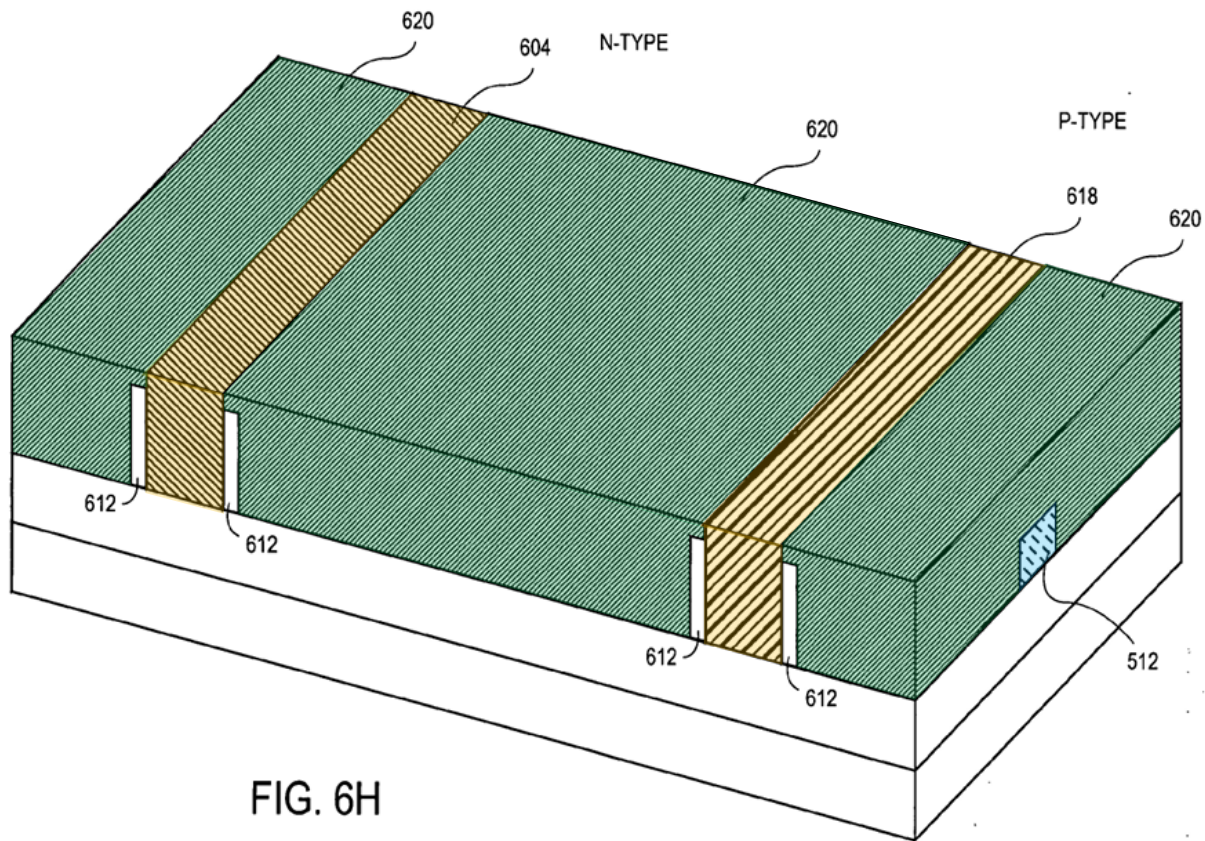
D. Claim 9

1. 9[pre]: The fabrication method according to claim 1, further comprising:

As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu in view of Brask further renders obvious claim 9.

2. 9[a]: depositing an interlayer dielectric to surround the gate structure;

Xu in view of Brask renders obvious this limitation. Ex. 1003 at ¶ 139. For example, Xu expressly recognizes that the FinFET device 100 “may include additional features,” such as “*interlayer-dielectrics*” that are formed “over the substrate 110.” Ex. 1004 at 6:44-53. A POSITA would recognize that the Xu-Brask combination will also comprise depositing an interlayer dielectric to surround the gate structure. Ex. 1003 at ¶ 139. Indeed, like Xu, Brask teaches depositing a dielectric layer 620 after the “sacrificial gate electrode” is deposited. Ex. 1006 at ¶ [0071]. A POSITA would have understood dielectric layer 620, which provides isolation between conductive structures in Brask, to be an “interlayer dielectric” as claimed. Ex. 1003 at ¶ 139 (citing Ex. 1011 at v, 3). As shown in Figure 6H of Brask, dielectric layer 620 surrounds the sacrificial gate electrode:



Further, as described above for Ground 1A, ILDs were well-known to a POSITA before 2013 and “used for isolating electrically conducting and semiconducting features and films” in transistors. Ex. 1003 at ¶ 140 (quoting Ex. 1011 at v). A POSITA would have understood and found obvious that to isolate the “electrically conducting” metal gate that will subsequently be formed, the interlayer dielectric would be deposited to surround the gate structure of the Xu-Brask combination. Ex. 1003 at ¶ 140.

3. 9[b]: removing the gate structure to leave a trench;

Xu in view of Brask renders obvious this limitation. Ex. 1003 at ¶ 141. For example, when Brask’s gate-last process is combined with Xu as discussed above, “the sacrificial gate electrode 604 is [] removed” thereby forming “an opening 622 where the gate electrode” is to be formed, as taught by Brask. Ex. 1006 at ¶ [0072]. Brask’s Figure 6I illustrates the opening (*i.e.*, “trench”) after removing the sacrificial gate, which will also be present in the Xu-Brask combination. Ex. 1003 at ¶ 141.

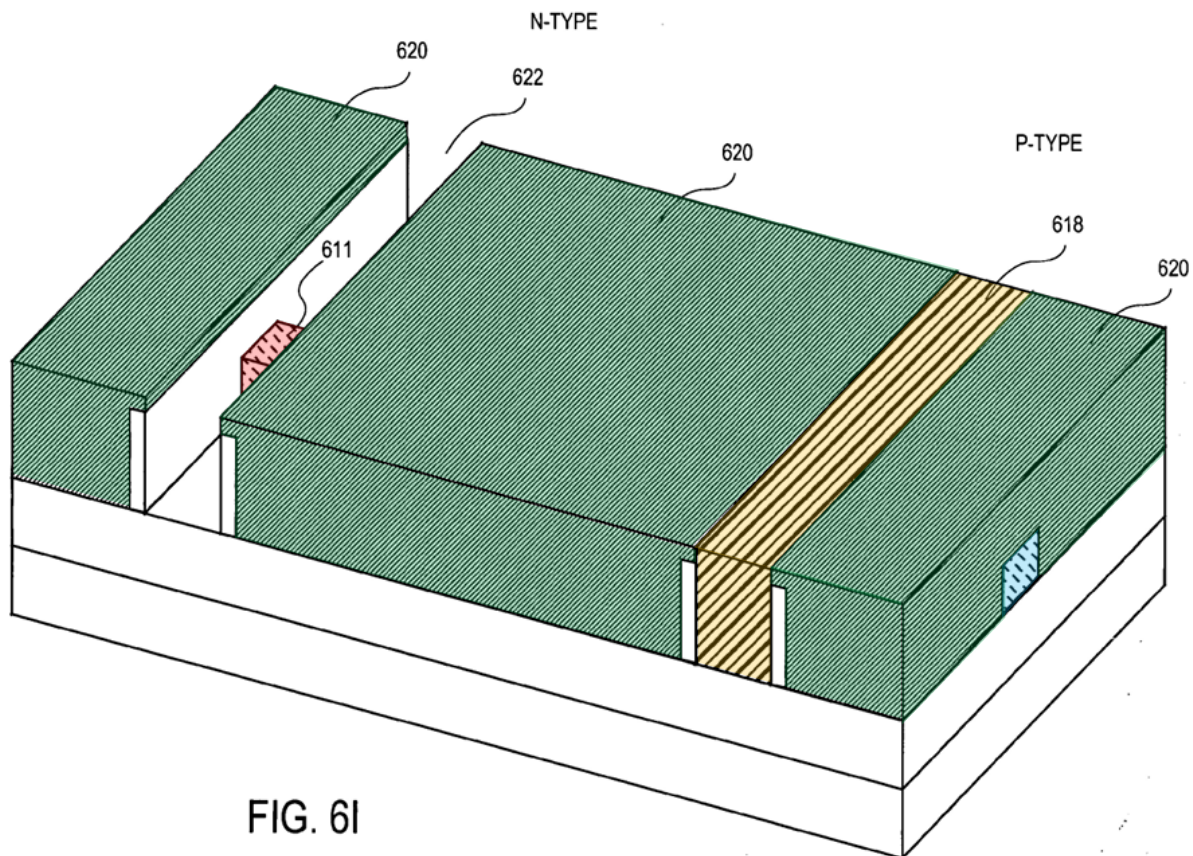
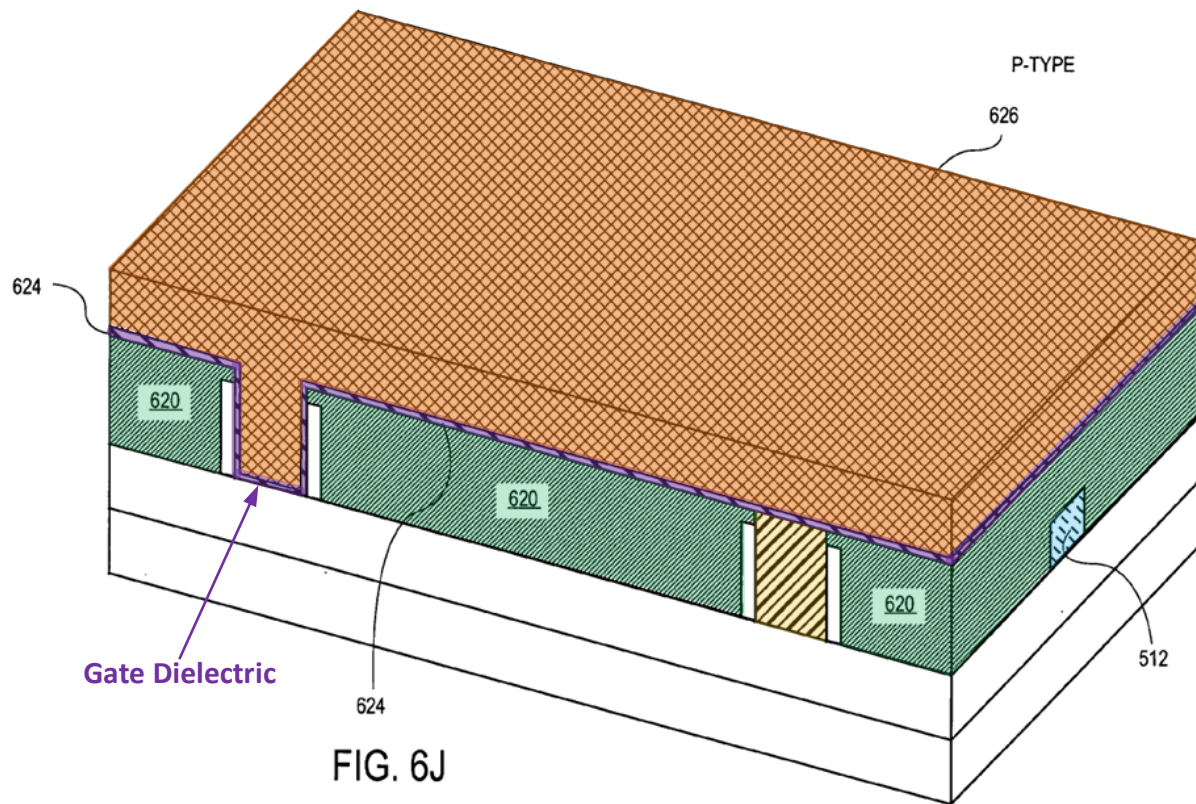


FIG. 6I

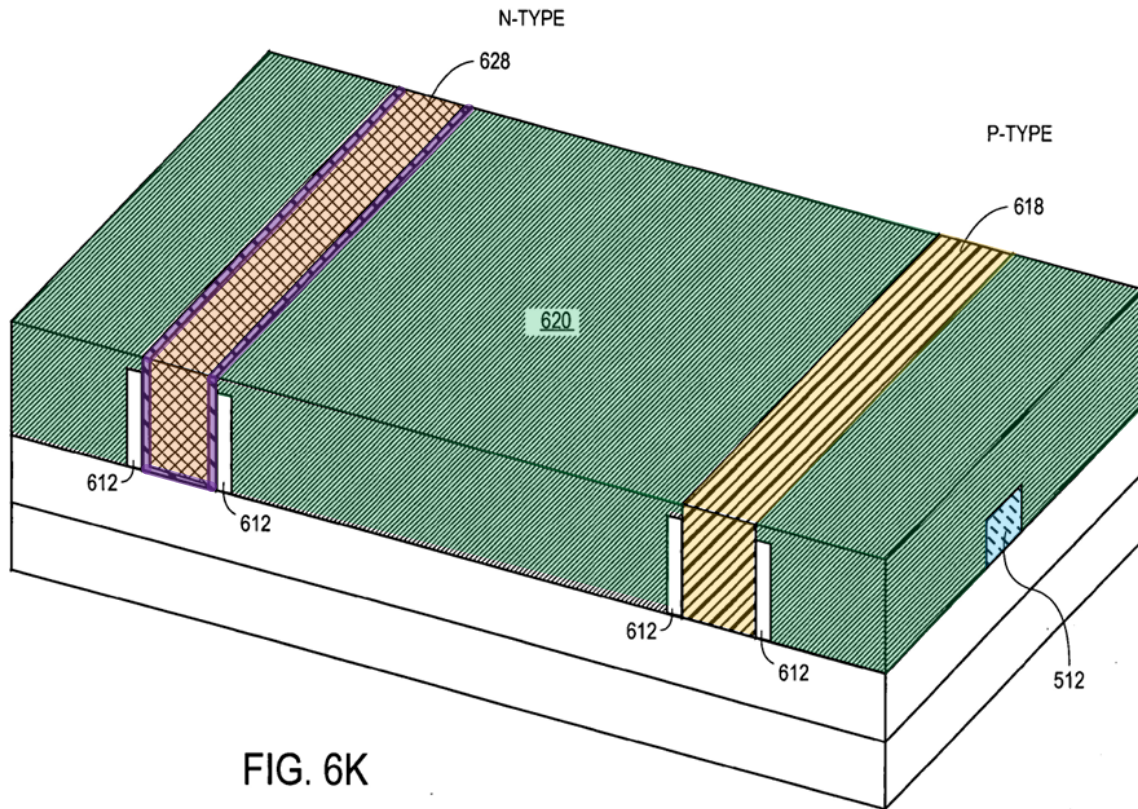
4. 9[c]: forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench; and

Xu in view of Brask renders obvious this limitation. Ex. 1003 at ¶ 142. For example, when Brask’s gate-last process is combined with Xu as discussed above, the process will include “a conformal deposition process, such as CVD or ALD ... to deposit a high K gate dielectric layer” in the trench, as taught by Brask. Ex. 1006 at ¶ [0074]. As shown in Figure 6J, the dielectric layer 624 (purple) of Brask conformally covers a sidewall and a bottom of the trench, which will also be present in the Xu-Brask combination. Ex. 1003 at ¶ 142.



5. 9[d]: forming a conductive layer to fill up the trench.

Xu in view of Brask renders obvious this limitation. Ex. 1003 at ¶ 143. For example, when Brask's gate-last process is combined with Xu as discussed above, the process will include blanket depositing a gate electrode material (*i.e.*, "a conductive layer") over the gate dielectric layer, as taught by Brask. Ex. 1006 at ¶ [0074]. Figure 6J of Brask, reproduced above, shows the gate electrode material 626 (orange) filling up the trench. Ex. 1006 at Fig. 6J; Ex. 1003 at ¶ 143. This gate electrode material filling up the trench will also be present in the Xu-Brask combination, and forms the gate electrode of the transistor after planarizing. Ex. 1006 at ¶ [0074], Fig. 6K; Ex. 1003 at ¶ 143.



VI. Ground 2A: Claims 1-3, And 5-8 Are Obvious Over Lin In View Of The Knowledge Of A POSITA

A. Overview of Lin

Lin was filed on October 13, 2010 by TSMC. Lin describes a “FinFET and Method of Fabricating the Same.” Ex. 1005 at Title. Because Lin is in the same field (FinFETs) and reasonably pertinent to a problem the ’384 patent purports to address (FinFET fabrication), Lin is analogous art. *See* Ex. 1001 at Abstr., 3:39-54; Ex. 1005 at Abstr., ¶ [0001]; Ex. 1003 at ¶ 62. Lin’s Figure 1 show “a method of fabricating a FinFET according to various aspects of the present disclosure.” Ex. 1005 at ¶ [0010].

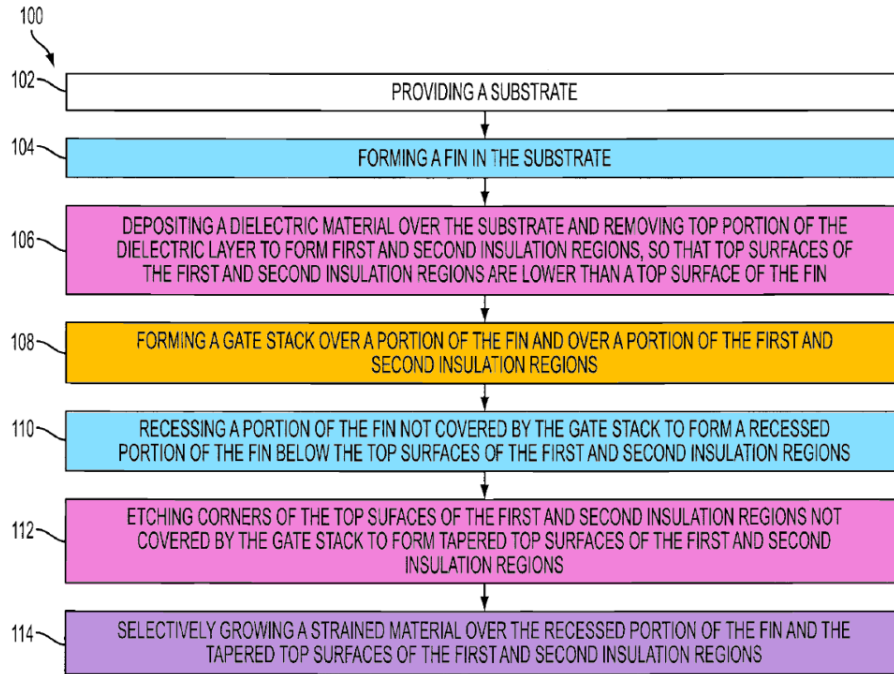


FIG. 1

First, “fins [blue] are formed by etching into the substrate 202,” as shown in Figure 3A. *Id.* at ¶¶ [0018]–[0019].

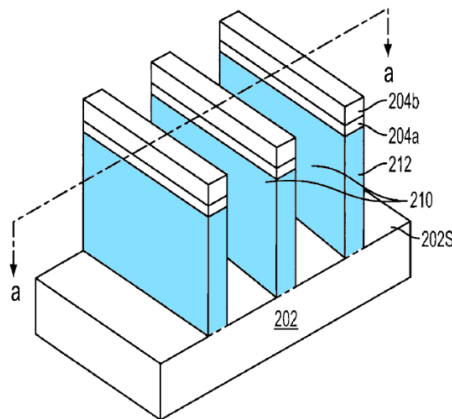


FIG. 3A

Next, “[t]renches 210 are filled with a dielectric material 214” as shown in Figure 4A. *Id.* at ¶ [0022]. Subsequently, Lin discloses “recessing of the insulation regions 216 [magenta],” as shown in Figure 6A. *Id.* at ¶ [0023].

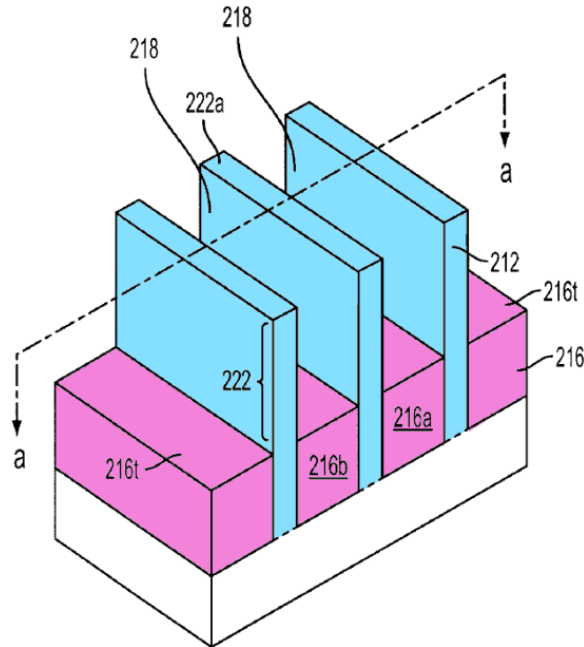


FIG. 6A

After that, “[a] gate stack 220 [gold] is formed over the substrate 202 over the top surface 222t and sidewalls 222s of a non-recessed portion of the channel fin 222a [blue] and extending to the flat top surfaces 216t of the first and second insulation regions [magenta],” as shown in Figure 7A. *Id.* at ¶ [0027].

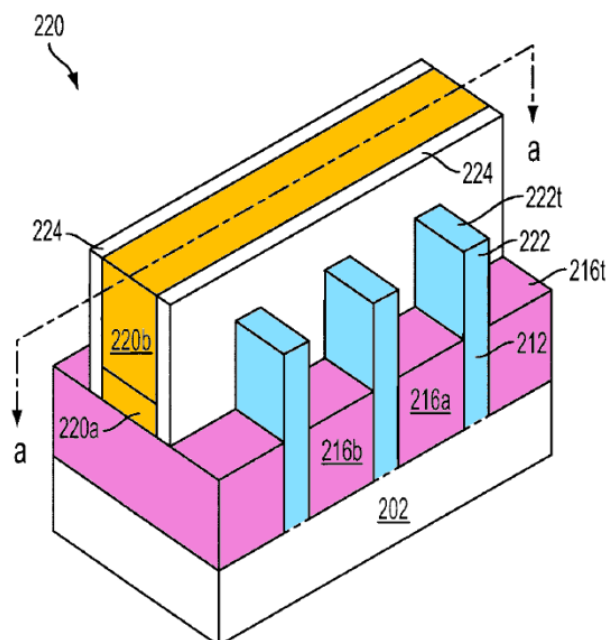


FIG. 7A

According to Lin, “[t]he portion of the semiconductor fin 212 [blue] not covered by the gate stack 220 [gold] and spacers 224 formed thereover are recessed to form a recessed portion 226 of the fin 212 [blue]” as shown in Figure 8A. *Id.* at ¶ [0031].

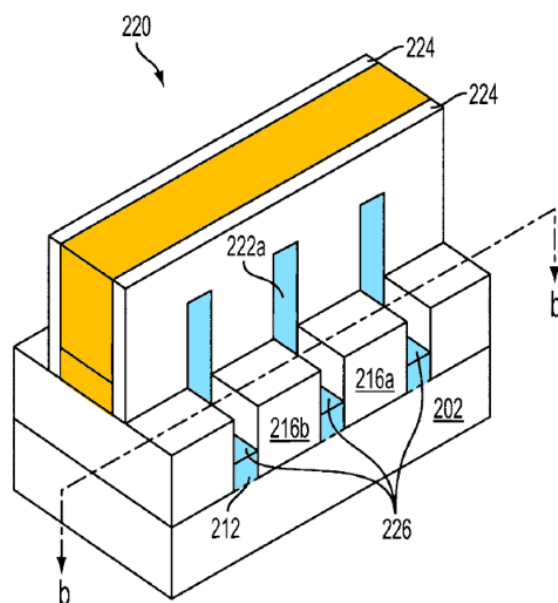


FIG. 8A

The isolation structure 216b and 216a are first “etched to form tapered top surfaces 216u” as shown in Figure 9B. *Id.* at ¶ [0032]. In one embodiment, those isolation structures are then further etched so that the “top surface 216u disappear[s] to form a curved top portion” of the isolation structure (magenta), which can be seen in Figure 9C. *Id.* at ¶ [0034].

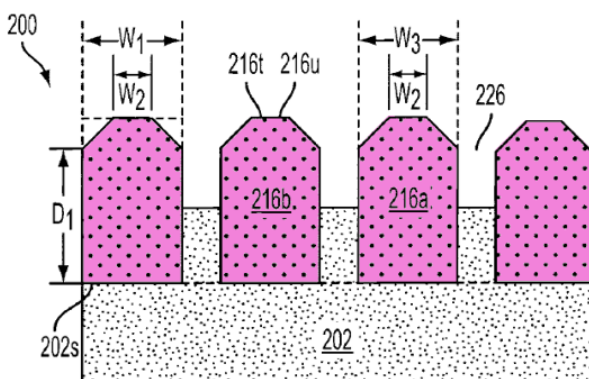


FIG. 9B

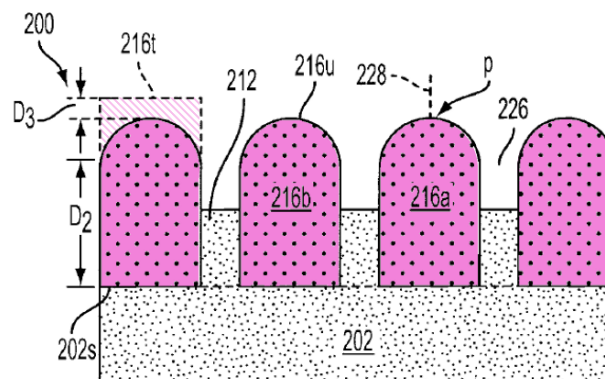


FIG. 9C

Finally, a “strained material 230” (purple) is “formed over the structure depicted in FIG. 9C” by “selectively growing a strained material 230 [purple] over the recessed portion 226 of the semiconductor fin 212 and extending over the tapered top surfaces 216u of the first and second insulation regions 216a, 216b [magenta].” *Id.* at ¶ [0035]. The resulting structure is depicted in Figures 10A and 10C.

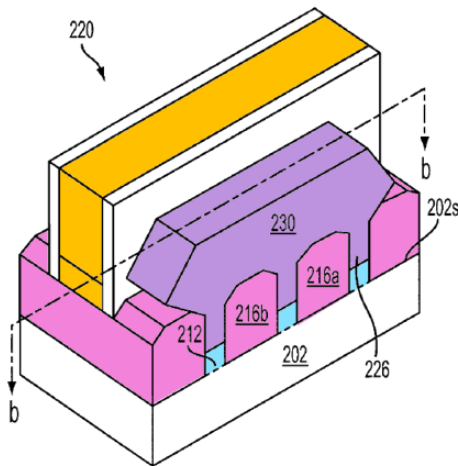


FIG. 10A

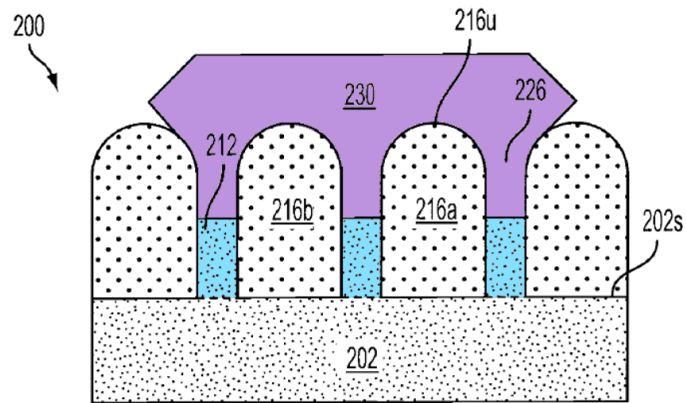


FIG. 10C

B. Claim 1

1. 1[pre]: A fabrication method for a semiconductor device:

The preamble is not limiting. Regardless, Lin discloses and renders obvious a fabrication method for a semiconductor device. Ex. 1003 at ¶ 145. Specifically, Lin describes its “Technical Field” as “relat[ing] to integrated circuit fabrication, and more particularly to a fin field effect transistor.” Ex. 1005 at ¶ [0001]. Lin describes a fabrication method for FinFET devices, including fabricating a fin, providing a gate over the fin, and growing strained materials in the source/drain regions from silicon germanium. *Id.* at ¶ [0002]. Figure 1 of Lin, reproduced below,

illustrates a method of fabricating a FinFET, which is a semiconductor device. *Id.* at ¶ [0010].

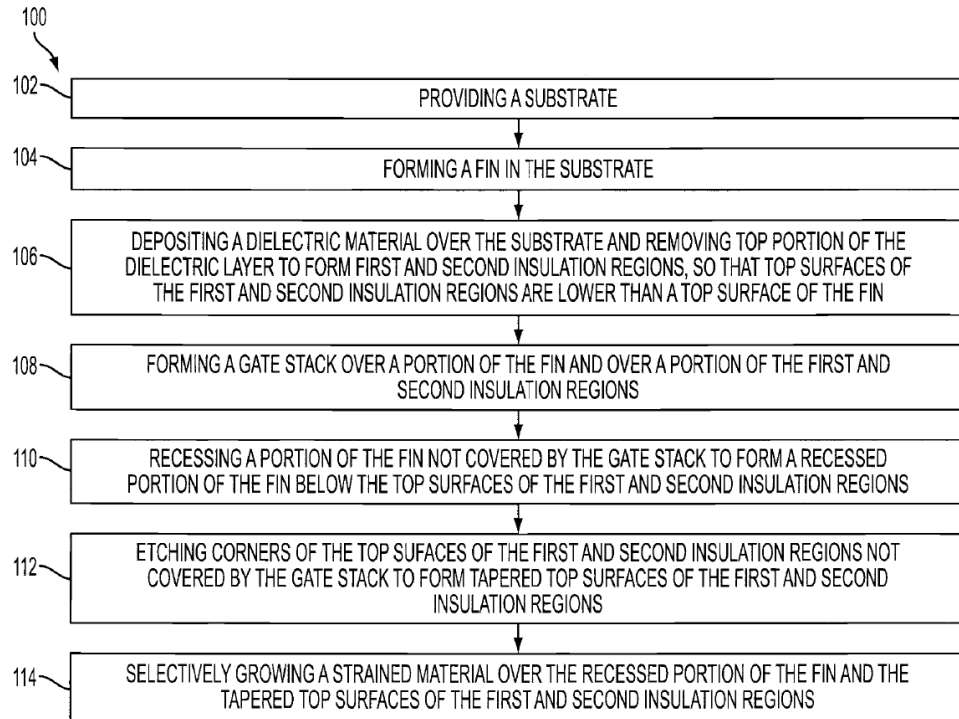


FIG. 1

2. **1[a]: forming a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;**

Lin discloses and renders obvious this limitation. Ex. 1003 at ¶ 146. For example, step 104 of Lin’s fabrication method 100 is “forming a fin in the substrate,” as shown in Figure 1 below. Ex. 1005 at ¶ [0013].

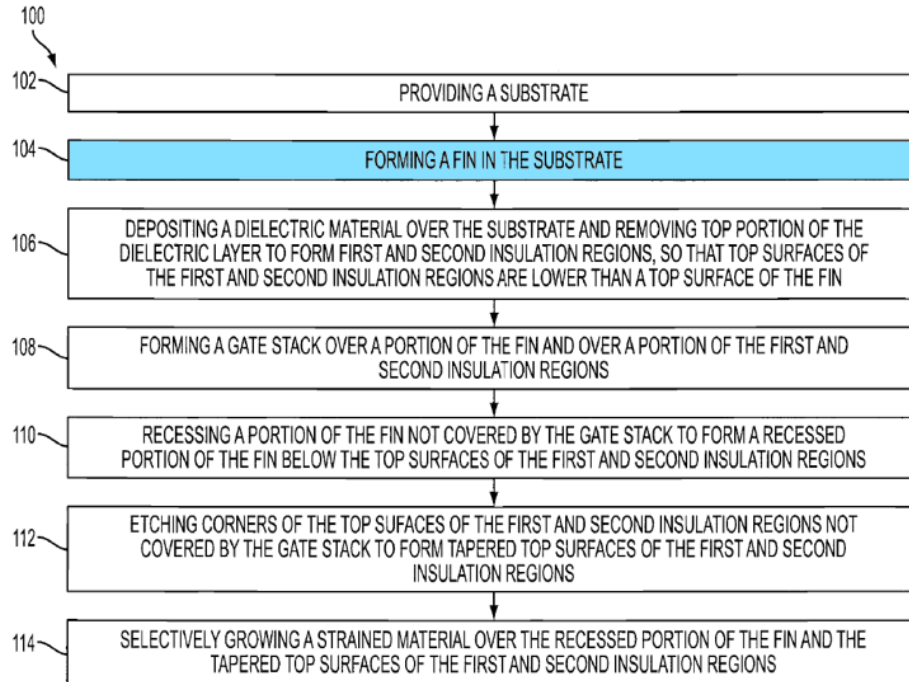


FIG. 1

As shown in Figures 3A and 3B, Lin forms fins 212 (blue) protruding from a surface 202S of substrate 202. See Ex. 1005 at ¶ [0018]; ¶ [0019] (“Portions of the semiconductor substrate 202 between trenches 210 form semiconductor fins 212”).

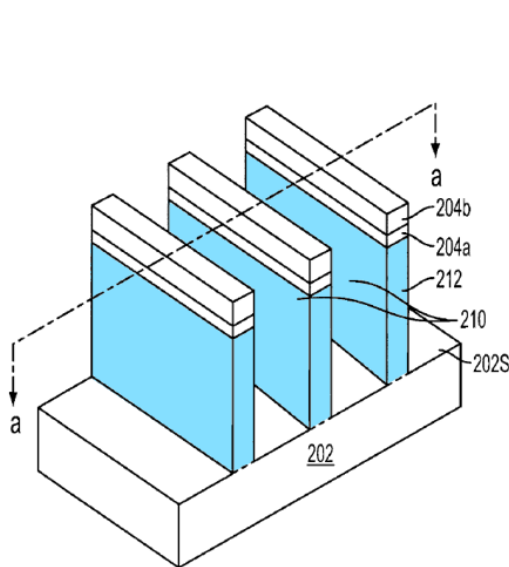


FIG. 3A

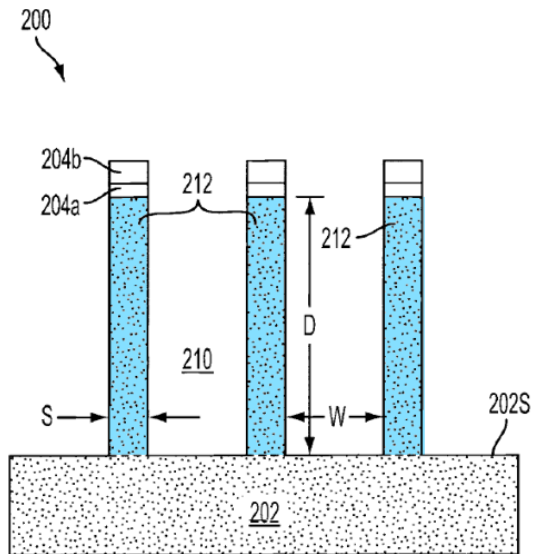


FIG. 3B

As shown in Figures 3A and 3B, the fins 212 each have a top surface and two side surfaces.

3. 1[b]: forming an isolation structure to surround the fin structure;

Lin discloses and renders obvious this limitation. Ex. 1003 at ¶ 149. For example, step 106 of Lin's method 100 includes depositing a dielectric material over the substrate and removing top portion of the dielectric layer to form first and second insulation regions. Ex. 1005 at ¶ [0013].

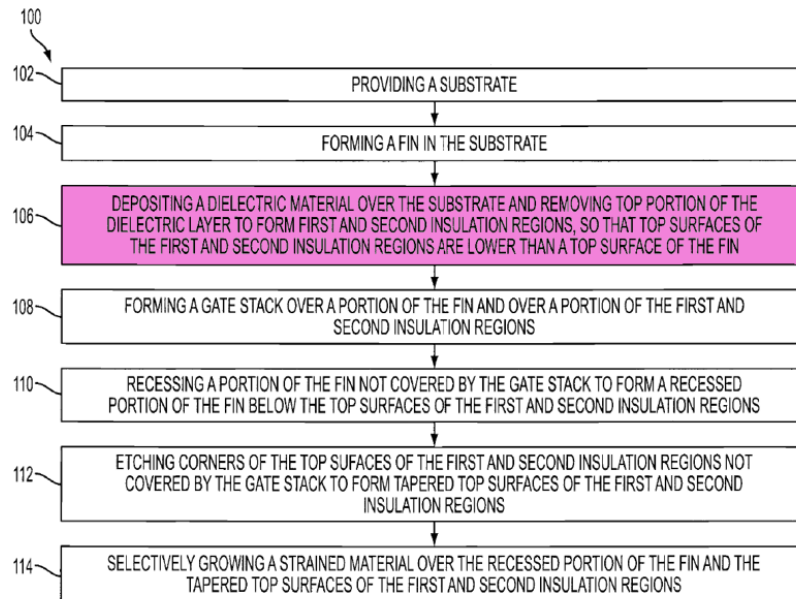


FIG. 1

The resulting insulation regions 216 (the claimed isolation structure) surround the fins 212 as shown in Figures 6A and 6B. *Id.* at ¶ [0026] (“fin 212 between the first and second insulation regions 216a, 216b....”).

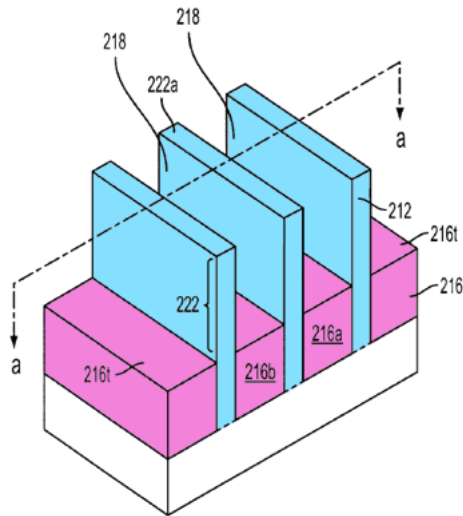


FIG. 6A

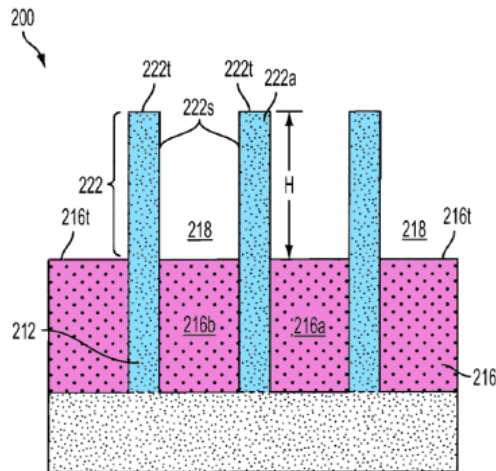


FIG. 6B

A POSITA would have further understood, and it would have been obvious to a POSITA, that the insulation regions 216 are isolation structures because they isolate the transistors that will ultimately be formed from the fins 212 from one another. Ex. 1003 at ¶ 151. Therefore, a POSITA would have understood and found obvious that the insulation regions 216 surround the fins 212 for the resulting transistors to function properly. *Id.*

4. 1[c]: forming a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure, and covering a portion of the isolation structure;

Lin discloses and renders obvious this limitation. Ex. 1003 at ¶ 152. For example, step 108 of Lin's method includes forming a gate stack "over a portion of the fin and over a portion of the first and second insulation regions." Ex. 1005 at ¶ [0013].

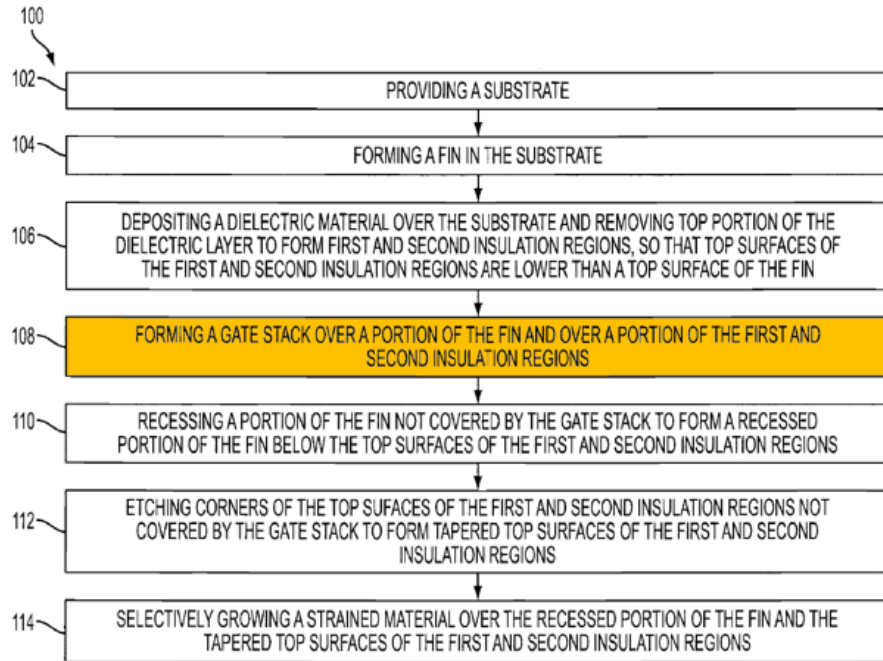


FIG. 1

As shown in Figures 7A and 7B, the gate stack 220 (gold) is formed “over the top surface 222t and sidewalls 222s of a non-recessed portion of the channel fin 222a.” *Id.* at ¶ [0027]. The gate stack 220 also “extend[s] to the flat top surfaces 216t of the first and second insulation regions 216a, 216b.” *Id.*

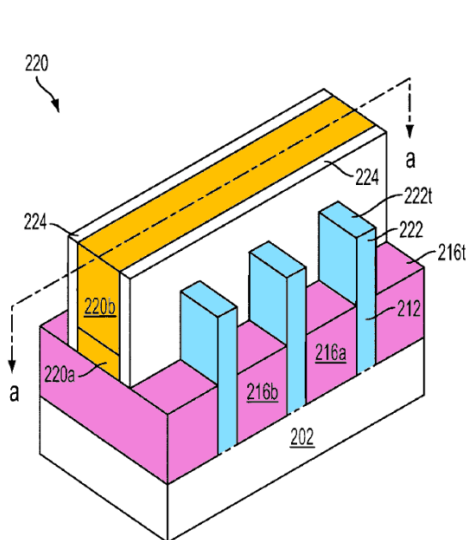


FIG. 7A

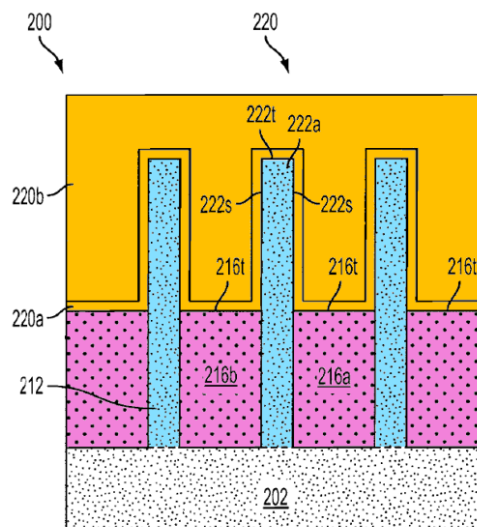


FIG. 7B

5. **1[d]: after the step of forming the gate structure, etching the isolation structure exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth;**

Lin discloses and renders obvious this limitation. Ex. 1003 at ¶ 154. For example, step 112 of Lin’s method 100 includes etching “corners of the top surfaces of the first and second insulation regions not covered by the gate stack . . . to form tapered top surfaces of the first and second insulation region.” Ex. 1005 at ¶ [0013]. As shown in Figure 1, this etching step 112 is performed after forming the gate structure in step 108.

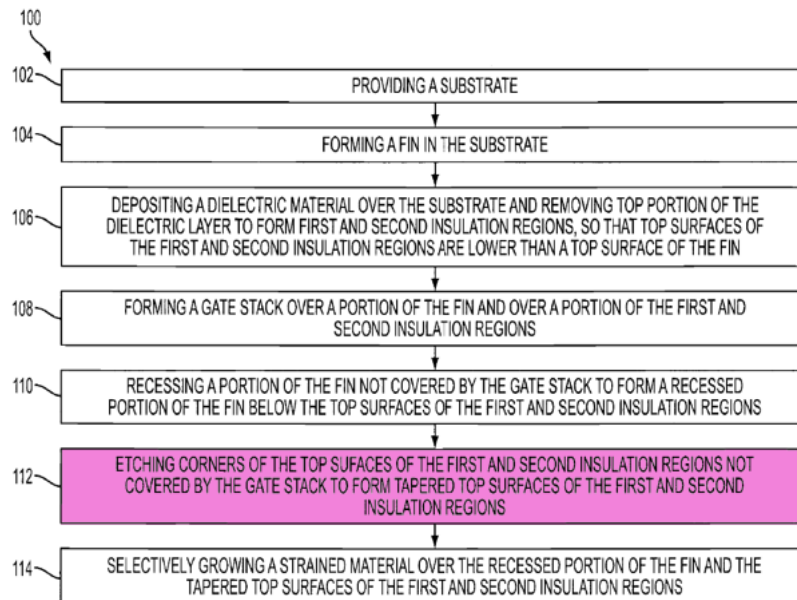


FIG. 1

Lin discloses further etching the “corners of the flat top surfaces 216t of the first and second insulation regions 216a, 216b not covered by the gate stack 220” to “form a curved top portion of the tapered top surface 216u,” as shown in Figure 9C. *Id.* at 8:2-7. According to Lin, “the flat top surface 216t is higher than the highest

point P of the tapered top surface 216u.” *Id.* at ¶ [0034]. Therefore, the second etching step etches the isolation structure exposed from the gate structure with top surface 216t until it is etched down to a first depth with new top surface 216u. *Id.* (“[T]he corners of the flat top surfaces 216t of the first and second insulation regions 216a, 216b not covered by the gate stack 220 are further removed until the flat portion of the tapered top surface 216u disappear to form a curved top portion of the tapered top surface 216u”). The top surface of insulation regions 216a, 216b is a curved surface etched to a minimum depth of D3 and a maximum depth corresponding to the original height of the isolation region minus D2, as shown below. According to Lin, D3 “is in the range of about 0.1 to 0.3 nm.” *Id.*

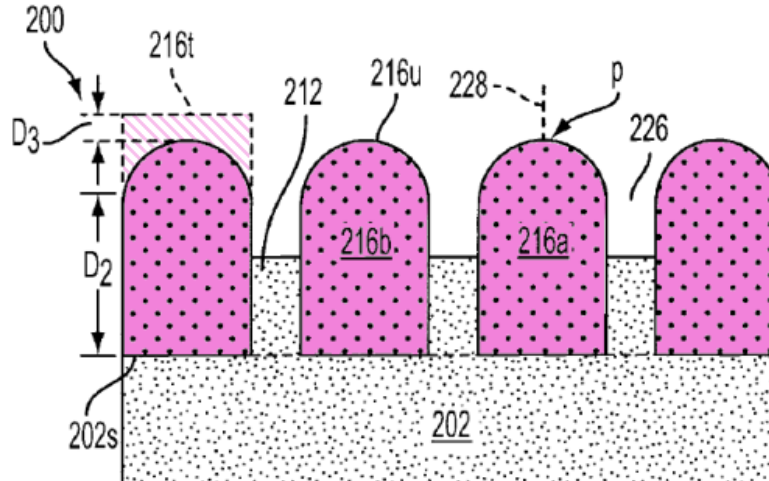


FIG. 9C

6. 1[e]: forming a recess in the fin structure at a side of the gate structure;

Lin discloses and renders obvious this limitation. Ex. 1003 at ¶ 156. For example, step 110 of Lin’s fabrication method 100 includes recessing “a portion of the fin not covered by the gate stack . . . to form a recessed portion of the fin below the top surfaces of the first and second insulation regions.” Ex. 1005 at ¶ [0013].

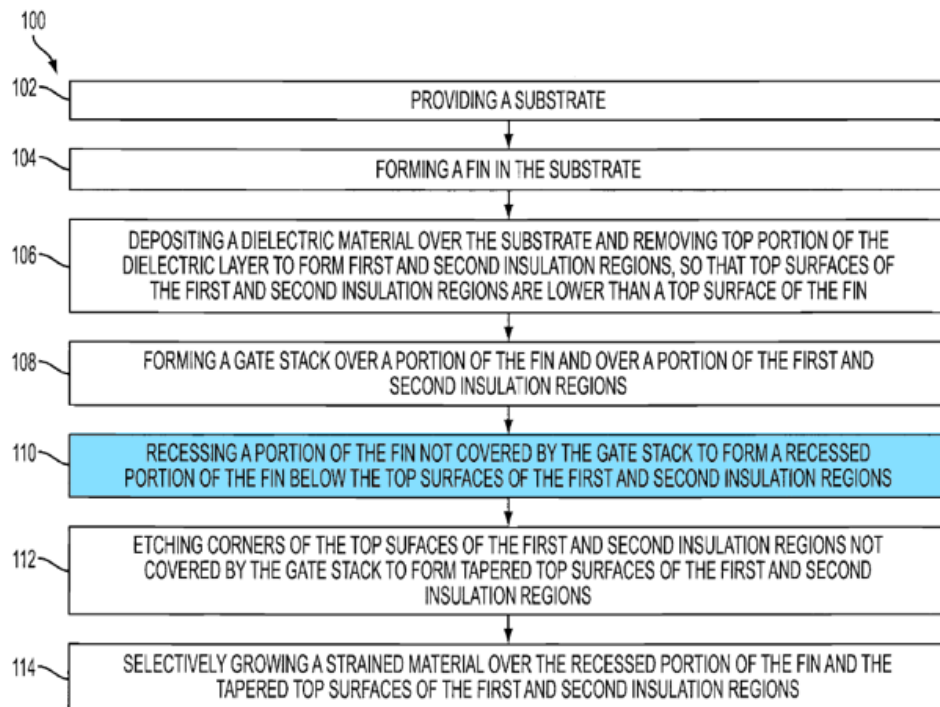


FIG. 1

Figures 8A and 8B illustrate the recessing of the fins 212 (blue) at a side of the gate structure 220 (gold):

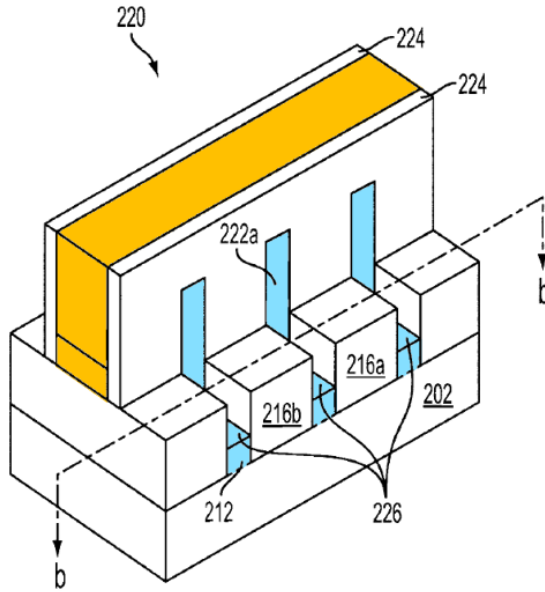


FIG. 8A

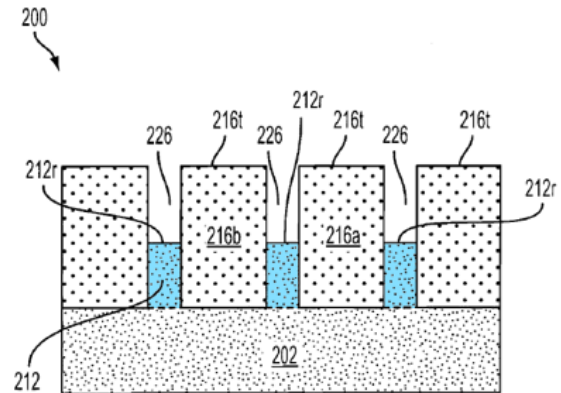


FIG. 8B

Ex. 1005 at Figs. 8A, 8B, cl. 14 (“recessing a portion of the fin ... to form a recessed portion of the fin below the top surfaces of the first and second insulation regions”).

As the '384 Patent expressly discloses, “the timing for etching the isolation structure 20 exposed from the gate structure 30 and the spacers 40 and the timing for etching the fin structures 12 may be reversed.” *Id.* at 6:22-65. Reflecting this, claim 1 does not require a particular order for these steps. Ex. 1001 at cl. 1. In fact, when a particular order is needed, the '384 Patent explicitly requires it. Ex. 1003 at ¶ 158. For example, claim 1 explicitly limits that “etching the isolation structure” is performed “**after** the step of forming the gate structure.” Ex. 1001 at cl. 1. In contrast, claim 1 imposes no temporal requirement on any other steps including between the etching of the fins and the etching of the isolation structure. *Id.* Accordingly, the step of forming a recess is not required to be performed after

etching the isolation structure because “[a]s a general rule, unless the steps of a method claim actually recite an order, the steps are not ordinarily construed to require one.” *Mformation Techs., Inc. v. Rsch. in Motion Ltd.*, 764 F.3d 1392, 1398 (Fed. Cir. 2014) (cleaned up). Likewise, under this general rule, Lin also does not require the sequence of the etching of the fins and the etching of the isolation structure. Ex. 1005 at cl. 14.

To the extent Patent Owner argues that claim 1 requires the fin-recess step 1[e] to occur before the isolation-etching step 1[d], which the Patent Owner cannot because doing so would explicitly contradict its own admission, Lin renders obvious any such temporal requirement. Specifically, a POSITA would have at least found it obvious that etching of the isolation region of Lin can be performed either before or after etching the fin structure. Ex. 1003 at ¶¶ 159-162. As explained by Dr. Lee, both etch steps comprise well-known, conventional processes that a POSITA would have been able to perform in either order to arrive at the same resultant structure, and performing the isolation etch first does not achieve any unexpected results. *Id.* Accordingly, a POSITA would have found it obvious to perform the steps of Lin in this order. *Id.* at ¶ 162. *See also Ex Parte Wilson*, Appeal 2014-003909, 2016 WL 1107699, at *11 (PTAB March 17, 2016) (“a mere change in the timing or sequence of method steps without any new or unexpected results is *prima facie* obvious.”). *See also In re Burhans*, 154 F.2d 690, 692 (C.C.P.A. 1946) (the selection of the order

of process steps is obvious “in the absence of any proof in the record that the order of performing the steps produces any new and unexpected results”). As mentioned above, the ’384 Patent admits that the order can be reversed (Ex. 1001 at 6:22-65), which is consistent with the understanding of the POSITA.

7. 1[f]: forming an epitaxial layer to fill up the recess

Lin discloses and renders obvious this limitation. Ex. 1003 at ¶ 163. For example, Lin’s fabrication method 100 includes step 114 where “a strained material is selectively grown over the recessed portion of the fin and the tapered top surfaces of the first and second insulation regions.” Ex. 1005 at ¶ [0013].

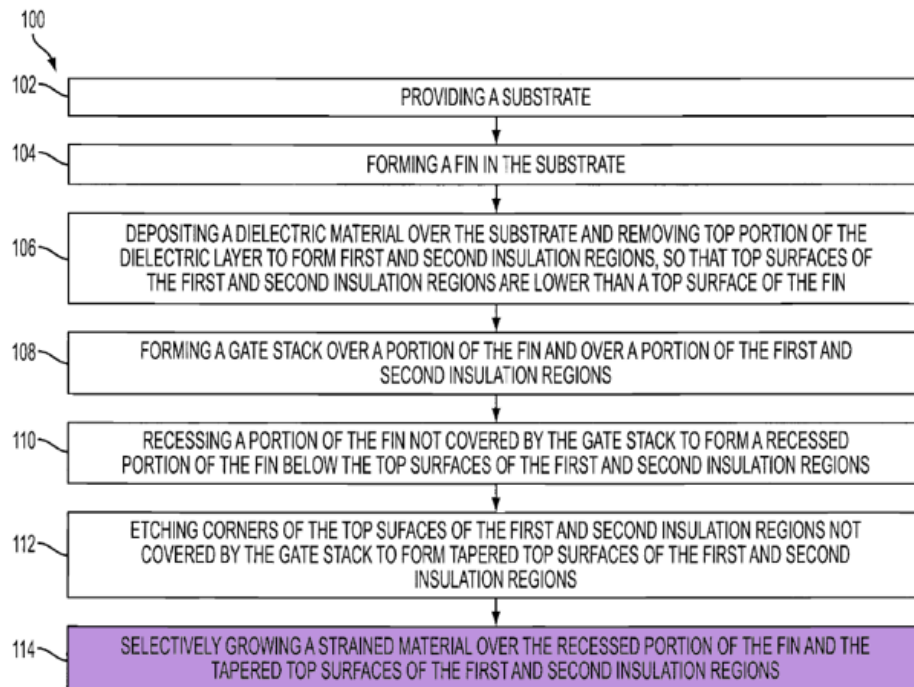


FIG. 1

Figure 10C illustrates the strained material 230 filling the recesses 226 in the fin structure 212. *Id.* at Fig. 10C.

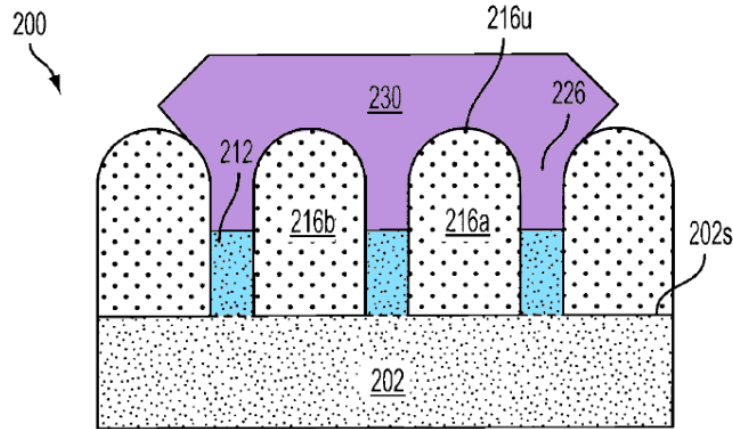


FIG. 10C

Lin further discloses that strained material 230 is an epitaxial layer because it can be silicon carbon (SiC) that is “epi-grown by a LPCVD process to form the source and drain regions of the n-type FinFET.” *Id.* at ¶ [0035]. Additionally, the strained material can be “silicon germanium (SiGe)” that “is epi-grown by a LPCVD process to form the source and drain regions of the p-type FinFET.” *Id.*

8. 1[g]: wherein a bottom surface of the recess has a second depth, and the second depth is deeper than the first depth.

Lin discloses and renders obvious this limitation. Ex. 1003 at ¶ 166. For example, Lin discloses that when the recesses 226 are formed they have a top surface 212r that is “below the flat top surfaces 216t of the first and second insulation regions 216a, 216b.” Ex. 1005 at ¶ [0031]. Further, in Figure 9C the bottom surface of the recess 226 is the top surface of the remaining fin portion 212. Ex. 1003 at ¶ 166.

The depth of this surface (the claimed second depth) is shown as D_R in cyan and is deeper than the first depth D_3 .³ *Id.*

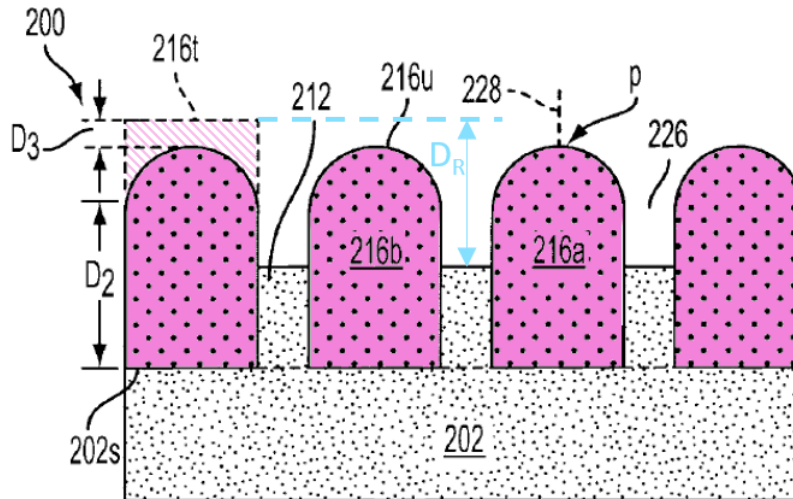


FIG. 9C

C. Claim 2: The fabrication method according to claim 1, wherein the isolation structure is a shallow trench isolation structure.

As discussed above, Lin discloses and renders obvious the fabrication method according to claim 1. Lin further discloses and renders obvious the additional limitation of claim 2. Ex. 1003 at ¶ 167. For example, Lin discloses forming insulation regions between fins (alternately referred to as “*isolation region[s]*”) by depositing insulation material in trenches 210. *See* Ex. 1005 at Figures 3A-5B, ¶¶ [0023]-[0025]. A POSITA would have understood Lin’s process comprises forming

³ The second depth is D_R is deeper even if the first depth is taken as the deepest portion of the tapered top surface 216u. Ex. 1003 at ¶ 166, n.7.

a shallow trench isolation (STI) structure. Ex. 1003 at ¶¶ 168-170. For example, a POSITA would have recognized the process steps disclosed for forming this insulation (*i.e.*, etching trenches into a silicon substrate and filling them with oxide) as the hallmarks of STI technology which “is the preferred method for device isolation in advanced wafer fabs.” *Id.* at ¶ 169 (quoting Ex. 1010 at 25).

Furthermore, a shallow trench isolation structure would have been obvious in view of the knowledge of a POSITA. *Id.* For example, as early as 2001, “[s]hallow trench isolation (STI) is the preferred method for device isolation in advanced wafer fabs.” Ex. 1010 at 25. A POSITA would have been motivated to use the “preferred method for device isolation” for what Lin variously refers to as “isolation region[s]” and “insulation regions.” Ex. 1005 at ¶ [0025].

D. Claim 3: The fabrication method according to claim 1, wherein a step for etching the isolation structure comprises wet etching or dry etching.

As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin further discloses and renders obvious the additional limitation of claim 3. Ex. 1003 at ¶ 171. Specifically, Lin discloses that the etching of the isolation regions illustrated in Figures 9A-9C can be performed with either wet or dry etching: “In one embodiment, the etching step may be performed using a wet etching process, for example, by dipping the substrate 202 in hydrofluoric acid (HF).” Ex. 1005 at ¶ [0032]. “In another embodiment, the etching step may be

performed using a non-biased dry etching process, for example, the dry etching process may be performed using CHF_3 or BF_3 as etching gases.” *Id.*

E. Claim 5: The fabrication method according to claim 1, wherein a step for forming the recess comprises wet etching or dry etching.

As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin further discloses and renders obvious the additional limitation of claim 5. Ex. 1003 at ¶ 172. For example, Lin discloses the etching of the fin 212 to form the recessed portion 226 can be performed using a dry etching process. *Id.* Lin discloses a “biased etching process” that “may be performed under a pressure of about 1 mTorr to 1000 mTorr... [and] using a HBr and/or Cl_2 as etch gases.” Ex. 1005 at ¶ [0031]. A POSITA would have understood that this process is a dry etching process at least because it uses etch gases rather than an etching liquid. Ex. 1003 at ¶ 173. For example, HBr and Cl_2 were both known to be used in plasma etching, which is a form of dry etching. *Id.* (citing Ex. 1024 at 97-99).

F. Claim 6: The fabrication method according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin further discloses and renders obvious the additional limitation of claim 6. Ex. 1003 at ¶ 174. For example, Lin discloses that the strained material 230 (the epitaxial structure as shown above for limitation 1.f) can be silicon germanium (SiGe) in a p-type FinFET and is “epi-grown” (*i.e.*, “epitaxially grown”).

Ex. 1005 at ¶ [0035]; Ex. 1003 at ¶ 174. Lin also discloses that in an n-type FinFET, the strained material 230 can be silicon carbon (SiC), another name for silicon carbide and is also “epi-grown.” *Id.* It also would have been obvious to a POSITA to dope the silicon carbide with phosphorous to form phosphor-doped silicon carbide. Ex. 1003 at ¶ 174. For example, Lin teaches that phosphorous is an n-type dopant, which also would have been well-known to a POSITA. Ex. 1005 at ¶ [0016].

G. Claim 7: The fabrication method according to claim 1, further comprising forming a spacer before etching the isolation structure, wherein the spacer is disposed on a sidewall of the gate structure.

As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin further discloses and renders obvious the additional limitation of claim 7. Ex. 1003 at ¶ 175. For example, before the etching of the isolation structure depicted in Figs. 9A-9C, Lin discloses spacers 224 (dark blue) that are formed “on two sides of the gate stack 220” (gold) in Figs 7A-7B. Ex. 1005 at ¶ [0030].

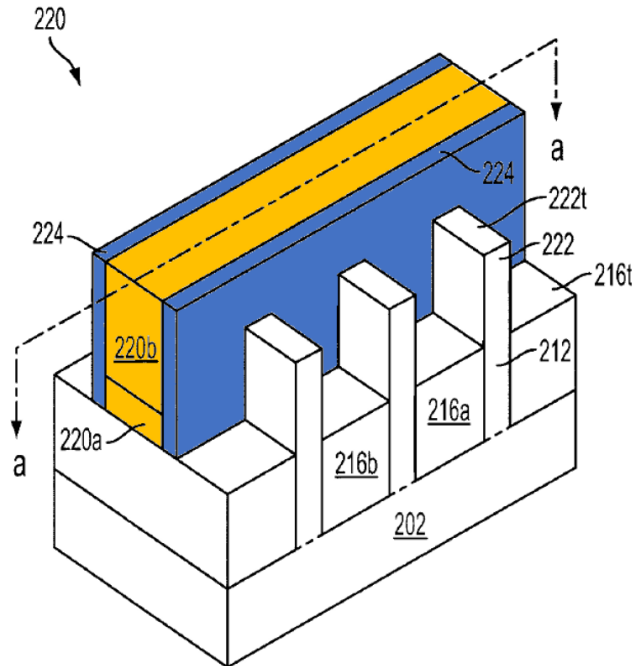


FIG. 7A

Specifically, Lin discloses that “a dielectric layer 224 [is] formed over the substrate” and then “etching is performed on the dielectric layer 224 to form *a pair of spacers 224* on two sides of the gate stack 220.” *Id.* (emphasis added). Because these spacers are present when Lin’s isolation structure is etched, as shown in Figs. 8A-9C, a POSITA would have understood that the spacer formation occurs “before etching the isolation structure” as claimed. Ex. 1003 at ¶ 176.

H. Claim 8: The fabrication method according to claim 7, wherein a step for forming the spacer comprises: depositing a material layer to conformally cover the gate structure and the fin structure, and etching the material layer until the isolation structure is exposed.

As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin further discloses and renders obvious the additional limitation of

claim 8. Ex. 1003 at ¶ 177. Lin discloses that forming the spacer comprises forming a “blanket layer of the dielectric layer 224.” Ex. 1005 at ¶ [0030]. Lin further discloses that dielectric layer 224 may be formed by CVD and ALD (*id.*), which a POSITA would have understood are conformal deposition processes designed to uniformly coat all exposed surfaces. Ex. 1003 at ¶ 177. Because the gate structure and fin structure exist and are exposed at this point of the fabrication method, a POSITA would have understood and found obvious that this blanket layer conformally covers the gate structure and the fin structure. Ex. 1003 at ¶ 177.

Lin further discloses etching the blanket layer to form a pair of spacers 224 on the sides of the gate stack 220. Ex. 1005 at ¶ [0030]. As shown in Figure 7A, above, the isolation structure 216 is exposed as a result of this etching. *Id.* at Fig. 7. Additionally, spacers were well-known in the art and were used to isolate the gate structure from the source/drain regions of a transistor. Ex. 1003 at ¶ 178. Thus, the function of the well-known spacers dictates that it would not cover the entire isolation structure but only needs to be disposed on the sidewalls of the gate structure. *Id.*

VII. Ground 2B: Claims 4 and 9 Are Obvious Over Lin in View of Brask

A. A POSITA would have been motivated to combine Lin and Brask

Lin discloses a “gate-first” fabrication process where the operative metal gate is formed before the source and drain regions of the transistor. Ex. 1003 at ¶ 180.

But by the priority date of the '384 patent, POSITAs would have understood that “gate-first” processes would expose the gate structure to the “high activation anneal for the junctions” thereby degrading performance of the transistor. Ex. 1008 at 16; *see also* Ex. 1012 at xxiii (describing thermal annealing at high temperature to remove damage caused by ion implantation), 17 (“Thermal annealing is a required step after implantation.”); Ex. 1006 at ¶ [0069]; Ex. 1003 at ¶ 180. A POSITA also would have understood that gate-last processing avoids this issue by deferring gate formation until after the annealing step, thereby enabling tighter control of the gate “work function for nMOS and pMOS [devices].” Ex. 1008 at 16. For this reason, by 2013, there was an industry-wide “shift from ‘gate first’ to ‘gate last’ processing.” *Id.*; Ex. 1003 at ¶ 180.

A POSITA therefore would have been motivated to modify Lin’s gate-first process by adopting a gate-last approach, such as the process taught by Brask, in order to avoid thermal degradation of the gate stack. Ex. 1003 at ¶ 181. Specifically, Brask teaches fabricating a FinFET transistor with a gate-last process where a “sacrificial gate electrode” is first formed on the fins. Ex. 1006 at ¶ [0059]; *see id.* at ¶ [0046] (“semiconductor bodies *or fins* 510 and 512”) (emphasis added); Ex. 1003 at ¶ 181. After source/drain regions of the transistor are formed, the sacrificial gate is removed to form an opening 622 exposing the channel region of the fin. Ex. 1006 at ¶ [0072]. The opening is then filled with a gate dielectric layer and gate

electrode material which serve as a “gate dielectric layer” and “gate electrode,” respectively, of the final FinFET device. *Id.* at ¶ [0074]. A POSITA would have understood Brask’s process of forming a sacrificial gate (*i.e.*, “dummy gate”) first, and then removing the sacrificial gate (*i.e.*, “dummy gate”) and replacing it with a metal gate, is a “gate-last” process. Ex. 1003 at ¶ 181 (explaining that Brask’s process comprises the same steps as the “gate last” processing described in Ex. 1008). Brask’s gate-last process is thus a well-known technique applicable to Lin’s FinFET fabrication method, ready for improvement for the reasons described above, and with the predictable results of avoiding exposing the gate to the required high-activation anneal. *Id.*

Further, the combination of Lin and Brask is expressly motivated by the teachings of Brask. For example, Brask discloses that gate-last processing enables tailoring of gate electrode work functions such that performance of the transistor may be “dramatically improved.” Ex. 1006 at ¶ [0058]. This provides an express motivation to combine Brask’s gate-last processing with the teachings of Lin to improve gate control and overall device characteristics. *Id.*; Ex. 1003 at ¶ 182.

In the combination of Lin and Brask, a POSITA would understand that the “gate stack 220” of Lin would instead be formed by depositing a “sacrificial gate electrode” over the fins (Ex. 1006 at ¶ [0059]) as taught by Brask. Fabrication would

proceed through Lin's steps for source/drain formation and remaining features of the FinFET. Ex. 1005 at Fig 1; Ex. 1003 at ¶ 183.

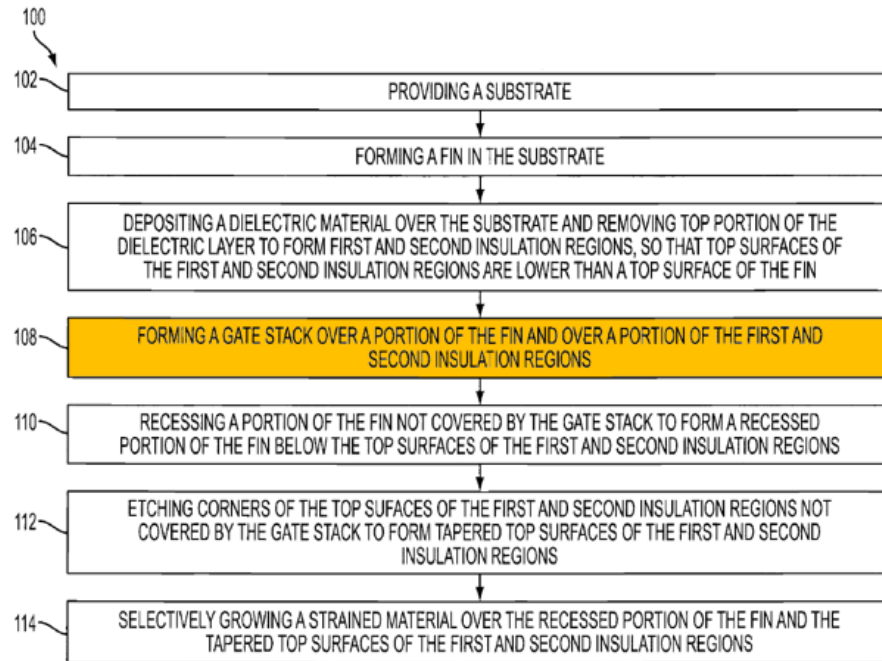


FIG. 1

After formation of the source and drain regions (e.g., in Lin's steps 110, 112, and 114), an interlayer dielectric layer is formed. *See* Ex. 1005 at ¶ [0037]; Ex. 1006 at ¶ [0071]. At that point, a POSITA would understand that the sacrificial gate is removed to form an opening exposing the fin, as taught by Brask. Ex. 1006 at ¶ [0072]. The gate dielectric and metal gate are subsequently formed in that opening. *Id.* at ¶ [0074]. Notably, Lin and Brask disclose highly similar methods forming the final gate structure. Ex. 1003 at ¶ 184. Both teach conformally depositing a gate dielectric layer (Ex. 1005 at ¶ [0030], Figure 7B; Ex. 1006 at ¶ [0074], Figure 6J) followed by forming a metal gate to fill the trench (Ex. 1005 at 6:55-56, Figures 7A-

7B; Ex. 1006 ¶ [0074], Fig. 6J). Ex. 1003 at ¶ 184. These shared steps further support the obviousness of their combination. *Id.* This obvious combination of Lin and Brask discloses all of the limitations of claims 4 and 9, as shown below, rendering those claims obvious to a POSITA.

B. Claim 4: The fabrication method according to claim 1, wherein the gate structure is a dummy gate structure.

As discussed above for Ground 2A, Lin discloses and renders obvious the fabrication method of claim 1. Lin in view of Brask renders obvious claim 4. Ex. 1003 at ¶ 185.

The combination of Lin and Brask teaches a dummy gate structure. Ex. 1003 at ¶ 186. When Lin is combined with Brask as discussed above, the fabrication method will include depositing a “a sacrificial gate electrode.” Ex. 1006 at ¶ [0060]. A POSITA would have recognized that the “sacrificial gate electrode” is a “dummy gate structure” because it is not an operative gate and will subsequently be replaced. Ex. 1003 at ¶ 186.

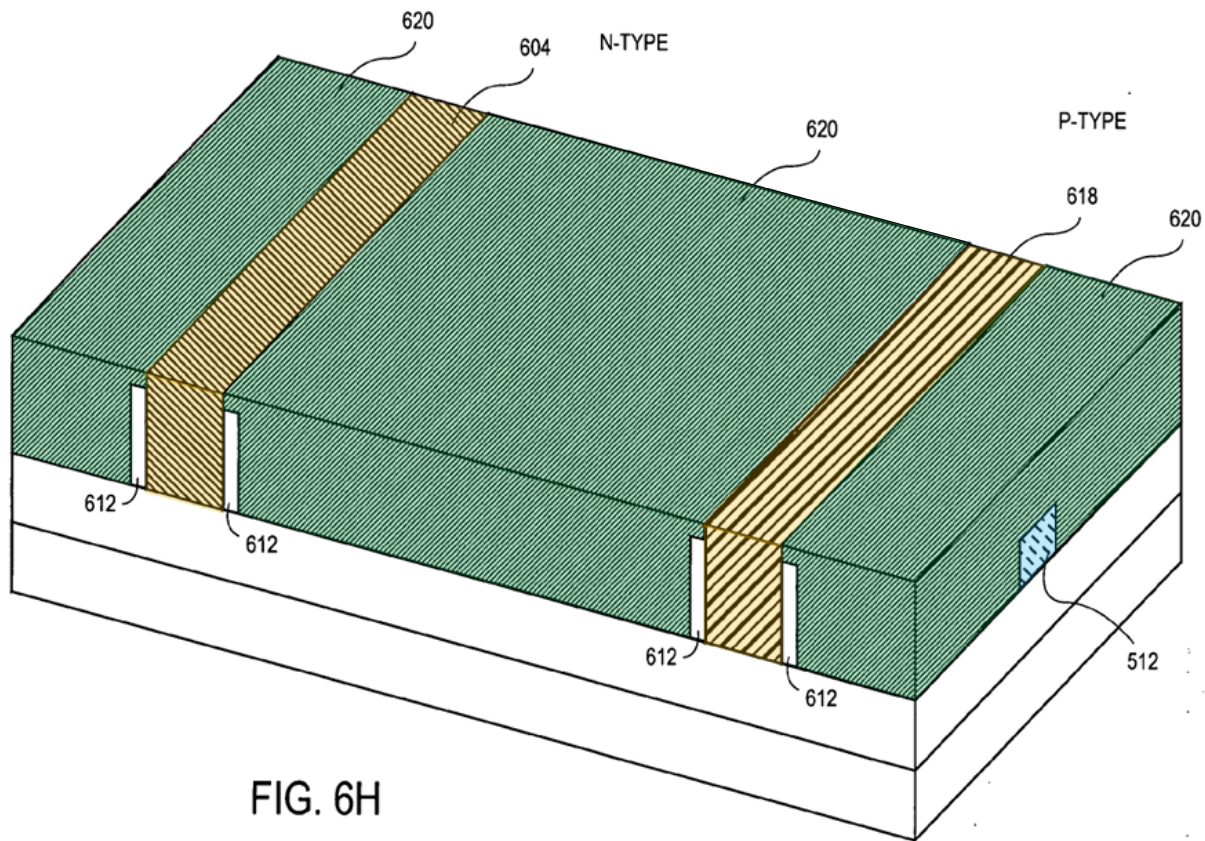
C. Claim 9

1. 9[pre]: The fabrication method according to claim 1, further comprising:

As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin in view of Brask renders obvious claim 9. Ex. 1003 at ¶ 187.

2. 9[a]: depositing an interlayer dielectric to surround the gate structure;

Lin in view of Brask renders obvious this limitation. Ex. 1003 at ¶ 188. For example, Lin expressly recognizes that the FinFET device 200 “may undergo further CMOS processes to form various features,” such as “dielectric layers.” Ex. 1005 at [0037]. A POSITA would have recognized that the Lin-Brask combination will also comprise depositing an interlayer dielectric to surround the gate structure. Ex. 1003 at ¶ 188. Brask also teaches depositing a dielectric layer 620 after the “sacrificial gate electrode” is deposited. Ex. 1006 at ¶ [0071]. As described in section V.D.2., *supra*, a POSITA would have understood this dielectric layer to be an “interlayer dielectric” as claimed. Ex. 1003 at ¶ 188. As shown in Figure 6H of Brask, dielectric layer 620 (green) surrounds the sacrificial gate electrode (gold):



Further, as described above for Grounds 1A and 1B, ILDs were well-known to a POSITA before 2013 and used for “isolating electrically conducting and semiconducting features and films” in transistors. *See* Ex. 1010 at 27 (“The interlayer dielectric (ILD) is used between different metal layers has traditionally been silicon dioxide (doped or undoped).”); Ex. 1011 at v. A POSITA would have understood and found obvious that to isolate the “electrically conducting” metal gate that will subsequently be formed, the interlayer dielectric would be deposited to surround the gate structure of the Lin-Brask combination. Ex. 1003 at ¶ 190.

3. 9[b]: removing the gate structure to leave a trench;

Lin in view of Brask renders obvious this limitation. Ex. 1003 at ¶ 191. For example, when Brask’s gate-last process is combined with Lin as discussed above, “the sacrificial gate electrode 604 is [] removed” thereby forming “an opening 622 where the gate electrode” is to be formed, as taught by Brask. Ex. 1006 at ¶ [0072]. Brask’s Figure 6I illustrates the opening (*i.e.*, “trench”) after removing the sacrificial gate, which will also be present in the Lin-Brask combination. Ex. 1003 at ¶ 191.

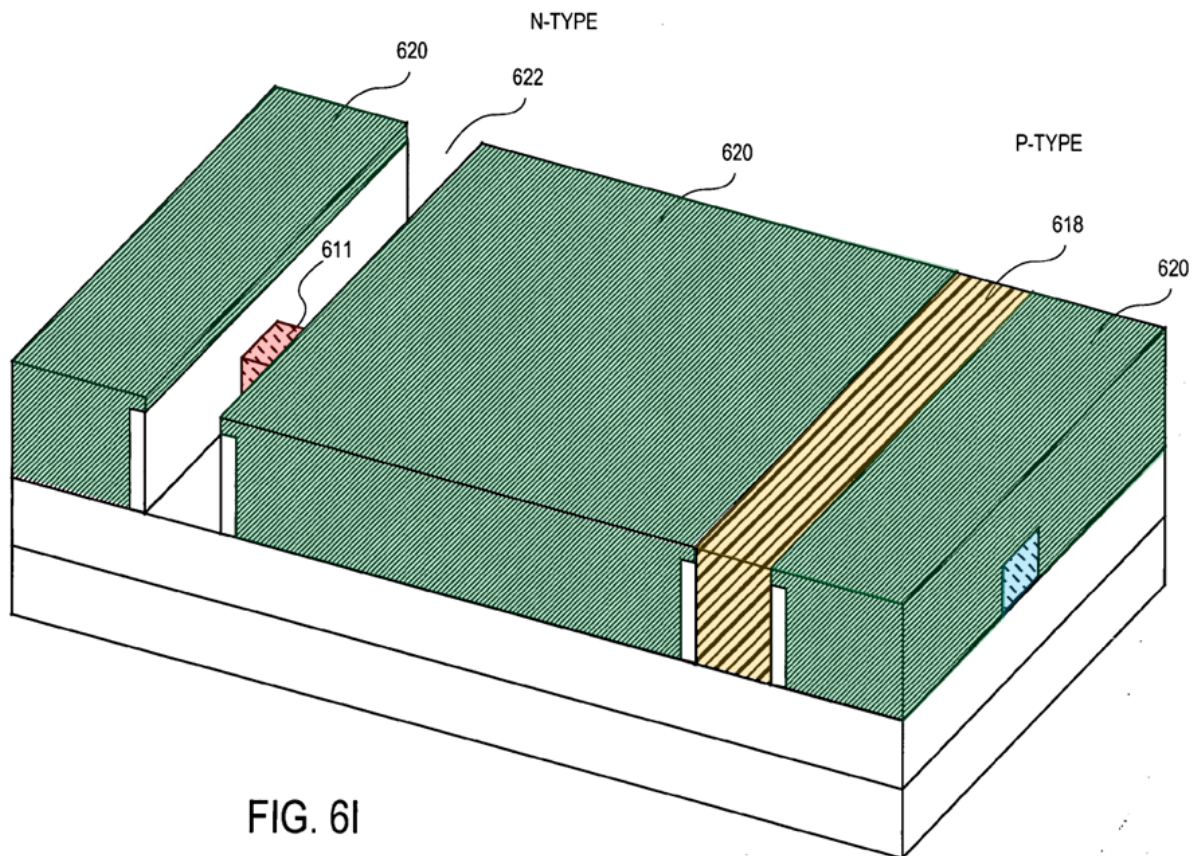
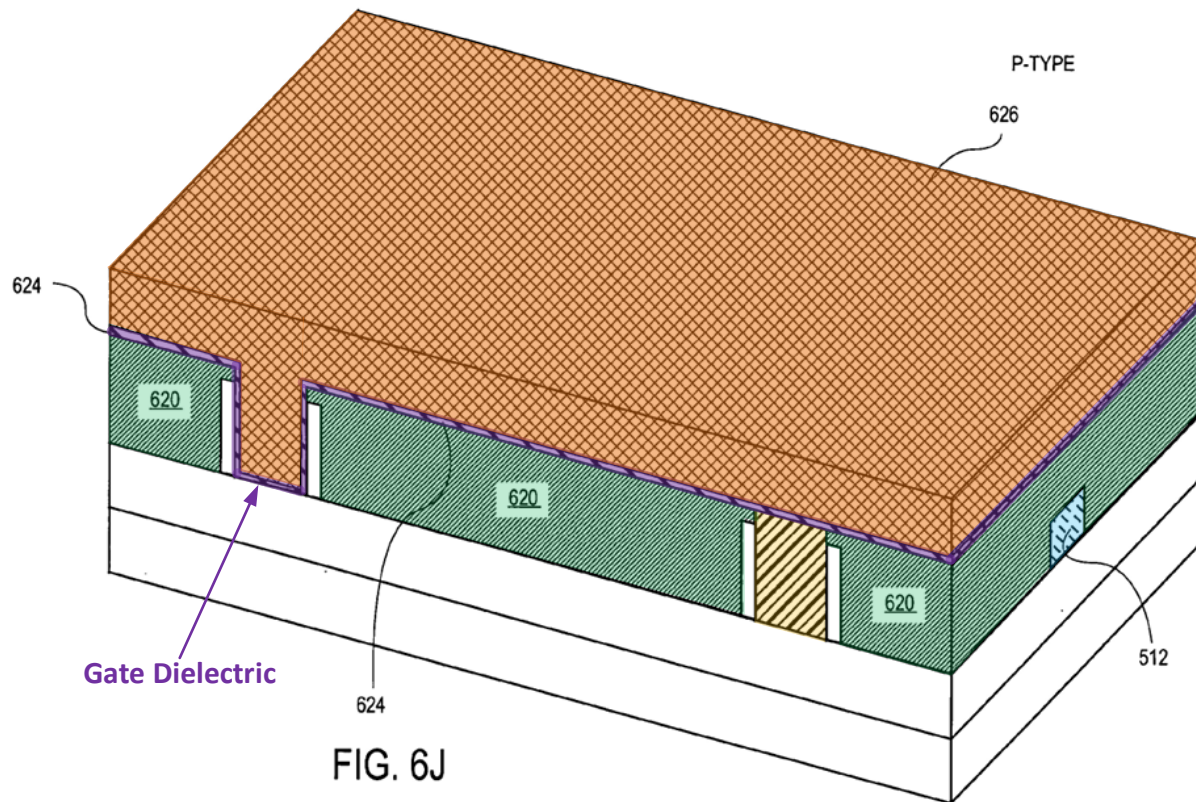


FIG. 6I

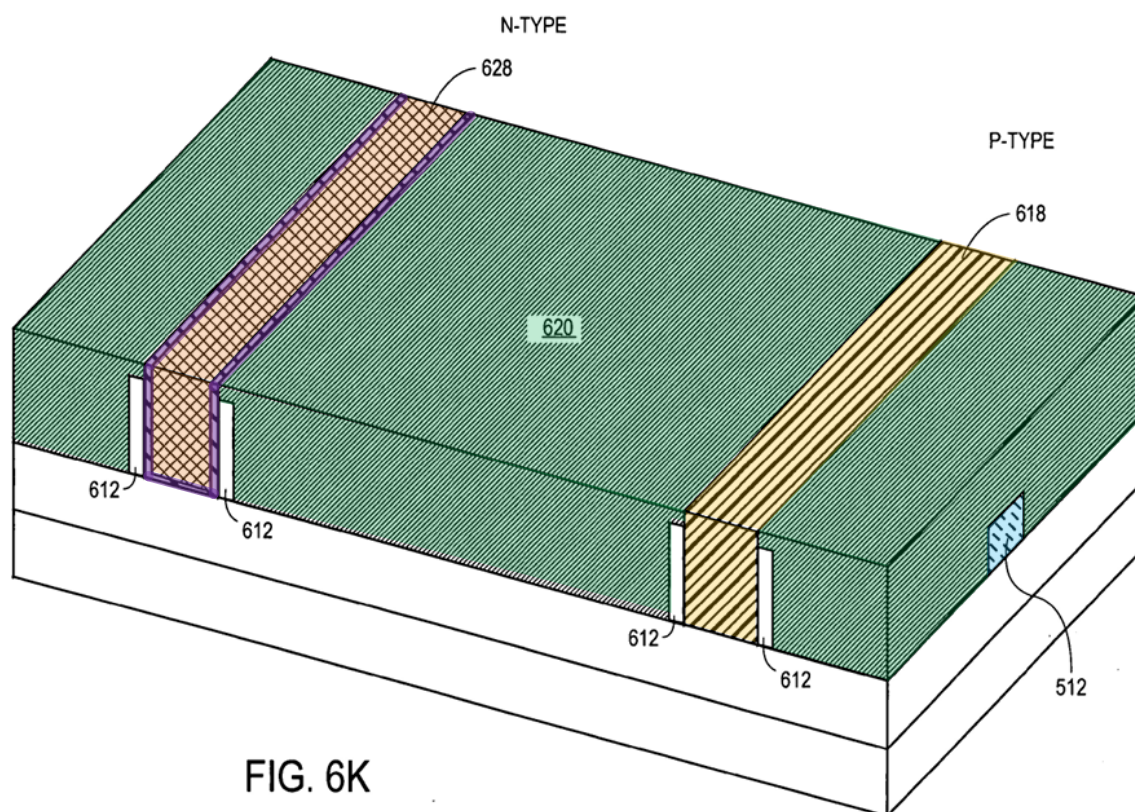
4. 9[c]: forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench; and

Lin in view of Brask renders obvious this limitation. Ex. 1003 at ¶ 192. For example, when Brask’s gate-last process is combined with Lin as discussed above, the process will include “a conformal deposition process, such as CVD or ALD ... to deposit a high K gate dielectric layer” in the trench, as taught by Brask. Ex. 1006 at ¶ [0074]. As shown in Figure 6J, the dielectric layer 624 (purple) of Brask conformally covers a sidewall and a bottom of the trench, which will also be present in the Lin-Brask combination. Ex. 1003 at ¶ 192.



5. 9[d]: forming a conductive layer to fill up the trench.

Lin in view of Brask renders obvious this limitation. Ex. 1003 at ¶ 193. For example, when Brask's gate-last process is combined with Lin as discussed above, the process will include blanket depositing a gate electrode material (*i.e.*, "a conductive layer") over the gate dielectric layer, as taught by Brask. Ex. 1006 at ¶ [0074]. Figure 6J of Brask, reproduced above, shows the gate electrode material 626 (orange) filling up the trench. Ex. 1006 at Fig. 6J; Ex. 1003 at ¶ 193. This gate electrode material filling up the trench will also be present in the Lin-Brask combination, and forms the gate electrode of the transistor after planarizing. Ex. 1006 at ¶ [0074], Fig. 6K Ex. 1003 at ¶ 193.



VIII. Mandatory Notices under 37 C.F.R. § 42.8

A. Real Parties-in-Interest

The real party-in-interest is Taiwan Semiconductor Manufacturing Company Limited.

B. Related Matters

The '384 patent is not currently the subject of any litigation.

C. Grounds for Standing

Petitioner certifies that the '384 patent is available for *inter partes* review and that TSMC is not barred from requesting this proceeding.

D. Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner designates the following lead and backup counsel:

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Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney from TSMC is attached. TSMC consents to electronic service.

E. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a) to Deposit Account No. 506269.

IX. Conclusion

For the reasons set forth above, Petitioner TSMC respectfully requests *inter partes* review of the challenged claims of the '384 patent.

Dated: July 8, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing petition for *Inter Partes* Review of U.S. Patent No. 8,993,384, including all Exhibits, was served on July 8, 2025 via Express Mail delivery directed to the attorney of record for the patent at the following address:

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CERTIFICATE OF WORD COUNT UNDER 37 C.F.R. § 42.24(a)

I, the undersigned, do hereby certify that the attached petition contains 13,969 words, as measured by the Word Count function of Microsoft Word, excluding this Certification and the following: Table of Contents, Table of Authorities, List of Exhibits, Mandatory Notices, and Certificate of Service. This is less than the limit of 14,000 words as specified by 37 C.F.R. § 42.24(a)(i).

Date: July 8, 2025

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