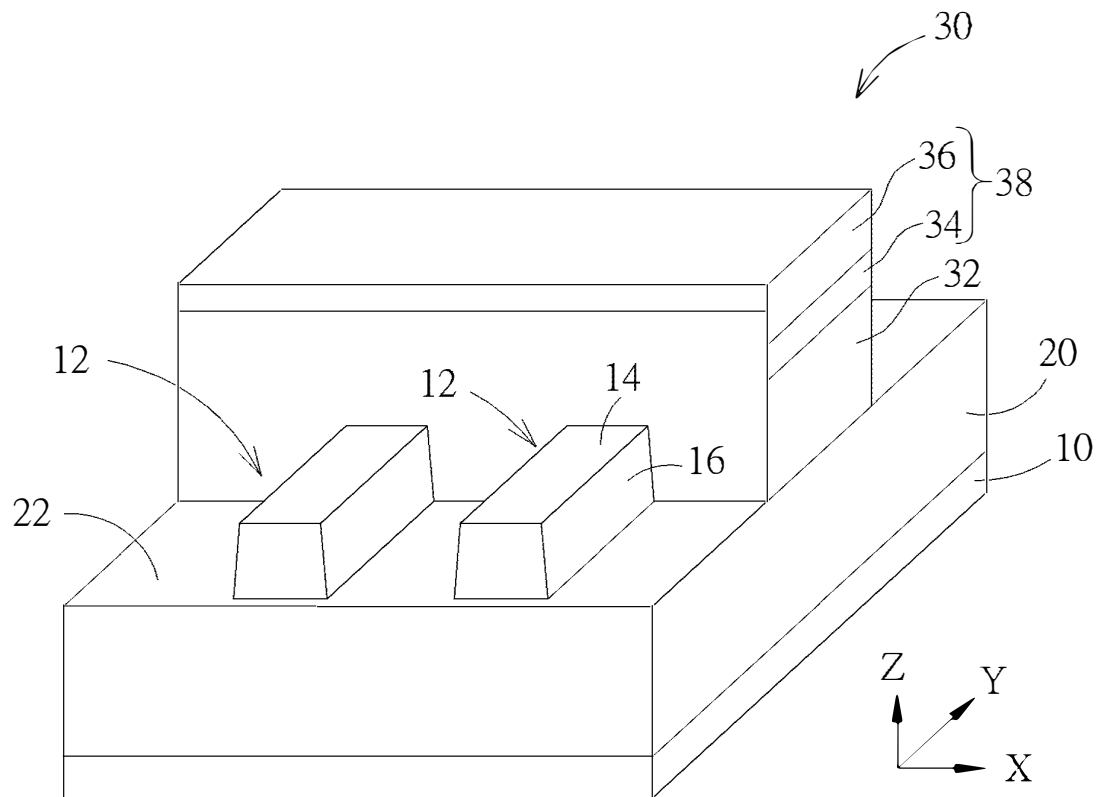
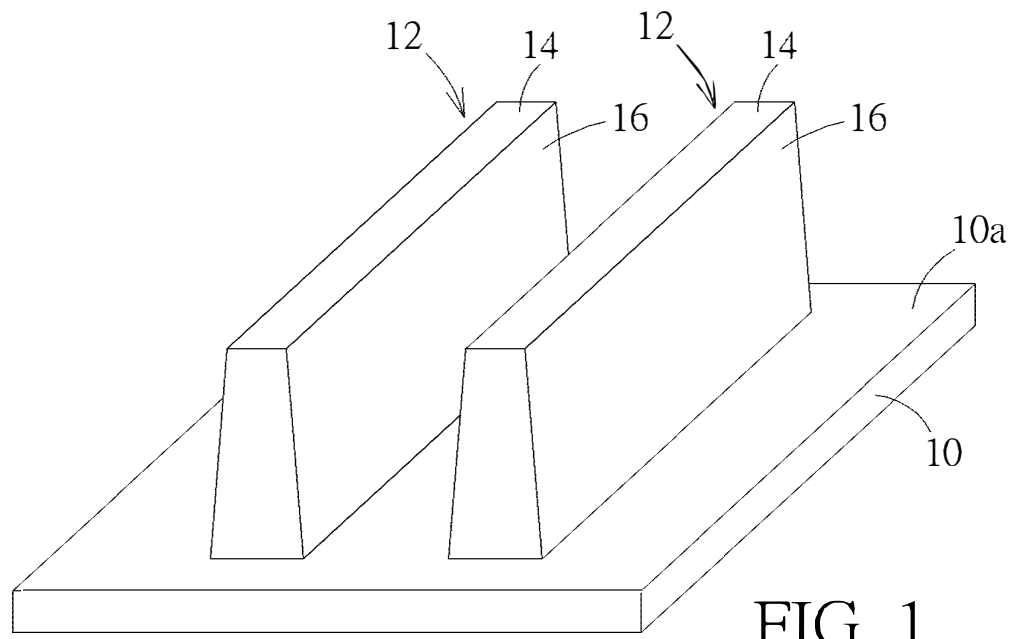




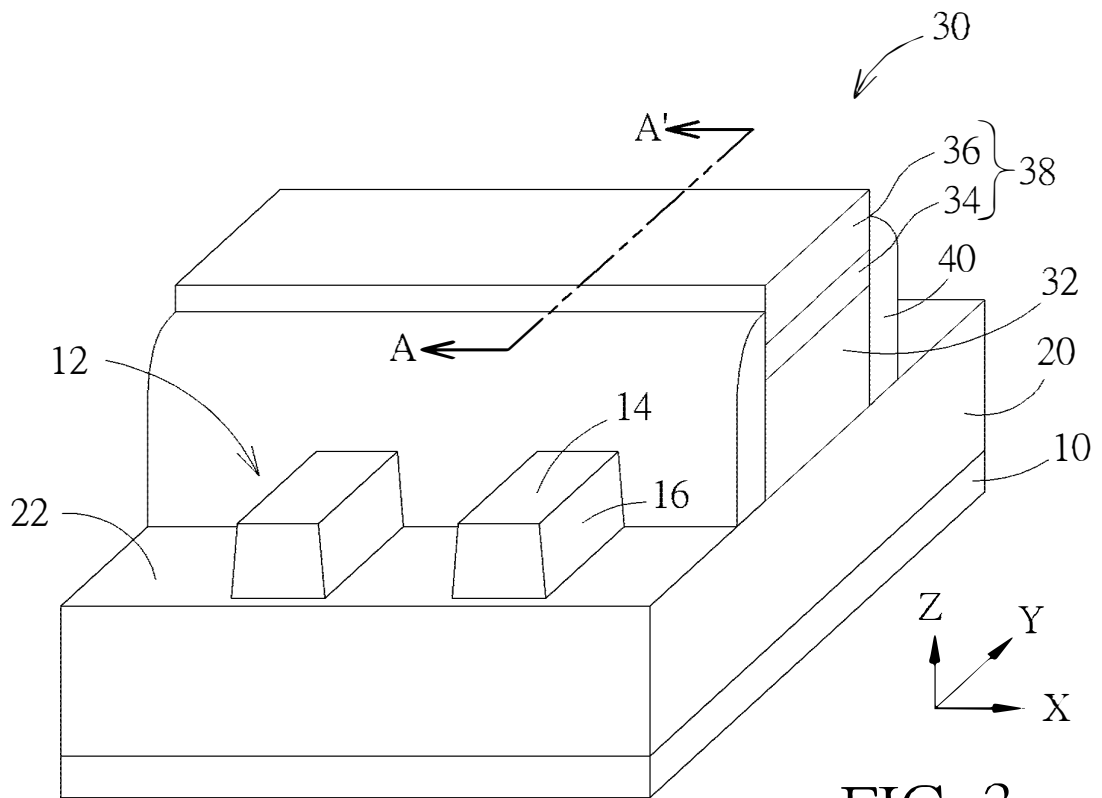


FIG. 3

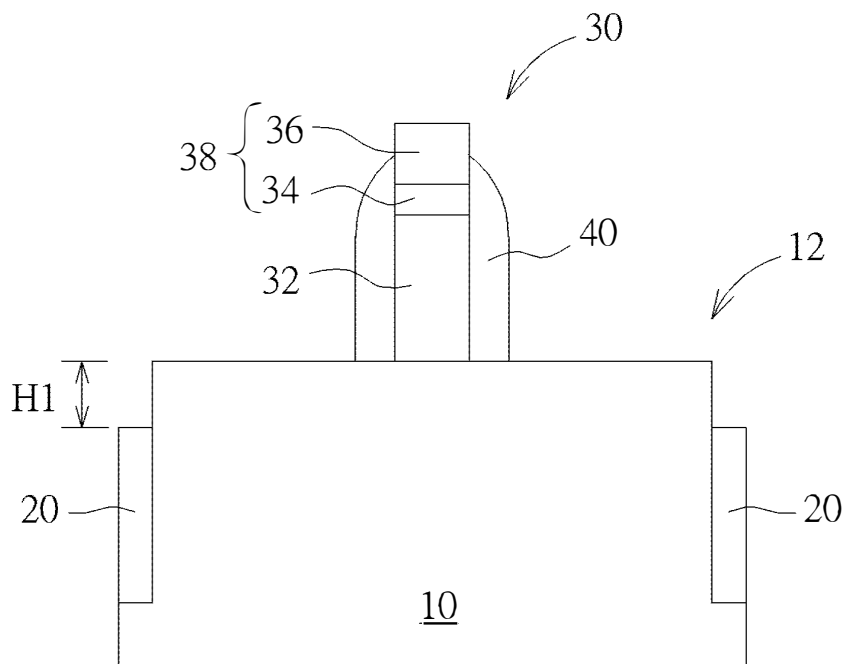
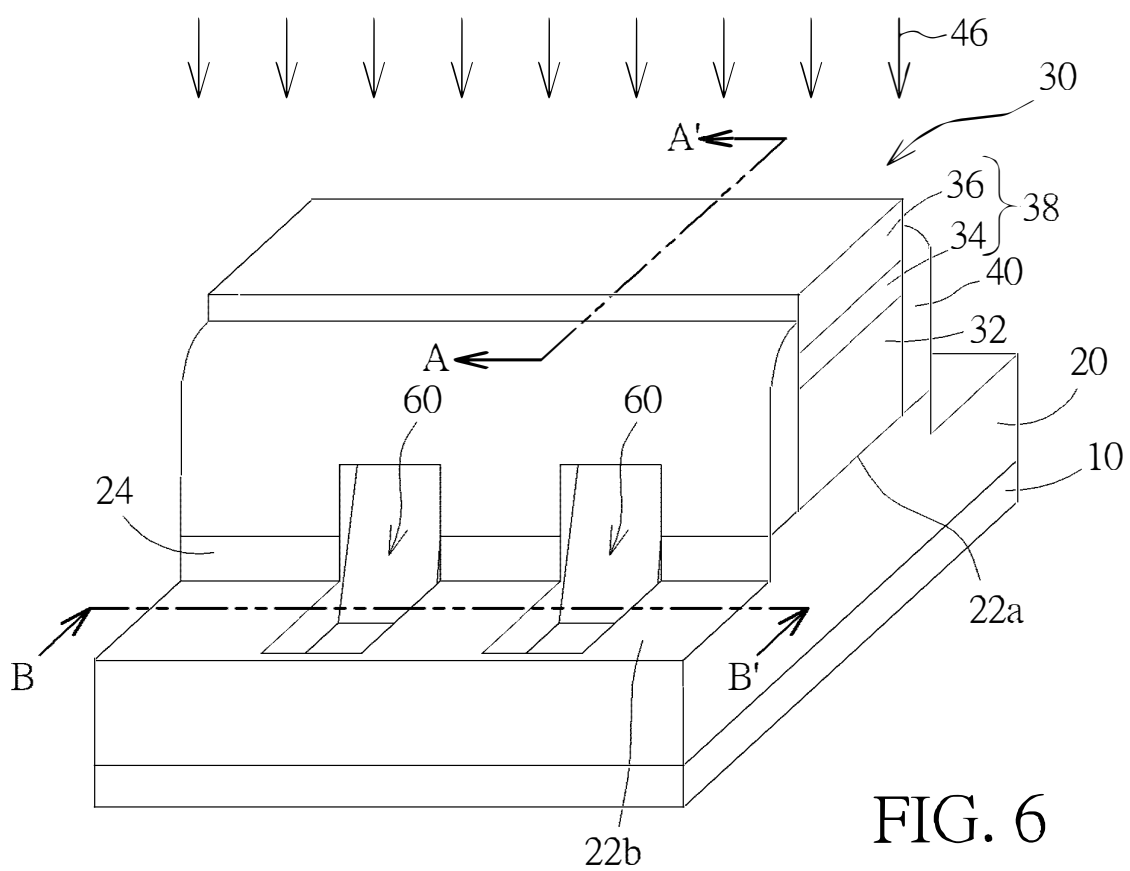
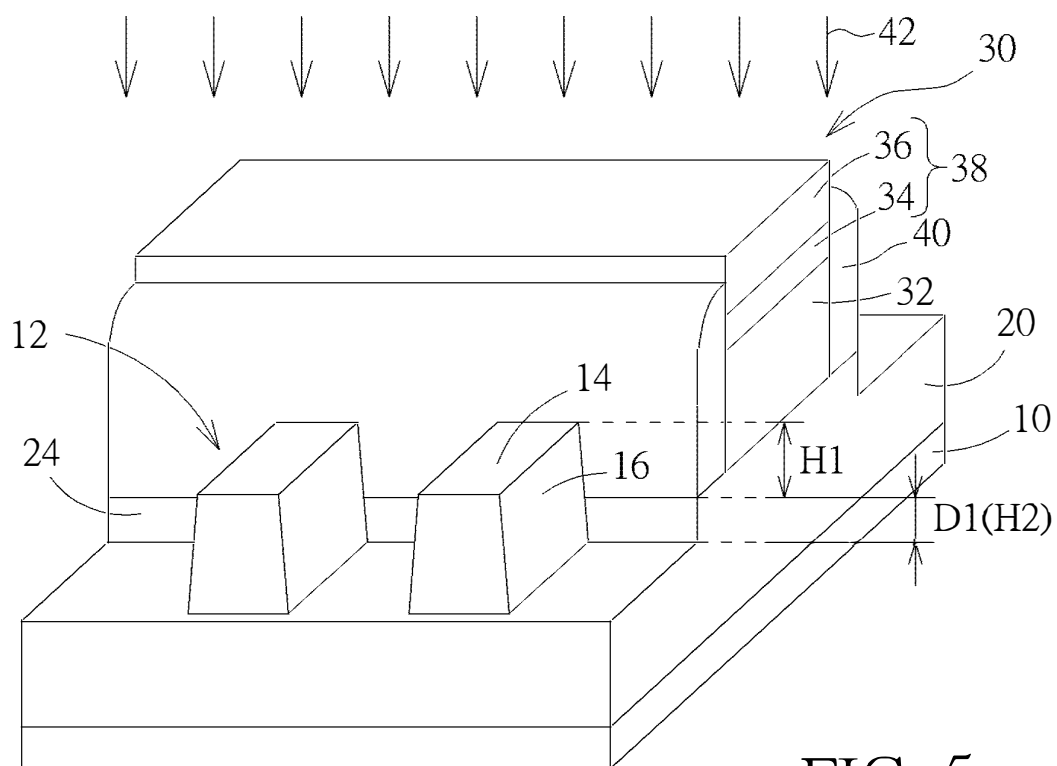


FIG. 4



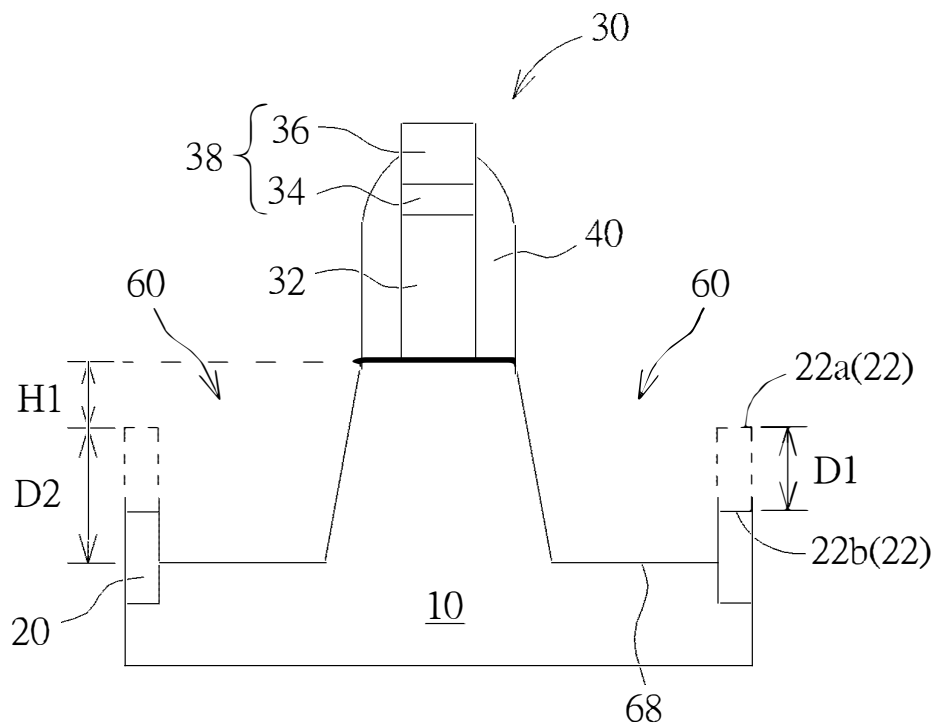


FIG. 7

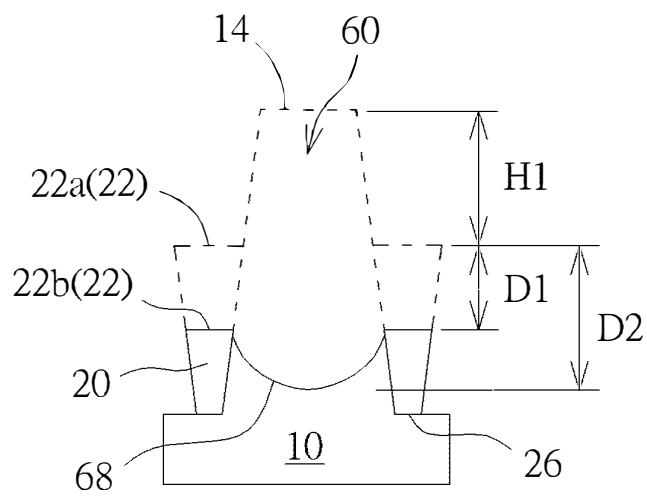


FIG. 8

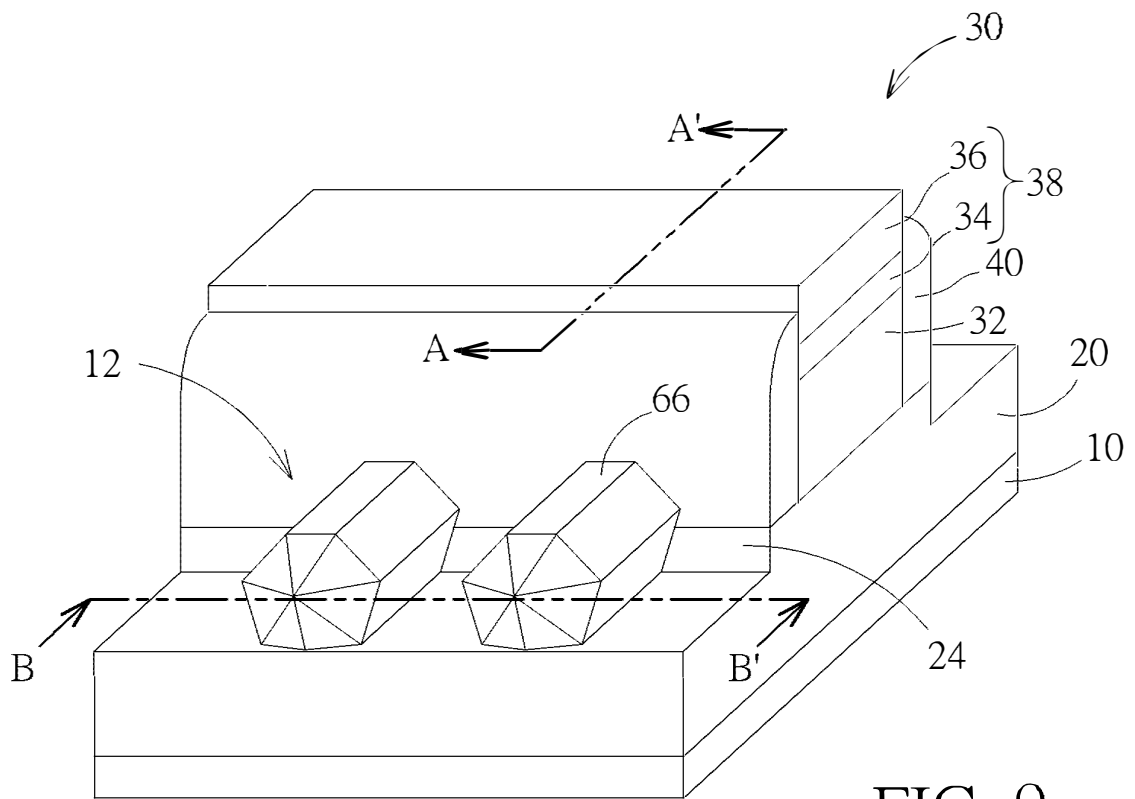


FIG. 9

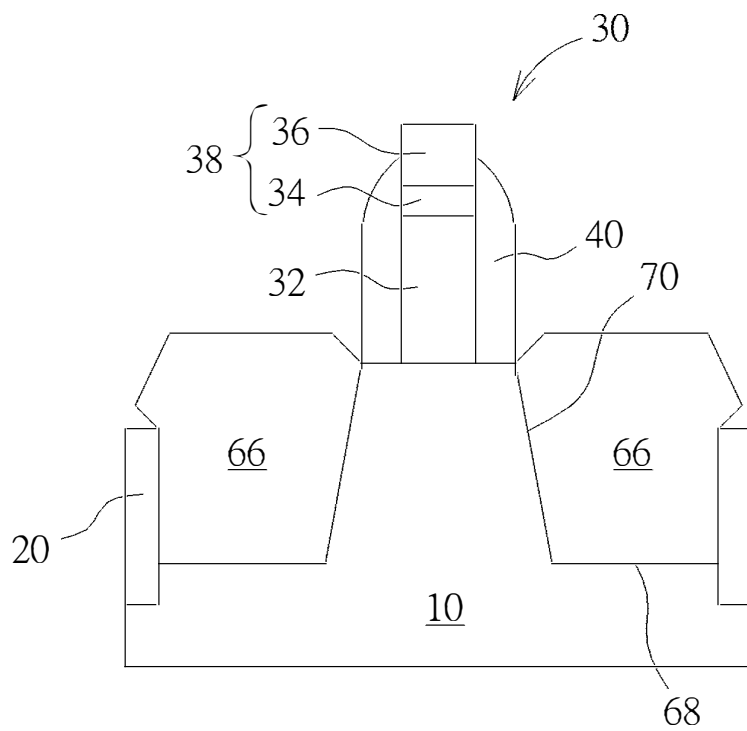


FIG. 10

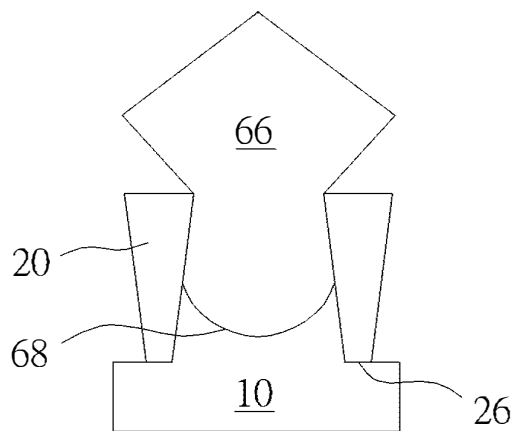


FIG. 11

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	Yu-Hsiang Hung
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	NAUP1656USA

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	7250658		2007-07-31	Doris; Bruce B.	all
	2	7091551		2006-08-15	Anderson; Brent A.	all
	3	7352034		2008-04-01	Booth, Jr.; Roger Allen	all
	4	6492216		2002-12-10	Yeo; Yee-Chia	all
	5	6921963		2005-07-26	Krivokapic; Zoran	all
	6	7087477		2006-08-08	Fried; David M.	all
	7	7247887		2007-07-24	King; Tsu-Jae	all
	8	7309626		2007-12-18	leong; Mei-Kei	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA

	9	7470570		2008-12-30	Beintner; Jochen	all
	10	7531437		2009-05-12	Brask; Justin K.	all
	11	6043138		2000-03-28	Ibok; Effiong E.	all
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	13	7525160		2009-04-28	Kavalieros	

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	2	20090242964		2009-10-01	Akil; Nader;	all
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	4	20100144121		2010-06-10	Chang; Cheng-Hung;	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA

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	6	20050051825		2005-03-10	Fujiwara, Makoto;	all
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	8	20070108528		2007-05-17	Anderson; Brent A.;	all
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	13	20100072553		2010-03-25	XU; Jeff J.;	all
	14	20100167506		2010-07-01	LIN; Simon Su-Horng;	all
	15	20120193713		2012-08-02	Kulkarni	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA

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FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
	1							
NON-PATENT LITERATURE DOCUMENTS								
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.						
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott Margo/	Date (YYYY-MM-DD)	2013-06-05
Name/Print	Scott Margo	Registration Number	56277

Abstract of Disclosure

A semiconductor device includes a fin structure, an isolation structure, a gate structure and an epitaxial structure. The fin structure protrudes from the surface of the substrate and includes a top surface and two sidewalls. The isolation structure surrounds the fin structure. The gate structure overlays the top surface and the two sidewalls of a portion of the fin structure, and covers a portion of the isolation structure. The isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, wherein the first top surface is higher than the second top surface. The epitaxial layer is disposed at one side of the gate structure and is in direct contact with the fin structure.

Claims

What is claimed is:

1. A semiconductor device, comprising:

- a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;
- an isolation structure, surrounding the fin structure;
- a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure, and covering a portion of the isolation structure, wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, and the first top surface is higher than the second top surface; and
- an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure.

2. The semiconductor device according to claim 1, wherein there is a height difference between the first top surface and second top surface, and the height difference ranges from 100 Angstroms to 250 Angstroms.

3. The semiconductor device according to claim 1, wherein the gate structure is a metal gate structure.

4. The semiconductor device according to claim 1, wherein the isolation structure under the gate structure comprises a sidewall and the epitaxial structure is in direct contact with the sidewall.

5. The semiconductor device according to claim 1, further comprising a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess.

6. The semiconductor device according to claim 5, wherein a bottom surface of the epitaxial structure is shallower than a bottom surface of the isolation structure.

7. The semiconductor device according to claim 6, wherein there is a height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure, and the height difference ranges from 100 Angstroms to 250 Angstroms.

8. The semiconductor device according to claim 1, wherein the epitaxial structure comprises

silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

9. The semiconductor device according to claim 1, further comprising a spacer disposed on a sidewall of the gate structure.
10. The semiconductor device according to claim 1, further comprising:
 - another epitaxial structure, disposed at another side of the gate structure and in direct contact with the fin structure; and
 - a channel region, contiguous to the top surface and the side surfaces of the fin structure, and between the epitaxial structure and said another epitaxial structure.
11. A fabrication method for a semiconductor device, comprising:
 - forming a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;
 - forming an isolation structure to surrounding the fin structure;
 - forming a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure, and covering a portion of the isolation structure;
 - etching the isolation structure exposed from the gate structure until a top surface of the isolation structure down to a first depth;
 - forming a recess in the fin structure at a side of the gate structure; and
 - forming an epitaxial layer to fill up the recess, wherein a bottom surface of the recess has a second depth, and the second depth is deeper than the first depth.
12. The fabrication method according to claim 11, wherein the isolation structure is a shallow trench isolation structure.
13. The fabrication method according to claim 11, wherein a step for etching the isolation structure comprises wet etching or dry etching.
14. The fabrication method according to claim 11, wherein the gate structure is a dummy gate structure.
15. The fabrication method according to claim 11, wherein a step for forming the recess comprises wet etching or dry etching.

16. The fabrication method according to claim 11, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.
17. The fabrication method according to claim 11, further comprising forming a spacer before etching the isolation structure, wherein the spacer is disposed on a sidewall of the gate structure.
18. The fabrication method according to claim 17, wherein a step for forming the spacer comprises:
depositing a material layer to conformally cover the gate structure and the fin structure, and etching the material layer until the isolation structure is exposed.
19. The fabrication method according to claim 11, further comprising:
depositing an interlayer dielectric to surround the gate structure;
removing the gate structure to leave a trench;
forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench;
and
forming a conductive layer to fill up the trench.

Title

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

Background of the Invention

1. Field of the Invention

[0001] The present invention generally relates to the field of semiconductor devices, and more particularly to a semiconductor device with an epitaxial structure and a fabrication method thereof.

2. Description of the Prior Art

[0002] As semiconductor devices switching speeds continue to increase and operating voltage levels continue to decrease, the performances of metal-oxide-semiconductor field effect transistors (MOSFETs) and other types of transistors, such as bipolar junction transistors, need to be correspondingly improved. Currently, along with the development of the MOSFETs, one of the main goals in the industry is to increase the carrier mobility so as to further increase the operation speed of the MOSFETs.

[0003] In order to improve the device performances, crystal strain technology has been developed. Crystal strain technology is becoming more and more attractive as a means for getting better performances in the field of MOS transistor fabrication. Putting a strain on a semiconductor crystal alters the speed at which charges move through that crystal. Strains make the MOS transistors work better by enabling charge carriers, such as electrons or holes, to pass through the silicon lattice of the channel more easily. Currently, attempts have been made to use a strained silicon layer as a part of MOS transistors in which an epitaxial silicon germanium (SiGe) structure or an epitaxial silicon carbide (SiC) structure is formed. In this type of MOS transistor, a biaxial tensile strain is induced in the epitaxy silicon layer due to the difference in lattice constants between SiGe or SiC and Si. As a result, the band structure is altered, and the carrier mobility is increased.

[0004] However, due to the continuous shrinkage in the size of the semiconductor devices, the aspect ratio of the epitaxial layer also gets higher, which often incur unwanted defects, such as void defects in the epitaxial layer. These defects inside the epitaxial layer reduce the stress required to be imposed onto the corresponding channel region. As a result, how to prevent the formation of the defects inside the epitaxial layer is an important issue.

Summary of the Invention

[0005] To this end, an object of the present invention is to provide a semiconductor device with an epitaxial layer so that stress imposed on the channel region can be increased.

[0006] According to a preferred embodiment of the invention, a semiconductor device is provided. The semiconductor device includes a fin structure, an isolation structure, a gate structure and an epitaxial structure. The fin structure protrudes from the surface of the substrate and includes a top surface and two sidewalls. The isolation structure surrounds the fin structure. The gate structure overlays the top surface and the two sidewalls of a portion of the fin structure, and covers a portion of the isolation structure. The isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, wherein the first top surface is higher than the second top surface. The epitaxial layer is disposed at one side of the gate structure and is in direct contact with the fin structure.

[0007] According to another preferred embodiment of the present invention, a fabrication method for a semiconductor device is provided. The method includes at least the following steps. First, a fin structure is formed. The fin structure protrudes from the surface of a substrate, wherein the fin structure includes a top surface and two side surfaces. Then, an isolation structure is formed around the fin structure. A gate structure is formed subsequently to overlay the top surface and the two side surfaces of a portion of the fin structure and to cover a portion of the isolation structure. The isolation structure exposed from the gate structure is etched until a top surface of the isolation structure is recessed down to a first depth. Afterwards, a recess is formed in the fin structure at a side of the gate structure. Finally, the recess is filled up with an epitaxial layer, wherein a bottom surface of the recess has a second depth, and the second depth is deeper than the first depth.

[0008] One feature of the present invention is to provide a semiconductor device with an epitaxial layer and a fabrication method thereof. Since the process for etching the isolation structure is optionally carried out prior to and/or after the formation of the recess, the height of the isolation structure at two sides of the gate structure may be reduced. In this way, the epitaxial layer may be filled into the corresponding recess easily during the epitaxial growth process. Furthermore, since the epitaxial structure is not sealed during the epitaxial growth process, the void defects may be also avoided as a result.

[0009] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0010] FIG. 1 to FIG. 11 are schematic diagrams showing a fabrication method of a semiconductor device according to a preferred embodiment of the present invention, wherein:

[0011] FIG. 1 is a schematic perspective diagram showing the semiconductor device at the beginning of the fabrication process;

[0012] FIG. 2 is a schematic perspective diagram showing the semiconductor device after the formation of a gate structure;

[0013] FIG. 3 is a schematic perspective diagram showing the semiconductor device after the formation of a spacer;

[0014] FIG. 4 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 3;

[0015] FIG. 5 is a schematic perspective diagram showing the semiconductor device after etching the isolation structure;

[0016] FIG. 6 is a schematic perspective diagram showing the semiconductor device after etching fin structures;

[0017] FIG. 7 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 6;

[0018] FIG. 8 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 6;

[0019] FIG. 9 is a schematic perspective diagram showing the semiconductor device after the formation of an epitaxial layer;

[0020] FIG. 10 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 9; and

[0021] FIG. 11 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 9.

Detailed Description

[0022] In the following description, numerous specific details are given to provide a thorough understanding of the invention. It will, however, be apparent to one skilled in the art that the invention may be practiced without these specific details. Furthermore, some well-known system configurations and process steps are not disclosed in detail, as these should be well-known to those skilled in the art.

[0023] Likewise, the drawings showing embodiments of the apparatus are not to scale and some dimensions are exaggerated for clarity of presentation. Also, where multiple embodiments

are disclosed and described as having some features in common, like or similar features will usually be described with same reference numerals for ease of illustration and description thereof.

[0024] FIG. 1 to FIG. 11 are schematic diagrams showing a fabrication method of a semiconductor device according to a preferred embodiment of the present invention. Please refer to FIG. 1. FIG. 1 is a schematic perspective view showing the semiconductor device of at the beginning of the fabrication process. As shown in FIG. 1, a substrate 10 is provided. The substrate 10 may be a semiconductor substrate such as a silicon substrate, a silicon containing substrate, a III-V semiconductor-on-silicon (such as GaAs-on-silicon) substrate, or a graphene-on-silicon substrate. Preferably, the substrate 10 is not a silicon-on-insulator (SOI) substrate. Still referring to FIG. 1, a plurality of fin structures 12 is disposed on the substrate 10. More precisely, the method for fabricating the fin structures 12 may include the following processes, but not limited thereto. First, a bulk substrate (not shown) is provided and a hard mask layer (not shown) is formed thereon. The hard mask layer is then patterned to define the location for forming fin structures 12 in the bulk substrate. Afterwards, an etching process is performed to form fin structures 12 in the bulk substrate. After the above processes, the fabrication method for the fin structures 12 is complete. In this case, the fin structures 12 may be regarded as protruding from the surface 10a of the substrate and the compositions of the fin structures 12 and the substrate 10 may be the same, such as epitaxial silicon. In another case, when the substrate is chosen from a III-V semiconductor-on-silicon substrate rather than the above-mentioned bulk substrate, the main compositions of the fin structures may differ from that of the underlying substrate.

[0025] In this embodiment, the hard mask layer (not shown) is optionally removed in a later process after the formation of the fin structures 12, so that a tri-gate MOSFET can be formed in the following processes. There are three contact faces between each fin structure 12 and the following formed dielectric layer serving as a carrier channel region. Compared with planar MOSFETs, the tri-gate MOSFETs have wider channel width within the same channel length. When a driving voltage is applied, the tri-gate MOSFET may produce an on-current twice higher than conventional planar MOSFETs. In another embodiment, the hard mask layer (not shown) is reserved to form a fin field effect transistor (Fin FET), which is another kind of multi-gate MOSFET. Since the hard mask layer is reserved in the fin field effect transistor, there are only two contact surfaces between each fin structure 12 and the following formed dielectric layer.

[0026] Please refer to FIG. 2. FIG. 2 is a schematic perspective diagram showing the semiconductor device after the formation of a dummy gate structure. An isolation structure 10 is formed on the substrate 10 between each fin structure 12 so as to electrically isolate subsequently-formed transistors from one another. The isolation structure 20 may have the configuration shown in FIG. 2. At this stage, a lower portion of each fin structure 12 is embedded in the isolation structure 20 and each fin structure 12 exposed out of the isolation structure 20 may have a first height H1. The isolation structure 10, for example, may be a shallow trench isolation (STI) structure, which may be formed through a STI fabrication process. Since the fabrication process for the STI structure is well-known to those skilled in the art, the detailed description of this is therefore omitted, and is not limited thereto.

[0027] Still referring to FIG. 2, in a following step, a gate dielectric layer (not shown), a sacrificial electrode layer (not shown) and a cap layer (not shown) are sequentially formed to cover the substrate 10 and the fin structures 12. Then, the gate dielectric layer, the sacrificial electrode layer and the cap layer are patterned to form a stack structure. The stack structure may be regarded as a gate structure 30 including the gate dielectric layer (not shown), the sacrificial electrode layer 32 and the cap layer 38. The gate structure 30 crosses over two fin structures 12 and covers the isolation structure 20 between them. Specifically, the gate structure 30 may cover a top surface 14 and two side surfaces 16 of portions of each fin structure 12, and may cover a top surface 22 of portions of the isolation structure 20. Additionally, the gate structure 30 is preferably aligned with a first direction X, while the fin structures 12 are preferably aligned with a second direction Y and protruding from the substrate 10 along a third direction X. In this embodiment, the first direction X, the second direction Y, and the third direction Z are mutually orthogonal to one another, but not limited thereto.

[0028] For the sake of clarity, only one gate structure 30 is depicted in FIG. 2 to FIG. 11. The number of which, however, may be increased depending on the requirements for different products. For example, more than one mutually parallel gate structure may be disposed on the substrate so that one fin structure may be concurrently covered by more than one gate structure. Besides, the same one gate structure 30 is preferably used as a gate for transistors with the same conductivity type, like gates for PMOS transistors or gates for NMOS transistors.

[0029] In this embodiment, a gate-last for high-k last process is used so that the gate structure 30 may be regarded as a dummy gate structure. In other words, the gate dielectric layer will be

replaced with a gate dielectric layer having a high dielectric constant in later processes and the sacrificial electrode layer 32 will be replaced with a conductive metal layer. Therefore, the material of the gate dielectric layer may be just a sacrificial material suitable for being removed in later processes. The sacrificial electrode layer 32 may be made of polysilicon, but it is not limited thereto. The cap layer 36 may be a single-layered or a multi-layered structure composed of a nitride layer or an oxide layer used to serve as a patterned hard mask. In this embodiment, the cap layer 36 is a double-layered structure composed of a bottom layer 34 and a top layer 34. The bottom layer 34 may be a nitride layer and the top layer 34 may be an oxide layer, but not limited thereto.

[0030] In the above paragraphs, a gate-last for high-k first process is used. However, the present embodiment may also adopt a gate-last for high-k last process. In this case, the gate dielectric layer is a gate dielectric layer having a high dielectric constant, which may be the group selected from hafnium oxide (HfO_2), hafnium silicate (HfSiO_4), hafnium silicon oxynitride (HfSiON), aluminum oxide (Al_2O_3), lanthanum oxide (La_2O_3), tantalum oxide (Ta_2O_5), yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), strontium titanate (SrTiO_3), zirconium silicate (ZrSiO_4), hafnium zirconate (HfZrO_4), strontium bismuth tantalate ($\text{SrBi}_2\text{Ta}_2\text{O}_9$, SBT), lead zirconate titanate ($\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$, PZT) and barium strontium titanate ($\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$, BST), but it is not limited thereto. Additionally, a barrier layer (not shown) may be formed on the gate dielectric layer to serve as an etching stop layer to protect the gate dielectric layer during the removal of the sacrificial electrode layer 32 and to prevent above disposed metals from diffusing downwards to the gate dielectric layer and from polluting the gate dielectric layer. The barrier layer (not shown) may be a single layer structure or a multilayer structure composed of tantalum nitride (TaN) or titanium nitride (TiN) etc.

[0031] Please refer to FIG. 3 and FIG. 4, wherein FIG. 4 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 3. After the formation of the gate structure, a spacer 40 is formed on the sidewalls of the gate structure 30 to define the position of an epitaxial structure. In this embodiment, the spacers 40 are respectively formed on each side of the gate structure 30 and cover portions of the top surface 22 of the isolation structure 20. More precisely, the method for forming the spacers 40 may includes the following steps. A material layer is deposited on the gate structure 30 and the substrate 10, and then an etching process is performed to form the spacers 40. The spacers 40 may be a single-layered structure, such as a silicon nitride layer or a silicon oxynitride layer, or a double-layered structure, such as a silicon oxide/silicon nitride layer, but not limited thereto. In this embodiment, the spacers 40 represent spacers for defining and

forming an epitaxial structure, so that other spacers may be formed before/after the spacers 40 are formed to form a lightly doped source/drain region (as shown) or a source/drain region (as shown). For simplifying and clarifying the present invention, FIG.3 to FIG. 11 only depict the spacers 40 for forming the epitaxial structure.

[0032] Please refer to FIG. 5. FIG. 5 is a schematic perspective view showing the semiconductor device after etching the isolation structure. After the formation of the spacers 40, the isolation structure 20 exposed from the gate structure 30 and the spacers 40 may be further etched by a suitable etching process. In this way, a top surface 22 of portions of the isolation structure 20 may be etched down to a predetermined depth (also called a first depth D1) and a structure shown in FIG. 5 is obtained. More precisely, a first etching process 42, such as a wet etching or a dry etching process, may be carried out to selectively remove the isolation structure 20 rather than the gate structure 30 and the fin structures 12. Through this process, not only portions of the sidewalls of the isolation structure 20 that are disposed under gate structure 30 and the spacers 40 may be exposed, but also portions of the fin structures 12 originally embedded in and in direct contact with the isolation structure 20 are exposed. At this time, the isolation structure 20 under the gate structure 30 and the spacers 40 may have a relatively high first top surface 22a, while the isolation structure 20 exposed from the gate structure 30 may have a relatively low second top surface 22b. There is a height difference H2 between the first top surface 22a and the second top surface 22b. For example, the height difference H2 may range from 100 Angstroms' to 250 Angstroms, preferably 150 Angstroms, but not limited thereto.

[0033] Please refer to FIG. 6 to FIG. 8. FIG. 6 is a schematic perspective view showing the semiconductor device after etching fin structures. FIG. 7 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 6. FIG. 8 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 6. As shown in FIG. 6 to FIG. 8, a second etching process 46 is carried out to etch the fin structures 12 under the gate structure 30 and the spacers 40. After the etching process, a recess 60 may be formed in each fin structure 12 at at least one side of the gate structure 30. Furthermore, according to this embodiment, the ends of the fin structures 12 at two sides of the gate structure 30 may respectively have a recess 60, and a bottom surface 68 of the recess 60 is preferably shallower than a bottom surface 26 of the isolation structure 20. More precisely, as shown in FIG. 7 and FIG. 8, there is a difference between the bottom surfaces 62 of the recesses 60 and the top surface 14 of the original fin structure 12, which height is equal to the first height H1 plus the second depth D2. During the second etching process 46, the top surface 22 of the isolation structure 20 at both sides of the gate structure 30 is also recessed down to a

predetermined depth. This diminished value is equal to a first depth D1. Preferably, the second depth D2 is greater (also called deeper) than the first depth D1.

[0034] Furthermore, the above etching process may include at least a dry etching step and/or at least a wet etching step. For example, the substrate 10 may be etched down to a predetermined depth through a dry etching step and then may be laterally etched to form a desired profile of the recess 60 through a wet etching step, but is not limited thereto. In this embodiment, the recess 60 has an upwardly-curved cross-sectional profile, but is not limited thereto, as the cross-sectional profile of the recess depends upon the specific requirements. Additionally, a wet cleaning process (not shown) may be performed optionally to clean the surface of the recess 60 after the etching. The wet cleaning process may include a dilute hydrofluoric acid (DHF) containing process, but it is not limited thereto.

[0035] It should be noted that, the timing for etching the isolation structure 20 exposed from the gate structure 30 and the spacers 40 and the timing for etching the fin structures 12 may be reversed. More precisely, according to the present embodiment, the fin structures 12 exposed from the gate structure 30 and the spacers 40 may be etched first and the isolation structure 20 not covered by the gate structure 30 and the spacers 40 are etched thereafter. In other words, one feature of the present invention is that, through etching the isolation structure 20, the height difference between the bottom surface 68 of each recess 60 and the top surfaces 22 of the isolation structure 20 at both sides of the gate structure 30 can be reduced. Therefore, the removal of the isolation structure 20 and the formation of the recess 60 may be carried out in either sequence and both can meet the needs of the present invention.

[0036] Please refer to FIG. 9 to FIG. 11. FIG. 9 is a schematic perspective view showing the semiconductor device after the formation of an epitaxial layer. FIG. 10 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 9. FIG. 11 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 9. As shown in FIG. 9 to FIG. 11, an epitaxial growth process, such as a molecular beam epitaxy (MBE) process, a co-flow epitaxial growth process, a cyclic selective epitaxial growth process or the likes, may be carried out in order to grow an epitaxial structure 60 in each corresponding recess 60. More precisely, each epitaxial structure 66 may completely cover the bottom surface 68 and sidewalls 70 of the corresponding recess 60. Furthermore, the composition of the epitaxial structure 66 may be correspondingly modified according to the conductivity types of the semiconductor devices. In this way, a certain stress may be imposed on the channel regions adjacent to the top surface 14 and the two sides of the fin

structure 12. For example, in a P-type semiconductor device, the epitaxial structure 66 may be doped or un-doped silicon germanium layer so as to apply a compressive stress to the channel regions. Besides, the epitaxial structure 66 may include a multilayer or a surrounded structure with a different germanium concentration gradually varying from the inside to the outside or/and from bottom to top. For example, the epitaxial layer 66 may include epitaxial Si, at least a layer of epitaxial SiGe with a relatively low concentration of Ge, at least a layer of epitaxial SiGe with a relatively high concentration of Ge, an epitaxial Si layer and so forth, which are disposed sequentially from bottom to up. In another case, in an N-type semiconductor device, the composition of the epitaxial structure 66 may include silicon phosphorous (SiP), silicon carbide (SiC), phosphorus-doped silicon carbide or the likes, so as to provide a tensile stress to the channel regions.

[0037] Furthermore, regardless of the composition of the epitaxial structure 66, since the height difference between the bottom surface 68 of each recess 60 and the top surface 22b of the isolation structure 20 at two sides of the gate structure 30 has been reduced in the above processes, the epitaxial structure 66 may not be sealed during the following epitaxial growth process and the void defects may be avoided as a result. In other words, one feature of the present invention is that, through etching the isolation structure 20 at two sides of the gate structure 30, the epitaxial structure 66 may be formed with a desired height (also called depth) and without any void defects. Accordingly, the epitaxial structure may apply the required stress to the channel regions thereby increasing the carrier mobility of the semiconductor device.

[0038] After the formation of the above epitaxial structures, the following semiconductor processes may be optionally carried out. For example, a high-k last replacement metal gate (RMG) process may be carried out so that the gate structure composed of polysilicon inside may be replaced with a metal gate structure. The RMG process may include the following processes: (1) depositing an interlayer dielectric to surround the gate structure; (2) removing the gate structure to leave a trench; (3) forming a gate dielectric layer to conformally cover the sidewalls and bottom of the trench; and (4) forming a conductive layer to fill up the trench. Afterwards, a contact formation process may be carried out to form a contact electrically connecting the epitaxial structure. Since the RMG process and the contact formation process are well-known to those skilled in the art, the detailed description of these is therefore omitted for the sake of clarity.

[0039] In the following paragraph, a modified embodiment of the above embodiment is

disclosed and the description below is mainly focused on differences among each embodiment. In addition, like or similar features will usually be described with same reference numerals for ease of illustration and description thereof.

[0040] Please refer to FIG. 3 and FIG. 5. According to this modified embodiment, after the formation of the spacers, the first etching process is also carried out to expose not only portions of the sidewalls of the isolation structure 20 disposed under the gate structure 30 and the spacers 40, but also to expose portions of the fin structures 12 originally embedded in and in direct contact with the isolation structure 20. Afterwards, with a slight difference from the process described in the above embodiment, the second etching process is not carried out in this modified embodiment so that no recess is formed in the fin structures. Finally, similarly to the structure shown in FIG. 9, the epitaxial growth process is carried out to form the epitaxial structure 66 on the surface of the fin structure. The following processes are all similar to those described in the previous embodiment, the detailed description of which is therefore omitted for the sake of clarity. In this modified embodiment, since portions of the isolation structure 20 are removed, the epitaxial structure 66 may effectively apply stress to the corresponding channel regions.

[0041] It should be noted that, for the sake of clarity, only the non-planar FETs are described in the above paragraphs. However, planar FETs may also be formed without departing from the scope and spirit of the present invention. More precisely, in this case, the gate structure may be formed to cover a planar active region and portions of the isolation structures. Then, the active region and the isolation structure at two sides of the gate structure are etched sequentially. Finally, an epitaxial growth process is carried out. Similarly, through etching the isolation structure at two sides of the gate structure, the epitaxial structure may be formed with a desired height (also called depth) without void defects. Accordingly, the epitaxial structure may apply the required stress to the channel regions thereby increasing the carrier mobility of the semiconductor device.

[0042] To summarize, the present invention provides a semiconductor device and a fabrication method thereof. By performing the process for etching the isolation structure and associated with an optional recess, the difference in height between the bottom surface of the recess and the top surface of the isolation structure at two sides of the gate structure may be reduced. In this way, the epitaxial structure may not be sealed during the following epitaxial growth process and the void defects may be avoided. Accordingly, the epitaxial structure may apply a required stress to the channel regions and increase the carrier mobility of the semiconductor device.

[0043] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1656USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Yu-Hsiang		Hung		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
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Inventor 3					Remove
Legal Name					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1656USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF		

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Legal Name				

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	Cheng-Guo		Chen	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
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Postal Code		Country i	TW	
Inventor 5				Remove
Legal Name				

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Postal Code		Country i	TW	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1656USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF		

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

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Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence Information of this application.

Customer Number	27765		
Email Address	scottmargo@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF		
Attorney Docket Number	NAUP1656USA	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	27765		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status		TSMC Exhibit 1002
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1656USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)
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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1656USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF		

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1			Remove
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
Clear			
☒ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor :			
If the Applicant is an Organization check here. ☒			
Organization Name	UNITED MICROELECTRONICS CORP.		
Mailing Address Information:			
Address 1	No.3, Li-Hsin Road 2,		
Address 2	Science-Based Industrial Park		
City	Hsin-Chu City	State/Province	
Country ⁱ	TW	Postal Code	
Phone Number		Fax Number	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1656USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF		
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.				
Assignee 1				
Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).				
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Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications				
Signature	/Scott Margo/		Date (YYYY-MM-DD)	2013-06-05
First Name	Scott	Last Name	Margo	Registration Number
				56277
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1656USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT**

Title of Invention:

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

As the below named inventor, I hereby declare that:
This declaration is directed to:

☒ The attached application, or

☐ United States application number _____ filed on _____, or

☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of _____

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the purposes thereof.

IN WITNESS WHEREOF, I have hereunto set hand and seal this MAY 02 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1656USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Yu-Hsiang Hung**

Date: 2013.05.02

Signature: Yu-Hsiang Hung

NPO#NAU-P1656-USA:0
CUST#UMCD-2012-0534

Page 2 of 10

F#NPO-P0002E-US1201
DSC0-102U003310

TSMC Exhibit 1002

Page 36 of 131

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT**

Title of Invention:

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

As the below named inventor, I hereby declare that:
This declaration is directed to:

☒ The attached application, or

☐ United States application number _____ filed on _____, or

☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of _____

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(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.

IN WITNESS WHEREOF, I have hereunto set hand and seal this JUN 03 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1656USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Ssu-I Fu**

Date: **JUN 03 2013**

Signature: Ssu-I Fu

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CUST#UMCD-2012-0534

Page 4 of 10

F#NPO-P0002E-US1201
DSC0-102U003310

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT**

Title of Invention:

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

As the below named inventor, I hereby declare that:
This declaration is directed to:

☒ The attached application, or

☐ United States application number _____ filed on _____, or

☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS** having a postal address of **CORP.**

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.

IN WITNESS WHEREOF, I have hereunto set hand and seal this JUN 03 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1656USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chung-Fu Chang**

Date: **JUN 03 2013**

Signature:

Chung-fu chang

NPO#NAU-P1656-USA:0
CUST#UMCD-2012-0534

Page 6 of 10

F#NPO-P0002E-US1201
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Docket No NAUP1656USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Cheng-Guo Chen**

Date: **JUN 03 2013**

Signature: Cheng-Guo Chen

NPO#NAU-P1656-USA:0
CUST#UMCD-2012-0534

Page 8 of 10

F#NPO-P0002E-US1201
DSC0-102U003310

— TSMC Exhibit 1002

Page 42 of 131

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Docket No NAUP1656USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chien-Ting Lin**

Date: **JUN 03 2013**

Signature:

Chien-Ting Lin

NPO#NAU-P1656-USA:0
CUST#UMCD-2012-0534

Page 10 of 10

F#NPO-P0002E-US1201
DSC0-102U003310

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒ Practitioners associated with Customer Number: 27765

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒ The address associated with Customer Number: 27765

OR

☐	Firm or Individual Name		
	Address		
	City		
	Country		
	Telephone		Email

Assignee Name and Address:

UNITED MICROELECTRONICS CORP.
No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	SEP 26 2012
Name	Chia-Tsung Hung	Telephone	+886-3-5782258
Title	CHAIRMAN		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: UNITED MICROELECTRONICS CORP.

Application No./Patent No.: _____ Filed/Issue Date: _____

Titled: SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOFUNITED MICROELECTRONICS CORP., a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Scott Margo/

Signature

Scott Margo

Printed or Typed Name

06/05/2013

Date

56277

Title or Registration Number

[Page 2 of 2]

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT**

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SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

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IN WITNESS WHEREOF, I have hereunto set hand and seal this MAY 02 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1656USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: Yu-Hsiang Hung

Date: 2013.05.02

Signature: Yu-Hsiang Hung

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
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Docket No NAUP1656USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Ssu-I Fu**

Date: **JUN 03 2013**

Signature: Ssu-I Fu

NPO#NAU-P1656-USA:0
CUST#UMCD-2012-0534

Page 4 of 10

F#NPO-P0002E-US1201
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Signature: _____

Chung-fu Chang

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Date:

JUN 03 2013

Signature:

Cheng-Guo Chen

NPO#NAU-P1656-USA:0
CUST#UMCD-2012-0534

Page 8 of 10

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~~TSMC Exhibit 1002~~

Page 55 of 131

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Inventor: **Chien-Ting Lin**

Date: **JUN 03 2013**

Signature: Chien-Ting Lin

NPO#NAU-P1656-USA:0
CUST#UMCD-2012-0534

Page 10 of 10

F#NPO-P0002E-US1201
DSC0-102U003310

Electronic Patent Application Fee Transmittal

Application Number:				
Filing Date:				
Title of Invention:	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF			
First Named Inventor/Applicant Name:	Yu-Hsiang Hung			
Filer:	Winston Hsu/Sandra Yen			
Attorney Docket Number:	NAUP1656USA			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt

EFS ID:	15962975
Application Number:	13913511
International Application Number:	
Confirmation Number:	9100
Title of Invention:	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF
First Named Inventor/Applicant Name:	Yu-Hsiang Hung
Customer Number:	27765
Filer:	Winston Hsu/Kate Yeh
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1656USA
Receipt Date:	09-JUN-2013
Filing Date:	
Time Stamp:	23:40:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	8431
Deposit Account	503105
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

TSMC Exhibit 1002

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Authorization to access Appl. by Trilateral Office	1663920.PDF	37498	no	1
			8b2f50629c4b650895ffa807e948219eb7cb8a		
Warnings:					
Information:					
2	Drawings-only black and white line drawings	1663768.PDF	85202	no	6
			1a644bd5c33778770a1e819e42e49a2f661b1f		
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	1663867.PDF	36589	no	5
			6fa7f1271a3a800718b58b5fe48fb4f438c3a6		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
4	Abstract	1663767.PDF	34438	no	1
			ec513fbfb3a38f7cffeef7c0eb4b859b3e55f8		
Warnings:					
Information:					
5	Claims	1663766.PDF	41410	no	3
			ee9d2858e931176f1135f750a9dce5d8082d6a9b		
Warnings:					
Information:					
6	Specification	1663765.PDF	120209	no	11
			08b1a6073febb25d39289f22034e64cd3c34ec3		
Warnings:					
Information:					
7	Application Data Sheet	1663985.PDF	1619677	no	8
			9df8d41978b7ff9af080e25514c98d5d2b6af9		
Warnings:					
Information:					

8	Oath or Declaration filed	1663845.PDF	337157	no	10
			6ab79c421f071372dca8d9d095b7f8f3e35a276a		
Warnings:					
Information:					
9	Power of Attorney	1663844.pdf	2364860	no	13
			01844a65f728b1111df8e42b2ea96747761b41cc		
Warnings:					
Information:					
10	Fee Worksheet (SB06)	fee-info.pdf	33056	no	2
			5ee08b28943a858d8fcb37110220c1ae5295980f		
Warnings:					
Information:					
Total Files Size (in bytes):			4710096		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/913,511				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720			
TOTAL CLAIMS (37 CFR 1.16(j))	19	minus 20 = *			OR	x 80 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *				x 420 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))						0.00				
			TOTAL			TOTAL	1600			
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/913,511	06/09/2013	2812	1600	NAUP1656USA	19	2

CONFIRMATION NO. 9100

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

FILING RECEIPT



Date Mailed: 07/09/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Yu-Hsiang Hung, Tainan City, TAIWAN;
Ssu-I Fu, Kaohsiung City, TAIWAN;
Chung-Fu Chang, Tainan City, TAIWAN;
Cheng-Guo Chen, Changhua County, TAIWAN;
Chien-Ting Lin, Hsinchu City, TAIWAN;

Applicant(s)

United Microelectronics Corp., Hsin-chu City, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 07/01/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/913,511**

Projected Publication Date: 12/11/2014

Non-Publication Request: No

Early Publication Request: No
Title

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/913,511	06/09/2013	Yu-Hsiang Hung	NAUP1656USA

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

CONFIRMATION NO. 9100
POA ACCEPTANCE LETTER



Date Mailed: 07/09/2013

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/09/2013.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/qtran/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/913,511	06/09/2013	Yu-Hsiang Hung	NAUP1656USA	9100

27765 7500 05/15/2014
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
05/15/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Office Action Summary	Application No. 13/913,511	Applicant(s) HUNG ET AL.	
	Examiner IDA M. SOWARD	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06/09/2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-19 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☐ Claim(s) ____ is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☒ Claim(s) 1-19 are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☐ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____. | 4) ☐ Other: ____. |

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-10, drawn to a semiconductor device, classified in 257/401.
- II. Claims 11-19, drawn to a fabrication method for a semiconductor device, classified in 438/197.

The inventions are distinct, each from the other because of the following reasons: Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). Patentability of the Group I invention would not necessarily imply patentability of the Group II invention, since the device of the Group I invention could be made by a process materially different from those/that of the Group II invention. In the instant case, the fin structure could have been formed subsequent to forming the isolation structure to obtain the same result.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not

Art Unit: 2822

required because one or more of the following reasons apply: the inventions have acquired a separate status in the art in view of their different classification and would require a different knowledge base and a different thought processes for a search.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of an invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition less than 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be corrected in compliance with 37 CFR 1.48(a) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. A request to correct inventorship under 37 CFR 1.48(a) must be accompanied by an application data sheet in accordance with 37 CFR 1.76 that identifies each inventor by his or her legal name and by the processing fee required under 37 CFR 1.17(i).

The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an

Art Unit: 2822

allowable product/apparatus claim will not be rejoined. See MPEP § 821.04.

Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDA M. SOWARD whose telephone number is (571)272-1845. The examiner can normally be reached on Monday - Thursday 6:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2822

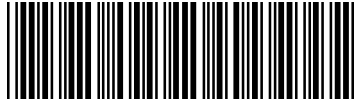
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IMS

May 8, 2014

/IDA M SOWARD/

Primary Examiner, Art Unit 2822

<i>Index of Claims</i> 	Application/Control No. 13913511	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner IDA M SOWARD	Art Unit 2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	05/08/2014							
	1	÷							
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	19	÷							

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

Appl. No. : 13/913,511 Confirmation No. 9100
First Named Inventor : Yu-Hsiang Hung
Filed : June 9, 2013
TC/A.U. : 2822
Examiner : Soward, Ida M
Docket No. : NAUP1656USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

5 In response to the Office action of May 15, 2014, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

- 5 1 (withdrawn): A semiconductor device, comprising:
 a fin structure, protruding from a surface of a substrate, wherein the fin structure
 comprises a top surface and two side surfaces;
 an isolation structure, surrounding the fin structure;
 a gate structure, overlaying the top surface and the two side surfaces of a portion of
10 the fin structure, and covering a portion of the isolation structure, wherein the
 isolation structure under the gate structure has a first top surface and the
 isolation structure at two sides of the gate structure has a second top surface,
 and the first top surface is higher than the second top surface; and
 an epitaxial layer, disposed at one side of the gate structure and in direct contact
15 with the fin structure.
- 20 2 (withdrawn): The semiconductor device according to claim 1, wherein there is a
height difference between the first top surface and second top surface, and the height
difference ranges from 100 Angstroms to 250 Angstroms.
- 25 3 (withdrawn): The semiconductor device according to claim 1, wherein the gate
structure is a metal gate structure.
- 30 4 (withdrawn): The semiconductor device according to claim 1, wherein the isolation
structure under the gate structure comprises a sidewall and the epitaxial structure is in
direct contact with the sidewall.
- 5 (withdrawn): The semiconductor device according to claim 1, further comprising a
recess formed at one end of the fin structure, wherein the epitaxial structure fills up
the recess.

6 (withdrawn): The semiconductor device according to claim 5, wherein a bottom surface of the epitaxial structure is shallower than a bottom surface of the isolation structure.

5

7 (withdrawn): The semiconductor device according to claim 6, wherein there is a height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure, and the height difference ranges from 100 Angstroms to 250 Angstroms.

10

8 (withdrawn): The semiconductor device according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

15 9 (withdrawn): The semiconductor device according to claim 1, further comprising a spacer disposed on a sidewall of the gate structure.

10 (withdrawn): The semiconductor device according to claim 1, further comprising:
another epitaxial structure, disposed at another side of the gate structure and in
20 direct contact with the fin structure; and
a channel region, contiguous to the top surface and the side surfaces of the fin structure, and between the epitaxial structure and said another epitaxial structure.

25 11 (original): A fabrication method for a semiconductor device, comprising:
forming a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;
forming an isolation structure to surrounding the fin structure;
forming a gate structure, overlaying the top surface and the two side surfaces of a
30 portion of the fin structure, and covering a portion of the isolation structure;

etching the isolation structure exposed from the gate structure until a top surface
of the isolation structure down to a first depth;
forming a recess in the fin structure at a side of the gate structure; and
forming an epitaxial layer to fill up the recess, wherein a bottom surface of the
5 recess has a second depth, and the second depth is deeper than the first depth.

12 (original): The fabrication method according to claim 11, wherein the isolation
structure is a shallow trench isolation structure.

10 13 (original): The fabrication method according to claim 11, wherein a step for etching
the isolation structure comprises wet etching or dry etching.

14 (original): The fabrication method according to claim 11, wherein the gate structure
is a dummy gate structure.

15 15 (original): The fabrication method according to claim 11, wherein a step for
forming the recess comprises wet etching or dry etching.

16 (original): The fabrication method according to claim 11, wherein the epitaxial
20 structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon
carbide.

17 (original): The fabrication method according to claim 11, further comprising
forming a spacer before etching the isolation structure, wherein the spacer is
25 disposed on a sidewall of the gate structure.

18 (original): The fabrication method according to claim 17, wherein a step for
forming the spacer comprises:
depositing a material layer to conformally cover the gate structure and the fin
30 structure, and

etching the material layer until the isolation structure is exposed.

19 (original): The fabrication method according to claim 11, further comprising:

- depositing an interlayer dielectric to surround the gate structure;
- 5 removing the gate structure to leave a trench;
- forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench; and
- forming a conductive layer to fill up the trench.

Electronic Acknowledgement Receipt

EFS ID:	19280979
Application Number:	13913511
International Application Number:	
Confirmation Number:	9100
Title of Invention:	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF
First Named Inventor/Applicant Name:	Yu-Hsiang Hung
Customer Number:	27765
Filer:	Winston Hsu/Connie Chen
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1656USA
Receipt Date:	12-JUN-2014
Filing Date:	09-JUN-2013
Time Stamp:	05:12:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	1976826.PDF	583395 9535710d9dcb9b789a35d8cf540ec34778faabca	no	2

Warnings:

Information:

TSMC Exhibit 1002

Page 81 of 131

2	Response to Election / Restriction Filed	1976825.PDF	76082 7c29c0c87656eeaca521fa597e#8eb26bb786cb6	no	1
Warnings:					
Information:					
3	Claims	1976824.PDF	81705 a78fe831efcc279e4607af7108ba4cae64699e03	no	4
Warnings:					
Information:					
Total Files Size (in bytes):			741182		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record
5 in the application file.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-10, drawn to a semiconductor device, classified in 257/401.
10 II. Claims 11-19, drawn to a fabrication method for a semiconductor device,
classified in 438/197.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process
15 as claimed can be used to make another and materially different product or (2) that
the product as claimed can be made by another and materially different
process (MPEP § 806.05(f)). Patentability of the Group I invention
would not necessarily imply patentability of the Group II invention,
since the device of the Group I invention could be made by a process
20 materially different from those/that of the Group II invention. In the
instant case, the fin structure could have been formed subsequent to
forming the isolation structure to obtain the same result.

Response

Applicant hereby elects Group II invention in response to the above restriction
25 requirements. The claims readable upon the Group II invention are claims 11–19.
Claims 1-10 are withdrawn without prejudice or disclaimer to the merits
thereof as the applicant still reserves the right of filing divisional
application(s) for prosecution of the non-elected inventions. No new
claims are added in this reply.

30 Applicant respectfully requests that a timely Notice of Allowance be issued in this

case.

Sincerely yours,

5 /Scott Margo/ Date: 06/11/2014

Scott Margo, Patent Agent No. 56,277

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

10 e-mail : ScottMargo@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in
D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

15

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/913,511	Filing Date 06/09/2013	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	06/12/2014	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/SHARON HARRIS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/913,511	06/09/2013	Yu-Hsiang Hung	NAUP1656USA	9100
27765 7500 08/28/2014 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER PICARDAT, KEVIN M	
			ART UNIT 2822	PAPER NUMBER
			NOTIFICATION DATE 08/28/2014	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Office Action Summary	Application No. 13/913,511	Applicant(s) HUNG ET AL.	
	Examiner KEVIN M. PICARDAT	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 June 2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-19 is/are pending in the application.
5a) Of the above claim(s) 1-10 is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☒ Claim(s) 11-19 is/are rejected.
- 8) ☐ Claim(s) _____ is/are objected to.
- 9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 09 June 2013 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 6-9-13
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 4) ☐ Other: _____

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

Applicant's election without traverse of Group II, claims 11-19 in the reply filed on 12 June 2014 is acknowledged.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

Claims 11-13, and 15-18 are rejected under 35 U.S.C. 102(a)(2) as being anticipated by Kavalieros et al. US 7,525,160.

Kavalieros et al. discloses a method of making a semiconductor device including forming a fin structure (118) protruding from a substrate (102) having a top and two sides, forming a STI to surround the fin, forming a gate structure (106) over the top and two sides of the fin and covering a portion of the STI, etching the STI exposed from the

Art Unit: 2822

gate structure to a first depth (see fig. 10), forming a recess (126) in the fin structure at a side of the gate structure and forming an epitaxial layer to fill up the recess, where in the recess has a second depth deeper than the first depth, also disclosed is using known etching methods, the epitaxial layer can be SiGe (col. 9, lines 15-20), and forming sidewall spacers (110) on the gate structure prior to etching (see figs. 5-12 and related text).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 14 and 19 are rejected under 35 U.S.C. 103 as being unpatentable over Kavalieros et al. as applied to claim 11 above, and further in view of Hsieh et al. US 8,765,533.

Kavalieros et al. discloses as stated above, however it does not disclose using a dummy gate.

Hsieh et al. discloses using a dummy gate in forming a fin device including removing the dummy gate after the epitaxial source/drain are forming and replacing with the real gate (see figs. 10A-13B and related text).

Therefore it would have been obvious to one of ordinary skill in the art to modify Kavalieros et al. as taught by Hsieh et al., because it would eliminate the possibility of damage to the gate during the earlier processing steps.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. PICARDAT whose telephone number is (571)272-1841. The examiner can normally be reached on Monday-Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KEVIN M. PICARDAT/
Primary Examiner, Art Unit 2822

Notice of References Cited	Application/Control No. 13/913,511	Applicant(s)/Patent Under Reexamination HUNG ET AL.	
	Examiner KEVIN M. PICARDAT	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,765,533	07-2014	Hsieh et al.	438/151
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

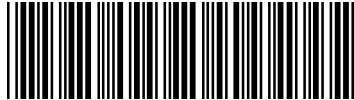
FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 13913511	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner IDA M SOWARD	Art Unit 2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	05/08/2014	08/21/2014						
	1	÷	N						
	2	÷	N						
	3	÷	N						
	4	÷	N						
	5	÷	N						
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	11	÷	✓						
	12	÷	✓						
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	19	÷	✓						



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BIB DATA SHEET

CONFIRMATION NO. 9100

SERIAL NUMBER 13/913,511	FILING or 371(c) DATE 06/09/2013 RULE	CLASS 257	GROUP ART UNIT 2822	ATTORNEY DOCKET NO. NAUP1656USA
APPLICANTS United Microelectronics Corp., Hsin-chu City, TAIWAN, Assignee (with 37 CFR 1.172 Interest); INVENTORS Yu-Hsiang Hung, Tainan City, TAIWAN; Ssu-I Fu, Kaohsiung City, TAIWAN; Chung-Fu Chang, Tainan City, TAIWAN; Cheng-Guo Chen, Changhua County, TAIWAN; Chien-Ting Lin, Hsinchu City, TAIWAN;				
** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/01/2013				
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/KEVIN M PICARDAT/</u> Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 6	TOTAL CLAIMS 19
INDEPENDENT CLAIMS 2				
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES				
TITLE SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF				
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit	

Search Notes 	Application/Control No. 13913511	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner KEVIN M PICARDAT	Art Unit 2822

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
438	149, 151, 229, 230, 294, 297, 299, 300	8-19-14	KMP

SEARCH NOTES		
Search Notes	Date	Examiner
EAST: listed subs	8-19-14	KMP
EAST: inventor name search	8-19-14	KMP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	7250658		2007-07-31	Doris; Bruce B.	all
	2	7091551		2006-08-15	Anderson; Brent A.	all
	3	7352034		2008-04-01	Booth, Jr.; Roger Allen	all
	4	6492216		2002-12-10	Yeo; Yee-Chia	all
	5	6921963		2005-07-26	Krivokapic; Zoran	all
	6	7087477		2006-08-08	Fried; David M.	all
	7	7247887		2007-07-24	King; Tsu-Jae	all
	8	7309626		2007-12-18	leong; Mei-Kei	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA

	9	7470570		2008-12-30	Beintner; Jochen	all
	10	7531437		2009-05-12	Brask; Justin K.	all
	11	6043138		2000-03-28	Ibok; Effiong E.	all
	12	7569857		2009-08-04	Simon, legal representative; David	all
	13	7525160		2009-04-28	Kavalieros	

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20060099830		2006-05-11	Walther; Steven R.;	all
	2	20090242964		2009-10-01	Akil; Nader;	all
	3	20100048027		2010-02-25	Cheng; Kangguo;	all
	4	20100144121		2010-06-10	Chang; Cheng-Hung;	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA

5	20040195624		2004-10-07	Liu, Chee-Wee;	all
6	20050051825		2005-03-10	Fujiwara, Makoto;	all
7	20060286729		2006-12-21	Kavalieros; Jack;	all
8	20070108528		2007-05-17	Anderson; Brent A.;	all
9	20070158756		2007-07-12	Dreeskornfeld; Lars;	all
10	20080157208		2008-07-03	Fischer; Kevin J.;	all
11	20090124097		2009-05-14	Cheng; Kangguo;	all
12	20090269916		2009-10-29	KANG; Inkuk;	all
13	20100072553		2010-03-25	XU; Jeff J.;	all
14	20100167506		2010-07-01	LIN; Simon Su-Horng;	all
15	20120193713		2012-08-02	Kulkarni	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
	1							

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

EXAMINER SIGNATURE			
Examiner Signature	/Kevin Picardat/	Date Considered	08/21/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott Margo/	Date (YYYY-MM-DD)	2013-06-05
Name/Print	Scott Margo	Registration Number	56277

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

Appl. No. : 13/913,511 Confirmation No. 9100
First Named Inventor : Yu-Hsiang Hung
Filed : June 9, 2013
TC/A.U. : 2822
Examiner : Picardat, Kevin M
Docket No. : NAUP1656USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

5 In response to the Office action of August 28, 2014, please amend the
above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2
of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 5 1 (withdrawn): A semiconductor device, comprising:
a fin structure, protruding from a surface of a substrate, wherein the fin structure
comprises a top surface and two side surfaces;
an isolation structure, surrounding the fin structure;
a gate structure, overlaying the top surface and the two side surfaces of a portion of
10 the fin structure, and covering a portion of the isolation structure, wherein the
isolation structure under the gate structure has a first top surface and the
isolation structure at two sides of the gate structure has a second top surface,
and the first top surface is higher than the second top surface; and
an epitaxial layer, disposed at one side of the gate structure and in direct contact
15 with the fin structure.
- 2 (withdrawn): The semiconductor device according to claim 1, wherein there is a
height difference between the first top surface and second top surface, and the height
difference ranges from 100 Angstroms to 250 Angstroms.
- 20 3 (withdrawn): The semiconductor device according to claim 1, wherein the gate
structure is a metal gate structure.
- 4 (withdrawn): The semiconductor device according to claim 1, wherein the isolation
25 structure under the gate structure comprises a sidewall and the epitaxial structure is in
direct contact with the sidewall.
- 5 (withdrawn): The semiconductor device according to claim 1, further comprising a
recess formed at one end of the fin structure, wherein the epitaxial structure fills up
30 the recess.

6 (withdrawn): The semiconductor device according to claim 5, wherein a bottom surface of the epitaxial structure is shallower than a bottom surface of the isolation structure.

5

7 (withdrawn): The semiconductor device according to claim 6, wherein there is a height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure, and the height difference ranges from 100 Angstroms to 250 Angstroms.

10

8 (withdrawn): The semiconductor device according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

15 9 (withdrawn): The semiconductor device according to claim 1, further comprising a spacer disposed on a sidewall of the gate structure.

10 (withdrawn): The semiconductor device according to claim 1, further comprising:
another epitaxial structure, disposed at another side of the gate structure and in
20 direct contact with the fin structure; and
a channel region, contiguous to the top surface and the side surfaces of the fin structure, and between the epitaxial structure and said another epitaxial structure.

25 11 (currently amended): A fabrication method for a semiconductor device, comprising:

forming a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;
forming an isolation structure to ~~surrounding~~ surround the fin structure;
30 forming a gate structure, overlaying the top surface and the two side surfaces of a

- portion of the fin structure, and covering a portion of the isolation structure;
after the step of forming the gate structure, etching the isolation structure exposed
from the gate structure until a top surface of the isolation structure is etched
down to a first depth;
- 5 forming a recess in the fin structure at a side of the gate structure; and
forming an epitaxial layer to fill up the recess, wherein a bottom surface of the
recess has a second depth, and the second depth is deeper than the first depth.
- 12 (original): The fabrication method according to claim 11, wherein the isolation
10 structure is a shallow trench isolation structure.
- 13 (original): The fabrication method according to claim 11, wherein a step for etching
the isolation structure comprises wet etching or dry etching.
- 15 14 (original): The fabrication method according to claim 11, wherein the gate structure
is a dummy gate structure.
- 15 (original): The fabrication method according to claim 11, wherein a step for
forming the recess comprises wet etching or dry etching.
- 20 16 (original): The fabrication method according to claim 11, wherein the epitaxial
structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon
carbide.
- 25 17 (original): The fabrication method according to claim 11, further comprising
forming a spacer before etching the isolation structure, wherein the spacer is disposed
on a sidewall of the gate structure.
- 18 (original): The fabrication method according to claim 17, wherein a step for
30 forming the spacer comprises:

depositing a material layer to conformally cover the gate structure and the fin structure, and
etching the material layer until the isolation structure is exposed.

- 5 19 (original): The fabrication method according to claim 11, further comprising:
depositing an interlayer dielectric to surround the gate structure;
removing the gate structure to leave a trench;
forming a gate dielectric layer to conformally cover a sidewall and a bottom of
the trench; and
10 forming a conductive layer to fill up the trench.

Electronic Acknowledgement Receipt

EFS ID:	20817543
Application Number:	13913511
International Application Number:	
Confirmation Number:	9100
Title of Invention:	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF
First Named Inventor/Applicant Name:	Yu-Hsiang Hung
Customer Number:	27765
Filer:	Winston Hsu/Eve Hsieh
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1656USA
Receipt Date:	28-NOV-2014
Filing Date:	09-JUN-2013
Time Stamp:	01:02:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	2117742.PDF	615548 56705b77d4c9875489e67d4f2cdeba21b5e8e c3607	no	4

Warnings:

Information:

TSMC Exhibit 1002

Page 105 of 131

2	Amendment/Req. Reconsideration-After Non-Final Reject	2117741.PDF	79669 5f12ef4930a46a956af8a272a77f9c4e26065b28	no	1
Warnings:					
Information:					
3	Claims	2117740.PDF	85446 ae9574fe4454524443b58175b77c5f260be7b04	no	4
Warnings:					
Information:					
Total Files Size (in bytes):				780663	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record
5 in the application file.

1. Claim Rejections – 35 U.S.C. 102

Claims 11-13 and 15-18 were rejected under 35 U.S.C. 102(a)(2) as being anticipated by Kavalieros et al. (US 7,525,160; hereinafter “Kavalieros”).

Response

Claim 11

Claim 11 has been amended to correct some wording errors and to introduce a feature disclosed in the specification of the original application. Specifically, a feature
15 “after the step of forming the gate structure, etching the isolation structure exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth” (emphasis added) as recited in amended claim 11 is disclosed at least in paragraph [0032] and shown in FIG. 5 of the original application. No new matter is introduced in this amendment and acceptance of the amendment is politely requested.

Applicant submits that the cited reference, Kavalieros, fails to teach or suggest
20 the above-mentioned feature. For example, as shown in FIG. 11 of Kavalieros, although Kavalieros discloses performing an etching process to form recesses (126) in a body (118, also-called fin) after the steps of forming a gate electrode (106) and spacers (110), Kavalieros fails to teach etching the top surface of a STI (116) exposed from the gate electrode (106) and the spacers (110) down to a first depth after the
25 steps of forming the gate electrode (106) and the spacers (110).

Additionally, in the outstanding Office action, the examiner states that
“Kavalieros discloses...etching the STI exposed from the gate structure to a first depth (see fig. 10)” (Office action: pages 2-3) and submits that this feature is already anticipated by Kavalieros. However, applicant respectfully disagrees with the Examiner’s opinion.
30 For example, as shown in FIG. 10 of Kavalieros, although there is a height difference

between the top surface of the STI (116) and that of the body (118), this height difference is actually produced by an etching process before, rather than after, the formation of the gate electrode (106) and the spacers (110). This point of view is clearly supported by a structure shown in FIG. 4 of Kavalieros as a height (152) between the top surface of the STI (116) and that of the body (118) is defined before the formation of the gate electrode (106) and the spacers (110).

Also, another cited reference, Hsieh, also fails to teach or suggest the above-mentioned feature.

Thus, for these reasons, even if a person having ordinary skill in the art refers to the cited references, he/she would not anticipate the feature “after the step of forming the gate structure, etching the isolation structure exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth” as recited in amended claim 11. Applicant submits that all the limitations in claim 11 are novel and unobvious over the prior art and claim 11 should be found allowable. Applicant therefore respectfully requests that Examiner withdraws the rejection of claim 11 under 35 U.S.C. §102(a)(2).

Claims 12, 13 and 15-18

Claims 12, 13 and 15-18 are dependent upon claim 11, and if claim 11 is allowable for the reasons explained above, claims 12, 13 and 15-18 should be also allowable. Applicant therefore respectfully requests that the Examiner withdraws the rejection of claims 12, 13 and 15-18 under 35 U.S.C. §102(a)(2).

2. Claim Rejections – 35 U.S.C. 103

Claims 14 and 19 were rejected under 35 U.S.C. 103 as being unpatentable over Kavalieros et al. as applied to claim 11 above, and further in view of Hsieh et al. (US 8,765,533; hereinafter “Hsieh”).

Response

Claims 14 and 19

Claims 14 and 19 are dependent upon claim 11, and if claim 11 is allowable for the reasons explained above, claims 14 and 19 should be also allowable. Applicant

therefore respectively requests that the Examiner withdraws the rejection of claims 14 and 19 under 35 U.S.C. §103.

3. Conclusion

5 In view of the forging, Applicant submits that the imposed rejections have been overcome, and that all pending claims are in condition for allowance. Favorable consideration is therefore solicited. In the event that Examiner finds remaining impediment to a prompt allowance of the application that may be clarified through a telephone interview or overcome by an Examiner's Amendment, the Examiner is
10 requested to contact the undersigned attorney.

 As Applicant's remarks with respect to the Examiner's rejections are sufficient to overcome these rejections, Applicant's silence as to assertions by the Examiner in the Office Action or certain requirements that may be applicable to such rejections (e.g., whether a reference constitutes prior art, ability to combine references,
15 assertions as to patentability of dependent claims) is not a concession by Applicant that such assertions are accurate or such requirements have been met, and Applicant reserves the right to analyze and dispute such assertions in the future.

 Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

20

Sincerely yours,

/Scott Margo/

Date: 11/27/2014

Scott Margo, Patent Agent No. 56,277

5 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : ScottMargo@naipo.com

- 10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/913,511	Filing Date 06/09/2013	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	11/28/2014	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DORRETTA BROOKS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/913,511	06/09/2013	Yu-Hsiang Hung	NAUP1656USA

CONFIRMATION NO. 9100

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

PUBLICATION NOTICE



Title: SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

Publication No. US-2014-0361373-A1

Publication Date: 12/11/2014

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7500 01/12/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

PICARDAT, KEVIN M

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 01/12/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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13/913,511

06/09/2013

Yu-Hsiang Hung

NAUP1656USA

9100

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	04/13/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

27765 7590 01/12/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/913,511	06/09/2013	Yu-Hsiang Hung	NAUP1656USA	9100

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	04/13/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
PICARDAT, KEVIN M	2822	438-151000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/913,511	06/09/2013	Yu-Hsiang Hung	NAUPI656USA	9100
27765 7500 01/12/2015 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER PICARDAT, KEVIN M	
			ART UNIT 2822	PAPER NUMBER
DATE MAILED: 01/12/2015				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/913,511	Applicant(s) HUNG ET AL.	
	Examiner KEVIN M. PICARDAT	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on 14 November 2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 11-19. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☒ Examiner's Amendment/Comment |
| 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/KEVIN M. PICARDAT/
Primary Examiner, Art Unit 2822

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Cancel claims 1-10.

This application is in condition for allowance except for the presence of claims 1-10 directed to the product non-elected without traverse. Accordingly, claims 1-10 have been cancelled.

The following is an examiner's statement of reasons for allowance: Examiner agrees with applicant's arguments, with regard to the amended claim, filed on 28 November 2014.

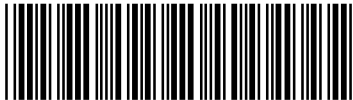
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. PICARDAT whose telephone number is (571)272-1841. The examiner can normally be reached on Monday-Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KEVIN M. PICARDAT/
Primary Examiner, Art Unit 2822

Issue Classification 	Application/Control No. 13913511	Applicant(s)/Patent Under Reexamination HUNG ET AL.	
	Examiner KEVIN M PICARDAT	Art Unit 2822	

CPC						
Symbol					Type	Version
H01L		29	/	7848	F	2013-01-01
H01L		29	/	6681	I	2013-01-01
H01L		29	/	7855	I	2013-01-01
H01L		21	/	8234	I	2013-01-01
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CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
		9	
(Assistant Examiner) /KEVIN M PICARDAT/ Primary Examiner.Art Unit 2822	(Date) 12/11/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9

Issue Classification 	Application/Control No. 13913511	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner KEVIN M PICARDAT	Art Unit 2822

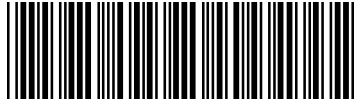
US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION										
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED					
438		151				H	0	1	L	21 / 00 (2006.01.01)						
CROSS REFERENCE(S)																
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)															
438	149	229														

NONE		Total Claims Allowed:	
		9	
(Assistant Examiner) /KEVIN M PICARDAT/ Primary Examiner.Art Unit 2822	(Date) 12/11/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9

Issue Classification 	Application/Control No. 13913511	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner KEVIN M PICARDAT	Art Unit 2822

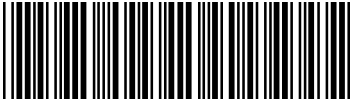
☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
-	1	7	17												
-	2	8	18												
-	3	9	19												
-	4														
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-	6														
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-	8														
-	9														
-	10														
1	11														
2	12														
3	13														
4	14														
5	15														
6	16														

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 9	
/KEVIN M PICARDAT/ Primary Examiner.Art Unit 2822 (Primary Examiner) _____ (Date) _____		O.G. Print Claim(s) 1	O.G. Print Figure 9

<i>Index of Claims</i> 	Application/Control No. 13913511	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner IDA M SOWARD	Art Unit 2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant					☐ CPA					☐ T.D.					☐ R.1.47				
CLAIM		DATE																	
Final	Original	05/08/2014	08/21/2014	12/11/2014															
	1	÷	N	-															
	2	÷	N	-															
	3	÷	N	-															
	4	÷	N	-															
	5	÷	N	-															
	6	÷	N	-															
	7	÷	N	-															
	8	÷	N	-															
	9	÷	N	-															
	10	÷	N	-															
1	11	÷	✓	=															
2	12	÷	✓	=															
3	13	÷	✓	=															
4	14	÷	✓	=															
5	15	÷	✓	=															
6	16	÷	✓	=															
7	17	÷	✓	=															
8	18	÷	✓	=															
9	19	÷	✓	=															

Search Notes 	Application/Control No. 13913511	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner KEVIN M PICARDAT	Art Unit 2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L/822, 8232 ,9234, 8258	12-9-14	KMP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
438	149, 151, 229, 230, 294, 297, 299, 300	8-19-14	KMP
Upated	above search	12-9-14	KMP

SEARCH NOTES		
Search Notes	Date	Examiner
EAST: listed subs	8-19-14	KMP
EAST: inventor name search	8-19-14	KMP
Update above	12-9-14	KMP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
AS	ABOVE	12-9-14	KMP

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BIB DATA SHEET

CONFIRMATION NO. 9100

SERIAL NUMBER 13/913,511	FILING or 371(c) DATE 06/09/2013 RULE	CLASS 257	GROUP ART UNIT 2822	ATTORNEY DOCKET NO. NAUP1656USA
APPLICANTS United Microelectronics Corp., Hsin-chu City, TAIWAN, Assignee (with 37 CFR 1.172 Interest); INVENTORS Yu-Hsiang Hung, Tainan City, TAIWAN; Ssu-I Fu, Kaohsiung City, TAIWAN; Chung-Fu Chang, Tainan City, TAIWAN; Cheng-Guo Chen, Changhua County, TAIWAN; Chien-Ting Lin, Hsinchu City, TAIWAN;				
** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/01/2013				
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/KEVIN M PICARDAT/</u> Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 6	TOTAL CLAIMS 19
INDEPENDENT CLAIMS 2				
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES				
TITLE SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF				
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit	

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 01/12/2015

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Shelley Kuo	(Depositor's name)
/Shelley Kuo/	(Signature)
02/25/2015	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/913,511	06/09/2013	Yu-Hsiang Hung	NAUP1656USA	9100

TITLE OF INVENTION:

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	No	\$960	\$0	\$0	\$960	04/13/2015
EXAMINER	ART UNIT	CLASS-SUBCLASS				
Picardat, Kevin M	2822	438-151000				

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Winston Hsu

2 Scott Margo

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

UNITED MICROELECTRONICS CORP.

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

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- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
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5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Authorized Signature /Winston Hsu/

Date 02/23/2015

Typed or printed name Wnston Hsu

Registration No. 41,526

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal

Application Number:	13913511			
Filing Date:	09-Jun-2013			
Title of Invention:	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF			
First Named Inventor/Applicant Name:	Yu-Hsiang Hung			
Filer:	Winston Hsu/Shelley Kuo			
Attorney Docket Number:	NAUP1656USA			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	21577901
Application Number:	13913511
International Application Number:	
Confirmation Number:	9100
Title of Invention:	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF
First Named Inventor/Applicant Name:	Yu-Hsiang Hung
Customer Number:	27765
Filer:	Winston Hsu/Shelley Kuo
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1656USA
Receipt Date:	25-FEB-2015
Filing Date:	09-JUN-2013
Time Stamp:	22:50:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$960
RAM confirmation Number	11374
Deposit Account	503105
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

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TSMC Exhibit 1002

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Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	NAUP1656USA0_AN_1_NP072.pdf	333523	no	1
			3fa5728ec5d5e77e56a3652ffe29f1283d47d9b0		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30438	no	2
			e8606f2e8ab697f2d4fc3a6e6a358292e1b2c0b41		

Warnings:

Information:

Total Files Size (in bytes):	363961
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/913,511	03/31/2015	8993384	NAUP1656USA	9100

27765 759 03/11/2015

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

United Microelectronics Corp., Hsin-chu City, TAIWAN, Assignee (with 37 CFR 1.172 Interest);
Yu-Hsiang Hung, Tainan City, TAIWAN;
Ssu-I Fu, Kaohsiung City, TAIWAN;
Chung-Fu Chang, Tainan City, TAIWAN;
Cheng-Guo Chen, Changhua County, TAIWAN;
Chien-Ting Lin, Hsinchu City, TAIWAN;

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