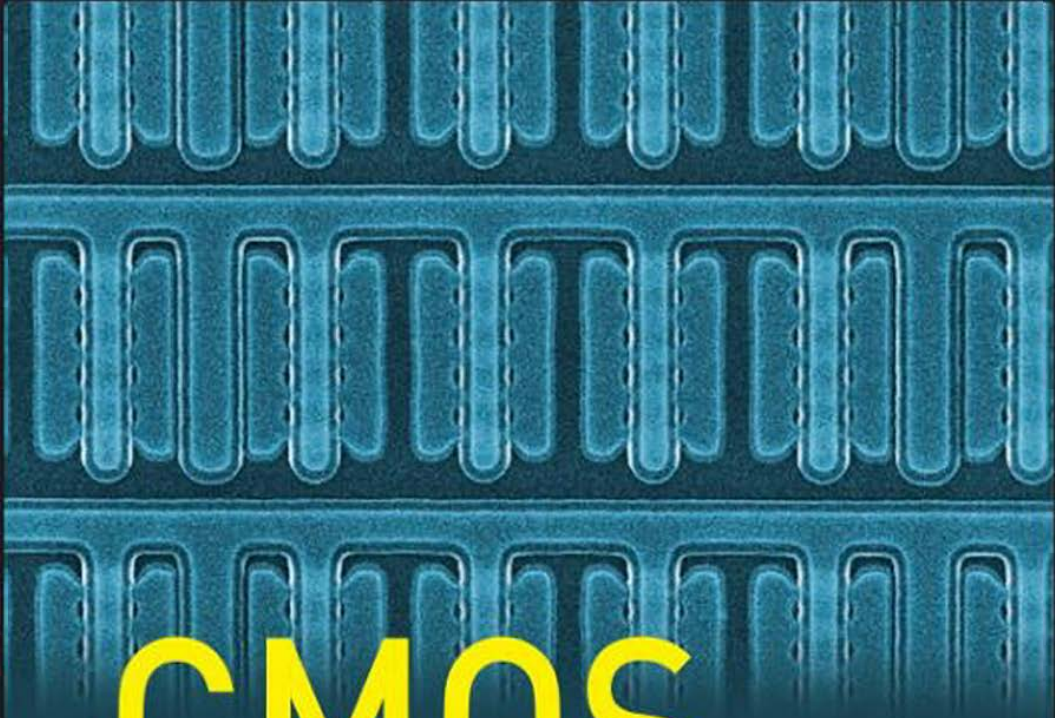

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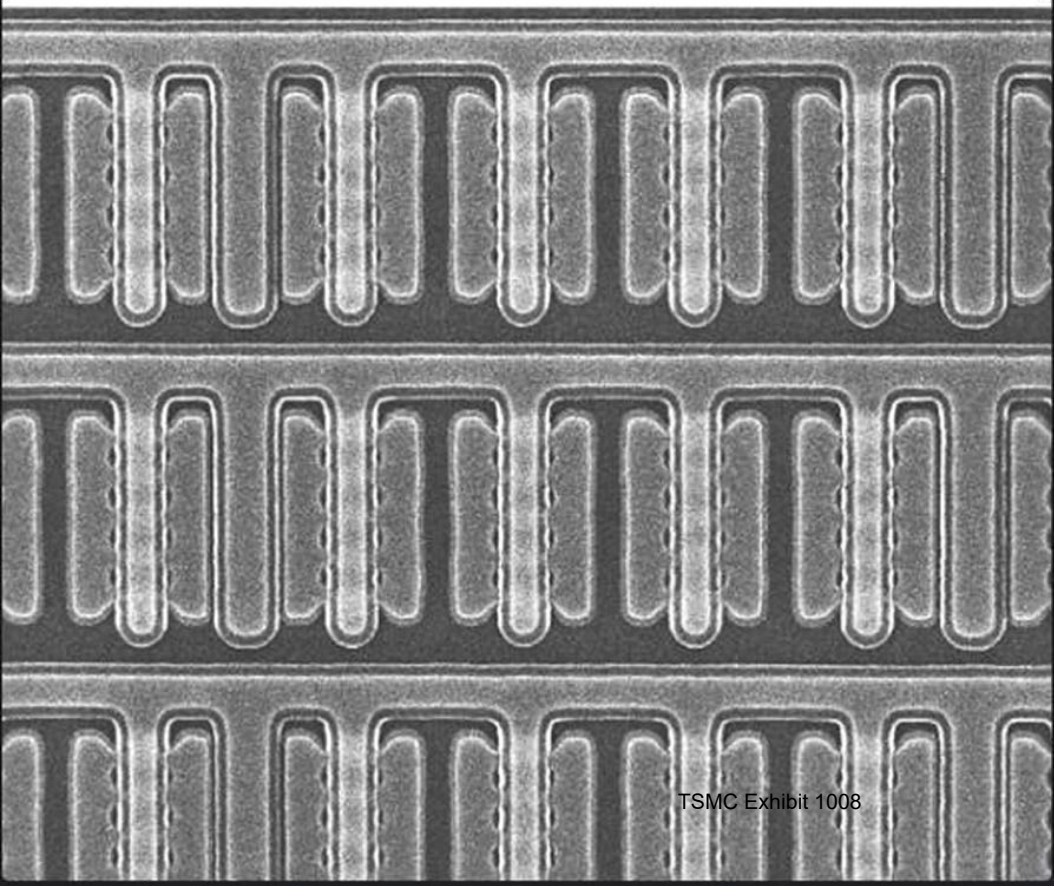

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Chapter 1

Introduction to Multi-Gate Devices and Integration Challenges

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1.1 Introduction

In May 2011 Intel announced the introduction of the tri-gate architecture at the 22 nm technology node [1]. As such, Intel was the first big player in the semiconductor industry to use a 3D device, going from a pure 2D structure that had been introduced in 1960 [2] and that had basically not changed much during almost five decades of scaling to a new device architecture that was still a MOSFET but with some new complexities and advantages: in this architecture the gate is wrapped around a thin conducting channel, also called "fin."

Tri-gate or multi-gate devices (MuGFET) in general have been the subject of much research, especially over the last 10 years. Until Intel's announcement there was still a big debate at what technology node and, if ever, they would be introduced.

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The first double-gate device, called XMOS, was proposed by the Electrotechnical Laboratory (ETL) under the Agency for Industrial Science and Technology (former AIST) in 1984 [3]. The paper demonstrated that significant reduction of short-channel effects (SCE) can be achieved by considering a fully depleted channel with more than one gate. By the end of the 1980s more publications had appeared introducing different multi-gate architectures, amongst them the Gate-All-Around (GAA) transistor [4] and the DELTA FET [5]. However, although most structures demonstrated superior electrostatics as compared to the standard bulk devices, it never came to a real breakthrough at that time.

The renewed interest was triggered by a publication at the International Electron Devices Meeting (IEDM) 1998 [6]. Although the device architecture, called FinFET (Fin Field Effect Transistor), was pretty much the same as in [5], it came at a time when CMOS scaling started to become much more challenging. The era of "happy scaling" was over: with the 90 nm technology node, leakage reduction started to become extremely challenging. So the time was right to put this device architecture in the picture again.

Many different flavors of FinFETs have been proposed over the last decade and typically they can be classified in terms of number of gates or channels and fin aspect ratio: pi-gate [7], omega gate [8] and tri-gate [9].

An overview of the most important multi-gate architectures, based on the FinFET concept, is shown and compared in Fig. 1.1. The figure shows device architectures fabricated on silicon-on-insulator (SOI) substrates; however, as we will see later, standard bulk substrates can be used as well to realize these devices. In the remainder of the chapter, we will also refer to the FinFET-based multi-gate devices as MuGFETs.

Next to FinFETs and vertical transistors [10], which can be seen as GAA, planar double-gate structures have been proposed: the silicon-on-nothing (SON) architecture [11] and the use of wafer bonding [12]. A quasi double-gate device that has gained a lot of interest lately is the ultra-thin buried oxide (UTBOX) fully depleted silicon-on-insulator (FDSOI). The BOX, scaled down to 10 nm and

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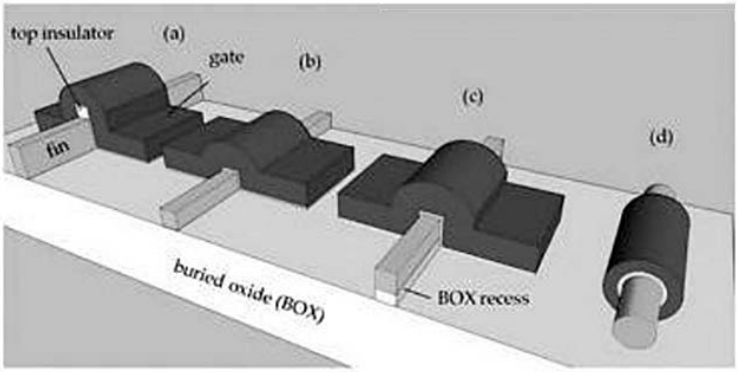

Figure 1.1. Comparison of different device architectures, the devices are schematically presented after gate patterning: (a) the originally proposed FinFET was a double-gate device, having a thick insulator on the top channel, (b) tri-gate device as proposed by Intel with a 1:1 fin aspect ratio, (c) a pi-gate device, where the recess in the buried oxide or STI allows to create a quasi fourth gate; (d) a horizontal gate-all-around nanowire.

even below, allows back gate biasing with low voltages for tuning the device performance [13].

1.2 It Is All in the Lambda...

Why are these multi-gate devices so interesting? As already mentioned in Section 1.1, until the 90 nm technology node, CMOS scaling was pretty straightforward. It was mostly lithography driven, where with every new technology node the dimensions of the MOSFET were scaled down with a factor α and the voltages with a factor k. This is known as the "constant field" scaling and was first proposed by Dennard *et al.* in 1974 [14]. Gate oxide scaling, by far the most important way of boosting the device performance, reached its limit at the 90 nm technology node and material innovations like high-k/metal gates and mobility enhancement techniques were introduced. However, it was clear that it would become more and more difficult to keep the SCE like drain-induced barrier lowering (DIBL) and the degradation of the sub-threshold swing under control in a standard planar bulk device

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1.2.1 *Where do These Short-Channel Effects Come From?*

The ideal MOSFET behavior is disturbed by the presence of the source and drain areas. For long channel devices, the impact is small and the threshold voltage V_T, off-state leakage I_{OFF} and the sub-threshold swing S are well defined and independent of the gate length and drain bias. As the channel length is scaled down, the shorter distance between source and drain will lower the potential barrier and make it dependent on the drain bias V_{DS}. A large barrier is mandatory in order to prevent the carriers from flowing to the drain when the transistor is switched off, i.e., when the gate voltage is (in absolute value) lower than $|V_T|$. This is shown in Fig. 1.2.

As a consequence V_T shows a typical roll-off behavior and DIBL increases. The latter is a measure for the V_{DS} dependency of the V_T and is defined as DIBL $= (V_T(V_{D2}) - V_T(V_{D1}))/(V_{D2} - V_{D1})$ with $V_{D1} < V_{D2}$. The latter is the case for an nMOS. Ideally the DIBL should be as low as possible because any reduction in V_T leads to increasing I_{OFF} and S (Fig. 1.3).

Multi-gate devices in general have more than one gate and allow increasing the gate control and thus the vertical electric field, thereby reducing the lateral field and the off-state leakage. In order to explain this, we will use the characteristic length lambda λ as a

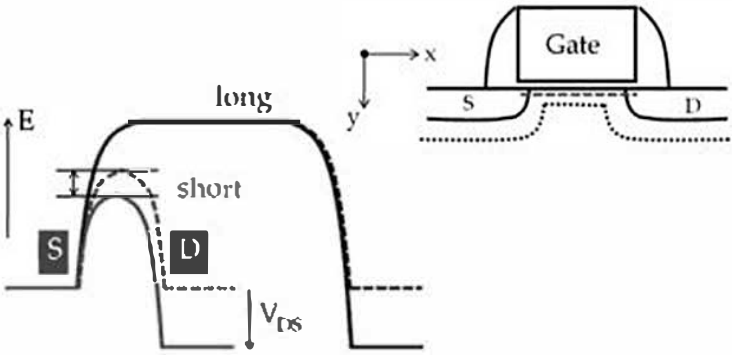

Figure 1.2. Schematic presentation of the impact of the drain bias on the potential barrier of a long channel device and a short-channel device; the potential is taken at the interface between the channel and the gate dielectric. S = source and D = drain.

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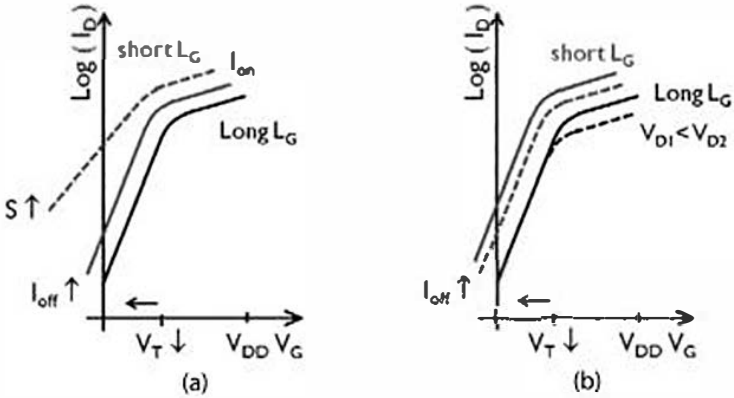

Figure 1.3. $I_{DS}-V_{GS}$ characteristics showing the impact of (a) L_G scaling and (b) the V_{DS} impact on the characteristics of short-channel devices (red curves). See also Color Insert.

figure of merit to compare different device architectures. The 3D Poisson equation is the fundamental electrostatic equation that can be used to derive the channel potential in semiconductor devices. It is usually simplified to its 2D form (Eq. 1.1).

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}=\frac{-\rho}{\varepsilon} \tag{1.1}$$

where Ψ represents the 2D electrical potential in the channel, ρ the total charge and ε the dielectric constant of the semiconductor used in the channel.

Many quasi 2D expressions of Ψ can be found in literature, amongst them the equation that can be found below (Eq. 1.2):

$$\psi(x,y)=\psi_o(y)+(V_{bi}+V_{DS}-\psi_o(y))\frac{\sinh\left(\frac{x}{\lambda}\right)}{\sinh\left(\frac{L_G}{\lambda}\right)}+(V_{bi}-\psi_o(y))\frac{\sinh\left(\frac{L_G-x}{\lambda}\right)}{\sinh\left(\frac{L_G}{\lambda}\right)} \tag{1.2}$$

where Ψ_o is the long channel surface potential, V_{bi} the built-in potential, V_{DS} the drain bias, x is the position along the channel and L_G the gate length.

An important parameter in this equation is the characteristic length λ which represents the steepness or fall-off of the potential

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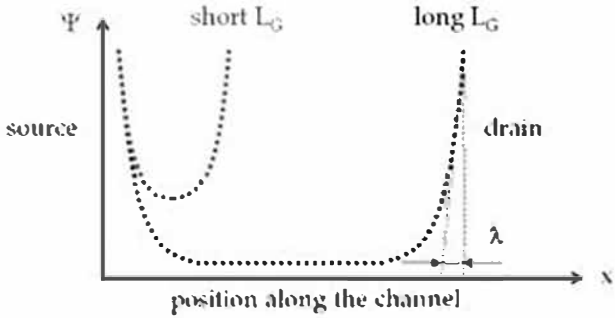

Figure 1.4. Surface potential as a function of a position x along the channel; the characteristic or natural length λ is indicated. See also Color Insert.

as shown in Fig. 1.4. A smaller λ will give rise to a steeper potential and thus lower SCE. As a rule of thumb $L \gg 2\lambda$ is needed to keep SCE under control.

Parameter λ results from the boundary conditions and is different for different device architectures (Table 1.1).

Table 1.1 clearly shows that SCE in planar devices can be reduced by either increasing the channel doping N_{SUB} (through X_{dep}) or reducing the gate dielectric thickness. Introduction of higher k

Table 1.1. Comparison of the characteristic length for various architectures; t_{ox} = gate dielectric thickness, ε_{ox} = permittivity of the gate dielectric, ε_{Si} = permittivity of the semiconductor (in this case Si), X_{dep} = maximum depletion depth and t_{Si} = Si film thickness.

Device architecture	Characteristic length λ
Planar bulk	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} X_{dep}}$
FDSOI	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} t_{Si}}$
Double gate	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{ox} t_{Si}}$
Tri-gate	$\lambda \approx \sqrt{\frac{\varepsilon_{Si}}{3\varepsilon_{ox}} t_{ox} t_{Si}}$
Gate-all-around of quadruple gate	$\lambda \approx \sqrt{\frac{\varepsilon_{Si}}{4\varepsilon_{ox}} t_{ox} t_{Si}}$
Cylindrical gate-all-around	$\lambda = \sqrt{\frac{2\varepsilon_{Si} t_{Si}^2 \ln\left(1 + \frac{2t_{ox}}{t_{Si}}\right) + \varepsilon_{ox} t_{Si}^2}{16\varepsilon_{ox}}}$

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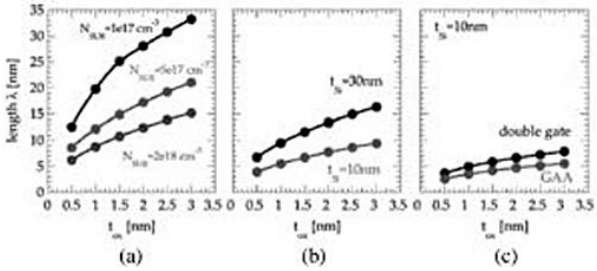

Figure 1.5. The characteristic or natural length λ is shown as function of the gate oxide thickness; in this case SiO_2 ($\varepsilon_r = 3.9$) has been assumed; (a) planar devices with different channel doping N_{SUB}, (b) FDSOI with different Si film thickness t_{Si}, (c) double-gate and GAA devices are compared. See also Color Insert.

materials like HfO_2 as gate dielectric will also be beneficial since by increasing the dielectric permittivity ε_r, λ will be decreased. The depletion depth in fully depleted devices like FDSOI, double-gate, Gate-All-Around (GAA) is defined by the Si film thickness t_{Si} or fin width W_{FIN}, as such, the natural length can be reduced significantly as is shown in Fig. 1.5.

It is clear from Fig. 1.5 that t_{Si} and t_{ox} are interchangeable: going to thin-film devices will relax the scaling requirement for the gate dielectric and vice versa. The additional benefit of going from double gate devices to Tri-gate and GAA might seem small, but one needs to realize that these device architectures will be finally considered for the sub 22 nm technology nodes where every nm counts.

Apart from the natural length other figures of merit like the electrostatic integrity EI [15] have been proposed to compare architectures and provide guidelines for device design. As a rule of thumb, typically the minimum gate length for a FinFET device needs to fulfill $L_{gmin} \geq 1.5\ W_{FIN}$ in order to have a good electrostatic control and reduce the SCE.

1.3 SOI MuGFET Versus Bulk MuGFET

A typical single fin SOI MuGFET is shown in Fig. 1.6. All relevant device dimensions are indicated. Increase of the total transistor width is usually done by patterning several fins in parallel.

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FinFET-based multi-gate devices can be fabricated on SOI substrates but also on standard bulk substrates. This architecture was first proposed in 2003 [16]. Bulk FinFET uses a fabrication scheme very close to standard bulk processing. After the Shallow-Trench-Isolation (STI), the STI oxide is recessed in order to define the fin height H_{FIN} as is shown in Fig. 1.7. During active area patterning, hard mask (HM) and resist trimming are typically used

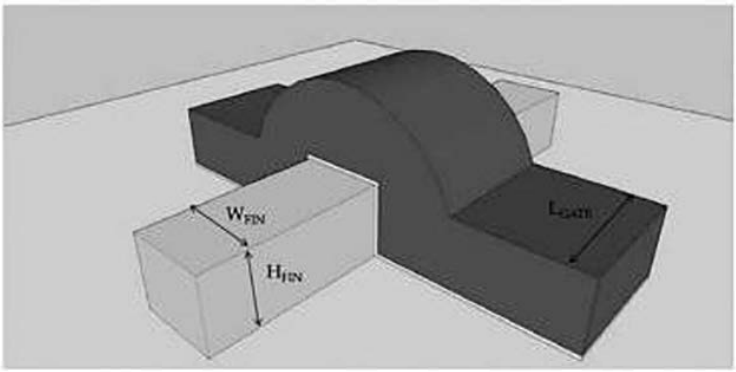

Figure 1.6. Schematic presentation of a single fin SOI MuGFET; the fin width W_{FIN}, fin height H_{FIN}, fin pitch and gate length L_{GATE} have been indicated.

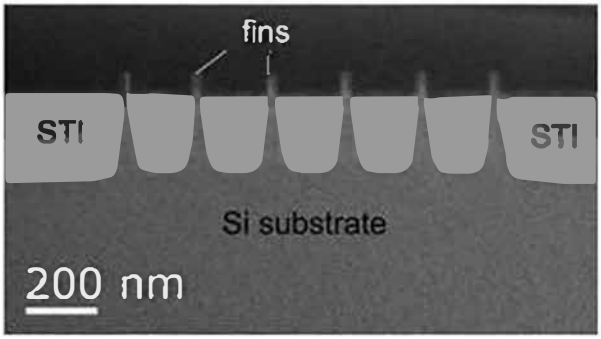

Figure 1.7. Cross section TEM showing a bulk FinFET device with six fins in parallel; the recessed STI in between the fins is visible thereby defining the fin height H_{FIN} [17].

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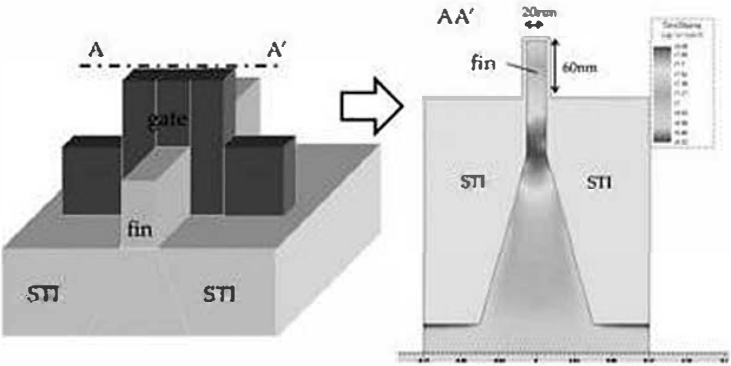

Figure 1.8. Schematic presentation of a bulk FinFET device indicating the fin/channel implantation profile; the implantation profile was obtained by TCAD process simulations [20]; in the cross section, the gate stack has been omitted. See also Color Insert.

to define the narrow fins. Well and ground plane (GP) implantations are used to reduce the leakage between transistors and between fins (Fig. 1.8). After gate stack deposition, the gate is patterned in such a way that it is wrapped around the top part of the active area.

The overall advantage of bulk FinFET is the lower cost of the substrate and the easy co-integration with standard planar bulk CMOS. The multi-gate architecture that will be used in Intel's 22 nm technology node is a bulk tri-gate device. Many other companies [18, 19] are actively looking into bulk FinFET for future technology nodes.

Finally, one needs to point out that Hisamoto's DELTA FET [5] was fabricated on a standard bulk substrate. However, local oxidation was used to finally isolate the channel from the underlying substrate.

1.4 A Typical MuGFET Process Flow

Figure 1.9 shows a schematic presentation of a MuGFET flow. For completeness, both the SOI and bulk MuGFET flows are shown. Apart from the fin patterning and channel implantations, both flows are identical from the gate patterning steps on. The figure

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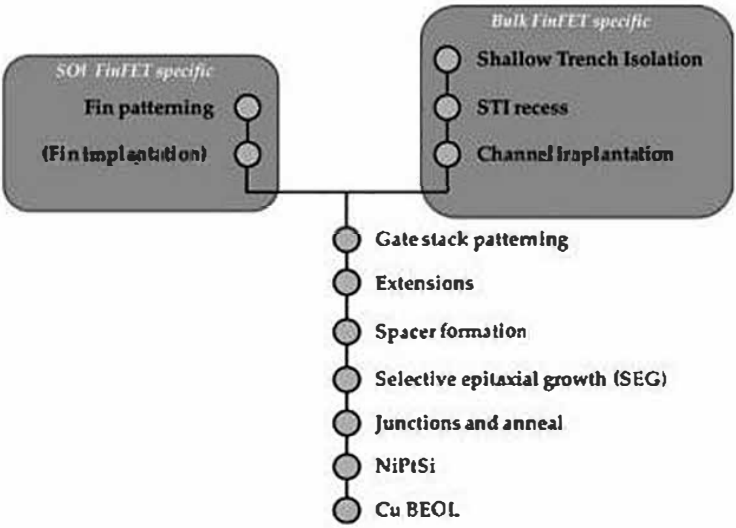

Figure 1.9. Schematic presentation of a MuGFET flow. Comparison between the SOI and bulk MuGFET flow has been made.

shows that the MuGFET fabrication follows a quite conventional Si processing. However, some specific process steps or modules will require additional restrictions and optimization, e.g., fin critical dimension (CD) control and fin height control. Next to that, process modules such as selective epitaxial growth of Si or SiGe (SEG), optional in planar bulk processing (as stressor), will be mandatory in MuGFET fabrication.

In the following sections, some of the technological challenges like fin patterning, workfunction engineering and strain engineering will be briefly addressed. In part I, some selected topics will be discussed in detail.

1.4.1 *Challenges*

1.4.1.1 Fin width patterning

One of the most important challenges in MuGFET integration is the formation of sub-10 nm wide fins. As we have seen in Section 1.2, narrow fins are required to fully benefit from the increased short-

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channel control in multi-gate devices. A standard way of defining the fins is by optical lithography and dry etch. The MuGFET device layout can be very diverse depending on the application, for example, standalone single fins are used in the case of SRAMs while multiple fin devices with large source and drain pads are more suitable for ring-oscillators etc. Each of these different device layouts requires optimization of the lithography settings in order to control the fin width [21]. As such the development of a model-based Optical Proximity Correction (OPC) is needed.

The requirement at litho level is very stringent: assuming a target fin width of 10 nm and allowing a maximum variation in fin width of 10% in order to keep the maximum V_T shift at L_{GATE} = 20 nm smaller than 70 mV, this would mean that at litho level only a litho CD variation of 1.5% can be allowed taking into account a specific and constant etch bias (which is in this case 60 nm). However, this assumes that W_{FIN} variation is the main cause of V_T variability. Other important sources of variability are L_{GATE} and fin height H_{FIN} variations. The latter is especially important for bulk MuGFET. Figure 1.10 shows the V_{T_lin} dependency on fin width and L_{GATE}. In this case, the results are for SOI MuGFETs. For short (< 70 nm) gates, the W_{FIN} dependency on V_{T_lin} is found to be surprisingly weak, while for longer gate lengths, a strong V_{T_lin} increase is observed, especially for narrow fins. This increase can be attributed to fin width fluctuations, as is confirmed by Monte Carlo simulations accounting for the quantum confinement. The largest impact on variability is seen for long gates and narrow fins. In Chapter 2, the trade-offs that need to be considered for fin patterning in high density circuits will be further detailed out.

An alternative fin fabrication technique is the spacer defined patterning technique. This technique can provide double and even quadruple fin density with less stringent lithography requirements [23]. In this case, a dummy pattern (typically SiGe or oxide) is defined and then spacers are formed next to the dummy pattern, which will eventually define the fin spacing. The dummy areas are removed selectively towards the spacers and the spacers are used as a hard mask during the formation of the fins. This can finally also be done in combination with optical lithography if, for example, large source/drain pads need to be patterned. A schematic

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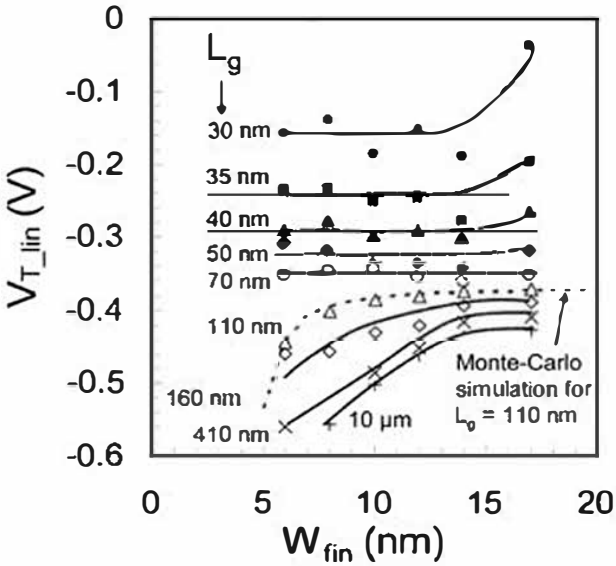

Figure 1.10. pMOS $V_{T,lin}$ *vs.* W_{FIN} for various L_{GATE}. The dashed line corresponds to the simulation of a device with L_{GATE} = 110 nm including W_{FIN} fluctuations [22].

view of the process flow is shown in Fig. 1.11. Although the processing is somewhat more complex and only allows patterning even number of fins, it has quite some advantages: it provides a more uniform pattern size, thereby reducing the fin width variability, and much higher device density than the current optical lithography. Devices and circuits with a fin pitch as small as 50 nm have been demonstrated in [23].

Apart from the ability to fabricate these narrow fins, metrology tools have to guarantee a high enough accuracy to measure features far below 10 nm. For example, a 5 nm accuracy error would correspond to a 30% change in CD when dealing with a 15 nm feature, which is unacceptable. Next to that, Line Width Roughness (LWR) and sidewall roughness have a direct impact on device performance. A robust metrology to characterize these elements in both development and production is required [24].

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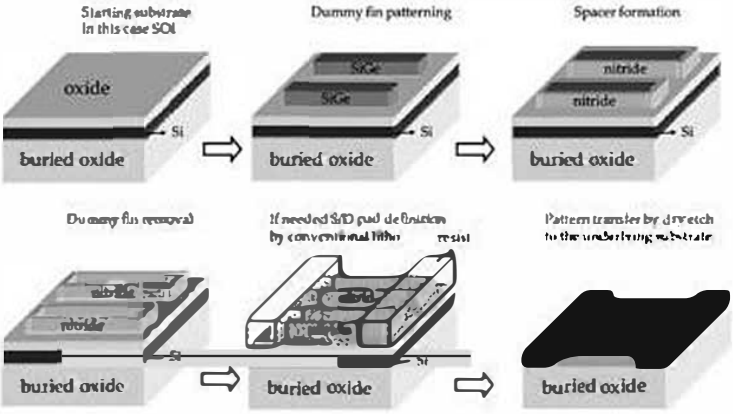

Figure 1.11. A schematic presentation of the spacer defined MuGFET process flow.

1.4.1.2 Work function engineering

Work function engineering relates to the V_T setting and tuning and will be discussed in more details in chapter three. The threshold voltage setting and tuning in planar devices is usually achieved by increasing or decreasing the channel implant, using halo implantations for the short gate lengths, scaling the gate dielectric or using a metal gate to tune the work function (Eqs. 1.3 and 1.4):

$$V_T = 2\varphi_F + V_{FB} + \frac{\sqrt{2q\varepsilon_{Si}N_{sub}|2\varphi_F + V_{BS}|}}{C_{ox}} \tag{1.3}$$

$$\varphi_F = \frac{kT}{q}\ln\left(\frac{N_{sub}}{n_i}\right) \tag{1.4}$$

with φ_F the fermi voltage, V_{FB} the flatband voltage, C_{ox} the gate capacitance per unit area, k the Boltzmann constant, T the temperature, q the electron charge, V_{BS} the substrate bias and N_{sub} the channel doping.

In the case of MuGFET devices, the full depletion of the fin makes threshold voltage setting and tuning with implantation very difficult [25]: the depletion width of the transistor is determined by the Si film thickness and cannot be changed by mere channel implantation. One needs to note that this is also the case in narrow bulk FinFET

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devices. The well and GP implants, in this case, are only used to prevent a large subsurface leakage current from flowing.

Therefore work function tuning with metal gate is the most efficient way of setting the V_T in MuGFET devices. Integration of a single metal gate is the preferred solution when considering process complexity. A single mid-gap metal like TiN or TaN on planar bulk devices typically results in either high threshold voltages or poor short-channel control. In MuGFET, the mid-gap work function leads to almost symmetric threshold voltages for nMOS and pMOS, which are able to fulfill the LSTP requirements [26]. However, different flavors of V_T are needed: low, medium, high V_T. Different from planar bulk devices, MuGFETs need less shifting from the mid-gap work function in order to reach the low V_T targets [27]. Different techniques have been considered for V_T tuning: implantation into the metal gate [28], TiN thickness variation [29] and the use of dielectric capping layers [30]. Recently also the use of buried channel architectures has been considered. Especially Si/SiGe buried channels for pMOS allow reducing the V_T by more than 300 mV (for $Si_{55}Ge_{45}$) [31] while using a metal gate with a work function closer to the n-type band edge.

These are all "gate first" fabrication schemes, where the final gate stack (electrode and gate dielectric) is fabricated quite early in the process flow. Over the last years, there has also been a shift from "gate first" to "gate last" processing [32]. In the latter fabrication scheme, a dummy gate is patterned. The dummy gate is removed after source/drain silicidation and replaced by the final gate stack. Several combinations are possible: either both electrode and gate dielectric are replaced or only the gate electrode is replaced. One of the advantages of the "gate last" process is that the final metal gate is not exposed to the high activation anneal for the junctions. As a result, a better controlled work function for nMOS and pMOS can be achieved.

All these techniques, typically used in planar bulk devices, need to be compatible with the higher topography in MuGFETs. This requires highly conformal deposition techniques for the gate electrode and dielectric, and in the "gate last" process this also requires a careful optimization of the dummy gate processing and

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subsequent Chemical Mechanical Polishing (CMP) of this dummy gate in order to be able to remove it efficiently after silicidation.

1.4.1.3 Access resistance

For the 22 nm technology node and beyond, fin widths smaller than 10 nm will be needed to maintain good short-channel behavior as was discussed in Section 1.2. Just like in fully depleted SOI (FD SOI) where ultra-thin Si films are needed to obtain good electrostatic control, the access resistance is very high in narrow fin devices [33]. Many publications [34] have addressed the issue and it will be briefly discussed in this section. Chapter 4 will give a more detailed overview of the challenges and solutions to reduce the access resistance.

Overall the parasitic source/drain resistance $R_{S/D}$, which becomes more dominant when the gate length is scaled down, consists of the following contributions [35]:

$$R_{S/D} = R_{CON} + R_{SH} + R_{SP} + R_{ACC} \tag{1.5}$$

where R_{CON} represents the contact resistance, R_{SH} the sheet resistance of the deep source/drain areas with uniform current flow, R_{SP} the spreading resistance and R_{ACC} the accumulation resistance under the gate overlap. Especially the early MuGFET devices suffered from very high R_{CON}. One way to reduce the contact resistance is increasing the contact area. This can be achieved by the implementation of selective epitaxial growth of Si or SiGe (SEG) on the source and drain areas. At the same time, SEG reduces the over-silicidation that occurs in aggressively scaled fins. This problem is more severe for nMOS than for pMOS since p-type dopants like boron typically retard the Ni-silicidation. As a consequence, the NiSi thickness on n-type areas is overall much thicker than on p-type areas. Next to that, the multi-directional consumption of Si during the silicidation and the limited amount of available Si can lead to a full silicidation of the fin. In the worst case, the silicide can overrun the source and drain areas since the Ni is the diffusing species and it will look for available Si to form NiSi. This silicide encroachment will not only lead to an increase in source/drain resistance but also an increase in gate-induced drain leakage (GIDL) [36]. A typical

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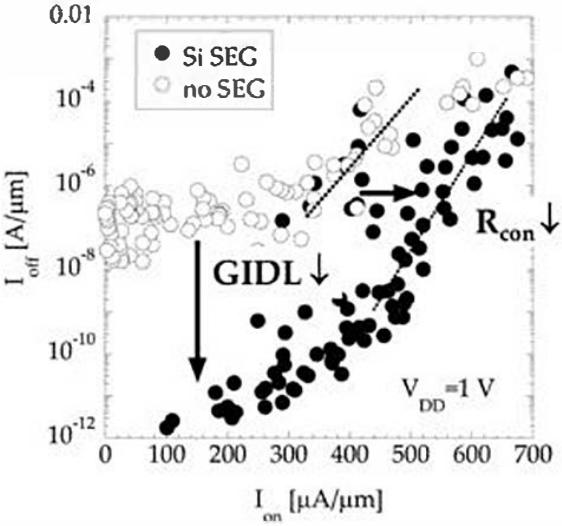

Figure 1.12. $I_{ON} - I_{OFF}$ characteristics comparing nMOS devices with and without Si S/D SEG; the fin width of the devices is 25 nm and the SEG thickness is 30 nm [36].

Schottky barrier FET behavior is seen and this leads to an increased off-state leakage. Also here, the use of SEG can reduce the GIDL significantly (Fig. 1.12).

In order to meet the ITRS requirements for the 22 nm technology node and beyond [26], other contributors like the spreading and sheet resistance will need to be addressed. In [38] it was shown that one of the root causes for the high access resistance in aggressively scaled fins is related to the full amorphization of the fins during source/drain implant and its problematic recrystallization during the high temperature anneal. In sub-20 nm wide fins, surface proximity suppresses crystal regrowth and promotes the formation of twin boundary defects in the implanted region. If solid-phase epitaxy (SPE) is significantly retarded, random nucleation and growth (RNG) may take place and part of the fin transforms into polysilicon. Therefore, alternative implantation techniques like plasma doping and vapor phase doping can bring some extra benefits in forming conformal junctions with limited amorphization

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of the fins. The latter techniques might also solve the problem of implant tilt limitation in high density circuits like SRAMs. The close proximity of the implant masks and the small fin-to-fin spacing do not allow high implantation angles. Consequently, the implantation profile is largely non-conformal (the implantation of the top is different from the sidewalls). Device simulations have shown that this reduces the on-state current of the devices significantly. Some groups have proposed the use of one-sided implants to partially overcome this issue [39].

1.4.1.4 Strain engineering

Since the 90 nm technology node, strain engineering techniques like SiGe S/D stressors and strained contact etch stop layers (sCESL) have been very efficient in boosting the performance of planar bulk devices. MuGFET devices in general do not require channel implants and intrinsically the mobility can be higher than the standard planar devices. However, the different crystal orientation of the sidewalls as compared to the top, can either improve the mobility or decrease it [40]. The former situation is valid for pMOS when the sidewall orientation/current direction is (110)/<110> while this combination of crystal plane and current direction is more detrimental for nMOS devices. Next to that, the fin patterning reactive ion etch (RIE) leads to increased sidewall roughness thereby reducing the channel mobility. Surface smoothening by H_2 anneal [41] has been demonstrated to increase the mobility. However, the impact of the H_2 anneal is quite layout dependent and careful optimization of the process conditions is needed. One of the most straightforward and efficient ways of introducing strain into both planar and multi-gate devices is the use of intrinsically strained SiN layers or sCESL. Publications [43] have shown that the nMOS performance can be improved significantly by the use of tensile sCESL (Fig. 1.13). With the help of TCAD [43] it has been demonstrated that downscaling of the fin width and increase of the fin height will lead to higher top-down and longitudinal stress components. Both are beneficial for nMOS mobility. Furthermore it has been demonstrated that tensile sCESL can also be used on pMOS without degradation of the current. This allows a more simple

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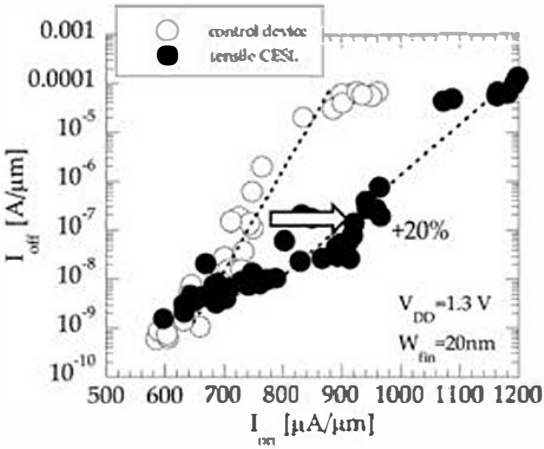

Figure 1.13. I_{ON}–I_{OFF} of nMOS devices with W_{fin} = 20 nm and H_{fin} = 65 nm; the impact of tensile sCESL is shown [46].

process scheme where a single tensile sCESL can be used to improve nMOS without negative impact on the pMOS. sCESL can also be combined with substrate level stressor like strained SOI (SSOI) for nMOS [44] or strained SiGe (SGOI) for pMOS [45].

However, it is important to point out that the efficiency of sCESL is reduced or altered when the fin and poly pitch are scaled down and the device layout is different, e.g., single vs. multiple fins.

The use of embedded SiGe S/D for pMOS [46] and Si:C for nMOS has also been demonstrated in MuGFET devices [48]. In SOI MuGFETs, typically the impact on the mobility is small as the recess depth is limited due to the Si film thickness. This stressor has shown to be more efficient in planar bulk devices [49].

Finally, all strain need to be compatible with "gate last" processing which is considered the most feasible way of introducing metal gates. Only a small amount of publications have appeared on the latter topic but it can be noticed that the overall trends in MuGFET devices are the same as compared to planar bulk. Stressors like sCESL give higher improvement when combined with a "gate last" process [50].

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1.5 From MuGFET to Nanowires

Nanowires are devices with a diameter of 10 nm and less, even down to a few nanometers. These devices demonstrate unique properties because, at this scale, quantum mechanical effects cannot be neglected anymore [51]. A wide variety of nanowires have been studied and processed, some are non-Si like carbon nanotubes (CNTs) [52] and they can have a wide variety of applications, but most Si nanowire transistors are FinFET-based. Typically, the fins are scaled down by sacrificial oxidation and HF wet etch [53] or rounded by H_2 anneal [54], and the gate is completely wrapped around the wire. The gate all-around structure allows for the most optimal electrostatic control and these devices have shown excellent scalability [55, 56]. Publications have also demonstrated that the gate length can be reduced to the extent that quasi-ballistic transport occurs [57, 58]. However, the quantum confinement, which is a result of the aggressive scaling of the channel diameter, leads to an unwanted increase in threshold voltage [59]. The carriers in the channel start to occupy discrete energy levels where the lowest energy level is located at a higher level than the bottom of the conduction band. This is different from the traditional continuum of energy levels or bands found in bulk materials. As such, more band bending is required to form the inversion layer in the channel.

Different groups have also described the observation of oscillations in the drain current versus gate voltage at low temperatures, but even at room temperature when the drain bias is low enough [60, 61]. These oscillations can be attributed to the filling of the consecutive 1-D energy sub-bands by electrons as the gate voltage is increased. Next to horizontal devices, vertical nanowire FETs [62] and multi-stacked nanowires, based on the SON technology, have been demonstrated [63].

Apart from their use in standard CMOS applications, there are many possible applications that can benefit from the specific properties of nanowire devices: optics, mechanics, sensors etc. Due to the high surface-to-volume ratio, they can be used as highly sensitive biosensors [64]. Solar cell applications benefit from the reduced reflection, extreme light trapping, improved band gap tuning, easy strain relaxation and increased defect tolerance [65].

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1.6 Conclusions

In this introductory chapter, we have briefly reviewed the history of multi-gate devices, starting with the very first demonstrations in the early 1980s up to Intel's announcement to introduce the tri-gate architecture, fabricated on a standard bulk substrate, at the 22 nm technology node.

The advantages of these devices lie in their excellent electrostatic control and SCE robustness. The significant reduction of the off-state leakage as compared to the standard planar bulk MOSFETs make them into excellent candidates for low voltage-low power applications.

For more than a decade, FinFET-based multi-gate devices have been studied by many research groups and although the integration of these devices is very similar to their planar counterparts, the challenges lie in the process control of specific steps like fin and gate patterning. Similar to the thin film in FDSOI, the scaled fin gives rise to an increased external resistance which has typically been seen as one of the possible showstoppers. Introduction of SEG and novel doping techniques has provided a solution to the aforementioned problem. Next to that, strain engineering techniques will be required to enhance the mobility, similar to planar bulk technology.

The ultimate MOSFET architecture will be a gate all-around device where the gate stack is wrapped around a nanowire of only a few nanometers. These devices demonstrate unique features like quantum confinement and possible ballistic transport when the gate length is scaled down. Apart from the standard CMOS applications, there is a growing interest of using nanowires in, for example, bio-applications and solar cells.

Acknowledgments

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