

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,
Petitioner

v.

Marlin Semiconductor Ltd.,
Patent Owner

Case No. – Not Yet Assigned
U.S. Patent No. 8,993,384

**DECLARATION OF DR. JACK LEE IN SUPPORT OF PETITION FOR
INTER PARTES REVIEW OF UNITED STATES PATENT NO. 8,993,384**

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I, Jack Lee, do hereby declare:

1. My name is Jack Lee. I am making this declaration at the request of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) in the matter of the *Inter Partes* Review of U.S. Patent No. 8,993,384 (“the ’384 Patent”).

2. I am being compensated for my work in this matter at my standard rate of \$680 per hour for such consulting services. My compensation in no way depends on the outcome of this proceeding.

3. I have been asked to provide my opinion on the technology covered by the ’384 Patent and the validity or invalidity of claims 1-9 of the ’384 Patent (“Challenged Claims”).

I. Qualifications

4. My qualifications generally are set forth in my *curriculum vitae*, which is submitted as Exhibit 1026.

5. I am an expert in the field of semiconductor design and process technology and have forty years of first-hand experience as a researcher, educator, and consultant in this field.

6. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

7. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

8. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

9. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

10. My current research and teaching interests encompass semiconductor devices including 3D structures such as FinFETs or tri-gate MOSFETs, high-K gate dielectrics and gate electrodes, fabrication processes, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and

passivation processes, display technologies, photovoltaic and solar cell technologies, semiconductor memory applications, and alternative channel materials.

11. I have been invited to give talks, teach short courses and participate in panel discussions at numerous conferences specifically on the topic of fabrication processes for nanoscale devices such as FinFETs and gate-all-around MOSFETs, high-K gate dielectrics, gate electrodes, and semiconductor memory devices. This includes prestigious conferences such as the Symposium on VLSI Technology, the IEEE International Electron Devices Meeting, and other global forums. My research group at The University of Texas at Austin is recognized as a pioneer in developing high-K gate dielectric metal-gate processes for nanoscale MOSFETs including FinFETs. I have extensive experience in this field, with numerous publications in journals and conference proceedings on the topics of nanoscale MOSFETs and FinFETs, fabrication processes, characterization, and device reliability.

12. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

13. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 book and book chapters on semiconductor technologies.

I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g. inventor recognition and best paper awards.

14. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

15. I have served in various technology consulting and business advisor roles. For example, I have been teaching short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field

16. Taken as a whole, my academic and practical experience have given me a substantial basis upon which to evaluate the technology that is in question in the claims of the '384 patent. Based on my experience and education, and the acceptance of my publications and professional recognition by peers in my field, I believe that I am qualified to opine as to the knowledge and level of skill of one of ordinary skill in the art at the time of the alleged invention of the '384 patent (which I further describe

below) and what such a person would have understood at that time, and the state of the art during that time.

II. Materials Reviewed

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field, and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the invention of the '384 Patent.

18. I understand that the prior art references and other documents that I discuss in this declaration will be filed with the Petition for *Inter Partes* Review in this matter ("Petition") and assigned exhibit numbers. I also understand that other exhibits, not referenced in this declaration may also be filed with the Petition.

19. In forming my opinions, I have reviewed and considered the following documents, identified by exhibit number:

Exhibit No.	Description
Exhibit 1001	U.S. Patent No. 8,993,384 ("384 patent").
Exhibit 1002	Prosecution History of the '384 patent.
Exhibit 1004	U.S. Patent No. 9,166,022 B2 ("Xu").
Exhibit 1005	U.S. Patent 2012/0091538 A1 ("Lin").
Exhibit 1006	U.S. Patent Pub. No. 2005/0148137 A1 ("Brask").
Exhibit 1007	T. Ghani et al, <i>A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45 Nm Gate Length Strained Silicon CMOS Transistors</i> , IEEE International Electron Devices Meeting 2003, pp. 11.6.1-11.6.3, (2003).
Exhibit 1008	Excerpts from N. Collaert, <i>CMOS Nanoelectronics</i> (2012).

Exhibit 1009	A. Veloso et al., <i>Gate-Last vs. Gate-First Technology for aggressively scaled EOT Logic/RF CMOS</i> , Symposium on VLSI Technology – Digest of Technical Papers, pp. 34-35, (2011)
Exhibit 1010	M. Quirk and J. Serda, <i>Semiconductor Manufacturing Technology Instructor's Manual</i> (2001) (archived Sep. 28, 2007).
Exhibit 1011	Excerpts from S. P. Muraka et al., <i>Interlayer Dielectrics for Semiconductor Technologies</i> (2003).
Exhibit 1012	Excerpts from D. Neaman, <i>Semiconductor Physics and Devices</i> (2012).
Exhibit 1013	D. Hisamoto et al., <i>Folded-channel MOSFET for deep-sub-tenth micron era</i> , International Electron Devices Meeting 1998 – Technical Digest, pp. 1032-1034, (1998).
Exhibit 1014	X. Huang et al., <i>Sub 50-nm FinFET: PMOS</i> , International Electron Devices Meeting 1999 – Technical Digest, pp. 67-70, (1999)
Exhibit 1015	D. Hisamoto et al., <i>FinFET – a self-aligned double-gate MOSFET scalable to 20 nm</i> , IEEE Transactions on Electron Devices, Vol. 47, No. 12, pp. 2320-2325 (2000)
Exhibit 1016	J. Markoff, <i>Intel Increases Transistor Speed by Building Upward</i> , New York Times (2011)
Exhibit 1017	Intel, <i>Intel's Revolutionary 22 nm Transistor Technology</i> (2011).
Exhibit 1018	A. Shimpi, <i>Intel Announces first 22nm 3D Tri-Gate Transistors, Shipping in 2H 2011</i> , AnandTech (2011) (archived May 18, 2011).
Exhibit 1019	K. Mistry et al., <i>A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging</i> , 2007 IEEE International Electron Devices Meeting, pp. 247-250 (2007).
Exhibit 1020	U.S. Patent No. 7,525,160 B2 (“Kavalieros”)
Exhibit 1021	S. Thompson et al., <i>Key Differences for Process-Induced Uniaxial vs. Substrate-Induced Biaxial Stressed Si and Ge Channel MOSFETs</i> , Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 221-224 (2004)

Exhibit 1022	C. Auth et al., <i>45nm High-k + Metal Gate Strain-Enhanced Transistors</i> , 2008 Symposium on VLSI Technology, pp. 128-129, (2008)
Exhibit 1023	S. Mayuzumi et al., <i>High-Performance Metal/High-k n- and p-MOSFETs With Top-Cut Dual Stress liners Using Gate-Last Damascene Process on (100) Substrates</i> , IEEE Transactions on Electron Devices, Vol. 56, No. 4, pp. 620-626, (2009)
Exhibit 1024	Excerpts from G. May and S. Sze, <i>Fundamentals of Semiconductor Fabrication</i> (2004).
Exhibit 1025	Excerpts from S. Wolf, <i>Microchip Manufacturing</i> (2004).
Exhibit 1026	Curriculum Vitae of Jack Lee, Ph.D

III. Relevant Legal Standards

20. I am an engineer by training and profession. The opinions I am expressing in this report involve the application of my knowledge and experience to the evaluation of certain prior art with respect to the '384 patent. My formal knowledge of patent law is no different than that of any lay person. Therefore, I have requested the attorneys from Jones Day, who represent TSMC, to provide me with guidance as to the applicable patent law in this matter. The paragraphs below express my understanding of how I must apply current principles related to patent validity to my analysis.

A. Claim Construction

21. I have been informed that that in determining whether a patent claim is obvious in view of the prior art, the Patent Office must apply the *Phillips* standard to construe the claim by giving the claim its plain and ordinary meaning as understood

by a POSITA at the time of the invention, in light of the specification and prosecution history.

22. For the '384 patent, I have been asked to consider the relevant time as just prior to June 9, 2013, the filing date of the '384 patent. For the purposes of this review, I have construed each claim term in accordance with its plain and ordinary meaning under the *Phillips* standard, unless otherwise indicated.

B. Obviousness

23. I have been informed that a claim is unpatentable under 35 U.S.C. § 103 if the claimed subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the invention. As mentioned above with respect to claim construction, I have been asked to consider the relevant time as just prior to June 9, 2013, which is the filing date of the '384 patent. I understand that an obviousness analysis takes into account the scope and content of the prior art, the differences between the claimed subject matter and the prior art, and the level of ordinary skill in the art at the time of the invention.

24. In determining the scope and content of the prior art, it is my understanding that a reference is considered analogous prior art if it falls within the field of the inventor's endeavor. In addition, a reference is analogous prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an

inventor's attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

25. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires the claimed invention to be considered as a whole. This "as a whole" assessment requires showing that one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

26. It is my further understanding that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include:

- combining prior art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- a predictable use of prior art elements according to their established functions; applying a known technique to a known device (method or product) ready for improvement to yield predictable results;

- choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and
- some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

27. I have been told that a prior art reference may combined with one or more references and/or with the knowledge of a person of ordinary skill in the art to show obviousness. I have also been told that a person of ordinary skill in the is presumed to know all relevant prior art. I have also been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

28. I understand that when combining prior art elements, the obviousness analysis requires determining whether a person of ordinary skill in the art would have had a “reasonable expectation of success” in arriving at the claimed invention by combining those elements. I have been told that a “reasonable expectation of success” does not require “absolute predictability.”

29. I have been told that the strongest rationale for combining references is a recognition, expressly or impliedly, in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their

combination. I have also been told that combining two embodiments disclosed adjacent to each other does not require a leap of inventiveness.

C. Applicant Admitted Prior Art

30. I have been told that admissions in a patent's specification ("Applicant admitted prior art" or "AAPA") may, in certain instances, be relevant to an analysis of whether the patent's claims would have been obvious. I have also been told that an example of such an instance where it may be permissible to rely AAPA is to show the general knowledge of a skilled artisan.

IV. Person Of Ordinary Skill In The Art

31. It is my understanding that when interpreting the claims of the '384 Patent, I must do so based on the perspective of a POSITA as of the relevant priority date. My understanding is that the earliest claimed priority date of the '384 Patent is June 9, 2013.

32. In my opinion, a person of ordinary skill in the art for the '384 Patent would have been a person having at least a Master's degree in electrical engineering, physics, chemistry, materials science, or a related field, and three years of work experience in semiconductor manufacturing, such as, for example, in integrated circuit device (or transistor) design and/or manufacturing, as of June 9, 2013. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for formal less education.

33. As described in detail above in the “Qualifications” section, my own training and experience exceeds that of one of ordinary skill in the art.

V. Background

A. Technology Background

34. The '384 patent relates to semiconductor devices. Semiconductor devices are generally manufactured on silicon wafers and comprise billions of transistors.

35. Transistors are the fundamental building blocks for semiconductor chips. Each transistor operates as a switch that either allows or blocks the flow of electrical current. By combining thousands, or even billions of transistors together, circuit designers can implement electronic hardware like processors used in computers, mobile phones and other semiconductor devices.

36. A typical transistor, known as a MOSFET (metal-oxide-semiconductor field-effect transistor) has three main components: a “source,” a “drain,” and a “gate.” When the transistor is “off,” no current flows between the source and drain. When a proper voltage is applied to the gate, the transistor is turned on, allowing current to flow through the “channel region” between the source and drain.

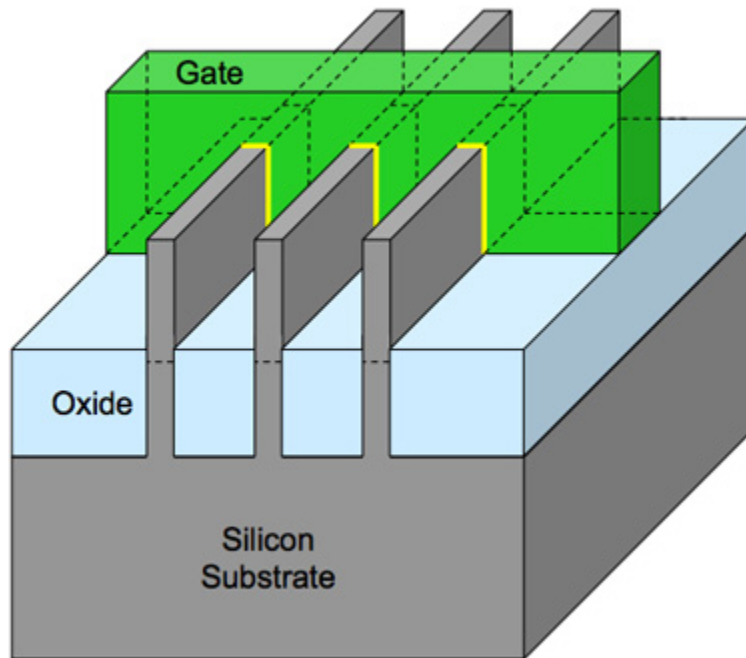
37. Transistors are classified as either “n-type” or “p-type.” In n-type MOSFET (or nMOS), current is carried by negatively charged electrons, and the source and drain regions doped with n-type impurities (e.g. arsenic or phosphorus),

which contribute free electrons due to their higher valence electron count. In contrast, p-type MOSFET (or pMOS) conducts current via holes (positively charged carriers), and the source and drain regions are doped with p-type impurities (e.g., boron) which have fewer valence electrons and create a surplus of holes. In both cases, current flows through the channel when the transistor is in the on-state.

1. FinFETs

38. Around 1999, Chenming Hu, who served as TSMC's CTO, introduced a new type of transistor that he called "FinFETs." *See* Exhibits 1013, 1014, 1015. FinFETs are so named because the transistor channel is formed in a thin vertical "fin" of silicon protruding from the substrate. The gate electrode wraps around multiple sides of this fin, typically the top and two sidewalls, offering improved electrostatic control over the channel compared to traditional planar MOSFETs. For this contribution, President Obama awarded Dr. Hu the National Medal of Technology and Innovation for his invention of FinFETs.¹ A representative FinFET structure is shown below:

¹ *See* <https://www.chu.berkeley.edu/biography/>.



Ex. 1017 at 7. As shown above, the gate overlays multiple surfaces of the silicon fin, allowing for more effective control of the channel region between source and drain. FinFET transistors on the wafer are separated by dielectric materials, e.g. oxide, on the wafer. These devices are often referred to as tri-gate transistors, and later generations evolved into gate-all-around (GAA) structures, where the gate completely surrounds the channel. A POSITA would have understood “FinFET” to refer broadly to a class of non-planar transistors characterized by a raised semiconductor fin structure with tri-gate, double-gate, and gate-all-around configurations recognized as specific implementations with that broader FinFET architecture. The motivation for these non-planar geometries was to improve gate control over the channel, thereby reducing leakage current during the off-state. This translates into lower static power dissipation and

significantly enhanced battery life, making such transistors particularly attractive for mobile and low-power applications.

39. As described further below, by 2004, it was already known that transistor performance is improved by introducing strain into the transistor channel by using epitaxial techniques. For example, silicon germanium (or “SiGe”) was commonly used in the source and drain regions to induce compressive strain, particularly for pMOS devices, thereby improving carrier mobility and drive current. Ex. 1007 at 978-980 and Ex. 1019 at 247-250.

40. Thus, long before the priority date of the '384 patent, FinFET transistors fabricated by forming fin structures, isolation structures, gate structures, and epitaxially formed source/drains were already well-known in the art. In fact, by 2013, the priority date of the '384 patent, Intel had already commercialized FinFET-based products with this architecture. *See* Exs. 1016,² 1017,³ 1018.⁴ TSMC, likewise, had developed and held numerous patents on FinFET transistors featuring these same fabrication elements, as further discussed below in connection with the Xu and Lin prior art references.

² <https://www.nytimes.com/2011/05/05/science/05chip.html>.

³ https://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf.

⁴ <https://web.archive.org/web/20110518133030/http://www.anandtech.com:80/print/4313/intel-announces-first-22nm-3d-trigate-transistors-shipping-in-2h-2011>.

2. Stressed/Strained Channels

41. The introduction of strained silicon channels in the early 2000s marked a major leap in CMOS technology by significantly enhancing carrier mobility. This innovation enabled higher transistor speeds and improved drive current without requiring aggressive reductions in gate length. A key technique for inducing strain involved recessing the source/drain (S/D) regions adjacent to the gate and then epitaxially regrowing them with lattice-mismatched materials. For example, silicon-germanium (SiGe) was widely adopted in pMOS transistors to apply compressive strain, while silicon-carbon (SiC) or pure silicon was used in NMOS devices to induce tensile strain. *See e.g., Ex. 1004 at 1:16-38; Ex. 1005 at ¶¶ [0002], [0035].* Strain engineering works by altering the silicon crystal lattice in the channel region, which reduces carrier scattering and increases the speed at which electrons or holes can travel through the device, thereby lowering transistor delay and improving switching performance. *See Ex. 1021 at 221-224.*

42. This technique became mainstream in high-performance CMOS processes starting around the 90 nm node (~2003) and continues to be used in advanced nodes today. The process typically involves selective etching (i.e., recessing) of the S/D regions followed by selective epitaxial growth (SEG)—i.e., regrowing—using chemical vapor deposition (CVD), which deposits the desired stressor material only on exposed silicon surfaces. This induces localized stress in the

channel region without significantly altering the device geometry, and the substrate remains silicon throughout. Over time, this method became standard practice and is often combined with other strain-engineering techniques, such as stress liners and contact etch stop layers (CESLs). *See*, e.g. Ex. 1007 at 978-980. The combined effect led to substantial improvements in drive current, switching speed, and energy efficiency, supporting continued device scaling and increased integration density.

3. Replacement Metal Gates

43. The gate-first process was the standard approach in early CMOS technology, particularly through the 90 nm (~2003) and 65 nm (~2005) technology nodes. In this method, the gate electrode and dielectric are formed early, enabling self-aligned source and drain formation, which ensures precise alignment and helps minimize parasitic capacitance -- key to enhancing device performance. However, the gate-first approach became problematic with the introduction of high-K (high dielectric constant) materials and metal gates, which replaced traditional poly/SiO₂ stacks to address excessive gate leakage and degraded electrostatic control at smaller nodes.

44. By the 45 nm node (~2007) and beyond, it became clear that high-K/metal gate (HKMG) stacks are thermally sensitive, particularly to the junction activation anneals and SiGe source/drain regrowth processes used to form low-resistance, strain-enhanced regions. These high-temperature steps can degrade the

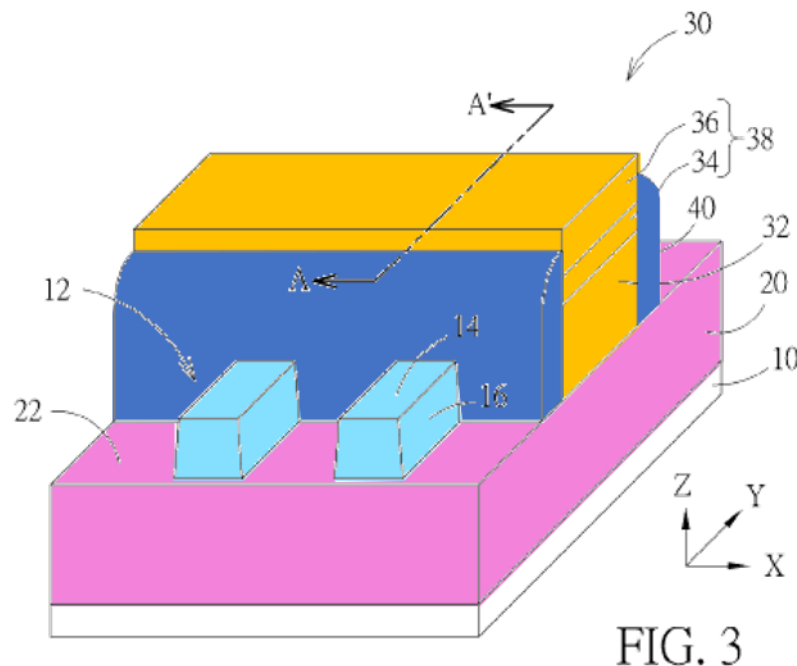
high-K dielectric and alter the metal gate's work function, leading to threshold voltage instability and reduced device reliability. To overcome this, the industry adopted the *gate-last*, or replacement metal gate (RMG), process. *See* e.g., Ex. 1004 at 4:13-17; Ex. 1006 at [0017-0019]. In this approach, a sacrificial polysilicon "dummy" gate is patterned early to preserve self-alignment, while the final high-K dielectric and metal gate stack are introduced after all high-temperature processing is complete. *See* Ex. 1022; Ex. 1023.

45. The gate-last process typically involves depositing the dummy gate, forming sidewall spacers, creating source/drain regions through implantation and activation annealing — or by recessing and regrowing embedded S/D stressors — and then removing the dummy gate to expose the channel. A conformal high-K dielectric (e.g., HfO_2) and a metal gate stack are then deposited into the resulting trench. This method offers two major advantages: (1) enhanced work function tunability, since metals optimized for nMOS and pMOS can be selected post-anneal; and (2) preservation of gate stack integrity, as sensitive materials are never exposed to damaging thermal steps. Even at the most advanced nodes today, the gate-last process remains the industry standard for high-performance 3D nanoscale integrated-circuit devices.

B. The '384 Patent

46. The '384 patent is titled “Semiconductor Device and Fabrication Method Thereof.” It describes a method of fabricating FinFET transistors that include “a fin structure, an isolation structure, a gate structure and an epitaxial structure.” Ex. 1001 at Abst.

47. Figures 1 through 3 of the '384 patent depict the fabrication of a conventional FinFET device, which was known by the priority date. As shown in Figure 3, the FinFET comprises a “a plurality of fin structures 12” (light blue), a “gate structure” 30 (gold) formed over the fins 12, and “a spacer 40” (dark blue) formed “on the sidewalls of the gate structure 30.” *Id.* at 3:20-22, 5:4-8. Figure 3 also depicts “isolation structure 20” (magenta) formed on the substrate 10. *Id.* at 3:60-61.



48. After forming the gate structure 30, “a first etching process 42, such as a wet etching or a dry etching process, may be carried out to selectively remove” the exposed portions of “isolation structure 20,” resulting in the structure shown in Figure 5. *Id.* at 5:26-37. As a result, “[t]here is a height difference H2 between the first top surface 22a [red] and the second top surface 22b [green]” of the isolation structure (magenta) depicted as “D1” in Figure 5. *Id.* at 5:42-48.

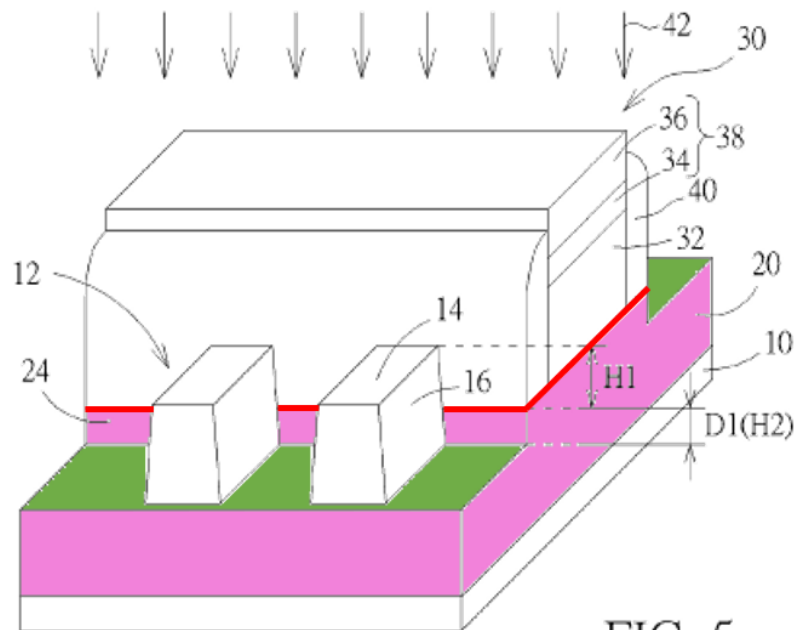


FIG. 5

49. Next, the fin structures 12 are etched and “a recess 60 may be formed in each fin structure 12.” *Id.* at 5:56-60. An “epitaxial growth process” is then “carried out in order to grow an epitaxial structure 60 [*sic.* 66] in each corresponding recess 60.” *Id.* at 6:43-50. The recess is shown below in blue (Figure 6) and the epitaxial structures are shown below in purple (Figure 9). According to the '384 patent, the

recessed fin has a depth that is “deeper” than the depth of the etched isolation structure.

Id. at 6:1-7.

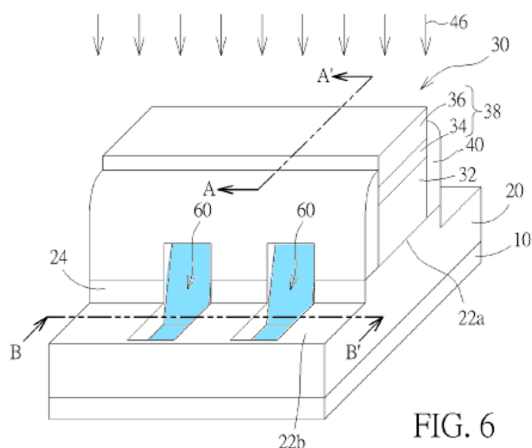


FIG. 6

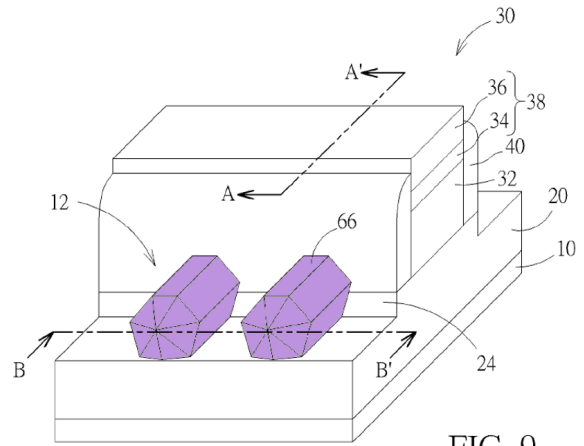


FIG. 9

C. Prosecution History

50. The Challenged Claims were allowed after one non-final rejection. Prior to that rejection, the Examiner imposed a restriction requirement between device and method claims in the pending application. Ex. 1002 at 70. In response, the Applicant elected method claims, originally numbered 11-19. *Id.* at 83.

51. In the next Office Action, the Examiner rejected claims 11-13 and 15-18 as anticipated by U.S. Patent 7,525,160 to Kavalieros et al. (“Kavalieros”, Exhibit 1020). Ex. 1002 at 88. Kavalieros relates to transistors including a stressor material (e.g., SiGe or SiC) in recesses of a fin that provide a stress to the channel region of the device, thereby improving carrier mobility. Ex. 1020 at 2:32-44, 9:17-20. In an embodiment, Kavalieros discloses forming the fin by etching portions of surrounding STI regions, as shown in Figs. 3-4, below:

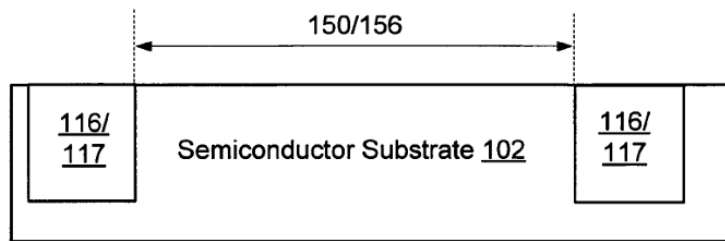


Figure 3

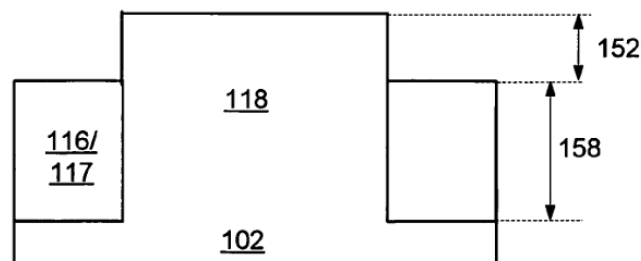


Figure 4

52. In addition, the Examiner rejected claims 14 and 19 (corresponding to current claims 4 and 9) as obvious over Kavalieros and Hsieh. Ex. 1002 at 89. The Examiner explained that while Kavalieros does not disclose a dummy gate process, this is disclosed in Hsieh, and “it would have been obvious to one of ordinary skill in the art to modify Kavalieros et al. as taught by Hsieh et al., because it would eliminate the possibility of damage to the gate during the earlier processing steps.” *Id.*

53. In response, the Applicant amended pending claim 11 (the only independent claim) to recite that the step of etching the isolation structure be performed “after the step of forming the gate structure.” Ex. 1002 at 107. The claims

were subsequently allowed, with the Examiner “agree[ing] with applicant’s arguments, with regard to the amended claim.” *Id.* at 118.

VI. Overview Of The Prior Art

A. Overview of Xu

54. Xu was filed on November 2, 2010 by TSMC. *See* Ex. 1004. Xu qualifies as analogous art because it is in the same field (FinFET technology) and is reasonably pertinent to a problem the ’384 patent purports to address, namely, the fabrication of FinFET devices. *See* Ex. 1001 at Abstr., 3:39-54; Ex. 1004 at Abstr. Xu describes “a FinFET device and method for fabricating a FinFET device.” *Id.* at Abstr. “FIGS. 2-6 provide various perspective views of a FinFET device 100, in portion or entirety, at various stages of fabrication according to the method 10 of FIG. 1.” *Id.* at 2:51-53. “The term FinFET device refers to any fin-based transistor.” *Id.* at 2:53-55.

55. Figure 2 of Xu depicts a “fin structure 115A and 115B [blue] that extends from a substrate 110.” *Id.* at 3:9-12. Figure 2 also shows “[i]solation features 130” that can be “shallow trench isolation (STI) structures” (magenta) that “surround the fin structure 115A and 115B.” *Id.* at 3:54-58. The FinFET device also includes a “gate structure 150” (gold). *Id.* at 3:66-4:3.

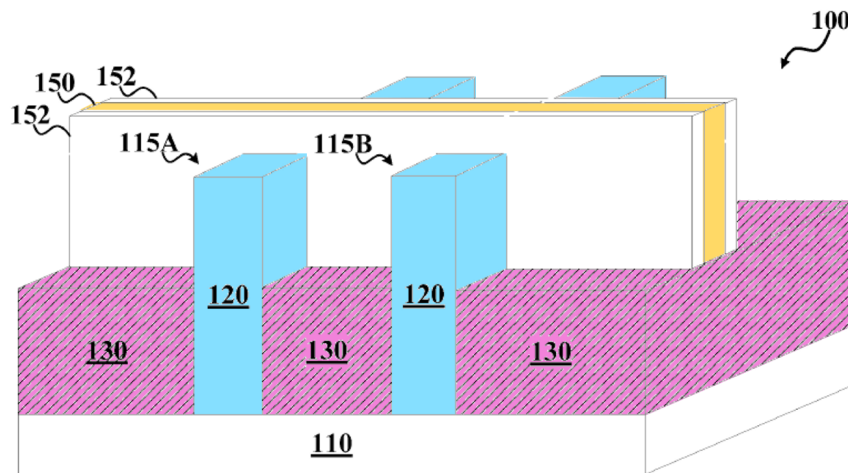


FIG. 2

56. After forming the gate structure, as shown in Figure 3, “a process is performed to recess the isolation features 130” using an “etching process.” *Id.* at 4:54-56. The “etching process selectively etches the isolation features 130.” *Id.* at 4:58-61. The process creates a height difference (or depth) between a top surface (red) under the gate and a top surface (green) to the sides of the gate as shown below.

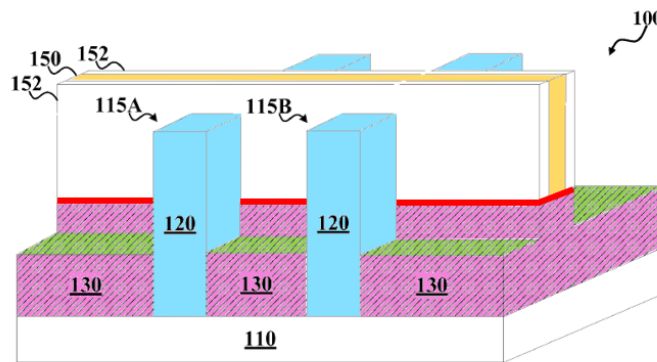


FIG. 3

57. Next, as shown in Figure 4, a “fin template 135” (purple) is formed by “merging the fins 120 together” via “epitaxially (epi) growing a semiconductor

material on exposed portions of the fins 120 in the source and drain regions of the fin structure 115A and 115B.” Ex. 1004 at 5:1-15.

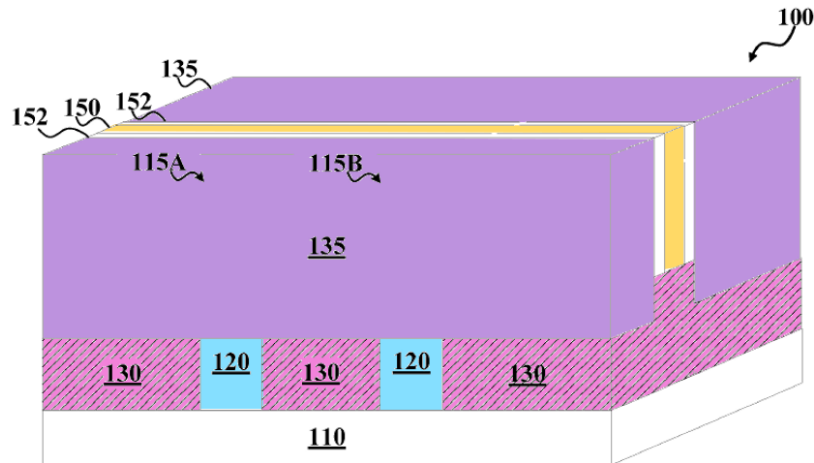


FIG. 4

58. The resulting fin template 135 (purple) and fins 120 (blue) are recessed in Figure 5 and, as shown in Figure 6, another “semiconductor material 160 [purple] is epitaxially grown over the fin template 135,” which “generates channel strain.” *Id.* at 5:34-35, 5:49-55.

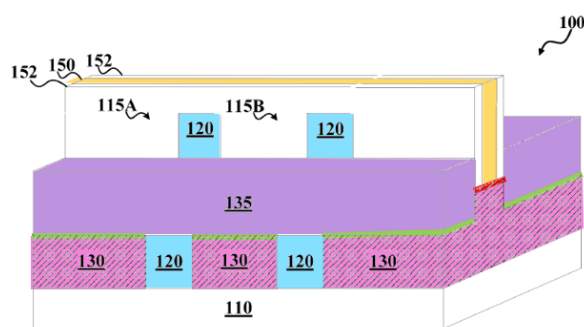


FIG. 5

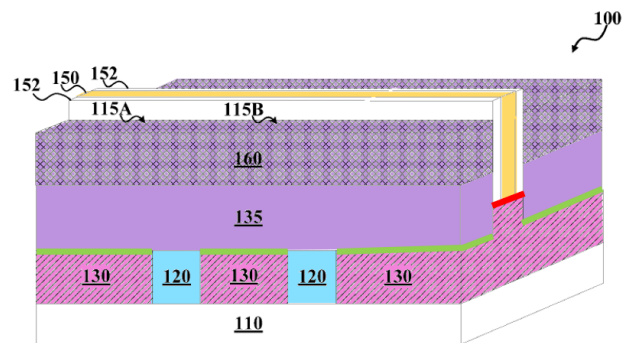


FIG. 6

59. Xu teaches that “[t]he semiconductor material 160 may be referred to as raised source and drain features of the source and drain regions of the fin structure

115A and 115B,” and that the “fin template 135 in the source and drain regions of the fin structures 115A and 115B may also be considered as part of the raised source and drain features.” *Id.* at 6:2-7.

60. Xu also discloses a second embodiment where “an etching process” removes portions “of the fin structures 215A and 215B,” resulting in recessed fins, as shown below. *Id.* at 7:58-61, 10:34-36; Fig. 7 (“[c]ompletely remove the second material portion [230] from the source and drain regions of the first and second fin structure”).

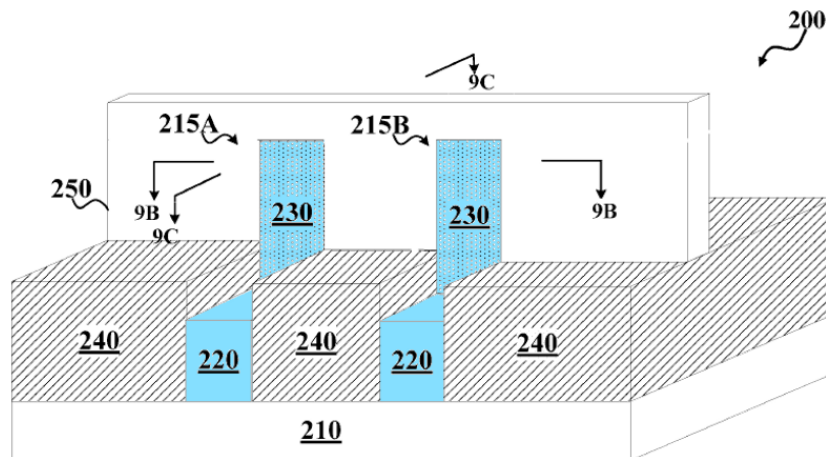


FIG. 9A

61. After that, the epitaxial materials (*i.e.*, the “fin template”) “may be formed by a process similar to that described above with reference to FIG. 5” (*i.e.*, the first embodiment discussed above) to fill the recesses. *Id.* at 11:2-4. Xu contemplates that a fabrication method can include both etching the isolation structure as well as recessing the fin structure. *See, e.g., id.* at 16:5-17:10 and claim 19

B. Overview of Lin

62. Lin was filed on October 13, 2010 by TSMC. Lin describes a “FinFET and Method of Fabricating the Same.” Ex. 1005 at Title. Lin qualifies as analogous art because it is in the same field (FinFET technology) and is reasonably pertinent to a problem the ’384 patent purports to address, namely, the fabrication of FinFET devices. See Ex. 1001 at Abstr., 3:39-54; Ex. 1005 at Abstr., ¶ [0001]. Lin’s Figure 1 show “a method of fabricating a FinFET according to various aspects of the present disclosure.” *Id.* at 3:3-5.

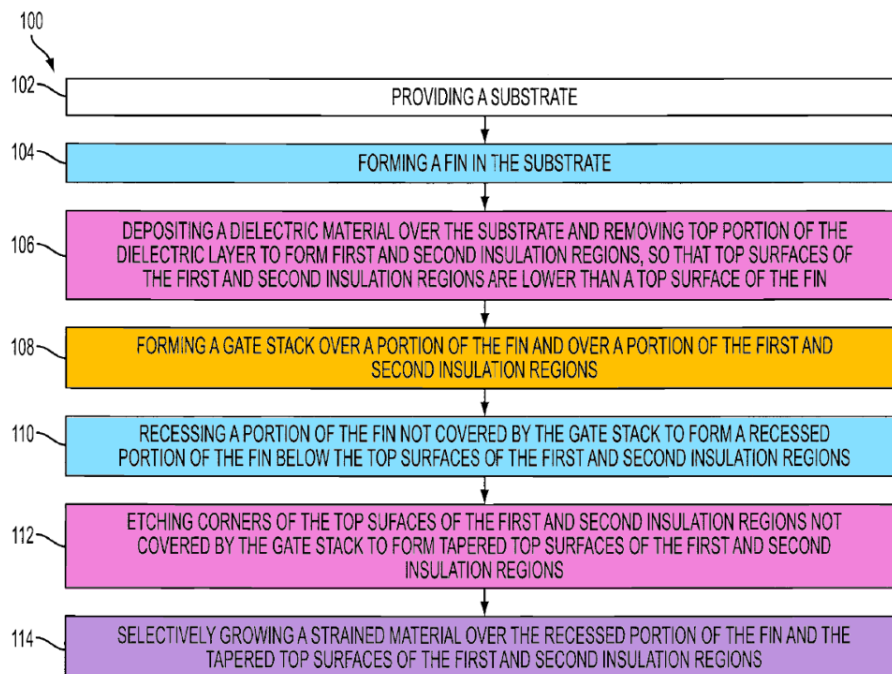


FIG. 1

63. First, “fins [blue] are formed by etching into the substrate 202,” as shown in Figure 3A. *Id.* at ¶¶ [0018]-[0019].

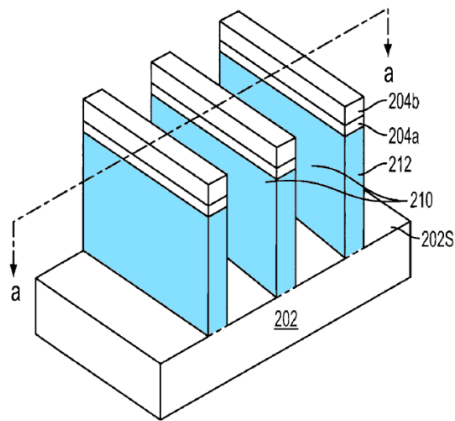


FIG. 3A

64. Next, “[t]renches 210 are filled with a dielectric material 214” as shown in Figure 4A. *Id.* at ¶ [0022]. Subsequently, Lin discloses “recessing of the insulation regions 216 [magenta],” as shown in Figure 6A. *Id.* at ¶ [0023].

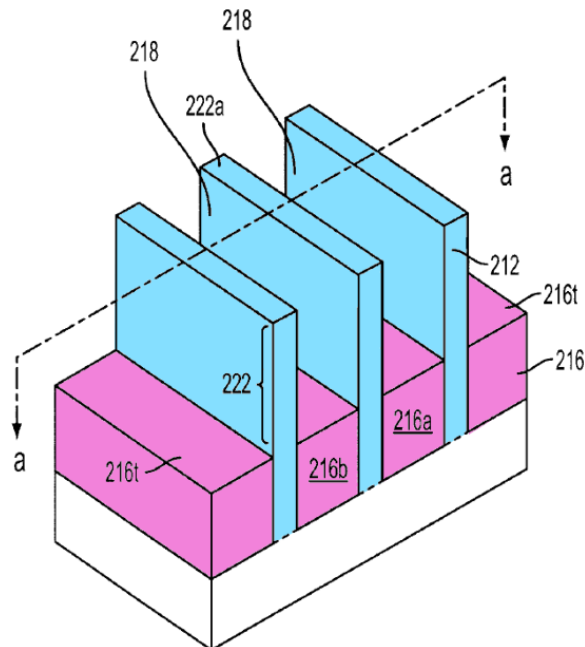


FIG. 6A

65. After that, “[a] gate stack 220 [gold] is formed over the substrate 202 over the top surface 222t and sidewalls 222s of a non-recessed portion of the channel

fin 222a [blue] and extending to the flat top surfaces 216t of the first and second insulation regions [magenta],” as shown in Figure 7A. *Id.* at ¶ [0027].

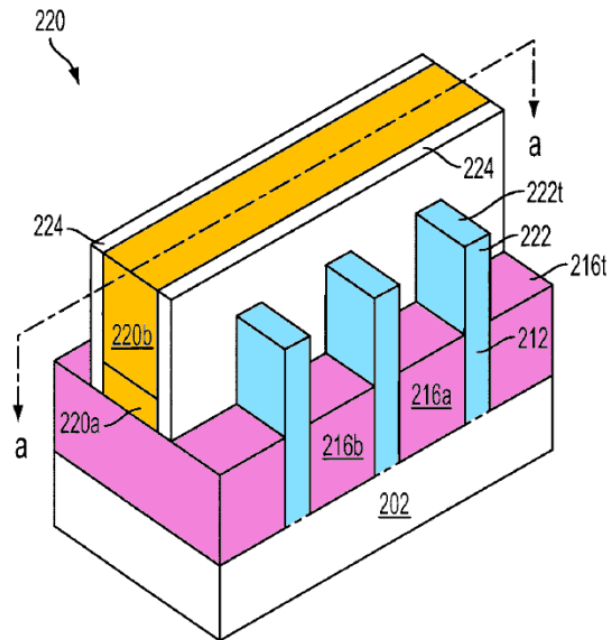


FIG. 7A

66. According to Lin, “[t]he portion of the semiconductor fin 212 [blue] not covered by the gate stack 220 [gold] and spacers 224 formed thereover are recessed to form a recessed portion 226 of the fin 212 [blue]” as shown in Figure 8A. *Id.* at ¶ [0031].

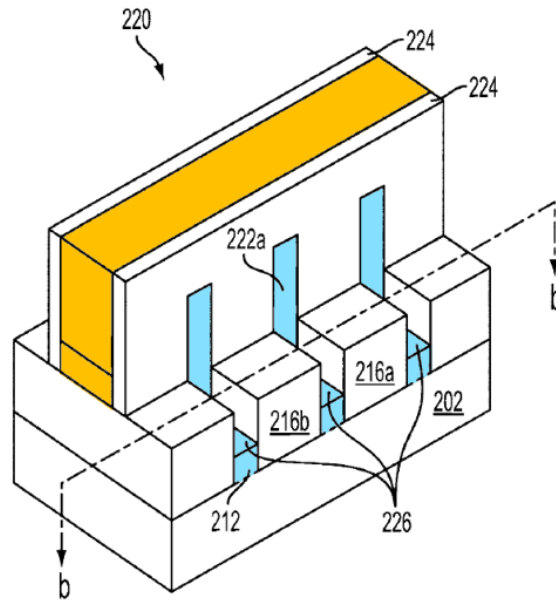


FIG. 8A

67. The isolation structure 216b and 216a are first “etched to form tapered top surfaces 216u” as shown in Figure 9B. *Id.* at ¶ [0032]. In one embodiment, those isolation structures are then further etched so that the “top surface 216u disappear[s] to form a curved top portion” of the isolation structure (magenta), which can be seen in Figure 9C. *Id.* at ¶ [0034].

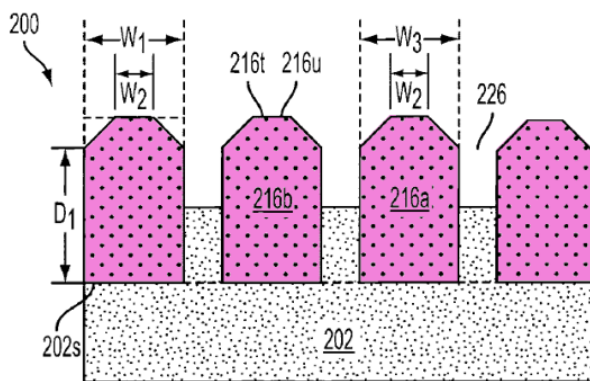


FIG. 9B

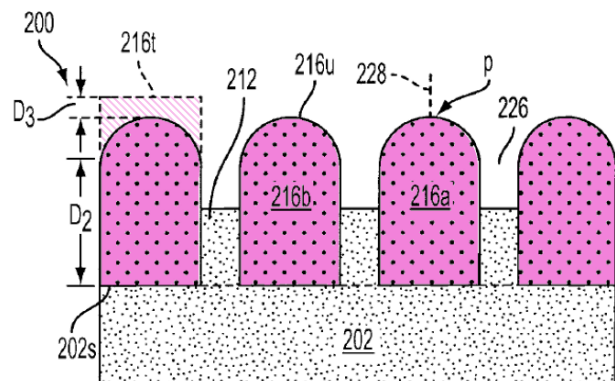


FIG. 9C

68. Finally, a “strained material 230” (purple) is “formed over the structure depicted in FIG. 9C” by “selectively growing a strained material 230 [purple] over the recessed portion 226 of the semiconductor fin 212 and extending over the tapered top surfaces 216u of the first and second insulation regions 216a, 216b [magenta].” *Id.* at ¶ [0035]. The resulting structure is depicted in Figures 10A and 10C.

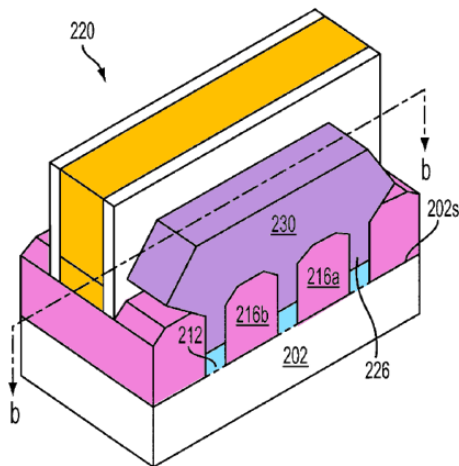


FIG. 10A

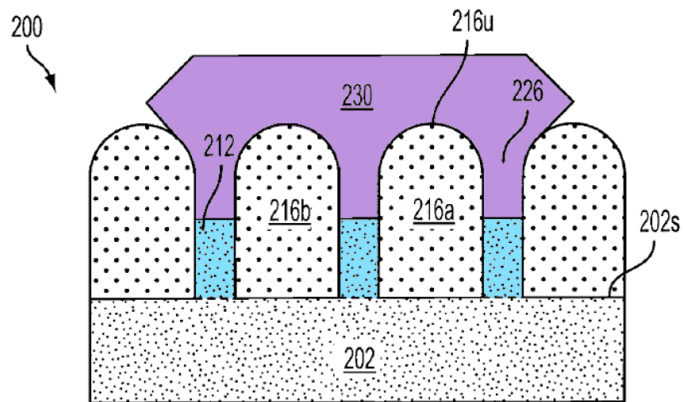


FIG. 10C

C. Overview of Brask

69. Brask is titled “Nonplanar Transistors With Metal Gate Electrodes” and was filed on December 30, 2003 and published on July 7, 2005. *See* Ex. 1006. Brask qualifies as analogous art because it is in the same field (FinFET technology) and is reasonably pertinent to a problem the ’384 patent purports address, namely the fabrication of FinFET devices. *See* Ex. 1001 at Abstr., 3:39-54; Ex. 1006 at ¶¶ [0015]-[0017], [0046]. Brask is directed to “semiconductor integrated circuit manufacture” and in particular, integrated circuits including “nonplanar transistors.” *Id.* at ¶ [0002].

Brask discloses such “nonplanar transistors” include transistors comprising semiconductor fins—*i.e.*, FinFETs. *Id.* at ¶ [0046]. Brask further discloses forming such transistors “utilizing a replacement gate technique.” Ex. 1006 at ¶ [0058]. An example of such a technique is depicted in Figures. 6G-6K of Brask. These figures depict the replacement gate process for an n-type transistor, but Brask also discloses further steps to form a replacement gate for a p-type transistor with respect to Figures 6L-6O.

70. Figure 6G depicts a nonplanar transistor prior to the replacement gate process having source/drain regions 613 of a semiconductor body (*i.e.*, “fin”) (blue) separated by a sacrificial gate 604 (gold). Ex. 1006 at ¶ [0069]. An annealing process is carried out in Figure 6G to activate dopants within the source/drain regions. *Id.* The anneal process causes “dopants placed into the sacrificial gate electrode 604 to move from interstitial sites and substitute with atoms in the lattice of the sacrificial gate electrode 604.” *Id.* Next, in Figure 6H, a dielectric material (green) is “blanket deposited over the substrate” and then “planarized ... until the top surface of the dielectric film is planar with the sacrificial gate electrode.” Ex. 1006 at ¶ [0071].

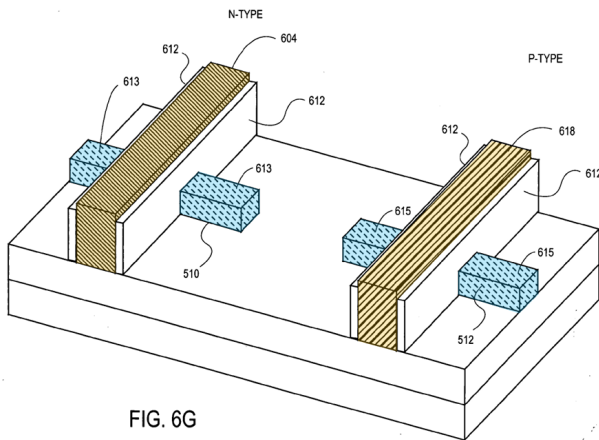


FIG. 6G

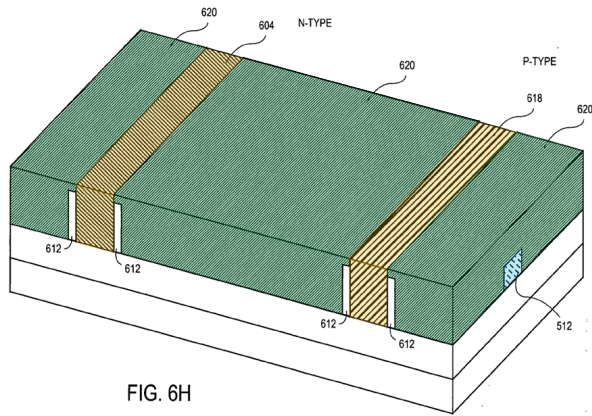


FIG. 6H

71. In Figure 6I, after forming the dielectric layer, the sacrificial gate is removed to form an opening for the gate electrode, exposing a channel of the fin (red).
Ex. 1006 at ¶ [0072].

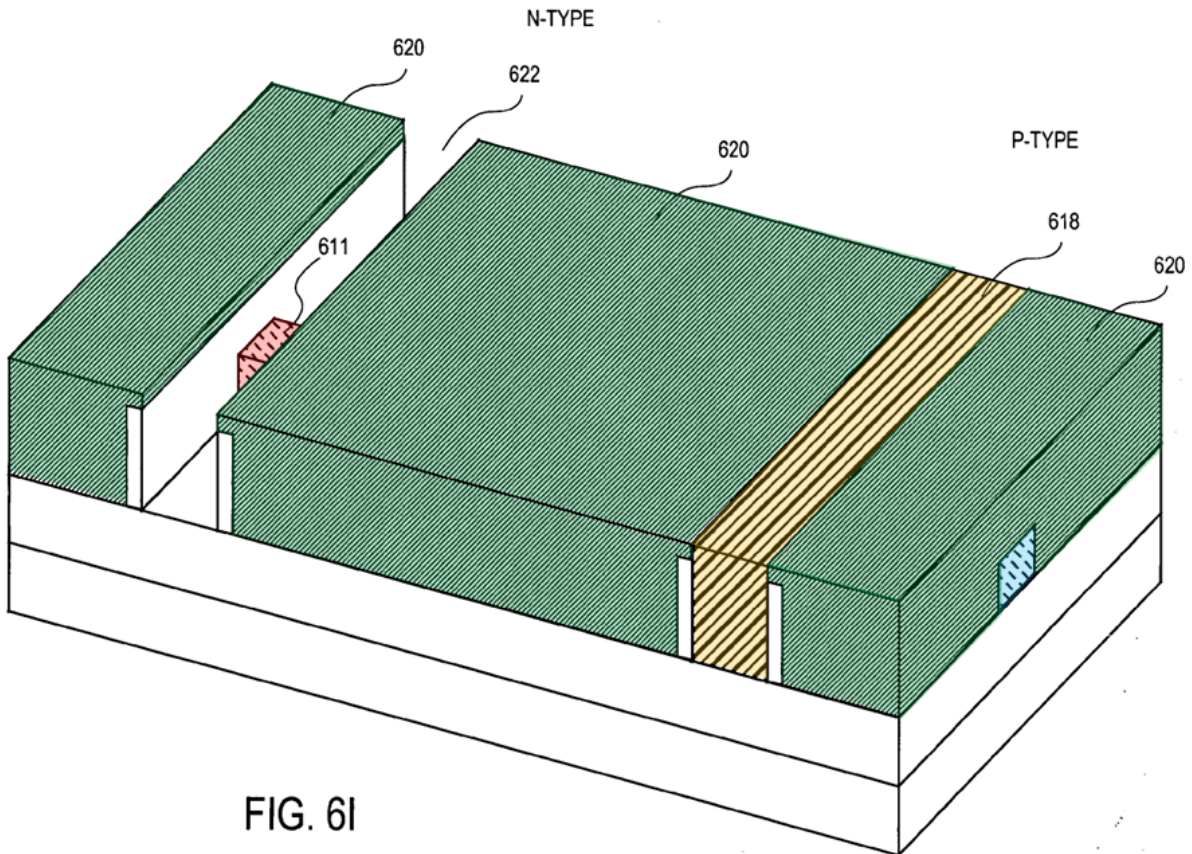
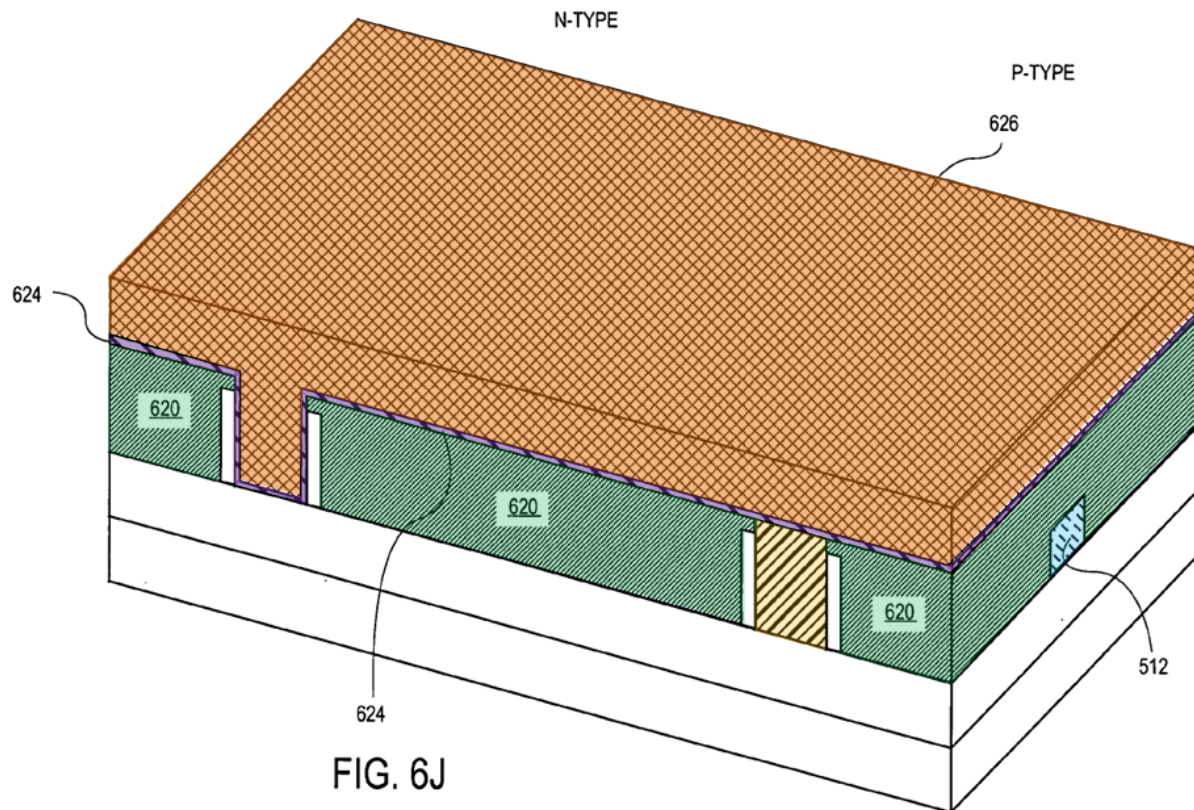
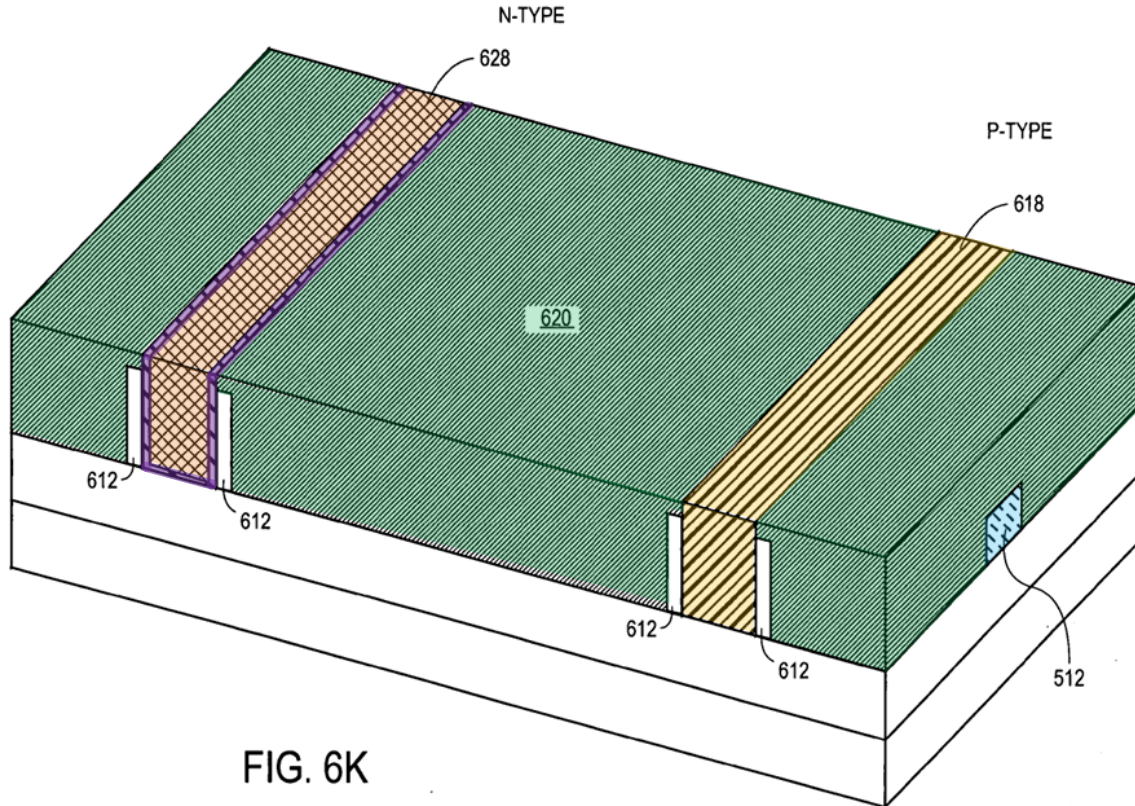


FIG. 6I

72. “Next, the gate dielectric layer [(purple)] and the gate electrode material [(orange)] for the ... device are formed in the openings 622 as shown in FIG. 6.J.” *Id.* at ¶ [0074]. Brask discloses that a “conformal deposition process, such as CVD or ALD is used to deposit a high K gate dielectric layer.” *Id.*



73. The deposited gate dielectric layer and gate electrode material are then polished back or removed resulting in the gate structure shown in Fig. 6K. *Id.*



VII. Ground 1A: Claims 1-9 Would Have Been Obvious Over Xu In View Of The Knowledge Of A POSITA

74. In my opinion, claims 1-9 of the '384 Patent would have been obvious to a POSITA over the teachings of Xu in light of the knowledge of a POSITA.

A. Claim 1

1. 1[pre]: A fabrication method for a semiconductor device:

75. Xu discloses and renders obvious a fabrication method for a semiconductor device. For example, Xu discloses “[a] FinFET device and method for fabricating a FinFET device,” which is a semiconductor device. *See, e.g.*, Ex. 1004

at Abst.; *id.*, 2:51-53 (“FIGS. 2-6 provide various perspective views of a FinFET device 100, in portion or entirety, at various stages of fabrication according to the method 10 of FIG.1.”). Figure 1, reproduced below, depicts a “flow chart of a method for fabricating a fin-like field effect transistor (FinFET) device according to aspects of the present disclosure.” *Id.* at 1:49-51; Fig. 1.

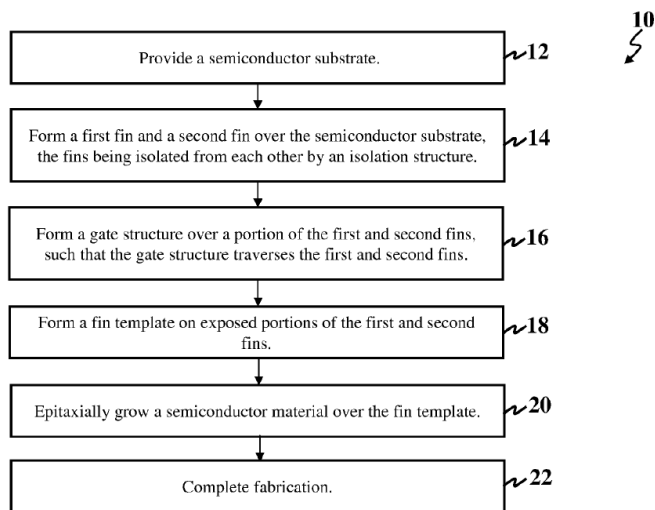


FIG. 1

76. Xu discloses a second fabrication method, illustrated in Figure 7, below, that includes a step 38 of forming a recess in the fin structure. *Id.* at Fig. 7.

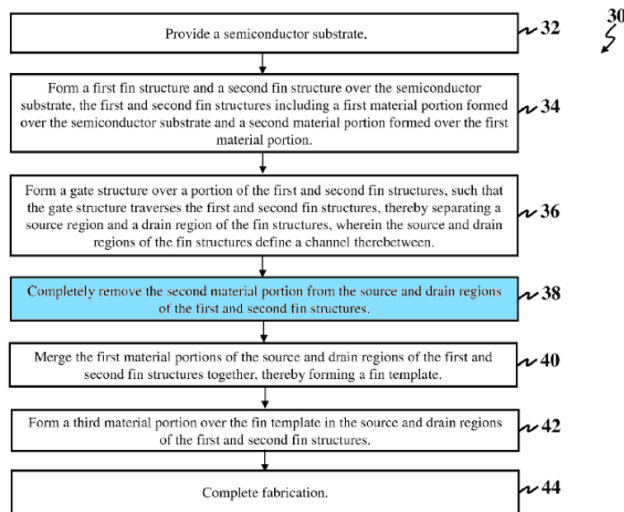


FIG. 7

77. Xu further discloses fabrication methods that incorporate the various steps of Figures 1 and Figures 7 together, including etching the isolation layer and forming recesses in the fin structure, as discussed in greater detail below. *See* Ex. 1004 at 16:5-17:10 and claim 19.

2. 1[a]: forming a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces

78. Xu discloses and renders obvious this limitation. For example, step 14 of Xu's method is "[f]orm[ing] a first fin and a second fin over the semiconductor substrate, the fins being isolated from each other by an isolation structure." Ex. 1004 at Fig. 1.

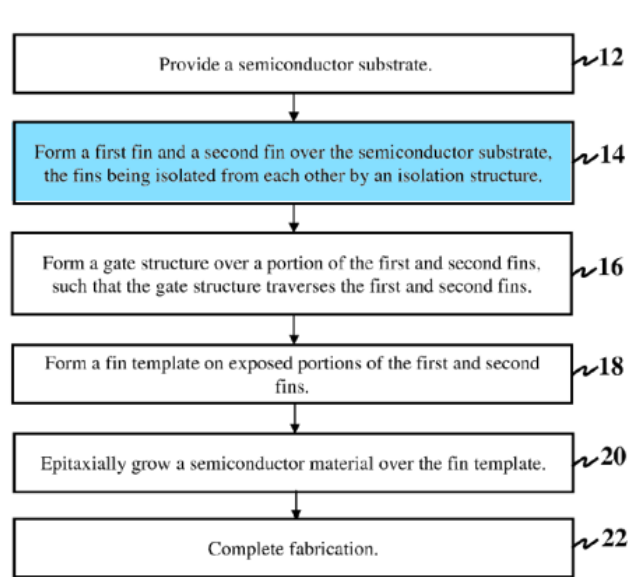


FIG. 1

79. Xu discloses that “FinFET device 100 includes fin structure 115A and 115B that extend from the substrate 110.” *Id.* at 3:9-10. Figure 2, for example, illustrates substrate 110 and fin structures 115A and 115B (annotated in blue) protruding from the top surface of substrate 110 and comprising a top surface and two side surfaces. *Id.* at Fig. 2.

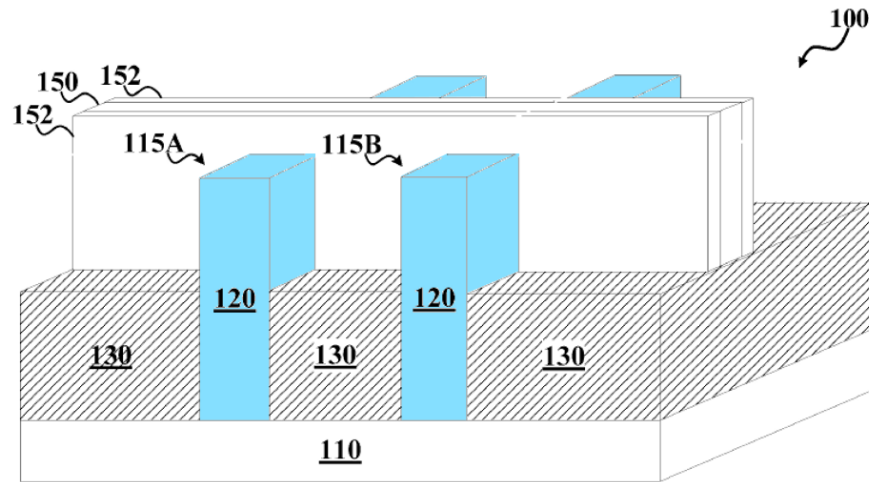


FIG. 2

3. 1[b]: forming an isolation structure to surround the fin structure;

80. Xu discloses and renders obvious this limitation. For example, in step 14 of fabrication method 10, Xu specifies that the formed fins are “isolated from each other by an isolation structure.” Ex. 1004 at Fig. 1. The isolation structure is shown, for example, as isolation features 130 (magenta) in Figure 2 (below) and surround the fins structures 120 (blue). *Id.* at 3:54-58.

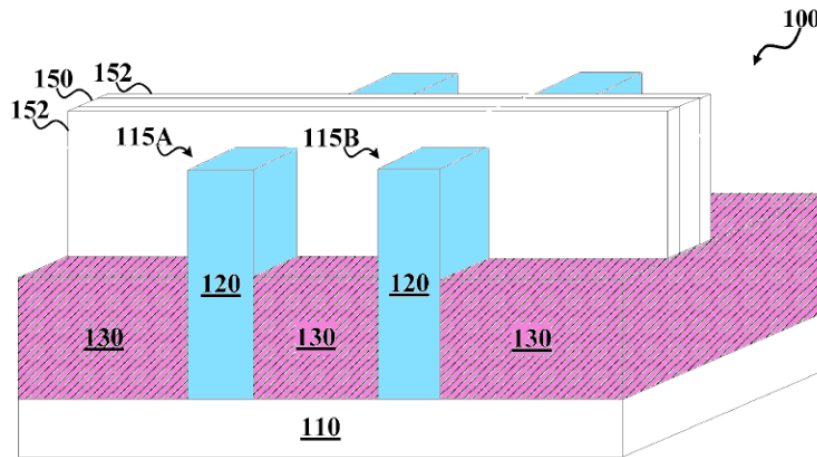
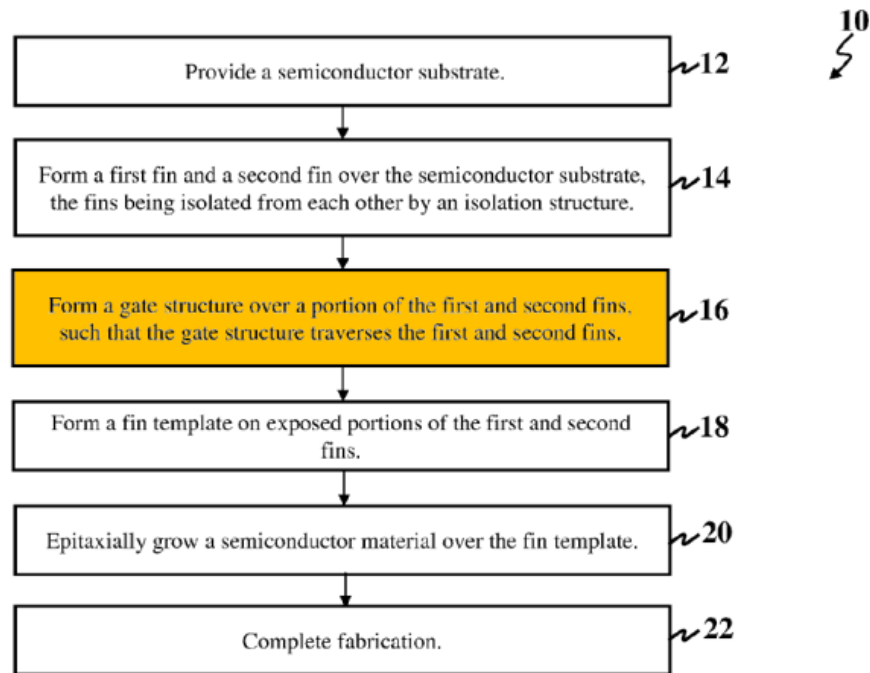


FIG. 2

81. According to Xu, “[i]solation features 130, such as shallow trench isolation (STI) structures, *surround the fin structures* 115A and 115B (in the depicted embodiment, the fins 120), isolating the fins 120 from each other and other not-illustrated integrated circuit devices.” *Id.* at 3:54-58 (emphasis added).

4. **1[c]: forming a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure, and covering a portion of the isolation structure;**

82. Xu discloses and renders obvious this limitation. For example, Step 16 of Xu’s fabrication method 10 includes “[f]orm[ing] a gate structure over a portion of the first and second fins, such that the gate structure traverses the first and second fins.” Ex. 1004 at Fig. 1.



83. Figure 2, for example, illustrates the gate structure 150 (gold) overlaying the top surface and two side surfaces of a portion of fins 120 (blue) and covering a portion of the isolation structure 130 (magenta). *Id.* at Fig. 2; *id.* at 3:66-4:1.

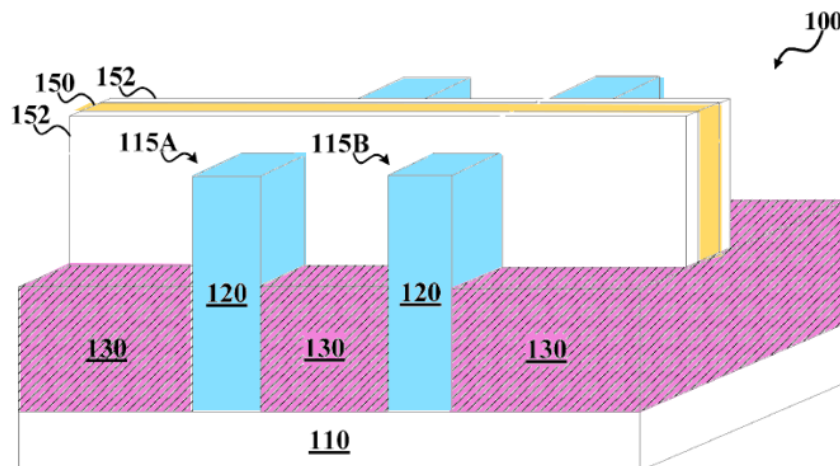


FIG. 2

5. **1[d]: after the step of forming the gate structure, etching the isolation structure exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth;**

84. Xu discloses and renders obvious this limitation. For example, Xu discloses that “an etching process is applied to recess the isolation features 130” and, as shown in Figure 3, the top surface (green) of the isolation structure 130 (magenta) is etched down to a first depth. Ex. 1004 at 4:54-56.

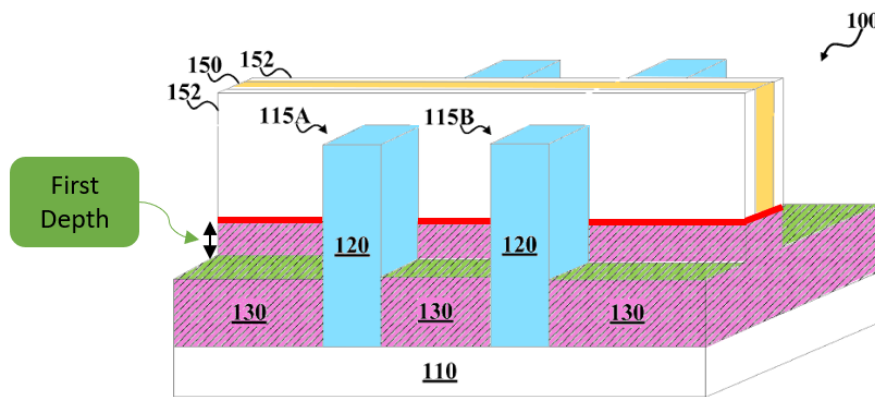


FIG. 3

85. The recessing step is performed after the step of forming the gate structure. Ex. 1004 at Figs. 2-3, 4:39-67. As shown in Figure 2 (below), the gate structure (gold) is first formed over an isolation structure 130 (magenta) that has not yet been etched. In the next step (Figure 3), the isolation structure 130 (magenta) is etched after the gate structure is formed, resulting in the exposed top surface (green) of the isolation structure 130 (magenta) etched down to a first depth.

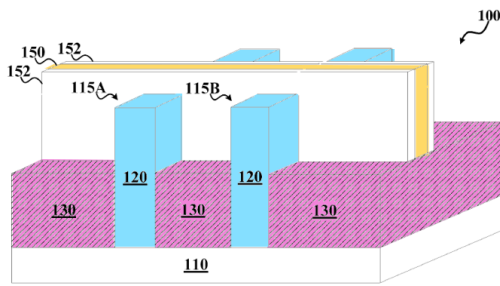


FIG. 2

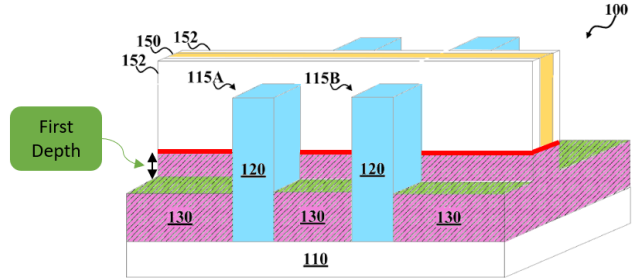


FIG. 3

86. Further, Xu explains that etching of the isolation structure is performed “selectively” so that it “avoid[s] etching the silicon nitride spacers 152.” Ex. 1004 at 4:58-61. Because the spacers are formed after the gate structure is formed (*id.* at 4:39-40), this further confirms that the isolation structures 130 are etched “after the step of forming the gate structure” as claimed.

6. 1[e]: forming a recess in the fin structure at a side of the gate structure; and

87. Xu discloses and renders obvious this limitation. For example, Figure 7 of Xu discloses removing material from a fin structure:

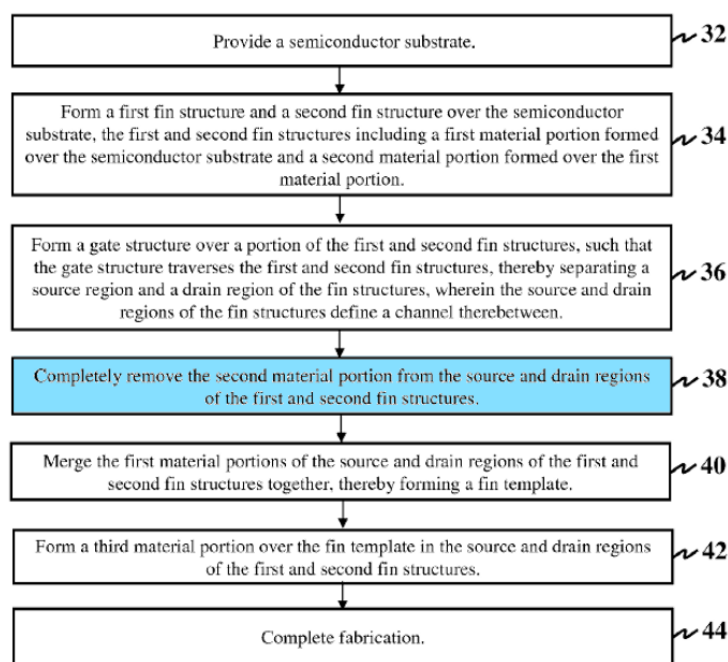


FIG. 7

88. Specifically, Xu discloses a second embodiment of the FinFET device 200 where the “fin structures 215A and 215B” have two portions 220 and 230 (as shown in Figure 8A) and **“an etching process completely removes the fin portions 230 from the source and drain regions** of the fin structures 215A and 215B, exposing the fin portions 220” (as shown in Figure 9A). Ex. 1004 at 7:58-61, 10:34-36; Fig. 7 (“[c]ompletely remove the second material portion [230] from the source and drain regions of the first and second fin structure”). The result of these steps is the creation of a recess in the fin structure at the side of the gate structures as shown in Figures 8A and 9A.

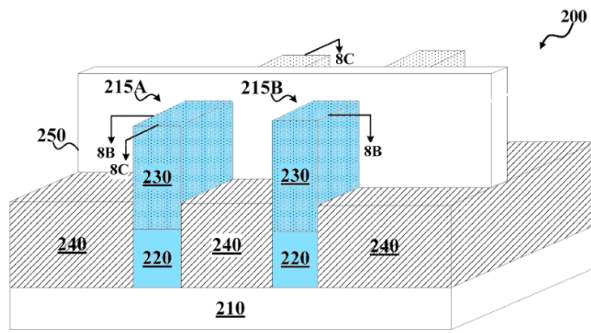


FIG. 8A

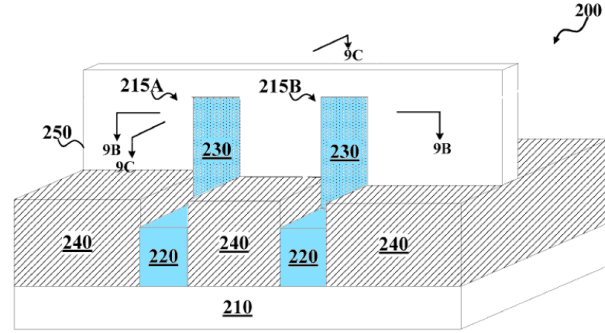


FIG. 9A

This etching process forms recesses in fin structures 215A, 215B at a side of the gate—*i.e.*, either the source or drain region. *Id.* at Fig. 9A.

89. In my opinion, it would have been obvious to a POSITA to combine the fin-recessing step with Xu's first embodiment. As Xu discloses, it was known in the art, and a POSITA would have understood, that "strained source/drain features [] enhance carrier mobility and improve device performance." Ex. 1004 at 1:28-29. Xu explains that forming recesses in the fin structure is beneficial in that it allows for optimization of this strain, specifically noting that "by controlling source and drain trench depth" — which is dictated by the depth of the recess — "strain for both PMOS and NMOS FinFET devices can be achieved and optimized" and "different types of strain can be achieved." Ex. 1004 at 15:56-66. "Accordingly, the trench depth can be tuned to independently optimize performance of each FinFET device in an integrated circuit device." *Id.* at 15:67-16:2. Thus, a POSITA would have understood and found obvious that recessing "fins 120" of Xu's first embodiment will result in "achiev[ing] and optimiz[ing]" strain. *Id.* at 15:56-60, 15:67-16:2. Xu therefore

expressly recognizes an advantage or expected beneficial result that would have motivated a POSITA to combine the recessing of the fins of the second embodiment with Xu's first embodiment.

90. Further, a POSITA would have understood that NMOS devices benefit from tensile strain (*e.g.*, via SiC source/drain regions) and PMOS devices benefit from compressive strain (*e.g.*, via SiGe source/drain regions). *See, e.g.*, Ex. 1004 at 1:16–38; Ex. 1005 at ¶¶ [0002], [0035]. As discussed above, tensile strain enhances electron mobility by reducing effective mass and scattering in the conduction band, while compressive strain improves hole mobility by modifying the valence band structure. Improved mobility directly translates into higher drive current, faster switching speed, and reduced delay, which are critical for achieving high-performance, low-power logic. A POSITA would also have known that strain must be carefully localized in the channel region to be effective, and that epitaxial regrowth of lattice-mismatched materials after selective S/D recessing was an established and effective technique to introduce such localized strain without disrupting overall device geometry or reliability. Tailoring strain for different transistor types (nMOS vs pMOS) using these epitaxial stressors was a well-understood and widely practiced technique, before the filing date of the '384 patent. *See, e.g.*, Ex. 1004 at 1:16–38; Ex. 1005 at [0002], [0035]. A POSITA therefore would have been familiar with the goal of imparting and optimizing strain sought by Xu's recessing process and would have found it obvious

to apply this technique Xu's first embodiment in order to further tailor the strain. In short, Xu's disclosure would have been viewed as compatible with, and motivated by, the well-known design objective of improving channel strain through source/drain engineering.

91. Moreover, starting from 16:5 through 17:10, Xu summarizes the invention in a way that a POSITA would have understood as expressly suggesting the combination of steps from both the first and second embodiments in a single fabrication method. Ex. 1004 at 16:5-44, 16:45-17:10. Xu explicitly states that the "disclosure provides for **many** different embodiments." Ex. 1004 at 16:5-6 (emphasis added). For example, Xu discloses a method (Ex. 1004 at 16:7-26) that may include "etching back the isolation structure" as taught in Xu's first embodiment. Ex. 1004 at 16:17-19. Xu then presents alternative modifications to this method. *Id.* at 16:27-44. Specifically, Xu discloses "[t]he method may include completely removing the second material portion from the source and drain regions of the fins before forming the fin template." *Id.* at 16:40-43. These techniques correspond to the fin-recessing steps described in Xu's second embodiment, as shown in Figures 7, 8A and 9A. Ex. 1004 at 16:45-17:10 (describing "another embodiment" that may include "etching back the isolation structure" and "removing a portion of the first and second fin structures before epitaxially growing the first semiconductor material" which may include "completely removing the second

material portion”). In my opinion, Xu’s express disclosure of using these steps together clearly suggests and renders obvious the combination of the first and second embodiments. A POSITA reading Xu’s disclosures of the first embodiment and second embodiment would not have had to consult other references, perform additional research or conduct further experimentation to arrive at this combined approach and to become appraised of all elements of the combination *and* an explanation of the potential advantages of including the fin recessing step. Rather, Xu’s own summary of the invention provides a direct rationale and support for combining the disclosed etch-back and fin-recess steps into a unified process, rendering such a combination obvious. In my opinion, it would have been readily apparent and obvious to a POSITA to combine the teachings of both embodiments from these disclosures in a single reference. This is especially true given that Xu itself suggests such a combination when summarizing the invention.

92. Additionally, it is my opinion that a POSITA would have had a reasonable expectation of success in making this combination. Xu discloses exemplary etch processes which can be used to perform the step of recessing the fin. Ex. 1004 at 10:36-61; 13:44-55. A POSITA would have understood these to be conventional, well-controlled etching techniques, readily applicable to the fin structures of Xu’s first embodiment for precisely controlling the recess depth.

93. In particular, a POSITA would not view the etch-back of the STI in Xu's first embodiment as a technical barrier to implementing an optimized fin recess. These two steps, STI recessing and fin recessing, are independent and separable, and can be performed using known anisotropic etching techniques, including those explicitly disclosed in Xu, which teach etch selectivity and depth control. Ex. 1004 at 10:27-62.

94. In my opinion, the combination of Xu's first and second embodiments is merely the application of a known technique to a known method that is ready for improvement. Specifically, Xu's first embodiment is a well-known conventional method for fabricating FinFET devices. The recessing of the fins of Xu's second embodiment is also a known technique, and one that may be applied to the first embodiment. A POSITA would have recognized that applying the recessing of the fins to the first embodiment would have yielded predictable results in enhanced channel strain, consistent with Xu's own teaching of "provid[ing] different starting substrates for forming the fin templates, such that different types of strain can be achieved." Ex. 1004 at 15:64-16:2.

95. Finally, I note that Claim 19 of Xu, which depends from independent claim 11, further reinforces the obviousness of such a combination. Like the summary portions of the specification described above, Claim 19 sets forth a method that combines steps of the first embodiment with steps of the second embodiment.

Specifically, claim 19 combines “recessing the isolation structure by removing a portion of the isolation structure”—as disclosed in the first embodiment—with the step of removing materials from the source and drain regions of the fins to form recesses in the fin structures—as described in the second embodiment. Ex. 1004 at Claim 19. That Xu claims these steps together demonstrates that a POSITA would have found it obvious to combine the first embodiment with the fin-recessing of the second embodiment to arrive at the claimed method. A POSITA reading claim 19 could have easily contemplated such a combination would have had a reasonable expectation of success in making it using conventional fabrication tools and known process flows.

7. 1[f]: forming an epitaxial layer to fill up the recess,

96. Xu discloses and renders obvious this limitation. As discussed above, a POSITA would have been motivated to combine Xu’s first embodiment with the technique for recessing the “fins 120.” *See supra* 1[e]. A POSITA would have been further motivated to form an epitaxial layer to fill up the recess when recessed fins of the second embodiment are combined with the first embodiment. For example, Xu notes that after the fins are recessed, fin template 280 “may be formed by a process similar to that described above with reference to FIG. 5” of Xu’s first embodiment. Ex. 1004 at 11:2-4. In other words, after recessing the fins of Xu’s first embodiment,

Xu expressly recognizes that the same epitaxial growth process of the first embodiment is used to fill the recess with the “fin template” (purple). *Id.*; Ex. 1004.

97. As shown in Figure 10A, this epitaxially-grown layer 280 (purple) fills the recesses above fins 220 in the second embodiment where recesses are formed in the fins. Ex. 1004 at Fig. 10A.

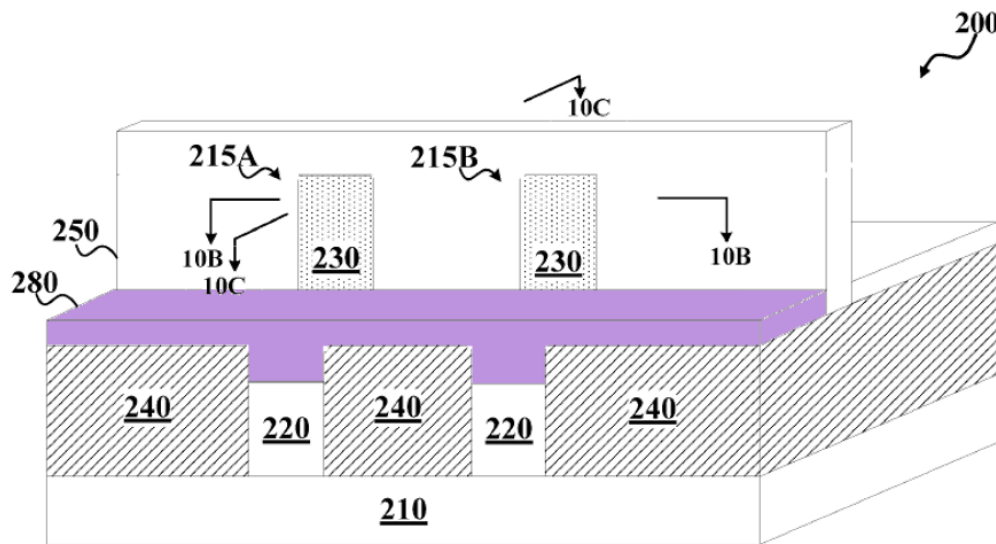


FIG. 10A

98. Figure 5 illustrates the corresponding epitaxial structure 135 for the first embodiment without a recess in the fin structure above fins 120. Ex. 1004 at Fig. 5.

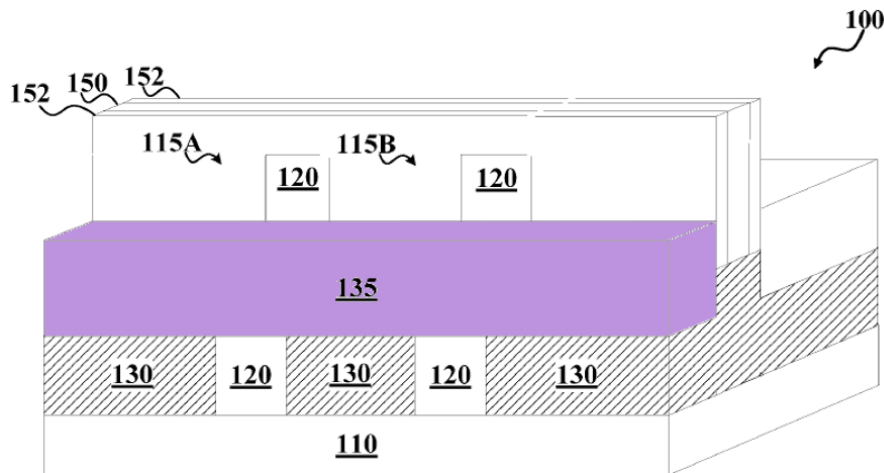
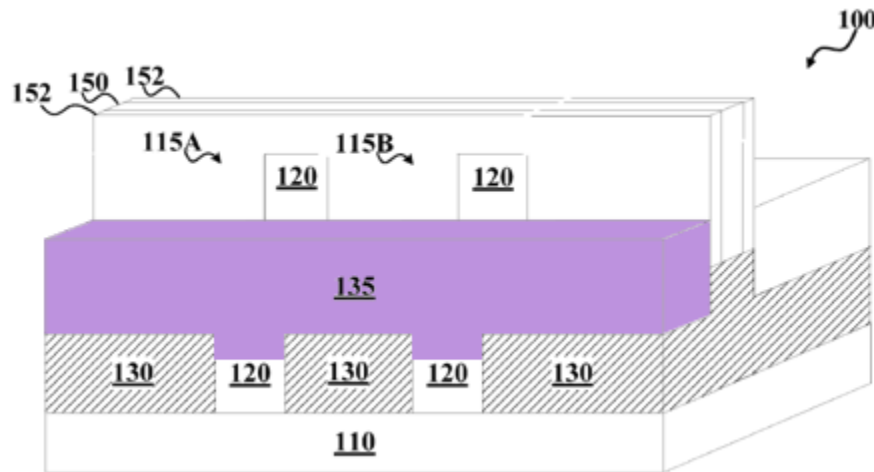


FIG. 5

99. Thus, when the fin-recesses of the second embodiment are formed in the first embodiment, a POSITA would have understood and found it obvious that an epitaxial layer (purple) will “fill the recesses” because Xu teaches that, in both embodiments, the epitaxial layer is formed on the “exposed portions of the fins 120.” Ex. 1004 at 5:1-2 (first embodiment); 11:4-8 (second embodiment). This is shown in the modified figure below, showing the combination of the second embodiment’s recesses with the first embodiment:



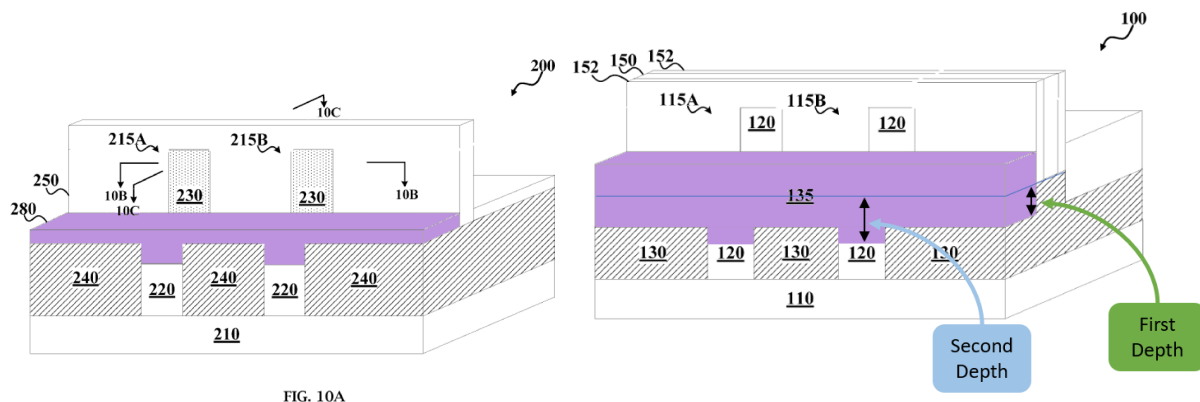
100. As discussed, fin template 280 of the second embodiment “may be formed by a process similar to that described above with reference to FIG. 5” of Xu’s first embodiment. Ex. 1004 at 11:2-4. Thus, fin template 135/280 is an epitaxial layer because it is formed by “epitaxially (epi) growing a semiconductor material on exposed portions of the fins 120 in the source and drain regions of the fin structures 115A and 115B.” *Id.* at 5:4-8. The fin template 135 “could be silicon germanium (SiGe) formed by a silicon germanium epitaxial deposition process.” *Id.* at 5:18-20.

8. 1[g]: wherein a bottom surface of the recess has a second depth, and the second depth is deeper than the first depth.

101. Xu discloses and renders obvious this limitation. For example, when recessed fins of the second embodiment are applied to the first embodiment of Xu as discussed above, the recesses form “trenches” that “extend[]” to an “exposed surface of the fin portion 220.” Ex. 1004 at 10:50-57. The bottoms of these trenches define the claimed “second depth” which extends to the recessed surface of the fin.

102. The “trench sidewalls” are defined by the “isolation features” (Ex. 1004 at 10:52-54), the top surfaces of which were previously etched to the claimed “first depth.” *See supra cl. 1[d]*. Because the top surfaces of the isolation features define the “first depth” and the bottom of the trench defines the “second depth,” the second depth is necessarily “deeper than the first depth” as claimed.

103. Figure 10A depicts the second embodiment of Xu, which shows the “second depth.” Ex. 1004 at Fig. 10A. Because the isolation structure is not shown to be etched, Figure 10A does not depict the “first depth.” A POSITA, however, would have understood that combining the recessed fins 220 of the second embodiment with the first embodiment’s etched isolation structures (as shown in modified version of Figure 5 below), results in a structure where the second depth is deeper than the first depth.⁵



⁵ For visual comparison, the annotated figure extends with a blue line the plane of the top surface of the isolation structure below the gate, which serves as reference points for the first and second depths.

104. Therefore, in the combined device, where the isolation structure has been etched to a first depth, the bottom of the trench has a second depth that is deeper than the “first depth” because the “first depth” terminates at the top surface of the adjacent isolation structures whose sidewalls form the trench.

B. Claim 2: The fabrication method according to claim 1, wherein the isolation structure is a shallow trench isolation structure.

105. As discussed above, Xu discloses and renders obvious the fabrication method according to claim 1. Xu further discloses and renders obvious the additional limitation of claim 2. For example, Xu discloses that isolation features 130 can be “shallow trench isolation (STI) structures, surround[ing] the fin structures 115A and 115B.” Ex. 1004 at 3:54-58; *see also id.* at 9:30-33 (same for isolation features 240 in second embodiment).

C. Claim 3: The fabrication method according to claim 1, wherein a step for etching the isolation structure comprises wet etching or dry etching.

106. As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 3. For example, Xu discloses that “an etching process is applied to recess the isolation features 130” and that the etching can be “a dry etching process, wet etching process, other etching process, or combinations thereof.” Ex. 1004 at 4:55-58.

D. Claim 4: The fabrication method according to claim 1, wherein the gate structure is a dummy gate structure.

107. As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 4. For example, Xu discloses that the gate structure 150 may be formed in a “gate last process.” Ex. 1004 at 4:13-14. A POSITA would have understood and found it obvious that a gate last process comprises forming a dummy gate structure as the “gate structure.”

108. The use of dummy gates in gate last processing was well-known by 2013. For example, a POSITA would have understood that by 2013, there was “a shift from ‘gate first’ to ‘gate last’ processing.” Ex. 1008 at 16. In gate-last processing, a “dummy gate” is the first gate structure that is formed. *Id.* Subsequently, it is “removed after source/drain silicidation and replaced by the final gate stack.” *Id.* A gate-last process has the advantage that the “final metal gate is not exposed to the high activation anneal for the junctions.” *Id.* “As a result, a better controlled work function for nMOS and pMOS can be achieved.” *Id.*

109. The '384 patent admits that, a gate-last process, forming dummy gates first was well-known to a POSITA by the time it was filed. Ex. 1001 at 7:21-27. For example, the '384 patent describes a “high-k last replacement metal gate (RMG) process” that involves first forming a dummy gate and then “removing the [dummy]

gate structure to leave a trench.” Ex. 1001 at 7:21-27. This “RMG process . . . [is] well-known to those skilled in the art” and therefore the ’384 patent “omitted” a detailed description of it. *Id.* at 7:31-34. A POSITA would have understood and found obvious that “gate-last” and “replacement metal gate” refer to the same process, where the final metal gate structures are formed last and replace dummy gates. Indeed, skilled artisans used “gate-last” and “RMG” interchangeably during the relevant timeframe. *See* Ex. 1009 at 34 (“[T]wo main approaches being followed for metal gate integration: gate-first (GF) and gate-last (**GL=RMG**).”)

110. Thus, a POSITA would have understood and found obvious that in the gate-last process in Xu, a dummy gate structure is formed at the step 16 of forming the gate structure in the Figure 1 fabrication method. The rest of the fabrication would be the same, with additional unclaimed steps at the end of the method for removing the dummy gate and forming the replacement metal gate.

E. Claim 5: The fabrication method according to claim 1, wherein a step for forming the recess comprises wet etching or dry etching.

111. As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 5. For example, Xu discloses that the etching process that removes the fin portions 230 to form the claimed recess can be “a dry etching process, [or] wet etching process . . .” Ex. 1004 at 10:34-38; see also *supra* discussion of claim limitation 1[e].

F. Claim 6: The fabrication method according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

112. As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 6. For example, Xu discloses that the fin template 135 (an epitaxial structure as shown above for limitation 1.f), “could be silicon germanium (SiGe) formed by a silicon germanium epitaxial deposition process.” Ex. 1004 at 5:18-20; *see also* Xu at 11:14-16 (same for fin template 280 in the second embodiment).

113. Xu also discloses that the fin template could be silicon phosphide. Specifically, “the epi silicon fin template 135 may be doped with phosphorous (to form a Si:P epi layer). The doped epitaxial layer may have a gradient doping profile.” Ex. 1004 at 5:23-25. A POSITA would have understood this disclosure, and specifically “Si:P”, to mean the epitaxial structure 135 can be silicon phosphide.

G. Claim 7: The fabrication method according to claim 1, further comprising forming a spacer before etching the isolation structure, wherein the spacer is disposed on a sidewall of the gate structure.

114. As described above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 7. For example, Xu discloses “spacers 152 are disposed on the sidewalls of the gate structure 150, such as along the gate electrode.” Ex. 1004 at 4:39-40. And Figure 2 shows the spacers 152 (blue) formed on the sidewalls of the gate structure

150 before etching the isolation structure 130 as shown in Figure 3. *Id.* at Figs. 2, 3. Although the figures for Xu's second embodiment do not show the spacers, Xu discloses that they exist in the same manner as Figure 2. *Id.* at 10:11-14.

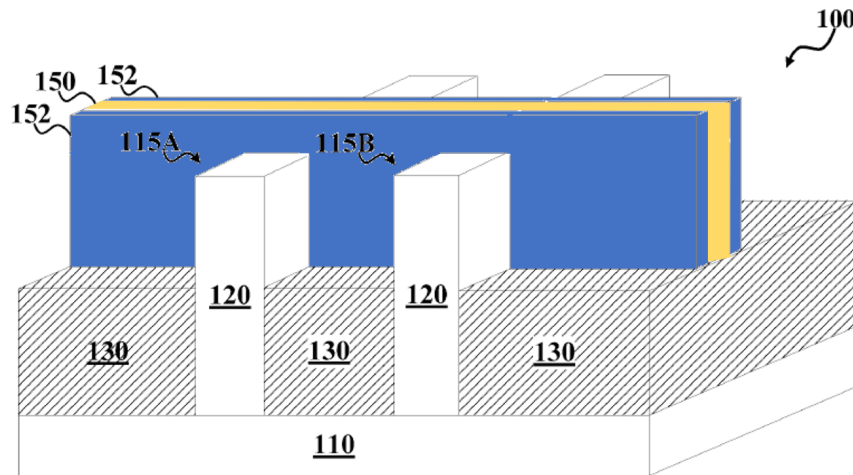


FIG. 2

H. Claim 8: The fabrication method according to claim 7, wherein a step for forming the spacer comprises: depositing a material layer to conformally cover the gate structure and the fin structure, and etching the material layer until the isolation structure is exposed.

115. As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu further discloses and renders obvious the additional limitation of claim 8. For example, Xu discloses that “spacers 152 may be formed by depositing a silicon nitride layer.” Ex. 1004 at 4:46-49.

116. A POSITA would have understood and found it obvious that the deposited silicon nitride layer would conformally cover the gate structure and the fin structure as recited in claim 8. By 2013, materials such as silicon nitride were

typically deposited using conformal deposition techniques like LPCVD (low-pressure chemical vapor deposition) or PECVD (plasma-enhanced CVD). *See* Ex. 1025 at 270, (“... some of the most widely-used films deposited by CVD (including ... silicon-nitride ...”), 296 (describing LPCVD and PEVD as common techniques for depositing SiN). These techniques were well known to provide uniform, conformal coverage over complex topographies (*see id.* at 298 (noting “conformal” step coverage for PECVD of silicon nitride films)), which would include the vertical sidewalls of the gate and fins, as well as horizontal surfaces in the context of Xu. Specifically, as Ex. 1025 explains that when used as a sidewall spacer, silicon nitride acts as a passivation structure and “[w]hen used a passivation-layer ... PECVD is the deposition method of choice” for silicon nitride. Ex. 1025 at 297. Thus, a POSITA would have understood that depositing silicon nitride via PECVD results in conformal step coverage that conformally coats all exposed surfaces uniformly. *Id.* at 298 (Table 16-2 showing conformal step coverage for PECVD of silicon nitride).

117. Here, Xu explicitly states that “spacers 152 may be formed by depositing a silicon nitride layer” (Ex. 1004 at 4:46–49), and spacers by definition must extend along the sidewalls of the gate. Further, in Xu, the gate structure 150 and fin structure 115A/115B are formed before the spacers and therefore exposed at this point of the fabrication method. Given that the fins and gate structure are both present and exposed prior to this deposition, a POSITA would have understood that the deposited SiN layer

conformally coats these structures before being anisotropically etched to form spacers along the gate sidewalls and above the fins.

118. Even if it were argued that Xu's deposition of the silicon nitride spacer material is non-conformal, it would have been obvious to a POSITA to substitute a conformal deposition process, based on their general knowledge of these well-established fabrication processing techniques. In such a case, the only difference between Xu and the claim limitation would be the use of a non-conformal versus a conformal deposition process. By 2013, a POSITA would have understood that both conformal, e.g. PECVD and LPCVD, and non-conformal depositions, e.g. sputtering, were known in the art and their functions were well understood. Further, a POSITA could have substituted a conformal process into the method of Xu, yielding the predictable results of conformal deposition described above such as a uniform coating over all exposed topographies. Accordingly, it would have been an obvious and routine substitution to use a conformal deposition method in Xu's process to meet the limitation of claim 8.

119. Further, Xu discloses that the silicon nitride layer is dry etched to form the spacers as illustrated in Figure 2, above. Ex. 1004 at 4:46-49. A POSITA would have understood and found obvious that this etching constitutes etching the material layer until the isolation structure is exposed. For example, Figure 2 illustrates that the isolation layer is exposed after formation of the spacers 152. Ex. 1004 at Fig. 2.

Additionally, spacers were well-known in the art and were used to isolate the gate structure from the source/drain regions of a transistor. Thus, the function of the well-known spacers dictates that it is disposed on the sidewalls of the gate structure and therefore would be removed from other features like the isolation structures.

I. Claim 9

1. 9[pre]: The fabrication method according to claim 1, further comprising:

120. As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu also renders obvious claim 9 in view of the knowledge of a POSITA, as detailed below.

2. 9[a]: depositing an interlayer dielectric to surround the gate structure;

121. Xu discloses and renders obvious this limitation. For example, As detailed above for claim 4, a POSITA would have understood and found obvious that Xu's disclosure of a "gate-last" process (Ex. 1004 at 4:13-14) refers to the "well-known" replacement metal gate (or "RMG process"). *See supra* cl. 4; *see also* Ex. 1001 at 7:31-34. A POSITA would have understood that Xu's gate-last process includes depositing an interlayer dielectric to surround the gate structure, as evidenced at least by the '384 patent's admissions.

122. Specifically, the '384 Patent expressly admits that "the RMG process" was "well-known to those skilled in the art" at the time of filing. Ex. 1001 at 7:31-

34. I understand that this renders the “RMG process” as “applicant admitted prior art.” I understand that applicant admitted prior art may be used to evidence the knowledge of a POSITA at the relevant time. In my opinion RMG processing was well-known before the filing date of the ’384 patent, and a POSITA would have understood the applicant admitted prior art disclosures of the ’384 patent to be describing this well-known process.

123. In particular, a POSITA would have understood that Xu’s “gate-last process” is the applicant admitted prior art “RMG process,” which a POSITA would have understood to include “depositing an interlayer dielectric *to surround the gate structure*.” Ex. 1001 at 7:24-34.

124. Further, Xu expressly recognizes that the FinFET device 100 “may include additional features,” such as “*interlayer-dielectrics*” that are formed “over the substrate 110.” Ex. 1004 at 6:44-53. A POSITA would have understood that this dielectric layer refers to an interlayer dielectric (ILD), which is a standard insulating material used to electrically isolate conducting and semiconductor features and films in transistors. Ex. 1011 at v. *See also* Ex. 1010⁶ at 27 (describing materials “traditionally” used as ILDs). ILDs and their use in transistor devices were well-known to those skilled in the art before 2013. As described in Ex. 1011 (Muraka),

⁶ https://web.archive.org/web/20070928192450/http://smtbook.com/instructor_guide.pdf.

ILDs are typically silicon dioxide (doped or undoped), silicon nitride, or low-k dielectrics deposited using processes such as plasma-enhanced chemical vapor deposition (PECVD), low-pressure CVD or spin-on techniques. These layers are designed to surround and separate electrically conductive structures while enabling subsequent contact formation and interconnect routing. *See* Ex. 1011 at Chapter 1. In Xu, the dielectric layer surrounding the gate structure serves exactly this purpose: it isolates the gate electrode from other components in the vertical stack and facilitates the subsequent formation of vias and metallization. Because this layer is deposited after gate formation and encapsulates the gate region, a POSITA would have readily recognized it as an interlayer dielectric as recited in claim 9[a]. A POSITA also would have understood and found obvious that to isolate the “electrically conducting” gate, the interlayer dielectric would be deposited to surround the gate structure of Xu.

3. 9[b]: removing the gate structure to leave a trench;

125. Xu discloses and renders obvious this limitation. For example, a POSITA would have understood that Xu’s “gate-last process” is the applicant admitted prior art “RMG process,” which a POSITA would have understood includes “removing the gate structure to leave a trench.” Ex. 1001 at 7:24-34.

126. Moreover, as discussed above for claim 4, a POSITA would have understood and found obvious that the “gate last process” of Xu uses a dummy gate as the initial gate structure, which is subsequently removed. Ex. 1008 at 16 (in a gate-

last process “a dummy gate is patterned” and later “removed after source/drain silicidation and replaced by the final gate stack.”). A POSITA would further have understood that removing the gate structure 152 (gold) of Xu would leave a trench between the spacers 152. *See* Ex. 1004 at Fig. 2.

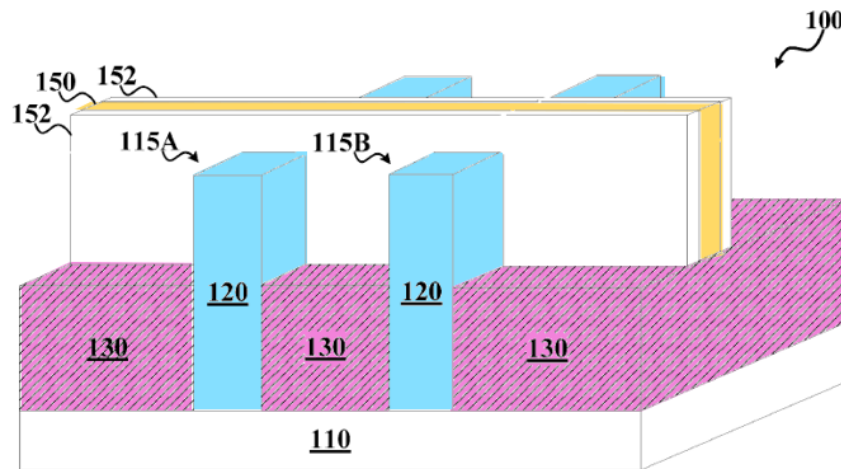


FIG. 2

4. 9[c]: forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench; and

127. Xu discloses and renders obvious this limitation. For example, a POSITA would have understood that Xu’s “gate-last process” is the admitted prior art “RMG process,” which a POSITA would have understood includes “forming a gate dielectric layer to conformally cover the sidewalls and bottom of the trench.” Ex. 1001 at 7:27-28.

128. Moreover, Xu discloses that its “gate structure 150 may include a gate dielectric layer.” Ex. 1004 at 4:2-3. A POSITA would have understood and found

obvious that the gate dielectric layer is deposited conformally to cover a sidewall and a bottom of the trench in a gate-last process. *See* Ex. 1008 at 16 (describing that multi-gate FETs “require[] highly conformal deposition techniques for the gate electrode and dielectric”).

5. 9[d]: forming a conductive layer to fill up the trench.

129. Xu discloses and renders obvious this limitation. For example, a POSITA would have understood that Xu’s “gate-last process” is the admitted prior art “RMG process,” which a POSITA would have understood includes “forming a conductive layer to fill up the trench.” Ex. 1001 at 7:28-29.

130. Further, Xu discloses that its “gate structure 150 may include . . . a gate electrode.” Ex. 1004 at 4:2-3. A POSITA would have understood and found obvious that in Xu’s “gate last process,” that final gate structure would include this “gate electrode” because it is a conductive layer replacing the dummy gate. Ex. 1004 at 4:10-13 (gate electrode includes “polysilicon and/or a metal . . . or other conductive materials”). Without it, the transistor would not work. In fact, it was well-known that the gate-last process forms a “replacement metal gate” that replaces the dummy gate and fills the trench left by the dummy gate. *See, e.g.*, Ex. 1009 at 34. After forming the replacement metal gate, the transistor would be as shown in Figure 6 of Xu, below, where the gate structure of FinFET 100 would fill the trench between spacers 152 left by removing the dummy gate (gold). Ex. 1004 at Fig. 6.

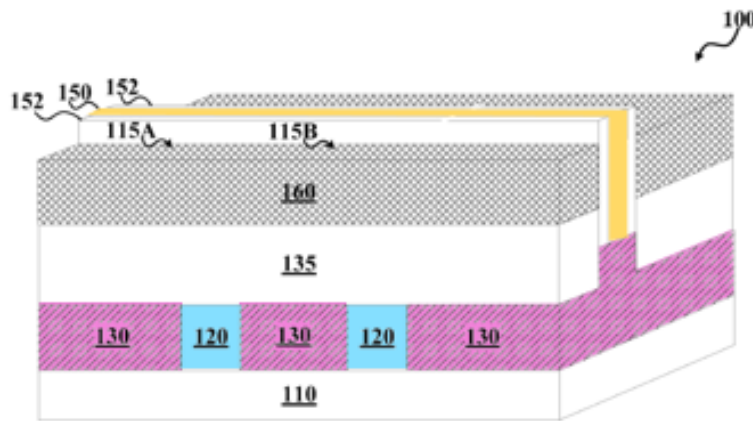


FIG. 6

VIII. Ground 1B: Claims 4 and 9 Would Have Been Obvious Over Xu In View Of Brask

131. In my opinion, claims 4 and 9 also would have been obvious to a POSITA over Xu in combination with Brask.

A. Motivation to Combine

132. As discussed above in Ground 1A, Xu discloses that the gate structure 150 may be formed in a “gate last process.” Ex. 1004 at 4:13-14. However, Xu does not explicitly disclose details of a gate-last process. A POSITA therefore would have looked to the prior art for details on FinFET fabrication using a gate-last process, such as the process disclosed by Brask. Brask teaches fabricating a FinFET transistor with a gate-last process where a “sacrificial gate electrode” (*i.e.*, “dummy gate”) is first formed on the fins. Ex. 1006 at ¶ [0059]; *see id.* at ¶ [0047] (“semiconductor bodies *or fins* 510 and 512”) (emphasis added). After source/drain regions of the transistor are formed, the sacrificial gate is removed to form an opening 622 exposing the

channel region of the fin. Ex. 1006 at ¶ [0072]. The opening is then filled with a gate dielectric layer and gate electrode material which serve as a “gate dielectric layer” and “gate electrode,” respectively, of the final FinFET device. *Id.* at ¶ [0074]. A POSITA would have understood Brask’s process of forming a sacrificial gate (*i.e.*, “dummy gate”) first, and then removing the sacrificial gate (*i.e.*, “dummy gate”) and replacing it with a metal gate, is a “gate-last” process.

133. Xu explicitly motivates the use of a gate-last process by stating that its gate structure may be formed this way. Ex. 1004 at 4:13-14. A POSITA would have known the benefits of gate-last processes, which were well-known by the ’384 patent’s priority date. For example, as discussed above in Ground 1A, *supra*, a gate-last process has the advantage that the “final metal gate is not exposed to the high activation anneal for the junctions.” Ex. 1008 at 16. “As a result, a better controlled work function for nMOS and pMOS can be achieved.” *Id.* Brask expressly recognizes this advantage, disclosing that gate-last processing enables tuning of gate electrode work functions such that performance of the transistor may be “dramatically improved.” Ex. 1006 at ¶ [0058]. Brask’s therefore expressly teaches, suggests, or otherwise motivates a POSITA to combine the teachings of Xu with the implementation details of Brask in order to achieve these advantages.

134. In the combination of Xu and Brask, a POSITA would recognize that the “gate structure 150” formed in step 16 of Figure 1 would be formed with a “gate-last

process” (Ex. 1004 at 4:13-14) as taught by Brask, *e.g.*, by initially forming a “sacrificial gate electrode” over the fins (Ex. 1006 at ¶ [0059]). Xu’s process would then proceed through source/drain formation.

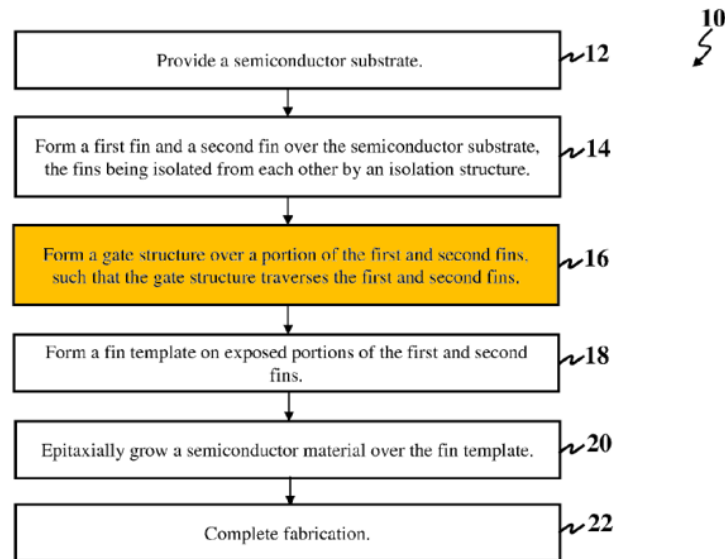


FIG. 1

135. After formation of the source and drain regions (*e.g.*, in Xu’s steps 18 and 20), an interlayer dielectric layer is formed. Ex. 1004 at 6:49-53; Ex. 1006 at ¶ [0071]. The dummy gate (*i.e.*, Brask’s sacrificial gate) is then removed to expose the fin, as taught by Brask. Ex. 1006 at ¶ [0072]. The gate dielectric and metal gate are subsequently formed in its place. *Id.* at ¶ [0074]. Notably, Xu and Brask teach forming the operative metal gate structure using substantially the same process—including conformally depositing a gate dielectric layer (Ex. 1004 at 4:2-3; Ex. 1006 at ¶ [0074], Figure 6J) and then forming a metal gate to fill the trench (Ex. 1004 at

4:2-3, Figures 2-3; Ex. 1006 ¶ [0074], Fig. 6J). This obvious combination of Xu and Brask discloses all of the limitations of claims 4 and 9, as shown below, rendering those claims obvious to a POSITA.

B. Claim 4: The fabrication method according to claim 1, wherein the gate structure is a dummy gate structure.

136. As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu in view of Brask renders obvious claim 4.

137. Xu contemplates using a “gate-last process,” such as the process taught by Brask. Ex. 1004 at 4:13-14. When Xu is combined with Brask as discussed above, the fabrication method will include depositing a “sacrificial gate electrode.” Ex. 1006 at ¶ [0060]. A POSITA would have recognized that the “sacrificial gate electrode” is a “dummy gate structure” because it is not an operative gate and will subsequently be replaced.

C. Claim 9:

138. As discussed above, Xu discloses and renders obvious the fabrication method of claim 1. Xu in view of Brask further renders obvious claim 9.

1. 9[a]: depositing an interlayer dielectric to surround the gate structure;

139. Xu in view of Brask renders obvious this limitation. For example, Xu expressly recognizes that the FinFET device 100 “may include additional features,” such as “*interlayer-dielectrics*” that are formed “over the substrate 110.” Ex. 1004 at

6:44-53. A POSITA would recognize that the Xu-Brask combination will also comprise depositing an interlayer dielectric to surround the gate structure. Indeed, like Xu, Brask teaches depositing a dielectric layer 620 after the “sacrificial gate electrode” is deposited. Ex. 1006 at ¶ [0071]. A POSITA would have understood this dielectric layer 620, which provides isolation between conductive structures in Brask, to be an “interlayer dielectric” as claimed. Ex. 1011 at v (“Interlayer dielectric (ILD) materials play the role of isolating electrically conducting features and films); *id.* at 3 (“isolation between metal lines in the same level is carried out by an inter-metal dielectric, and that between two metal levels is performed by an interlevel dielectric. Both types are usually called interlayer dielectrics (ILDs).”). As shown in Figure 6H of Brask, dielectric layer 620 surrounds the sacrificial gate electrode 604:

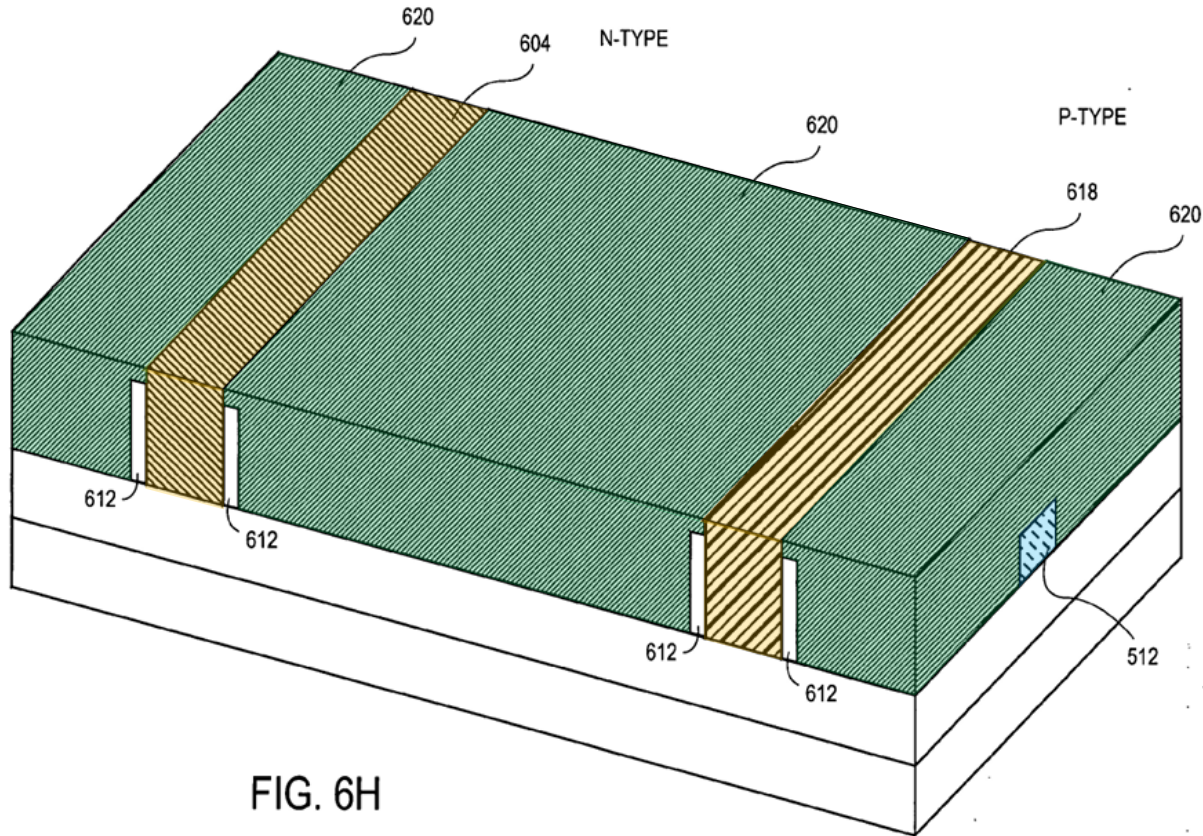


FIG. 6H

140. Further, as described above for Ground 1A, ILDs were well-known to a POSITA before 2013 and “used for isolating electrically conducting and semiconducting features and films” in transistors. Ex. 1011 at v. A POSITA would have understood and found obvious that to isolate the “electrically conducting” metal gate that will subsequently be formed, the interlayer dielectric would be deposited to surround the gate structure of the Xu-Brask combination.

2. 9[b]: removing the gate structure to leave a trench;

141. Xu in view of Brask renders obvious this limitation. For example, when Brask’s gate-last process is combined with Xu as discussed above, “the sacrificial gate

electrode 604 is [] removed” thereby forming “an opening 622 where the gate electrode” is to be formed, as taught by Brask. Ex. 1006 at ¶ [0072]. Brask’s Figure 6I illustrates the opening (*i.e.*, “trench”) after removing the sacrificial gate, which will also be present in the Xu-Brask combination.

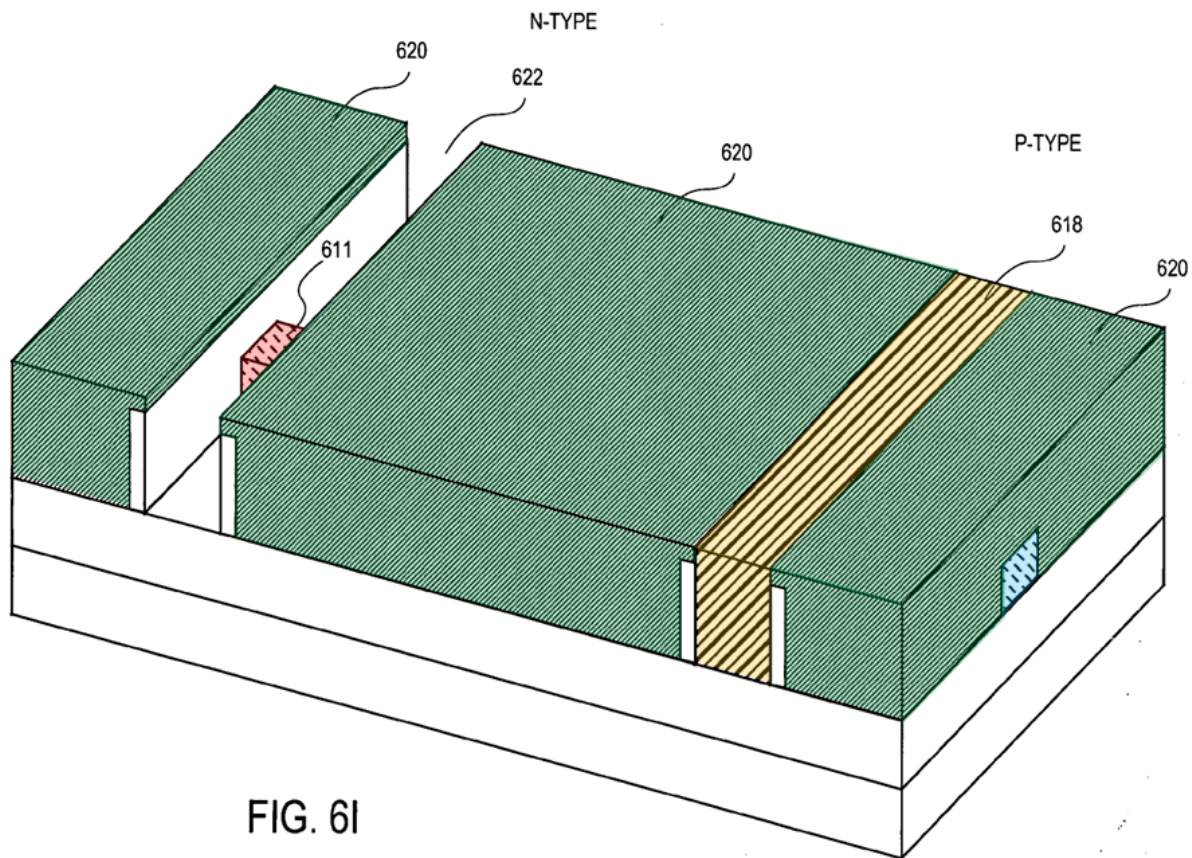
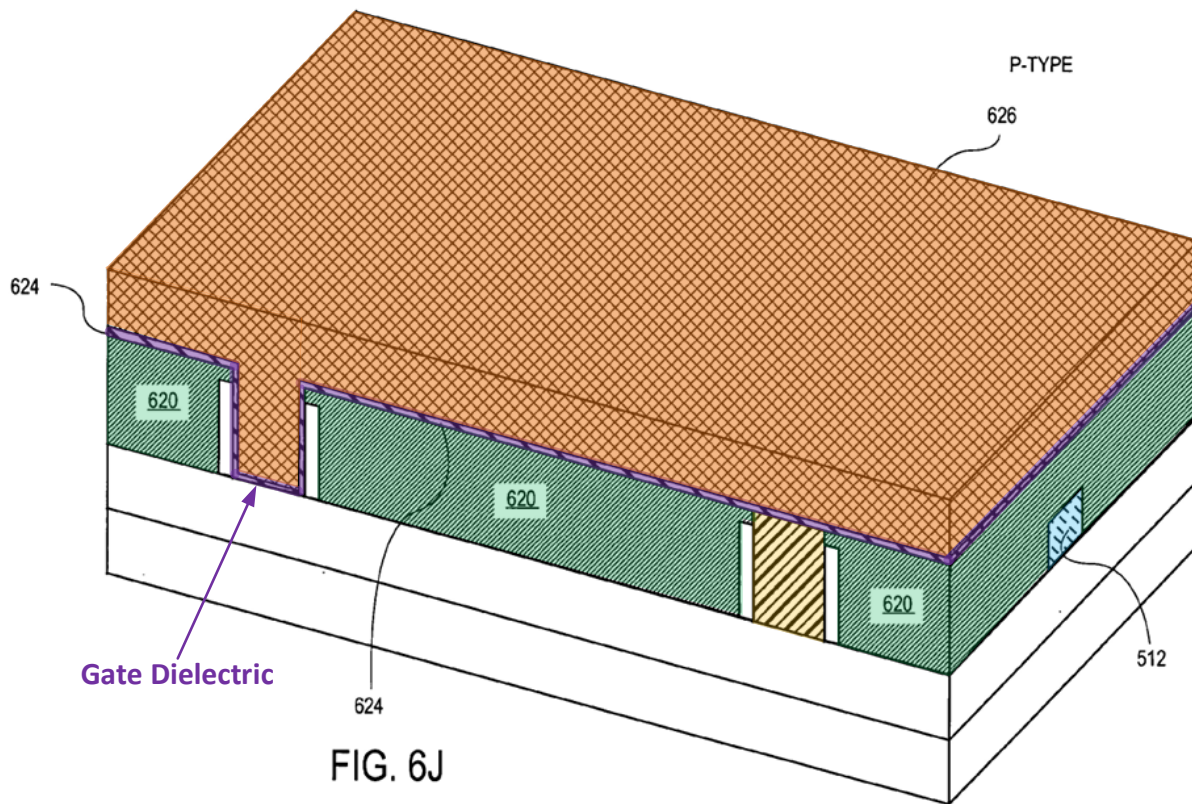


FIG. 6I

3. 9[c]: forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench; and

142. Xu in view of Brask renders obvious this limitation. For example, when Brask’s gate-last process is combined with Xu as discussed above, the process will include “a conformal deposition process, such as CVD or ALD ... to deposit a high

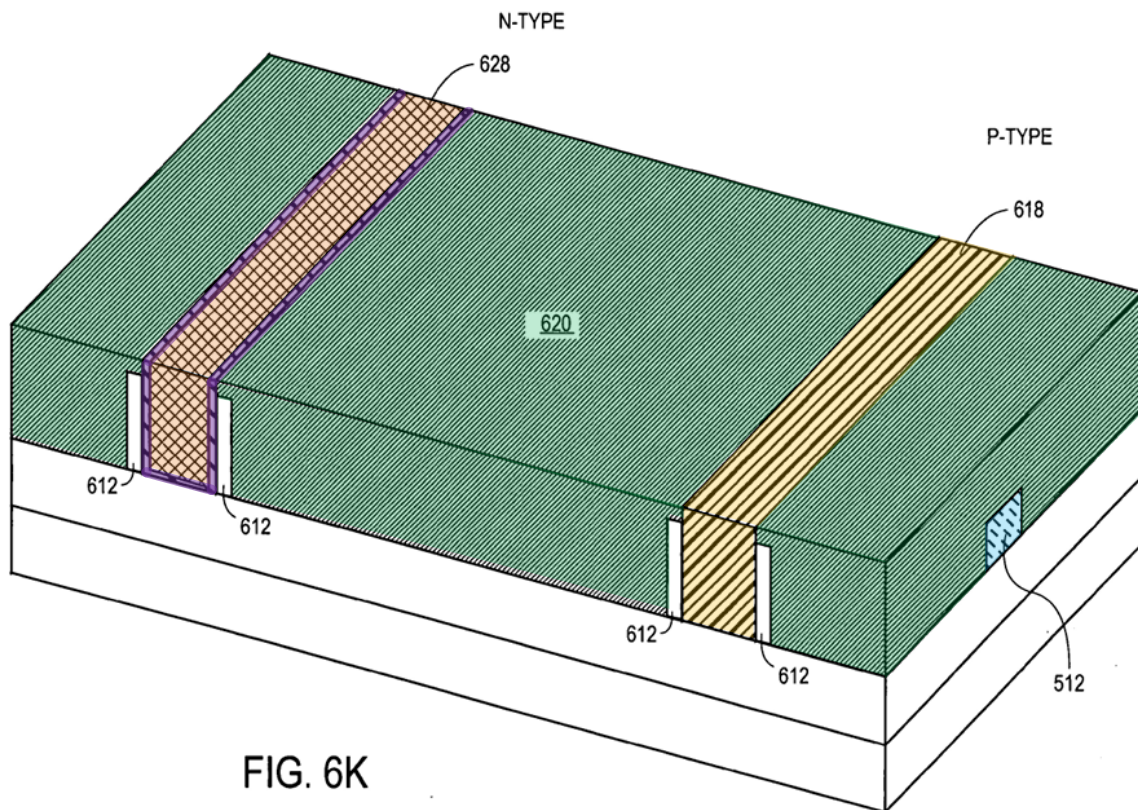
K gate dielectric layer” in the trench, as taught by Brask. Ex. 1006 at ¶ [0074]. As shown in Figure 6J, the dielectric layer 624 (purple) of Brask conformally covers a sidewall and a bottom of the trench, which will also be present in the Xu-Brask combination.



4. 9[d]: forming a conductive layer to fill up the trench.

143. Xu in view of Brask renders obvious this limitation. For example, when Brask’s gate-last process is combined with Xu as discussed above, the process will include blanket depositing a gate electrode material (*i.e.*, “a conductive layer”) over the gate dielectric layer, as taught by Brask. Ex. 1006 at ¶ [0074]. Figure 6J of Brask,

reproduced above, shows the gate electrode material 626 (orange) filling up the trench. Ex. 1006 at Fig. 6J. This gate electrode material filling up the trench will also be present in the Xu-Brask combination, and forms the gate electrode of the transistor after planarizing. Ex. 1006 at ¶ [0074], Fig. 6K.



IX. Ground 2A: Claims 1-3 And 5-8 Would Have Been Obvious Over Lin In View Of The Knowledge Of A POSITA

144. In my opinion, claims 1-3 and 5-8 would have been obvious to a POSITA over Lin in view of the knowledge of a POSITA.

A. Claim 1

1. 1[pre]: A fabrication method for a semiconductor device:

145. Lin discloses and renders obvious a fabrication method for a semiconductor device. Specifically, Lin describes its “Technical Field” as “relat[ing] to integrated circuit fabrication, and more particularly to a fin field effect transistor.” Ex. 1005 at ¶ [0001]. Lin describes a fabrication method for FinFET devices, including fabricating a fin, providing a gate over the fin, and growing strained materials in the source/drain regions from silicon germanium. *Id.* at ¶ [0002]. Figure 1 of Lin, reproduced below, illustrates a method of fabricating a FinFET, which is a semiconductor device. *Id.* at ¶ [0010].

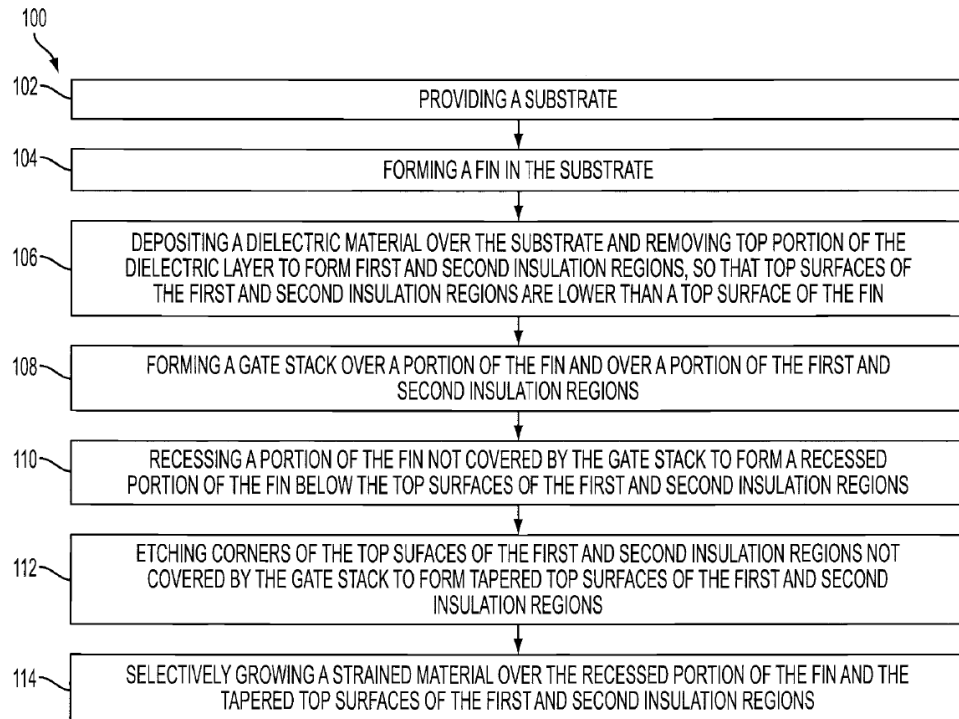


FIG. 1

2. 1[a]: forming a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces

146. Lin discloses and renders obvious this limitation. For example, step 104 of Lin's fabrication method 100 is "forming a fin in the substrate," as shown in Figure 1 below. Ex. 1005 at ¶ [0013].

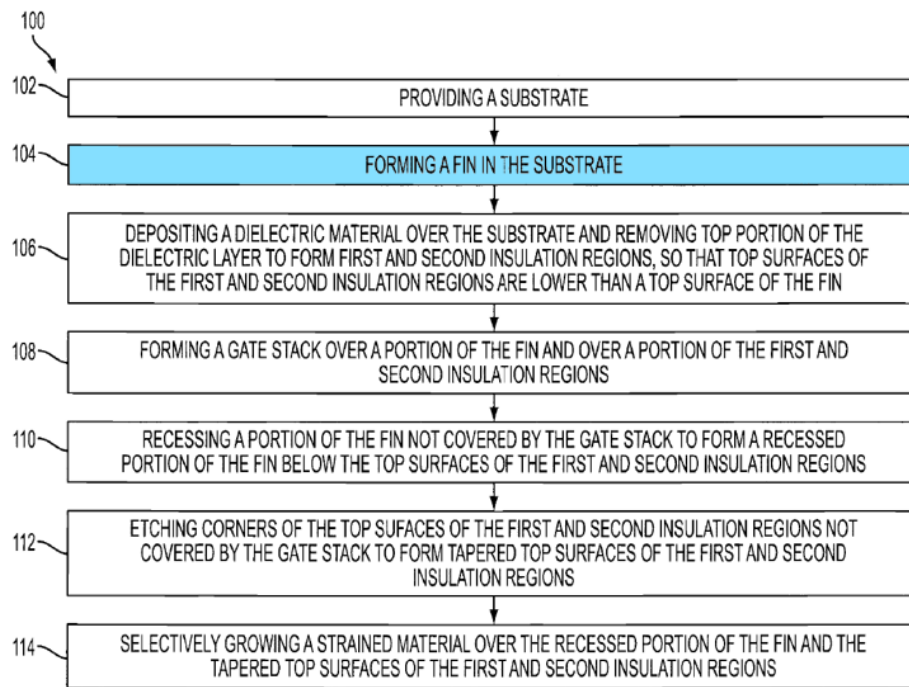


FIG. 1

147. As shown in Figures 3A and 3B, Lin forms fins 212 (blue) protruding from a surface 202S of substrate 202. *See* Ex. 1005 at ¶ [0018]; ¶ [0019] ("Portions of the semiconductor substrate 202 between trenches 210 form semiconductor fins 212").

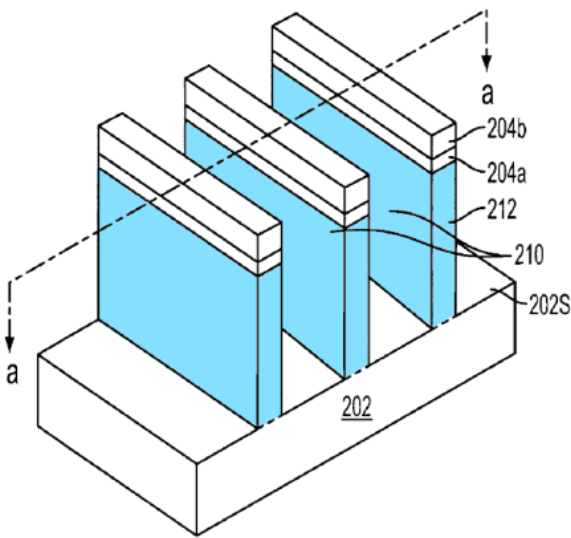


FIG. 3A

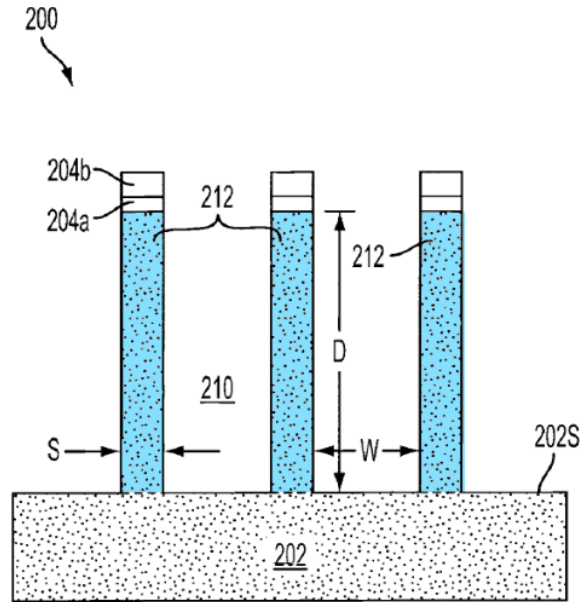


FIG. 3B

148. As shown in Figures 3A and 3B, the fins 212 each have a top surface and two side surfaces.

3. 1[b]: forming an isolation structure to surround the fin structure;

149. Lin discloses and renders obvious this limitation. For example, step 106 of Lin's method 100 includes depositing a dielectric material over the substrate and removing top portion of the dielectric layer to form first and second insulation regions. Ex. 1005 at ¶ [0013].

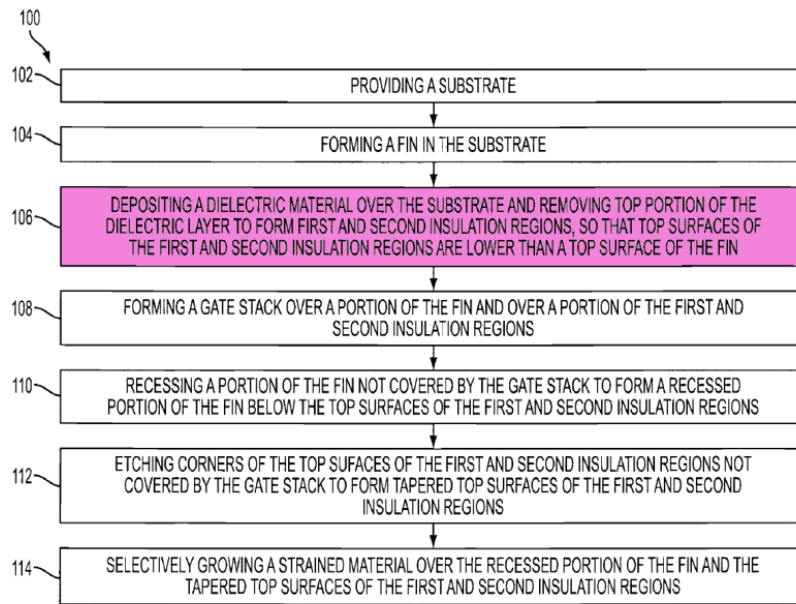


FIG. 1

150. The resulting insulation regions 216 (the claimed isolation structure) surround the fins 212 as shown in Figures 6A and 6B. *Id.* at ¶ [0026] (“fin 212 between the first and second insulation regions 216a, 216b....”).

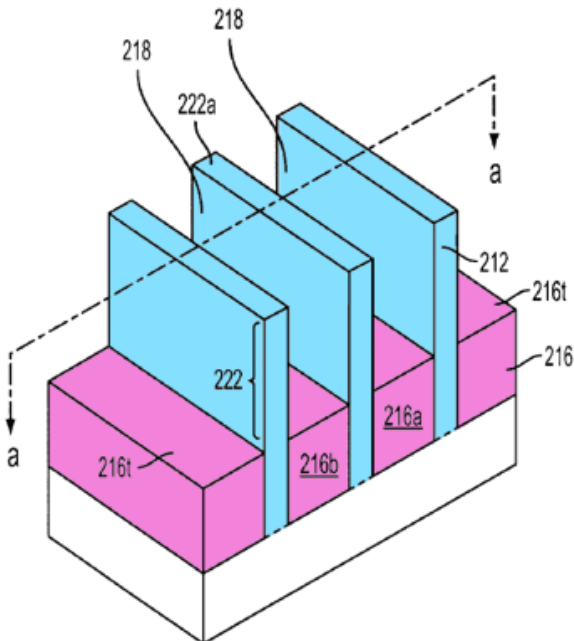


FIG. 6A

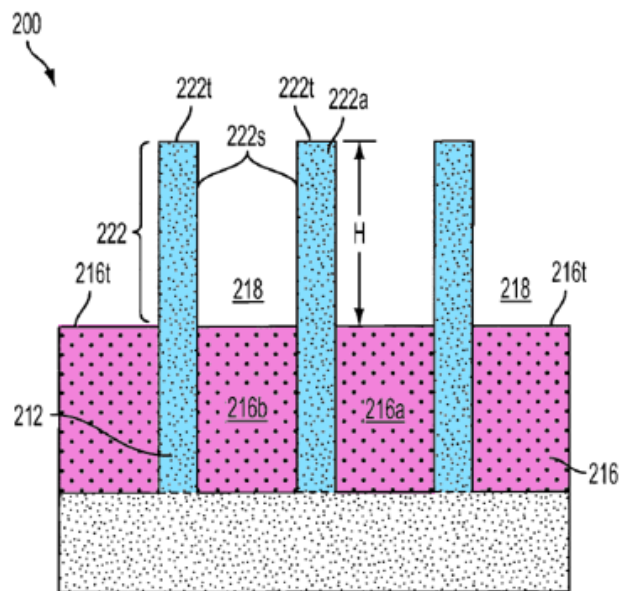


FIG. 6B

151. A POSITA would have further understood, and it would have been obvious to a POSITA, that the insulation regions 216 are isolation structures because they isolate the transistors that will ultimately be formed from the fins 212 from one another. Therefore, a POSITA would have understood and found obvious that the insulation regions 216 surround the fins 212 for the resulting transistors to function properly.

4. 1[c]: forming a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure, and covering a portion of the isolation structure;

152. Lin discloses and renders obvious this limitation. For example, step 108 of Lin's method includes forming a gate stack "over a portion of the fin and over a portion of the first and second insulation regions." Ex. 1005 at ¶ [0013].

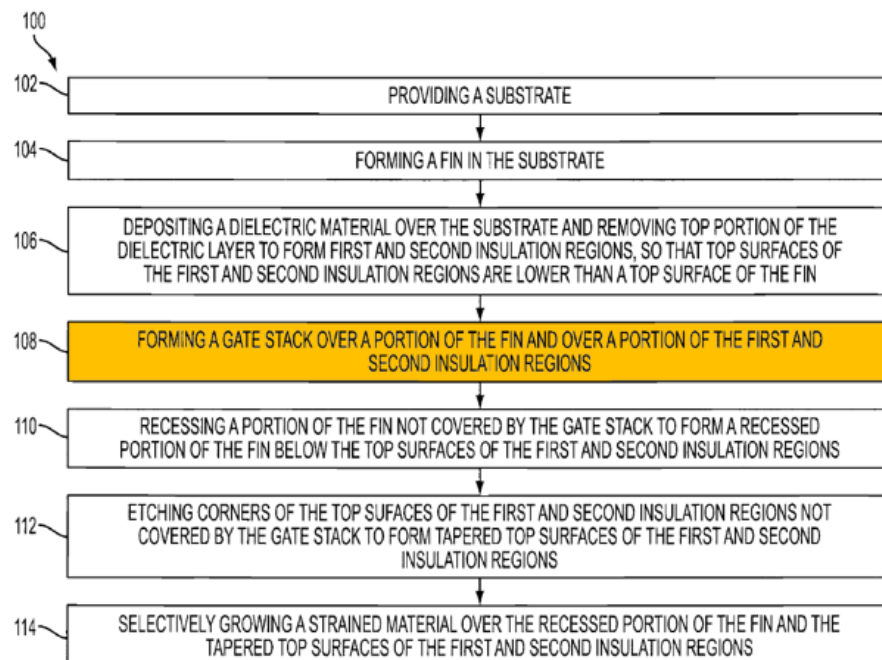


FIG. 1

153. As shown in Figures 7A and 7B, the gate stack 220 (gold) is formed “over the top surface 222t and sidewalls 222s of a non-recessed portion of the channel fin 222a.” *Id.* at ¶ [0027]. The gate stack 220 also “extend[s] to the flat top surfaces 216t of the first and second insulation regions 216a, 216b.” *Id.*

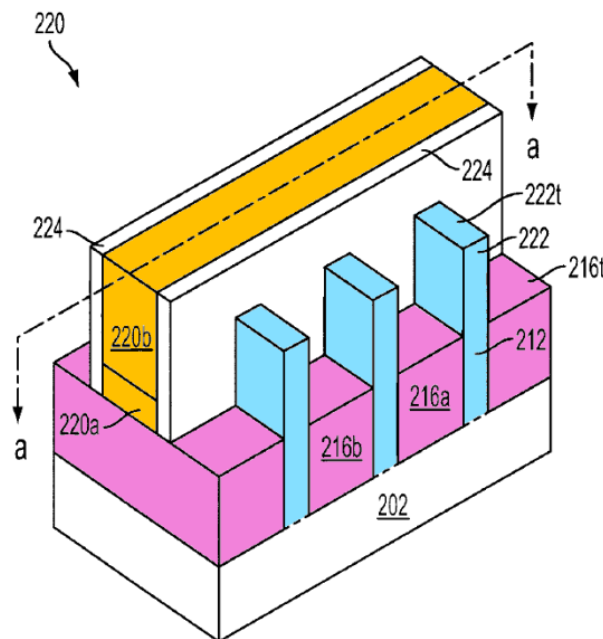


FIG. 7A

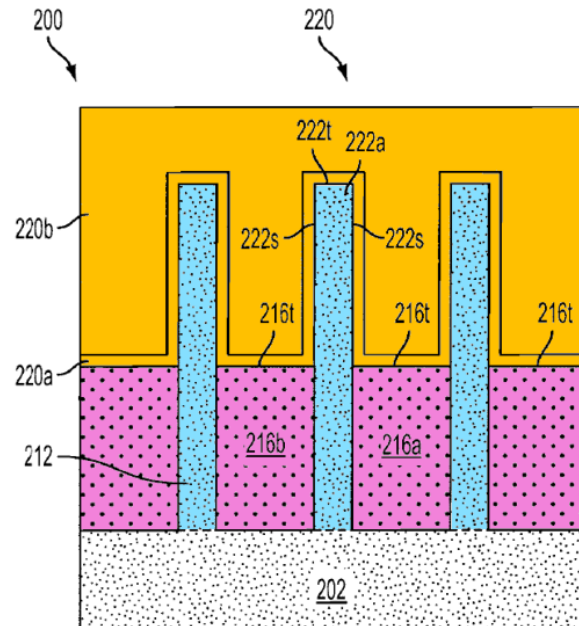
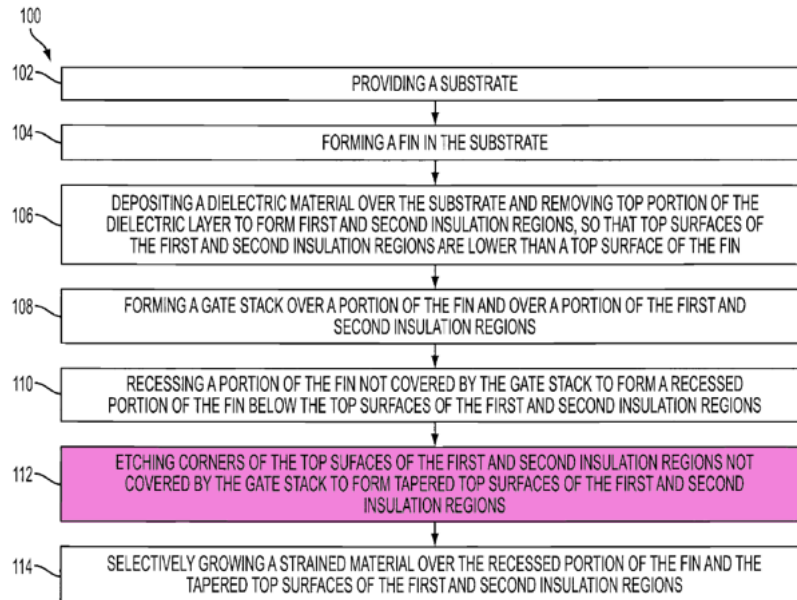


FIG. 7B

5. **1[d]: after the step of forming the gate structure, etching the isolation structure exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth;**

154. Lin discloses and renders obvious this limitation. For example, step 112 of Lin’s method 100 includes etching “corners of the top surfaces of the first and second insulation regions not covered by the gate stack . . . to form tapered top surfaces of the first and second insulation region.” Ex. 1005 at ¶ [0013]. As shown

in Figure 1, this etching step 112 is performed after forming the gate structure in step 108.



155. Lin discloses further etching the “corners of the flat top surfaces 216t of the first and second insulation regions 216a, 216b not covered by the gate stack 220” to “form a curved top portion of the tapered top surface 216u,” as shown in Figure 9C. *Id.* at 8:2-7. According to Lin, “the flat top surface 216t is higher than the highest point P of the tapered top surface 216u.” *Id.* at ¶ [0034]. Therefore, the second etching step etches the isolation structure exposed from the gate structure with top surface 216t until it is etched down to a first depth with new top surface 216u. *Id.* (“[T]he corners of the flat top surfaces 216t of the first and second insulation regions 216a, 216b not covered by the gate stack 220 are further removed until the flat portion of

the tapered top surface 216u disappear to form a curved top portion of the tapered top surface 216u”). In Lin, the minimum *etch depth* of the isolation structure is represented by D3, while the maximum *etch depth* corresponds to the original height of the isolation region minus D2 (see Fig. 9C below). Accordingly, the “first depth” limitation is satisfied by D3 in Lin. Specifically, the top surface of insulation regions 216a, 216b is a curved surface etched to a minimum depth of D3 and a maximum depth corresponding to the original height of the isolation region minus D2, as shown below. According to Lin, D3 “is in the range of about 0.1 to 0.3 nm.” *Id.*

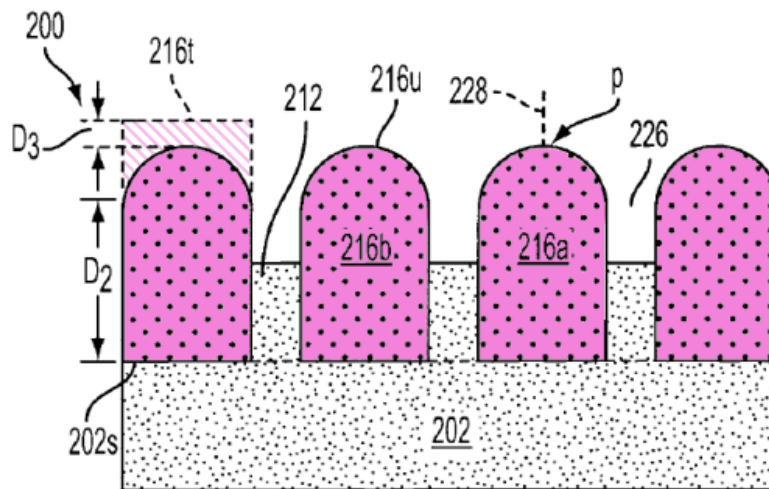


FIG. 9C

6. **1[e]: forming a recess in the fin structure at a side of the gate structure; and**

156. Lin discloses and renders obvious this limitation. For example, step 110 of Lin's fabrication method 100 includes recessing "a portion of the fin not covered

by the gate stack . . . to form a recessed portion of the fin below the top surfaces of the first and second insulation regions.” Ex. 1005 at ¶ [0013].

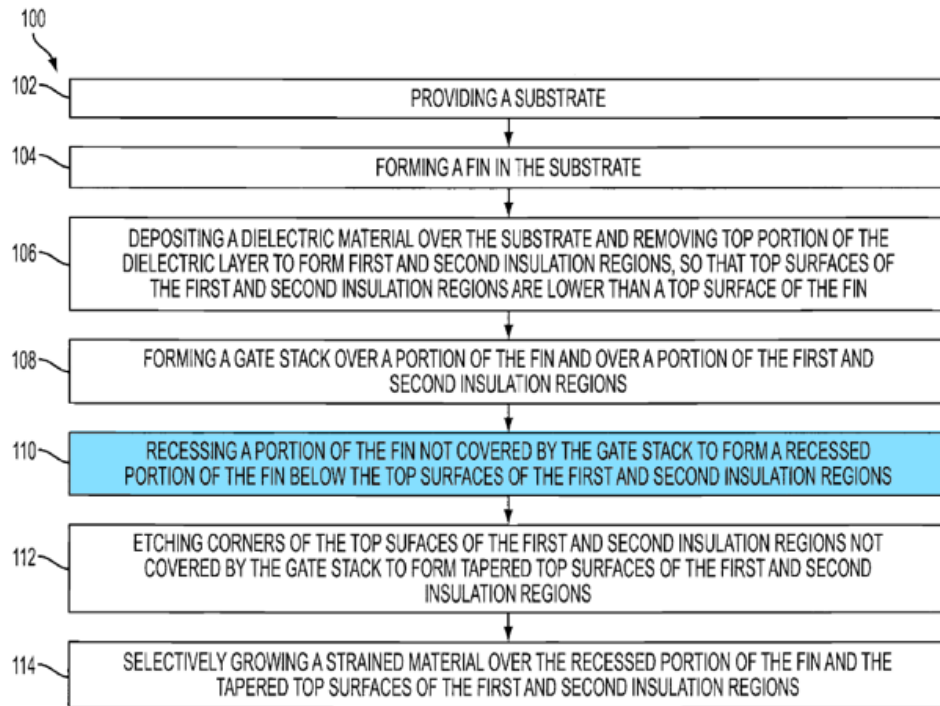


FIG. 1

157. Figures 8A and 8B illustrate the recessing of the fins 212 (blue) at a side of the gate structure 220 (gold):

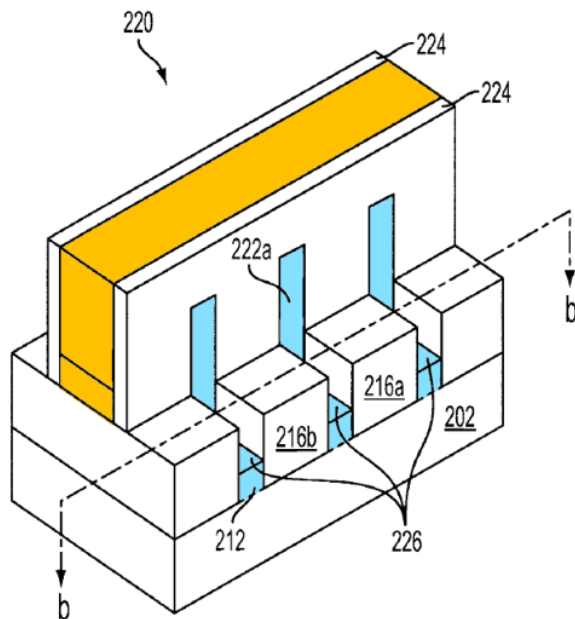


FIG. 8A

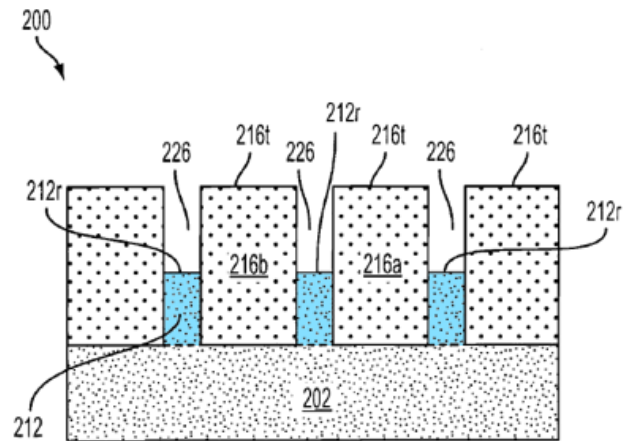


FIG. 8B

Ex. 1005 at Figs. 8A, 8B, cl. 14 (“recessing a portion of the fin ... to form a recessed portion of the fin below the top surfaces of the first and second insulation regions”).

158. As the '384 Patent expressly discloses, the timing for etching the isolation structure 20 exposed from the gate structure 30 and the spacers 40 and the timing for etching the fin structures 12 may be reversed.” Ex. 1001 at 6:22-25. Reflecting this, claim 1 does not require a particular order for these steps. *Id.* at cl. 1. In fact, when a particular order is needed, the '384 Patent explicitly requires it. For example, claim 1 explicitly limits that “etching the isolation structure” is performed “**after** the step of forming the gate structure.” Ex. 1001 at cl. 1. In contrast, claim 1 imposes no temporal requirement between the etching of the fins and the etching of the isolation structure. *Id.*

159. Nevertheless, a POSITA would have at least found it obvious to reorder the operations such that the isolation structure of Lin is etched before the formation of a recess in the fin structure. Both etch steps comprise well-known, conventional processes that a POSITA would have been able to perform in either order to arrive at the same resultant structure, and performing the isolation etch first does not achieve any unexpected results.

160. Specifically, the etching of the STI and the recessing of the fin are each independent, well-established processes. They target different materials (oxide and semiconductor, respectively) using highly selective etch chemistries. A POSITA would have recognized that chemistries for etching oxide (*e.g.*, CF₄ or CHF₃-based) could be used for etching back the STI and standard chemistries for etching silicon or SiGe (*e.g.*, Cl₂ or HBr-based) could be used for recessing the fin, and these processes could be performed without interfering with one another. *See* Ex. 1024 at 97-98. The processes could be performed in either order without affecting the ability to achieve the same resultant device structure.

161. Further, a POSITA would have understood that the anisotropic STI etch used in Lin to form the tapered isolation structures can be effectively performed when the fin is present. This is standard practice in FinFET fabrication, where STI shaping or recessing is often done after fin patterning. The tapered STI profile is formed using well-known anisotropic etch processes — such as fluorocarbon-based plasma etches

— that exhibit high selectivity to oxide over silicon or SiGe, allowing the STI to be etched without damaging or significantly affecting the fin. Masking techniques, including hard masks or resist layers, can be used to protect the fin sidewalls during the etch. Therefore, the presence of the fin does not prevent achieving the tapered STI shape disclosed in Lin, and a POSITA would not see any technical barrier to performing the STI etch in that context.

162. Accordingly, a POSITA would have found it obvious to perform the steps of Lin in this order.

7. 1[f]: forming an epitaxial layer to fill up the recess,

163. Lin discloses and renders obvious this limitation. For example, Lin's fabrication method 100 includes step 114 where "a strained material is selectively grown over the recessed portion of the fin and the tapered top surfaces of the first and second insulation regions." Ex. 1005 at ¶ [0013].

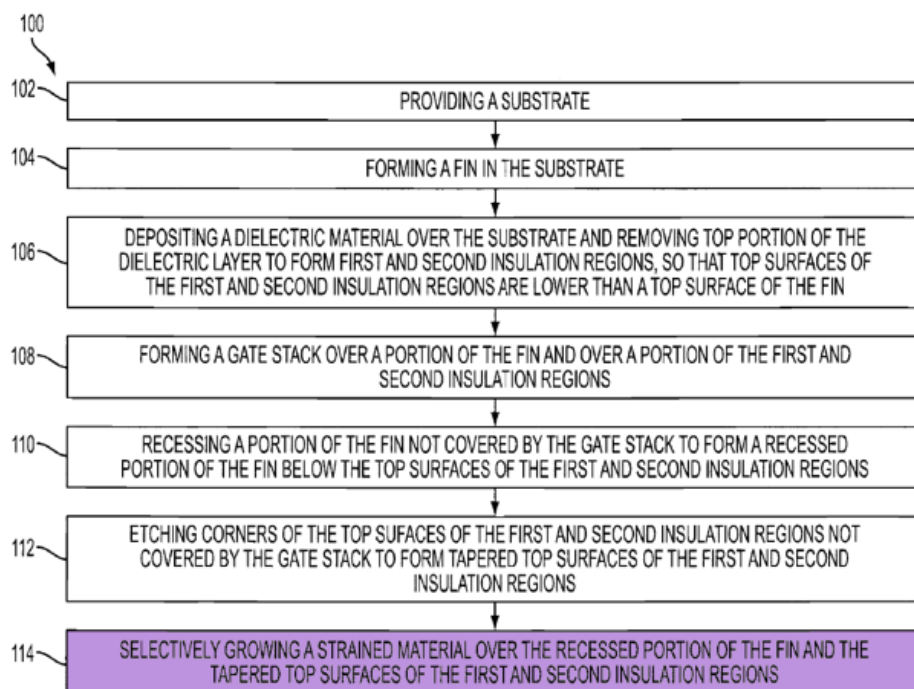


FIG. 1

164. Figure 10C illustrates the strained material 230 filling the recesses 226 in the fin structure 212. *Id.* at Fig. 10C.

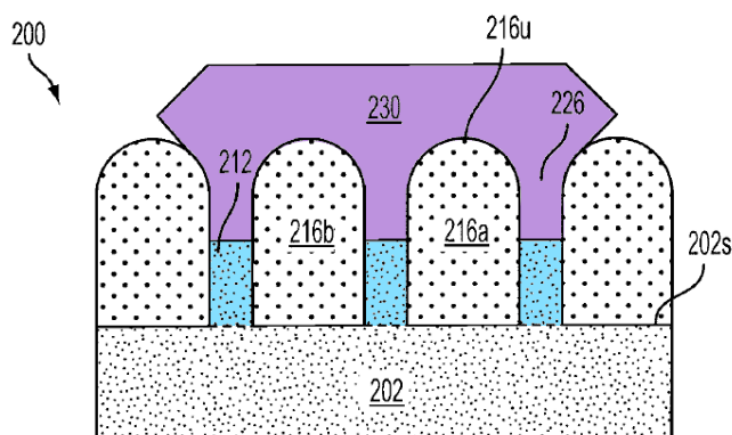


FIG. 10C

165. Lin further discloses that strained material 230 is an epitaxial layer because it can be silicon carbon (SiC) that is “epi-grown by a LPCVD process to form

the source and drain regions of the n-type FinFET.” *Id.* at ¶ [0035]. Additionally, the strained material can be “silicon germanium (SiGe)” that “is epi-grown by a LPCVD process to form the source and drain regions of the p-type FinFET.” *Id.*

8. 1[g]: wherein a bottom surface of the recess has a second depth, and the second depth is deeper than the first depth.

166. Lin discloses and renders obvious this limitation. For example, Lin discloses that when the recesses 226 are formed they have a top surface 212r that is “below the flat top surfaces 216t of the first and second insulation regions 216a, 216b.” Ex. 1005 at ¶ [0031]. Further, in Figure 9C the bottom surface of the recess 226 is the top surface of the remaining fin portion 212. The depth of this surface (the claimed second depth) is shown as D_R in cyan and is deeper than the first depth D_3 .⁷ *Id.*

⁷ The second depth is D_R is deeper even if the first depth is taken as the deepest portion of the tapered top surface 216u.

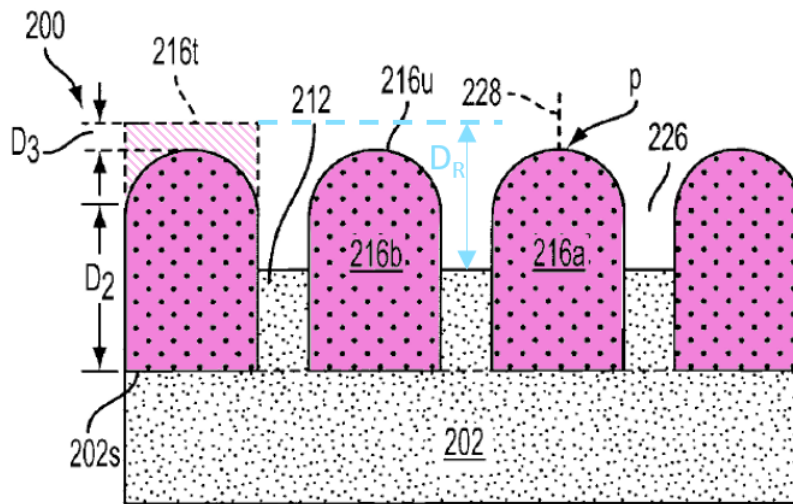


FIG. 9C

B. Claim 2: The fabrication method according to claim 1, wherein the isolation structure is a shallow trench isolation structure.

167. As discussed above, Lin discloses and renders obvious the fabrication method according to claim 1. Lin further discloses and renders obvious the additional limitation of claim 2. For example, Lin discloses forming insulation regions between fins (alternately referred to as “*isolation region[s]*”) by depositing insulation material in trenches 210. See Ex. 1005 at Figures 3A-5B, ¶¶ [0023]-[0025].

168. A POSITA would have understood that the insulation structure formed in trenches 210 of Lin is a shallow trench isolation (STI) structure. As described in Lin (Ex. 1005 at ¶¶ [0019] – [0023], Figs. 3A-5B), the fabrication process involves etching narrow and shallow trenches into a silicon substrate and then filling them with oxide (e.g., silicon dioxide) using high-density plasma CVD or low-pressure CVD

processes. These steps are hallmarks of STI technology, which has been the standard method for device isolation in CMOS manufacturing since at least the early 2000s.

169. Moreover, Ex. 1010 at p. 25 confirms that “shallow trench isolation (STI) is the preferred method for device isolation in advanced wafer fabs,” highlighting the widespread industry adoption and familiarity with STI techniques by the relevant time period. A POSITA would have recognized that the insulation regions described in Lin, which isolate the fin structures and are recessed below the fin top surface (see Ex. 1005 at ¶ [0025]), conform to the functional and structural characteristics of STI. This understanding would have made it obvious to interpret or implement Lin’s “insulation regions” using conventional STI processes.

170. Furthermore, a shallow trench isolation structure would have been obvious in view of the knowledge of a POSITA. *Id.* For example, as early as 2001, “[s]hallow trench isolation (STI) is the preferred method for device isolation in advanced wafer fabs.” Ex. 1010 at 25. A POSITA would have been motivated to use the “preferred method for device isolation” for what Lin variously refers to as “isolation regions” and “insulation regions.” Ex. 1005 at ¶ [0025].

C. Claim 3: The fabrication method according to claim 1, wherein a step for etching the isolation structure comprises wet etching or dry etching.

171. As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin further discloses and renders obvious the additional limitation

of claim 3. Specifically, Lin discloses that the etching of the isolation regions illustrated in Figures 9A-9C can be performed with either wet or dry etching: “In one embodiment, the etching step may be performed using a wet etching process, for example, by dipping the substrate 202 in hydrofluoric acid (HF).” Ex. 1005 at ¶ [0032]. “In another embodiment, the etching step may be performed using a non-biased dry etching process, for example, the dry etching process may be performed using CHF₃ or BF₃ as etching gases.” *Id.*

D. Claim 5: The fabrication method according to claim 1, wherein a step for forming the recess comprises wet etching or dry etching.

172. As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin further discloses and renders obvious the additional limitation of claim 5. For example, Lin discloses the etching of the fin 212 to form the recessed portion 226 can be performed using a dry etching process. Lin discloses a “biased etching process” that “may be performed under a pressure of about 1 mTorr to 1000 mTorr... [and] using a HBr and/or Cl₂ as etch gases.” Ex. 1005 at ¶ [0031].

173. A POSITA would have understood that this process is a dry etching process at least because it uses etch gases rather than an etching liquid. HBr and Cl₂ were widely recognized in the field as standard etch gases for reactive ion etching (RIE) and plasma etching of silicon (which are forms of dry etching), especially for applications like gate patterning and fin formation. *See* Ex. 1024 at 97-99. These

gases are standard for forming precise recesses with vertical sidewalls in FinFET and STI processes. Therefore, a POSITA would have recognized that Lin's described etch step falls squarely within the scope of "dry etching" as recited in claim 5.

E. Claim 6: The fabrication method according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

174. As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin further discloses and renders obvious the additional limitation of claim 6. For example, Lin discloses that the strained material 230 (the epitaxial structure as shown above for limitation 1.f) can be silicon germanium (SiGe) in a p-type FinFET and is "epi-grown" (*i.e.*, "epitaxially grown"). Ex. 1005 at ¶ [0035]. Lin also discloses that in an n-type FinFET, the strained material 230 can be silicon carbon (SiC), another name for silicon carbide, and is also "epi-grown." *Id.* It also would have been obvious to a POSITA to dope the silicon carbide with phosphorous to form phosphor-doped silicon carbide. For example, Lin teaches that phosphorous is an n-type dopant, which also would have been well-known to a POSITA. Ex. 1005 at ¶ [0016].

F. Claim 7: The fabrication method according to claim 1, further comprising forming a spacer before etching the isolation structure, wherein the spacer is disposed on a sidewall of the gate structure.

175. As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin further discloses and renders obvious the additional limitation

of claim 7. For example, before the etching of the isolation structure depicted in Figs. 9A-9C, Lin discloses spacers 224 (dark blue) that are formed “on two sides of the gate stack 220” (gold). Ex. 1005 at ¶ [0030].

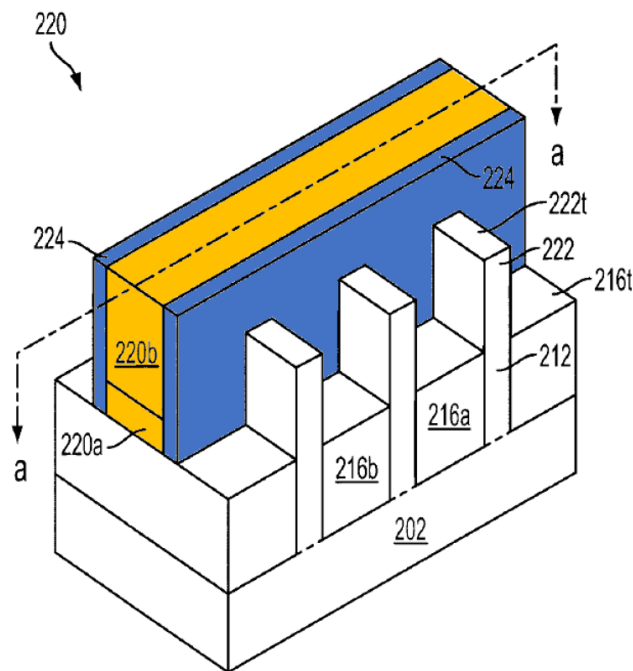


FIG. 7A

176. Specifically, Lin discloses that “a dielectric layer 224 [is] formed over the substrate” and then “etching is performed on the dielectric layer to form *a pair of spacers* 224 on two sides of the gate stack. *Id.* (emphasis added). Because these spacers are present when Lin’s isolation structure is etched, as shown in Figs. 8A-9C, a POSITA would have understood that the spacer formation occurs “before etching the isolation structure” as claimed.

- G. Claim 8: The fabrication method according to claim 7, wherein a step for forming the spacer comprises: depositing a material layer to conformally cover the gate structure and the fin structure, and etching the material layer until the isolation structure is exposed.**

177. As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin further discloses and renders obvious the additional limitation of claim 8. Lin discloses that forming the spacer comprises forming a “blanket layer of the dielectric layer 224.” Ex. 1005 at ¶ [0030]. A POSITA would have understood this “blanket layer” to be deposited conformally, as Lin explicitly discloses that the dielectric layer may be formed using deposition techniques such as chemical vapor deposition (CVD), physical vapor deposition (PVD), or atomic layer deposition (ALD). Ex. 1005 at ¶ [0030]. It was well-known by 2013 that both CVD and ALD are conformal deposition methods, commonly used in spacer formation to ensure uniform coating over complex topographies. *See generally* Ex. 1025 (describing conformal nature of CVD processes); Ex. 1011 at Chapter 10 (Describing conformal nature of ALD processes). In particular, CVD (including LPCVD and PECVD) and ALD were routinely used in FinFET fabrication to deposit spacer materials such as silicon nitride with high step coverage. These techniques are designed to conformally coat all exposed surfaces, including the top and sidewalls of both the gate and fin structures. Because Lin’s gate structure 220 and fin 212 are already formed and exposed at this stage of the process (see Ex. 1005, Figs. 6A–7A), a POSITA would have understood

and found obvious that the blanket dielectric layer 224 necessarily conformally covers both the gate and the fin, as recited in claim 8.

178. Lin further discloses etching the blanket layer to form a pair of spacers 224 on the sides of the gate stack 220. Ex. 1005 at ¶ [0030]. As shown in Figure 7A, above, the isolation structure 216 is exposed as a result of this etching, indicating that horizontal portions of the dielectric layer have been removed by anisotropic etching, consistent with known spacer formation methods. *Id.* at Fig. 7. Additionally, spacers were well-known in the art and were used to isolate the gate structure from the source/drain regions of a transistor and to control dopant placement and stress profiles. As such, the function of the well-known spacers dictates it would not cover the entire isolation structure, but only needs to be disposed on the sidewalls of the gate structure. Thus, a POSITA would have recognized that dielectric layer 224 must be deposited conformally in order to result in spacers that meet both the structural and functional requirements.

X. Ground 2B: Claims 4 and 9 Would Have Been Obvious Over Lin In View Of Brask

179. In my opinion, claims 4 and 9 would have been obvious to a POSITA over Liu in view of Brask.

A. Motivation to Combine

180. Lin discloses a “gate-first” fabrication process where the operative metal gate is formed before the source and drain regions of the transistor. But by the priority date of the ’384 patent, POSITAs would have understood that “gate-first” processes would expose the gate structure to the “high activation anneal for the junctions” thereby degrading performance of the transistor. Ex. 1008 at 16; *see also* Ex. 1012 at xxiii (describing thermal annealing at high temperature to remove damage caused by ion implantation), 17 (“Thermal annealing is a required step after implantation.”); Ex. 1006 at ¶ [0069]. A POSITA also would have understood that gate-last processing avoids this issue by deferring gate formation until after the annealing step, thereby enabling tighter control of the gate “work function for nMOS and pMOS [devices].” Ex. 1008 at 16. For this reason, by 2013, there was an industry-wide “shift from ‘gate first’ to ‘gate last’ processing.” *Id.*

181. A POSITA therefore would have been motivated to modify Lin’s gate-first process by adopting a gate-last approach, such as the process taught by Brask, in order to avoid thermal degradation of the gate stack. Specifically, Brask teaches fabricating a FinFET transistor with a gate-last process where a “sacrificial gate electrode” is first formed on the fins. Ex. 1006 at ¶ [0059]; *see id.* at ¶ [0046] (“semiconductor bodies *or fins* 510 and 512”) (emphasis added). After source/drain regions of the transistor are formed, the sacrificial gate is removed to form an opening

622 exposing the channel region of the fin. Ex. 1006 at ¶ [0072]. The opening is then filled with a gate dielectric layer and gate electrode material which serve as a “gate dielectric layer” and “gate electrode,” respectively, of the final FinFET device. *Id.* at ¶ [0074]. A POSITA would have understood Brask’s process of forming a sacrificial gate (*i.e.*, “dummy gate”) first, and then removing the sacrificial gate (*i.e.*, “dummy gate”) and replacing it with a metal gate, is a “gate-last” process. For example, the “gate last” processing described in Ex. 1008 comprises patterning a dummy gate that later removed after source/drain processing and replaced by the final gate stack. Ex. 1008 at 16. Brask’s sacrificial gate process includes these same steps and forms the gate “last” after processing other features of the transistor. *See* Ex. 1006 at ¶ [0074]. Brask’s gate-last process is thus a well-known technique applicable to Lin’s FinFET fabrication method, ready for improvement for the reasons described above, and with the predictable results of avoiding exposing the gate to the required high-activation anneal.

182. Further, the combination of Lin and Brask is expressly motivated by the teachings of Brask. For example, Brask discloses that gate-last processing enables tailoring of gate electrode work functions such that performance of the transistor may be “dramatically improved.” Ex. 1006 at ¶ [0058]. This provides an express motivation to combine Brask’s gate-last processing with the teachings of Lin to improve gate control and overall device characteristics. *Id.*

183. In the combination of Lin and Brask, a POSITA would understand that the “gate stack 220” of Lin would instead be formed by depositing a “sacrificial gate electrode” over the fins (Ex. 1006 at ¶ [0059]) as taught by Brask. Fabrication would proceed through Lin’s steps for source/drain formation and remaining features of the FinFET. Ex. 1005 at Fig 1.

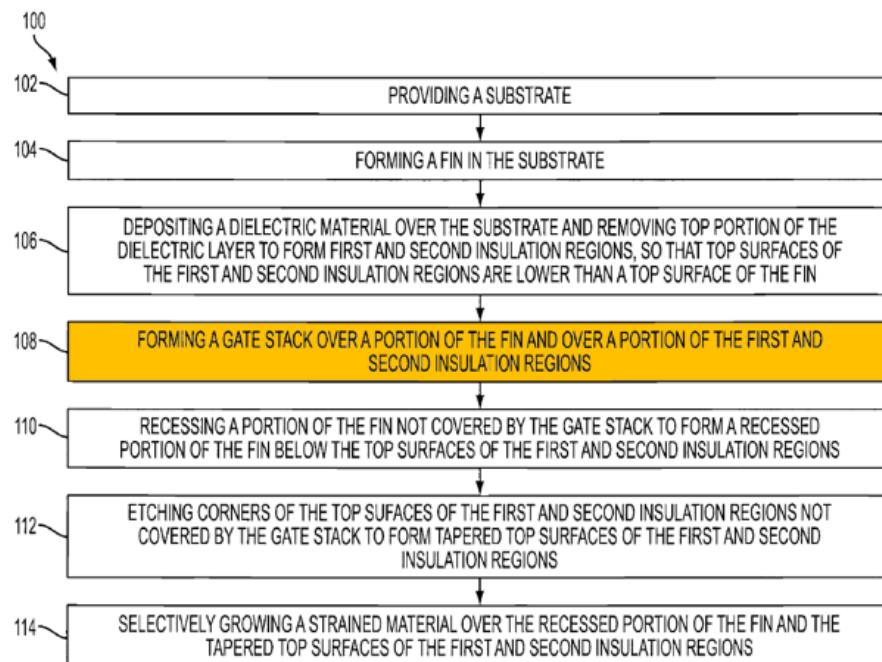


FIG. 1

184. After formation of the source and drain regions (e.g., in Lin’s steps 110, 112, and 114), an interlayer dielectric layer is formed. *See* Ex. 1005 at ¶ [0037]; Ex. 1006 at ¶ [0071]. At that point, a POSITA would understand that the sacrificial gate is removed to form an opening exposing the fin, as taught by Brask. Ex. 1006 at ¶ [0072]. The gate dielectric and metal gate are subsequently formed in that opening. *Id.* at ¶ [0074]. Notably, Lin and Brask disclose highly similar methods forming the

final gate structure. Both teach conformally depositing a gate dielectric layer (Ex. 1005 at 6:36-38, Figure 7B; Ex. 1006 at ¶ [0074], Figure 6J) followed by forming a metal gate to fill the trench (Ex. 1005 at ¶ [0030], Figures 7A-7B; Ex. 1006 ¶ [0074], Fig. 6J). These shared steps further support the obviousness of their combination. This obvious combination of Lin and Brask discloses all of the limitations of claims 4 and 9, as shown below, rendering those claims obvious to a POSITA.

B. Claim 4: The fabrication method according to claim 1, wherein the gate structure is a dummy gate structure.

185. As discussed above for Ground 2A, Lin discloses and renders obvious the fabrication method of claim 1. Lin in view of Brask renders obvious claim 4.

186. The combination of Lin and Brask teaches a dummy gate structure. When Lin is combined with Brask as discussed above, the fabrication method will include depositing a “a sacrificial gate electrode.” Ex. 1006 at ¶ [0060]. A POSITA would have recognized that the “sacrificial gate electrode” is a “dummy gate structure” because it is not an operative gate and will subsequently be replaced

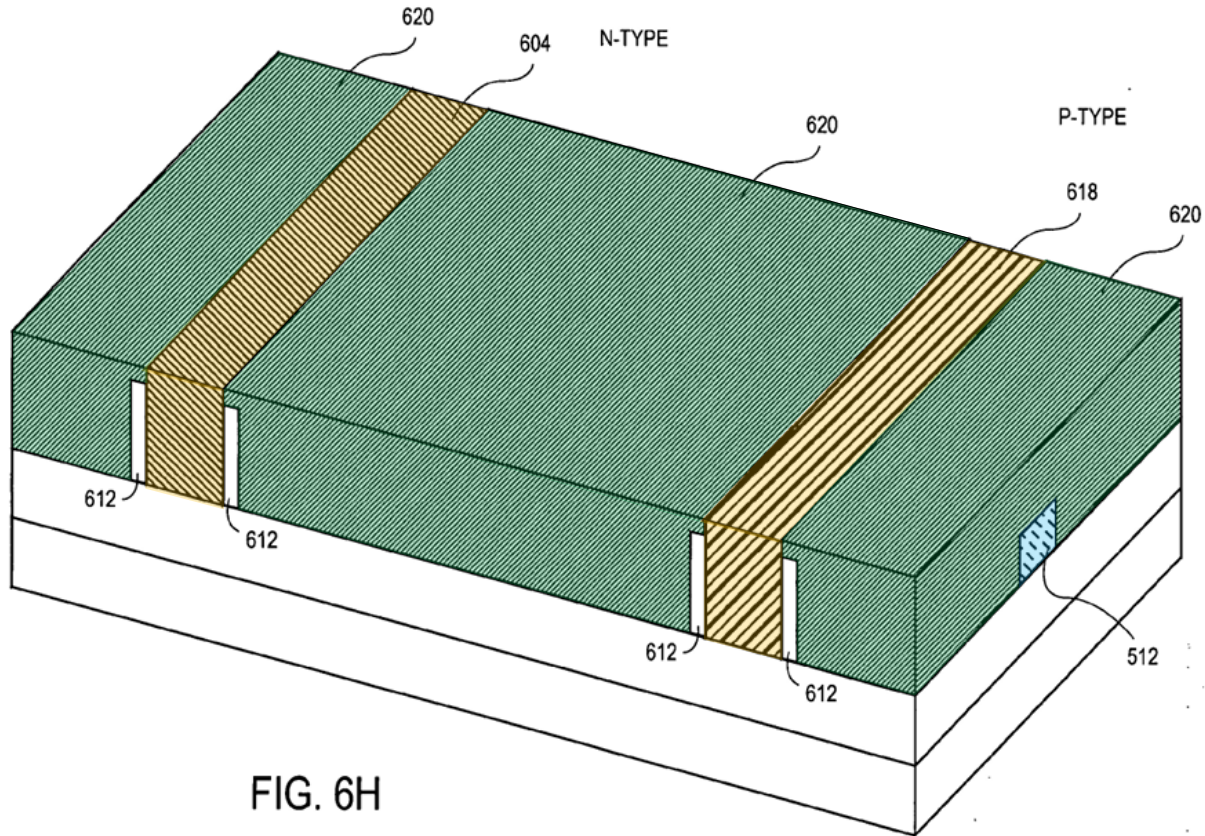
C. Claim 9:

1. 9[pre]: The fabrication method according to claim 1, further comprising:

187. As discussed above, Lin discloses and renders obvious the fabrication method of claim 1. Lin in view of Brask renders obvious claim 9.

2. 9[a]: depositing an interlayer dielectric to surround the gate structure;

188. Lin in view of Brask renders obvious this limitation. For example, Lin expressly recognizes that the FinFET device 200 “may undergo further CMOS processes to form various features,” such as “dielectric layers.” Ex. 1005 at ¶ [0037]. A POSITA would have recognized that the Lin-Brask combination will also comprise depositing an interlayer dielectric to surround the gate structure. Brask also teaches depositing a dielectric layer 620 after the “sacrificial gate electrode” is deposited. Ex. 1006 at ¶ [0071]. As shown in Figure 6H of Brask, dielectric layer 620 (green) surrounds the sacrificial gate electrode (gold):



189. As described above with respect to the combination of Xu and Brask, a POSITA would understand this dielectric layer to function as an interlayer dielectric (ILD). As described in Exhibit 1011, ILDs are electrically insulating films used to isolate electrically conducting and semiconducting features in an integrated circuit. *See* Ex. 1011 at v, 3. In particular, ILDs are deposited between or around features such as gate electrodes and interconnects to prevent electrical interference and to enable multilevel integration. *Id.* at 1–6. Brask’s dielectric layer 620 performs this very function by encapsulating the sacrificial gate and isolating it from the subsequently

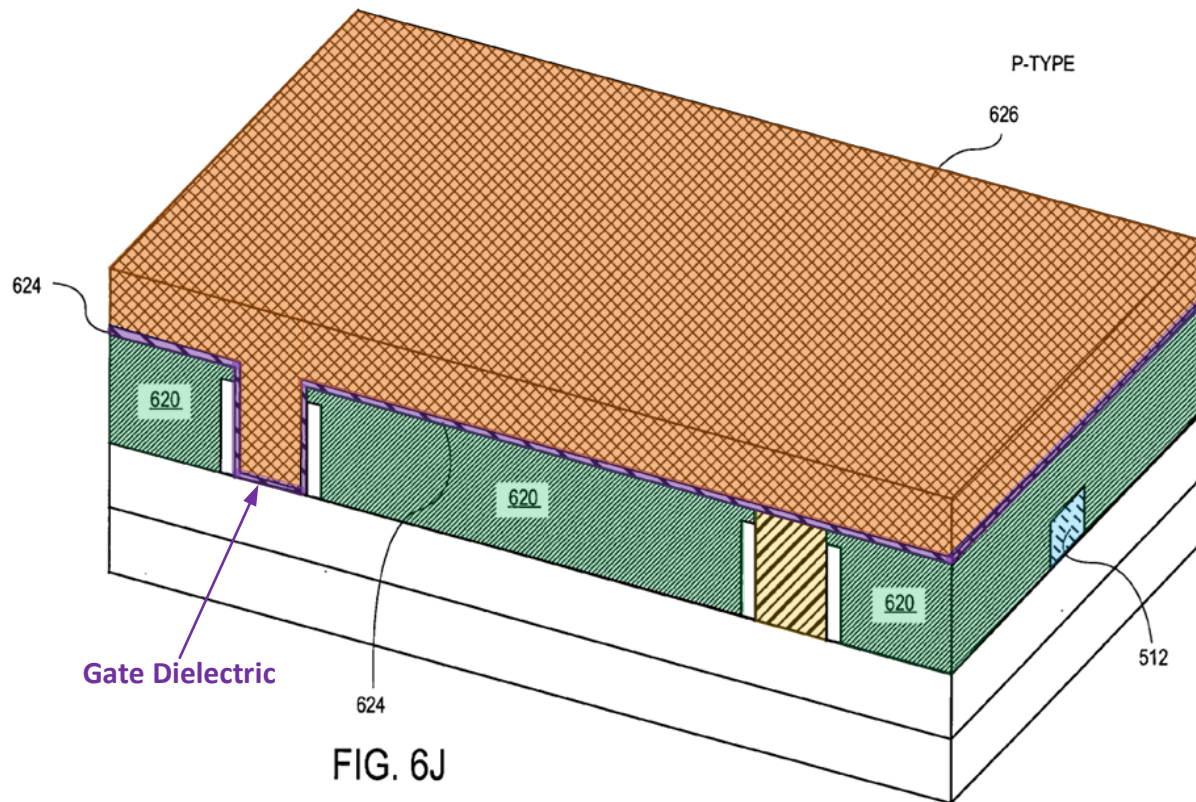
formed contacts or metallization layers. Therefore, a POSITA would have recognized dielectric layer 620 as a conventional ILD used for isolation and integration in gate-last FinFET processing.

190. Further, as described above for Grounds 1A and 1B, ILDs were well-known to a POSITA before 2013 and used for isolating electrically conducting and semiconducting features and films” in transistors. *See* Ex. 1010 at 27 (“The interlayer dielectric (ILD) is used between different metal layers has traditionally been silicon dioxide (doped or undoped).”); Ex. 1011 at v. A POSITA would have understood and found obvious that to isolate the “electrically conducting” metal gate that will subsequently be formed, the interlayer dielectric would be deposited to surround the gate structure of the Lin-Brask combination.

3. 9[b]: removing the gate structure to leave a trench;

191. Lin in view of Brask renders obvious this limitation. For example, when Brask’s gate-last process is combined with Lin as discussed above, “the sacrificial gate electrode 604 is [] removed” thereby forming “an opening 622 where the gate electrode” is to be formed, as taught by Brask. Ex. 1006 at ¶ [0072]. Brask’s Figure 6I illustrates the opening (*i.e.*, “trench”) after removing the sacrificial gate, which will also be present in the Lin-Brask combination.

sidewall and a bottom of the trench, which will also be present in the Lin-Brask combination.



5. 9[d]: forming a conductive layer to fill up the trench.

193. Lin in view of Brask renders obvious this limitation. For example, when Brask's gate-last process is combined with Lin as discussed above, the process will include blanket depositing a gate electrode material (*i.e.*, "a conductive layer") over the gate dielectric layer, as taught by Brask. Ex. 1006 at ¶ [0074]. Figure 6J of Brask, reproduced above, shows the gate electrode material 626 (orange) filling up the trench. Ex. 1006 at Fig. 6J. This gate electrode material filling up the trench will also be

present in the Lin-Brask combination, and forms the gate electrode of the transistor after planarizing. Ex. 1006 at ¶ [0074], Fig. 6K.

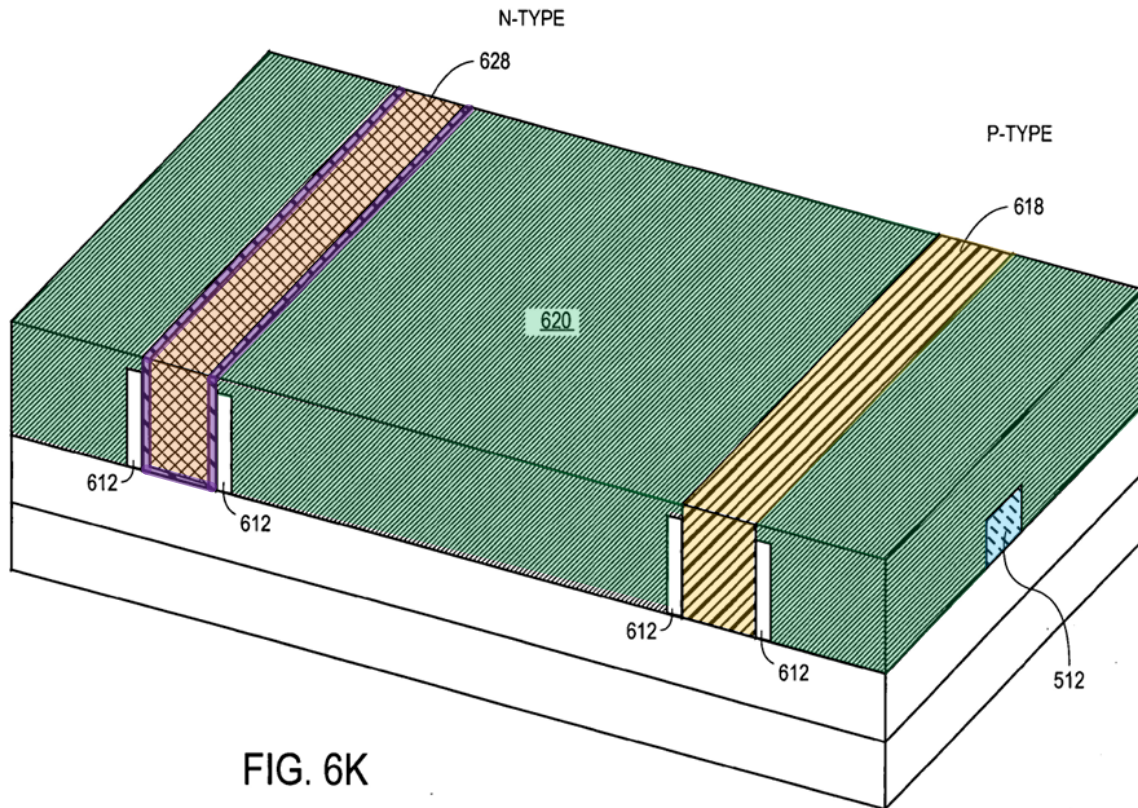


FIG. 6K

XI. Conclusion

194. As set forth above, it is my opinion that the Challenged Claims of the '384 Patent are unpatentable because they are rendered obvious by the prior art.

195. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within

the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

196. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent owner raises and to account for new information as it becomes available to me.

197. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: July 2, 2025

By: _____
Jack Lee, Ph. D.