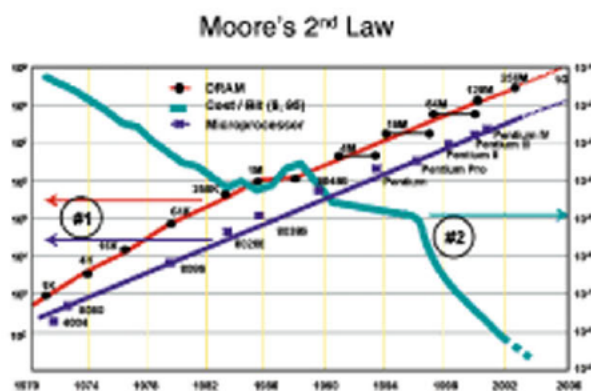


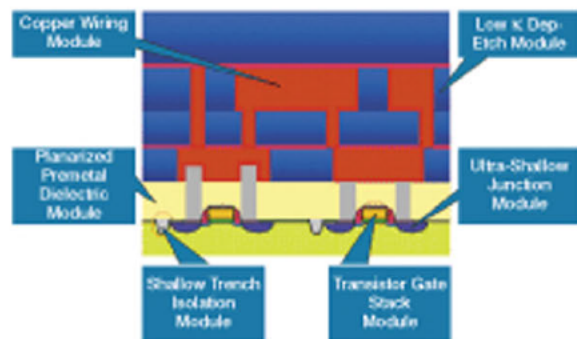


Interlayer Dielectrics

for Semiconductor Technologies



Edited by:
S. P. Murarka
M. Eizenberg
A. K. Sinha



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Preface

Electrically insulating materials form the dielectric films used in capacitors, the gate dielectrics in the metal–oxide–semiconductor field-effect transistors (MOSFETs), and the isolation between the electrical conductors used as contacts and interconnections (both on-chip and in packaging). Interlayer dielectric (ILD) materials play the role of isolating electrically conducting and semiconducting features and films. They also perform as masks against impurities, such as in selective-area diffusion, ion implantation, and impurities from the processing environment. More recently, they have also served as a stop layer for the chemical mechanical polishing of a metal on top of the ILD. Classically, silicon dioxide, deposited by chemical vapor deposition techniques, has been the preferred ILD material, both undoped and doped with phosphorus, boron, arsenic, and/or germanium. However, with the continued shrinking of the channel length of the MOSFET, the interconnect dimensions are also shrinking to accommodate an increasing number of devices. This has led to a serious interconnect-related circuit delay and to compromising the performance advantages of decreasing channel length. This delay, generally known as RC delay, is associated with the increasing interconnect resistance (R) and increasing ILD capacitance (C). Use of Cu as a replacement for Al has lowered R by about 40%. There is considerable effort expended, now, in lowering C by replacing SiO_2 (dielectric constant $\kappa = 4.0$) with lower- κ ILD materials.* This book, for the first time, puts together the science and technology of the ILD materials and associated processes in one volume, written by authors with experience in the field. It is, thus, an edited volume with 13 chapters written to cover the science, properties, and applications of different ILD materials, including silicon-based dielectrics, low- κ materials, such as polymers, porous materials, C and/or F doped silicon oxides, high dielectric constant materials, and those useful for wave guide applications in optical communications on the chip and the package. The book provides up-to-date knowledge with appropriate references for further reading and research. It is noted that the knowledge (both from materials and process points of view) about the SiO_2 -based dielectrics is thought to be more or less complete. However, the continued shrinkage in the dielectric film dimensions and the use of newer materials (e.g. Cu), which contact dielectrics, have led into much more stringent requirements and thus into newer domains of research and applicability determinations of SiO_2 as ILD and as gate oxide. As far as newer low- κ ILD materials are concerned, we know very little. Admittedly, the field of ILD materials, both low- κ and high- κ , is young and this book provides a up-to-date starting point. In Chapter 1, the subject of ILD is

*Both the symbols ' k ' and ' κ ' are used in literature for dielectric constant. Throughout the book, except chapters 7, 8, 10, and 11, symbol ' κ ' is used.

introduced with reference to the present and future semiconductor integrated circuit technologies and the challenges that lie ahead in the development of ILD materials and processes.

In Chapter 2, the properties of ILD materials are discussed in four groupings: electrical, mechanical, chemical and electrochemical, and thermal and thermodynamic. The chapter focuses on the properties of the ILD materials in particular emphasizing the impact of processing, actual use, and interactions with other materials that the ILD is in contact with. Many known and relevant properties are presented, for easy reference, in tabular format.

Chapter 3 focuses on ILD materials characterization techniques necessary in evaluating and thus in the development of low dielectric constant materials. Development of characterization techniques, with some emphasis on thermo-mechanical properties is discussed. Recently developed techniques used for porous dielectrics are included. Finally, an attempt is made to correlate molecular structure and materials properties, specifically using three classes of dielectrics, namely polymers, silsesquioxanes, and porous materials.

Chapter 4 examines the key interfaces and interactions between dielectrics and metals, dielectrics and semiconductors, and between different dielectrics for advanced semiconductor technologies, such as porous and dense dielectrics, organic, and silicon-based materials. The different methods for detecting interactions are compared. Modeling is presented as a method to predict interface reliability and the impact of material changes and interface modifications. The impact of dielectric interface properties on performance and reliability issues such as chemical mechanical polishing (CMP) compatibility, packaging reliability, as well as transistor performance, RC delay, and electromigration (EM) resistance, is also addressed.

Chapter 5 focuses on silicon-based deposited dielectric oxides, nitrides, and oxynitrides, and includes doped oxides. Deposition, resultant properties, and applications such as ILD are discussed.

Chapter 6 examines the status of polymer-ILD related work, with special emphasis on the role of the structure and its stability, preparation methods, interactions with surrounding materials, and adhesion. The discussion includes a brief presentation of polymer-chemistry related variations in the monomers and their polymerized (ILD films) products.

Chapter 7 covers CVD deposited amorphous carbon fluorides, a new group of low- κ materials. They contain C, F, H, and O and are shown to yield κ as low as 2.3. This chapter discusses the fundamentals, deposition, and properties of C-F films and issues related to integration of C-F films as an ILD in the advanced Si ICs.

Trapped air or inert gases can lower the κ very effectively. Chapters 8 and 9 explore a range of low- κ porous materials focusing on nanoporous silica xerogels as a benchmark. Preparation, defect-porosity characterization, properties, adhesion, processing, and interaction with metals have been critically examined and discussed. Tables and figures provide relevant data.

Chapter 10 diverts from the general thrust of the low- κ dielectrics. There is a serious need of high- κ dielectrics for applications such as capacitor and gate dielectrics and as isolation layers in packages. The dielectric constants of such materials range from 10 to >1000 . The key to their applicability lies in keeping leakage currents very low. This chapter examines such materials and their deposition with emphasis on atomic layer deposition (ALD).

The possibility of using photonic interconnects on-chip is being examined as a replacement for slower electronic (metallic) interconnects. An integral part of this photonic interconnect scheme is a guided wave system for the photon's propagation. The bit rate capacity or bandwidth of a passive waveguide is independent of its length for chip-level interconnects. Chapter 11 focuses on these guided wave systems. Applications of such systems are examined for a variety of cases, for example, on-chip, off-chip, and three-dimensional stacked chips. Materials characteristics, of both low- and high- κ materials are defined and examined.

Chapter 12 discusses the reliability of ILD materials used as insulating layers in a multi-level interconnection scheme. It focuses on considering all types of failure and the causes that affect the usefulness and the intended life of the ILD, thus of the device/circuit and on identifying and eliminating these causes. Standard modes of evaluation and prediction of the useful life are reviewed.

Chapter 13 examines the requirements for the continuation of CMOS scaling, both for high-performance logic and memory devices, and the implications for future process and material technology requirements, with emphasis on dielectrics.

Wherever the fast-moving semiconductor technologies take us, it is becoming obvious that new materials are needed for all types of applications. Manipulating the materials and their properties at atomic dimensions has become a must and a challenge at the same time. This book attempts to present the case of ILD materials with these thoughts in mind.

S.P. Murarka
M. Eizenberg
A.K. Sinha

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Chapter 1

Introduction: interlayer dielectrics in microelectronic devices

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The last few decades are frequently described as the solid-state electronics revolution era, the most significant technological revolution since the industrial revolution of the nineteenth century. Solid-state electronics has now totally engulfed our life, and its applications continue to grow at an unprecedented rate.

The most significant characteristic of the development and evolution of the solid-state electronics industry lies in the continuous miniaturization of the device dimensions in the circuit (expressed in The International Technology Roadmap for Semiconductors, 2001 [1]), leading to more components and more functions per area, as described by Moore's law (Fig. 1.1). This shrink and the efforts of the industry to abide by Moore's law are driven by two factors: the improved performance due to increased speed and more functions per unit area, and the lower cost per bit. Thus, the solid-state electronics of the 1960s evolved into microelectronics when typical lateral device dimensions reached the micrometer range. Now we are rapidly approaching the era of nanoelectronics as lateral dimensions are set to decrease below 100 nm (0.1 μm).

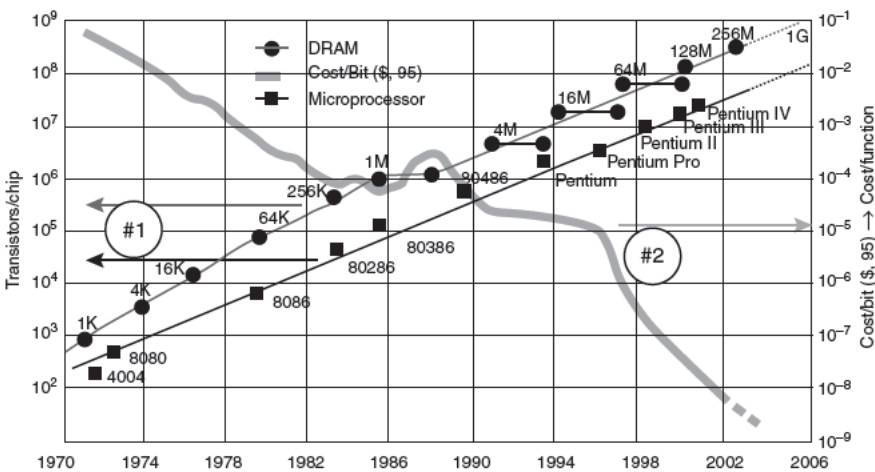


Fig. 1.1 Moore's law (Source: *Forbes* March 25, 1995 and *Applied Materials*, 1999).

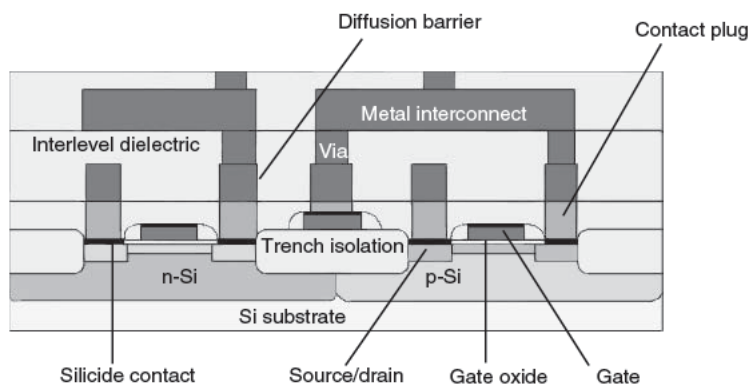


Fig. 1.2 Schematic drawing of a CMOS device.

Materials have played and will play increasingly a crucial role in this microelectronics revolution and evolution. The ability to produce devices with high performance, high reliability, and affordable price depends on the materials chosen and on our ability to process them in such a way that they will function in the desired manner during the device fabrication and in the actual use with a predicted reliability.

The core of a microelectronic device is the semiconducting material. Most of current microelectronic devices are based on silicon (Si), while some, especially the optoelectronic devices, utilize mainly III–V semiconductors such as GaAs, InP, and GaN. This book focuses on developments and trends in ultra-large-scale integrated (ULSI) microelectric devices, and therefore, by default, the semiconductor is Si (at this stage). The transistors and other active parts of the semiconductor are connected by horizontal and vertical conducting segments, mostly metallic (doped poly-Si is also used), that serve as the gate metallization, contacts, and metal interconnects that may consist of an adhesion promoter/diffusion barrier under and over the main current carrier metal, as illustrated in Fig. 1.2. Advanced microprocessors may consist of close to 10 levels of metallization, see Fig. 1.3.

The third-component of a device consists of the dielectric layers. These layers can be divided into three groups according to their function: (i) the active dielectric layers; (ii) the layers needed mainly during device processing; and (iii) the insulating layers.

The first group consists of dielectric films that play an active role in device operation, mainly for the storage of charge. These are the gate oxide and the capacitor dielectric in memory devices.

The second group consists of dielectric films that are needed during device processing. Examples are: (a) anti-reflection coatings (ARC) such as silicon nitride or carbide based layers used for the lithography step; (b) etch stop layers such as silicon nitride or carbide needed during the etching process and more recently during chemical mechanical planarization (CMP); and (c) masks against impurities, for example, metal ion getters, or layers introduced to enable

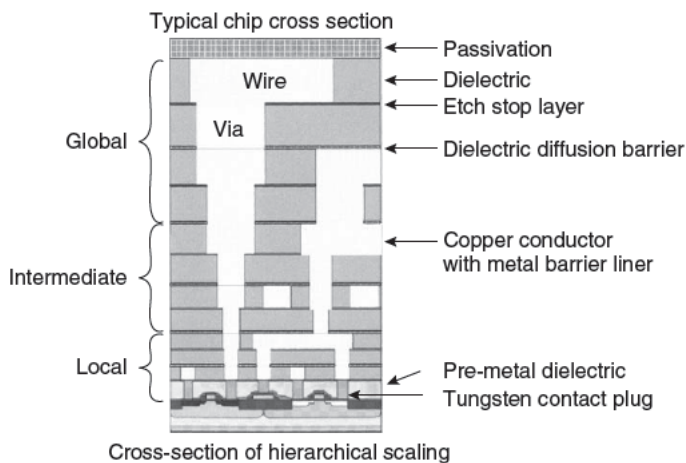


Fig. 1.3 Schematic drawing of a microprocessor with a hierarchical wiring approach for multilevel interconnects. (Copied from Ref. [1].)

selective area diffusion or ion implantation. Most of the layers described above do not have any specific role in device functioning after the completion of its processing. On the contrary, in many cases they affect, interfere, and even degrade the performance. This is the case, as an example, when the etch or CMP stop layer causes an increase in the effective dielectric constant of an interlevel dielectric layer (to be described below) that is desired to have the lowest possible dielectric constant, namely, to serve as a low- κ material.

The third group of dielectric films utilized in microelectronic devices consists of insulating layers. The isolation between two adjacent transistors is done by trench isolation (see Fig. 1.2), and when isolation of the device from the ambient is needed, a dielectric material is used as a passivation cap. The isolation between metal lines in the same level is carried out by an inter-metal dielectric, and that between two metal levels is performed by an interlevel dielectric. Both types are usually called interlayer dielectrics (ILDs).

The continued evolution of the microelectronics industry requires the introduction of new materials in order to accommodate the continued miniaturization (shrink in dimensions) with projected improvement in the performance. The latter is expected to continue even if at some point in time the shrink will stop due to economical reasons (might become too complicated and therefore too expensive) or due to physical limitations in device operation (e.g. reaching dimensions where quantum mechanical effects dominate, completely changing the nature of charge transport). The introduction of new materials necessarily requires simultaneous development of processes and studies that examine the compatibility of such materials in the surroundings of the device and the circuit. Simultaneously, other large number of new issues have emerged, all in response to interconnect (the metal and the dielectric) materials, structures, close proximity of

the vertical and horizontal interconnects, power dissipation, and the anisotropy of the dielectric constant. Note that we are heading into smaller and smaller volumes of material, which must be effective and reliable, defect-free with zero or very low stress, and with no or minimal chemical/metallurgical activity (since smallest amounts of matter will coexist in these structures). Such small volume or width or thickness requirements may lead to properties beyond present and naturally accepted values.

New materials have recently been introduced in microelectronic devices in the semi-conducting and metallic parts of the device. As new semiconductors, $\text{Si}_{1-x}\text{Ge}_x$ alloys, either grown epitaxially on the Si substrate or deposited as polycrystalline material, have now been introduced (yet in a limited extent) in order to enhance the charge carrier mobility. Also a dramatic change in the metallic materials is currently taking place. Cu is replacing the currently used Al(Si,Cu) alloys as the interconnect metal in order to increase the circuit speed, to enable operation at higher power levels, and to improve device reliability. Cu has lower electrical resistivity and better electromigration resistance than Al and its alloys. The replacement of the interconnect metal requires also a change in the use of the adhesion promoter/diffusion barrier, and thus TaN_x currently replaces TiN in this function. With further shrink, newer and thinner adhesion promoter/diffusion barrier materials are being sought to replace the current materials in this class. A less dramatic, but not less important, materials change is occurring in the silicides used for contacts, local interconnects, and gate metallization formed with a metal silicide on polysilicon. TiSi_2 is phasing out, being replaced by CoSi_2 , with the possibility of the introduction of NiSi or PtSi for some applications (which in the future might even be replaced by metal gates). All these materials changes practically skipped the dielectric part of the device. Silicon dioxide, in all respects, has been the ideal dielectric for use in Si-based devices and circuits. However, today its limitation, for use as an ILD, is mainly due to its high dielectric constant of about 4.

Now we are on the verge of a period when new materials will be introduced into the third component of the device materials: the dielectrics. The importance of this sector is increasing significantly, and in many aspects it has a critical role in limiting device performance. As device dimensions shrink, the switching speed of its basic element, the MOSFET (metal oxide silicon field effect transistor), is expected to increase, since the carriers transit time (for a given applied voltage) across the length of the channel is decreasing with the shrink of this dimension. However, the effective speed of the device is controlled not only by this intrinsic gate delay, but also by the speed of signal propagation to and from the device through the metal interconnects, the basic charge carriers. These are capacitatively coupled to the insulating dielectrics engulfing them, the ILDs, leading to a so called interconnect RC delay time. A simple model of the interconnects equivalent circuit is given in Fig. 1.4, where P represents the line pitch, W the line width, S the line spacing, T the line thickness, and the ILD line thickness above and below is equal.

The RC delay [2, 3] is given by:

$$RC = 2\rho \kappa \epsilon_0 (4L^2/P^2 + L^2/T^2), \quad (1.1)$$

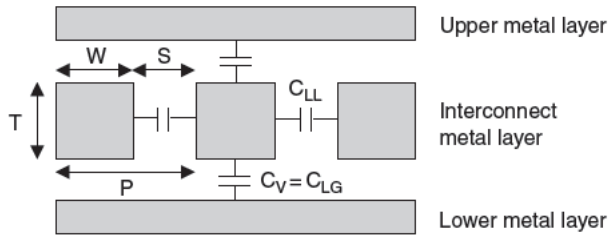


Fig. 1.4 Schematic diagram of a typical interconnect element. Subscripts LG and LL refer to the line-to-ground and line-to-line contributions. (Adapted from Ref. [2] © 1995 IEEE.)

where ρ is the metal resistivity, ϵ_0 the vacuum permittivity, κ the relative dielectric constant of the ILD, and L the line length. The decrease in features size results in a sharp increase in the RC delay time, which for devices smaller than $0.25\ \mu\text{m}$ controls the overall on-chip cycle time [2, 3]. Therefore, in order to increase device speed, the lower resistivity Cu is replacing Al (as discussed above), and the current ILD, SiO_2 (with $\kappa = 4$), will be replaced by other dielectrics with a lower dielectric constant (so-called low- κ materials). An additional reason for the search for the low- k dielectrics is the fact that power dissipation in a circuit is given by:

$$P = \left(\frac{1}{2}\right) f_d C V^2 f, \quad (1.2)$$

where C is the total on-capacitance, V the supply voltage, f the operational frequency, and f_d the fraction of gates that switch during a clock period. Reducing κ , thus C , will reduce the power dissipation, will make circuits faster, hence also more portable. The search for suitable low- κ dielectrics is currently the most important and urgent step. There are large number of choices being pursued by the researchers and the microelectronic industry. Thus, the subject of these new and experimental low- κ materials is covered in a significant portion of this book, Chapters 5–9.

The other need to introduce new dielectric materials is that of replacing SiO_2 as the dielectric material in gate and memory capacitors by materials with a higher dielectric constant, so-called high- κ dielectrics. The lateral shrink in device dimensions also requires scaling down the gate oxide thickness to a value which is approaching 1 nm. In such a thin layer of SiO_2 , leakage current will increase dramatically due to quantum mechanical tunneling. The problem can be avoided by using a thicker dielectric with a higher κ , still maintaining a capacitance equivalent to a 1 nm SiO_2 film. The drive to replace SiO_2 by a high- κ dielectric for the memory capacitor dielectric is due to the need to reduce memory cell size (especially in embedded memory microprocessors). The extremely small size of the capacitor results in a very small charge, too low to be reliable, especially for portable appliances based on a reduced operating/charging voltage. Replacing SiO_2 , with $\kappa = 4$, by a material with a very high κ value (in the range of 100 and even >1000) is important to enable the above discussed shrink of the memory cell size. These two implementations of high- κ dielectrics are discussed in Chapter 10 of our book.

The important role of dielectric materials is expected to increase beyond the scope discussed so far. First, the trend of increases in complexity and performance of devices can continue in spite of the fact that we are approaching the limits of miniaturization of lateral dimensions, by overcoming the difficulties and building three dimensional devices. Also Si transistors will be fabricated on top of an insulator (SOI), and the challenge lies both in the ability to overgrow high-quality Si as well as to control the properties of the underlying insulator. In parallel, efforts are taking place to improve performance by integrating the packaging on the chip. This trend may require adding insulators specific for the packaging process into the device processing sequence, with all possible interactions and limitations. And finally, in order to enhance device speed, optical interconnects may replace some of the current metal interconnects. Dielectric layers will be used in a role new to current Si devices: as optically active layers, waveguides, etc. The possible implementation of high- κ dielectrics for packaging and waveguide applications is discussed in Chapter 11.

This book intends to examine the science of dielectric materials relevant for microelectronic devices, as well as to review the current and future materials for the various applications. Special attention is given to the importance of the various interfaces between the dielectrics and the adjacent metallic, dielectric or semiconducting materials (Chapter 4). We must characterize as well as control these interfaces in order to prevent negative interactions and interferences during processing or operation. Characterization of the dielectrics, covering a very wide range of properties, is a real challenge that is discussed in depth in Chapter 3, but is also embedded in many other chapters. A special chapter is dedicated to the important issues of reliability (Chapter 12).

Although the book has focused mainly on our current knowledge of the properties, processing, and applications of dielectric deposited films in Si-based microelectronic devices, it also examines the future trends in this fascinating field of electrically insulating films made of inorganic, organic, mixed inorganic–organic, and porous materials. The book endeavors in raising some fundamental issues about the properties and use of such interlayer dielectric materials. Presently, finding functional ILD materials with κ less than 2 seems very difficult, and physics and chemistry of such materials in near-atomic-size applications are being examined to find the needed solution. A brief discussion of these scientific issues and hopes and some of our predictions (short term as well as long term) are summarized in Chapter 13.

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Chapter 5

Silicon-based dielectrics

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Abstract

Silicon-based dielectrics are the most widely used materials in the semiconductor industry. These include oxides (both doped and undoped), nitrides, oxynitrides, and carbides. Their applications span from the front-end device isolation steps to the back-end interconnect steps. This is due to their compatibility to the silicon substrate. In this chapter, we mainly focus on the deposited silicon-based dielectric films, and do not include the thermally grown silicon oxide or nitride films. The deposition techniques of Si-based dielectrics include both thermal and plasma assisted CVD. Their resultant film properties, including both mechanical and electrical properties, and their consequent applications in the semiconductor fabrication process are extensively discussed.

5.1 Introduction

During integrated circuit fabrication, dielectric layers are used for both active and passive functions. The active dielectrics are those used for charge storage in the transistor and capacitor, as well as those used for isolation between adjacent transistors and the metal lines. The passive dielectrics are those used in antireflection coating, dielectric diffusion barriers and caps, etch stops layer as well as passivation layers. Various chemical vapor deposition (CVD) techniques are used to deposit these films. They can be divided into thermal- and plasma-assisted CVD processes. Thermal CVD process include low-pressure CVD (LPCVD), atmospheric (AP) and sub-atmospheric (SA) CVD, while plasma-assisted CVD includes conventional low-density plasma-enhanced CVD (PECVD) and high-density plasma CVD (HDPCVD). This chapter describes the current methods used for depositing silicon-based dielectrics, their deposition chemistry, their resulting material properties, and their applications in semiconductor microfabrication.

5.2 Deposition techniques

5.2.1 Thermal chemical vapor deposition process

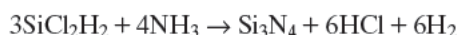
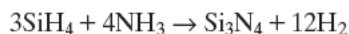
5.2.1.1 Low-pressure chemical vapor deposition

This technique is also referred to as thermal CVD, due to its high-temperature process. The dielectric deposition is typically carried out in a tube furnace. A vertical furnace is commonly used today, although the industry has moved towards a single-wafer reactor as shown in Fig. 5.1.

The vertical furnace typically consists of a quartz tube, heated by a three-zone heater, with gas introduced from the bottom of the tube and exhausted on top. The wafers are held and stacked vertically on a quartz boat across the length of the tube. Typical operating pressure range between approximately 200 mTorr and 2 Torr.

Individual gases are introduced into the chamber through a shower head and mixed inside the chamber, the wafer sits on top of a resistive heater, and at the bottom a nitrogen purge is introduced to prevent reactant gas and particle buildup in the lift pin area, which is used to lift the wafer for transport. Typical operating pressure ranges between 10 and 200 mTorr. High-temperature silicon oxide and nitride films, which are typically used in the front-end process for the fabrication of the transistor and capacitor device layers, are most commonly deposited by these techniques.

Silane and ammonia are typically used to deposit silicon nitride (Si_3N_4) film at temperatures between 700 and 800°C, although dichlorosilane is more commonly used today. The chemical reactions are:



Si_3N_4 deposited by conventional high-temperature LPCVD techniques is typically stoichiometric, has good uniformity and film quality. The LPCVD Si_3N_4 film is typically denser than plasma-deposited Si_3N_4 and has lower H content.

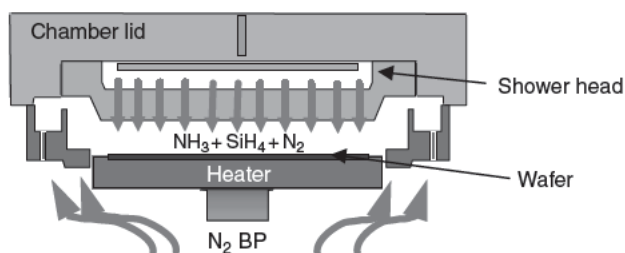


Fig. 5.1 A single-wafer LPCVD reactor.

The key advantages of a single-wafer reactor process compared to that of a batch furnace are: (a) lower thermal budget, which becomes more important with device shrinks; (b) uses non-chlorine chemistry for thermal nitride deposition, that is, SiH_4 chemistry is used in a single-wafer reactor while dichlorosilane is typically used for furnace processes, this could cause the incorporation of unwanted Cl into the film, which may react with polysilicon and cause film cracking; and (c) better particle performance, which affects device yield. Some of the disadvantages observed with the film deposited from a single-wafer reactor compared to the furnace are: (a) higher H content, which may affect charge storage properties; (b) film uniformity across the wafer; and (c) pattern loading effect.

Some of the applications for these high-temperature oxide and nitride films include chemical mechanical polish (CMP) stopping layer for shallow trench isolation, oxide hard mask for deep trench etch in DRAM capacitor, sidewall spacer for capacitor isolation in DRAM devices, as well as for salicide formation in logic devices. These will be illustrated in Section 5.4.

5.2.1.2 Atmospheric (APCVD) and sub-atmospheric chemical vapor deposition (SACVD)

In a typical atmospheric reactor, wafers lie on top of a horizontal heater with reactive gases flowing over the substrates at atmospheric pressure, that is, 760 Torr. In an APCVD batch reactor, multiple wafers rest on top of a large ‘pancake’ heater and are processed at the same time. In a continuous reactor, wafers are transported through the reactor on a conveyer belt. Inert gas curtains around the outer edge of the reactor are used to contain the reactive gases.

The typical hardware for SACVD is similar to that of a single-wafer LPCVD reactor discussed above. The operating pressure of the SACVD process ranges from 20 to as high as 600 Torr; hence, ‘Sub-atmospheric’.

SACVD is generally preferred over APCVD for PMD applications since it offers better particle performance without using high-flow inert gas curtains and higher productivity, allowing a larger number of wafers to be processed in the reactor before a wet clean is needed.

5.2.2 Plasma-assisted chemical vapor deposition

5.2.2.1 Plasma-enhanced chemical vapor deposition

After the first metal layer has been deposited, conventional LPCVD processes, which are typically of higher temperatures (i.e. $> 450^{\circ}\text{C}$), can no longer be used because they will melt the metal, cause hillocks or electromigration problems. Any subsequent deposition must be done at low temperature (less than 450°C). In order to accomplish this, an electrically charged gas, called plasma, is used to provide the energy for the deposition reaction. The plasma density of PECVD is typically low. A typical single-wafer PECVD reactor is shown in Fig. 5.3.

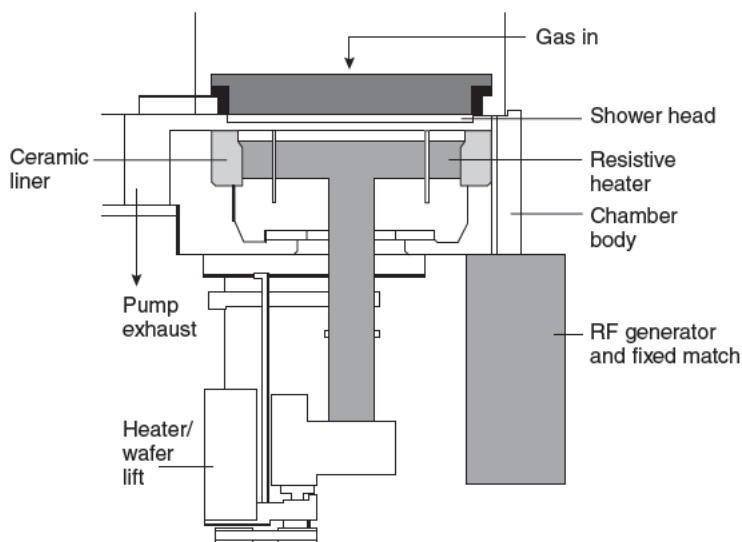


Fig. 5.3 A typical PECVD chamber.

This chamber is also called a ‘cold wall’ reactor since the chamber body is usually maintained between 60 and 70°C. The substrate is placed on a heater made of either aluminum or ceramic and heated to a temperature of around 400°C. The heater and the chamber wall are grounded electrically whereas the showerhead is the powered electrode. The process pressure is relatively low, in the 0.5–15 Torr range. After the gas flows and the pressure is stabilized, radio-frequency (RF) energy is applied to the chamber to generate a plasma, ionizing the reactive gases. One of the advantages of plasma-enhanced deposition is that the wafer temperature can be maintained relatively low. Conventional LPCVD processes usually require temperatures substantially higher and are not suitable for certain substrate materials such as aluminum or copper. Typically, RF at 13.56 MHz is used for generating the plasma, although in some cases mixed frequencies of 13.56 MHz and 450 kHz are used to control film stress and other film properties.

5.2.2.1.1 Oxides

5.2.2.1.1.1 Undoped silicon dioxide and fluorosilicate glass

Two common precursors used to form PECVD USG and FSG are silane (SiH_4) and TEOS.

SiH_4 USG is formed by the reaction of SiH_4 with nitrous oxide (N_2O) over a substrate temperature of ~400°C in the presence of plasma. Since SiH_4 and N_2O are fairly reactive, only a low RF power (~300 W) is needed to sustain the plasma. On the other hand, since the reaction is in the flow-limited regime, sufficiently high SiH_4 flows and pressure (in the Torr range) are necessary to achieve a high deposition rate. Silicon tetrafluoride, SiF_4 , is used as the precursor for fluorine in the FSG deposition.

TEOS is a liquid precursor that has been used for high-temperature oxide deposition in furnaces since the 1960s. [1, 2]. TEOS oxide has been known to have more conformal step coverage than SiH_4 oxide even over high aspect ratio structures [3]. The challenge is to deposit TEOS-based USG at a low enough temperature so that the film can be used as an inter-metal dielectric.

Starting at the 0.18 μm and below technology node, the gap fill requirement for aluminum interconnect has become too stringent for conventional PECVD techniques, even with TEOS USG, to achieve satisfactory results. Hence, device manufacturers have shifted to a different gap fill technology called HDPCVD, which will be discussed later in the chapter. PECVD TEOS films are then used as capping layers over the HDPCVD films, where the step coverage requirements are much less stringent. SiF_4 is also used as the fluorine precursor for TEOS FSG.

5.2.2.1.1.2 Carbon-doped oxide

Carbon-doped oxide (CDO), also known as organosilicate glass (OSG) or silicon oxycarbide (SiOC), can be deposited in a parallel-plate PECVD chamber. Various precursors have been used to deposit CDO films, including methylsilane, dimethylsilane, trimethylsilane (TMS) [4], and tetramethylsilane (4MS). Precursors with more methyl groups are capable of incorporating more carbon into the film, though the compounds are more difficult to dissociate. Therefore, 4MS, a liquid precursor, in general, deposits at a lower rate than that of TMS, which is a gas.

Other precursors such as tetramethylcyclotetrasiloxane (TOMCATS), octamethylcyclotetrasiloxane (OMCTS) [5], dimethyldimethoxysilane (DMDSO) [6] have also been demonstrated in CVD of CDO films.

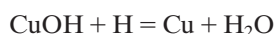
TMS and O₂ chemistry has been the most widely accepted method for depositing CDO film thus far due to the industry familiarity with the precursors and its simple gas-delivery system. TMS and O₂ are typically introduced into the chamber through separate gas lines, with or without carrier gases, in order to prevent any pre-mature reaction before they reach the chamber. Deposition temperature is usually kept below 400°C, preferably at around 350°C, since the dielectric is used between metal layers.

5.2.2.1.2 Nitrides (SiN)

Plasma-deposited silicon nitride has been widely used in microelectronic device fabrication for years. The applications include final passivation layer, diffusion barriers against mobile ions, and moisture barriers. Recently, silicon nitride film applications have been extended to advanced dual damascene processing, such as copper diffusion barrier and middle etch stop due to the film's excellent barrier properties against copper and the high etch selectivity to low- κ dielectric films.

Copper oxidizes readily in air. Therefore, before silicon nitride is deposited over copper, the native copper oxide must be removed first. A plasma treatment consisting of a hydrogen containing a gas such as ammonia (NH₃) is typically used to reduce the copper oxide to metallic copper in PECVD chambers [7].

The reaction of ammonia gas with copper oxide is as follows:



After the CuO removal step, SiH₄ is introduced to the chamber to react with ammonia, forming silicon nitride. It has been found that copper will start reacting with SiH₄ at temperature as low as 200°C. After CuO has been removed, if copper is exposed to an environment with high concentration of silane, copper silicide will be formed. It is known whether uncontrolled copper silicide formation on the copper surface increase the resistivity of copper inter-connections and degrades the adhesion of barrier layer. Very often, people refer copper silicide to as 'green' or 'black' copper.

5.2.2.1.3 Oxynitrides (SiON)

A typical single-wafer PECVD reactor with a 400°C heater is used for SiON deposition. A gas mixture of SiH₄ and nitrous oxide (N₂O) is introduced into the process chamber before high-frequency RF power is applied.

In addition to SiH_4 and N_2O , sometimes helium or nitrogen can be added to the reaction for various reasons. In the pressure and spacing regime the PECVD SiON process operates, helium requires a lower breakdown voltage than nitrogen [8]. Since helium is easier to breakdown, it helps to stabilize the plasma during deposition.

After SiON deposition, the film surface is treated by either capping the film with a very thin layer of silicon oxide or striking an oxygen-containing plasma to oxidize the SiON surface. The purpose of the treatment step is to prevent any interaction between the SiON film and the photoresist, causing ‘poisoning’ problems. Detailed discussion on poisoning will be covered in Section 5.4.

5.2.2.1.4 Silicon carbide

Silicon carbide is typically deposited in a parallel-plate PECVD reactor at around 300–400°C. Sometimes, the same chamber can be used for CDO deposition also. Since silicon carbide is also deposited over copper, a copper oxide removal step similar to that used for silicon nitride is also required prior to silicon carbide deposition. A similar chemistry involving ammonia and/or hydrogen is also used to reduce the native copper oxide.

TMS and 4MS are common precursors for depositing silicon carbide. Sometimes, helium and ammonia gases are added during the process to stabilize the plasma and improve the hardness of the film. However, using ammonia also incorporates nitrogen in the film, resulting in higher dielectric constant (~ 5) and resisting poisoning issues with 193-nm lithography than the film without nitrogen. Therefore, silicon carbide films for low- κ applications are also known as SiCH or SiCHN, depending on whether the precursors contain nitrogen or not. To further ensure good adhesion of SiCH to CDO, helium plasma treatment is sometimes performed on the wafer after film deposition.

5.2.2.2 High-density plasma chemical vapor deposition

Starting at the 0.18 μm and below technology node, the aspect ratio for gap fill requirement has become more and more challenging for PE TEOS USG to fulfill. Device manufacturers have shifted to a different gap fill technology called HDPCVD, which utilizes a new concept of depositing and sputtering at the same time to successfully fill the high aspect ratio gaps. (Fig. 5.4)

The key difference between an HDPCVD chamber (Fig. 5.5) and a conventional CVD chamber is that it simultaneously deposits and sputters in the same chamber. High-density plasma generates more ions and gives more directional deposition. It also yields higher sputtering rates.

Therefore, an HDPCVD chamber is designed with these objectives in mind. Key hardware components of the chamber include a turbo pump, RF power delivery (source and bias), gas distribution, monopolar or bipolar electrostatic chuck (ESC), and helium cooling.

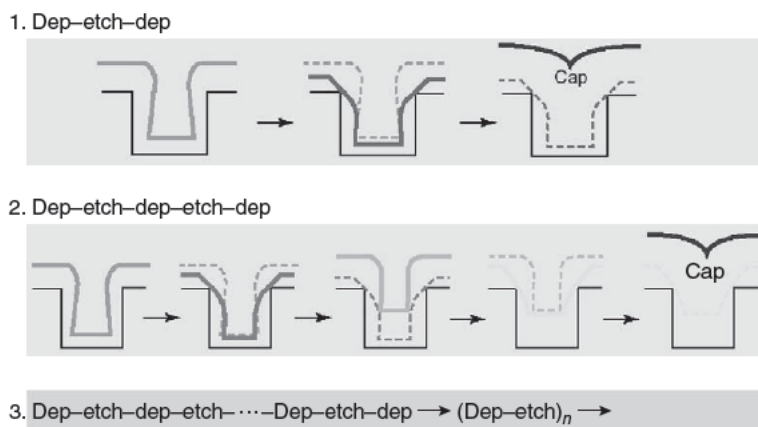


Fig. 5.4 Dep/etch concept of HDPCVD.

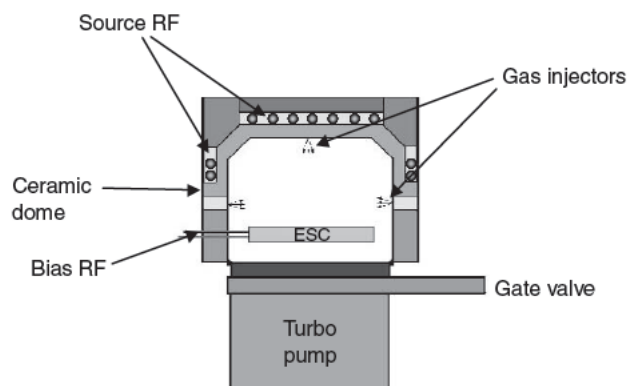


Fig. 5.5 Schematic of an HDPCVD chamber.

The dome and process kit components are made of ceramic mainly due to the requirements of low mobile ion contamination. In addition, the dome has to be made of dielectric material in order to allow the coils to couple into the chamber for high-density plasma generation. The turbo pump enables the chamber to operate in the 2–10 mTorr range. Low pressure is necessary to lengthen the mean free paths of the ions that are responsible for high sputter etch rates.

The bias RF generator delivers capacitively coupled energy to the ESC for sputtering whereas the source RF delivers inductively coupled power to the chamber through the coils and the dome and provide directional deposition.

Gases are delivered to the chamber through injectors that are distributed around the dome to provide uniform and symmetrical gas dispersion. Silane and oxygen are introduced separately into the chamber to prevent any undesirable upstream reaction. Argon is used to enhance the sputtering component. The ESC holds the wafer to allow helium backside cooling without mechanical clamping. Helium cooling is critical since wafer temperature could reach

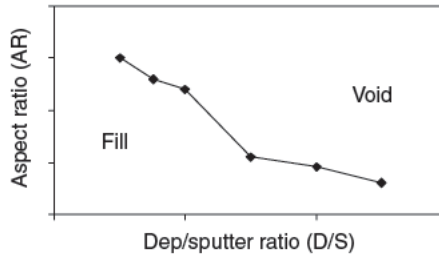


Fig. 5.6 Gap fill window as a function of D/S ratio and aspect ratio.

over 400°C during deposition and it is essential to conduct heat away from the wafer to avoid damage to the devices. Electrostatic chuck clamping is preferred over mechanical clamping since it provides much better particle performance.

Since HDPCVD is a combination of deposition and sputtering at the same time, proper deposition to etch ratio is required in order to achieve optimal results. Too much deposition and too little sputtering will generate cusping of deposited oxide, resulting in poor gapfilling and formation of voids. Too much sputtering relative to deposition can result in corner-cutting in the underlying film, either in the metal or the anti-reflective coating layer on top of the metal, which in some cases can cause leakage currents and device failure. Therefore, a balance between deposition and sputtering has to be established. The ratio between the two rates is called the D/S ratio, which has to be adjusted depending on the underlying topography and aspect ratio of the gap. The effect of different D/S ratios is shown in Fig. 5.6. In general, the higher the aspect ratio, the lower the D/S ratio required to fill the gap void free.

Sputtering is the result of ions bombarding the surface. As ions accelerate to the substrate, any collisions that occur will cause energy to be lost due to elastic/inelastic collisions. By minimizing the chamber pressure, the mean free path between collisions is increased and, therefore, minimal energy is lost. In addition, argon, which is a heavy ion, is used in HDP to enhance the sputtering rate.

HDPCVD can also be used to deposit FSG and PSG. Similar to PECVD, SiF_4 and PH_3 are used as precursors for fluorine and phosphorus, respectively.

5.3 Properties of Si-based dielectrics

5.3.1 Oxides

5.3.1.1 Undoped silicate glass

All three deposition methods, that is, PECVD, HDPCVD, and SACVD, can be used to form USG. However, some properties of the resulting USG films could be very different, depending on which deposition technique is used.

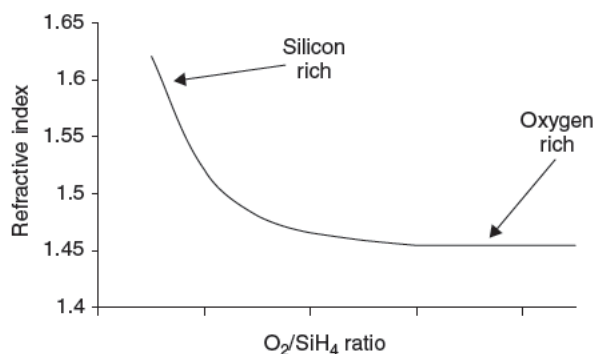


Fig. 5.7 Refractive index as a function of O_2/SiH_4 ratio.

The dielectric constant of CVD USG films is around 4.0 ± 0.2 whereas the refractive index (RI) is typically at 1.46 ± 0.005 . However, silicon-rich films with refractive index of 1.5 can be achieved by lowering the flow ratio of the silicon precursor such as SiH_4 to the oxygen precursor such as N_2O . On the other hand, a perfectly stoichiometric film with an RI of 1.46 can also be achieved by adjusting the flow ratio (Fig. 5.7).

Fourier transform infrared (FTIR) spectra of a stoichiometric oxide film and a Si-rich oxide film show no Si-H peak at 2250 cm^{-1} and a significant Si-H peak, indicating that Si dangling bonds might be present in the Si-rich film. These dangling bonds are highly polarizable and therefore are responsible for the high refractive index.

The film stress is typically compressive for HDP and PECVD oxide, in the range of $1\text{--}2 \times 10^9$ dyn/cm² while that for SACVD USG films is usually tensile. Both the HDP and PECVD oxide films demonstrate minimal changes after thermal anneal whereas SACVD oxides shrink and densify after thermal treatment.

Wet etch rate of CVD films in a buffer oxide etch solution is commonly used to measure relatively how dense the oxide films are when compared to thermally grown oxides. Although HDP, PECVD, and SACVD oxides are not as dense as thermally grown oxides, the wet etch rate ratio (WERR) of CVD oxides to thermal oxides is still less than 2.

Deposition rates vary in great degrees depending on which deposition technique is used. Over $1\text{ }\mu\text{m/min}$ deposition rate is readily achievable for PECVD oxides whereas up to $5000\text{ }\text{\AA}/\text{min}$ is more likely found in HDP- and SACVD oxides.

Absence of metallic contamination is extremely critical when HDP- and SACVD oxides are used in the front-end applications. Since HDPCVD chambers perform gap fill by depositing and sputtering simultaneously, the chamber is more susceptible to metallic contamination. Therefore, the process kit in the HDPCVD chamber is typically made of ceramic in order to achieve a metallic contamination level below 5×10^{10} atoms/cm³. Since the SACVD process is strictly a thermal one, low metallic contamination can easily be accomplished.

5.3.1.2 Fluorosilicate glass

Fluorine ions are very electronegative. When fluorine is bonded to the Si-O structure, electrons from the Si-O bond are drawn towards the electronegative fluorine side. This electron shift weakens the Si-O bonds and makes the entire oxide structure less polarizable, resulting in a lower dielectric constant. However, weakening of the Si-O bonds also reduces the hardness and mechanical strength of the FSG film. Furthermore, the hydrophilic nature of fluorine tends to increase the moisture absorption of the oxides. After the film has been exposed to a wet environment such as CMP, formation of hydrofluoric acid (HF) could possibly corrode the adjacent metals and cause adhesion problems. The maximum amount of stable fluorine incorporation is about a 6–8% for the inter-metal dielectric application. Regardless of the fluorine content, process optimization is required in order to achieve stable FSG films. The flow ratio of SiF_4 to silicon precursor has the strongest effect on the amount of fluorine in the resulting FSG film. Increasing SiF_4 flow decreases refractive index, and increases fluorine concentration. The relative fluorine concentration can be determined by the ratio of the peak heights of Si-F at $\sim 937\text{ cm}^{-1}$ and Si-O at $\sim 1081\text{ cm}^{-1}$ using FTIR spectroscopy as shown in Fig. 5.8.

Thermal Desorption Mass Spectroscopy (TDS) analysis can be used to study properties of FSG films (Fig. 5.9). When the film is heated to 800°C , any unstable species will start desorbing out of the film and species such as fluorine (F), water (H_2O), hydrogen (H_2), and hydrogen

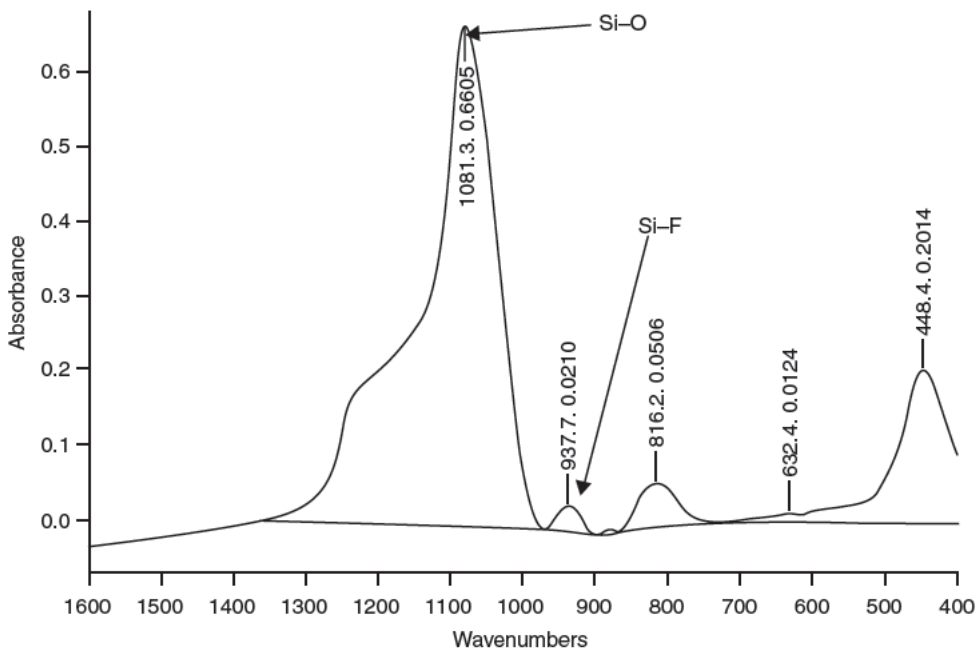


Fig. 5.8 FTIR of FSG film.

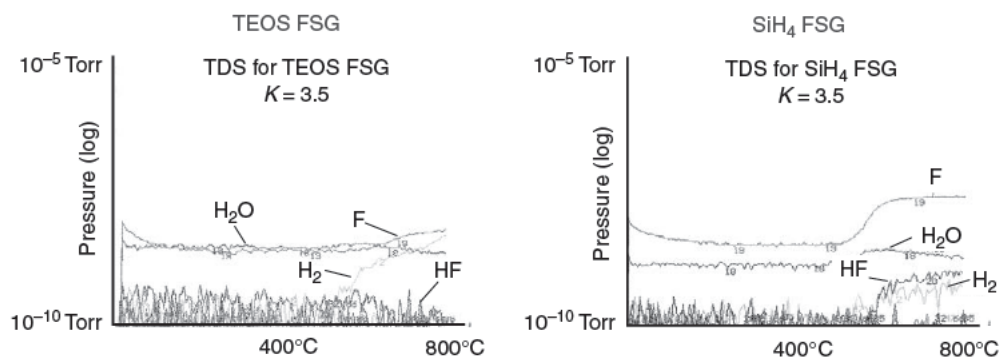


Fig. 5.9 FSG film stability analysis by thermal desorption spectroscopy.

fluoride (HF) can be detected using mass spectroscopy. The silane FSG (right) shows that F, HF, and H₂O start to out-gas at 500°C whereas the TEOS-based FSG (left) shows no F, HF, or H₂O evolution up to temperatures of 800°C (Fig. 5.9).

5.3.1.3 Phosphorus silicate glass

PSG has good gettering properties that remove metallic contaminants such as mobile ions from the devices so that no potential damage occurs. Typical phosphorus dopant concentrations range from 2 to 9 wt%. PSG films with phosphorus concentrations higher than 6% are usually less stable and more hygroscopic, potentially reacting with moisture in air and forming phosphoric acid. The peak height of the FTIR absorption band at 1330 cm^{-1} (P=O) can be used to quantify the phosphorus amount. In general, higher dopant concentration results in higher deposition rate and higher wet etch rate. SACVD PSG films tend to be less stable and need to be densified at high temperature in order to convert the unstable P_2O_3 to P_2O_5 completely.

5.3.1.4 Borophosphosilicate glass

Boron concentrations in BPSG range from 2 to 6 wt% whereas phosphorus concentrations range from 2 to 9 wt%. Properties of BPSG, deposited with the SACVD method are sensitive to TEOS flow and deposition temperature, as shown in the Table 5.1.

Since the operating regime of SACVD is TEOS flow limited, increasing TEOS flow will increase deposition rate but at the same time lower the dopant to TEOS flow ratio, therefore lowering the resulting boron and phosphorus concentration in the film. Higher deposition temperature yields a denser film with more dopant incorporation.

BPSG films have as-deposited tensile stress at less than $1 \times 10^{10} \text{ dyn/cm}^2$. Since the step coverage of as-deposited BPSG is not sufficient to fill the gap, the film has to be thermally

Table 5.1 Effect of TEOS flow and temperature on deposition rate and dopant concentrations

Parameter	Deposition rate	B%	P%
TEOS flow ↑	↑	↓	↓
Temperature ↑	↓	↑	↑

Table 5.2 FTIR absorption bonds in BPSG

Bond	Wavenumber (cm ⁻¹)
P=O	1330
Si-O	1050
B-O	930, 1350

annealed either in a furnace or a rapid thermal processing (RTP) chamber to flow the glass. Annealing the film also densifies it and makes it shrink.

Boron oxides have two FTIR absorption bands, that is, the B-O bond at 1350 cm⁻¹ and the Si-O-B bond at 930 cm⁻¹. Determining the boron concentration is straightforward, that is, by evaluating the peak at 930 cm⁻¹. However, measuring the phosphorus concentration in BPSG is more tricky since the P=O peak at 1330 cm⁻¹ overlaps with the B-O peak at 1350 cm⁻¹ and the two peaks must be deconvoluted. The different absorption bands in BPSG are summarized in Table 5.2.

5.3.1.5 Carbon doped oxide

CDO, also known as SiOC and organosilicate glass (OSG) has a dielectric constant, κ value, between 2.2 and 3.0. The lower κ value is achieved by introducing porosity to the films through the incorporation of methyl groups. CDO films have a composition of Si_wC_xO_yH_z with about 10–25% of the silicon atoms substituted with organic groups [9]. However, these methyl groups also affect other physical, thermal, and chemical properties of the CDO films [10].

Although CDO films are not as good as silicon dioxide films, they have many of the beneficial thermal and mechanical properties of silicon oxide. Table 5.3 shows a comparison of the properties between CDO and oxide.

CDO is a mixture of pores and the solid phase. Since pores are made of air with a dielectric constant of 1, the presence of pores in a solid material can lower the effective dielectric constant. Measurement of porosity allows one to understand the correlation between pores and the solid phase and therefore the dielectric constant.

The dielectric constant, κ , of the CDO film can be derived as

$$\kappa = (1 - P)\kappa_0 + P\kappa_{\text{air}} = \kappa_0 - (\kappa_0 - \kappa_{\text{air}})P$$

Table 5.3. Flim properties' comparison between CDO and SiO₂

Mechanical properties	CDO	PECVD SiO ₂
Dielectric constant	< 3.0	4.2
Refractive index	< 1.42	1.46
Stress	Tensile	Compressive
Hardness	< 2.0 GPa	7–9 GPa
Young's modulus	< 10 GPa	70–80 GPa
Mass density	< 1.4 g/cm ³	2.2 g/cm ³
Thermal conductivity	< 0.4 W/mC	~1 W/mC
Coefficient of thermal expansion	< 10 ppm/°C	< 1 ppm/°C

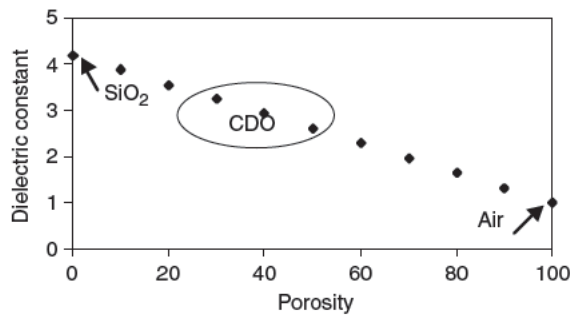


Fig. 5.10 A plot of dielectric constant as a function of porosity.

where κ_0 is the dielectric constant of SiO₂ at a value of 4.2 and P is the porosity. Since $\kappa_{\text{air}} = 1$,

$$\kappa = \kappa_0 - (\kappa_0 - 1) P$$

Porosity can be calculated according to the following formula: $P = 1 - D/D_0$, since D , the density of CDO film and D_0 , the density of the oxide can be calculated by measuring the mass of the film using a microbalance and thickness of the film using a stylus.

A plot of κ versus P is shown in Fig. 5.10. Empirical results show that if CDO has a porosity of about 40%, the equivalent κ value should be around 2.9, which agrees with the actual measured κ value by a mercury probe.

As the device geometry continues to shrink, spacing between metal lines becomes narrower and it becomes even more critical for the dielectric material to conduct heat away from the metal lines, especially on the top metal layers. CDO materials have good thermal conductivity, allowing heat to be dissipated effectively. Since the coefficient of thermal expansion (CTE) of CDO is similar to that of copper, it will help prevent cracking and peeling due to thermal mismatch between the dielectric and copper. Some low- κ materials, such as organic spin on dielectrics, have very low thermal conductivity and high CTE, making the material difficult to

integrate into the device scheme. Figure 5.11 shows the similarities and differences between USG, CDO, and spin-on type materials.

If the CDO film is to be used on all the metal layers throughout the device, the mechanical strength of the film has to be able to withstand cracking resistance tests, the abrasive chemical mechanical polish, and pressure from the final packaging processes. Since CDO films have a substantial amount of pores, they also have lower hardness and modulus of elasticity. However, when compared to spin-on type of materials, CDO films are at least an order of magnitude stronger. Figure 5.12 shows the comparison.

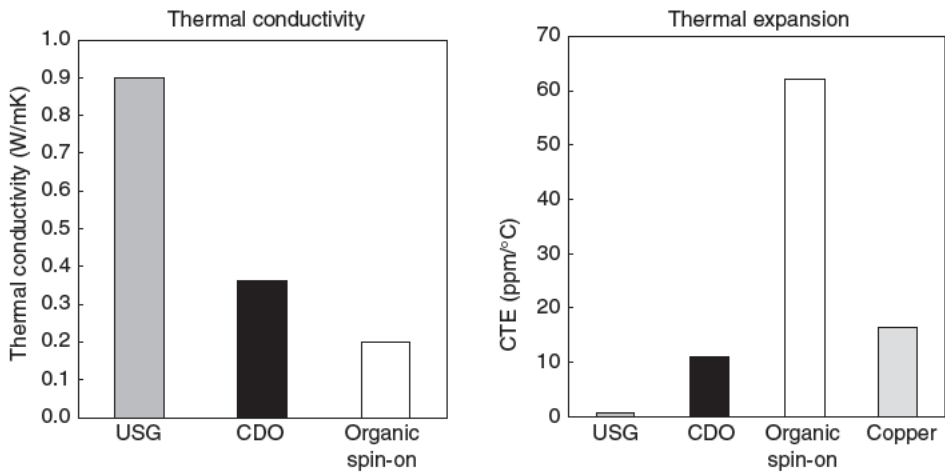


Fig. 5.11 Comparison of thermal properties between USG, CDO, and organic spin-on materials.

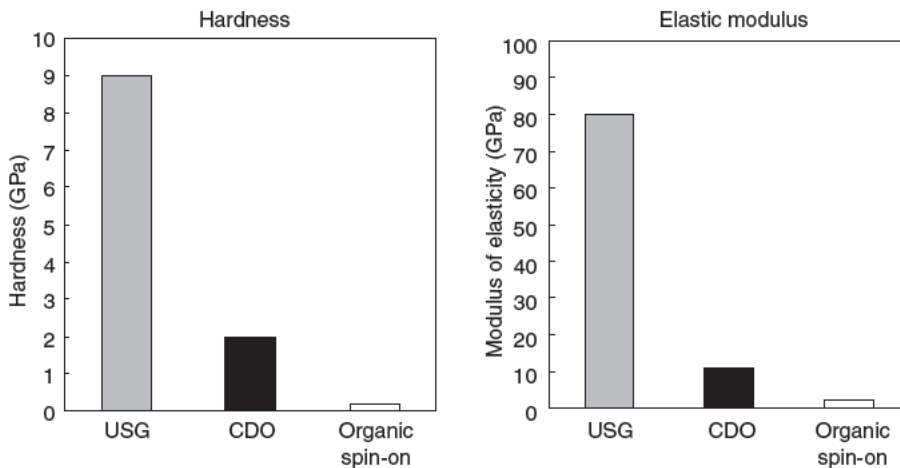


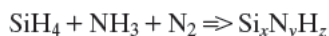
Fig. 5.12 Comparison of mechanical properties between USG, CDO, and organic spin-on materials.

5.3.2 Nitrides (SiN)

Silicon nitride films have been known for their moisture barrier properties and the high resistance to fluorine etch chemistries, compared to silicon oxides. Recently, SiN films have also been found to be excellent candidates for copper diffusion barriers and etch stop layers in dual damascene applications.

A good copper diffusion barrier should have minimal O₂ content (less than 2 at%). This is because nitride films with higher oxygen content are known to be more leaky electrically and chemically. The RI of the nitride film is a good indicator of the oxygen content in the film. The RI of a stoichiometric SiN film is around 2.0–2.1. When more oxygen is present in the film, the RI decreases since pure SiO₂ has a value of 1.46. Figure 5.13 gives the comparison of the RI versus O₂ content for a nitride film, measured by the X-ray photoelectron spectroscopy (XPS) technique. While very low RI would make a poor diffusion barrier, very high RI indicates that the film is silicon rich; and it is well known that copper can diffuse through a silicon-rich nitride film very easily.

The nitride reaction is expressed as



where x , y , and z are determined by different process parameters and hardware configurations. If only N₂ or no NH₃ is used in the process, very low hydrogen content can be obtained. There are still some hydrogen in the film since SiH₄ is still a source of hydrogen. When a high NH₃/N₂ flow ratio is used, up to 25% hydrogen can be incorporated into the film.

N–H bonds are stable and hence are difficult to break. Therefore, low hydrogen content can be achieved by hardware that breaks down the ammonia molecules completely so that only a minimal amount of hydrogen is left bonded to the nitrogen atoms.

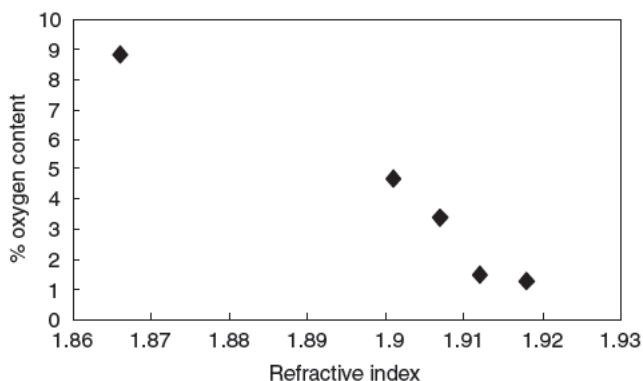


Fig. 5.13 A plot of correlation between oxygen content and refractive index of silicon nitride films.

Silicon nitride can also be deposited using HDPCVD with silane, nitrogen, and argon chemistry. The resulting film has very low hydrogen content also. However, since the cost of operating HDP is much higher than that of PECVD, HDP is not a popular method of producing silicon nitride films.

Hydrogen can be measured using techniques like nuclear reaction analysis (NRA), Rutherford backscattering spectroscopy (RBS), and hydrogen forward scattering (HFS). However, these methods are time consuming and expensive and therefore FTIR is the more economical method for measuring hydrogen content. Hydrogen is bonded to both Si and N forming Si-H and N-H bonds, respectively. N-H bonds are more stable than Si-H bonds due to the larger bond strengths, that is, 388 kJ/mol for N-H and 318 kJ/mol for Si-H. Therefore, it is undesirable to have Si-H bonds in the film since they can break loose during thermal anneal and form free hydrogen that causes problems. FTIR analysis can qualitatively measure the hydrogen content and at the same time distinguish the difference between hydrogen that is bonded to Si or N. A comparison between different nitride films with different reactor configurations and chemistries using FTIR is shown in Fig. 5.14. PE SiN A is deposited using no NH_3 and therefore has the minimum Si-H bonding whereas the other PE SiN films with high NH_3 flows have more significant Si-H bonds. HDP SiN also has very low hydrogen content.

Hydrogen content is the most important factor causing adhesion issues between SiN and FSG. Fluorine in the FSG tends to react with hydrogen in the nitride forming HF. One way to reduce the problem is to use an FSG with stable fluorine. Another way is to use a nitride film with very low hydrogen content. Of course, the best combination would be to use both.

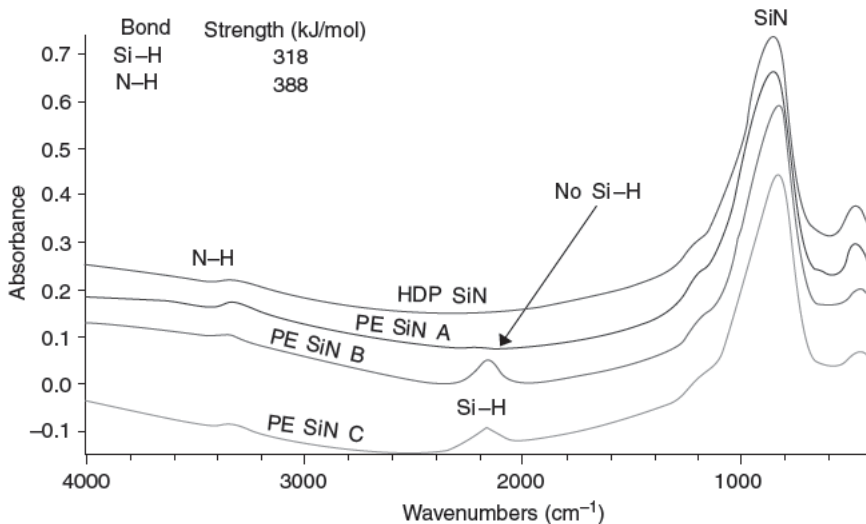


Fig. 5.14 FTIR spectra of silicon nitride films with different hydrogen content.

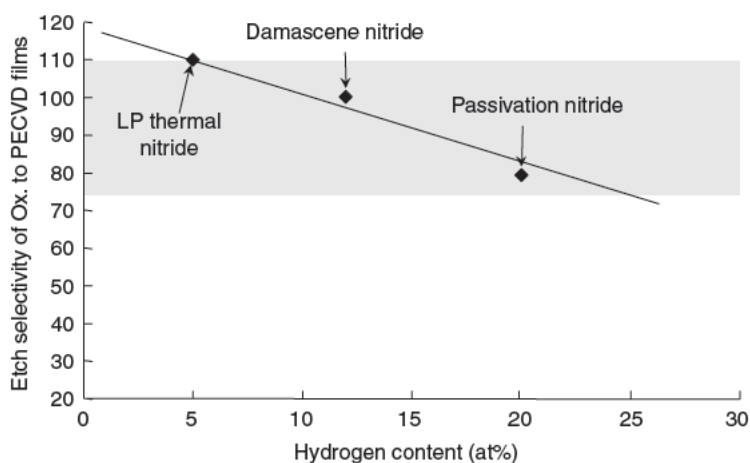


Fig. 5.15 A plot of etch selectivity as a function of hydrogen content in silicon nitride films.

Interestingly, the hydrogen content in the nitride film not only affects FSG adhesion, it also impacts the etch selectivity. Selectivity is defined as the etch rate of oxide to SiN. In order for SiN to function as a good etch stop, the selectivity has to be high. Figure 5.15 shows that films with lower hydrogen content provide higher selectivity.

5.3.3 Oxynitrides (SiON)

Antireflection coatings are used to minimize the amount of incident light that gets reflected back from the substrate. This effect is achieved by controlling the optical properties of the ARCs, namely the refractive index (n), the thickness (t), and the extinction coefficient (k). The absorption coefficient is directly proportional to k and inversely proportional to the wavelength of light. Silicon oxynitride films are commonly used for this application since the films' n and k values can be easily tuned to minimize reflections.

In addition to SiH_4 and N_2O , sometimes helium or nitrogen can be added to the reaction for various reasons. Since helium is easier to breakdown, it helps to stabilize the plasma during deposition and therefore allows tighter and more uniform control of the RI, extinction coefficient, and the thickness values. Since ARC layers are not removed after the patterning process in some integration schemes, it is critical that the film remains stable throughout all the subsequent processing steps.

By varying the SiH_4 to N_2O flow ratio, a wide range of n and k values can be achieved for 248- and 193-nm stepper wavelengths as shown in Fig. 5.16. Polysilicon is more reflective than aluminum and therefore requires a higher extinction coefficient to achieve the same minimal reflectivity. As the stepper wavelength decreases, the reflection for a given substrate increases and, therefore, a higher extinction coefficient is also needed as shown in Fig. 5.16.

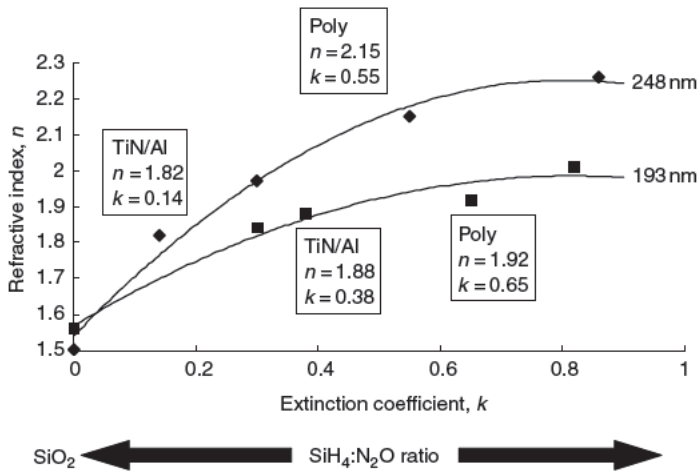


Fig. 5.16 A wide range of n and k values can be tuned by changing the SiH_4 to N_2O ratio.

Table 5.4. Effect of reactive gas flows on deposition rate, n and k values

	Deposition rate (Å/min)	Refractive index (n)	Extinction coefficient (k)
SiH_4 flow ↑	↑	↑	↑
N_2O flow ↑	↓	↓	↓

At a high N_2O to SiH_4 ratio, the film composition consists of more oxygen than nitrogen and therefore results in a lower refractive index and extinction coefficient, similar to the properties of silicon dioxide. As the SiH_4 flow increases, the film becomes more silicon rich and the film properties gradually approach that of silicon, with high n and k values. The typical effects of different process parameters on deposition rate, RI, and extinction coefficients are shown in Table 5.4.

5.3.4 Silicon carbide (SiC)

In order to use silicon carbide for low- κ applications, the dielectric constant needs to be low and the film needs to be electrically insulating. Conventional silicon carbide (SiC) has a dielectric constant of 7 and an RI of 2.2, similar to that of silicon nitride. It is also more electrically leaky due to conduction through the silicon atoms. Since silicon atoms are larger in size than carbon, they are more electronically polarizable than carbon, more specifically, 20 times that of carbon. Therefore, the less silicon content in the film, the less polarizable the film and the lower the dielectric constant. Moreover, the less silicon content, the less conduction and therefore the more electrically insulating the film is.

Table 5.5. Comparison of mechanical properties between silicon carbide and silicon nitride

Mechanical properties	Silicon carbide (SiCH)	PECVD SiN
Dielectric constant	< 5	7–8
Refractive index	< 1.9	1.9–2.2
Stress	Compressive	Compressive
Mass density	< 1.8 g/cm ³	2.2 g/cm ³

The relationship between dielectric constant, κ and RI, n , is as follows: $\kappa \propto n^2$. Therefore, lowering the RI of the SiC film will lead to lower κ . By incorporating CH₃ groups into the structure, the RI and the κ value can be lowered. However, if the film is too carbon and hydrogen rich, the subsequent ashing process that uses an O₂-based chemistry would attack the carbon in the SiC film. Since the SiC film has hydrogen and sometimes, nitrogen, it is also known as SiCH and SiCN, depending on the precursors used.

Properties of SiCH are similar to that of SiN in many ways. They are both good copper diffusion and moisture barriers. They are thermally stable during subsequent temperature cycles. They possess good mechanical strength and adhere to copper well. They have compressive stress to balance out the tensile stress of the CDO films. They also have high etch selectivity to oxide films when fluorine etch chemistry is applied. Last, but not least, they also have low leakage and high breakdown voltage. On the other hand, SiC has slightly lower density and dielectric constant than SiN due to the carbon and hydrogen incorporation. The bulk density of SiCH films is much lower than that of pure silicon carbide film due to the high hydrogen content in the SiCH film. Oxygen is usually only present on the surface of the SiCH film since oxygen in the bulk film will degrade the copper barrier performance.

A comparison between SiCH and SiN is summarized in Table 5.5.

5.4 Application of silicon-based dielectrics

Silicon-based dielectrics are used throughout the IC fabrication sequence for both logic and memory devices. Figure 5.17 and 5.18 show the cross-section of a logic and DRAM device, respectively, with the various silicon-based dielectric layers and the corresponding materials used for each layers. In this section, we will describe the material requirements for each of these layers, and the common materials and processes used for depositing these device layers. The interface properties and the interactions between these dielectrics and its underlying and overlying materials is thoroughly described in Chapter 4.

5.4.1 Shallow trench isolation

Shallow trench isolation (STI) is used to isolate between two transistors. The fabrication sequence and structure is shown in Fig. 5.19.

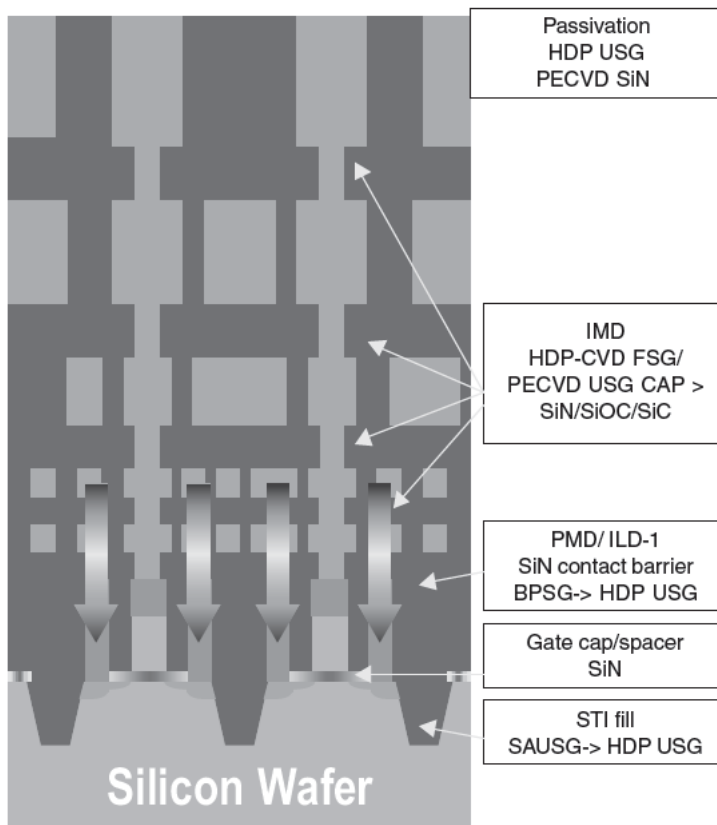


Fig. 5.17 Silicon-based dielectric layers in logic devices.

LPCVD Si_3N_4 is typically used as an etch mask for the Si trench etch and CMP stopping layer during STI formation. This is due to its better etch selectivity to Si than PECVD nitride and is less prone to erosion during CMP oxide polish.

STI also requires high aspect ratio ($>5:1$) gap fill, with low mobile ion and metallic contamination for low leakage current and mechanical integrity for CMP compatibility. HDPCVD is preferred due to its better gap fill capability and higher mechanical integrity than PECVD, SACVD, or LPCVD oxides.

SACVD USG films have been used but tend to have seams in the middle of the trench and, therefore, need to be annealed at high temperature to complete the fill. However, as the aspect ratio becomes higher, starting from the $0.25\text{ }\mu\text{m}$ technology node, even the high-temperature anneal is not sufficient to entirely fill the trench. HDPCVD, therefore, becomes the film of choice since the anneal step can be eliminated. However, excessive sputtering from HDPCVD can damage the corners of the trench as well as gate oxide, causing transistor leakage and low gate oxide integrity. Hence, the HDP process has to be optimized to ensure good gap fill as well as good electrical performance. Since the trench isolation step takes place before the transistor

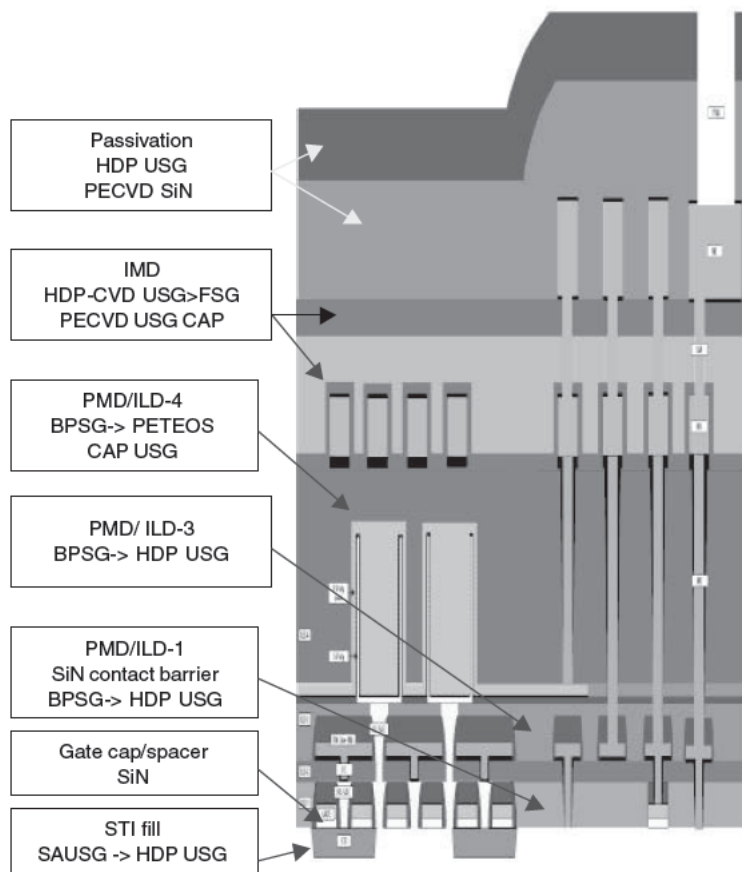


Fig. 5.18 Silicon-based dielectrics in DRAM devices.

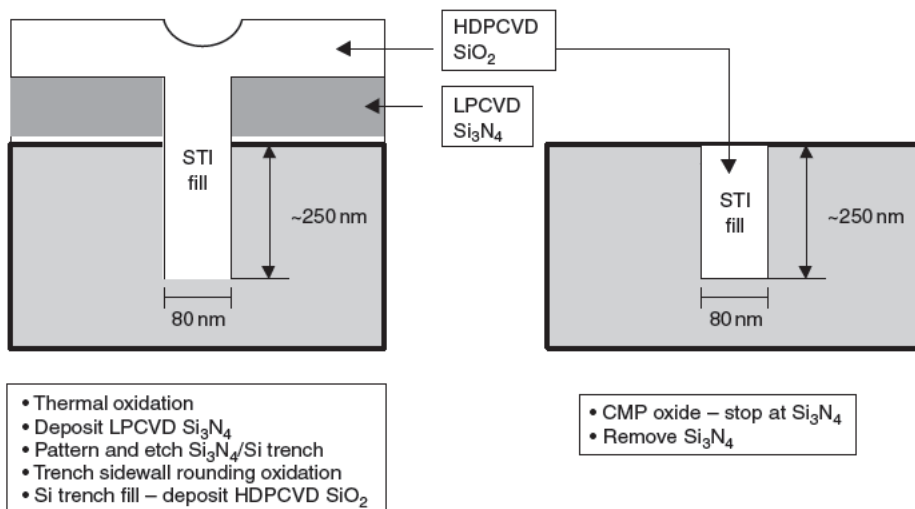


Fig. 5.19 STI formation.

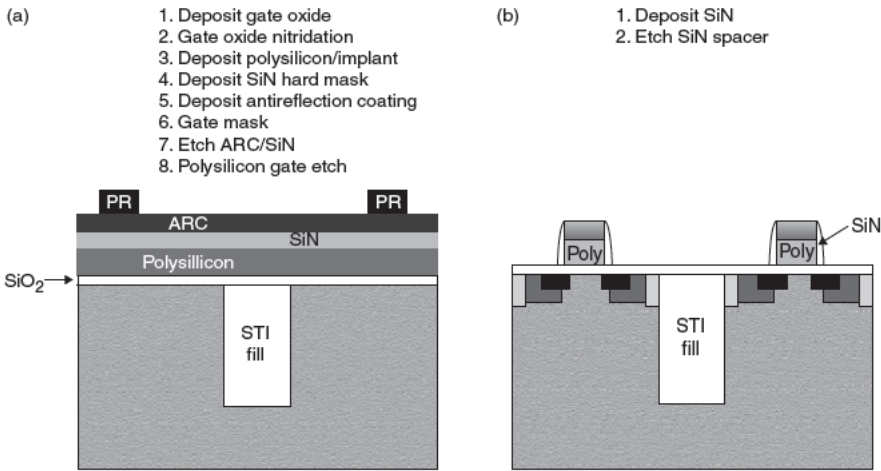


Fig. 5.20 (a) SiN as poly-etch mask. (b) SiN as sidewall spacer.

is formed, a higher-temperature ($\sim 750^\circ\text{C}$) HDPCVD process can be used to enhance gap fill of high aspect ratio structures.

5.4.2 Transistor and capacitor dielectrics

During gate transistor formation, LPCVD silicon nitride is used as an etch mask for poly-gate etch as well as sidewall spacer for salicidation and source drain implant as shown in Fig. 5.20(a) and (b).

During the trench capacitor formation of DRAM devices, LPCVD nitride and oxides are used as the etch mask for deep trench etch ($7\text{--}8\mu\text{m}$ deep), as well as in the various trench capacitor and gate transistor fabrication steps as shown in Fig. 5.21 [11].

Silicon nitride is also used as etch stop for self-aligned contact in the premetal dielectric (PMD) layer as shown in Fig. 5.22.

5.4.3 Premetal dielectric (PMD)

The dielectric layers that isolate the transistors and the capacitors from the metal interconnect layers are commonly referred to as PMD. For DRAM devices, there can be up to four PMD layers. For logic devices, there is usually only one PMD layer. It also physically protects the transistors from mobile ion contamination that might result from subsequent processing and handling.

PSG and BSG films are commonly used for PMD application. Phosphorus dopant from the PSG and BPSG is an excellent agent for gettering mobile ions like sodium and potassium.

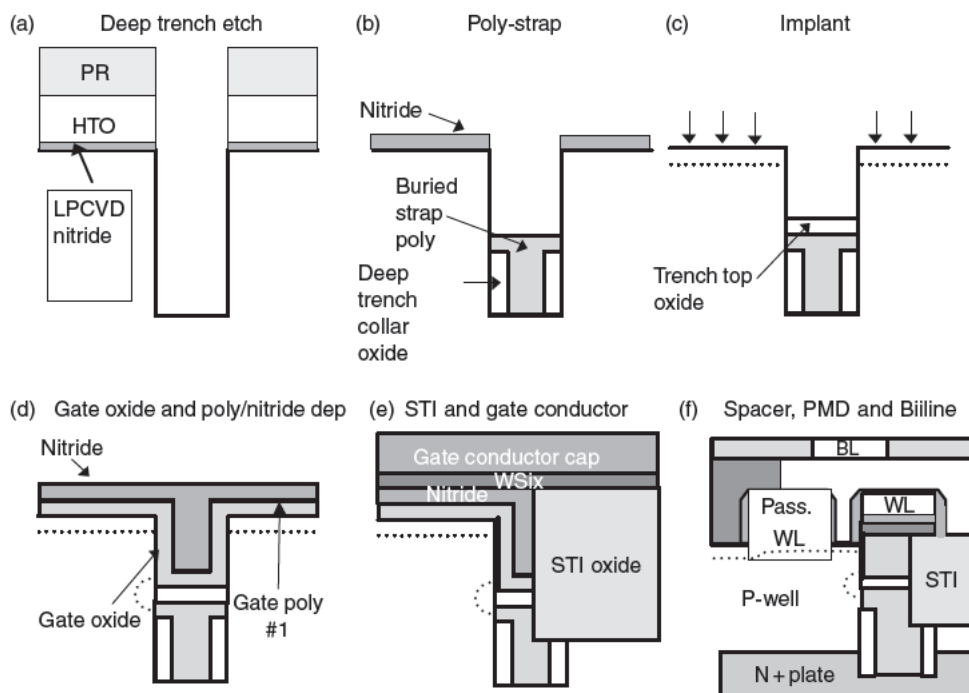


Fig. 5.21 Trench DRAM device fabrication steps.

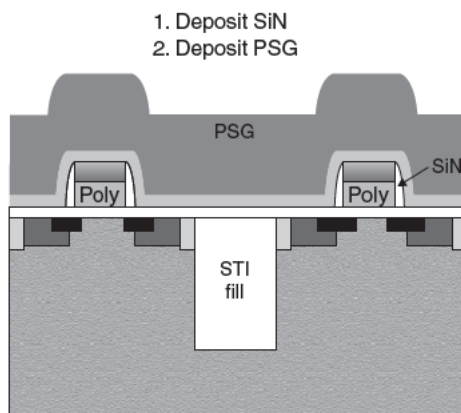


Fig. 5.22 Silicon nitride as an etch stop for pre-metal dielectric.

It prevents the mobile ions from diffusing to the active devices and degrading the electrical performance of the transistors. Boron, depending on the dopant concentration, decreases the glass reflow temperature to as low as 800°C, planarizing the topography without going to excessively high temperature.

SACVD BPSG has been the film of choice for PMD for many device nodes. However, BPSG films require high-temperature ($>800^{\circ}\text{C}$) anneal to flow the glass. Due to the incompatibility of the BPSG reflow temperature with titanium and cobalt silicides, which undergo phase transformations at around 600°C and increases the contact resistance, and to prevent junction dopant out diffusion, the high-temperature reflow step has to be eliminated. Therefore, HDPCVD PSG films deposited at $<550^{\circ}\text{C}$ is gradually replacing SACVD BPSG since planarization can be achieved without the high-temperature reflow and the difficult to control boron is also eliminated since reflow is no longer needed.

5.4.4 Inter-metal dielectric (IMD)

5.4.4.1 IMD for aluminum metallization

For the $0.25\text{-}\mu\text{m}$ and above technology nodes, PECVD TEOS USG films are commonly used for IMD to fill the gap between aluminum metal lines due to the conformal step coverage characteristics. However, as the device geometry continues to shrink below $0.25\text{ }\mu\text{m}$, the gap fill capability of TEOS USG films also runs out of steam. At that point, HDPCVD SiH_4 USG becomes the film of choice for IMD. By optimizing the D/S ratio, HDPCVD oxide films can easily fill aggressive aspect ratio structures. However, due to the high capital cost and low productivity of HDP equipment, a common scheme used today is to combine HDP and PECVD films to provide a high-productivity and low-cost solution.

In this scheme, HDPCVD is used to fill the gap just enough to cover the top of the aluminum line and then PECVD USG is used as capping layer or sacrificial layer on top of the HDP USG film. This scheme is illustrated in Fig. 5.23.

At the $0.18\text{ }\mu\text{m}$ technology node, high line-to-line capacitance of the undoped USG with $\kappa = 4.0$ becomes the limiting factor affecting the interconnect speed. Fluoro-silicate glass (FSG) with a κ value of ~ 3.5 provides an interim solution for reducing circuit delays. HDP FSG serves

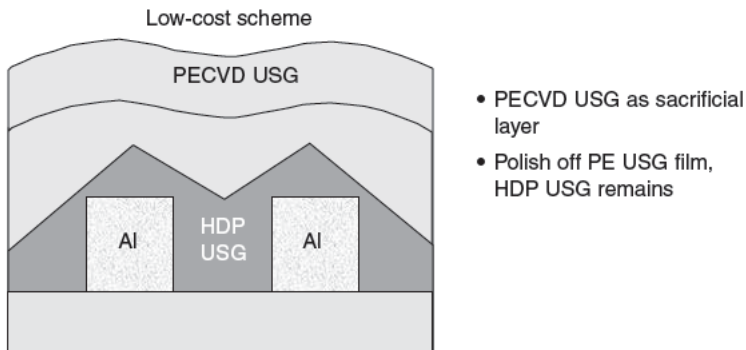


Fig. 5.23 PECVD USG as a capping layer over HDPCVD USG in the aluminum scheme.

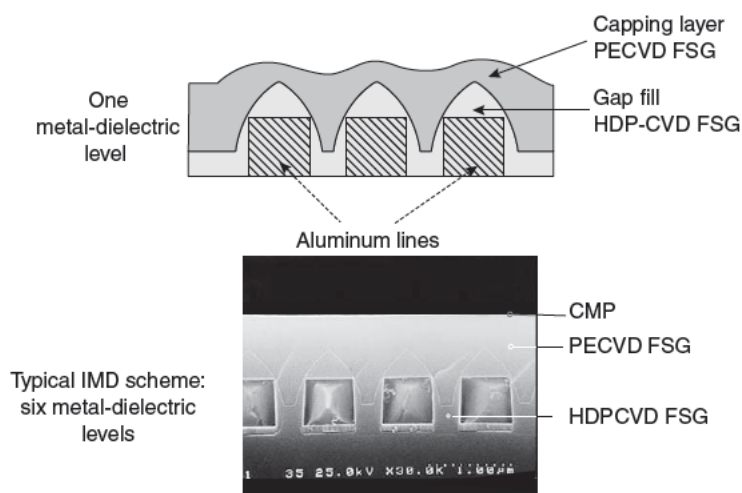


Fig. 5.24 PECVD FSG capping over HDPCVD FSG for aluminum scheme.

the purpose of gap fill as well as low κ . In order to cover the line as well as the gap, a thick layer of HDP FSG ($>1.5\ \mu\text{m}$) is needed. Since the cost of ownership of HDP films is high, it is more cost-effective to minimize the amount of HDP films deposited and then use a PECVD oxide as a cap [12]. As a result, the embedded FSG scheme, similar to the embedded USG scheme, is sometimes used (Fig. 5.24). In this scheme, only an adequate thickness of HDP FSG is used to fill the gap. Then, a very high deposition rate PECVD FSG is deposited on top of the HDP FSG as a sacrificial layer to provide enough thickness for CMP planarization. Some schemes even deposit PE USG on top of PE FSG to further lower gas cost. This way, both the gap fill and low-cost requirements are fulfilled.

Since most of the PECVD FSG is removed by CMP, it is very important that the film can withstand moisture during the CMP process. Otherwise, the film will require an extra bake out step after CMP to eliminate the moisture. Figure 5.25 shows the different FTIR Si-OH and H-O-H peaks between FSG with and without moisture absorption.

5.4.4.2 IMD for copper metallization

Since device speed is limited by the resistance of the aluminum metal lines that connect the transistors and the capacitance of the silicate glass dielectrics between them, the industry is transitioning to copper, which has lower resistance than aluminum, and to low- κ dielectrics, which have lower capacitance than USG. This switch involves many fundamental changes in the process flow. Since it is difficult to etch copper, a new approach called ‘damascene’ processing is used. In ‘dual damascene’ processing, both vias and trenches are etched and filled with copper to connect the overlying or underlying metal layers (Fig. 5.26).

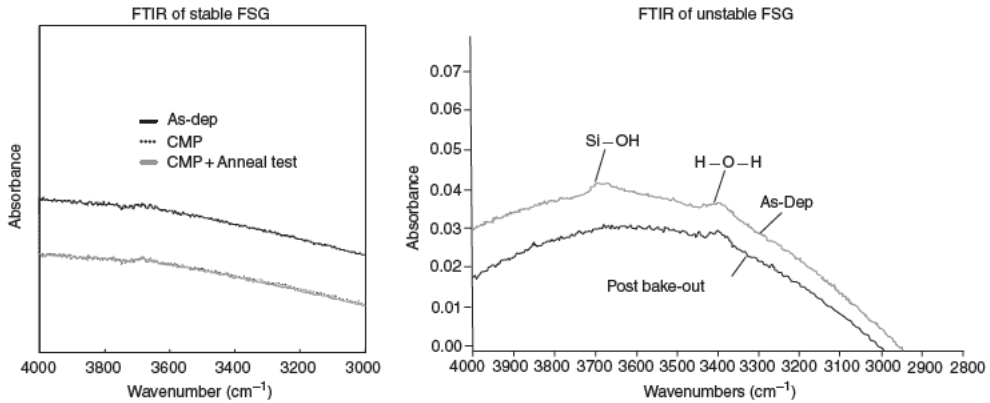


Fig. 5.25 Unstable PECVD FSG tends to absorb moisture from subsequent CMP steps.

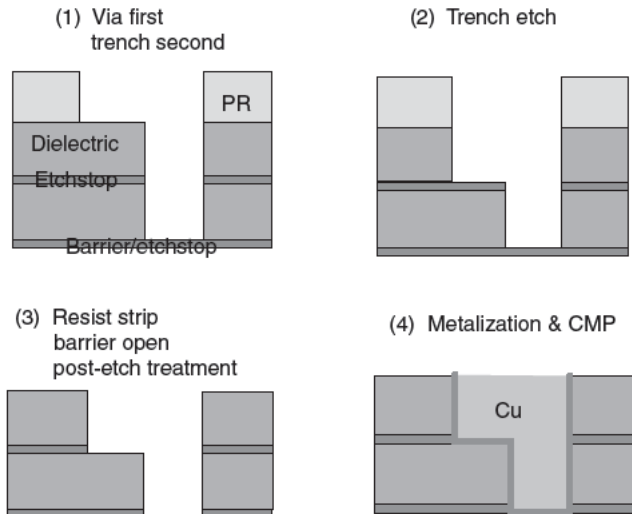


Fig. 5.26 Dual damascene scheme for copper processing.

FSG, with a κ value of 3.5–3.7, similar to that used in the aluminum scheme, has proven to be extremely effective in achieving an initial reduction in capacitance for copper dual damascene metallization. Since the properties of FSG films are largely similar to that of USG films, it can be readily adopted with the least integration risks. FSG films can be deposited either by the PECVD or HDP method. Minimal hardware modification is needed to convert a system from USG to FSG. This film, with $\kappa \sim 3.5$, is widely accepted by the industry and is being implemented as the first-generation low- κ dielectric.

Barth *et al.* [13] reported blistering problems while integrating SiH_4 FSG and SiN if the SiF_4 to SiH_4 flow ratio is not optimized. Wistrom *et al.* [14] compared the film properties and

integration of H-DP FSG, PE SiH₄ FSG, and PE TEOS FSG, and found that TEOS FSG appeared to be superior to PE SiH₄ FSG by a wide margin in several tests: stress stability ($20\times$ difference), dielectric constant (κ of SiH₄ FSG is similar to USG), blistering on as-deposited and annealed films, wet etch rate, F diffusion ($>4\times$ difference), breakdown voltage and leakage (three orders of magnitude difference). The comparison data show that a more stable FSG can be easily integrated into copper damascene schemes.

CDO is becoming the low- κ dielectric film of choice for copper dual damascene applications at the 100-nm technology node and beyond because it offers even lower κ value than FSG ($\kappa \sim 2.2\text{--}3.0$).

During the course of fabricating a device, the CDO films would go through at least 10–15 thermal cycles at about 400–425°C. CDO films and copper have similar coefficient of thermal expansion (CTE), creating less stress from thermal mismatch between metal and dielectric. This kind of stress could lead to film delamination if the adhesion between the dielectric and the metal is poor. CDO films also have high thermal conductivity, allowing heat generated from joule heating in metal lines to be removed efficiently. Lastly, mechanical strength of CDO films, that is, hardness or Young's modulus is sufficiently high to withstand all subsequent processing steps, especially during CMP processing since the film is exposed to harsh abrasive polish environment.

Although CDO films are constantly exposed to etch chemistry, post-etch photoresist removal, or ashing and solvent clean, they do not change properties after these integration steps. FTIR spectra of the CDO films show no change on the Si-CH₃, Si-H, C-H, and Si-OH peaks, before and after integration. Also, minimal change in dielectric constant after integration is found. Figure 5.27 shows the performance of a stable CDO film from FTIR analysis.

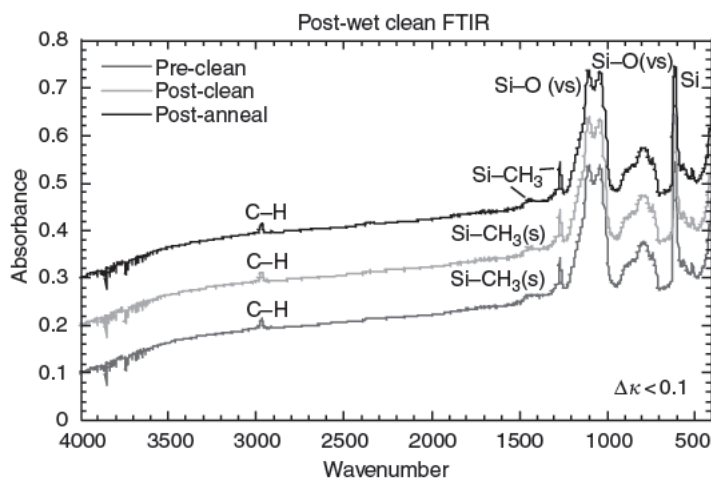


Fig. 5.27 CDO films show no change in FTIR spectra after integration.

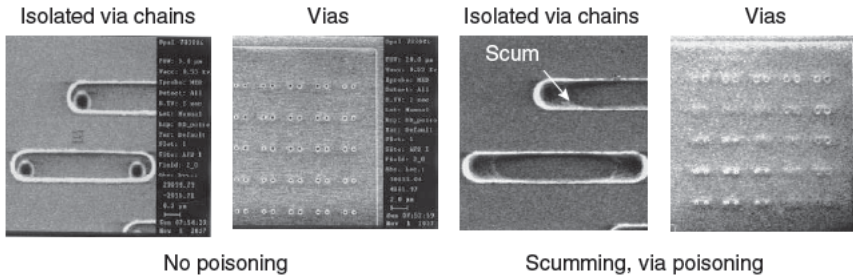


Fig. 5.28 Examples of with and without via poisoning.

Another potential problem experienced during integration of CDO is via poisoning. If there are N–H bonds in the barrier/etchstop layer, during the trench lithography step, photoresist could react with the N–H species and create scumming and mushrooming in the trenches and the vias. Figure 5.28 shows the difference between with and without poisoning.

5.4.5 Passivation

The passivation layer serves to isolate the silicon devices from moisture absorption as well as metal ion diffusion resulting from soldering and other device packaging steps. PECVD nitride and oxides have been used for this application and will continue to be used, although HDPCVD may gain acceptance as device shrinks and step coverage becomes an issue.

5.4.6 Other applications

5.4.6.1 Hardmask for copper dual damascene process

USG has been used as part of the multi-layer hardmask scheme over a spin-on type low- κ dielectric in the dual damascene application. The dual hardmask scheme typically consists of a thin low- κ copper diffusion and moisture barrier such as SiCH or SiN, followed by USG. Then photoresist is applied and developed over the USG hardmask layer, preparing the stack for via and trench etching. There are many advantages of using USG as the top hardmask layer. First, USG is inert to resist interaction, therefore preventing resist footing issue. Second, the chemical mechanical polish characteristics of USG are well understood, allowing the CMP process to stop at the SiCH or SiN interface precisely.

5.4.6.2 Etch stops and copper diffusion barrier for dual damascene process

Since copper readily diffuses into silicon oxide even at room temperature, an effective dielectric barrier for copper damascene integration scheme is required. Critical properties for such

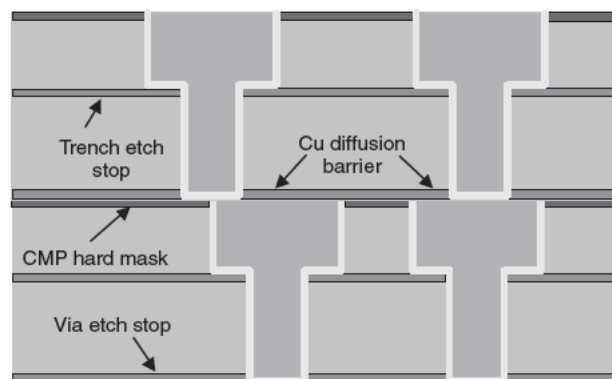


Fig. 5.29 Different applications for silicon nitride and silicon carbide.

a barrier are: good barrier performance with very short diffusion length of copper in the barrier, high etch selectivity with respect to oxide and low- κ dielectric films, low leakage and high dielectric breakdown voltage, strong adhesion to copper, oxide, and other low- κ dielectrics. In addition, the barrier film must be deposited at temperatures compatible with interconnect integration schemes.

Copper tends to oxidize when it comes in contact with air and forms native copper oxide. The presence of native copper oxide could lead to several integration problems. First, copper oxide causes poor adhesion at the copper/silicon nitride interface as well as the copper/tantalum nitride interface leading to peeling problems. Second, copper oxide degrades electromigration lifetimes. Third, copper oxide increases via resistance and eventually increases RC delay. Therefore, removal of the native oxide on a copper surface is a critical step in the damascene processing of copper-based interconnects. Unfortunately, there is no good way to determine when to terminate the NH_3 plasma during CuO removal. The only accurate way of measuring residual oxygen at the interface is by XPS.

Silicon nitride has been widely used in microelectronic device fabrication for years. The applications include final passivation layer, diffusion barriers, against mobile ions, moisture barriers, and etchstop layers for pre-metal dielectric. Recently, silicon nitride film applications have been extended to advanced dual damascene processing, such as copper diffusion barrier, etchstop, and CMP stop layers due to the film's excellent barrier properties against copper and moisture and the high etch selectivity to low- κ dielectric films. Figure 5.29 shows the different applications of SiN and SiC in the dual damascene copper process.

It is very important that silicon nitride is deposited on the copper immediately after the CuO is removed without breaking vacuum because once the copper is exposed to atmosphere, CuO will regrow right away. This process sequence is called *in situ* copper oxide removal. The oxygen concentration at the interface using the *ex situ* CuO removal method could be an order of magnitude higher than that of the *in situ* case.

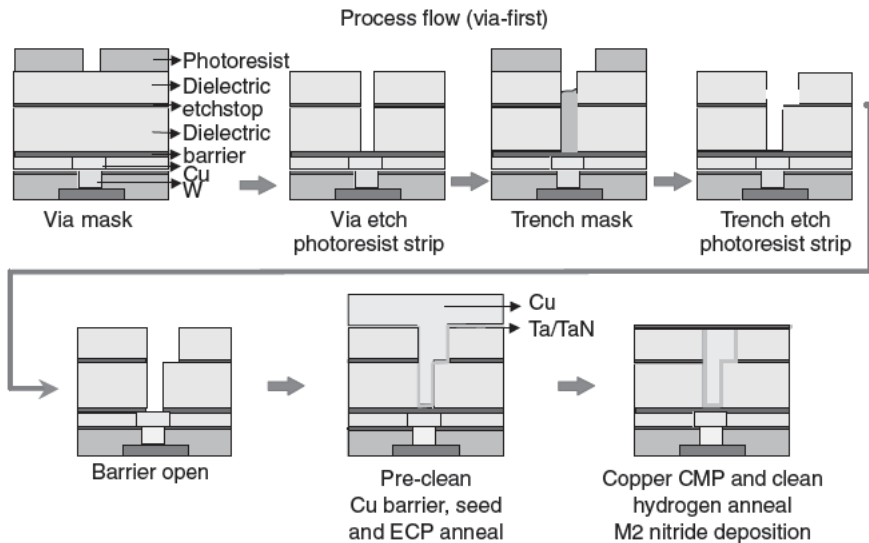


Fig. 5.30 Via-first dual damascene scheme.

The most common dual damascene etch scheme is called via-first and the scheme is shown in Fig. 5.30. After lithography is performed, the via is etched through the two layers of dielectric, without punching through the bottom nitride layer. Then the trench is patterned and etched through the top layer of dielectric, stopping at the first nitride layer. Without the high selectivity between the bulk dielectric and the etch stop, etch systems would need a tight control of etch uniformity to ensure that all the trenches are of the same depth across the wafer and from wafer to wafer. If there is no etch stop, the trench etch would have to be done based on time. Variations in the dielectric thickness would lead to differences in resulting trench depth and punch through of the bottom via.

Silicon carbide can also be used for copper diffusion and moisture barrier, etch stop for trench and via, CMP cap and hard mask layer with copper dual damascene applications.

SiCH has a lower dielectric constant than conventional SiN, and is also a good copper barrier, similar to SiN. Since SiCH is thermally and chemically stable, it can be used as a capping layer or moisture barrier over the more hydrophilic CDO films to protect the CDO films from absorbing moisture from subsequent chemical processing steps such as CMP.

Since SiCH etches slower than oxide-type materials and, therefore, exhibits high selectivity, it is also used as an etch stop layer. When used as the via etch stop in the dual damascene scheme, the high selectivity of SiCH widens the dielectric etch process window and prevents undesirable punch through to the copper underneath the dielectric. When used as the trench etch stop, it allows the trench dielectric etch to stop at the bottom of the trench; therefore, controlling the trench depth more precisely.

SiCH is also used as a CMP stop for several reasons. First, copper CMP has high selectivity to SiCH and therefore can stop easily when the SiCH layer is reached. Second, SiCH adheres to and protects the underlying low- κ material well and, therefore, allows the low- κ layer to stay intact after the aggressive CMP process.

If 248-nm lithography is used, SiCN films do not pose severe resist poisoning issues but at the same time offer greater hardness and better compatibility to the subsequent etching and ashing processes. However, when 193-nm lithography is used, nitrogen in the SiC film will lead to severe resist poisoning issues and, therefore, must be eliminated from the film. Resist poisoning is caused by N-H species reacting with photoresist in the dual damascene scheme.

5.4.6.3 Antireflection coatings

Silicon oxynitride is mainly used as an ARC during photolithography because of its ability to absorb light.

Photolithography is the process of printing images of the circuit pattern onto a wafer. This is usually accomplished by exposing a photosensitive layer called photoresist through a mask to transfer the image onto a wafer. When the underlying film is highly reflective, light reflected from the substrate surface and the photoresist surface tends to interfere with the incident light from the exposure source through the mask and cause unwanted reflections (Fig. 5.31) leading to linewidth variations, also known as critical dimension (CD) swing [15].

As the device features shrink, CD control becomes even more critical. Shrinking device features require lower exposure wavelengths, which, in turn, lead to increasing amount of substrate reflection, causing larger CD swing. Conventional ARC layers, such as spin-on polymers, have been used to suppress unwanted reflections by utilizing the absorption properties of the film. However, due to the self-planarizing nature of spin-on films, an organic ARC film has thickness variations over topology and, therefore, results in different absorptivity through the

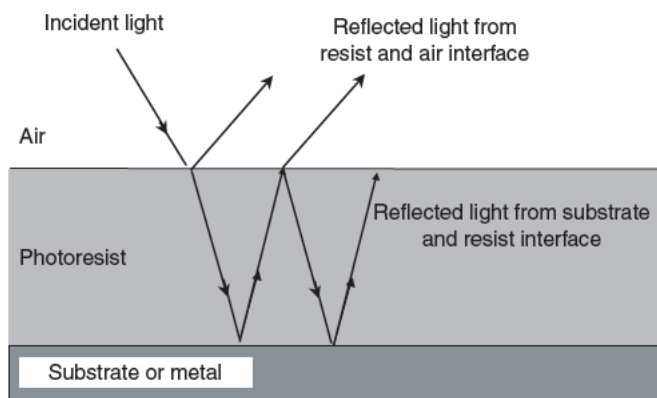


Fig. 5.31 Reflected light from substrate surface interferes with incident light.

layer. This would require the film thickness to be optimized for the thinnest layer to totally absorb light, which may result in a substantially thicker film over topography and would have to be optimized for different circuit patterns. The thickness variations in the polymer ARC would cause etching problems since there is minimum etch selectivity between organic photoresist and the organic ARC film.

Organic ARCs reduce light reflections by absorbing the reflections (Fig. 5.32). Therefore, starting at 0.35- μm device geometry, a dielectric ARC (DARC) film is used. DARC works by using phase-shift cancellation (Fig. 5.33).

When the reflections from the substrate and that from the ARC surface are 180° out of phase with each other, the reflections will cancel each other by destructive interference. A phase

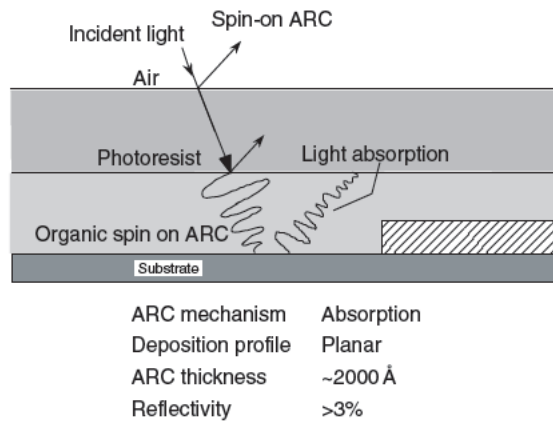


Fig. 5.32 Organic spin-on ARC works by absorption.

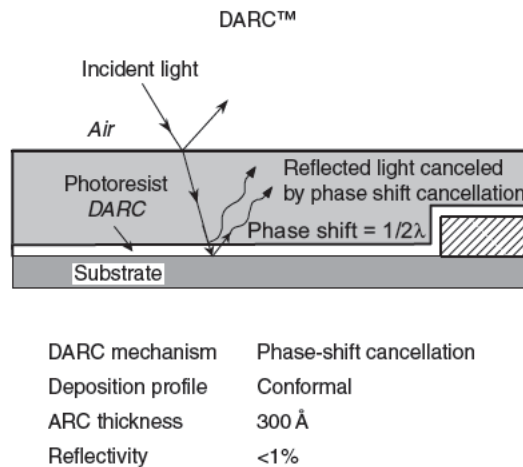


Fig. 5.33 Dielectric ARC works by phase-shift cancellation.

shift of half a wavelength for the wave passing through the DARC can be achieved by optimizing the thickness (t) and the RI (n) of the DARC. By optimizing the optical properties of the DARC film, the reflections can be minimized.

DARC is typically a thin conformal SiON film deposited by the PECVD method. SiON films are chosen for ARC applications for several reasons. First, SiON films have the suitable range of optical properties for ARCs. Second, the stoichiometry of the plasma-deposited SiON films can be tuned to provide the specific n and k values required for the specific exposure wavelength by modifying the ratio of reactive gases used for deposition. Third, SiON films have been widely used in the semiconductor industry for years and are familiar to users in terms of properties, metrology, and integration characteristics. Last but not least, only a thin layer, of the order of 300 Å of SiON, is needed since SiON is conformal over topography. This provides a significant advantage over an organic ARC film since it enables uniform etching as well as better etch selectivity to the organic resist layer due to their differing etch chemistry. As feature size decreases, conformality and etch selectivity of the ARC layer becomes even more important due to thinner resists.

One of the phenomena observed with ARC material is the presence of 'footing' (Fig. 5.34). Footing is a result of the amine groups (NH_2) on the surface of the ARC film reacting chemically with the photoresist. Deep UV resists are especially sensitive to footing. The interaction between N-H radicals and resist results in a 'foot' after resist development, causing loss of critical dimension control. Both titanium nitride (TiN) and SiON ARCs are known to cause footing problems. One way to prevent this interaction is to deposit a thin layer of oxide on top of the SiON before the photoresist is applied. The oxide serves as an inert barrier between SiON

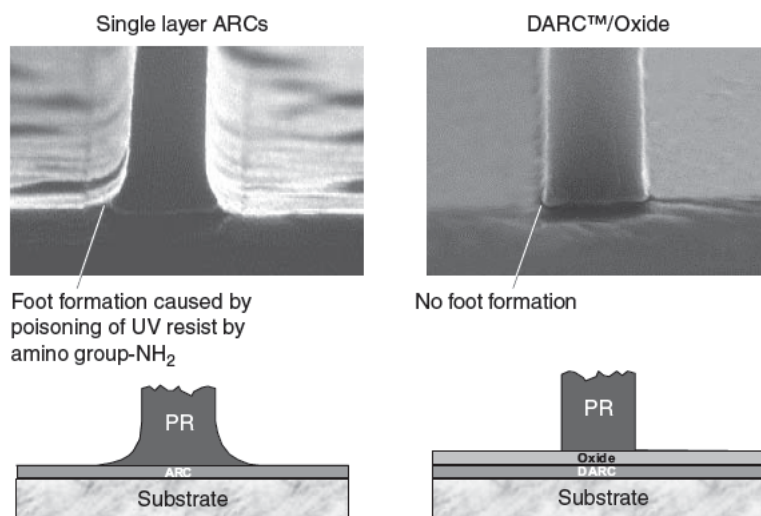


Fig. 5.34 Footing results from interaction between the amine groups in the ARC film and photoresist.

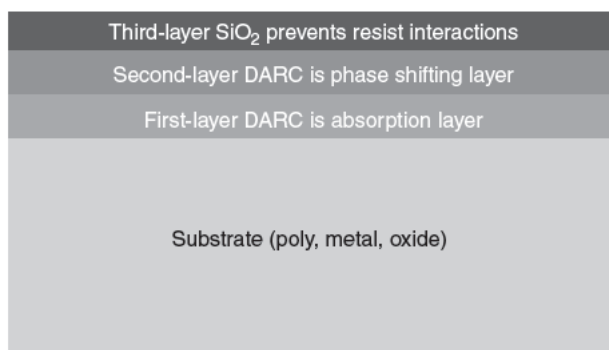


Fig. 5.35 Multi-layer ARC scheme is used to minimize reflected light and footing issue.

and resist but does not affect the optical properties of SiON. This thin oxide can be achieved by utilizing a high N_2O to SiH_4 ratio as mentioned earlier. Another way to avoid the interaction is to use an oxygen or N_2O plasma treatment after SiON deposition to effectively remove the NH groups from the surface. Both the oxide cap and the oxygen treatment can be performed *in situ*, that is, after the SiON deposition in the same chamber to prevent footing in just a simple and efficient step.

As the lithography requirements get more and more stringent, even the least amount of reflected light is not acceptable. A multilayer DARC scheme is designed to address this requirement. The first-layer DARC absorbs most of the light, the second layer of DARC uses the phase shift property to cancel out any remaining light and the last or top layer is a very thin silicon oxide film that prevents resist poisoning. The multilayer scheme is shown in Fig. 5.35.

5.5 Summary

The deposition techniques, material and film properties, as well as the applications of silicon-based dielectrics have been described. These include undoped and doped silicon oxide, silicon nitride, silicon oxynitride, and silicon carbide. Both thermal- and plasma-assisted CVD techniques have been used in the industry to deposit these films, with the resultant film properties, and their consequent applications in the semiconductor fabrication process. As discussed above, silicon-based dielectrics will continue to be the material of choice for fabricating silicon devices, albeit with new dopants (i.e. carbon) and their resultant material properties, due to its compatibility with silicon substrate as well as the industry familiarity with these materials.

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Chapter 10

High- k dielectrics grown by atomic layer deposition: capacitor and gate applications

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Abstract

The dramatic improvements in microelectronics performance over that past few decades have been accompanied by a severe reduction in the size of memory and logic devices. This scaling has required drastic decreases of the SiO_2 dielectric film thickness to achieve ever-higher capacitance densities. Fundamental limits of SiO_2 as a dielectric material, imposed by electron tunneling, will be reached as this SiO_2 film thickness approaches ~ 1 nm. By 2005, an as yet undetermined alternate high- k interlayer dielectric material will be needed to replace SiO_2 as a capacitor and gate dielectric material. Numerous alternate high- k materials are being actively investigated, ranging from Al_2O_3 ($k \sim 9$) to perovskites ($k \sim 10^2$ – 10^4). High- k materials hold the promise of achieving very high capacitance densities with relatively thick films. These thicker films should preclude the excessive tunneling currents observed for very thin SiO_2 films. However, finding a high- k material is a major challenge because the high- k material must have a high resistivity, act as a good barrier layer, be thermally stable, and form an ideal interface with silicon. SiO_2 films can be conveniently formed via oxidation of the silicon substrate. In contrast, alternate high- k materials must be formed by deposition. Atomic layer deposition (ALD) has emerged as a very promising technique for depositing alternate high- k thin films for the microelectronics industry. ALD can deposit films with atomic layer thickness control and conformally coat high aspect ratio structures. Most high- k dielectric materials have been successfully deposited by ALD. ALD is also very well suited for depositing various types of composites that combine the desirable properties of different materials.

10.1 Introduction

The semiconductor microelectronics industry requires interlayer dielectric films for a variety of applications. Dielectric layers are needed as gates in MOSFETs, as capacitors to store charge in memory devices, and as insulation in back-end interconnects. SiO_2 has been the dielectric

material of choice for all of these applications. SiO₂ is a dielectric material with very low leakage currents, acts as a good diffusion barrier for dopants and ionic contaminants, and forms a well-defined interface with silicon.

The continued drive towards faster processors has required the progressive shrinking of microelectronics devices [1]. The decrease in device feature size allows for increased speed, lower power consumption, and lower cost because of the increased density of devices per wafer. This size reduction presents challenges for the various SiO₂ applications. The insulation of interconnects requires lower dielectric constant materials. Applications such as capacitors and gate dielectrics require higher dielectric constant materials.

Decreasing the thickness of the SiO₂ dielectric film achieves the goal of increasing the capacitance to offset the decrease in the surface area of the capacitor. However, SiO₂ films will soon need to be so thin that tunneling through the film will become significant and will increase power consumption to unacceptable levels. High-*k* materials are needed to replace SiO₂ in these applications to achieve high capacitances while keeping the leakage currents low.

A wide range of materials has been proposed as alternate high-*k* dielectrics. The dielectric constants of these high-*k* materials range from $k < 10$ to $k > 10000$ [1–4]. Some of these materials, such as Al₂O₃, Ta₂O₅, and SrTiO₃ are already being used commercially for capacitor memory devices [1]. For the more demanding gate dielectric application in field effect transistors (FETs), the search for a suitable high-*k* dielectric material continues to be a challenge. To replace SiO₂ as the gate dielectric, the high-*k* material must also have a high resistivity, act as a good barrier layer, and be compatible with other materials and processes used in the microelectronics industry.

A wide range of techniques have been employed for depositing high-*k* material films [1, 3]. However, only a few of these deposition techniques are compatible with microelectronics processing. These techniques include chemical vapor deposition (CVD) and physical vapor deposition (PVD). This review will focus on a promising CVD-derived technique called atomic layer deposition (ALD) [5–7]. ALD is the only vacuum compatible deposition technique that allows for atomic layer thickness control and has the ability to coat conformally high aspect ratio trenches and three-dimensional (3D) structures. Furthermore, ALD is well-suited for making mixed materials and nanolaminates. Such composite materials have shown promise because the desirable characteristics of different materials can be tuned to achieve optimum properties.

For a detailed review of high-*k* materials as gate dielectrics, the reader is referred to a recent excellent review article [1]. Various books have also discussed in more detail the synthesis of high-*k* dielectrics [3] and the properties and applications of high-*k* dielectrics [8]. This chapter focuses on the high-*k* dielectrics that can be grown by ALD and will emphasize high-*k* materials that are important for capacitor and gate applications.

10.2 Limitations of SiO₂ as a dielectric

SiO₂ has served as the dielectric material for silicon-based microelectronic applications for the past three decades. SiO₂ has excellent dielectric properties, including a very high resistivity

of $\sim 10^{18} \Omega\text{cm}$ and a large bandgap of $\sim 9\text{eV}$. Furthermore, the ability to grow high quality, amorphous SiO_2 dielectric films by the oxidation of the silicon substrate is very convenient for process integration. With so much research and infrastructure invested in SiO_2 technology, finding a material to replace SiO_2 has proven to be a great challenge.

The ability to make reliable, ultra-thin SiO_2 layers has advanced greatly in recent years. In 2001, SiO_2 thicknesses on the order of $\sim 2\text{nm}$ were used in devices. Various studies have explored the minimum SiO_2 film thickness that still retains the bulk properties of SiO_2 [1]. Based on calculations and experimental results, the absolute lower limit for a SiO_2 film thickness is $7\text{\AA}$. Below this thickness, the material no longer has the SiO_2 bulk bandgap of 9eV . A further limitation for practical device applications of SiO_2 is the large tunneling current that can leak through such thin films.

A more practical limit of $10\text{--}12\text{\AA}$ has been established based on the maximum allowable tunneling current [1]. Transistors with SiO_2 film thicknesses of $10\text{--}12\text{\AA}$ can be used in FETs despite the high leakage current densities of $1\text{--}10\text{A/cm}^2$. Whether or not these $10\text{--}12\text{\AA}$ films will be economically feasible will depend on questions about ultrathin oxide reliability and contamination issues [1]. However, even if these optimistic predictions regarding ultrathin SiO_2 layers are realized, alternate high-*k* dielectric materials will be required by 2005 according to the International Technology Roadmap for Semiconductors [9].

Another way to extend the use of SiO_2 -based dielectrics has been through the incorporation of nitrogen into SiO_2 . Oxynitrides (SiO_xN_y) can achieve dielectric constants of $k \sim 6$, compared to $k = 3.9$ for SiO_2 [2]. Although oxynitrides offer only a small increase in the dielectric constant, they are much more compatible with existing processing technologies than other high-*k* dielectric materials. Oxynitrides have been used as dielectrics in memory devices and are currently being implemented in logic devices [1, 2]. By 2005, however, the equivalent oxide thickness requirements for high-performance devices, as well as for low stand-by power logic devices, can no longer be met by SiO_2 , oxynitrides, or any other currently known technology solution. At this date, the need for alternate high-*k* dielectrics becomes critical.

10.3 Desired high-*k* material properties

10.3.1 Requirements for capacitor and gate applications

Memory capacitor and gate applications both need alternate high-*k* dielectrics to achieve higher capacitance densities. However, the requirements for memory capacitor and gate applications are different [1]. Capacitors for memory need very low leakage currents on the order of 10^{-8}A/cm^2 . This requirement allows the charge stored in the capacitor to remain large enough to be read for a relatively long time period, typically $\sim 250\text{ms}$ [2]. In contrast, the nature of the high-*k*/electrode interface is not that critical, provided that the interface does not reduce the capacitance significantly. Metal or highly doped nitrided poly-Si may be used as the electrodes.

Gate dielectrics in FETs can have a much higher leakage current, but the quality of the high- k /Si bottom electrode interfacial region is critical [1]. Current densities as high as $1\text{--}10\text{ A/cm}^2$ are acceptable for some processors. Certain low power applications, such as portable devices, demand leakage currents of $<10^{-3}\text{ A/cm}^2$. These leakage current levels are still much less stringent than the requirements for memory capacitors. More important to the performance of an FET is the electric field that penetrates into the silicon channel. Interfacial layers and interface roughness adversely affect the strength and uniformity of this electric field and degrade FET performance [1].

10.3.2 *Electrical properties*

In addition to having a large dielectric constant, alternate high- k dielectrics should have a low leakage current, low loss factor, high breakdown voltage, and a large barrier height when in contact with Si. Unfortunately, high- k materials often do not exhibit these properties [1]. Optimizing the properties of alternative high- k dielectrics requires an examination of the various factors that influence the dielectric constant and leakage current.

The dielectric constant is determined by the polarizability of the dielectric material. The polarizability is dependant on a number of factors including the density of electrons in the material, the crystal structure, and dopants [1]. For example, transition metal oxides typically have higher dielectric constants than the oxides of lighter elements like Si and Al. There is often a wide range of published dielectric constants listed for a given material. This variability can be attributed, in part, to whether a material is amorphous or crystalline, the type of crystal structure, and the average crystalline grain size.

The dielectric constant of $\gamma\text{-Al}_2\text{O}_3$ is slightly higher than the dielectric constant of amorphous Al_2O_3 . This larger dielectric constant is partially explained by the higher density of $\gamma\text{-Al}_2\text{O}_3$. For TiO_2 , dielectric constant values ranging from 50 to 110 have been reported [1, 3, 4], with the rutile TiO_2 phase having higher k values than the anatase TiO_2 phase. In BaTiO_3 , grain size has been shown to affect significantly the dielectric constant [8]. The dielectric constant peaks at $k > 5000$ for BaTiO_3 with an average grain diameter of $\sim 1\text{ }\mu\text{m}$. Much smaller or larger grain sizes have $k < 2000$.

The deposition methods and the deposition conditions tend to determine the crystallinity and purity of a deposited dielectric film. High temperature annealing can result in the crystallization and densification of a dielectric material. This densification often increases the dielectric constant. Impurities are generally expected to lead to a decrease in the dielectric constant. However, the intentional doping of high- k perovskites has resulted in some very high dielectric constant values [3].

The dielectric relaxation losses of a dielectric material can have detrimental effects on the performance of memory and logic devices. This well-known, but poorly understood, phenomenon has the effect of adding RC shunts with varying time constants in parallel to the dielectric

capacitor [10]. While these losses are small for most AC power applications, they may be unacceptably large for memory and logic devices where read and write times are on the nanosecond time scale. The dielectric losses have been studied for some alternative high-*k* dielectrics [10]. HfO_2 was found to have a much higher dielectric loss than Al_2O_3 , Ta_2O_5 , BaSrTiO_3 (BST), and Y_2O_3 . Furthermore, the dielectric losses of all of these materials were at least an order of magnitude higher than the dielectric loss for SiO_2 .

High leakage currents are a major problem for memory capacitor applications. Amorphous SiO_2 has one of the highest resistivities of any material at $\sim 10^{18} \Omega \text{cm}$. Some alternate high-*k* materials, such as Al_2O_3 , come close to the resistivity of SiO_2 . Other high-*k* materials tend to have much lower resistivities. The measured resistivity of a dielectric material is not an intrinsic property of the material. Rather, the resistivity can be controlled by the purity, stoichiometry and crystallinity of the material.

Impurities can create defect sites or act as mobile ions. Small deviations from ideal stoichiometry can effectively dope a material, such as TiO_2 , and result in a dielectric becoming highly conductive [11]. Grain boundaries in polycrystalline materials also tend to increase conductivity [1, 2]. Crystallization of amorphous films through annealing can lead to increased leakage currents. Unfortunately, most alternate high-*k* material candidates, except for Al_2O_3 , crystallize during typical processing conditions.

A large barrier height at the electrode/high-*k* dielectric interface is important because this barrier height minimizes the leakage current. The barrier height at a Si/SiO_2 interface is $\sim 3.5 \text{ eV}$. However, the barrier heights and the bandgaps of high-*k* materials in contact with silicon tend to decrease with increasing dielectric constant [1, 12]. Some of the promising high-*k* materials, such as Ta_2O_5 and BaTiO_3 , have calculated barrier heights $< 0.5 \text{ eV}$. These low barrier heights may lead to unacceptably large leakage currents.

10.3.3 *Interfacial layers*

The nature of the interface between a high-*k* dielectric and an electrode plays an important role in determining whether a high-*k* material can be suitable for a certain application [1, 2]. Interfacial layers are sometimes intentionally inserted to passivate the surface, prevent diffusion, or promote adhesion. However, most interfacial layers that form spontaneously during deposition of the high-*k* material are detrimental to device performance.

Interfacial layers can severely decrease the capacitance of a high-*k* film. In FETs, these interfacial layers can limit the field penetration into the silicon channel. Interfacial oxide layers can be formed if the substrate reacts: (a) with the oxide precursors used to make the high-*k* film; (b) with the oxygen in the high-*k* film itself; and/or (c) with oxygen species that diffuse through the high-*k* film. Although some high-*k* materials are predicted to be stable in contact with silicon, nonequilibrium conditions are generally present during the deposition of these materials. On a silicon substrate, the interfacial layer formed tends to be SiO_2 or a silicate/high-*k* mixture.

Regardless of what kind of interfacial layer is formed, the overall capacitance that can be achieved with an interfacial layer/high- k stack will be lower than the capacitance of the high- k film alone. The capacitance of two capacitors in series is determined by $C_{\text{total}}^{-1} = C_1^{-1} + C_2^{-1}$. The capacitance is $C = k\epsilon_0 A/d$, where k is the dielectric constant, ϵ_0 is the permittivity of free space ($\epsilon_0 = 8.85 \times 10^{-14}$ F/cm), A the area, and d the dielectric thickness. Let us assume that a 1 nm thick SiO₂ layer with $k = 3.9$ and $A = 0.0001$ cm² is formed under a 5 nm thick high- k material with $k = 50$ and $A = 0.0001$ cm². The capacitance of the SiO₂ layer is $C = 0.35$ nF. The capacitance of the high- k layer is $C = 0.89$ nF. The resulting total capacitance is only 0.25 nF.

Another way to see this effect is to consider the equivalent oxide thickness (EOT). The EOT is the thickness of SiO₂ with $k = 3.9$ that would equal the capacitance of the high- k material. The high- k material with $k = 50$ and a thickness of 5 nm would have an EOT of only 0.39 nm. The total EOT of the stack, including the SiO₂ interfacial layer, is much higher and can be given by:

$$\text{EOT} = \frac{k(\text{SiO}_2)}{k(\text{high } k)} \times d(\text{high } k) + d(\text{SiO}_2)$$

The EOT of the stack, including the SiO₂ interfacial layer, is $\text{EOT} = 1.39$ nm. The capacitance of this film is not nearly as high as the original expectations. However, this stack should still have a lower leakage current than a 1.39 nm thick SiO₂ layer.

10.3.4 Processing issues

The processing of devices after depositing the high- k material typically involves annealing to high temperatures of $\sim 1000^\circ\text{C}$. High temperature annealing can lead to a number of problems [1, 2]. Many high- k materials crystallize at these high temperatures. Crystallization tends to result in higher leakage currents. In addition, mixed materials may phase segregate at higher temperatures. The high temperatures can also accelerate the diffusion of cations into and through high- k materials. This diffusion can degrade the dielectric and the material below the dielectric. Oxygen diffusion, especially at high temperatures, is also a known problem for high- k materials. Oxygen diffusion can result in increased interfacial SiO₂ growth.

10.4 Thin film deposition techniques for high- k materials

Thin films of high- k materials have been deposited by a number of methods. Techniques include CVD, reactive sputtering, physical vapor deposition (PVD), molecular beam epitaxy (MBE), sol-gel methods, and hydrothermal and electrochemical syntheses [3]. Only a few of these methods are compatible with the stringent requirements for microelectronics fabrication processes. CVD is perhaps the most well-known technique for the deposition of high- k thin films. During CVD, gas phase precursors are introduced into a vacuum chamber, where they react and deposit a film on the substrate.

Most high- k films in the microelectronics industry are presently deposited by CVD and CVD-derived techniques [13]. High- k Ta_2O_5 films have replaced oxynitride films for current use in DRAM fabrication [2]. BaSrTiO_3 (BST) has also been investigated for use in memory devices, although a MIM structure, instead of the conventional MIS structure, may be required to avoid interfacial oxides. Ferroelectric random access memory (FeRAM) devices have been developed using $\text{Pb}(\text{Zr,Ti})\text{O}_3$ (PZT) and $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT) dielectrics and are expected to replace DRAM devices [14]. For high- k gate applications, HfO_2 films deposited by CVD are promising. Many other films have been investigated for high- k gate dielectrics [1, 13].

Other methods that have been successfully employed for depositing high- k dielectric materials include MBE and PVD [1, 13]. Recently, HfSiON films deposited by PVD exhibited very good dielectric properties [15]. MBE was used to deposit SrTiO_3 films with an EOT $< 10 \text{ \AA}$ [1]. However, PVD and MBE do have some significant problems. PVD suffers from problems with sputtering damage and is a line-of-sight technique. MBE has an inherently slow throughput [1].

For future deposition of ultra-thin high- k materials, the need to deposit conformal films with precise thickness control becomes much more critical. ALD is a CVD-derived thin film deposition technique that appears to be the most promising technique for the deposition of ultrathin films of high- k materials for future microelectronics applications [1, 13]. ALD is based on the application of sequential, self-limiting surface reactions [5]. ALD may be considered a type of CVD where the gas phase precursors are introduced alternately instead of simultaneously.

A cartoon illustrating the sequential, self-limiting surface reactions that define ALD is shown in Fig. 10.1. Two sequential surface reactions, A and B, produce the ALD thin film growth. Because there are only a finite number of chemical species on the surface, both reactions are self-limiting. The chemical species are exchanged during each surface reaction. In the A reaction, the gas phase precursor reacts with the chemical species left by the B reaction. In the B reaction, the gas phase precursor reacts with the chemical species left by the A reaction. ALD is achieved by repeating the surface reactions in an ABAB... sequence.

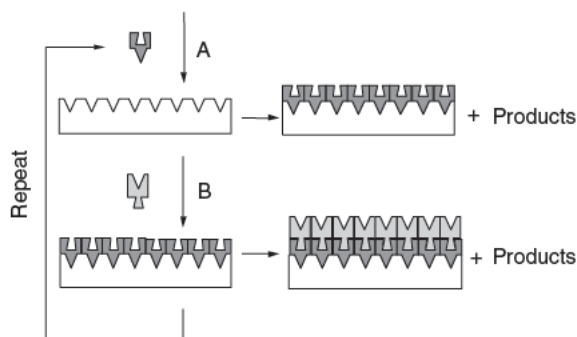


Fig. 10.1 Two sequential, self-limiting surface reactions that define ALD.

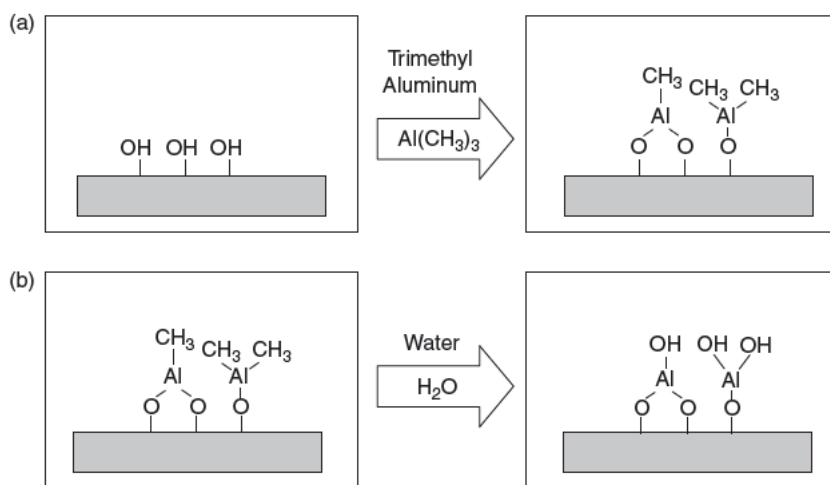
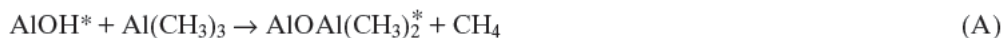


Fig. 10.2 Illustration of the two, sequential, self-limiting surface reactions that define Al_2O_3 ALD.

Al_2O_3 ALD can be used to describe ALD thin film growth. Al_2O_3 ALD is based on the CVD reaction: $2\text{Al}(\text{CH}_3)_3 + 3\text{H}_2\text{O} \rightarrow \text{Al}_2\text{O}_3 + 6\text{CH}_4$. To achieve Al_2O_3 ALD, this binary CVD reaction can be divided into two separate reactions [16, 17]:



where the asterisks designate the surface species. These two separate surface reactions are defined in Fig. 10.2.

During Al_2O_3 ALD film growth, $\text{Al}(\text{CH}_3)_3$, the gas phase precursor in the A reaction, reacts with hydroxyl groups on the substrate until this surface reaction reaches completion. Subsequently, $\text{Al}(\text{CH}_3)_3$ is pumped or carried away. The same process is then repeated with H_2O , the gas phase precursor in the B reaction. This procedure completes one AB cycle that deposits approximately one monolayer of Al_2O_3 .

These AB cycles are repeated to achieve the desired Al_2O_3 film thickness. The Al_2O_3 ALD growth rate is extremely linear with number of AB cycles. Figure 10.3 shows the linear growth during Al_2O_3 ALD measured using both ellipsometry and stylus profilometer measurements. The Al_2O_3 ALD growth rate is $\sim 1.2 \text{ \AA}$ per AB cycle at a growth temperature of 177°C [17]. The Al_2O_3 ALD films are also extremely flat and conformal to the underlying substrate. Previous atomic force microscope measurements have confirmed that the surface roughness is only nominally larger than the original underlying substrate [17]. The surface roughness remains nearly constant versus number of AB cycles [17, 18].

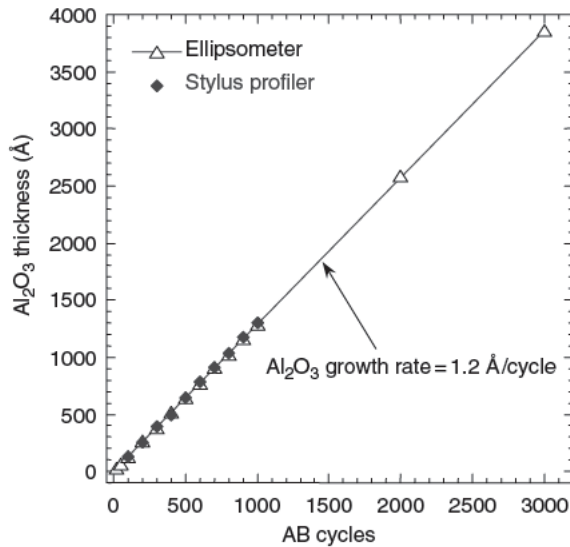


Fig. 10.3 Al₂O₃ ALD film thickness versus AB cycles showing linear growth during Al₂O₃ ALD. The Al₂O₃ ALD film thickness was measured using ellipsometry and stylus profilometry.

ALD is the only technique that combines the ability to grow thin films with atomic layer thickness control with the ability to coat conformally complex 3D structures. Conformality is achieved because the surface reactions are self-limiting [5]. For example, reactions may occur initially and reach completion at the opening of a trench. After this surface area reacts, the gas phase precursors can progressively reach surface area further down in the trench. As a function of reaction time, the reactants can eventually reach the surface area at the bottom of the trench. The chemical species at the bottom of the trench will react until the reaction reaches completion. Conformality is achieved because the maximum deposition is defined only by the surface density of chemical species.

Since the two reactants are present individually in the reaction chamber, ALD also avoids the gas phase particle generation problems associated with CVD. The deposition of these gas phase particles often leads to very granular depositions during CVD. The roughness of the ALD films is also extremely low, particularly for amorphous ALD films such as Al₂O₃ [18]. Because the surface reactions reach completion during each A and B reaction, there is negligible statistical randomness to the ALD growth process. ALD films are generally extremely continuous and pinhole-free. This characteristic is important for the application of ALD films as dielectric insulators. Moreover, deposition temperatures for ALD are generally lower than the temperatures required for CVD.

ALD has been used to deposit numerous high-*k* materials that could be used to replace SiO₂ in memory and gate dielectric applications. Al₂O₃ films grown by ALD are already being used as capacitors in DRAMs by Samsung [19, 20]. For this application, the low processing

temperature and the ability of ALD to coat uniformly intricate 3D structures was important. Several commercial ALD reactors are available, including those by ASM Microchemistry [21] and by Genus [22]. Many more companies are currently investing in ALD technology and more vendors will be providing products in the near future.

10.5 High- k dielectric materials

10.5.1 Binary oxides grown by ALD

Most of the known binary metal oxide high- k materials have been grown by ALD. These binary metal oxide materials include, approximately in order of increasing dielectric constant, Al_2O_3 , Y_2O_3 , CeO_2 , HfO_2 , ZrO_2 , Ta_2O_5 , TiO_2 , La_2O_3 , and Nb_2O_5 . The dielectric constants of these thin films grown by ALD range from $k < 10$ to $k > 100$. These dielectric constants are comparable with the dielectric constants measured for the same materials grown by other methods.

10.5.1.1 Al_2O_3

Al_2O_3 is the most widely studied high- k material grown by ALD. Al_2O_3 films grown by ALD are already used in DRAMs [19, 20]. Al_2O_3 films can be deposited rapidly by ALD. AB cycle times on the order of a second can be achieved in commercial reactors [22]. Furthermore, a variety of precursors can be used to grow Al_2O_3 by ALD [6].

Al_2O_3 exhibits excellent insulating properties. These favorable properties result from the large Al_2O_3 bandgap of 9 eV and the large barrier height of 2.8 eV when in contact with silicon [12]. Recent electrical investigations have measured the current–voltage (IV) and capacitance–voltage (CV) characteristics for Al_2O_3 ALD films on Si(100) [23]. The IV plots are excellent and display a very low leakage density on the order of $\sim 1 \text{ nA/cm}^2$. Various IV curves for Al_2O_3 ALD films of different thickness on Si(100) are shown in Fig. 10.4. These IV curves display behavior that is characteristic of Fowler–Nordheim tunneling.

Al_2O_3 is thermodynamically stable on silicon. However, SiO_2 or aluminum silicate layers are often formed at the $\text{Al}_2\text{O}_3/\text{SiO}_2$ interface. These interfacial SiO_2 layers appear to be inevitable, in part, because growth often does not occur under equilibrium conditions [1]. The interfacial SiO_2 layer will seriously compromise the dielectric constant that can be obtained from gate stacks. The dielectric constants for Al_2O_3 ALD films of various thickness on Si(100) are shown in Fig. 10.5. The reduction of the dielectric constant for thinner Al_2O_3 ALD film thicknesses is attributed to an interfacial SiO_2 layer with a thickness of $\sim 10\text{--}12 \text{ \AA}$ [23]. The calculations in Fig. 10.5 show the predicted behavior for a SiO_2 interfacial layer of $11 \text{ \AA}$ including quantum mechanical corrections.

Al_2O_3 ALD films hold promise for memory and gate dielectric applications. For memory applications, the interfacial SiO_2 problem can be avoided by using non-silicon electrodes.

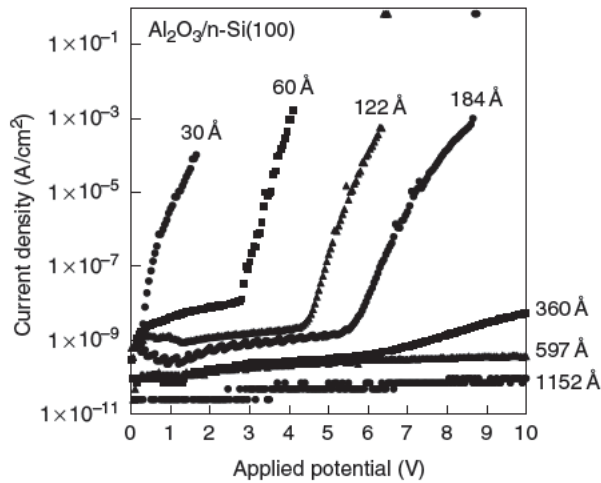


Fig. 10.4 Current–voltage (*IV*) plots for Al_2O_3 ALD films of different thicknesses grown on n-Si(100) at 177°C.

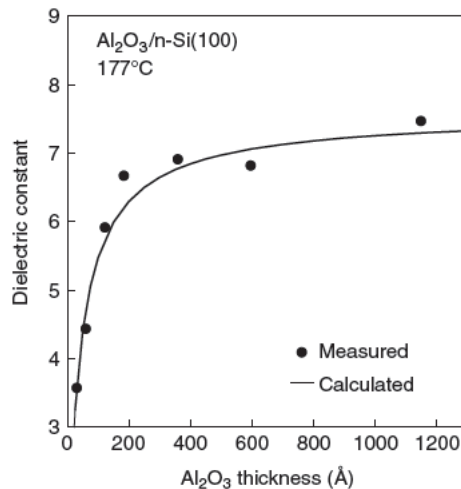


Fig. 10.5 Comparison of the measured and calculated dielectric constants for Al_2O_3 ALD films of different thicknesses grown on n-Si(100) at 177°C.

However, the interfacial SiO_2 is a serious problem for gate dielectric applications because the gate dielectric must be deposited directly on the silicon channel. Even if the interfacial SiO_2 problem can be minimized or avoided, the relatively low dielectric constant of $k \sim 8\text{--}10$ for Al_2O_3 is likely to limit its use to only a couple of generations before needing a dielectric with a higher k .

The earliest dielectric constant reported for Al_2O_3 ALD films was $k = 7.1$ [24]. Others who reported dielectric constants for relatively thick Al_2O_3 ALD films measured $k = 8.4$ [25],

$k = 5.3$ [26], $k = 8.5$ [27], $k = 7$ [28], $k = 8.1$ [29], and $k = 9.8$ [30]. A recent study examined ultra-thin Al_2O_3 ALD films with thicknesses down to 1 nm [31, 32]. Dielectric constants of $k \sim 10$ –11 were reported for the Al_2O_3 film. However, an interfacial SiO_2 layer with a thickness of 0.75 nm was present that reduced the overall dielectric constant of the gate stack.

Al_2O_3 ALD is possible not only on silicon but on a variety of substrates including various transition metals, alloys, oxides, and even noble metals [23]. Good electrical properties were measured for Al_2O_3 ALD on most of these substrates. The measured dielectric constant was consistently determined to be $k \sim 8$.

10.5.1.2 Y_2O_3

Dielectric constants ranging from $k = 12$ to $k = 20$ have been reported for Y_2O_3 [1]. However, as often observed for a variety of high- k dielectrics, silicate layers have been observed at the interface with silicon. These silicate layers produced much lower overall dielectric constant values. Y_2O_3 growth has been reported by ALD [32]. Dielectric constants of $k \sim 15$ and low leakage currents were observed for Y_2O_3 ALD films grown using $\text{Y}(\text{thd})_3$ and ozone. These films were polycrystalline and had a SiO_x interfacial layer with a thickness of ~ 1.1 nm. Y_2O_3 ALD growth has also been reported using various beta-diketonate yttrium precursors with ozone at temperatures of 250–375°C [33]. Unfortunately, no electrical measurements were reported in this study.

10.5.1.3 CeO_2

The dielectric constant of CeO_2 has been reported as $k = 20$ [4] and $k = 26$ [34]. CeO_2 ALD growth has been performed using $\text{Ce}(\text{thd})_4$ and ozone [35]. A later study compared $\text{Ce}(\text{thd})_3$ phen and $\text{Ce}(\text{thd})_4$ precursors for CeO_2 ALD films grown at lower temperatures [34]. The CeO_2 ALD films were polycrystalline. The preferred $\text{Ce}(\text{thd})_4$ precursor displayed CeO_2 ALD growth from 175–275°C. However, no electrical measurements were reported for these CeO_2 ALD films.

10.5.1.4 HfO_2

HfO_2 ALD growth has been reported using HfCl_4 and H_2O precursors [32]. These HfO_2 ALD films displayed a dielectric constant of $k \sim 20$. HRTEM images showed uniform, mostly amorphous HfO_2 films grown on a SiO_2 -covered Si substrate. Low leakage currents were measured during the electrical testing. Nucleation problems during HfO_2 ALD were observed on H-passivated silicon surfaces (so-called ‘HF-last’). These HfO_2 films also exhibited much higher leakage currents. In addition, a thin interfacial layer seems to be present in the HRTEM images.

Self-aligned n-channel MOSFETs have been fabricated using 3 nm thick HfO_2 gate dielectric films grown by ALD [36]. These transistors exhibited promising results after an anneal at 1000°C. Thin sub-oxides were observed at the interfaces with the poly-Si gate and the Si-substrate. The total stack with a thickness of 4.6 nm had an EOT of 1.7 nm.

10.5.1.5 ZrO_2

ZrO_2 ALD film growth has been studied by several researchers. Polycrystalline ZrO_2 films were grown at 200–300°C using $\text{Zr}[\text{OC}(\text{CH}_3)_3]_4$ and H_2O and yielded a dielectric constant $k \sim 32$ [37]. Crystalline ZrO_2 films have also been deposited using ZrCl_4 and H_2O [38]. A thick amorphous interfacial layer of $< 5 \text{ \AA}$, with a k value higher than the SiO_2 dielectric constant, was detected after deposition on an originally H-passivated silicon substrate. Accounting for this interfacial layer, a dielectric constant of $k \sim 25\text{--}35$ was estimated for the ZrO_2 .

Uneven nucleation on the H-passivated Si substrate was suggested as a reason for the high leakage currents and uneven film morphology of the ZrO_2 films [38]. Nucleation problems have also been reported for ZrO_2 ALD films grown on H-passivated silicon. These nucleation problems are avoided by depositing on a thin SiO_2 layer on silicon [32]. A dielectric constant of $k = 23$ was reported for these ZrO_2 films using ZrCl_4 and H_2O precursors.

n-Channel MOSFET devices have been fabricated using ZrO_2 ALD films with a thickness of 5 nm [36]. These MOSFET devices are similar to the transistors described above using HfO_2 . Unfortunately, excessive gate leakage currents were observed for these devices. No capacitance measurements were performed because of the high leakage currents.

10.5.1.6 Ta_2O_5

Ta_2O_5 ALD has been performed using TaCl_5 and H_2O at 310°C [29] and $\text{Ta}(\text{OC}_2\text{H}_5)_5$ and H_2O at 300°C [39]. These Ta_2O_5 films produced dielectric constants of $k = 28$ and $k \sim 24$, respectively, for the as-deposited amorphous films. However, a large increase to $k = 52$ was observed after annealing above 600°C produced a polycrystalline phase. Annealing at low temperatures reduced leakage currents, probably due to a reduction in impurities. The leakage currents increased greatly upon crystallization at higher temperatures [39].

Additional studies reported a dielectric constant for Ta_2O_5 ALD films of $k = 25$ using $\text{Ta}(\text{OC}_2\text{H}_5)_5$ and H_2O [40]. A dielectric constant of $k = 23$ was also observed for a water-free ALD process using only $\text{Ta}(\text{OC}_2\text{H}_5)_5$ and TaCl_5 precursors [41]. Unfortunately, the Ta_2O_5 ALD surface chemistry does have some complications. There is a slow etching of Ta_2O_5 by TaCl_5 . $\text{Ta}(\text{OC}_2\text{H}_5)_5$ can also thermally decompose at $> 275^\circ\text{C}$. Ta_2O_5 films grown at 325°C exhibited lower Cl contamination and higher dielectric constants than films grown at 275°C [41].

10.5.1.7 La_2O_3

La_2O_3 ALD films have been deposited using $\text{La}(\text{thd})_3$ and O_3 [42]. Cubic La_2O_3 was formed at growth temperatures above 300°C and the hexagonal phase formed upon annealing at 800°C. Carbonate contamination decreased with growth temperature but was still significant ($\sim 3\%$) even at growth temperatures $> 400^\circ\text{C}$. The La_2O_3 films were unstable in air and no dielectric constant measurements were reported in this investigation. From other investigations, the dielectric constant of La_2O_3 was reported as $k = 30$ [1].

10.5.1.8 TiO₂

TiO₂ ALD film growth has been described in numerous papers [6]. However, no dielectric constant values have been reported in these studies. Previous researchers have indicated that their TiO₂ ALD films were too leaky to measure the dielectric constant [43]. Titanium precursors included TiCl₄, TiI₄, Ti(OCH(CH₃)₂)₄, and Ti(OC₂H₅)₄ [6]. H₂O and sometimes H₂O₂ were used as the oxygen precursor. Dielectric constant values for TiO₂ include $k = 50$ [4], $k = 80$ [1] and $k = 100$ [3] depending on the crystalline phase of the TiO₂.

10.5.1.9 Nb₂O₅

Nb₂O₅ ALD films have been grown using Nb(OC₂H₅)₅ and H₂O at temperatures from 150–350°C [44]. No electrical measurements were reported in this investigation. However, the same researchers indicated that Nb₂O₅ had a dielectric constant of $k = 50$ –200 with high leakage currents in a separate study [45]. In another investigation, a dielectric constant of $k = 163$ was measured for Nb₂O₅ ALD films grown at 325°C [46]. In similarity to TiO₂, the low resistivity of Nb₂O₅ films is attributed, in part, to slight deviations from the ideal stoichiometry [11, 46]. Monocrystalline Nb₂O₅ was reported to have a dielectric constant of $k = 35$ –50 [11].

10.5.2 Ternary perovskites grown by ALD

Perovskites tend to have very large dielectric constants due to their ferroelectric properties at temperatures below their Curie point [1]. These ceramics have a face-centered-cubic crystal structure and no net polarization of charge above their Curie point. Below this temperature, the ions shift to create a permanent dipole in the material and a very high dielectric constant.

There is some indication that the dielectric constant of perovskites decreases for thin films with thicknesses $< 1\ \mu\text{m}$ [2]. This lack of scalability may mean that perovskites do not have an advantage over other high- k materials for memory and logic applications. Problems may also arise due to the low Curie temperature of some of these perovskite materials. The lower Curie temperature will make those perovskites unsuitable for devices with high operating temperatures.

BaTiO₃ (BTO) ALD films have been deposited using barium(pentamethylcyclopentadienyl), titanium tetraisopropoxide and water precursors at 275°C [47]. These BaTiO₃ ALD films yielded a dielectric constant of $k = 165$ after annealing at 500°C. BaTiO₃ ALD has also been achieved using barium dipivaloyl-methane chelate (Ba(DPM)₂·2tetraene), titanium tetraisopropoxide and H₂O [48]. These films produced a dielectric constant of $k = 90$.

SrTiO₃ (STO) ALD films have been deposited using strontium bis(triisopropylcyclopentadienyl), titanium tetraisopropoxide and water precursors at 250–325°C [47, 49]. These STO ALD films yielded a dielectric constant of $k = 180$. Additional studies measured a dielectric constant of $k = 170$ using strontium dipivaloyl-methane chelate (Sr(DPM)₂·2tetraene), titanium tetraisopropoxide and H₂O [48].

Additional studies have tried to grow other perovskite materials. Attempts were made to deposit $\text{Bi}_4\text{Ti}_3\text{O}_{12}$ using triphenyl bismuth, titanium isopropoxide, and water precursors [50]. This effort yielded $\text{Bi}_2\text{Ti}_2\text{O}_7$ with a dielectric constant of $k \sim 60$ after annealing at 500°C . However, $\text{Bi}_2\text{Ti}_2\text{O}_7$ is not a perovskite. LaMnO_3 was also deposited using $\text{La}(\text{thd})_3$, $\text{Mn}(\text{thd})_3$ and ozone precursors at temperatures above 250°C [51]. Unfortunately, no dielectric constants were reported in this study.

10.5.3 *Properties of composite dielectric materials*

Because finding one high- k material that exhibits all the desired properties is difficult, there have been many efforts to combine different materials to obtain the desired properties. Depending on the manner in which the materials are combined, the composite materials may be referred to as mixed materials, solid solutions, doped materials, nanolaminates, or superlattices. Mixed materials and solid solutions refer to fairly homogeneous mixtures of different materials. Superlattices and nanolaminates are layered materials. Doping refers to the intentional introduction of small amounts of impurities into a material.

In many cases, the resultant composite materials tend to have properties that are somewhere between those that were combined to make the composite material. This expectation is often referred to as the ‘rule of mixtures’. However, this ‘rule of mixtures’ behavior is not always observed in practice. Combining materials can sometimes result in unusual and unexpected properties such as extremely high dielectric constants or negative differential resistance. For example, the perovskites SrTiO_3 and BaTiO_3 have high dielectric constants ($k > 100$). Much higher dielectric constants of $k \sim 10^3$ – 10^4 have been achieved when these perovskites are mixed to form $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ (BST) [2]. BST has been used in bulk capacitors and is being investigated for DRAM capacitor applications. Even higher dielectric constants of $k > 10^4$ have been achieved by doping high- k perovskites materials [3].

Composite dielectric materials are often fabricated to prevent the crystallization of high- k dielectrics under processing conditions. Metal oxides are alloyed with SiO_2 and Al_2O_3 to prevent their crystallization. The oxides of La, Hf, Zr, and Y have been alloyed with SiO_2 [2]. The dielectric constants of 50/50 alloys of these materials were predicted and, in some cases, measured to be approximately an average of the two materials.

The crystallization temperature increased approximately proportionally with Si concentration in the $\text{La}_2\text{O}_3/\text{SiO}_2$ alloy. The crystallization temperature increased from $\sim 400^\circ\text{C}$ for pure La_2O_3 to over 1000°C for an alloy with 70% SiO_2 content [2]. No crystallization was reported for $\text{La}_2\text{O}_3/\text{SiO}_2$ alloys above 70% SiO_2 content. Promising results have also been achieved with Si-doped zirconium aluminates [52]. These materials exhibit reasonably high dielectric constants of $k > 15$ without crystallization during typical processing conditions. Zr and Si dopants have also been used in Al_2O_3 to quench traps and reduce leakage currents [53].

ALD is particularly well suited for depositing mixed materials (solid solutions) and layered materials (nanolaminates, superlattices). The exact sequence of a large number of different reactant pulses used to deposit the film can be easily and precisely controlled during ALD. Various properties of composite materials can be tailored to meet the requirements for specific applications. Mixed materials can be deposited by alternately dosing the various precursors for the different materials. Nanolaminates are formed by depositing more than one monolayer of each material before switching to the other set of precursors. ALD allows for the precise control of the thickness of the individual layers. TEM images have shown that ALD can conformally and uniformly coat 3D structures with multilayer nanolaminates [22].

10.5.4 Composite materials grown by ALD

Many nanolaminates and solid solutions consisting of combinations of Al, Hf, Nb, Ta, and Zr oxides have been grown using ALD. Dielectric constants ranging from $k = 28$ to $k = 98$ were measured for mixed $\text{Nb}_x\text{Ta}_y\text{O}$ solutions and $\text{Nb}_2\text{O}_5/\text{Ta}_2\text{O}_5$ nanolaminates [54]. In addition, the leakage currents were lower than the leakage currents measured for the individual materials. The addition of ZrO_2 further reduced the leakage currents and yielded $k = 28\text{--}33$. Another study of the $\text{Nb}_x\text{Ta}_y\text{O}$ system was performed and reported dielectric constants as high as $k = 38$ with increasing Nb concentration [55]. Later studies investigated the temperature dependence of the electrical properties of $(\text{Nb}_{1-x}\text{Ta}_x)_2\text{O}_5$ films and measured $k = 24\text{--}38$ [46].

$\text{Ta}_2\text{O}_5/\text{HfO}_2$ nanolaminates have also been grown by ALD [56]. The dielectric constant of the nanolaminates varied between the dielectric constant of pure HfO_2 ($k = 16$) and pure Ta_2O_5 ($k = 25$). However, the leakage currents of the nanolaminates were many orders of magnitude lower than the pure materials. The low leakage is attributed to the nanolaminate structure hindering HfO_2 crystallization. Similar trends were observed for $\text{Ta}_2\text{O}_5/\text{Al}_2\text{O}_3$ and $\text{Ta}_2\text{O}_5/\text{ZrO}_2$ nanolaminates [57]. However, for the $\text{Ta}_2\text{O}_5/\text{ZrO}_2$ nanolaminates, the dielectric constant of $k \sim 28$ was higher than the dielectric constant of pure Ta_2O_5 ($k \sim 25$) or pure ZrO_2 ($k \sim 19$).

The dielectric properties of $\text{Nb}_2\text{O}_5/\text{Ta}_2\text{O}_5$ and $\text{Nb}_2\text{O}_5/\text{Al}_2\text{O}_3$ nanolaminates and solid solutions were also investigated more thoroughly in recent investigations [11]. The addition of Al and Ta to Nb_2O_5 dramatically decreased leakage currents by hindering crystallization. In the case of nanolaminates, crystallization was hindered by decreasing the Nb_2O_5 layer thickness. The measured dielectric constants were generally related to the percent composition of the material.

Ta_2O_5 and Al_2O_3 nanolaminates have displayed dielectric constants from $k = 8.1$ to $k = 28$ as the Ta_2O_5 layers became thicker and Al_2O_3 layers became thinner [29]. A related study showed similar results with dielectric constants rising from $k = 8.4$ to $k = 24$ with increasing percentage of Ta_2O_5 [25]. The leakage current of Ta_2O_5 also decreased drastically with the addition of Al_2O_3 . $\text{Al}_2\text{O}_3/\text{ZrO}_2$ dielectric stacks have also been deposited by ALD [58]. A NH_3 -treated silicon surface was used to deal with the nucleation problems of growing Al_2O_3 on H-passivated silicon. EOT thicknesses of < 1 nm were achieved using this approach while keeping leakage currents at ~ 1 mA/cm².

HfO_2 - SiO_2 and La_2O_3 - SiO_2 dielectric alloys have been grown to combine the crystallization resistance of SiO_2 with the high dielectric constants of HfO_2 and La_2O_3 [59]. No k values were reported in this work, but similar mixed films had dielectric constants between the dielectric constants of the individual films [2]. For the partially crystallized $\text{Zr}_x\text{Ti}_y\text{O}$ ALD films grown at 300°C , the dielectric constant was $k = 45$ – 65 when grown on ITO [43]. However, the effective dielectric constant was only $k = 35$ when grown on silicon. This lower dielectric constant probably resulted from an interfacial oxide layer.

The perovskite materials have also been explored in alloys and nanolaminates. Much of this work has focused on BaSrTiO_3 (BST). Several investigations have used ALD to fabricate $\text{SrTiO}_3/\text{BaTiO}_3$ solid solutions and nanolaminates [48, 60]. The maximum dielectric constant of $k = 450$ was measured for a 20/2 monolayer $\text{SrTiO}_3/\text{BaTiO}_3$ superlattice. This dielectric constant compares with $k = 170$ for SrTiO_3 and $k = 90$ for BaTiO_3 . The unusually high dielectric constants are attributed to the lattice strain at the $\text{SrTiO}_3/\text{BaTiO}_3$ interfaces. This lattice strain results in a change in polarization.

Dielectric relaxors are a class of dielectric materials with very high dielectric constants. Dielectric constants up to $k = 10000$ have been measured for La-doped PZT [4]. Even higher k values as high as $k = 65000$ have been measured for $\text{BaTi}_{1-x}\text{Sn}_x\text{O}_3$ [3]. No reports of the ALD growth of dielectric relaxors were found at the time of this review. However, this area remains an exciting possibility for ALD and awaits future research.

10.5.5 *Future use of ALD in device fabrication*

Most known high- k materials have been successfully deposited by ALD. These high- k materials deposited by ALD exhibit dielectric constants comparable with films grown by other techniques. The ease by which ALD can be used to grow mixed films and nanolaminates promises to facilitate the discovery of new composite high- k materials. These composite high- k materials can be designed for the best combination of high dielectric constant and low leakage current.

Despite all the promising research on alternate high- k materials, there are problems for microelectronics applications of high- k ALD films. The main problem is that the dielectric constant of high- k films tends to decrease significantly when the thickness is decreased to a few nanometers. For example, the dielectric constants for Al_2O_3 ALD films of various thickness on $\text{Si}(100)$ are shown in Fig. 10.5. The primary reason for this decrease is that many high- k dielectrics, such as Al_2O_3 , tend to form interfacial SiO_2 when in contact with silicon. The interfacial oxide reduces the gains that can be achieved with high- k materials. The elimination of this interfacial SiO_2 is a critical goal that should be the focus of future research.

Materials with very large dielectric constants, like perovskites, also do not appear to be scalable. The crystal structures that lead to the high- k values are no longer present in thin films. This lack of scalability will restrict the application of perovskites to devices with thicker dielectric films.

Researchers are also investigating alternate device designs in conjunction with high-*k* research [2]. Many of these devices are vertical designs rather than the conventional planar designs. Vertical designs will allow for increased device density. These vertical designs include high surface area trench capacitors [20] and vertical transistor geometries [61]. ALD allows for the uniform, conformal coating of complex 3D structures. Consequently, ALD is uniquely suited for fabricating these vertical device structures.

Al₂O₃ ALD films have been used to coat uniformly high surface area, cylinder-type poly-Si to make 1 Gbit DRAM [20]. By using a TiN top electrode to make a MIS structure, a 1 Gbit DRAM has been achieved with a cell capacitance of 30 fF and a leakage current of only 0.5 fA/cell at 1.2 V. Vertical replacement-gate (VRG) n-MOSFET devices have also been produced using Al₂O₃ and HfO₂ films grown by ALD [61]. The devices fabricated using HfO₂ films had an EOT of only 15 Å with very low leakage currents densities of 10⁻⁷ A/cm². This geometry produced 50 nm transistors that was a record as of 2001. Lastly, a new approach for high-density flash memory involves using Si quantum dots grown on a thin tunneling dielectric. A recent study has shown that Al₂O₃ tunneling dielectrics < 1 nm thick deposited by ALD are superior to the previously used Si₃N₄ and SiO₂ dielectrics [62].

10.6 Conclusions

Many promising high-*k* materials are currently being investigated as dielectric materials to replace SiO₂. However, the stringent requirements for microelectronics applications have proven extremely challenging. While some promising results have been obtained, the search for the ideal high-*k* material is continuing and leading towards various kinds of composite high-*k* materials and even new device structures. Atomic layer deposition (ALD) is an exciting and emerging deposition technology that promises to play a key role in enabling the fabrication of these new types of materials and structures. ALD facilitates the conformal, atomic layer controlled growth of high-*k* materials on 3D surfaces at temperatures that are generally lower than those required for CVD. ALD is also especially well suited for making various types of composite mixed materials and nanolaminates. The nanoengineering of materials using ALD has created composite materials that combine the desirable properties of different materials. These nanocomposites can also sometimes exhibit unexpectedly high dielectric constants. The ability of ALD to coat complex structures with thin high-*k* films is also essential for the development of some new alternate device structures.

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