Intel Increases Transistor Speed by Building Upward

By John Markoff
May 4, 2011

HILLSBORO, Ore. — Intel announced on Wednesday that it had again found a way to make computer chips that could process information more quickly and with less power in less space.

The transistors on computer chips — whether for PC's or smartphones — have been designed in essentially the same way since 1959 when Robert Noyce, Intel's co-founder, and Jack Kilby of Texas Instruments independently invented the first integrated circuits that became the basic building block of electronic devices in the information age.

These early transistors were built on a flat surface. But like a real estate developer building skyscrapers to get more rentable space from a plot of land, Intel is now building up. When the space between the billions of tiny electronic switches on the flat surface of a computer chip is measured in the width of just dozens of atoms, designers needed the third dimension to find more room.

The company has already begun making its microprocessors using a new 3-D transistor design, called a Finfet (for fin field-effect transistor), which is based around a remarkably small pillar, or fin, of silicon that rises above the surface of the chip. Intel, based in Santa Clara, Calif., plans to enter general production based on the new technology some time later this year.

Although the company did not give technical details about its new process in its Wednesday announcement, it said that it expected to be able to make chips that run as much as 37 percent faster in low-voltage applications and it would be able to

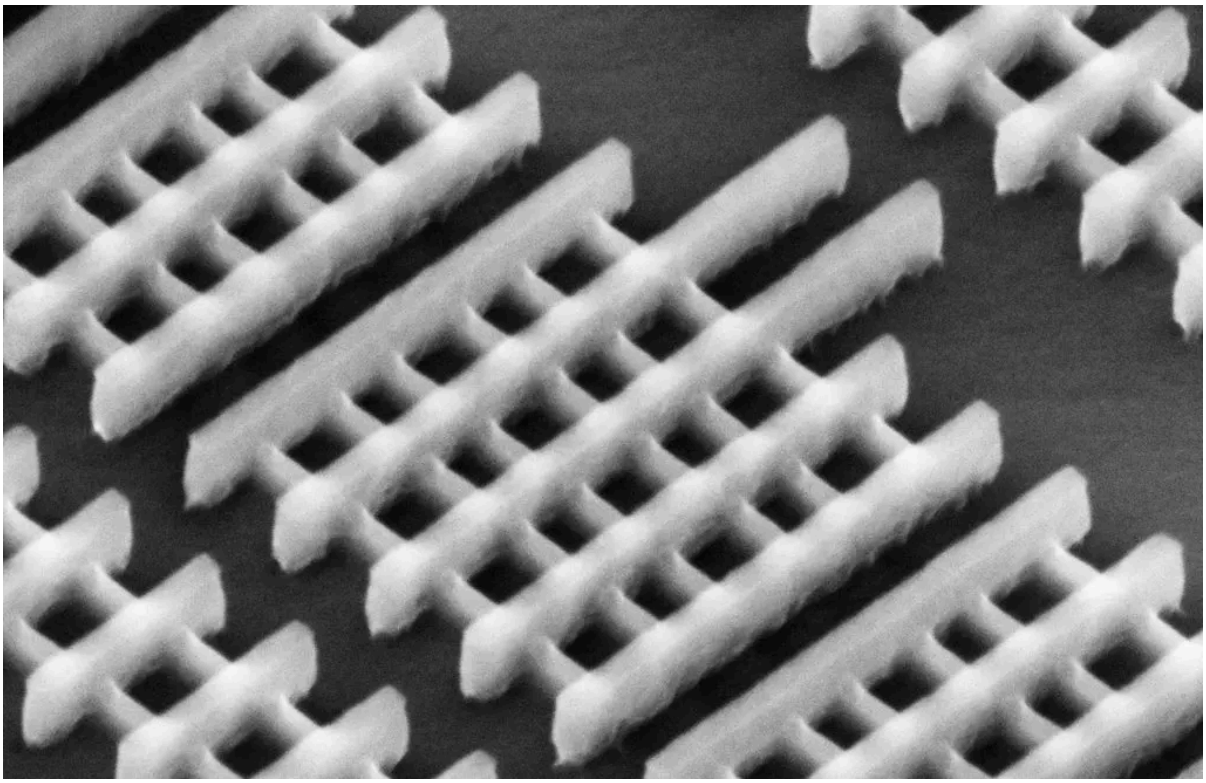
cut power consumption as much as 50 percent.

Intel currently uses a photolithographic process to make a chip, in which the smallest feature on the chip is just 32 nanometers, a level of microscopic manufacture that was reached in 2009. (By comparison a human red blood cell is 7,500 nanometers in width and a strand of DNA is 2.5 nanometers.) “Intel is on track for 22-nanometer manufacturing later this year,” said Mark T. Bohr, an Intel senior fellow and the scientist who has overseen the effort to develop the next generation of smaller transistors.

The company’s engineers said that they now felt confident that they would be able to solve the challenges of making chips through at least the 10-nanometer generation, which is likely to happen in 2015.

The timing of the announcement Wednesday is significant, Dr. Bohr said, because it is evidence that the world’s largest chip maker is not slipping from the pace of doubling the number of transistors that can be etched onto a sliver of silicon every two years, a phenomenon known as Moore’s Law. Although not a law of physics, the 1965 observation by Intel’s co-founder, Gordon Moore, has defined the speed of innovation for much of the world’s economy. It has also set the computing industry apart from other types of manufacturing because it has continued to improve at an accelerating rate, offering greater computing power and lower cost at regular intervals.

However, despite its promise and the company’s bold claims, Intel’s 3-D transistor is still a controversial technology within the chip industry. Indeed, a number of the company’s competitors say they believe that Intel is taking a what could be a disastrous multibillion-dollar gamble on an unproved technology.



Intel's new transistors have tiny pillars, or fins, that rise above the chip's surface.

There has been industry speculation that Finfet technology will give Intel a clear speed advantage, but possibly less control over power consumption than alternative approaches.

By opting for a technology that emphasizes speed over low power, Intel faces the possibility that it could win the technology battle and yet lose the more important battle in the marketplace. The scope of Intel’s gamble is underscored by the fact that while the company dominates in the markets for data center computers, desktops and laptops, it has largely been locked out of the tablet and smartphone markets, which are growing far more quickly than the traditional PC industry.

Those devices use ultra-low-powered chips to conserve battery power and reduce overheating. Apple, for example, uses Intel’s microprocessors for its desktops and laptops, but for the iPhone and iPad it has chosen to use a rival low-power design, built by others, that Apple originally helped pioneer in the late 1980s.

Industry executives and analysts have said that Intel is likely to have a lead of a full generation over its rivals in the shift to 3-D transistors. For example, T.S.M.C., the Taiwan-based chip maker, has said that it does not plan to deploy Finfet transistor technology for another two years.

Other companies, like ST Microelectronics, are wagering that an alternative technology based on placing a remarkably thin insulating layer below traditional transistors will chart a safer course toward the next generation of chip manufacturing. They believe that the insulation approach will excel in low-power applications, and that could be a crucial advantage in consumer-oriented markets where a vast majority of popular products are both hand-held and battery-powered.

“Silicon-on-insulator could be a win in terms of power efficiency,” said David Lammers, the editor in chief of Semiconductor Manufacturing and Design Community, a Web site. “From what I am hearing from the S.O.I. camp, there is a consensus and concession that Finfets are faster. That’s the way you want to go for leading-edge performance.”

In a factory tour here last week, Intel used a scanning electronic microscope to display a computer chip made using the new 22-nanometer manufacturing process. Viewed at a magnification of more than 100,000 times, the silicon fins are clearly visible as a series of walls projected above a flat surface.

It is possible to make transistors out of one or a number of the tiny fins to build switches that have different characteristics, such as faster switching speeds or extremely low power. Looking at the chip under less magnification, it is possible to see the wiring design, which appears much like a street map displaying millions of intersections.

Despite the impressive display, Intel’s executives acknowledge the challenge the company is facing in trying to catch up in the new consumer markets that so far have eluded it.

“The ecosystem right now is not aligned in our favor,” said Andy D. Bryant, Intel’s chief administrative officer, who now runs the company’s technology and manufacturing group. “It has to be good enough for the ecosystem to take notice and say, ‘We better pay attention to those guys.’ ”

A correction was made on May 4, 2011*: An earlier version of this article misspelled the dateline as Hillsborough.*

When we learn of a mistake, we acknowledge it with a correction. If you spot an error, please let us know at nytnews@nytimes.com. Learn more

A version of this article appears in print on , Section B, Page 1 of the New York edition with the headline: To Enhance Chip Speed, Intel Enters 3rd Dimension