

High-Performance Metal/High- k n- and p-MOSFETs With Top-Cut Dual Stress Liners Using Gate-Last Damascene Process on (100) Substrates

Satoru Mayuzumi, Shinya Yamakawa, *Member, IEEE*, Yasushi Tateshita, Tomoyuki Hirano, Masashi Nakata, Shinpei Yamaguchi, Kaori Tai, Hitoshi Wakabayashi, *Member, IEEE*, Masanori Tsukamoto, and Naoki Nagashima

Abstract—Newly proposed mobility-booster technologies are demonstrated for metal/high- k gate-stack n- and pMOSFETs. The process combination of top-cut SiN dual stress liners and damascene gates remarkably enhances local channel stress particularly for shorter gate lengths in comparison with a conventional gate-first process. Dummy gate removal in the damascene gate process induces high channel stress, because of the elimination of reaction force from the dummy gate. PFETs with top-cut compressive stress liners and embedded SiGe source/drains are performed by using atomic layer deposition TiN/HfO₂ gate stacks with $T_{\text{inv}} = 1.4$ nm on (100) substrates. On the other hand, nFETs with top-cut tensile stress liners are obtained by using HfSi_x/HfO₂ gate stacks with $T_{\text{inv}} = 1.4$ nm. High-performance n- and pFETs are achieved with $I_{\text{on}} = 1300$ and $1000 \mu\text{A}/\mu\text{m}$ at $I_{\text{off}} = 100 \text{ nA}/\mu\text{m}$, $V_{\text{dd}} = 1.0 \text{ V}$, and a gate length of 40 nm, respectively.

Index Terms—HfO₂, HfSi_x, Channel stress, damascene gate, electron mobility, embedded SiGe (eSiGe), gate last, high- k , hole mobility, metal gate, replacement gate, stress simulation, TiN, top-cut stress liner.

I. INTRODUCTION

METAL/HIGH- k gate stacks have been recently investigated for T_{inv} scaling, the reduction of gate leakage currents, and the suppression of V_{th} variations. The gate-last damascene process having dual band-edge work function metals is one of the candidates to achieve high-performance MOSFETs [1]–[4]. The damascene gate process has an advantage in the work function stability of metal electrodes to accomplish low V_{th} MOSFETs, because of the low-temperature process. Moreover, we have reported that the damascene gate process considerably enhances channel stress from embedded SiGe (eSiGe) source/drains, due to dummy gate removal [5]. The SiN stress liner is another important technology to enhance MOSFETs performance [6], [7]. The stress liners that are applied for the damascene gate devices are cut to remove the dummy gates, as shown in Fig. 1. It has been reported that

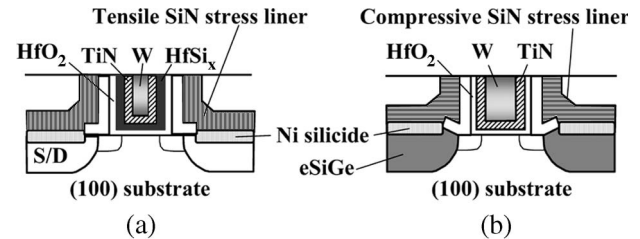


Fig. 1. Schematic diagrams of metal/high- k gate stack MOSFETs with top-cut stress liners using damascene gate process. (a) nFET. (b) pFET. Stress liners are cut on the top of gate electrodes.

discontinuous stress liners maintain high mobility for fully silicided gate MOSFETs [8]. However, the effects have been unclear for the damascene gate devices using the stressors yet.

In this paper, we present drivability effects on metal/high- k MOSFETs using the SiN stress liners with the damascene gate process and eSiGe. After device fabrication, channel stresses from both the top-cut dual stress liners and eSiGe will be discussed by using stress and mobility simulations in the damascene gate process. Then n- and pFETs with the stress enhancement technologies using dual work function metal/high- k gates are going to be demonstrated. After that, the advantages in the damascene gate technologies are going to be described by using benchmarks.

II. EXPERIMENTS

Cross-sectional structures of n- and pFETs are schematically shown in Fig. 1. The devices consist of metal/high- k gate stacks, top-cut SiN stress liners, and eSiGe, for only pFETs, on (100) substrates. A flow of device fabrication is shown in Fig. 2. MOSFETs are fabricated on the basis of the gate-last damascene process. After poly-Si dummy gate formation, Si recess was carried out and selective epitaxial films of eSiGe were formed by using dummy gates and spacers for only pFETs. SiN stress liners with 1.6-GPa tensile stress (t-SL) and 2.0-GPa compressive stress (c-SL) were deposited for n- and pFETs, respectively, after Ni silicidation. The stress liners were cut only on the top of dummy gates by using CMP to expose dummy gate tops after premetal dielectric (PMD) deposition. To improve mobility in the thinner T_{inv} region, ozone water treatment was used prior to HfO₂ atomic layer deposition (ALD) after dummy gate removal [9]. After postdeposition anneal at 500 °C, HfSi_x was deposited by utilizing physical vapor deposition for

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S. Mayuzumi is with Semiconductor Business Group, Sony Corporation, Atsugi 243-0014, Japan, and also with the School of Science and Engineering, Meiji University, Kanagawa 214-8571, Japan (e-mail: Satoru.Mayuzumi@jp.sony.com).

S. Yamakawa, Y. Tateshita, T. Hirano, M. Nakata, S. Yamaguchi, K. Tai, H. Wakabayashi, M. Tsukamoto, and N. Nagashima are with Semiconductor Business Group, Sony Corporation, Atsugi 243-0014, Japan.

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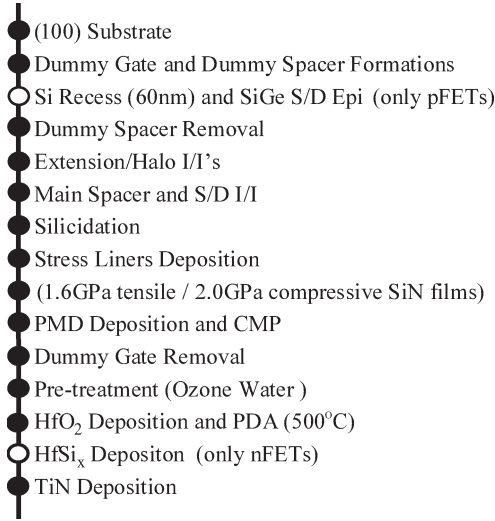


Fig. 2. Fabrication flow using gate-last damascene process for metal/high-*k* gate MOSFETs with SiN stress liners and eSiGe on (100) substrates.

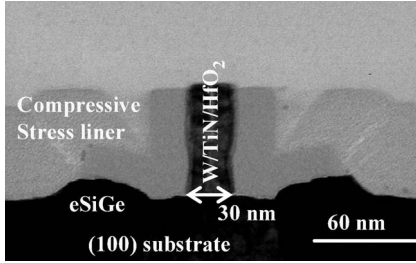


Fig. 3. Cross-sectional TEM image of pFET with W/TiN/HfO₂ gate stacks, c-SL, and eSiGe on (100) substrate. MOSFETs with 30-nm gate length were fabricated.

only nFETs. Following that, TiN was formed by using ALD for n- and pFETs. Fig. 3 shows a cross-sectional transmission-electron-microscope (TEM) image of a fabricated pFET. We successfully integrated top-cut stress liners into damascene gate devices with eSiGe and 30-nm gate length. For reference, metal/high-*k* and poly-Si/SiO₂ gate MOSFETs without top-cut stress liners were also fabricated.

III. STRESS AND MOBILITY SIMULATIONS

To investigate stress distributions around a channel, we simulated lateral (S_{xx}) and vertical (S_{zz}) stress distributions at four critical steps in the fabrication process: (a) after c-SL deposition; (b) after PMD CMP; (c) after dummy gate removal; and (d) after metal gate formation. Simulated S_{xx} and S_{zz} distributions around the channel of pFETs are shown in Figs. 4 and 5, where a gate length is 40 nm, and eSiGe and c-SL thicknesses are 80 and 60 nm, respectively. Fig. 6 shows average channel stress between the gate center and edge at a depth of 1 nm from the Si surface for simulated S_{xx} and S_{zz} , and relative hole mobility, corresponding to the four process steps in Figs. 4 and 5. The relative hole mobility was calculated by using simulated average values of the S_{xx} and S_{zz} , and piezoresistance coefficients [10]

$$\frac{\mu_{h_{xx}}}{\mu_{h_0}} = 1 - 0.718S_{xx} + 0.663S_{yy} + 0.011S_{zz} \quad (1)$$

where $\mu_{h_{xx}}$, μ_{h_0} , and S_{yy} are hole mobility in lateral, hole mobility without stress, and channel stress along the *y*-axis (Fig. 4), respectively. Equation (1) indicates that the hole mobility is enhanced by increases in compressive and tensile stress for the S_{xx} and S_{zz} , respectively, and also that the coefficient of the S_{xx} is approximately 70 times larger than that of the S_{zz} . As shown in Fig. 6, compressive S_{xx} after the PMD CMP slightly decreases in comparison with that after the c-SL deposition. However, after the dummy gate removal, compressive S_{xx} dramatically increases because of the elimination of reaction force from the dummy gate. On the other hand, tensile S_{zz} after the metal gate formation decreases, as compared to that after the c-SL deposition. Despite the decrease in the tensile S_{zz} , the hole mobility after the metal gate formation is greater than that after the c-SL deposition due to the large compressive S_{xx} , as shown in Fig. 6 and its large coefficient in (1).

Similarly, calculated average channel stress and relative electron mobility for nFETs are shown in Fig. 7, where a gate length and t-SL thickness are 40 and 25 nm, respectively. The relative electron mobility is expressed as

$$\frac{\mu_{e_{xx}}}{\mu_{e_0}} = 1 + 0.316S_{xx} + 0.176S_{yy} - 0.534S_{zz} \quad (2)$$

where $\mu_{e_{xx}}$ and μ_{e_0} are electron mobility in lateral and without stress, respectively. Equation (2) indicates that the electron mobility is enhanced by increases in tensile and compressive stress for the S_{xx} and S_{zz} , respectively. After the metal gate formation, tensile S_{xx} and S_{zz} increase, as compared to those after the t-SL deposition. Because of the relatively large coefficient of the S_{zz} in (2), an increase in the electron mobility are small in comparison with that in the hole mobility. However, due to the comparatively large increase in the tensile S_{xx} , the electron mobility after the metal gate formation is slightly higher than that after the t-SL deposition. Therefore, it is considered that both the hole and electron mobilities of damascene gate MOSFETs are enhanced by applying each top-cut stress liner.

IV. RESULTS AND DISCUSSION

A. Characteristics of pFETs

The dependence of peak transconductances ($g_{m,peak}$) on gate length for no-eSiGe pFETs with and without the c-SL is shown in Fig. 8. V_{th} roll-off characteristics of the devices are almost the same. Higher $g_{m,peak}$ indicates hole mobility enhancement because of the top-cut c-SL in the damascene gate process. Fig. 9 shows I_{on} dependence on $1/T_{inv}$ for poly-Si/SiO₂ and TiN/HfO₂ gate stacks without eSiGe. The I_{on} is extracted at $I_{off} = 100$ nA/ μ m and $V_{gs} = V_{ds} = -1.0$ V. A 60-nm c-SL achieves 46% I_{on} enhancement. Fig. 10 shows the relationship between normalized I_{on} ($I_{off} = 100$ nA/ μ m, $V_{ds} = V_{gs} = -1.0$ V) and c-SL thicknesses with and without eSiGe. The I_{on} increases with an increase in the c-SL thickness. The combination of a 40-nm c-SL and 80-nm eSiGe achieves more than 200% I_{on} enhancement in comparison with neither c-SL nor eSiGe. Therefore, it is confirmed that the drivability of eSiGe-S/D pFETs is further enhanced by the top-cut c-SL.

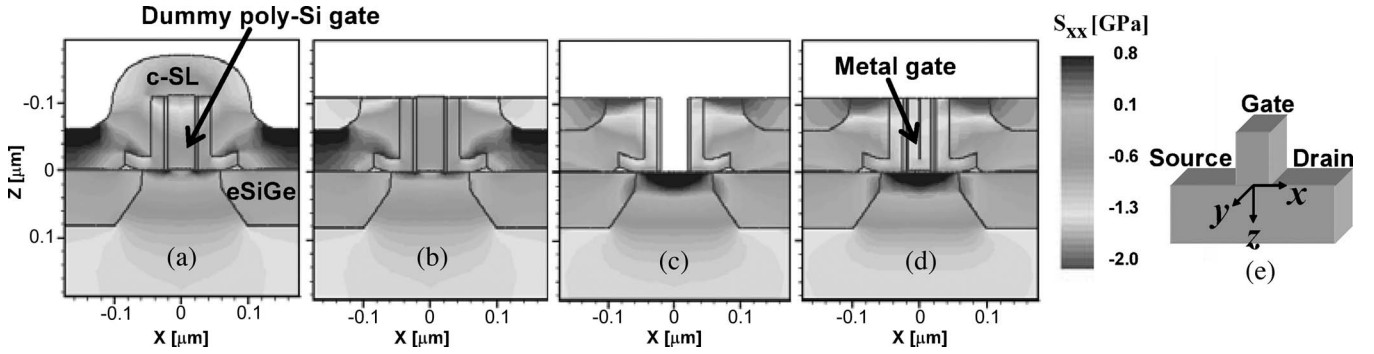


Fig. 4. Simulated lateral channel stress (S_{xx}) distributions for pFETs. (a) After c-SL deposition. (b) After PMD CMP. (c) After dummy gate removal. (d) After metal gate formation. (e) Axial directions in stress simulation. A gate length is 40 nm, and eSiGe and c-SL thicknesses are 80 and 60 nm, respectively.

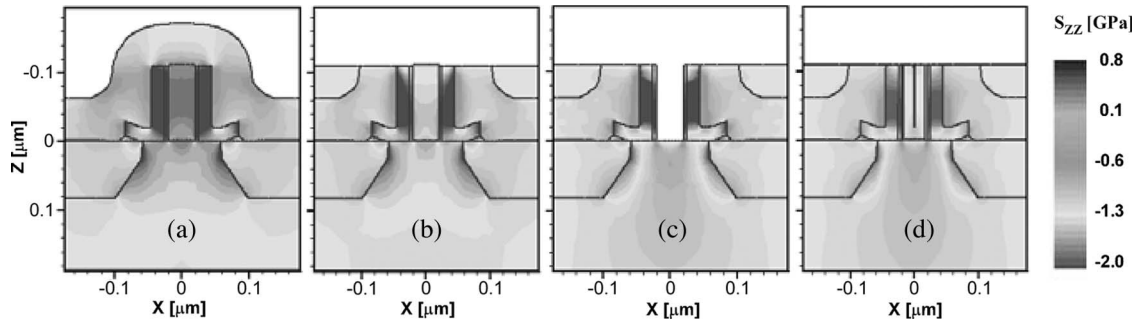


Fig. 5. Simulated vertical channel stress (S_{zz}) distributions for pFETs. Symbols of (a) to (d) correspond to the process steps, as shown in Fig. 4.

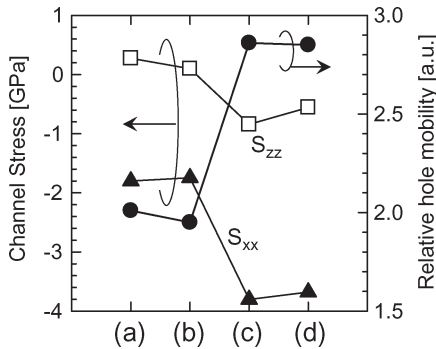


Fig. 6. Simulated S_{xx} and S_{zz} and relative hole mobility for pFETs, calculated by using piezocoefficients. Symbols of (a) to (d) correspond to the process steps, as shown in Figs. 4 and 5.

The dependence of I_d gain on gate length, due to the top-cut c-SL, is shown in Fig. 11, where the I_d gain means a fraction of I_d with and without the top-cut c-SL at a gate overdrive ($V_{gs} - V_{th}$) of -0.7 V. The I_d gain increases continuously with a decrease in the gate length for both linear and saturation regions. On the other hand, conventional gate-first pFETs have been reported that the I_d gain is saturated due to an increase in the surface doping concentration [6], [7]. This is possibly because of the process combination of the top-cut c-SL, eSiGe, and damascene gate. It seems that high channel stress is induced even for damascene gate pFETs with shorter gate lengths. Fig. 12 shows $I_{on}-I_{off}$ characteristics at $V_{ds} = V_{gs} = -1.0$ V, where c-SL and eSiGe thicknesses are 40 and 80 nm, respectively. I_{on} enhancement rates at $I_{off} = 100$ nA/ μm are 28% for no eSiGe and 35% for eSiGe devices. Excellent drivability enhancement is achieved by using the top-

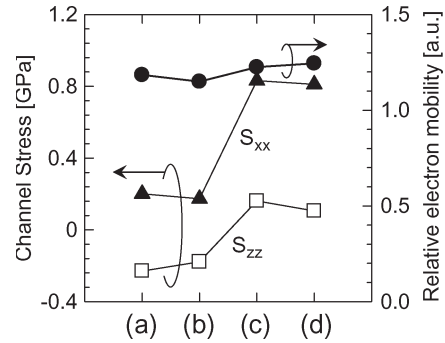


Fig. 7. Simulated S_{xx} and S_{zz} and relative electron mobility for nFETs at four critical steps in the fabrication process. (a) After t-SL deposition. (b) After PMD CMP. (c) After dummy gate removal. (d) After metal gate formation. A gate length and t-SL thickness are 40 and 25 nm, respectively.

cut c-SL and eSiGe for the damascene gate pFETs as supported by stress and mobility simulations.

B. Characteristics of nFETs

The dependence of $g_{m,peak}$ on gate length is shown in Fig. 13, where a t-SL thickness is 25 nm. Fig. 14 shows the $I_{on}-1/T_{inv}$ relationship for poly-Si/SiO₂ and HfSi_x/HfO₂ gate stack devices, where the I_{on} is extracted at $I_{off} = 100$ nA/ μm and $V_{ds} = V_{gs} = 1.0$ V. Higher $g_{m,peak}$ and 10% I_{on} enhancement are achieved by using the 25-nm top-cut t-SL. These results indicate that channel stress enhanced by the process combination of the top-cut t-SL and damascene gate improves the electron mobility. Fig. 15 shows I_d gain dependence on gate length, due to the top-cut t-SL, for linear and saturation currents, where gate overdrive is constant. I_d gains still increase

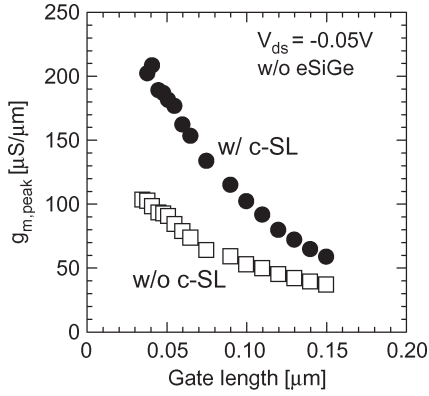


Fig. 8. Peak transconductance ($g_{m,peak}$) dependence on gate length for no-eSiGe pFETs with and without 60-nm c-SL.

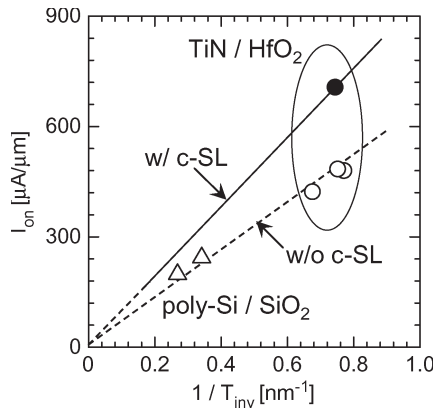


Fig. 9. I_{on} dependence on $1/T_{inv}$ for poly-Si/SiO₂ and TiN/HfO₂ gate stack pFETs without eSiGe. A c-SL thickness is 60 nm, and the I_{on} is extracted at $I_{off} = 100$ nA/μm, $V_{gs} = V_{ds} = -1.0$ V. By using the top-cut c-SL, 46% I_{on} enhancement is achieved.

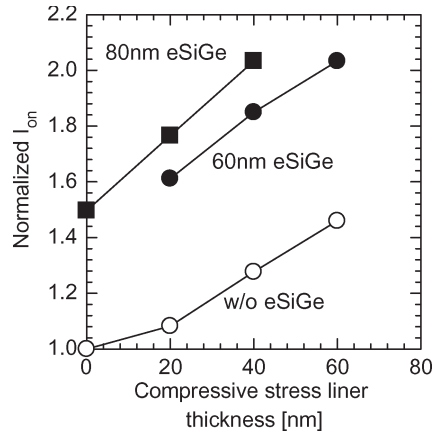


Fig. 10. Normalized I_{on} dependence on c-SL thickness with and without eSiGe for pFETs, where I_{on} is extracted at $I_{off} = 100$ nA/μm, $V_{ds} = V_{gs} = -1.0$ V. More than 200% I_{on} enhancement is achieved by the device with a 40-nm c-SL and 80-nm eSiGe in comparison with the no-stressor device.

even for shorter gate lengths. High channel stress in shorter gate lengths is probably caused by the process combination of the top-cut t-SL and damascene gate as well as pFETs. I_{on} - I_{off} characteristics are shown in Fig. 16. An I_{on} gain at $I_{off} = 100$ nA/μm and $V_{ds} = V_{gs} = 1.0$ V is approximately 10%. As supported by stress and mobility simulations, high

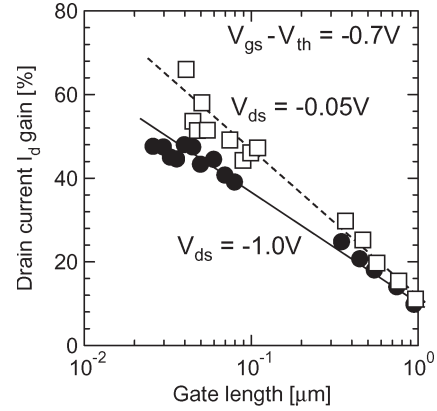


Fig. 11. I_d gain dependence, due to top-cut c-SL, on gate length for pFETs, where V_{gs} overdrive is constant. C-SL and eSiGe thicknesses are 40 and 80 nm, respectively. The I_d gains are plotted for both linear ($V_{ds} = -0.05$ V) and saturation ($V_{ds} = -1.0$ V) regions.

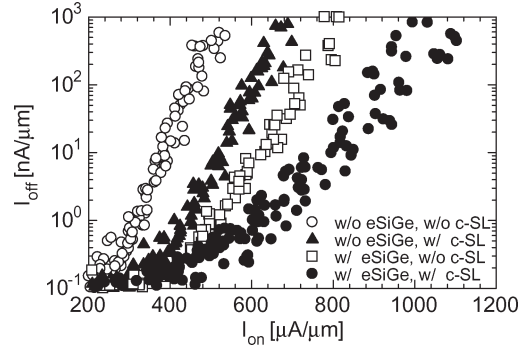


Fig. 12. I_{on} - I_{off} characteristics of pFETs with and without 40-nm c-SL and 80-nm eSiGe, at $V_{ds} = V_{gs} = -1.0$ V. I_{on} enhancement rates at $I_{off} = 100$ nA/μm are 28% for no eSiGe and 35% for eSiGe devices.

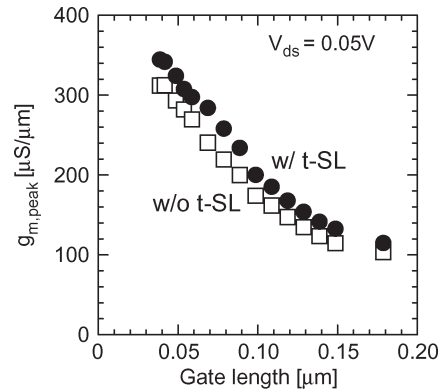


Fig. 13. Dependence of $g_{m,peak}$ on gate length for nFETs with and without 25-nm t-SL. V_{th} roll-off characteristics of the devices are almost the same.

drive currents for nFETs are also achieved by using the top-cut t-SL in the damascene gate process.

V. BENCHMARKS OF CMOS DEVICES

In this section, the performances achieved by this paper are summarized and the benchmark data are shown to compare with recently published data for high-performance MOSFETs. Figs. 17 and 18 show I_d - V_{gs} and I_d - V_{ds} characteristics of 40-nm gate length MOSFETs with top-cut stress liners. High

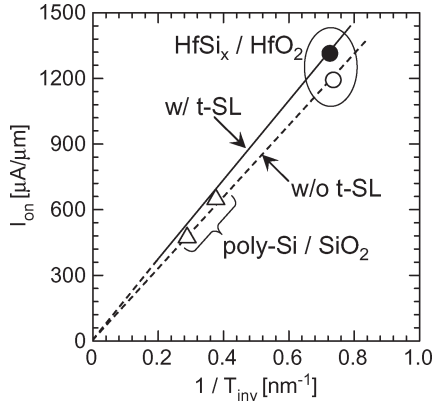


Fig. 14. I_{on} - $1/T_{inv}$ relationship between poly-Si/SiO₂ and HfSi_x/HfO₂ gate stacks, where t-SL thickness is 25 nm. The I_{on} is extracted at $I_{off} = 100$ nA/ μ m, $V_{ds} = V_{gs} = 1.0$ V.

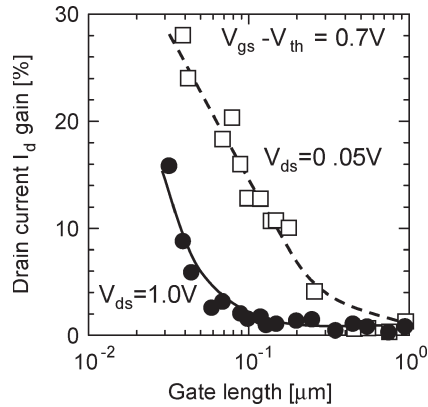


Fig. 15. Dependence of I_d gain, due to top-cut t-SL, on gate length for nFETs at $V_{gs} - V_{th} = 0.7$ V, where t-SL thickness is 25 nm. The I_d gains are plotted for both linear ($V_{ds} = 0.05$ V) and saturation ($V_{ds} = 1.0$ V) currents.

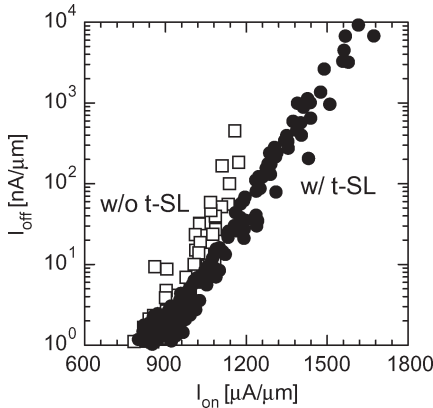


Fig. 16. I_{on} - I_{off} characteristics of nFETs at $V_{ds} = V_{gs} = 1.0$ V. A t-SL thickness is 25 nm. An I_{on} gain at $I_{off} = 100$ nA/ μ m is approximately 10%.

drive currents of 1300 and 1000 $\mu A/\mu m$ at $V_{dd} = 1.0$ V and $I_{off} = 100$ nA/ μm are remarkably obtained for n- and pFETs even on (100) substrates, respectively. The device performances compared with the published data are summarized in Table I [11]–[13]. Higher performances among the published data are achieved by our technologies. Fig. 19 shows the comparison of harmonic mean of V_{dd}/I_{on} for n- and pFETs on physical gate length for this paper, our previous work [2], published

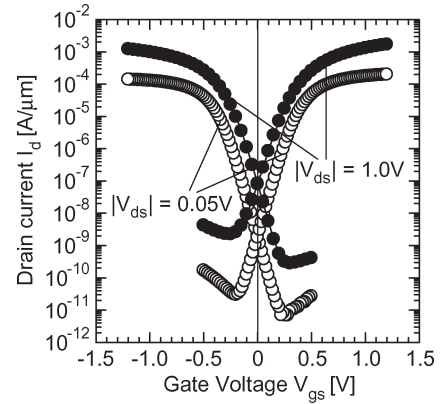


Fig. 17. I_d - V_{gs} characteristics of n- and pFETs at $V_{ds} = 0.05$ and 1.0 V, where gate length is 40 nm. Stress liner thicknesses are 25 and 40 nm for n- and pFETs, respectively. A 80-nm eSiGe is applied for pFETs.

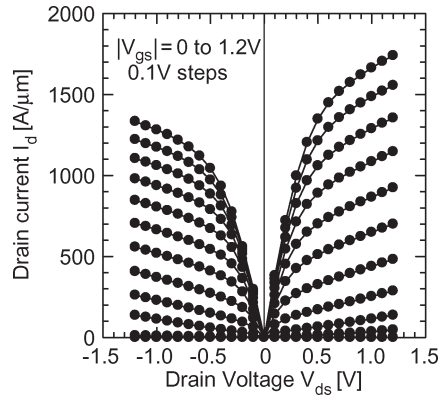


Fig. 18. I_d - V_{ds} characteristics of each device, as shown in Fig. 17.

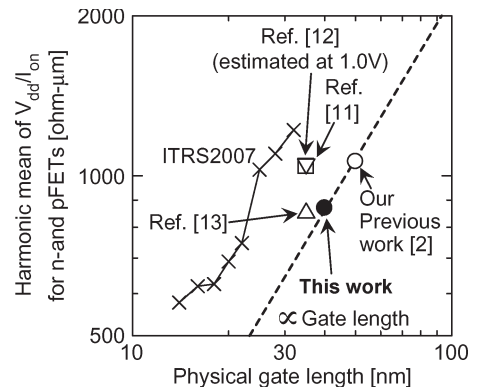


Fig. 19. Comparison of harmonic mean of V_{dd}/I_{on} for n- and pFETs on physical gate length for this paper, our previous work, published data and ITRS2007, where I_{on} ratio of n- to pFET for ITRS2007 applies 1.3 : 1.

papers (Table I) and International Technology Roadmap for Semiconductor (ITRS) 2007 [14]. It is observed that the harmonic mean of V_{dd}/I_{on} is proportional to gate length for this and our previous works by the application of channel strain technologies along with the demand of ITRS. Furthermore, it suggests that the technologies reported in this paper would accomplish further performance enhancement in proportion to gate length by scaling.

TABLE I
PERFORMANCE COMPARISON BETWEEN THIS PAPER AND PUBLISHED
DATA OF HIGH-PERFORMANCE MOSFETs

	This work	Our previous work [2]	Ref. [11]	Ref. [12]	Ref. [13]
V_{dd} [V]	1.0	1.0	1.0	1.2	1.0
Gate length [nm]	40	50	35	35	35
T_{inv} [nm]	1.4	1.6	1.2 (phy.)	1.2 (phy.)	1.0 (EOT)
nFET					
I_{on} [$\mu\text{A}/\mu\text{m}$]	1300	1050	1210	1750	1360
I_{off} [nA/ μm]	100	100	100	100	100
pFET					
I_{on} [$\mu\text{A}/\mu\text{m}$]	1000	830	710	1060	1070
I_{off} [nA/ μm]	100	100	100	100	100
Substrate	(100)	(110)	(100)	(100)	-

VI. CONCLUSION

The effects of top-cut stress liners for damascene gate MOSFETs were investigated by stress simulation and demonstration. These were found that the process combination of top-cut dual stress liners and damascene gates induces high channel stress and also that the I_d gain increases continuously with the decrease in the gate length for both n- and pFETs, as compared to conventional gate-first MOSFETs. These results indicated that high channel stress was induced particularly for shorter gate lengths. Therefore, high drive current n- and pFETs were successfully achieved by using top-cut stress liners with dual metal/high-*k* gates and eSiGe for damascene gate devices. In order to understand the mechanism of these effects on the gate length, it is needed to analyze exactly the channel strain for the damascene gate devices with short gate lengths. These technologies are strong candidates for high-performance devices in the coming generation.

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Satoru Mayuzumi received the B.S. and M.S. degrees in applied physics from the University of Electro-Communications, Tokyo, Japan, in 1995 and 1997, respectively.

In 1997, he was with NEC Corporation, Sagami-hara, Japan, where he had worked on the research and development of scaled CMOS devices. Since 2006, he has been with Semiconductor Business Group, Sony Corporation, Atsugi, Japan, where he has been working on the research and development of metal/high-*k* MOSFETs. He is also currently

working in electrical engineering with Meiji University, Kanagawa, Japan, from 2008. His research interests include the advanced MOSFET devices and technologies.

Mr. Mayuzumi is a member of the Japan Society of Applied Physics.

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Si MOSFETs.

Shinya Yamakawa (S'04–M'06) received the B.E. and M.E. degrees in electrical engineering from Osaka University, Osaka, Japan, in 1993 and 1995, respectively, and the Ph.D. degree in electrical engineering from Arizona State University, Tempe, in 2005. His Ph.D. research focused on the study of carrier transport and device modeling of GaN-based MESFETs and HEMTs.

Since 2005, he has been with Sony Corporation, Atsugi, Japan, and currently works in the area of TCAD device simulation focusing on strained



Kaori Tai received the B.S. degree in physical engineering from the University of Tokyo, Tokyo, Japan, in 1993.

She was with Oki Electric Industry Company, Ltd., Tokyo, Japan, in 1993. While there, she engaged in research and development of the CMOS process, focusing on metal film deposition and interconnect process integration. Since 2000, she has been with Sony Corporation, Atsugi, Japan, where she has been pursuing research and development of the interconnect process for Cu/low- k . Her current focus is on process technology of metal/high- k gate-stacks.



Yasushi Tateshita received the B.E. and M.E. degrees in electrical engineering from Iwate University, Iwate, Japan, in 1991 and 1993, respectively.

Since 1993, he has been with Semiconductor Business Group, Sony Corporation, Atsugi, Japan, where he has been engaging in the research and development of advanced CMOS devices and imaging devices.



Hitoshi Wakabayashi (M'00) received the M.E. and Ph.D. degrees in advanced applied electronics from Tokyo Institute of Technology, Tokyo, Japan, in 1993 and 2003, respectively.

In 1993, he was with NEC Corporation, Sagami-hara, Japan. He was a Visiting Scientist with the Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, from 2000 to 2001. He had made a lecture of "Nano-Scale CMOS Devices" with the Tokyo Institute of Technology in 2004 and 2005. Since

2006, he was with the Sony Corporation, Atsugi, Japan. His current research interests are in advanced device technologies including 3-D FETs.

Dr. Wakabayashi is a member of IEEE Electron Devices Society and Japan Society of Applied Physics. He has served as a member of the IEEE EDS Electronic Materials Committee since 2006, a Subcommittee Member on CMOS Devices of IEDM in 2005 and 2006, a Technical Program Committee member of Symposium on VLSI Technology since 2000 (Treasurer in 2004/2005, Publications in 2006/2007, and Secretary/Publicity/Local-arrangements in 2008/2009), Committee members of SSDM in 2007/2008/2009, VLSI-TSA in 2007/2008/2009, Silicon Nanoelectronics Workshop in 2003/2005/2006, and International Workshop of Junction Technologies (IWJT) in 2005/2007/2009. He was awarded the 8th Young Scientist Award for the Presentation of an Excellent Paper from the Japan Society of Applied Physics in 2000.



Tomoyuki Hirano received the B.E. and M.E. degrees in electrical engineering from Tokyo University of Science, Tokyo, Japan, in 1995 and 1997, respectively.

Since 1997, he has been with Semiconductor Business Group, Sony Corporation, Atsugi, Japan, where he has been engaging in the research and development of the capacitors for embedded DRAMs and metal/high- k gate stacks.



Masashi Nakata received the B.S. degree in electrical engineering from Yamaguchi University, Yamaguchi, Japan, in 2004 and the M.S. degree from Waseda University, Tokyo, Japan, in 2006.

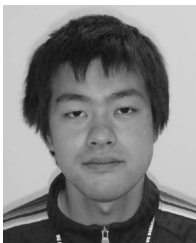
He had studied electronics at Waseda University and researched fabrication of planar nanogap electrodes for single molecule evaluation, with Core Research for Evolutional Science and Technology, Japan Science and Technology Agency, Kawaguchi, Japan. Since 2006, he has been with Sony Corporation, Atsugi, Japan, as Member of Semiconductor

Technology Development, where he has been engaging in the development of metal/high- k gate MOSFET. His recent interests include metal/high- k MOSFETs and CMOS image sensors.



Masanori Tsukamoto received the B.S. and M.S. degrees in electric engineering from the Chiba University, Chiba, Japan, in 1988 and 1990, respectively.

Since 1990, he has been with Sony Corporation, Atsugi, Japan, where he has been engaging in the technology development of 0.5- and 0.25- μm node SRAMs. Since 1994, he has been working on process development and manufacturing operation of 180-, 90-, and 32-nm node CMOS LSIs. He is currently a Senior Manager with the Device Technology Department, Sony Corporation.



Shinpei Yamaguchi was born in Japan, in 1979. He received the B.S. and M.S. degrees in physics from the University of Tokyo, Tokyo, Japan, in 2002 and 2004, respectively.

Since 2004, he has been with Semiconductor Business Group, Sony Corporation, Atsugi, Japan, where he has been engaging in the research and development of metal/high- k gate stacks.



Naoki Nagashima received B.S., M.S., and Ph.D. degrees in physics from Gakushuin University, Tokyo, Japan, in 1985, 1987, and 1990, respectively.

Since 1990, he has been with Sony Corporation, Atsugi, Japan, where he has been working on the development of both SOI and bulk CMOS technologies. His current interests include the low-power CMOS, DFM, NVM, and CMOS image sensor technologies.

Dr. Nagashima has served on Technical Program Committee of Symposium on VLSI Technology in

2004, 2005, and 2006.

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