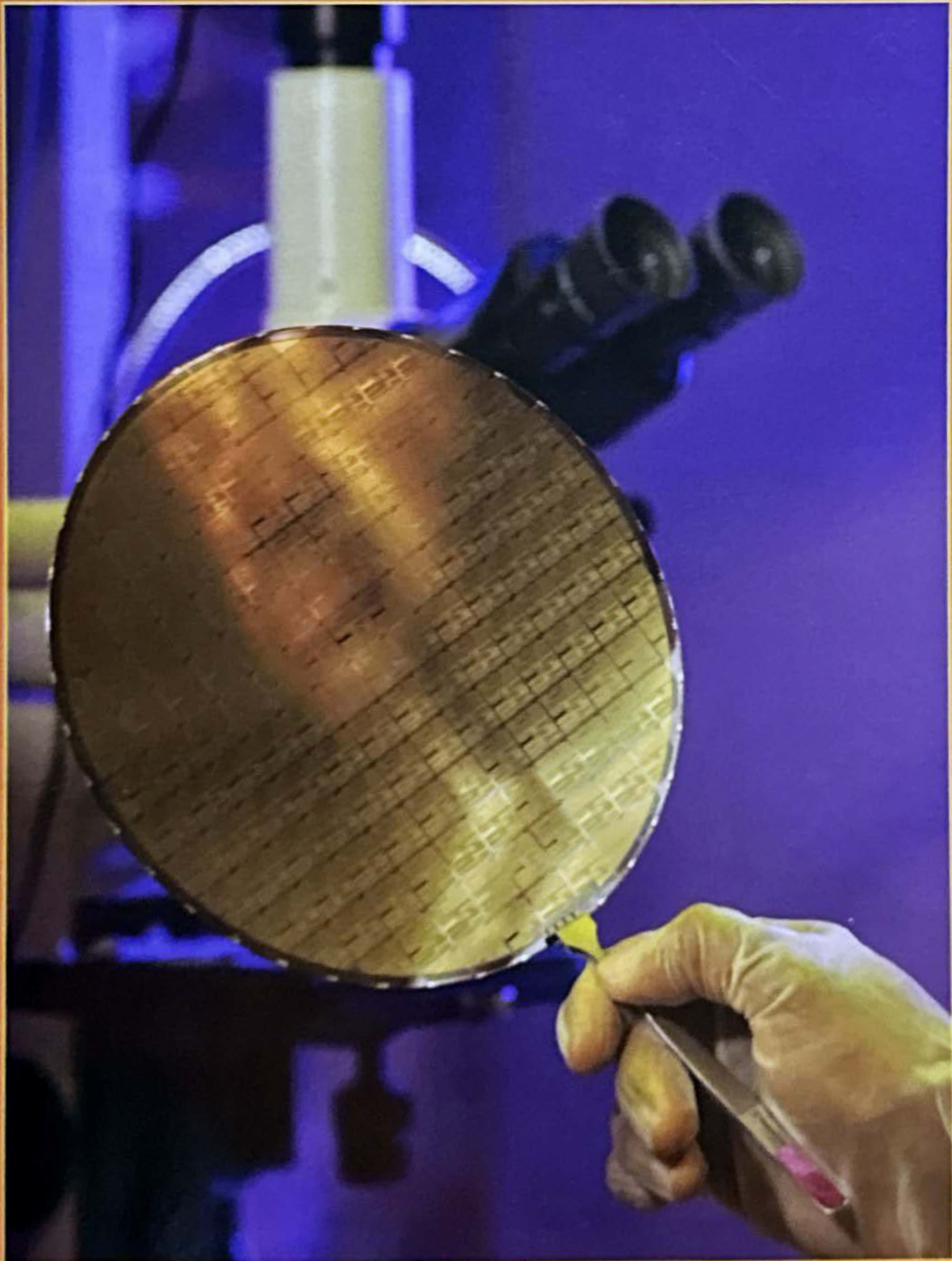


Fundamentals of SEMICONDUCTOR FABRICATION



Fundamentals of Semiconductor Fabrication

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Cover Description: An eight-inch silicon wafer containing Intel Pentium processors.

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Etching

As discussed in the previous chapter, lithography is the process of transferring patterns to photoresist covering the surface of a semiconductor wafer. To produce circuit features, these resist patterns must be transferred into the underlying layers comprising the device. The pattern transfer is accomplished by an etching process that selectively removes unmasked portions of a layer.¹ A brief description of etching was given in Section 1.4.2. The present chapter covers the following topics:

- Mechanisms for wet chemical etching of semiconductors, insulators, and metal films
- Plasma-assisted etching (also called dry etching) for high-fidelity pattern transfer

► 5.1 WET CHEMICAL ETCHING

Wet chemical etching is used extensively in semiconductor processing. Starting from semiconductor wafers sliced from an ingot (Chapter 2), chemical etchants are used for lapping and polishing to give an optically flat, damage-free surface. Prior to thermal oxidation (Chapter 3) or epitaxial growth (Chapter 8), semiconductor wafers are chemically cleaned to remove contamination that results from handling and storing. Wet chemical etching is especially suitable for blanket etches (i.e., over the whole wafer surface) of polysilicon, oxide, nitride, metals, and III-V compounds.

The mechanisms for wet chemical etching involve three essential steps, as illustrated in Figure 5.1: The reactants are transported by diffusion to the reacting surface, chemical reactions occur at the surface, and the products from the surface are removed by diffusion. Both agitation and the temperature of the etchant solution influence the etch rate, which is the amount of film removed by etching per unit time. In IC processing, most wet chemical etches proceed by immersing the wafers in a chemical solution or by spraying the wafers with the etchant solution. For immersion etching, the wafer is immersed in the etch solution, and mechanical agitation is usually required to ensure etch uniformity and a consistent etch rate. Spray etching has gradually replaced immersion etching because it greatly increases the etch rate and uniformity by constantly supplying fresh etchant to the wafer surface.

For semiconductor production lines, highly uniform etch rates are important. Etch rates must be uniform across a wafer, from wafer to wafer, from run to run, and for any variations in feature sizes and pattern densities. Etch rate uniformity is given by the following equation:

$$\text{Etch rate uniformity (\%)} = \frac{(\text{Maximum etch rate} - \text{Minimum etch rate})}{(\text{Maximum etch rate} + \text{Minimum etch rate})} \times 100\% \quad (1)$$

dielectric plate on the top of the reactor. The wafer is located away from the coil, so it is not affected by the electromagnetic field generated by the coil. There is little plasma density loss because plasma is generated only a few mean free paths away from the wafer surface. Therefore, a high-density plasma and high etch rates are achieved.

Clustered Plasma Processing

Semiconductor wafers are processed in clean rooms to minimize exposure to ambient particulate contamination. As device dimensions shrink, particulate contamination becomes a more serious problem. To minimize particulate contamination, clustered plasma tools use a wafer handler to pass wafers from one process chamber to another in a vacuum environment. Clustered plasma processing tools can also increase throughput. Figure 5.10 shows the multilayer metal (TiW/AlCu/TiW) etching process with clustered tools in an AlCu etch chamber, a TiW etch chamber, and a strip passivation chamber. Clustered tools provide an economic advantage by having high chip yield because the wafer is exposed to less ambient contamination and is handled less.

5.2.4 Reactive Plasma Etching Applications

Plasma etching has rapidly evolved from simple batch resist stripping to large and single-wafer processing. Etching systems continue to be improved, from the conventional RIE tool to the high-density plasma tool for pattern transfer of deep-submicron devices. Aside from the etching tool, etch chemistry also plays a critical role in the performance of the etch process. Table 5.3 lists some etch chemistries for different etch processes. Developing an etch process usually means optimizing etch rate, selectivity, profile control, critical dimension, damage, and so forth by adjusting a large number of process parameters.

Silicon Trench Etching

As device feature size decreases, a corresponding decrease is needed in the wafer surface area occupied by the isolation between circuit elements and the storage capacitor

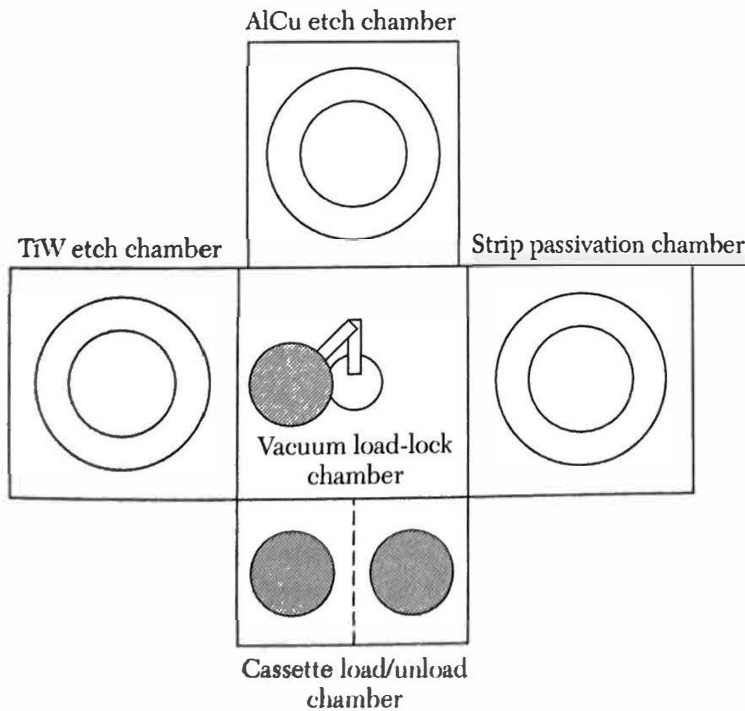


Figure 5.10 Cluster reactive ion etch tool for multilayer metal (TiW/AlCu/TiW) interconnect etching.²

TABLE 5.3 Etch Chemistries of Different Etch Processes

Material Being Etched	Etching Chemistry
Deep Si trench	HBr/NF ₃ /O ₂ /SF ₆
Shallow Si trench	HBr/Cl ₂ /O ₂
Poly Si	HBr/Cl ₂ /O ₂ , HBr/O ₂ , BCl ₃ /Cl ₂ , SF ₆
Al	BCl ₃ /Cl ₂ , SiCl ₄ /Cl ₂ , HBr/Cl ₂
AlSiCu	BCl ₃ /Cl ₂ /N ₂
W	SF ₆ only, NF ₃ /Cl ₂
TiW	SF ₆ only
WSi ₂ , TiSi ₂ , CoSi ₂	CCl ₂ F ₂ /NF ₃ , CF ₄ /Cl ₂ , Cl ₂ /N ₂ /C ₂ F ₆
SiO ₂	CF ₄ /CHF ₃ /Ar, C ₂ F ₆ , C ₃ F ₈ , C ₄ F ₇ /CO, C ₅ F ₈ , CH ₂ F ₂
Si ₃ N ₄	CHF ₃ /O ₂ , CH ₂ F ₂ , CH ₂ CHF ₂

of a DRAM cell. This surface area can be reduced by etching trenches into the silicon substrate and filling them with suitable dielectric or conductive materials. Deep trenches, usually with a depth greater than 5 μm , are used mainly for forming storage capacitors. Shallow trenches, usually with a depth less than 1 μm , are often used for isolation.

Chlorine-based and bromine-based chemistries have a high silicon etch rate and high etch selectivity to the silicon dioxide mask. The combination of HBr + NF₃ + SF₆ + O₂ gas mixtures is used to form a trench capacitor with a depth of approximately 7 μm . This combination is also used for shallow trench isolation etching. *Aspect ratio-dependent etching* (i.e., variation in etch rate with aspect ratio) is often observed in deep silicon trench etching, caused by limited ion and neutral transport within the trench. Figure 5.11 shows the dependence of average silicon trench etch rate on aspect ratio. Trenches with large aspect ratios are etched more slowly than trenches with small aspect ratios.

Polysilicon and Polycide Gate Etching

Polysilicon or polycide (i.e., low-resistance metal silicides over polysilicon) is usually used as a gate material for MOS devices. Anisotropic etching and high etch selectivity to the

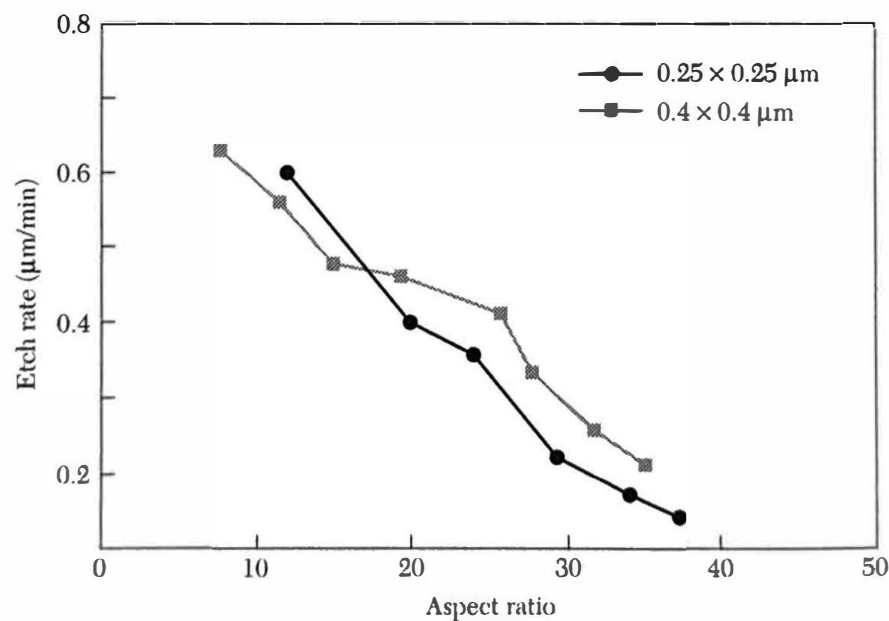


Figure 5.11 Dependence of average silicon trench etch rate on aspect ratio.²

gate oxide are the most important requirements for gate etching. For example, the selectivity required in 1G DRAM is more than 150 (i.e., the ratio of etch rates for polycide and gate oxide is 150:1). Achieving high selectivity and etch anisotropy at the same time is difficult for most ion-enhanced etching processes. Therefore, multistep processing is used, in which different etch steps in the process are optimized for etch anisotropy and selectivity. On the other hand, the trend in plasma technology for anisotropic etching and high selectivity is to utilize a low-pressure, high-density plasma using a relatively low power. Most chlorine-based and bromine-based chemistries can be used for gate etching to achieve the required etch anisotropy and selectivity.

Dielectric Etching

The patterning of dielectrics, especially silicon dioxide and silicon nitride, is a key process in the manufacture of modern semiconductor devices. Because of their higher bonding energies, dielectric etching requires aggressive ion-enhanced, fluorine-based plasma chemistry. Vertical profiles are achieved by sidewall passivation, typically by introducing a carbon-containing fluorine species to the plasma (e.g., CF_4 , CHF_3 , C_4F_8). High ion-bombardment energies are required to remove this polymer layer from the oxide, as well as to mix the reactive species into the oxide surface to form SiF_x products.

A low-pressure, high-density plasma is advantageous for aspect ratio-dependent etching. However, the HDP generates high-temperature electrons and subsequently generates a high degree of dissociation of ions and radicals. It generates far more active radicals and ions than RIE or MERIE plasmas. In particular, a high F concentration worsens the selectivity to silicon. Various methods have been tried to enhance the selectivities in the high-density plasma. First, a parent gas with a high C/F ratio, such as C_2F_6 , C_4F_8 , or C_5F_8 , was attempted. Other methods to scavenge F radicals have also been developed.⁹

Interconnect Metal Etching

Etching of a metallization layer is a very important step in IC fabrication. Aluminum, copper, and tungsten are the most popular materials used for interconnection. These materials usually require anisotropic etching. The reaction of aluminum with fluorine results in nonvolatile AlF_3 , which has a vapor pressure of only 1 Torr at 1240°C. Chlorine-based chemistry (e.g., a Cl_2/BCl_3 mixture) has been widely used for aluminum etching. Chlorine has a very high chemical etch rate with aluminum and tends to produce an undercut during etching. Carbon-containing gas (e.g., CHF_3) or N_2 is added to form sidewall passivation during aluminum etching to obtain anisotropic etching.

Exposure to the ambient is another problem in aluminum etching. Residual chlorine on the aluminum sidewall and the photoresist tends to react with atmospheric water to form HCl, which corrodes aluminum. An *in situ* exposure of the wafer to a CF_4 discharge to exchange Cl with F and then to an oxygen discharge to remove the resist, followed by immediate immersion in deionized water, can eliminate aluminum corrosion. Figure 5.12 shows 0.35- μm TiN/Al/Ti lines and spaces on a wafer maintained at ambient for 72 hours. No corrosion is present even after prolonged exposure to the ambient.

Copper has drawn much attention as a new metallization material in ULSI circuits because of its low resistivity ($\sim 1.7 \Omega\text{-cm}$) and superior resistance to electromigration compared with Al or Al alloys. However, because of the low volatility of copper halides, plasma etching at room temperature is difficult. Process temperatures higher than 200°C are required to etch copper films. Therefore, the *damascene* process is used to form Cu interconnection without dry etching. Damascene processing involves the creation of interconnect lines by first etching a trench or canal in a planar dielectric layer and then filling that trench with metal, such as aluminum or copper. In dual damascene processing (Fig. 5.13), a second level is involved where a series of holes (i.e., contacts or vias) are etched and filled