US 20140131776A1

(19) United States
(12) Patent Application Publication
Ching et al.
(10) Pub. No.: US 2014/0131776 A1
(43) Pub. Date: May 15, 2014

(54) **FIN RECESS LAST PROCESS FOR FINFET FABRICATION**

(71) Applicant: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, L**, Hsin-Chu (TW)

(72) Inventors: **Kuo-Cheng Ching**, Zhubei City (TW); **Shi Ning Ju**, Hsin-Chu (TW); **Guan-Lin Chen**, Hsin-Chu (TW)

(73) Assignee: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**, Hsin-Chu (TW)

(21) Appl. No.: **13/673,717**

(22) Filed: **Nov. 9, 2012**

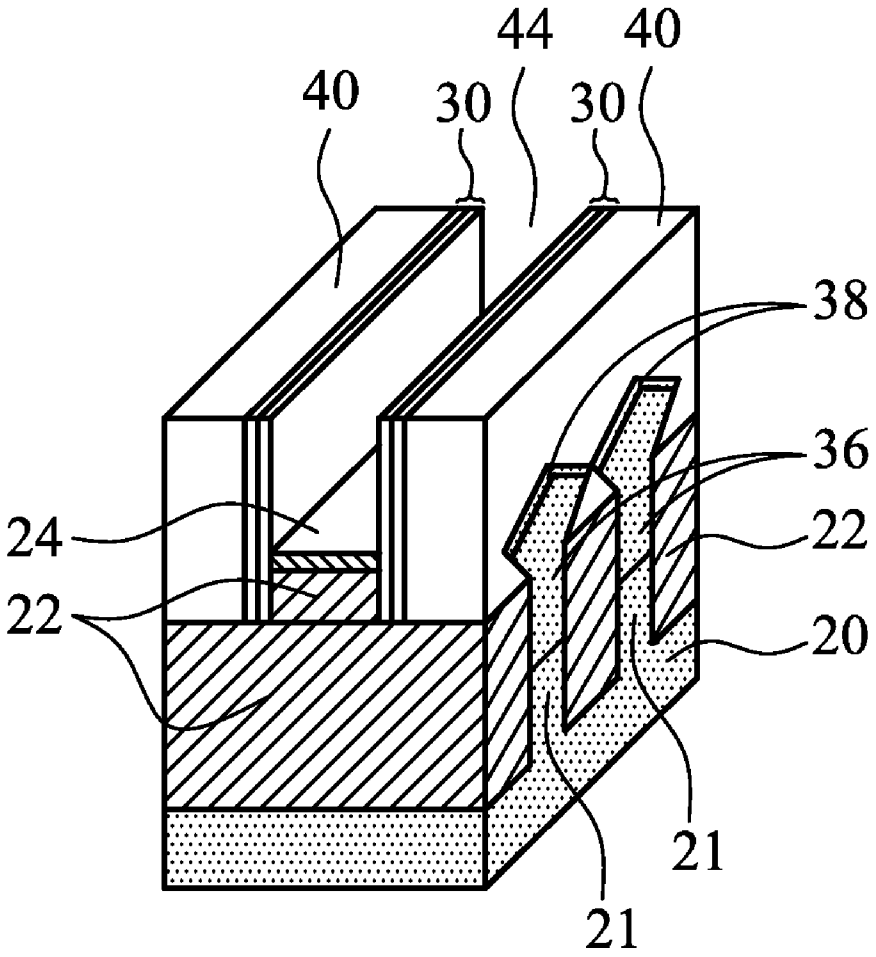
Publication Classification

(51) **Int. Cl.**
H01L 29/78 (2006.01)
H01L 21/336 (2006.01)

(52) **U.S. Cl.**
USPC **257/288**; 438/294; 257/E21.409; 257/E29.255

(57) **ABSTRACT**

A method includes forming isolation regions extending from a top surface of a semiconductor substrate into the semiconductor substrate, and forming a hard mask strip over the isolation regions and a semiconductor strip, wherein the semiconductor strip is between two neighboring ones of the isolation regions. A dummy gate strip is formed over the hard mask strip, wherein a lengthwise direction of the dummy gate strip is perpendicular to a lengthwise direction of the semiconductor strip, and wherein a portion of the dummy gate strip is aligned to a portion of the semiconductor strip. The method further includes removing the dummy gate strip, removing the hard mask strip, and recessing first portions of the isolation regions that are overlapped by the removed hard mask strip. A portion of the semiconductor strip between and contacting the removed first portions of the isolation regions forms a semiconductor fin.



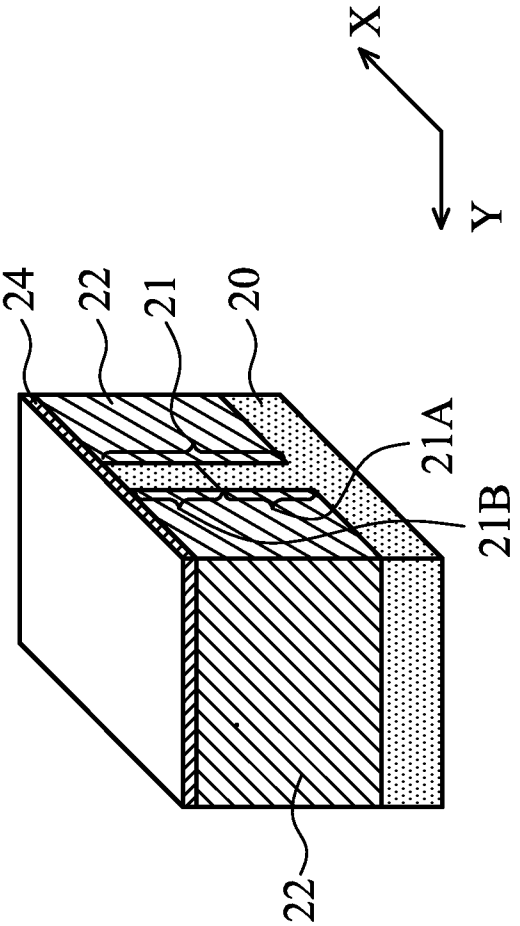


Fig. 1

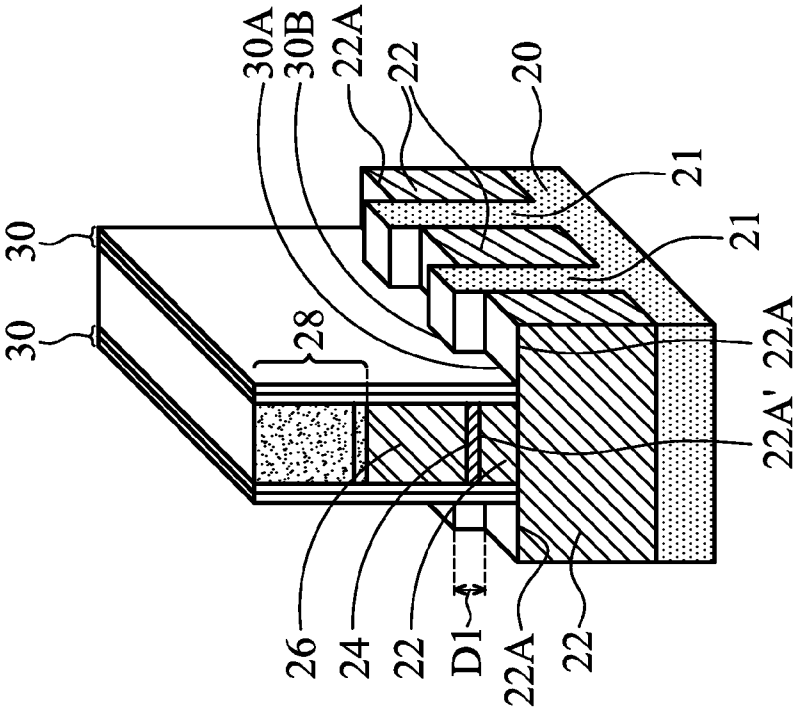

30
30
30A
30B
22A
22
20
21
21
28
22A
22A'
26
24
22
D1
22A
22

Fig. 3

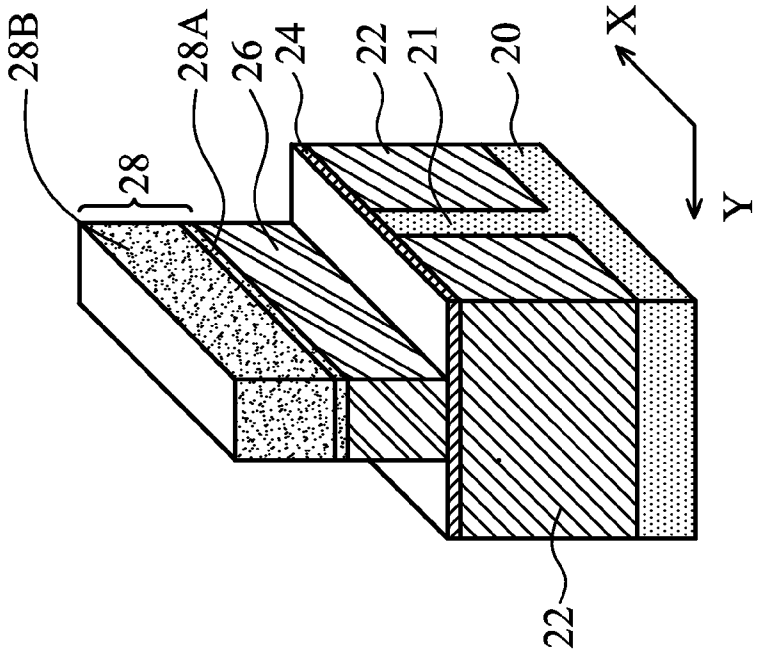

28B
28
28A
26
24
22
21
20
X
Y
22

Fig. 2

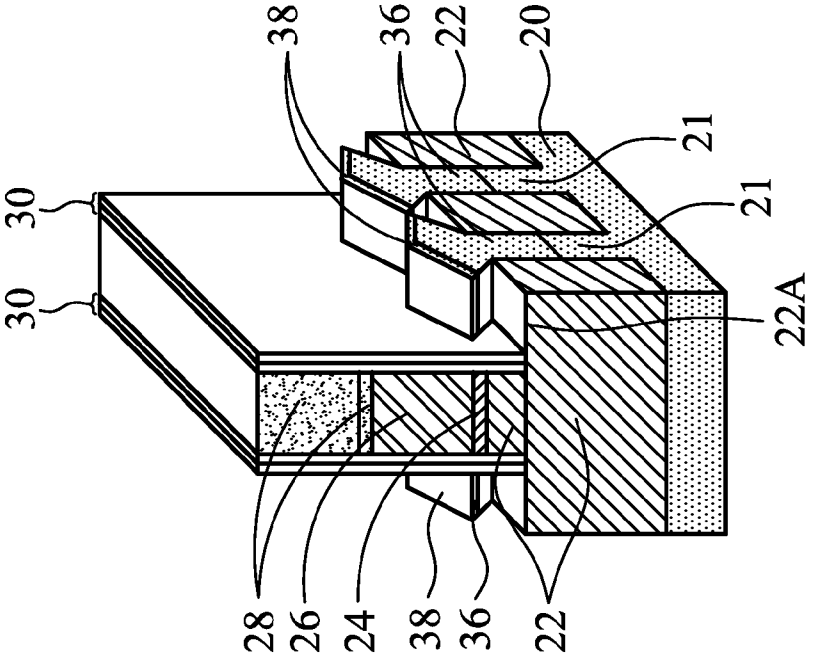

38
36
22
20
21
21
30
30
22A
28
26
24
38
36
22

Fig. 5

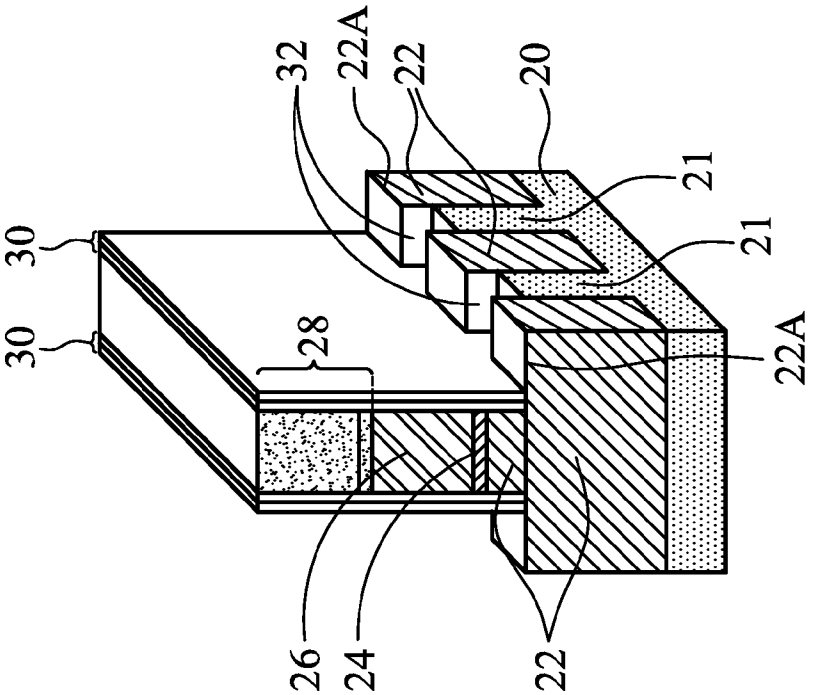

32
22A
22
20
21
21
30
30
28
22A
26
24
22

Fig. 4

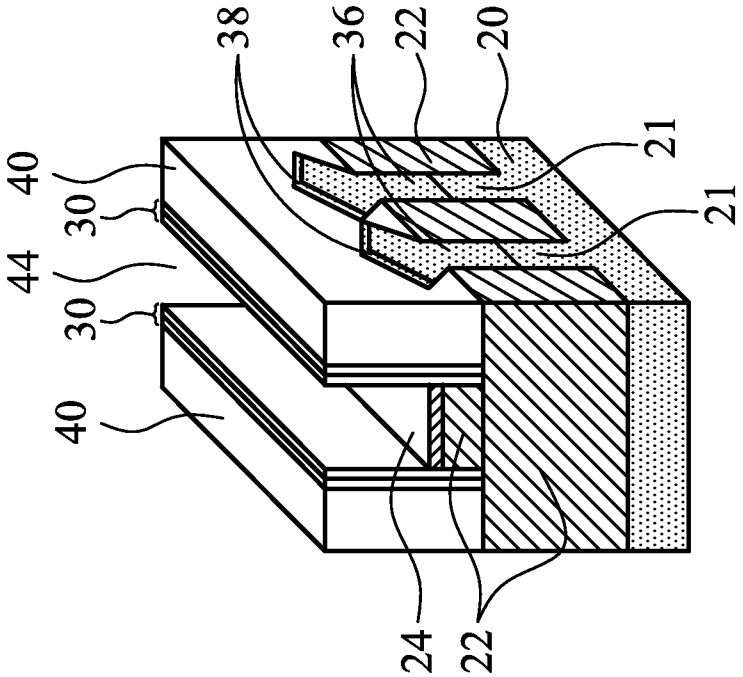

38
36
22
20
21
21
40
30
44
30
40
24
22

Fig. 7

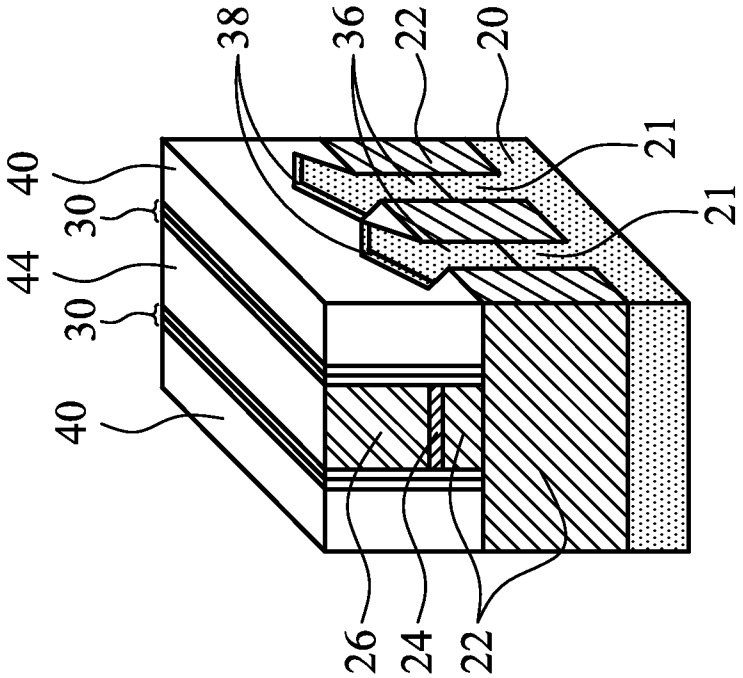

38
36
22
20
21
21
40
30
44
30
40
26
24
22

Fig. 6

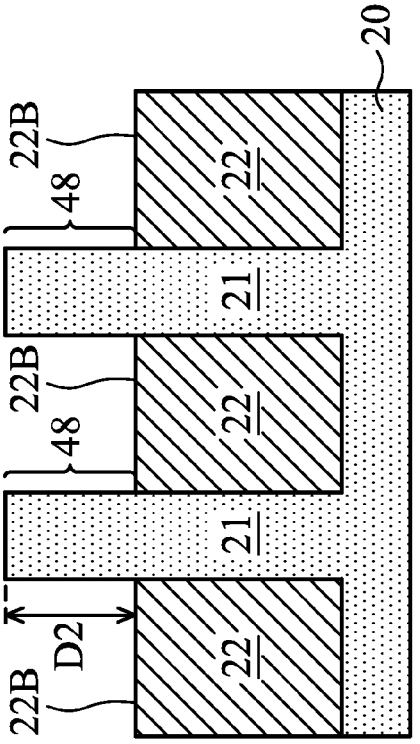

20
22B
48
22
21
22B
48
22
21
D2
22B
22

Fig. 8B

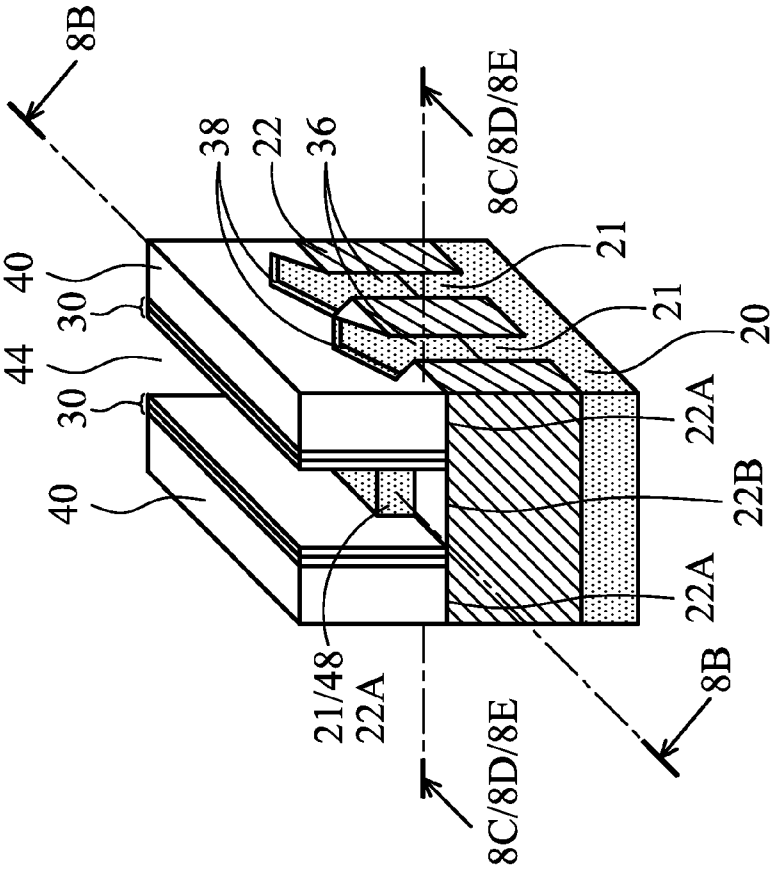

8B
38
22
36
8C/8D/8E
40
30
44
30
40
21
21
20
22A
22B
22A
21/48
22A
8C/8D/8E
8B

Fig. 8A

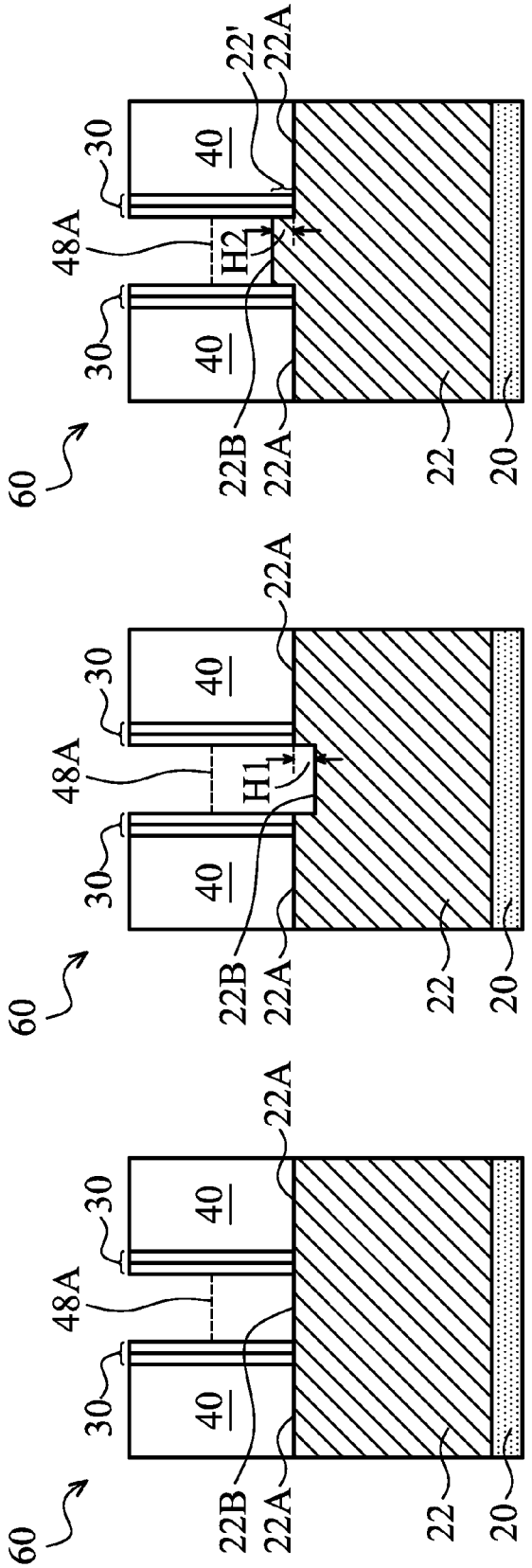


Fig. 8C

Fig. 8D

Fig. 8E

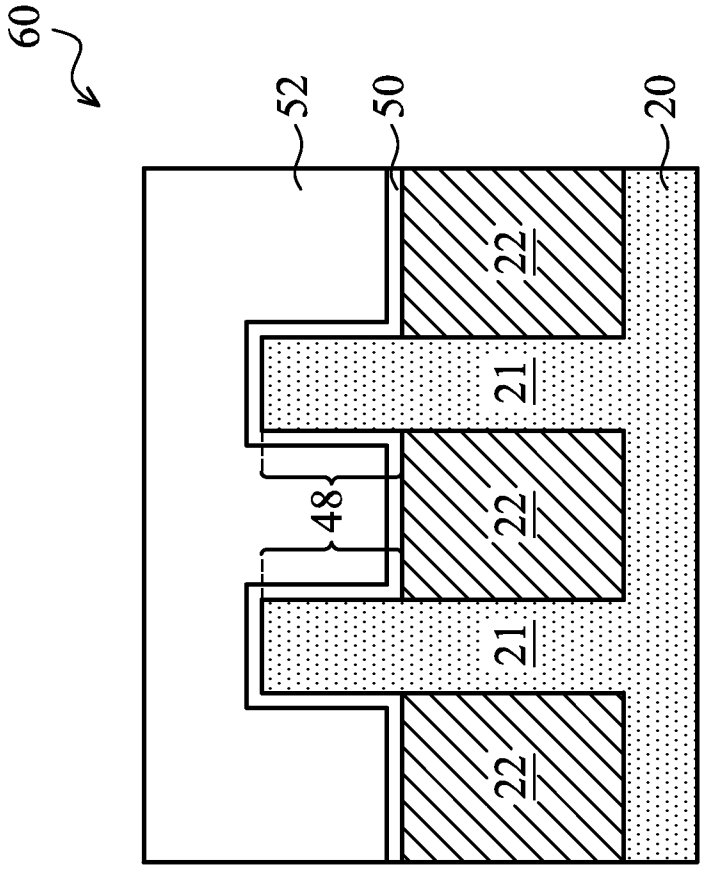


Fig. 9A

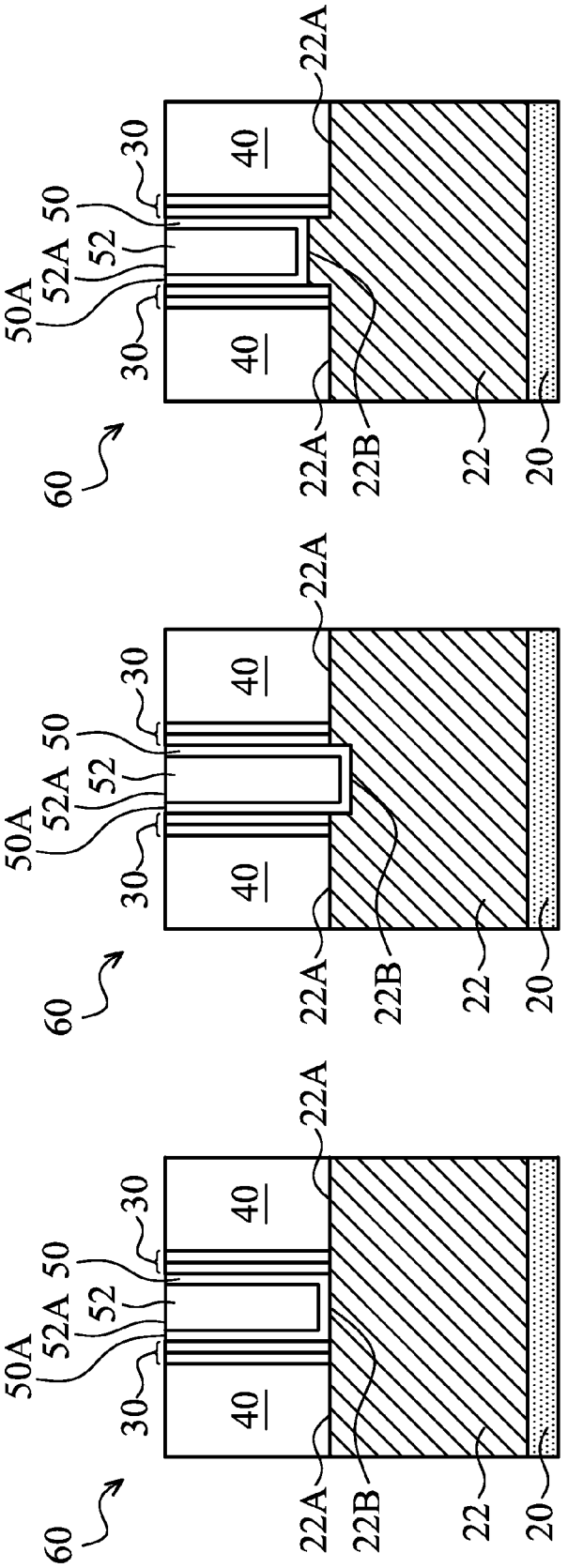


Fig. 9B

Fig. 9C

Fig. 9D

FIN RECESS LAST PROCESS FOR FINFET FABRICATION

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application relates to the following commonly-assigned U.S. patent application Ser. No. 13/356,769, filed Jan. 24, 2012, and entitled "FinFETs and Methods for Forming the Same," which application is hereby incorporated herein by reference.

BACKGROUND

[0002] With the increasing down-scaling of integrated circuits and increasingly demanding requirements to the speed of integrated circuits, transistors need to have higher drive currents with smaller dimensions. Fin Field-Effect Transistors (FinFETs) were thus developed. FinFETs have increased channel widths. The increase in the channel widths is achieved by forming channels that include portions on the sidewalls of semiconductor fins and portions on the top surfaces of the semiconductor fins. Since the drive currents of transistors are proportional to the channel widths, the drive currents of the FinFETs are increased.

[0003] In an existing FinFET formation process, Shallow Trench Isolation (STI) regions are first formed in a silicon substrate. The STI regions are then recessed to form silicon fins, which comprise portions of the silicon substrate that are over the recessed STI regions. Next, a gate dielectric, a gate electrode, and source and drain regions are formed to finish the formation of the FinFET.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0005] FIGS. **1** through **9**D are perspective views and cross-sectional views of intermediate stages in the manufacturing of a FinFET in accordance with various exemplary embodiments.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0006] The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are illustrative, and do not limit the scope of the disclosure.

[0007] A Fin Field-Effect Transistor (FinFET) and the methods of forming the same are provided in accordance with various embodiments. The intermediate stages of forming the FinFET are illustrated. The variations of the embodiments are discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

[0008] FIGS. **1** through **9**D are cross-sectional views and perspective views of intermediate stages in the manufacturing of a FinFET in accordance with some exemplary embodiments. FIG. **1** illustrates a perspective view of an initial structure. The initial structure includes substrate **20**. Substrate **20** may be a semiconductor substrate, which may further be a silicon substrate, a germanium substrate, or a substrate formed of other semiconductor materials. Substrate **20** may be doped with a p-type or an n-type impurity. Isolation regions such as Shallow Trench Isolation (STI) regions **22** are formed in substrate **20** and extend from a top surface of substrate **20** into substrate **20**.

[0009] As shown in FIG. **1**, semiconductor strip **21** is formed between, and contacting, neighboring STI regions **22**. The longitudinal direction of semiconductor strip **21** is in the Y direction. Although one semiconductor strip **21** is shown in FIG. **1** for clarity, there may be a plurality of semiconductor strip **21** parallel to each other, as also illustrated in FIG. **3**. In some exemplary embodiments, the material of semiconductor strip **21** is the same as the material of substrate **20**, which may be silicon, for example. In alternative embodiments, the material of semiconductor strip **21** is different from the material of substrate **20**. In some exemplary embodiments, the FinFET that is to be formed is a p-type FinFET, and semiconductor strip **21** includes relaxed silicon germanium (SiGe) region **21**A and substantially pure germanium region **21**B over relaxed SiGe region **21**A. In alternative exemplary embodiments, the FinFET that is to be formed is an n-type MOSFET, and semiconductor strip **21** includes relaxed silicon germanium (SiGe) region **21**A and substantially pure silicon region **21**B over relaxed SiGe region **21**A. In these embodiments, semiconductor strip **21** may be formed by etching a portion of the original substrate **20** between STI regions **22**, and epitaxially growing semiconductor strip **21** between STI regions **22**.

[0010] Hard mask layer **24** is formed over semiconductor strip **21** and STI regions **22**. Hard mask layer **24** may be in contact with the top surfaces of STI regions **22** and semiconductor strip **21**. In some embodiments, hard mask layer **24** comprises silicon nitride. In alternative embodiments, materials such as silicon oxide, silicon carbide, metal nitrides such as titanium nitride and tantalum nitride, or the like, may also be used.

[0011] Referring to FIG. **2**, polysilicon layer **26** is deposited. In accordance with some embodiments, a planarization step such as a grinding or a Chemical Mechanical Polish (CMP) is performed to level the top surface of polysilicon layer **26**. Hard mask layer **28** is then formed over polysilicon layer **26**. Hard mask layer **28** may be formed of silicon nitride, for example, although other materials such as silicon oxide may also be used. In some exemplary embodiments, as shown in FIG. **2**, hard mask layer **28** includes silicon nitride layer **28**A and oxide layer **28**B over silicon nitride layer **28**A.

[0012] As also shown in FIG. **2**, hard mask layer **28** is patterned. To pattern hard mask layer **28**, a photo resist (not shown) may be formed and patterned first, and the patterned photo resist is used as an etching mask to pattern hard mask layer **28**. The patterned photo resist is then removed. A remaining portion of hard mask layer **28** is referred to as hard mask strip **28** hereinafter. Next, hard mask strip **28** is used as an etching mask to etch the underlying polysilicon layer **26**, wherein the patterning may be stopped on hard mask layer **24**. A remaining portion of polysilicon layer **26** is referred to as polysilicon strip **26** hereinafter. Polysilicon strip **26** overlaps a middle portion of semiconductor strip **21**, and having a longitudinal direction in X direction, which is perpendicular to the Y direction.

[0013] Referring to FIG. **3**, hard mask strip **28** is used as an etching mask to selectively pattern hard mask layer **24**. In FIG. **3**, two semiconductor strips **21** are illustrated. Some

portions of STI regions **22** and semiconductor strips **21** are exposed as a result of the patterning of hard mask layer **24**. A first STI recessing may be performed after the patterning of hard mask layer **24**. As a result of the STI recessing, top surfaces **22**A of STI regions **22** are also recessed from the original top surface **22**A' of STI regions. In some embodiments, the exposed portions of semiconductor strips **21** that are not covered by hard mask strip **28** are not recessed. In some embodiments, after the patterning of hard mask layer **24**, and before or after the recessing of STI regions **22**, hard mask strip **28** is removed. In alternative embodiments, hard mask strip **28** may be removed after some subsequent steps are performed. For example, hard mask strip **28** may be performed after the formation of Inter-Layer Dielectric (ILD) **40** (FIG. **6**).

[0014] Next, as also shown in FIG. **3**, gate spacers **30** are formed on the sidewalls of hard mask strip **28**, polysilicon strip **26**, and the sidewalls of some un-recessed portions of STI regions **22**. Gate spacers **30** are formed of dielectric materials. Gate spacers **30** comprise first bottom surfaces **30**A landing on the top surfaces **22**A of STI regions **22**, and second top surfaces **30**B landing on the top surfaces of semiconductor strips **21**. Since top surfaces **22**A of the recessed STI regions **22** are lower than the top surfaces of semiconductor strips **21**, first bottom surfaces **30**A are lower than the second bottom surfaces **30**B.

[0015] Referring to FIG. **4**, after the formation of gate spacers **30**, exposed portions of semiconductor strip **21** are recessed, for example, using anisotropic etching. In some embodiments, portions of semiconductor strips **21** above the exposed top surface **22**A of STI regions **22** are etched. The etching of semiconductor strips **21** may be continued until the top surfaces of semiconductor strips **21** are lower the top surfaces **22**A of STI regions **22**, forming recesses **32** in STI regions **22**. Recesses **32** include portions that on opposite sides of polysilicon strip **26**.

[0016] Next, as shown in FIG. **5**, epitaxy regions **36** are formed by selectively growing epitaxy regions **36** from recesses **32** (FIG. **4**). In some exemplary embodiments, epitaxy regions **36** comprise silicon germanium or silicon carbon. Alternatively, epitaxy regions **36** are formed of silicon. After recesses **32** are filled with epitaxy regions **36**, the further epitaxial growth of epitaxy regions **36** causes epitaxy regions **36** to expand horizontally, and facets start to form. Furthermore, some of top surfaces **22**A of STI regions **22** are underlying some portions of epitaxy regions **36** due to the horizontal growth of epitaxy regions **36**. After the epitaxy step, epitaxy regions **36** may be implanted to form source and drain regions, which are also denoted using reference numeral **36**. Source and drain regions **36** are on opposite sides of polysilicon strip **26**, and may be overlying and overlapping portions of surfaces **22**A of STI regions **22**. Following the formation of source and drain regions **36**, source and drain silicide regions **38** may be formed by siliciding the top portions of epitaxy regions **36**. In alternative embodiments, source and drain silicide regions **38** are formed after the formation of replacement gate electrode **52** (FIGS. **9**A-**9**D).

[0017] FIG. **6** illustrates the formation of Inter-Layer Dielectric (ILD) **40**. In some embodiments, ILD **40** includes carbon-containing oxides, silicate glass, or other dielectric materials. ILD **40** may be filled until its top surface is higher than the top surface of polysilicon strip **26**, or higher than hard mask strip **28** (note shown in FIG. **6**, please refer to FIGS. **3** and **4**). A CMP is then performed to remove excess ILD **40**. In some embodiments, polysilicon strip **26** is used as a CMP stop layer, so that the top surfaces of ILD **40** is level with the top surfaces of polysilicon strips **26**. In alternative embodiments, hard mask strip **28** (FIG. **3**) may also be used as a CMP stop layer. In the embodiments wherein hard mask strip **28** is used as the CMP stop layer, after the CMP, an etching step may be performed to remove hard mask strip **28**.

[0018] Next, referring to FIG. **7**, polysilicon strip **26** is removed in an etching step, so that recess **44** is formed between opposite gate spacers **30**. Hard mask layer **24** is thus exposed. Since polysilicon strip **26** is not in the final structure, polysilicon strip **26** is referred to as a dummy polysilicon strip throughout the description.

[0019] After the removal of dummy polysilicon strip **26**, hard mask layer **24** is removed. The resulting structure is shown in FIG. **8**A. After the removal of hard mask layer **24**, the portions of STI regions **22** underlying the removed hard mask layer **24** are recessed in a second recessing step, which may be a selective etching step, so that recess **44** extends downwardly. The top surfaces the recessed STI regions **22** are also recessed from the original surfaces **22**A' (FIG. **3**) to top surfaces **22**B. As a result, STI regions **22** have top surfaces **22**B generated by the etching step. During the selective etching, semiconductor strips **21** are not etched, and the portions of semiconductor strips **21** over top surface **22**B form semiconductor fins **48**.

[0020] FIG. **8**B illustrates a cross-sectional view of the structure in FIG. **8**A, wherein the cross-sectional view is obtained from the plane crossing line **8**B-**8**B in FIG. **8**A. Semiconductor fins **48** are illustrated in FIG. **8**B.

[0021] FIGS. **8**C, **8**D, and **8**E illustrate cross-sectional views of the structure in FIG. **8**A in accordance various embodiments, wherein the cross-sectional views are obtained from the plane crossing line **8**C/**8**D/**8**E-**8**C/**8**D/**8**E in FIG. **8**A. In some embodiments, as illustrated in FIGS. **8**C and **8**A, top surfaces **22**B are level with top surfaces **22**A of STI regions **22**. In alternative embodiments, as shown in FIG. **8**D, top surfaces **22**B are lower than top surfaces **22**A of STI regions **22**. In yet alternative embodiments, as shown in FIG. **8**E, top surfaces **22**B are higher than top surfaces **22**A of STI regions **22**. In FIG. **8**E, portions **22'** of STI regions **22** are located between opposite gate spacers **30**, and the sidewalls of portions **22'** are in contact with the sidewalls of gate spacers **30**. Top surfaces **48**A of semiconductor fins **48** are illustrated using a dashed line in FIGS. **8**C, **8**D, and **8**E since semiconductor fin **48** is not in the planes illustrated in FIGS. **8**C, **8**D, and **8**E.

[0022] FIGS. **9**A and **9**B illustrate the formation of gate dielectric layer **50** and gate electrode **52**. The cross-sectional view in FIG. **9**A is obtained from the same plane that crosses lines **8**B-**8**B in FIG. **8**A. First, gate dielectric layer **50** is formed in recess **44** (FIG. **8**A) and on the top surfaces and the sidewalls of semiconductor fins **48**. In accordance with some embodiments, gate dielectric layer **50** comprises silicon oxide, silicon nitride, or multilayers thereof. In alternative embodiments, gate dielectric layer **50** comprises a high-k dielectric material, and hence is alternatively referred to as high-k gate dielectric layer **50** throughout the description. High-k gate dielectric layer **50** may have a k value greater than about 7.0, and may include a metal oxide or a silicate of Hf, Al, Zr, La, Mg, Ba, Ti, Pb, and combinations thereof. The formation methods of gate dielectric layer **50** may include Molecular-Beam Deposition (MBD), Atomic Layer Deposition (ALD), Physical Vapor Deposition (PVD), and the like.

[0023] Next, conductive material **52** is formed over gate dielectric layer **50**, and fills the remaining recess **44** (FIG. **8**A). Conductive material **52** may comprise a metal-containing material such as TiN, TaN, TaC, Co, Ru, Al, combinations thereof, and multi-layers thereof. The work function of conductive material **52** may be, or may not be, a band-edge work function, depending on whether the respective FinFET is a p-type FinFET or an n-type FinFET. After the filling of conductive material **52**, a CMP may be performed to remove the excess portions of gate dielectric layer **50** and conductive material **52** over the top surface of ILD **40**. The resulting remaining portions of the conductive material and gate dielectric layer **50** thus form the replacement gate, which includes gate electrode **52** and gate dielectric **50**, respectively, of the resulting FinFET **60**.

[0024] The cross-sectional views in FIGS. **9**B, **9**C, and **9**D are obtained in accordance with various embodiments, and are obtained from the same plane that crosses line **8**C/**8**D/**8**E-**8**C/**8**D/**8**E in FIG. **8**A. Furthermore, FinFETs **60** in FIGS. **9**B, **9**C, and **9**D are obtained from the structures in FIGS. **8**C, **8**D, and **8**E, respectively. Referring to FIGS. **9**B, **9**C, and **9**D, due to the replacement-gate formation process, top edge **50**A of gate dielectric **50** is level with top edge **52**A of gate electrode **52**. In subsequent process steps, an additional ILD (not shown) may be formed over ILD **40**, and contact plugs (not shown) may be formed to penetrate through the additional ILD and the underlying ILD **40** to electrically couple to gate electrode **52** and silicide regions **38** (FIG. **6**). The formation of FinFET **60** is thus finished.

[0025] The FinFETs **60** in accordance with embodiments have replacement gates. By recessing STI regions to form semiconductor fins after the formation of source and drain regions, there is no need to form dummy oxides to cover the fins of core FinFETs when Input/output (IO) devices are formed. The profile of the semiconductor fins are thus not prone to the damage caused by the formation and the removal of the dummy oxides.

[0026] It is observed that in the resulting FinFET **60**, the portions of STI regions **22** that are on the opposite sides of a same gate electrode **52** (FIGS. **9**B, **9**C, and **9**D) have top surfaces **22**A that are either higher than, level with, or lower than, top surface **22**B that are underlying (and aligned to) gate electrode **52**. This is different from the conventional FinFETs. In the conventional FinFETs, the STI regions **22** that are on the opposite sides of a gate electrode have top surfaces that are level with the top surface of the portion of the STI region that is underlying (and aligned to) the gate electrode.

[0027] In accordance with embodiments, a method includes forming isolation regions extending from a top surface of a semiconductor substrate into the semiconductor substrate, and forming a hard mask strip over the isolation regions and a semiconductor strip, wherein the semiconductor strip is between two neighboring ones of the isolation regions. A dummy gate strip is formed over the hard mask strip, wherein a lengthwise direction of the dummy gate strip is perpendicular to a lengthwise direction of the semiconductor strip, and wherein a portion of the dummy gate strip is aligned to a portion of the semiconductor strip. The method further includes removing the dummy gate strip, removing the hard mask strip, and recessing first portions of the isolation regions that are overlapped by the removed hard mask strip. A portion of the semiconductor strip between and contacting the removed first portions of the isolation regions forms a semiconductor fin.

[0028] In accordance with other embodiments, a method includes forming a hard mask layer over isolation regions and a semiconductor strip, wherein the isolation regions extend from a top surface of a semiconductor substrate into the semiconductor substrate, and wherein the semiconductor strip is between the isolation regions. The method further includes forming a hard mask strip over the isolation regions and the semiconductor strip, forming a dummy gate strip over the hard mask strip, and performing a first recessing to recess first portions of the isolation regions, wherein the first recessing has a first recessing depth. The first portions of the isolation regions are on opposite sides of the dummy gate strip. After the first recessing, the dummy gate strip is removed, and the hard mask strip is removed. A second recessing is performed to recess second portions of the isolation regions that are overlapped by the removed dummy gate strip. The second recessing has a second recessing depth, wherein a portion of the semiconductor strip between and contacting the second portions of the isolation regions forms a semiconductor fin.

[0029] In accordance with yet other embodiments, a FinFET includes a semiconductor fin, a gate dielectric on sidewalls of the semiconductor fin, a gate electrode over the gate dielectric, wherein the gate dielectric and the gate electrode form a replacement gate, and gate spacers on opposite sides of the gate dielectric and the gate electrode. The gate dielectric includes a portion between and contacting the gate electrode and one of the gate spacers.

[0030] Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

1. A method comprising:

forming isolation regions extending from a top surface of a semiconductor substrate into the semiconductor substrate;

forming a hard mask strip over the isolation regions and a semiconductor strip, wherein the semiconductor strip is between two neighboring ones of the isolation regions;

forming a dummy gate strip over the hard mask strip, wherein a lengthwise direction of the dummy gate strip is perpendicular to a lengthwise direction of the semiconductor strip, and wherein a portion of the dummy gate strip is aligned to a portion of the semiconductor strip;

removing the dummy gate strip;

removing the hard mask strip; and

recessing first portions of the isolation regions that are overlapped by the removed hard mask strip, wherein a portion of the semiconductor strip between and contacting the recessed first portions of the isolation regions forms a semiconductor fin.

2. The method of claim **1** further comprising:

before the step of removing the dummy gate strip, recessing second portions of the isolation regions un-covered by the dummy gate strip; and

forming a gate spacer on a sidewall of the dummy gate strip.

3. The method of claim **1** further comprising:

before the step of recessing the first portions of the isolation regions, forming source and drain regions on opposite sides of the dummy gate strip; and

forming an Inter-Layer Dielectric (ILD) on opposite sides of the dummy gate strip and over the source and drain regions.

4. The method of claim **3**, wherein the step of forming the source and drain regions comprises:

recessing portions of the semiconductor strip; and

performing an epitaxy to grow the source and drain regions in recesses formed by the step of recessing the portions of the semiconductor strip.

5. The method of claim **1** further comprising:

before forming the hard mask strip, recessing a semiconductor material between the neighboring ones of the isolation regions; and

performing an epitaxy to grow the semiconductor strip between the neighboring ones of the isolation regions.

6. The method of claim **1** further comprising:

forming a gate dielectric on sidewalls and a top surface of the semiconductor fin; and

forming a gate electrode over the gate dielectric.

7. A method comprising:

forming a hard mask layer over isolation regions and a semiconductor strip, wherein the isolation regions extend from a top surface of a semiconductor substrate into the semiconductor substrate, and wherein the semiconductor strip is between the isolation regions;

forming a hard mask strip over the isolation regions and the semiconductor strip;

forming a dummy gate strip over the hard mask strip;

performing a first recessing to recess first portions of the isolation regions, wherein the first recessing has a first recessing depth, and wherein the first portions of the isolation regions are on opposite sides of the dummy gate strip;

after the first recessing, removing the dummy gate strip;

removing the hard mask strip; and

performing a second recessing to recess second portions of the isolation regions that are overlapped by the removed dummy gate strip, wherein the second recessing has a second recessing depth, and wherein a portion of the semiconductor strip between and contacting the second portions of the isolation regions forms a semiconductor fin.

8. The method of claim **7** further comprising:

after the first recessing and before the step of removing the dummy gate strip, forming gate spacers on opposite sidewalls of the dummy gate strip; and

forming source and drain regions on opposite sides of the dummy gate strip.

9. The method of claim **8**, wherein the gate spacers are further on sidewalls of the hard mask strip and sidewalls of the second portions of the isolation regions.

10. The method of claim **8** further comprising, after the step of forming the source and drain regions, forming an Inter-Layer Dielectric (ILD) on opposite sides of the gate spacers and over the source and drain regions.

11. The method of claim **7**, wherein the first recessing and the second recessing are configured to make the first recessing depth greater than the second recessing depth.

12. The method of claim **7**, wherein the first recessing and the second recessing are configured to make the first recessing depth smaller than the second recessing depth.

13. The method of claim **7**, wherein the first recessing and the second recessing are configured to make the first recessing depth substantially equal to the second recessing depth.

14. The method of claim **7** further comprising:

forming a gate dielectric on sidewalls and a top surface of the semiconductor fin; and

forming a gate electrode over the gate dielectric.

15.-**20**. (canceled)

21. A method comprising:

forming isolation regions extending from a top surface of a semiconductor substrate into the semiconductor substrate, wherein a portion of the semiconductor substrate between neighboring ones of the isolation regions forms a semiconductor strip;

forming a source/drain region overlapping a bottom portion of the semiconductor strip;

forming an Inter-Level Dielectric (ILD) over the source/drain region;

after forming the ILD, performing a first recessing to recess portions of the isolation regions, wherein a top portion of a middle portion of the semiconductor strip forms a semiconductor fin protruding above surfaces of recessed isolation regions; and

forming a gate stack on a top surface and sidewalls of the semiconductor fin.

22. The method of claim **21** further comprising:

forming a dummy gate strip over the semiconductor strip and the isolation regions, wherein a lengthwise direction of the dummy gate strip is perpendicular to a lengthwise direction of the semiconductor strip; and

after the forming the ILD and before the first recessing, removing the dummy gate strip to form a recess in the ILD, wherein the first recessing is performed through the recess.

23. The method of claim **21**, wherein the forming the source/drain region comprises:

performing a second recessing to recess portions of the isolation regions on opposite sides of an end portion of the semiconductor strip; and

performing an epitaxy to grow the source/drain region from a space left by the second recessing.

24. The method of claim **23**, wherein during the second recessing, portions of the isolation regions on opposite sides of the middle portion of the semiconductor strip is not recessed.

25. The method of claim **23** further comprising:

before the second recessing, forming a gate spacer, wherein after the forming the source/drain region, the source/drain region is in contact with the gate spacer.

26. The method of claim **21**, wherein the forming the gate stack comprises:

forming a gate dielectric layer on the top surface and the sidewalls of the semiconductor fin;

forming a conductive material over the gate dielectric layer; and

performing a Chemical Mechanical Polish (CMP) to form a gate dielectric and a gate electrode from the gate dielectric layer and the conductive material, respectively, wherein portions of the gate dielectric layer and the conductive material over the ILD are removed during the CMP.

* * * * *