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(54) STRAINED CHANNEL FIELD EFFECT TRANSISTOR

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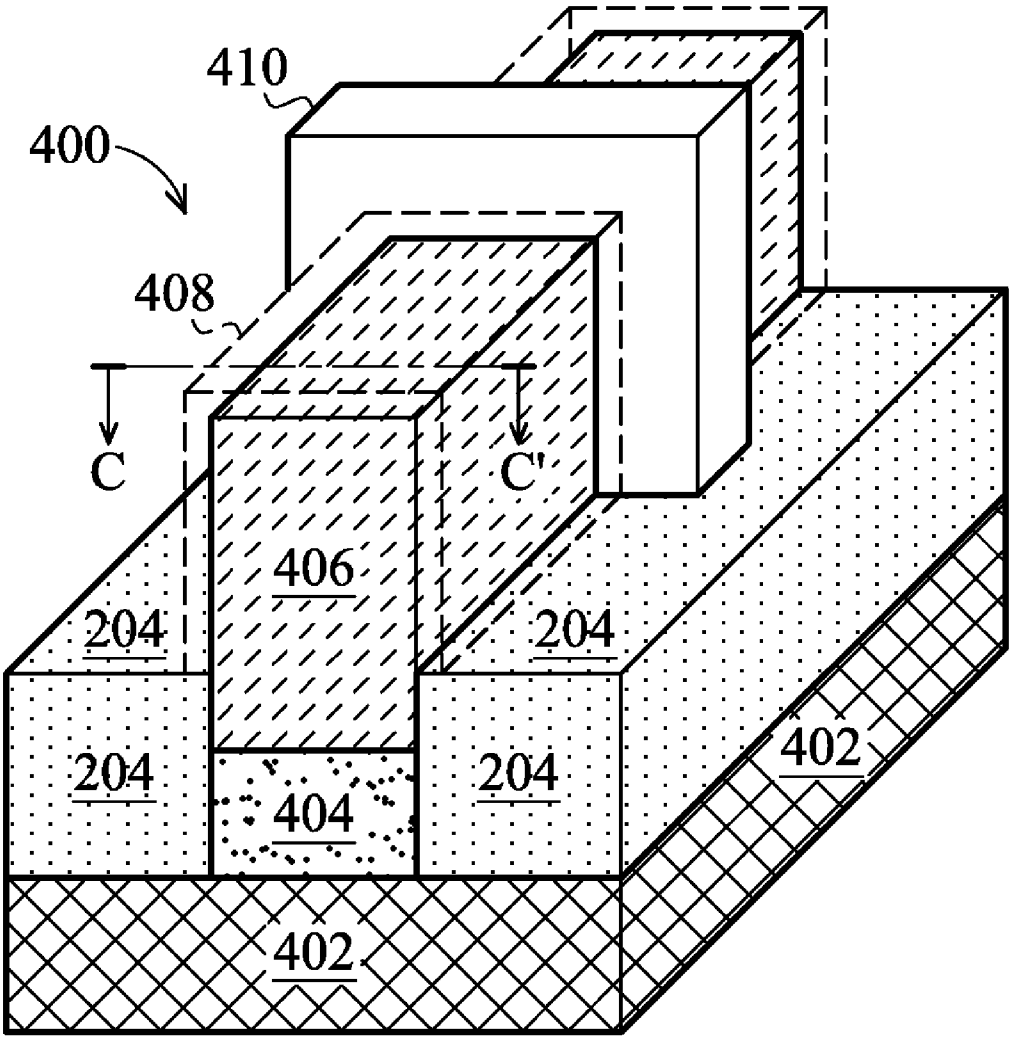
(57) **ABSTRACT**

The present disclosure provides a semiconductor device with a strained SiGe channel and a method for fabricating such a device. In an embodiment, a semiconductor device includes a substrate including at least two isolation features, a fin substrate disposed between and above the at least two isolation features, and an epitaxial layer disposed over exposed portions of the fin substrate. According to one aspect, the epitaxial layer may be disposed over a top surface and sidewalls of the fin substrate. According to another aspect, the fin substrate may be disposed substantially completely above the at least two isolation features.



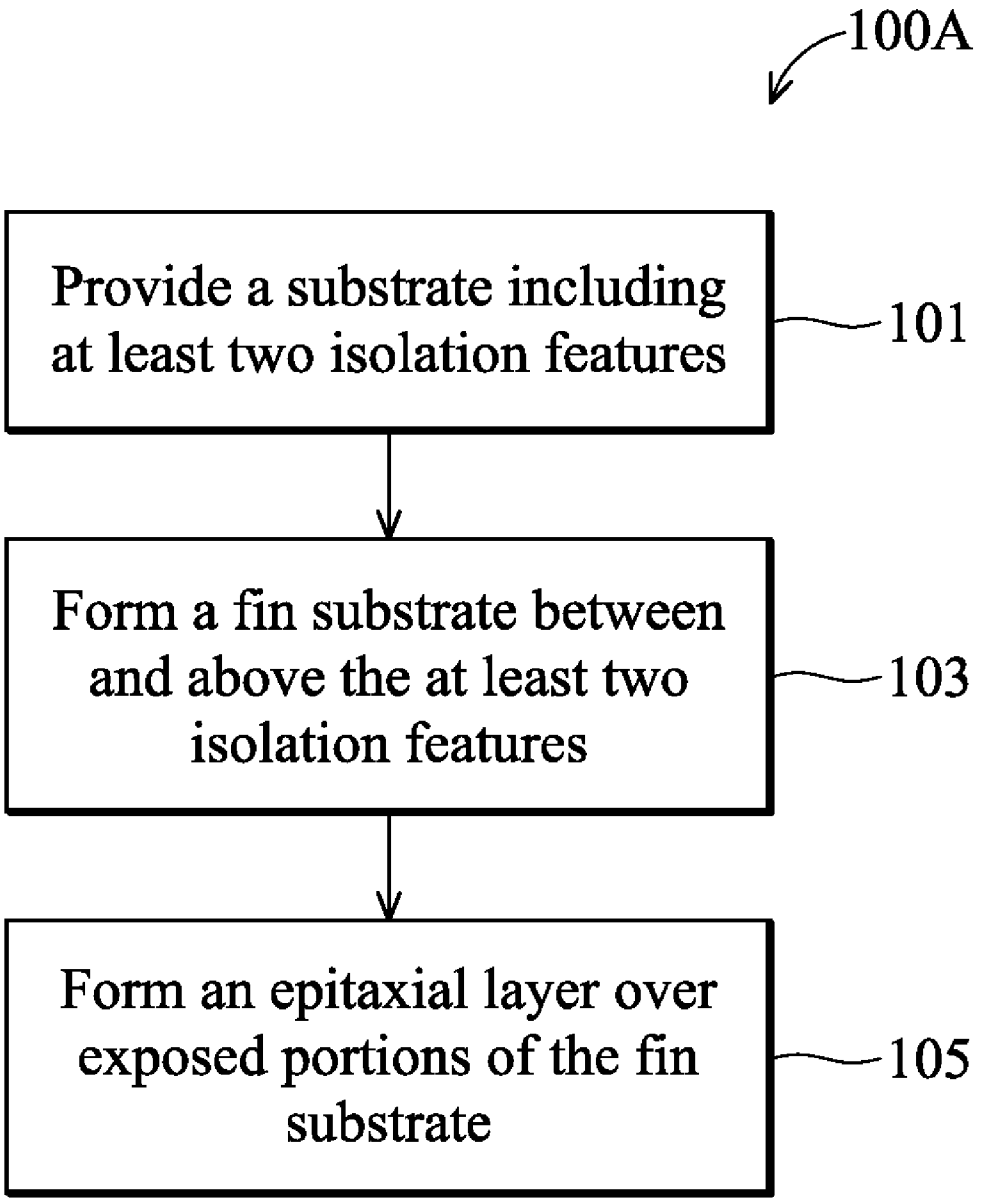

100A
Provide a substrate including at least two isolation features
101
Form a fin substrate between and above the at least two isolation features
103
Form an epitaxial layer over exposed portions of the fin substrate
105

FIG. 1A

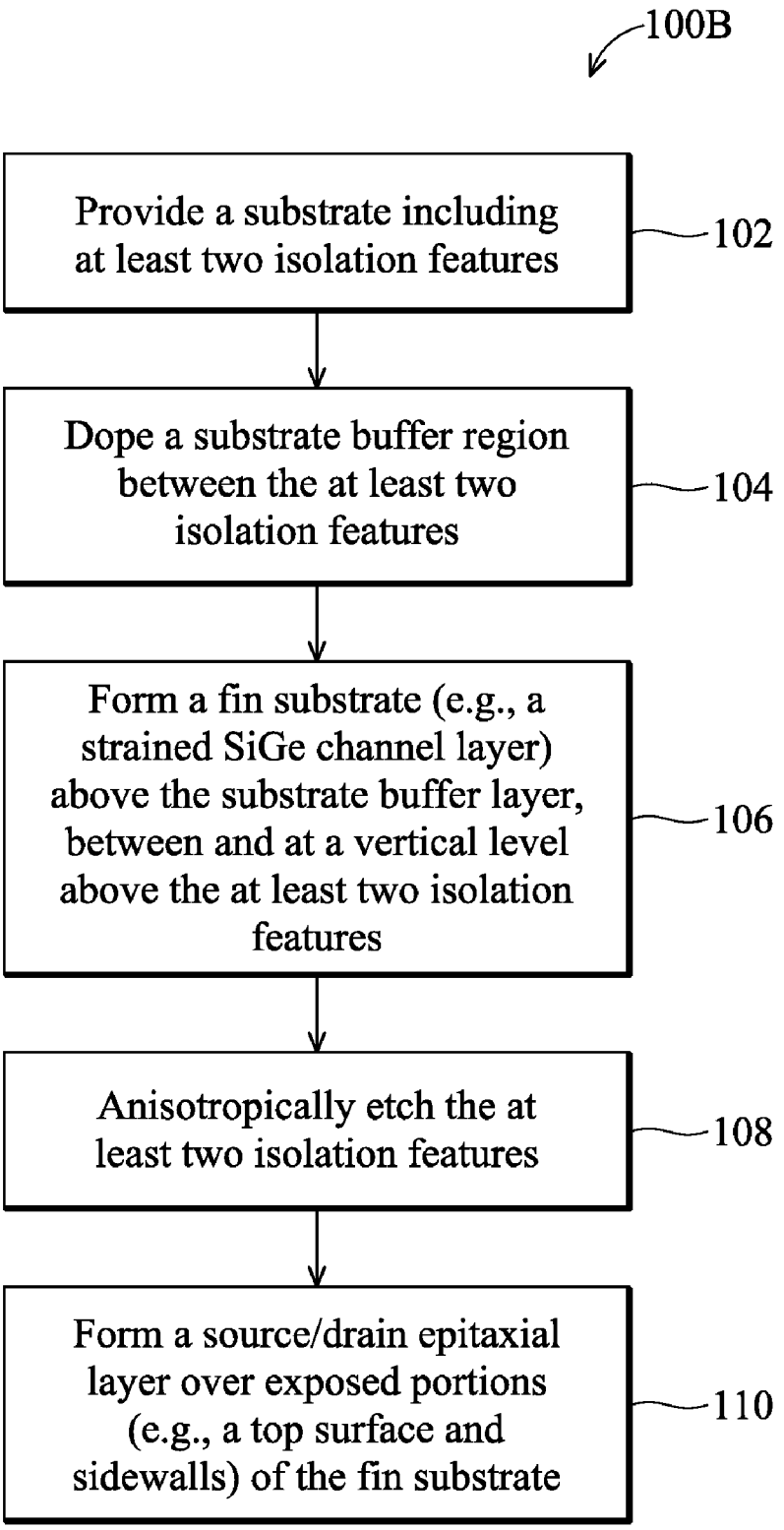

100B
Provide a substrate including at least two isolation features
102
Dope a substrate buffer region between the at least two isolation features
104
Form a fin substrate (e.g., a strained SiGe channel layer) above the substrate buffer layer, between and at a vertical level above the at least two isolation features
106
Anisotropically etch the at least two isolation features
108
Form a source/drain epitaxial layer over exposed portions (e.g., a top surface and sidewalls) of the fin substrate
110

FIG. 1B

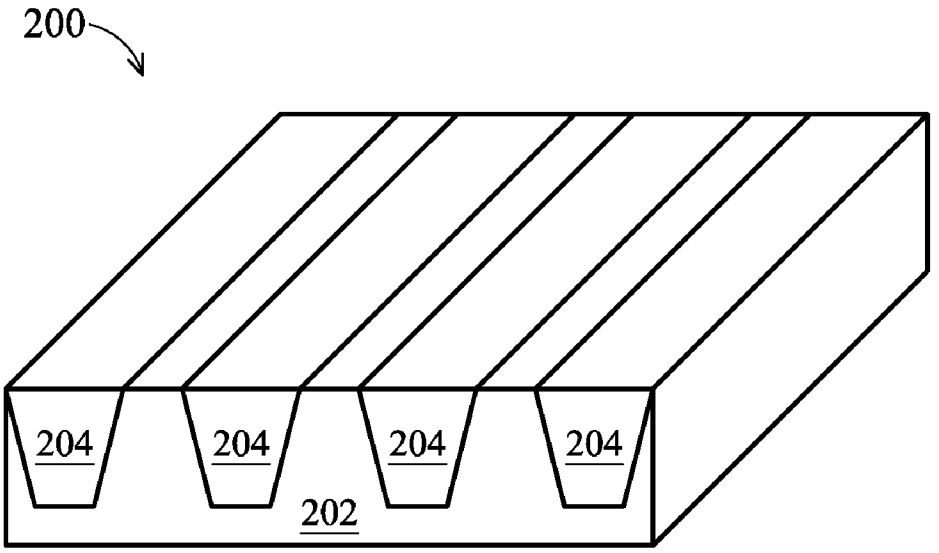


FIG. 2A

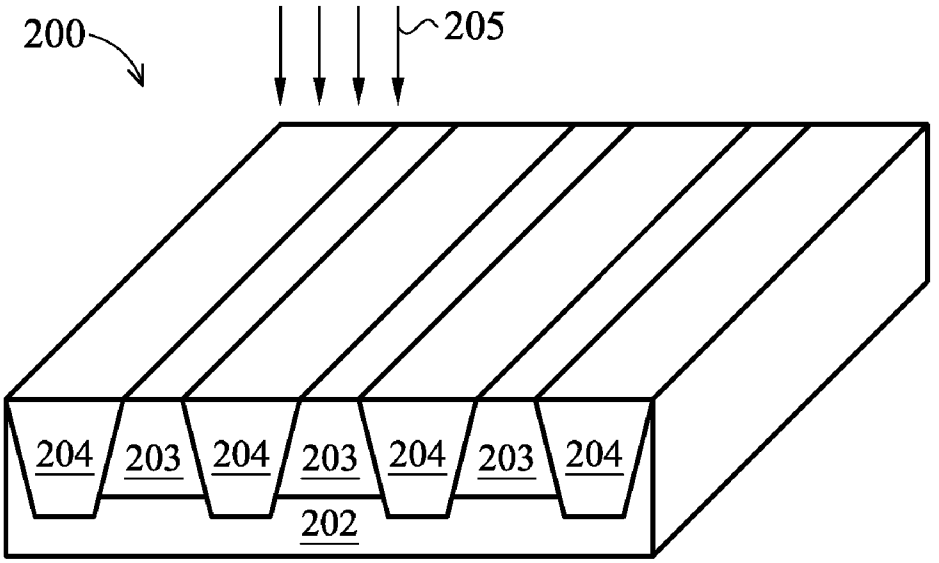


FIG. 2B

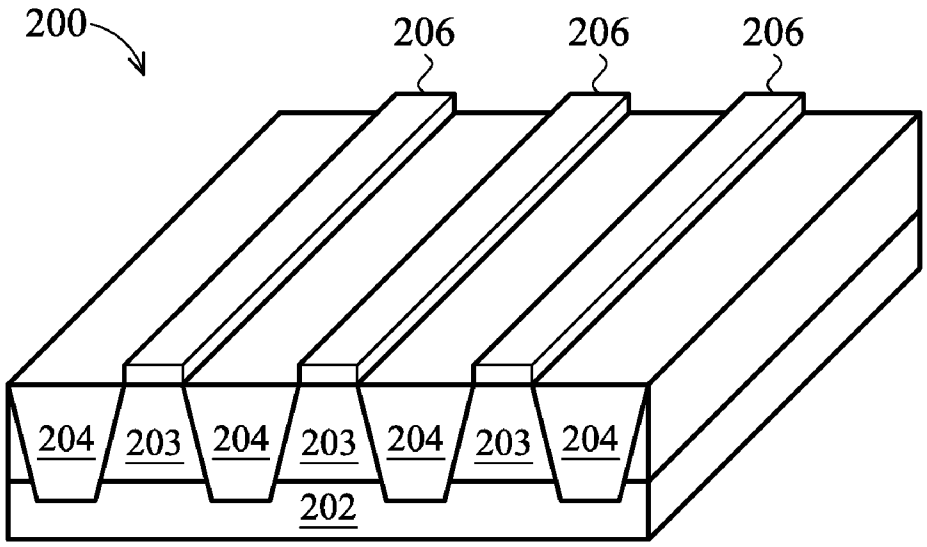
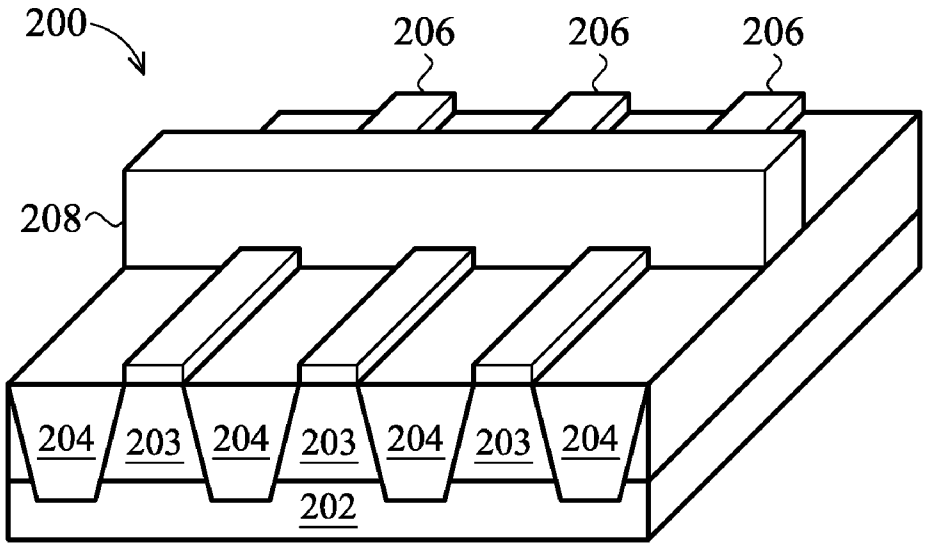

200
206
206
206
204
203
204
203
204
203
204
202

FIG. 2C


200
206
206
206
208
204
203
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203
204
203
204
202

FIG. 2D

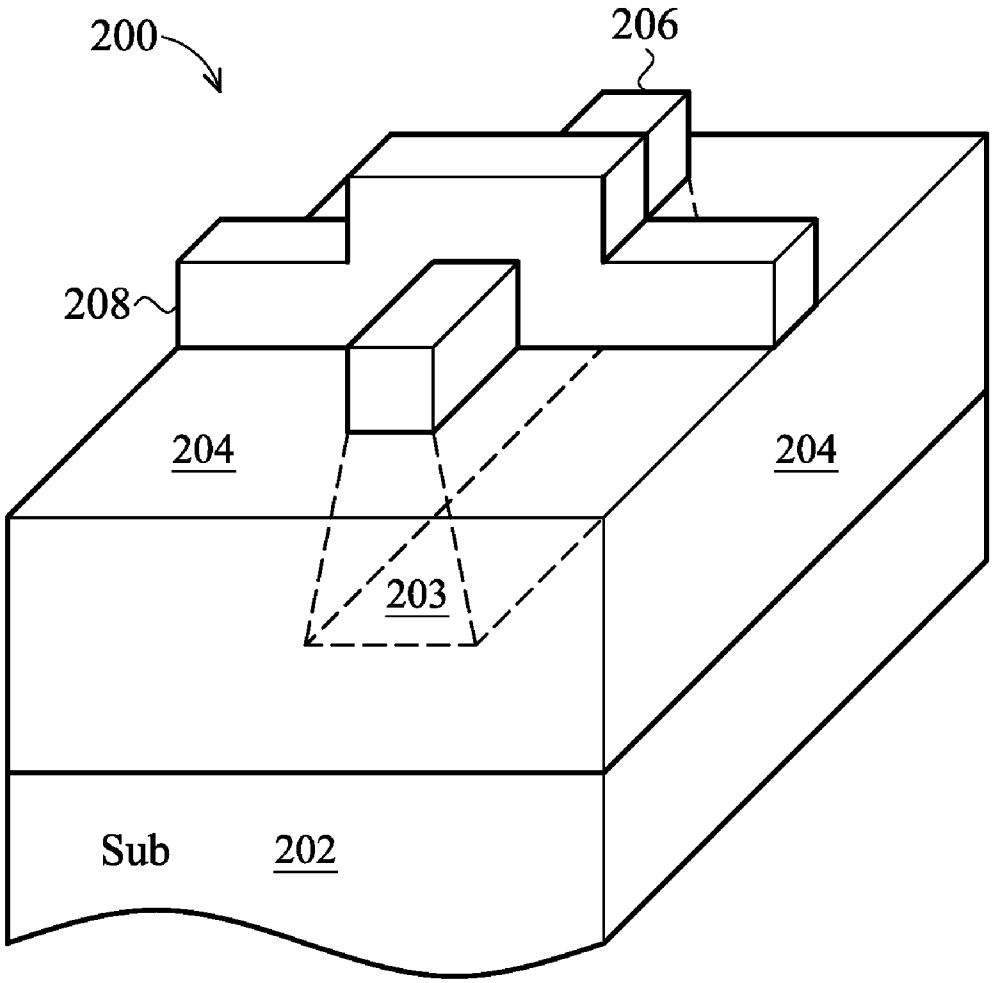


FIG. 3A

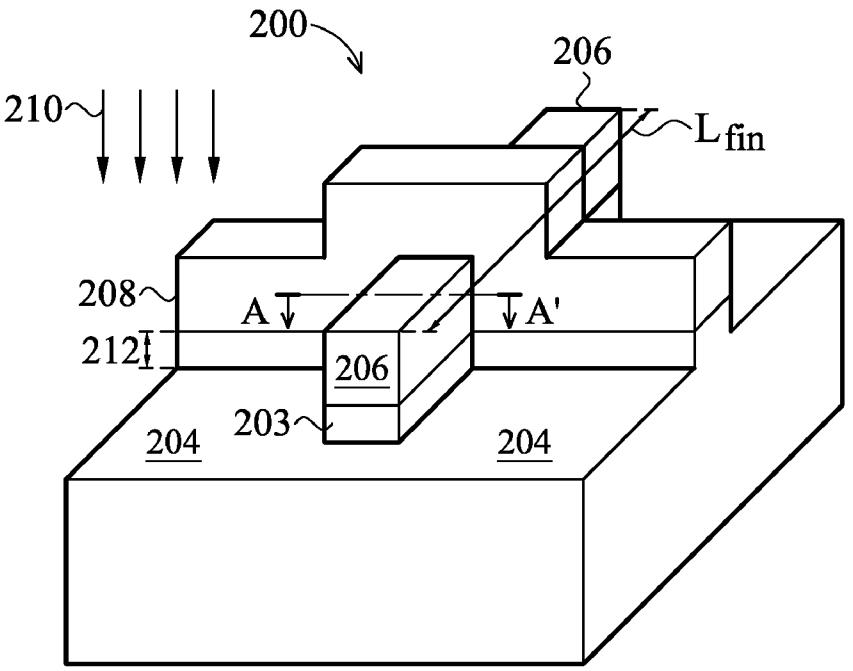

200
206
210
L_{fin}
208
A
A'
212
206
203
204
204

FIG. 3B

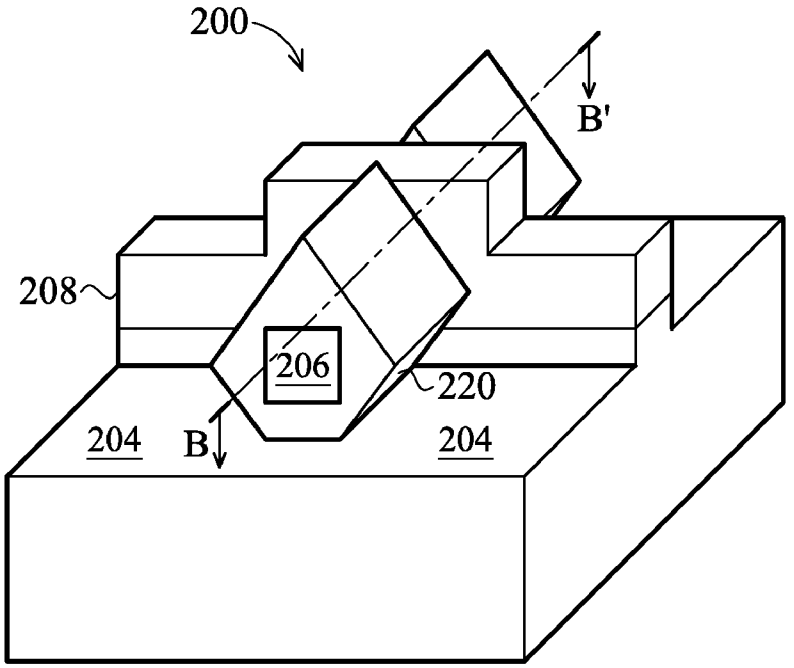

200
B'
208
206
220
204
B
204

FIG. 3C

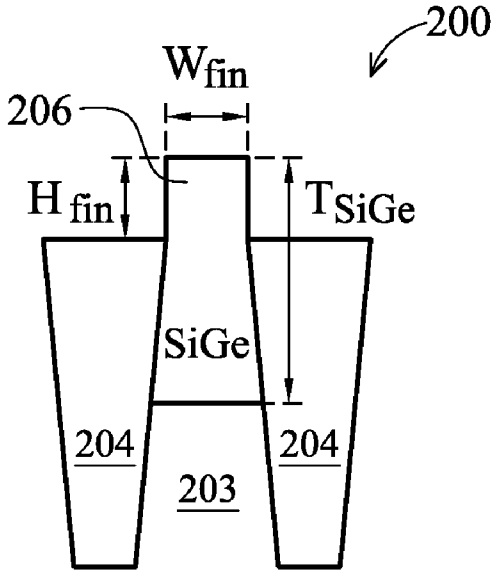

200
Wfin
206
H fin
TSiGe
SiGe
204
204
203

FIG. 4A

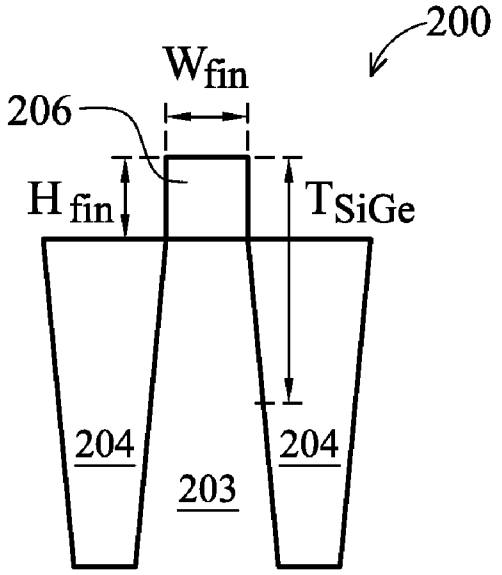

200
Wfin
206
H fin
TSiGe
204
204
203

FIG. 4B

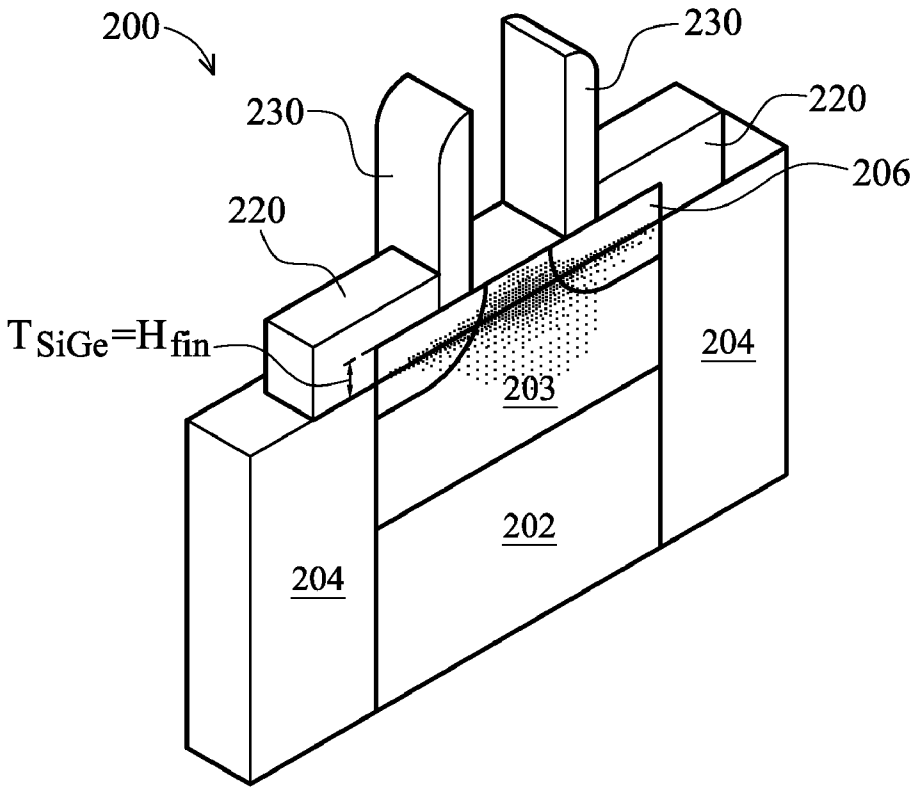

200
230
230
220
220
206
$T_{SiGe}=H_{fin}$
204
203
202
204

FIG. 5

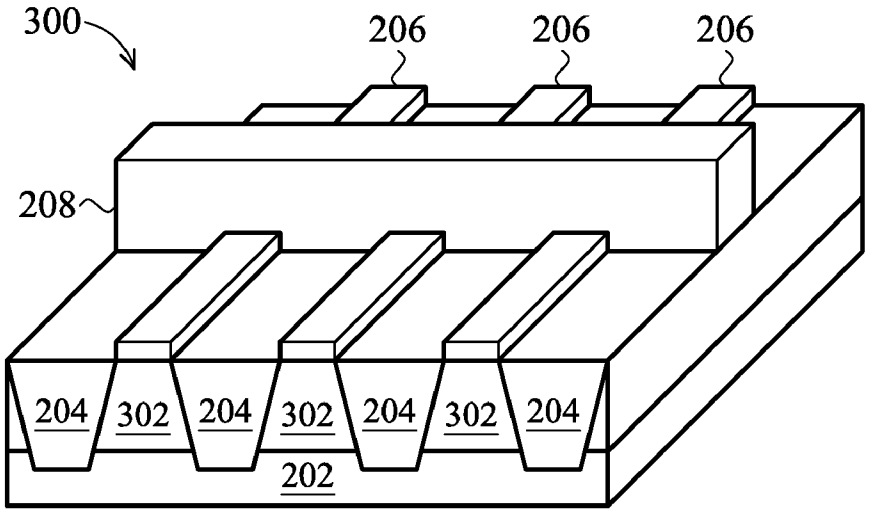

300
206
206
206
208
204
302
204
302
204
302
204
202

FIG. 6

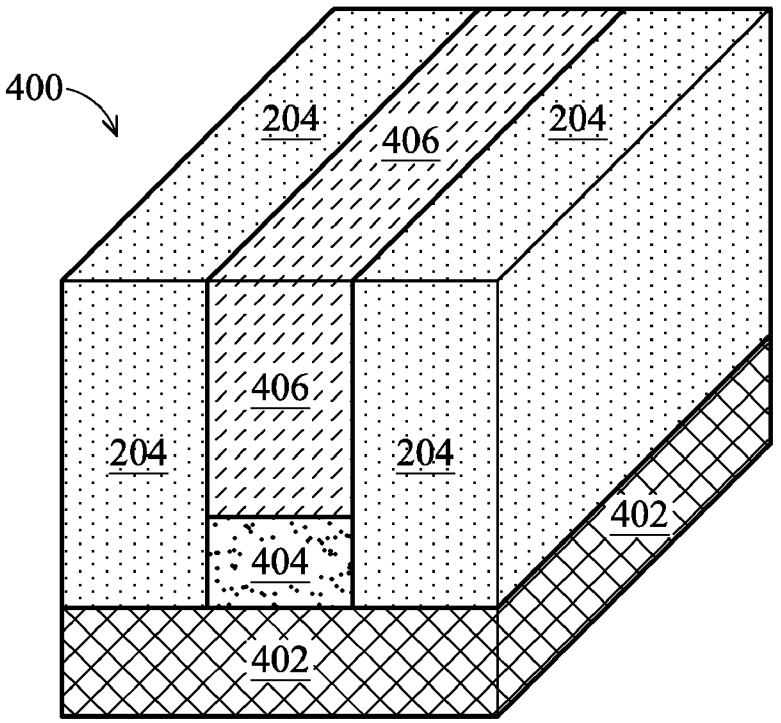
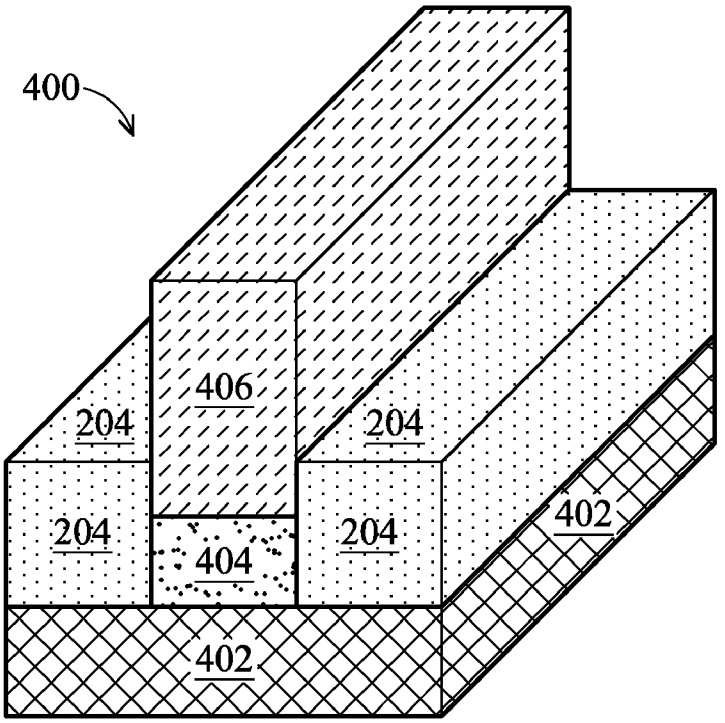

400
204
406
204
406
204
204
402
404
402

FIG. 7A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406
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204
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404
402

FIG. 7B

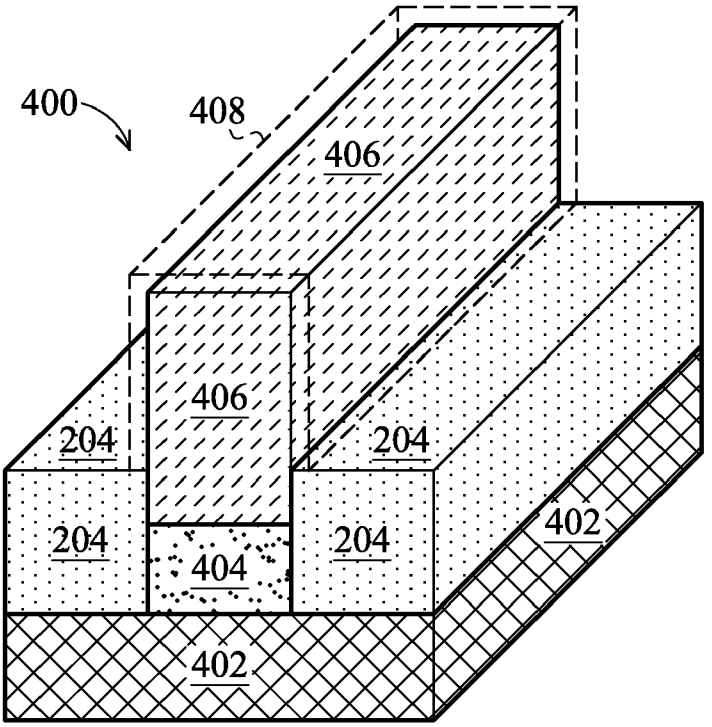

400
408
406
406
204
204
204
204
404
402
402

FIG. 7C

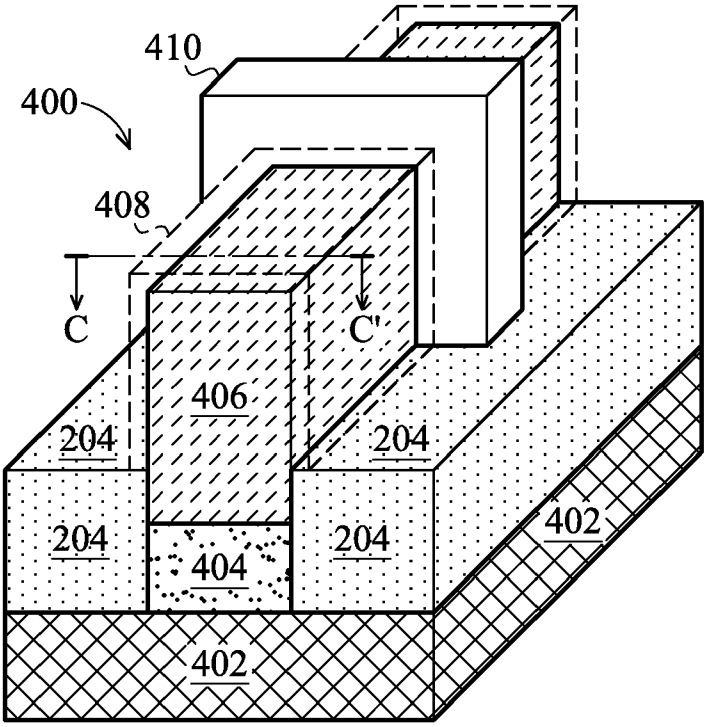

410
400
408
C
C'
406
204
204
204
204
404
402
402

FIG. 7D

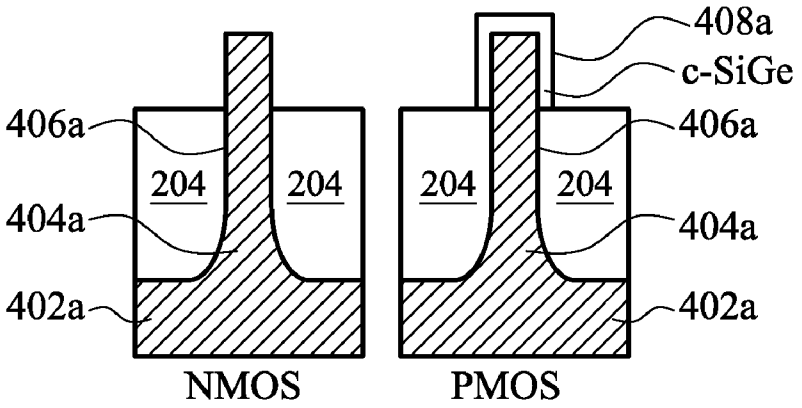


FIG. 8A

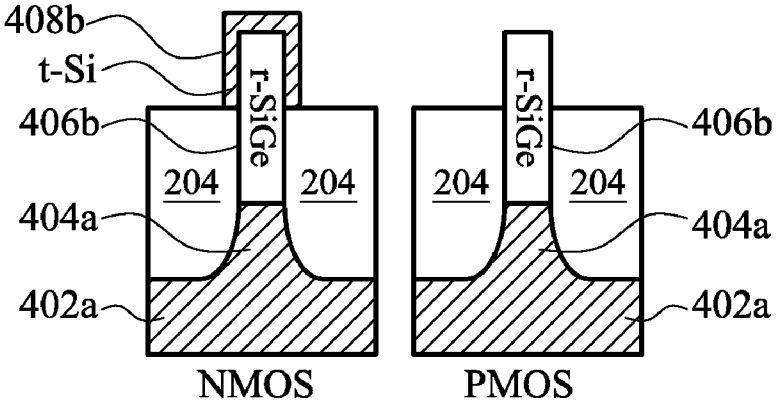


FIG. 8B

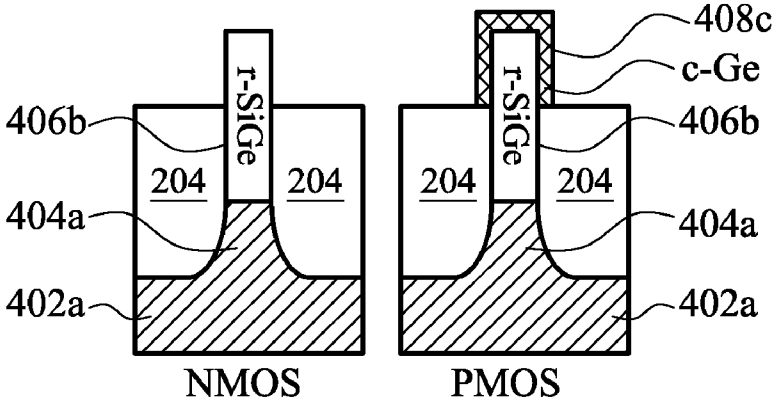


FIG. 8C

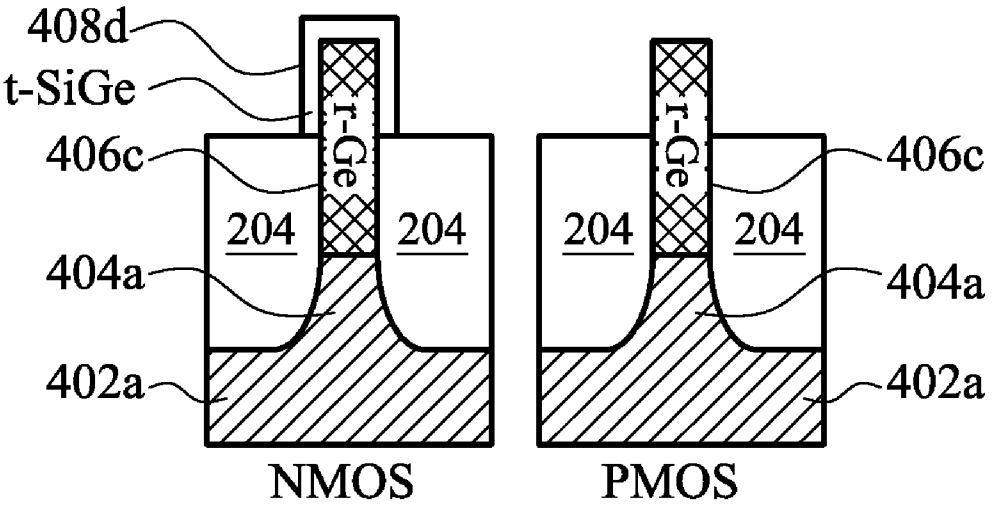

408d
t-SiGe
406c
404a
402a
r-Ge
204
204
NMOS
r-Ge
204
204
406c
404a
402a
PMOS

FIG. 8D

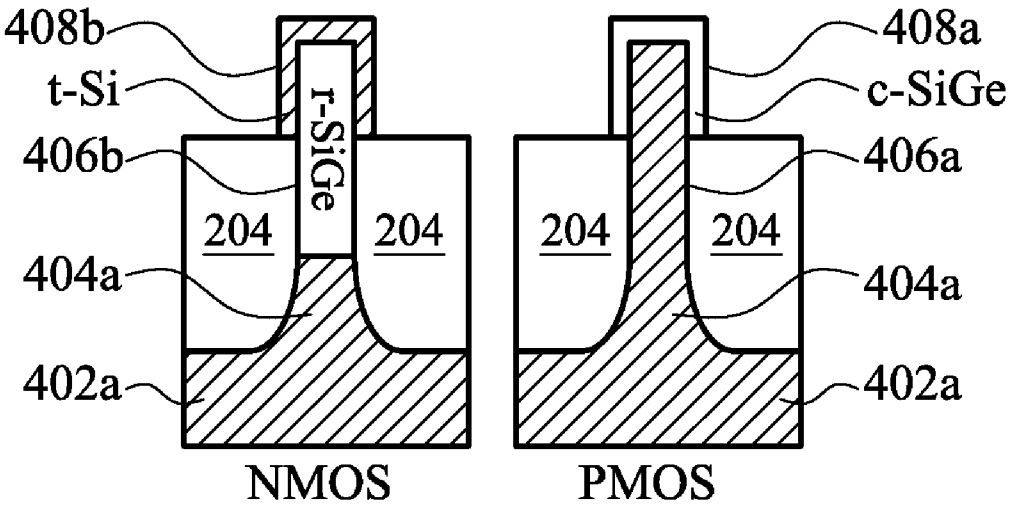

408b
t-Si
406b
404a
402a
r-SiGe
204
204
NMOS
204
204
408a
c-SiGe
406a
404a
402a
PMOS

FIG. 8E

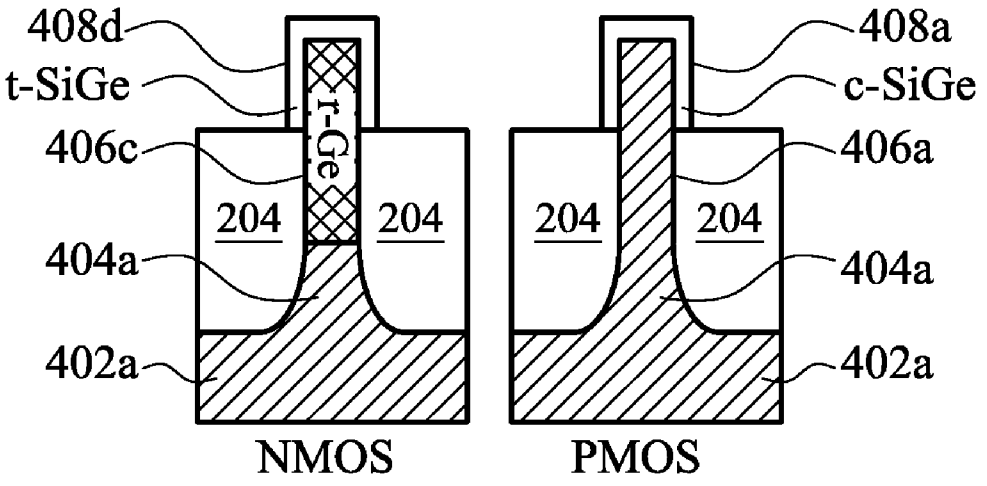

408d
t-SiGe
406c
404a
402a
r-Ge
204
204
NMOS
408a
c-SiGe
406a
404a
402a
204
204
PMOS

FIG. 8F

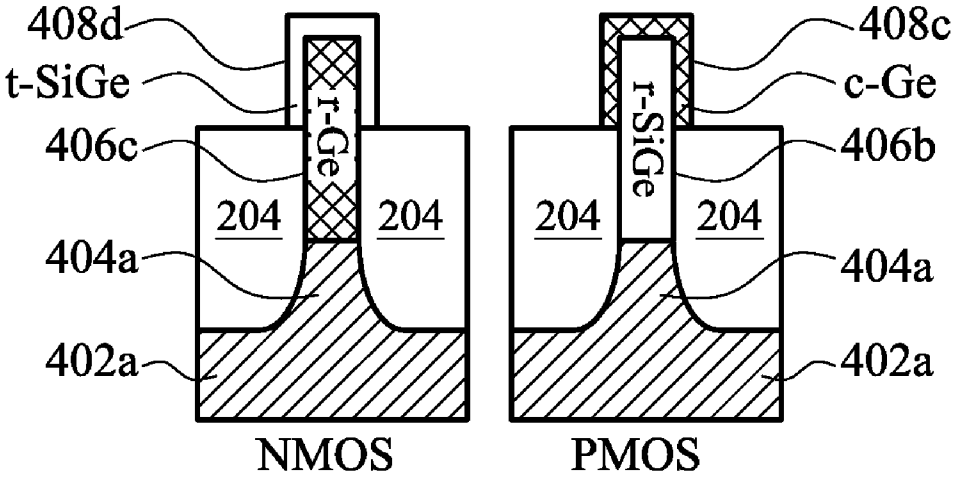

408d
t-SiGe
406c
404a
402a
r-Ge
204
204
NMOS
408c
c-Ge
406b
404a
402a
r-SiGe
204
204
PMOS

FIG. 8G

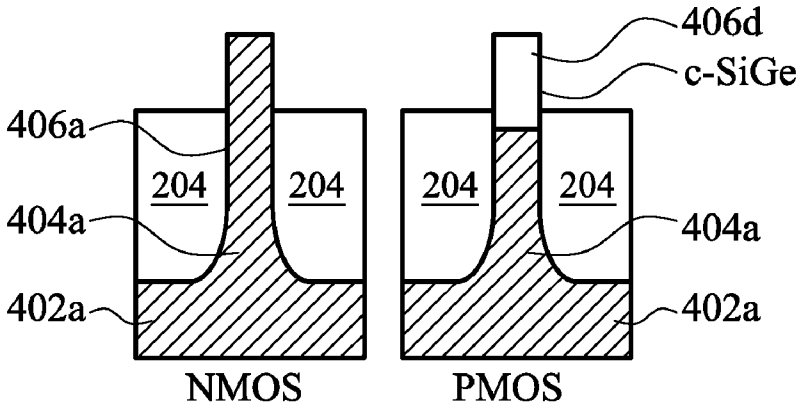


FIG. 9A

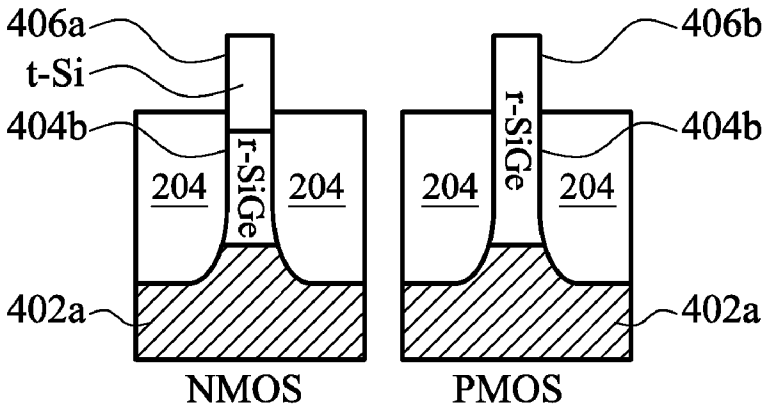


FIG. 9B

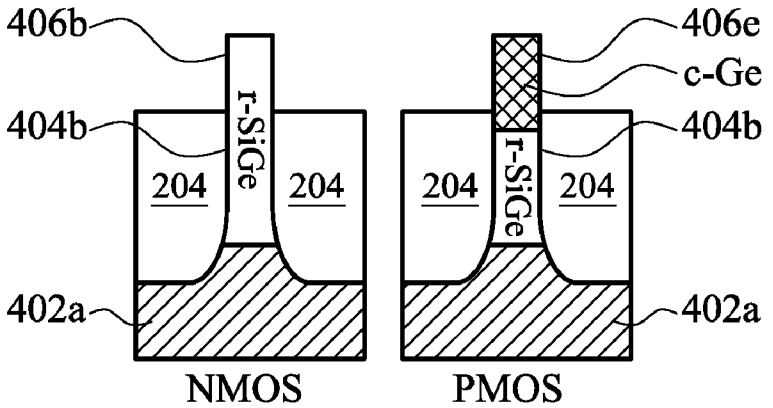


FIG. 9C

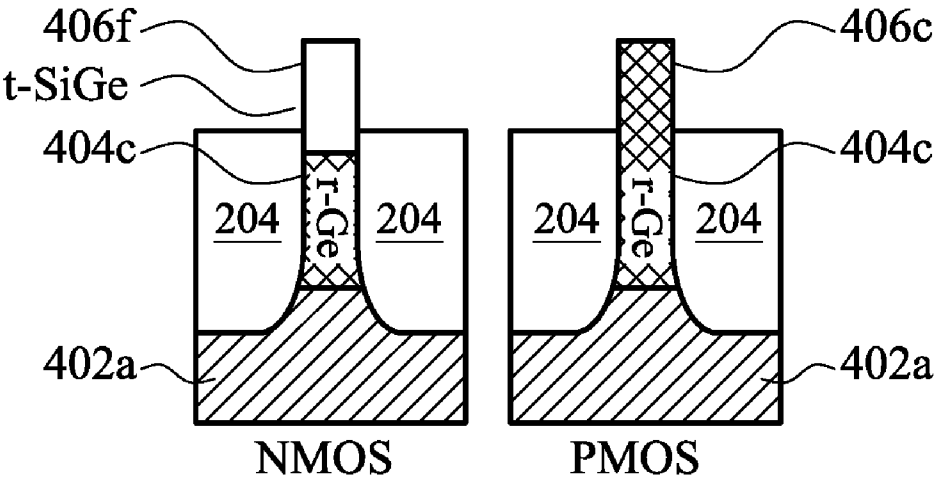

406f
t-SiGe
404c
204
r-Ge
204
402a
NMOS
406c
404c
204
r-Ge
204
402a
PMOS

FIG. 9D

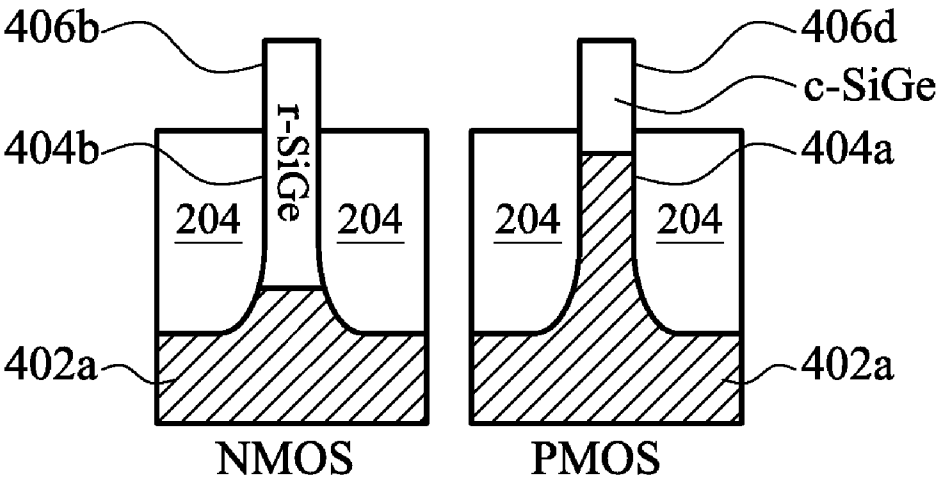

406b
404b
r-SiGe
204
204
402a
NMOS
406d
c-SiGe
404a
204
204
402a
PMOS

FIG. 9E

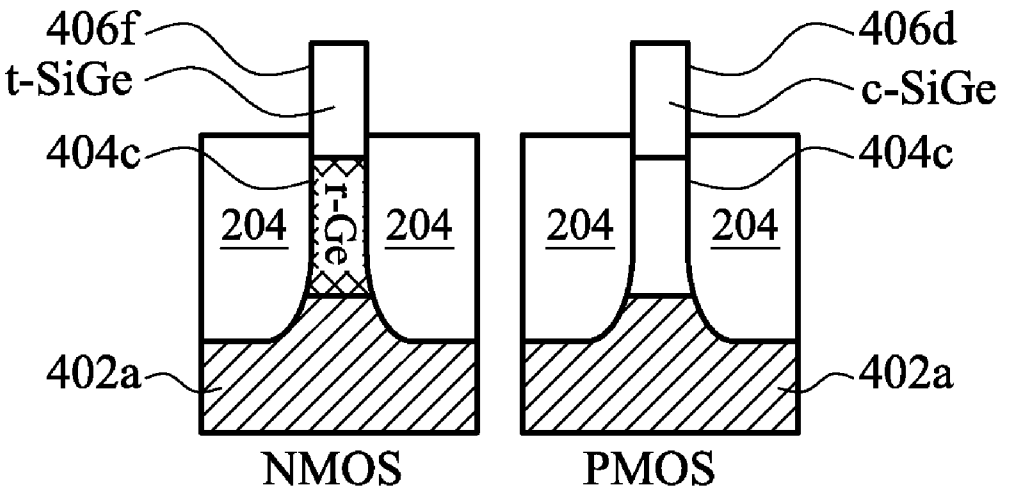
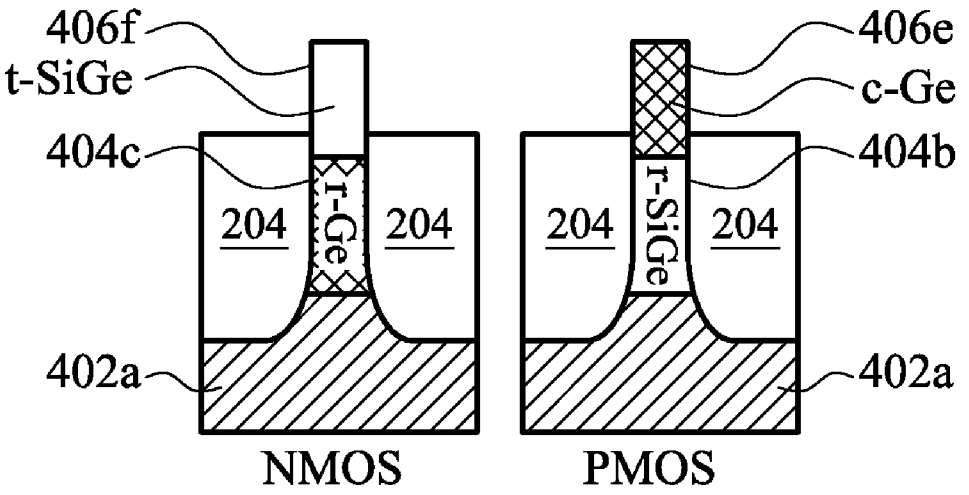

406f
t-SiGe
404c
r-Ge
204
204
402a
NMOS
406d
c-SiGe
404c
204
204
402a
PMOS

FIG. 9F


406f
t-SiGe
404c
r-Ge
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406e
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404b
r-SiGe
204
204
402a
PMOS

FIG. 9G

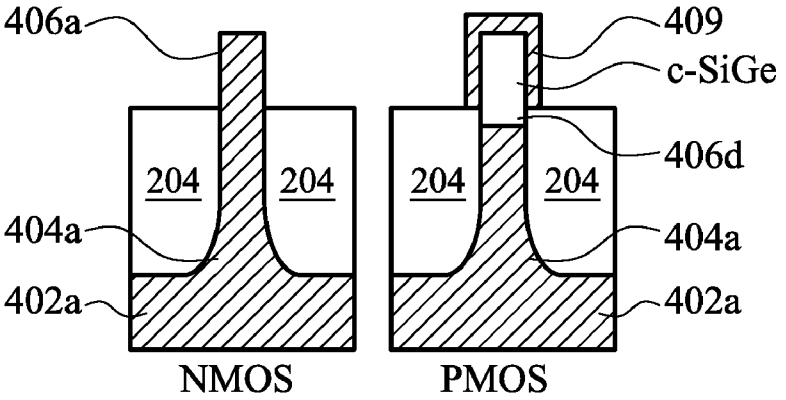

FIG. 10A

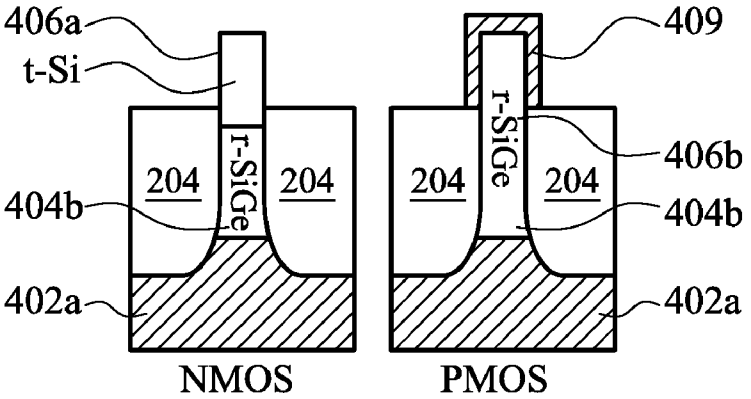

FIG. 10B

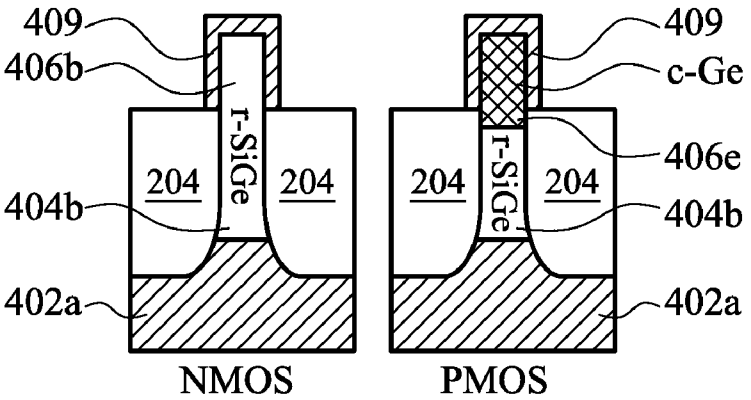

FIG. 10C

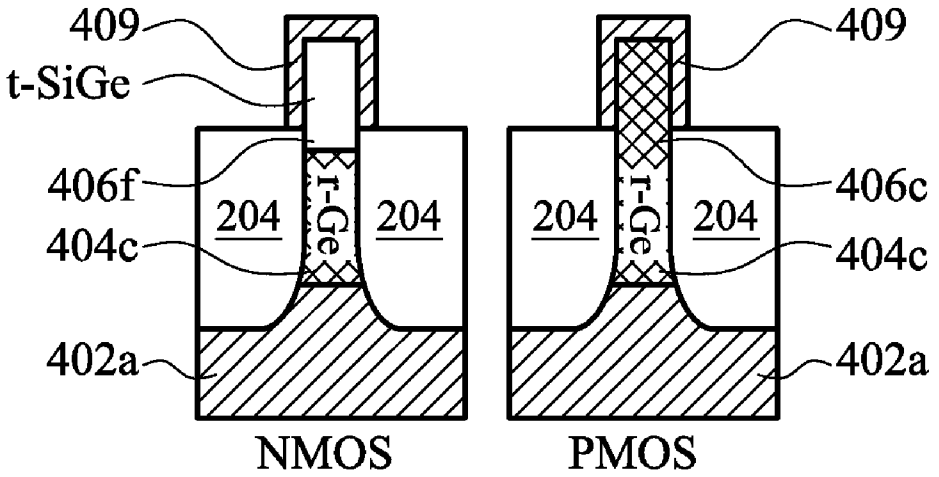

FIG. 10D

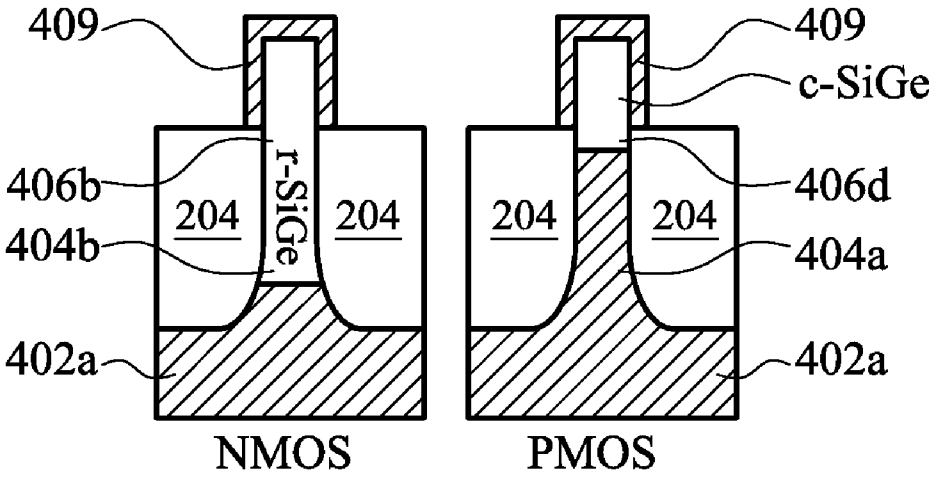

FIG. 10E

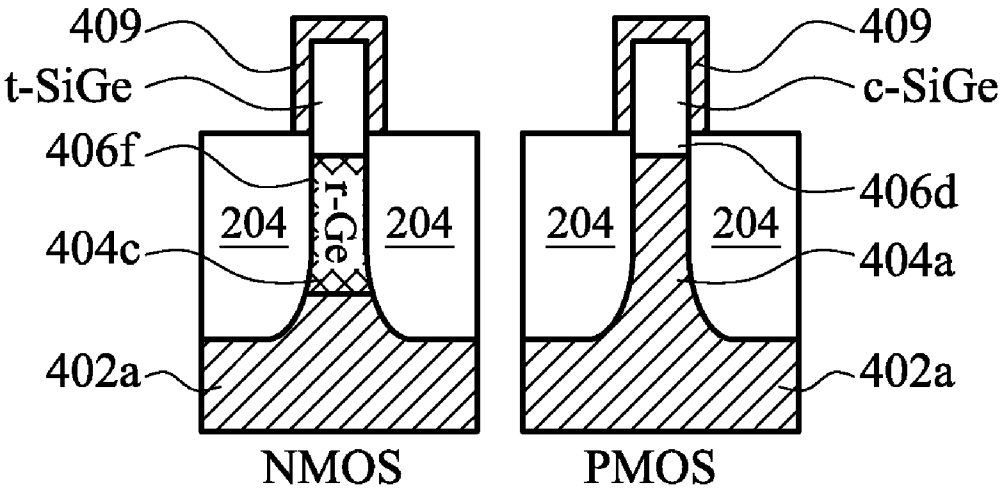

FIG. 10F

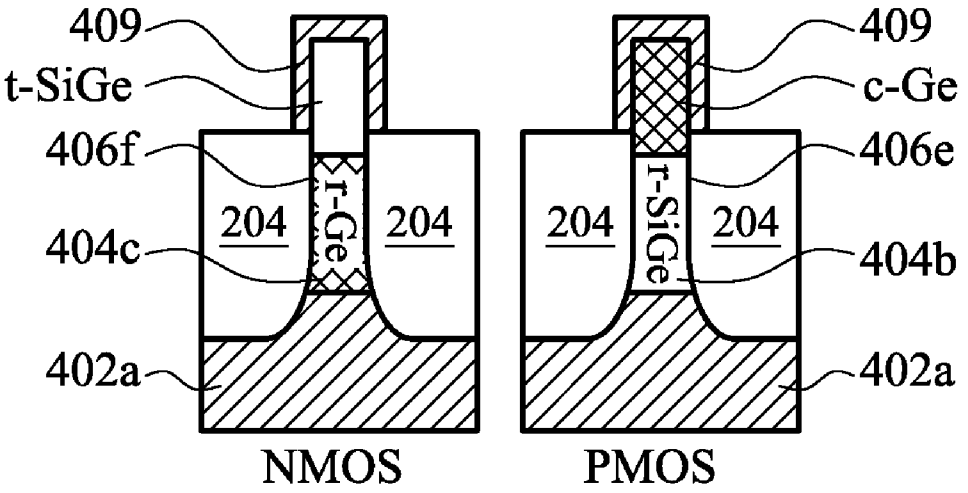

FIG. 10G

STRAINED CHANNEL FIELD EFFECT TRANSISTOR

BACKGROUND

[0001] Variations of metal-oxide-semiconductor field-effect transistor (MOSFET) structures have been explored for improvement in manufacturability and performance. One variation has been known as a "finFET", which includes a strip or "fin" of a material, such as silicon, and a gate formed to surround the fin on three exposed sides. The channel region of the device is located in the fin, and introduction of strain into such a strip or fin has been explored.

[0002] Silicon germanium (SiGe) fins located in the channel regions of a complementary metal-oxide-semiconductor (CMOS) device have been used to increase field effect transistor (FET) performance. However, as the fin length scales to larger lengths, axial stress components imparted on the fin may become relaxed and cause less than optimal finFET performance.

SUMMARY

[0003] The present disclosure provides for many different embodiments. According to one embodiment, a semiconductor device is provided. The device includes a substrate including at least two isolation features, a fin substrate disposed between and above the at least two isolation features, and an epitaxial layer disposed over exposed portions of the fin substrate. According to one aspect, the epitaxial layer may be disposed over a top surface and sidewalls of the fin substrate. According to another aspect, the fin substrate may be disposed substantially completely above the at least two isolation features.

[0004] In yet another embodiment, a semiconductor device includes a substrate including at least two isolation features, a substrate buffer region disposed between the at least two isolation features, and a fin substrate disposed above the substrate buffer region, between the at least two isolation features, and at a vertical level substantially completely above the at least two isolation features. The device further includes a source/drain epitaxial layer disposed over a top surface and sidewalls of the fin substrate.

[0005] The present disclosure also provides for a method of fabricating a semiconductor device. In one embodiment, the method includes providing a substrate including at least two isolation features, forming a fin substrate between the at least two isolation features, and at a vertical level above the at least two isolation features, and forming an epitaxial layer over exposed portions of the fin substrate. According to one aspect, the epitaxial layer may be deposited over a top surface and sidewalls of the fin substrate. According to another aspect, the fin substrate may be deposited substantially completely above the at least two isolation features.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0007] FIGS. **1**A and **1**B are flowcharts of methods of fabricating a semiconductor device in accordance with embodiments of the present disclosure.

[0008] FIGS. **2**A-**2**D and **3**A-**3**C are perspective cross-sectional views of a semiconductor device at various stages of fabrication in accordance with an embodiment of the present disclosure.

[0009] FIGS. **4**A and **4**B are embodiments of cross-sectional views of the semiconductor device of FIG. **3**B along a line A-A' in accordance with embodiments of the present disclosure.

[0010] FIG. **5** is a perspective cross-sectional view of the semiconductor device of FIG. **3**C along a line B-B' in accordance with embodiments of the present disclosure.

[0011] FIG. **6** is a perspective cross-sectional view of another semiconductor device in accordance with an embodiment of the present disclosure.

[0012] FIGS. **7**A-**7**D are perspective cross-sectional views of another semiconductor device at various stages of fabrication in accordance with an embodiment of the present disclosure.

[0013] FIGS. **8**A-**8**G, **9**A-**9**G, and **10**A-**10**G are embodiments of cross-sectional views of the semiconductor device of FIG. **7**D along a line C-C' in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

[0014] It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the disclosure. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. Moreover, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed interposing the first and second features, such that the first and second features may not be in direct contact. Various features may be arbitrarily drawn in different scales for the sake of simplicity and clarity. It is noted that the same or similar features may be similarly numbered herein for the sake of simplicity and clarity. In addition, some of the drawings may be simplified for clarity. Thus, the drawings may not depict all of the components of a given apparatus (e.g., device) or method.

[0015] Various aspects of the present disclosure will be described herein with reference to drawings that are schematic illustrations of idealized configurations of the present disclosure. As such, variations from the shapes of the illustrations as a result, for example, manufacturing techniques and/or tolerances, are to be expected. Thus, the various aspects of the present disclosure presented throughout this disclosure should not be construed as limited to the particular shapes of elements (e.g., regions, layers, sections, substrates, etc.) illustrated and described herein but are to include deviations in shapes that result, for example, from manufacturing. By way of example, an element illustrated or described as a rectangle may have rounded or curved features and/or a gradient concentration at its edges rather than a discrete change from one element to another. Thus, the elements illustrated in the drawings are schematic in nature and their shapes are not intended to illustrate the precise shape of an element and are not intended to limit the scope of the present disclosure.

[0016] It will be understood that when an element such as a region, layer, section, substrate, or the like, is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. It will be further understood that when an element is referred to as being "formed" on another element, it can be grown, deposited, etched, attached, connected, coupled, or otherwise prepared or fabricated on the other element or an intervening element.

[0017] Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top", may be used herein to describe one element's relationship to another element as illustrated in the drawings. It will be understood that relative terms are intended to encompass different orientations of an apparatus in addition to the orientation depicted in the drawings. By way of example, if an apparatus in the drawings is turned over, elements described as being on the "lower" side of other elements would then be oriented on the "upper" sides of the other elements. The term "lower", can therefore, encompass both an orientation of "lower" and "upper", depending on the particular orientation of the apparatus. Similarly, if an apparatus in the drawing is turned over, elements described as "below" or "beneath" other elements would then be oriented "above" the other elements. The terms "below" or "beneath" can, therefore, encompass both an orientation of above and below.

[0018] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and this disclosure.

[0019] As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising", when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof. The term "and/or" includes any and all combinations of one or more of the associated listed items

[0020] It will be understood that although the terms "first" and "second" may be used herein to describe various regions, layers and/or sections, these regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one region, layer or section from another region, layer or section. Thus, a first region, layer or section discussed below could be termed a second region, layer or section, and similarly, a second region, layer or section may be termed a first region, layer or section without departing from the teachings of the present disclosure.

[0021] It is understood that several processing steps and/or features of a device may be only briefly described, such steps and/or features being well known to those of ordinary skill in the art. Also, additional processing steps or features can be added, and certain of the following processing steps or features can be removed and/or changed while still implementing the claims. Thus, the following description should be understood to represent examples only, and are not intended to suggest that one or more steps or features is required.

[0022] Referring now to FIG. **1**A, a flowchart is shown illustrating a method **100**A for fabricating a semiconductor device in accordance with an embodiment of the present disclosure. The method **100**A includes providing a substrate including at least two isolation features at block **101**, depositing a fin substrate between and above the at least two isolation features at block **103**, and depositing an epitaxial layer over exposed portions of the fin substrate at block **105**.

[0023] Referring now to FIG. **1**B, a flowchart is shown illustrating a method **100**B for fabricating a semiconductor device in accordance with another embodiment of the present disclosure. The method **100**B begins at block **102** with providing a substrate including at least two isolation features. The isolation features may include shallow trench isolation (STI) features filled with an oxide or dielectric, but other isolation features may be used and are within the scope of the present disclosure.

[0024] The substrate may include various semiconductor devices, and/or other suitable active and/or passive devices. Example semiconductor devices include integrated circuits including a metal-insulator-semiconductor field effect transistor (MOSFET) including complementary MOSFET (CMOS) features, CIS, and/or other suitable active and/or passive devices. In an embodiment, the substrate may include an integrated circuit (or portion thereof) designed and formed using a CMOS-based process. A substrate having a device (e.g., integrated circuit) formed by other semiconductor fabrication technologies is also within the scope of the described method.

[0025] At block **104**, method **100**B further includes doping a substrate buffer region between the at least two isolation features.

[0026] At block **106**, method **100**B further includes depositing a fin substrate (e.g., a strained silicon germanium (SiGe) channel layer) above the substrate buffer region, between the at least two isolation features, and at a vertical level above the at least two isolation features.

[0027] At block **108**, method **100**B further includes anisotropically etching the at least two isolation features.

[0028] At block **110**, method **100**B further includes depositing a source/drain epitaxial layer over exposed portions of the fin substrate (e.g., the strained SiGe channel layer). In one example, the source/drain epitaxial layer is deposited to cover exposed surfaces (e.g., of the strained SiGe channel layer). In another example, the epitaxial layer is deposited at a vertical level above etched regions of the at least two isolation features (e.g., etched oxide of the isolation feature). In yet another example, the epitaxial layer is deposited over a top surface and sidewalls of the fin substrate.

[0029] The various structures in the methods **100**A and **100**B described above may be formed by various deposition, pattern, and/or etch techniques. It should be noted that the operations of the methods **100**A and **100**B may be rearranged or otherwise modified within the scope of the various aspects. It is further noted that additional processes may be provided before, during, and after the methods **100**A and **100**B of FIGS. **1**A and **1**B, and that some other processes may only be briefly described herein. Thus, other implementations are possible with the scope of the various aspects described herein.

[0030] In one example, the methods **100**A and **100**B may further include forming a gate electrode directly over the fin

substrate (or strained SiGe channel layer) or directly over the epitaxial layer, and/or forming spacers adjacent the sides of the gate electrode. In other words, in one embodiment, the epitaxial layer may be deposited to cover surfaces of the fin substrate not masked by the gate electrode and/or the spacers, or in another embodiment, the gate electrode and/or the spacers may be formed over the epitaxial layer.

[0031] In another example, the substrate, the fin substrate, and the epitaxial layer may each be comprised of silicon (Si), germanium (Ge), or a combination of Si and Ge. In other embodiments, the substrate, the fin substrate, and the epitaxial layer may each be comprised of other materials, such as Group III-V compounds or combinations thereof (e.g., InGaAs, InAs, GaSb, or InGaSb as channel material and AlAsSb as a buffer). The material of the substrate, fin substrate, and epitaxial layer may each be chosen such that the resulting stress is beneficial for either holes or electrons depending on the type of device being fabricated.

[0032] In yet another example, the fin substrate may be deposited as a strained SiGe channel layer comprised of between about 25% Ge and about 50% Ge, having a length between about 100 nm and about 200 nm, a width between about 10 nm and about 20 nm, and a thickness between about 10 nm and about 40 nm. In other examples, the fin substrate may have a lower limit length of about 100 nm and substantially no upper limit length.

[0033] In yet another example, the fin substrate may be deposited as a strained SiGe channel layer comprised of about 50% Ge, having a length of about 100 nm or greater, a width of about 10 nm, and a height above the at least two isolation features of about 10 nm.

[0034] In yet another example, the fin substrate or the epitaxial layer may be deposited to have a compressive uni-axial strain forming a PMOS device, or wherein the fin substrate is deposited to have a tensile uni-axial strain forming an NMOS device.

[0035] In yet another example, the epitaxial layer may be deposited as a passivation layer comprised of silicon.

[0036] Referring now to FIGS. **2**A-**2**D, perspective cross-sectional views of a semiconductor device at various stages of fabrication are illustrated in accordance with an embodiment of the present disclosure. FIG. **2**A illustrates a semiconductor device **200** having a substrate **202** including a plurality of (and at least two) isolation features **204**.

[0037] In one embodiment, substrate **202** may include a semiconductor substrate, and may be comprised of silicon, or alternatively may include silicon germanium, gallium arsenide, or other suitable semiconductor materials. The substrate may further include doped active regions and other features such as a buried layer, and/or an epitaxy layer. Furthermore, the substrate may be a semiconductor on insulator such as silicon on insulator (SOI). In other embodiments, the semiconductor substrate may include a doped epitaxy layer, a gradient semiconductor layer, and/or may further include a semiconductor layer overlying another semiconductor layer of a different type such as a silicon layer on a silicon germanium layer. In other examples, a compound semiconductor substrate may include a multilayer silicon structure or a silicon substrate may include a multilayer compound semiconductor structure. The active region may be configured as an NMOS device (e.g., nFET) or a PMOS device (e.g., pFET). The semiconductor substrate may include underlying layers, devices, junctions, and other features (not shown) formed during prior process steps or which may be formed during subsequent process steps.

[0038] In one embodiment, substrate **202** is comprised of silicon (Si), germanium (Ge), or a combination of Si and Ge, depending upon whether PMOS or NMOS devices are being fabricated. In one example, substrate **202** is comprised of silicon and substrate buffer region **203** is doped with p-type dopants to fabricate a PMOS device. In another example, substrate **202** is comprised of germanium or a combination of silicon and germanium and substrate buffer region **203** is doped with n-type dopants to fabricate an NMOS device.

[0039] The isolation features **204** may include shallow trench isolation (STI) features filled with an oxide or dielectric, but other isolation features may be used and are within the scope of the present disclosure. The oxide or dielectric of isolation features **204** may be formed by various processes, such as thermal oxidation and/or plasma enhanced chemical vapor deposition (PECVD).

[0040] In one embodiment, semiconductor substrate **202** may be comprised of single crystalline, P type silicon, featuring a <100> crystallographic orientation. Other crystallographic orientations are within the scope of the present disclosure. A silicon nitride layer, for example having a thickness between about 1000 to 2000 Angstroms, may formed on the top surface of semiconductor substrate **202**, via low pressure chemical vapor deposition (LPCVD), or plasma enhanced chemical vapor deposition (PECVD) procedures, for example. Conventional photolithographic and reactive ion etching (RIE) procedures may be used to define shallow trench shapes, through the silicon nitride layer, and to a depth between about 3000 to 6000 Angstroms in semiconductor substrate **202**. The RIE procedure may be performed using Cl_2 as an etchant for both the silicon nitride layer and the semiconductor substrate. After removal of the photoresist shape used to define shallow trench shapes, via plasma oxygen ashing procedures, for example, a silicon oxide layer may be deposited via LPCVD or PECVD procedures at a thickness between about 4000 to 10000 Angstroms, using tetraethylorthosilicate (TEOS) as a source, to completely fill the shallow trench shapes. A chemical mechanical polishing (CMP) procedure may then be employed to remove portions of the silicon oxide layer from the top surface, resulting in silicon oxide filled, STI regions, or isolation features **204**.

[0041] FIG. **2**B illustrates the formation of substrate buffer or fin substrate buffer regions **203** between isolation features **204**, such as by an ion implantation or doping process **205**. The formation of substrate buffer regions may be accomplished utilizing a photoresist shape (not shown in the drawings), to block a portion of the semiconductor substrate from an ion implantation procedure performed using p-type dopants or n-type dopants, as desired to fabricate PMOS and/or NMOS regions. P-type dopants, such as boron ions, may be applied at an energy between about 20 to 400 KeV, and at a dose between about 1e12 and about 1e14 atoms/cm^2. In other cases, or in additional fabrication areas, n-type implantation, such as arsenic or phosphorous ions, may be performed at an energy between about 20 to about 500 KeV, at a dose between about 1e12 to about 1e14 atoms/cm^2. If not previously performed, threshold adjust and anti-punch through implants may also be performed. Additional ion implantation procedures can be used. Removal of the photoresist block out shapes may be accomplished via plasma oxygen ashing procedures.

[0042] In yet another example, substrate buffer region **203** may be doped with p-type dopants at levels ranging between about 1e17 cm^{-3} and about 1e-19 cm^{-3}, and in one example is a silicon buffer region doped at 1e18 cm^{-3}.

[0043] In yet another example, a substrate buffer region may be formed by removing a portion of the silicon substrate and epitaxially regrowing an in-situ doped layer.

[0044] FIG. **2**C illustrates a plurality of fin substrates **206** (e.g., strained silicon germanium (SiGe) channel layers) disposed above the substrate **202** and between at least two isolation features **204**. In one example, fin substrates **206** are further disposed above substrate buffer regions **203** and at a vertical level above the at least two isolation features **204**. In one aspect, fin substrates **206** are formed at a vertical level substantially completely above the at least two isolation features. In another aspect, fin substrate **206** may be formed to have a portion at a vertical level above the at least two isolation features. In another example, the fin substrate **206** is formed as a strained SiGe channel layer comprised of between about 25% Ge and about 50% Ge, having a length between about 100 nm and about 200 nm, a width between about 10 nm and about 20 nm, and a thickness between about 10 nm and about 40 nm. In yet another example, the fin substrate **206** is a strained SiGe channel layer comprised of about 50% Ge, having a length of about 100 nm, a width of about 10 nm, and a height above the at least two isolation features of about 10 nm.

[0045] In one aspect of the present disclosure, fin substrates **206** may be formed by a SiGe or Ge condensation technique or epitaxially grown, as disclosed in U.S. application Ser. No. 11/861,931, the entire disclosure of which is incorporated by reference herein. For example, fin substrates **206** may be formed by selective epitaxial growth in any suitable epitaxial deposition system and process, such as metal-organic chemical vapor deposition (MOCVD), atmospheric pressure CVD (APCVD), low- (or reduced-) pressure CVD (LPCVD), ultra-high vacuum CVD (UHCVD), molecular beam epitaxy (MBE), or atomic layer deposition (ALD). In a CVD process, selective epitaxial growth typically includes introducing a source gas into a chamber. The source gas may include at least one precursor gas and a carrier gas. The reactor chamber may be heated by, for example, RF-heating, and the growth temperature in the chamber may range from about 300 degrees Celsius to about 900 degrees Celsius, depending on the composition of the crystalline material of the fin substrate to be formed. The epitaxial growth system may be a single-wafer or multiple-wafer batch or inline reactor.

[0046] FIG. **2**D illustrates the formation of a gate **208** formed in a perpendicular direction to the channel layers **206**, although gate **208** is not limited to this particular direction. In one example, gate **208** is formed directly over fin substrates **206** and isolation features **204**. In other examples, as will be disclosed with respect to FIGS. **7**A-**7**D, gate **208** may be formed over a prior grown epitaxial layer. Thus, gate **208** may be formed over a top surface and sidewalls of fin substrate **206** (see e.g., FIGS. **2**D and **3**A) or over a top surface and sidewalls of a prior grown epitaxial layer (see e.g., FIG. **7**D).

[0047] In one example, gate **208** may be formed by deposition and selective removal of a gate dielectric material and a conductive gate material. The gate dielectric material may include SiO_2, Si_3N_4, HfO_2, HfSiON, and/or HfSiO. The conductive gate material may include polysilicon, amorphous Si, Ge or SiGe gate material, and/or a metal or metal alloy.

[0048] Referring now to FIGS. **3**A-**3**C, closer perspective cross-sectional views of device **200** are illustrated at various stages of fabrication in accordance with an embodiment of the present disclosure.

[0049] FIG. **3**A illustrates a closer view of device **200** with a single fin substrate **206** and substrate buffer region **203** between two isolation features **204**. In one example, fin substrate **206** is deposited as a strained channel layer having a compressive uni-axial strain when forming a PMOS device, and having a tensile uni-axial strain when forming an NMOS device. As noted above, fin substrate **206** may be comprised of silicon (Si), germanium (Ge), a combination of Si and Ge, Group III-V compounds, or combinations thereof. In one example, fin substrate **206** comprises a strained SiGe channel layer in which a transversal stress component is fully relaxed due to the fin dimensions (e.g., in the width direction, the strain is relaxed because the width of the fin is relatively small as compared to the fin length or longitudinal direction), leading to a uniaxial stress in the channel length or longitudinal direction.

[0050] After a pre-clean procedure performed using a dilute or buffered hydrofluoric acid solution, for example, the fin substrate **206** may be selectively grown on exposed semiconductor surfaces above substrate buffer regions **203**. Various deposition processes may be used. In one example, an ultra-high vacuum chemical vapor deposition (UHV-CVD) procedure may be employed. The addition of chlorine gas or HCl gas may enhance the selectivity of the epitaxial growth. The growth of the fin substrate **206** may be selectively deposited using silane (SiH_4) or disilane (Si_2H_6), and germane (GeH_4) or digermane as reactants. In one example, a strained SiGe layer may be achieved using a germanium weight percent between about 25% to about 50%. The thickness is chosen to be sufficient enough to contain the inversion charge, however not thick enough to allow defect to lead to unwanted device leakage.

[0051] In another embodiment, the fin substrate **206** may be formed by growing a non-selective layer and subsequently using a patterning procedure to remove portions of the non-selective channel layers from non-active device regions, such as from the top surface of isolation features **204**.

[0052] In one example, an undoped polysilicon layer may next be deposited (e.g., via LPCVD procedures), and conventional photolithographic and anisotropic RIE procedures (e.g., using Cl_2 or SF_6 as an etchant) may be used to define polysilicon gate structure **208**. The photoresist shape, (not shown in the drawings), used as a defining mask for the polysilicon gate structures, may be removed via plasma oxygen ashing procedures and careful wet cleans.

[0053] A silicon nitride layer may then be deposited via LPCVD or PECVD procedures, and an anisotropic RIE procedure using SF_6 as an etchant may be used to define silicon nitride spacers **230** on the sides of the polysilicon gate structures, as shown in FIG. **5**.

[0054] FIG. **3**B illustrates an anisotropic etch **210** of the isolation features **204**, such as an anisotropic etch of a field oxide of shallow trench isolation features. Etch **210** forms a recess **212** within the isolation features **204**. Various etch techniques, such as dry and/or wet etch techniques may be used to etch the isolation features **204**. In one example, an oxide etcher with a fluorinated etchant gas may be used in conjunction with a patterned photoresist. In another example, an anisotropic RIE procedure (e.g., using Cl_2 or SF_6 as an etchant) may be used.

[0055] FIG. **3**C then illustrates the formation of an epitaxial layer **220** disposed over exposed portions of fin substrate **206**, such a strained SiGe channel layer. In one example, epitaxial layer **220** is formed over top and sidewall surfaces of fin substrate **206**, and in another example, substantially covers all exposed portions of the fin substrate **206**. In one example, epitaxial layer **220** may be comprised of silicon and may be selectively deposited by epitaxial growth using silane (SiH_4) or disilane (Si_2H_6). In another example, epitaxial layer **220** may function as source and drain regions of device **200**. In this embodiment, gate **208** is previously formed directly over fin substrate **206** and epitaxial layer **220** is subsequently formed over exposed portions of fin substrate **206**, including sidewalls and a top surface of fin substrate **206**. In other embodiments, as noted above, an epitaxial layer may be formed prior to formation of gate **208** and thus, gate **208** may be formed over a prior formed epitaxial layer.

[0056] In one example, epitaxial layer **220** may be formed by selective epitaxial growth in any suitable epitaxial deposition system and process, such as metal-organic chemical vapor deposition (MOCVD), atmospheric pressure CVD (APCVD), low- (or reduced-) pressure CVD (LPCVD), ultra-high vacuum CVD (UHCVD), molecular beam epitaxy (MBE), or atomic layer deposition (ALD). In a CVD process, selective epitaxial growth typically includes introducing a source gas into a chamber. The source gas may include at least one precursor gas and a carrier gas. The reactor chamber may be heated by, for example, RF-heating, and the growth temperature in the chamber may range from about 300 degrees Celsius to about 900 degrees Celsius, depending on the composition of the crystalline material of the epitaxial layer to be formed. The epitaxial growth system may be a single-wafer or multiple-wafer batch or inline reactor.

[0057] Advantageously, the epitaxial layer **220** counterbalances relaxation of the longitudinal stress component in the lengthwise direction of the fin substrate **206**, thus providing for improved transistor performance.

[0058] Referring now to FIGS. **4**A and **4**B, different embodiments are illustrated of cross-sectional views of semiconductor device **200** of FIG. **3**B along a line A-A' in accordance with embodiments of the present disclosure. FIGS. **4**A and **4**B illustrate dimensions of fin substrate **206** above substrate buffer layer **203**, including a fin width denoted by W_{finn}, a fin height above the etched isolation feature **204** denoted by H_{fin}, and a fin thickness denoted by T_{SiGe}. FIG. **3**B illustrates a fin length denoted by L_{fin}.

[0059] In one example, the fin substrate **206** is a strained SiGe channel layer comprised of between about 25% Ge and about 50% Ge, and has a fin length L_{fin} between about 100 nm and about 200 nm, a fin width W_{fin} between about 10 nm and about 20 nm, and a fin thickness T_{SiGe} between about 10 nm and about 40 nm.

[0060] Referring now to FIG. **5**, a perspective cross-sectional view is illustrated of the semiconductor device **200** of FIG. **3**C along a line B-B' in accordance with embodiments of the present disclosure. It is noted that FIG. **5** does not show gate **208**. Device **200** includes epitaxial layer **220** disposed over exposed portions of fin substrate **206** (e.g., ends of the strained SiGe channel layer. In one example, the gate electrode **208** has a width (i.e., along the longitudinal axis of the fin substrate **206**) of about 20 nm and the spacers **230** each have a length of about 15 nm.

[0061] In one example, as illustrated in FIGS. **4**B and **5**, the strained SiGe channel layer is comprised of about 50% Ge, and has a fin length L_{fin} of about 100 nm, a fin width W_{fin} of about 10 nm, and a fin height above the at least two isolation features H_{fin} of about 10 nm. An average uni-axial compressive stress level of the SiGe channel layer **206** has been modeled to be greater than about 3 GPa.

[0062] As illustrated in one embodiment of FIGS. **4**B and **5**, a strained fin substrate **206** (e.g., a silicon germanium (SiGe) channel layer) is disposed above the substrate buffer region **203**, between the at least two isolation features **204**, and at a vertical level substantially completely above the at least two isolation features **204**. For example, according to one aspect of the present disclosure, FIG. **4**A illustrates a portion of fin substrate **206** above the at least two isolation features **204**, and according to another aspect of the present disclosure, FIG. **4**B illustrates the fin substrate **206** substantially completely above the at least two isolation features **204**. In one example, FIGS. **4**B and **5** further illustrate fin height above the etched isolation feature **204** denoted by H_{fin} substantially equal to fin thickness denoted by T_{SiGe}.

[0063] In one example, the epitaxial layer **220** (e.g., source drain regions) is deposited to cover exposed surfaces of the fin substrate **206** (e.g., a strained SiGe channel layer), and in another example, epitaxial layer **220** is deposited to cover exposed surfaces of the strained SiGe channel layer **206** not masked by gate **208** and/or spacers **230**, including sidewalls and top surfaces of the fin substrate **206**. In yet another example, portions of the epitaxial layer **220** are deposited over portions of the etched isolation features **204** (e.g., etched oxide of the isolation feature). In yet another example, epitaxial layer **220** is comprised of the same material as the substrate, and in one example is comprised of silicon.

[0064] Recessing the isolation features provide a topography or template for epitaxial deposition of the epitaxial layer **220**. For the case the epitaxial layer **220** is comprised of silicon, the inventors believe the SiGe channel will adapt to the silicon lattice structure and counterbalance relaxation of the longitudinal stress component. Advantageously, the epitaxial layer **220** optimizes transistor performance by counteracting relaxation of the longitudinal stress component of the fin substrate **206**.

[0065] Referring now to FIG. **6**, a perspective cross-sectional view is illustrated of semiconductor device **300** in accordance with another embodiment of the present disclosure. Device **300** includes a substrate **202**, a plurality of (and at least two) isolation features **204**, and a plurality of fin substrates **206** (e.g., strained silicon germanium (SiGe) channel layers) disposed above the substrate **202** and between at least two isolation features **204**, and at a vertical level above the at least two isolation features **204**. A gate **208** is formed across the fin substrates **206**. Similarly numbered features in device **200** (such as the substrate **202**, isolation features **204**, fin substrate **206**, and gate **208**) are fully applicable in this embodiment with respect to device **300** although descriptions may not be repeated here to avoid repetitive descriptions. In this embodiment, device **300** further includes a germanium substrate **302** above which is formed respective SiGe channel layers for forming NMOS devices.

[0066] Referring now to FIGS. **7**A-**7**D, perspective cross-sectional views are illustrated of another semiconductor device **400** at various stages of fabrication in accordance with an embodiment of the present disclosure.

[0067] FIG. **7**A illustrates semiconductor device **400** including a substrate **402**, at least two isolation features **204**, and a fin substrate **404**, **406** between the at least two isolation

features **204**. Substrate **402** and isolation features **204** are substantially similar to substrate **202** and isolation features **204** described above with respect to device **200** (FIGS. **2**A-**5**) and the descriptions of substrate **202** and isolation features **204** above are fully applicable in this embodiment although related description may not be included below to avoid repetitive descriptions. In one example, the fin substrate includes a first fin substrate **404** above substrate **402**, and a second fin substrate **406** above first fin substrate **404**. Fin substrates **404**, **406** are between isolation features **204**. Substrate **402** is comprised of a first semiconductor material, first fin substrate **404** is comprised of a second semiconductor material, and second fin substrate **406** is comprised of a third semiconductor material, and in one example substrate **402**, first fin substrate **404**, and second fin substrate **406** may each be comprised of silicon (Si), germanium (Ge), or a combination of Si and Ge.

[0068] In one embodiment, a dielectric material of isolation features **204** may be formed over substrate **402**, and then a trench may be defined in the dielectric layer, extending to a top surface of substrate **402**. Crystalline material of first fin substrate **404** and second fin substrate **406** is then formed within the trench by any suitable process, such as by a SiGe or Ge condensation technique or epitaxially grown, as disclosed in U.S. application Ser. No. 11/861,931, the entire disclosure of which has been incorporated by reference herein.

[0069] FIG. **7**B illustrates an etch of the isolation features **204** to expose sidewalls of fin substrate **406**. Various etch techniques, such as dry and/or wet etch techniques may be used to etch the isolation features **204**. In one example, an oxide etcher with a fluorinated etchant gas may be used in conjunction with a patterned photoresist. In another example, an anisotropic RIE procedure (e.g., using Cl_2 or SF_6 as an etchant) may be used.

[0070] FIG. **7**C illustrates the formation of an epitaxial layer **408** disposed over exposed portions of fin substrate **406**, such as over top surfaces and sidewalls of fin substrate **406**. In one example, epitaxial layer **408** substantially covers all exposed portions of the fin substrate **406**. Epitaxial layer **408** is comprised of a fourth semiconductor material and in one example may be comprised of silicon (Si), germanium (Ge), or a combination of Si and Ge.

[0071] According to one aspect of the present disclosure, epitaxial layer **408** may be formed by selective epitaxial growth in any suitable epitaxial deposition system and process, such as metal-organic chemical vapor deposition (MOCVD), atmospheric pressure CVD (APCVD), low- (or reduced-) pressure CVD (LPCVD), ultra-high vacuum CVD (UHCVD), molecular beam epitaxy (MBE), or atomic layer deposition (ALD). In a CVD process, selective epitaxial growth typically includes introducing a source gas into a chamber. The source gas may include at least one precursor gas and a carrier gas. The reactor chamber may be heated by, for example, RF-heating, and the growth temperature in the chamber may range from about 300 degrees Celsius to about 900 degrees Celsius, depending on the composition of the crystalline material of the epitaxial layer to be formed. The epitaxial growth system may be a single-wafer or multiple-wafer batch or inline reactor.

[0072] FIG. **7**D illustrates the formation of gate **410** over epitaxial layer **408**. In this embodiment, gate **410** is formed directly over epitaxial layer **408**, including sidewalls and a top surface of epitaxial layer **408**, and epitaxial layer **408** may function as a strained channel layer. Gate **410** may be substantially similar to gate **208** described above with respect to FIGS. **2**D-**3**C and the descriptions of gate **208** above are fully applicable in this embodiment although related description may not be included below to avoid repetitive descriptions.

[0073] Referring now to FIGS. **8**A-**8**G, **9**A-**9**G, and **10**A-**10**G, cross-sectional views are illustrated of the semiconductor device **400** of FIG. **7**D along a line C-C' in accordance with embodiments of the present disclosure. As noted above, the substrate **402**, the fin substrate **404**, **406**, and the epitaxial layer **408** are comprised of a first semiconductor material, a second semiconductor material, a third semiconductor material, and a fourth semiconductor material, respectively, and the first, second, third, and fourth semiconductor materials may be the same or different, and the first, second, third, and fourth semiconductor materials may have the same or different lattice constants. In one example, the substrate **402**, the fin substrate **404**, **406**, and the epitaxial layer **408** may each be comprised of silicon (Si), germanium (Ge), a combination of Si and Ge, Group III-V materials (e.g., InGaAs, InAs, GaSb, InGaSb, AlAsSb), or combinations thereof. FIGS. **8**A-**8**G, **9**A-**9**G, and **10**A-**10**G illustrate different permutations of Si, Ge, and SiGe materials for the fin substrate and the epitaxial layer in accordance with Tables 1, 2, and 3, respectively, below. In Tables 1, 2, and 3, the "r" prefix stands for "relaxed", the "c" prefix stands for "compressive strain", and the "t" prefix stands for "tensile strain".

TABLE 1

		Si fin	SiGe fin		Ge fin	Hybrid		
		FIG. 8A	FIG. 8B	FIG. 8C	FIG. 8D	FIG. 8E	FIG. 8F	FIG. 8G
NMOS	fin	Si	r-SiGe	r-SiGe	r-Ge	r-SiGe	r-Ge	r-Ge
	epi channel	—	t-Si	—	t-SiGe	t-Si	t-SiGe	t-SiGe
	μ (intrinsic)	—	—	increased	increased	—	increased	increased
	μ (strain)	—	increased	—	increased	increased	increased	increased
PMOS	fin	Si	r-SiGe	r-SiGe	r-Ge	Si	Si	r-SiGe
	epi channel	c-SiGe	—	c-Ge	—	c-SiGe	c-SiGe	c-Ge
	μ (intrinsic)	increased	increased	increased	increased	increased	increased	increased
	μ (strain)	increased	—	increased	—	increased	increased	increased

TABLE 2

		Si fin	SiGe fin		Ge fin	Hybrid		
		FIG. 9A	FIG. 9B	FIG. 9C	FIG. 9D	FIG. 9E	FIG. 9F	FIG. 9G
NMOS	fin	Si	r-SiGe	r-SiGe	r-Ge	r-SiGe	r-Ge	r-Ge
	epi channel	—	t-Si	—	t-SiGe	t-Si	t-SiGe	t-SiGe
	μ (intrinsic)	—	—	increased	increased	—	increased	increased
	μ (strain)	—	increased	—	increased	increased	increased	increased
PMOS	fin	Si	r-SiGe	r-SiGe	r-Ge	Si	Si	r-SiGe
	epi channel	c-SiGe	—	c-Ge	—	c-SiGe	c-SiGe	c-Ge
	μ (intrinsic)	increased	increased	increased	increased	increased	increased	increased
	μ (strain)	increased	—	increased	—	increased	increased	increased

TABLE 3

		Si fin	SiGe fin		Ge fin	Hybrid		
		FIG. 10A	FIG. 10B	FIG. 10C	FIG. 10D	FIG. 10E	FIG. 10F	FIG. 10G
NMOS	fin	Si	r-SiGe	r-SiGe	r-Ge	r-SiGe	r-Ge	r-Ge
	epi channel	—	t-Si	—	t-SiGe	t-Si	t-SiGe	t-SiGe
	Si cap	N	N	N	Y	N	Y	Y
	μ (intrinsic)	—	—	increased	increased	—	increased	increased
	μ (strain)	—	increased	—	increased	increased	increased	increased
PMOS	fin	Si	r-SiGe	r-SiGe	r-Ge	Si	Si	r-SiGe
	epi channel	c-SiGe	—	c-Ge	—	c-SiGe	c-SiGe	c-Ge
	Si cap	Y	Y	Y	Y	Y	Y	Y
	μ (intrinsic)	increased	increased	increased	increased	increased	increased	increased
	μ (strain)	increased	—	increased	—	increased	increased	increased

[0074] FIG. **8**A illustrates an NMOS device and a PMOS device each having substrate **402***a*, first fin substrate **404***a*, and second fin substrate **406***a*. Substrate **402**, first fin substrate **404***a*, and second fin substrate **406***a* are each comprised of silicon. The PMOS device further includes epitaxial layer **408***a* comprised of SiGe and having a compressive uni-axial strain. Epitaxial layer **408***a* is formed over a top surface and sidewalls of fin substrate **406***a*. Intrinsic carrier mobility as compared to Si (μ(intrinsic)) and strain (μ(strain)) in the epitaxial layer **408***a* of the PMOS device is increased. The strain has an additive effect on the carrier mobility in the epitaxial layer.

[0075] FIG. **8**B illustrates an NMOS device and a PMOS device each having substrate **402***a*, first fin substrate **404***a*, and second fin substrate **406***b*. Substrate **402** and first fin substrate **404***a* are each comprised of silicon, and second fin substrate **406***b* is comprised of relaxed SiGe. The NMOS device further includes epitaxial layer **408***b* comprised of Si and having a tensile uni-axial strain. Epitaxial layer **408***b* is formed over a top surface and sidewalls of fin substrate **406***b*. Strain μ(strain) in epitaxial layer **408***b* of the NMOS device is increased, and intrinsic carrier mobility μ(intrinsic) in fin substrate **406***b* of the PMOS device is increased.

[0076] FIG. **8**C illustrates an NMOS device and a PMOS device each having substrate **402***a*, first fin substrate **404***a*, and second fin substrate **406***b*. Substrate **402** and first fin substrate **404***a* are each comprised of silicon, and second fin substrate **406***b* is comprised of relaxed SiGe. The PMOS device further includes epitaxial layer **408***c* comprised of Ge and having a compressive uni-axial strain. Epitaxial layer **408***c* is formed over a top surface and sidewalls of fin substrate **406***b*. Intrinsic carrier mobility μ(intrinsic) in the fin substrate **406***b* of the NMOS device is increased, and both intrinsic carrier mobility and strain μ(strain) in the epitaxial layer **408***c* of the PMOS device is increased.

[0077] FIG. **8**D illustrates an NMOS device and a PMOS device each having substrate **402***a*, first fin substrate **404***a*, and second fin substrate **406***c*. Substrate **402** and first fin substrate **404***a* are each comprised of silicon, and second fin substrate **406***c* is comprised of relaxed Ge. The NMOS device further includes epitaxial layer **408***d* comprised of SiGe and having a tensile uni-axial strain. Epitaxial layer **408***d* is formed over a top surface and sidewalls of fin substrate **406***c*. Both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in the epitaxial layer **408***d* of the NMOS device is increased, and intrinsic carrier mobility μ(intrinsic) in the fin substrate **406***c* of the PMOS device is increased.

[0078] FIG. **8**E illustrates an NMOS device and a PMOS device each having substrate **402***a* and first fin substrate **404***a*. The NMOS device further includes second fin substrate **406***b* and the PMOS device further includes second fin substrate **406***a*. Substrate **402** and first fin substrate **404***a* are each comprised of silicon, second fin substrate **406***b* is comprised of relaxed SiGe, and second fin substrate **406***a* is comprised of silicon. The NMOS device further includes epitaxial layer **408***b* comprised of Si and having a tensile uni-axial strain, and the PMOS device further includes epitaxial layer **408***a* comprised of SiGe and having a compressive uni-axial strain. Epitaxial layers **408***b* and **408***a* are formed over a top surface and sidewalls of fin substrates **406***b* and **406***a*, respectively. Strain μ(strain) in the epitaxial layer **408***b* of the NMOS device is increased, and both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in the epitaxial layer **408***a* of the PMOS device is increased.

[0079] FIG. **8**F illustrates an NMOS device and a PMOS device each having substrate **402***a* and first fin substrate **404***a*. The NMOS device further includes second fin substrate **406***c*

and the PMOS device further includes second fin substrate **406***a*. Substrate **402** and first fin substrate **404***a* are each comprised of silicon, second fin substrate **406***c* is comprised of relaxed Ge, and second fin substrate **406***a* is comprised of silicon. The NMOS device further includes epitaxial layer **408***d* comprised of SiGe and having a tensile uni-axial strain, and the PMOS device further includes epitaxial layer **408***a* comprised of SiGe and having a compressive uni-axial strain. Epitaxial layers **408***d* and **408***a* are formed over a top surface and sidewalls of fin substrates **406***c* and **406***a*, respectively. Both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in the epitaxial layer **408***d* of the NMOS device is increased, and both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in the epitaxial layer **408***a* of the PMOS device is increased.

[0080] FIG. **8**G illustrates an NMOS device and a PMOS device each having substrate **402***a* and first fin substrate **404***a*. The NMOS device further includes second fin substrate **406***c* and the PMOS device further includes second fin substrate **406***b*. Substrate **402** and first fin substrate **404***a* are each comprised of silicon, second fin substrate **406***c* is comprised of relaxed Ge, and second fin substrate **406***b* is comprised of relaxed SiGe. The NMOS device further includes epitaxial layer **408***d* comprised of SiGe and having a tensile uni-axial strain, and the PMOS device further includes epitaxial layer **408***c* comprised of Ge and having a compressive uni-axial strain. Epitaxial layers **408***d* and **408***c* are formed over a top surface and sidewalls of fin substrates **406***c* and **406***b*, respectively. Both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in the epitaxial layer **408***d* of the NMOS device is increased, and both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in the epitaxial layer **408***c* of the PMOS device is increased.

[0081] FIG. **9**A illustrates an NMOS device and a PMOS device each having substrate **402***a* and first fin substrate **404***a*. The NMOS device further includes second fin substrate **406***a* and the PMOS device further includes second fin substrate **406***d*. Substrate **402**, first fin substrate **404***a*, and second fin substrate **406***a* are each comprised of silicon. Second fin substrate **406***d* is comprised of SiGe and has a compressive uni-axial strain. Both intrinsic carrier mobility as compared to Si (μ(intrinsic)) and strain (μ(strain)) in second fin substrate **406***d* of the PMOS device is increased.

[0082] FIG. **9**B illustrates an NMOS device including substrate **402***a*, first fin substrate **404***b*, and second fin substrate **406***a*, and a PMOS device including substrate **402***a*, first fin substrate **404***b*, and second fin substrate **406***b*. Substrate **402***a* is comprised of silicon, first fin substrate **404***b* and second fin substrate **406***b* are each comprised of relaxed SiGe, and second fin substrate **406***a* is comprised of silicon and has a tensile uni-axial strain. Strain μ(strain) in the second fin substrate **406***a* of the NMOS device is increased, and intrinsic carrier mobility μ(intrinsic) in second fin substrate **406***b* of the PMOS device is increased.

[0083] FIG. **9**C illustrates an NMOS device including substrate **402***a*, first fin substrate **404***b*, and second fin substrate **406***b*, and a PMOS device including substrate **402***a*, first fin substrate **404***b*, and second fin substrate **406***e*. Substrate **402***a* is comprised of silicon, first fin substrate **404***b* and second fin substrate **406***b* are each comprised of relaxed SiGe, and second fin substrate **406***e* is comprised of Ge and has a compressive uni-axial strain. Intrinsic carrier mobility μ(intrinsic) in the second fin substrate **406***b* of the NMOS device is increased, and both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in second fin substrate **406***e* of the PMOS device is increased.

[0084] FIG. **9**D illustrates an NMOS device including substrate **402***a*, first fin substrate **404***c*, and second fin substrate **406***f*, and a PMOS device including substrate **402***a*, first fin substrate **404***c*, and second fin substrate **406***c*. Substrate **402***a* is comprised of silicon, first fin substrate **404***c* and second fin substrate **406***c* are each comprised of relaxed Ge, and second fin substrate **406***f* is comprised of SiGe and has a tensile uni-axial strain. Both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in the second fin substrate **406***f* of the NMOS device is increased, and intrinsic carrier mobility μ(intrinsic) in second fin substrate **406***c* of the PMOS device is increased.

[0085] FIG. **9**E illustrates an NMOS device including substrate **402***a*, first fin substrate **404***b*, and second fin substrate **406***b*, and a PMOS device including substrate **402***a*, first fin substrate **404***a*, and second fin substrate **406***d*. Substrate **402***a* and first fin substrate **404***a* are each comprised of silicon, first fin substrate **404***b* and second fin substrate **406***b* are each comprised of relaxed SiGe, and second fin substrate **406***d* is comprised of SiGe and has a compressive uni-axial strain. Strain μ(strain) in the second fin substrate **406***b* of the NMOS device is increased, and both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in second fin substrate **406***d* of the PMOS device is increased.

[0086] FIG. **9**F illustrates an NMOS device including substrate **402***a*, first fin substrate **404***c*, and second fin substrate **406***f*, and a PMOS device including substrate **402***a*, first fin substrate **404***a*, and second fin substrate **406***d*. Substrate **402***a* and first fin substrate **404***a* are each comprised of silicon, first fin substrate **404***c* is comprised of relaxed Ge, second fin substrate **406***f* is comprised of SiGe having a tensile uni-axial strain, and second fin substrate **406***d* is comprised of SiGe having a compressive uni-axial strain. Both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in the second fin substrate **406***f* of the NMOS device is increased, and both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in second fin substrate **406***d* of the PMOS device is increased.

[0087] FIG. **9**G illustrates an NMOS device including substrate **402***a*, first fin substrate **404***c*, and second fin substrate **406***f*, and a PMOS device including substrate **402***a*, first fin substrate **404***b*, and second fin substrate **406***e*. Substrate **402***a* is comprised of silicon, first fin substrate **404***c* is comprised of relaxed Ge, first fin substrate **404***b* is comprised of relaxed SiGe, second fin substrate **406***f* is comprised of SiGe having a tensile uni-axial strain, and second fin substrate **406***e* is comprised of Ge having a compressive uni-axial strain. Both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in the second fin substrate **406***f* of the NMOS device is increased, and both intrinsic carrier mobility μ(intrinsic) and strain μ(strain) in second fin substrate **406***e* of the PMOS device is increased.

[0088] FIGS. **10**A-**10**G illustrate the NMOS and PMOS devices of FIGS. **9**A-**9**G, respectively, including a silicon passivation layer **409** epitaxially grown on exposed surfaces of a second fin substrate that is not comprised of silicon. Silicon passivation may improve the channel/dielectric interface by reducing the interface trap density.

[0089] FIG. **10**A illustrates silicon passivation layer **409** formed over second fin substrate **406***d* comprised of SiGe having a compressive uni-axial strain. FIG. **10**B illustrates silicon passivation layer **409** formed over second fin substrate

406*b* comprised of relaxed SiGe. FIG. **10**C illustrates silicon passivation layer **409** formed over second fin substrate **406***b* comprised of relaxed SiGe and over second fin substrate **406***e* comprised of Ge having a compressive uni-axial strain. FIG. **10**D illustrates silicon passivation layer **409** formed over second fin substrate **406***f* comprised of SiGe having a tensile uni-axial strain and over second fin substrate **406***c* comprised of relaxed Ge. FIG. **10**E illustrates silicon passivation layer **409** formed over second fin substrate **406***b* comprised of relaxed SiGe and over second fin substrate **406***d* comprised of SiGe having a compressive uni-axial strain. FIG. **10**F illustrates silicon passivation layer **409** formed over second fin substrate **406***f* comprised of SiGe having a tensile uni-axial strain and over second fin substrate **406***d* comprised of SiGe having a compressive uni-axial strain. FIG. **10**G illustrates silicon passivation layer **409** formed over second fin substrate **406***f* comprised of SiGe having a tensile uni-axial strain and over second fin substrate **406***e* comprised of Ge having a compressive uni-axial strain.

[0090] Thus, strained SiGe, Ge, or Si channel layers (e.g., epitaxial layer **408**) may be epitaxially grown on relaxed SiGe, Ge, or Si fin substrates (e.g., fin substrate **406**) utilizing lattice mismatch of the channel layer material and the underlying fin substrate material. In the case of SiGe, Ge, or Si channels, materials are chosen such that the channel material will be tensile strained for the NMOS device and compressive strained for the PMOS device. It is noted that other combinations of materials for the NMOS and PMOS devices above are within the scope of the present disclosure (e.g., c-SiGe on Si for PMOS devices and t-Si on r-SiGe for NMOS devices).

[0091] Advantageously, the transistor devices and fabrication methods described above may be easily integrated with standard CMOS processes. Furthermore, the present disclosure allows for counteracting relaxation of the longitudinal stress component of the channel layer to provide high uni-axial compressive stress levels (e.g., greater than about 3 GPa), which optimizes transistor performance.

[0092] Thus, the present disclosure provides for various embodiments. In one embodiment, a semiconductor device is disclosed. A semiconductor device includes a substrate including at least two isolation features, a fin substrate disposed between and above the at least two isolation features, and an epitaxial layer disposed over exposed portions of the fin substrate. According to one aspect, the epitaxial layer may be disposed over a top surface and sidewalls of the fin substrate. According to another aspect, the fin substrate may be disposed substantially completely above the at least two isolation features.

[0093] In yet another embodiment, a semiconductor device includes a substrate including at least two isolation features, a substrate buffer region disposed between the at least two isolation features, and a fin substrate disposed above the substrate buffer region, between the at least two isolation features, and at a vertical level substantially completely above the at least two isolation features. The device further includes a source/drain epitaxial layer disposed over a top surface and sidewalls of the fin substrate.

[0094] The present disclosure also provides for a method of fabricating a semiconductor device. In one embodiment, the method includes providing a substrate including at least two isolation features, forming a fin substrate between the at least two isolation features, and at a vertical level above the at least two isolation features, and forming an epitaxial layer over exposed portions of the fin substrate. According to one aspect, the epitaxial layer may be deposited over a top surface and sidewalls of the fin substrate. According to another aspect, the fin substrate may be deposited substantially completely above the at least two isolation features.

[0095] Although embodiments of the present disclosure have been described in detail, those skilled in the art should understand that they may make various changes, substitutions and alterations herein without departing from the spirit and scope of the present disclosure. For example, other materials for the substrate, fin substrate, and epitaxial layers, such as Group III-V materials, are also within the scope of the present disclosure. Accordingly, all such changes, substitutions and alterations are intended to be included within the scope of the present disclosure as defined in the following claims. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents, but also equivalent structures.

What is claimed is:

1. A semiconductor device, comprising:
a substrate including at least two isolation features;
a fin substrate disposed between and above the at least two isolation features; and
an epitaxial layer disposed over exposed portions of the fin substrate.

2. The device of claim **1**, wherein each of the substrate, the fin substrate, and the epitaxial layer comprises silicon (Si), germanium (Ge), a combination of Si and Ge, Group III-V compounds, or combinations thereof.

3. The device of claim **1**, wherein the fin substrate or the epitaxial layer has a compressive uni-axial strain forming a PMOS device, or wherein the fin substrate or the epitaxial layer has a tensile uni-axial strain forming an NMOS device.

4. The device of claim **1**, wherein the fin substrate is disposed at a vertical level substantially completely above the at least two isolation features.

5. The device of claim **1**, wherein the epitaxial layer is disposed at a vertical level above etched regions of the at least two isolation features and over a top surface and sidewalls of the fin substrate.

6. The device of claim **1**, wherein the epitaxial layer is a passivation layer comprised of silicon.

7. The device of claim **1**, further comprising a fin substrate buffer region disposed below the fin substrate.

8. The device of claim **1**, further comprising a gate electrode disposed over the epitaxial layer or over the fin substrate.

9. A semiconductor device, comprising:
a substrate including at least two isolation features;
a substrate buffer region disposed between the at least two isolation features;
a fin substrate disposed above the substrate buffer region, between the at least two isolation features, and at a vertical level substantially completely above the at least two isolation features; and
a source/drain epitaxial layer disposed over a top surface and sidewalls of the fin substrate.

10. The device of claim **9**, wherein each of the substrate, the substrate buffer region, the fin substrate, and the epitaxial layer comprises silicon (Si), germanium (Ge), a combination of Si and Ge, Group III-V compounds, or combinations thereof.

11. The device of claim **9**, wherein the fin substrate is a strained SiGe channel layer comprised of between about 25%

Ge and about 50% Ge, having a length between about 100 nm and about 200 nm, a width between about 10 nm and about 20 nm, and a thickness between about 10 nm and about 40 nm.

12. The device of claim **9**, wherein the fin substrate is a strained SiGe channel layer comprised of about 50% Ge, having a length of about 100 nm, a width of about 10 nm, and a height above the at least two isolation features of about 10 nm.

13. The device of claim **9**, further comprising:

a gate electrode disposed above the strained SiGe channel layer; and

spacers disposed adjacent the sides of the gate electrode.

14. A method of fabricating a semiconductor device, the method comprising:

providing a substrate including at least two isolation features;

forming a fin substrate between the at least two isolation features, and at a vertical level above the at least two isolation features; and

forming an epitaxial layer over exposed portions of the fin substrate.

15. The method of claim **14**, wherein each of the substrate, the fin substrate, and the epitaxial layer comprises silicon (Si), germanium (Ge), a combination of Si and Ge, Group III-V compounds, or combinations thereof.

16. The method of claim **14**, wherein the fin substrate is deposited as a strained SiGe channel layer comprised of between about 25% Ge and about 50% Ge, having a length between about 100 nm and about 200 nm, a width between about 10 nm and about 20 nm, and a thickness between about 10 nm and about 40 nm.

17. The method of claim **14**, wherein the fin substrate or the epitaxial layer is deposited to have a compressive uni-axial strain forming a PMOS device, or wherein the fin substrate or the epitaxial layer is deposited to have a tensile uni-axial strain forming an NMOS device.

18. The method of claim **14**, wherein the epitaxial layer is formed at a vertical level above etched regions of the at least two isolation features and over a top surface and sidewalls of the fin substrate.

19. The method of claim **14**, wherein the epitaxial layer is deposited as a passivation layer comprised of silicon.

20. The method of claim **14**, further comprising:

forming a fin substrate buffer region below the fin substrate;

anisotropically etching the at least two isolation features; and

forming a gate electrode over the epitaxial layer or over the fin substrate.

* * * * *