US009570567B1

(12) **United States Patent**
Chang et al.

(10) **Patent No.: US 9,570,567 B1**
(45) **Date of Patent: Feb. 14, 2017**

(54) **SOURCE AND DRAIN PROCESS FOR FINFET**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/984,514**

(22) Filed: **Dec. 30, 2015**

(51) **Int. Cl.**

H01L 27/088	(2006.01)
H01L 29/417	(2006.01)
H01L 29/78	(2006.01)
H01L 29/66	(2006.01)
H01L 21/306	(2006.01)

(52) **U.S. Cl.**
CPC ... ***H01L 29/41791*** (2013.01); ***H01L 21/30604*** (2013.01); ***H01L 29/6656*** (2013.01); ***H01L 29/66545*** (2013.01); ***H01L 29/66795*** (2013.01); ***H01L 29/785*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 29/785; H01L 29/7841; H01L 29/66795; H01L 29/7851; H01L 29/0688; H01L 29/0649; H01L 29/0847; H01L 29/7848; H01L 29/165; H01L 29/66545
USPC 257/401; 438/283
See application file for complete search history.

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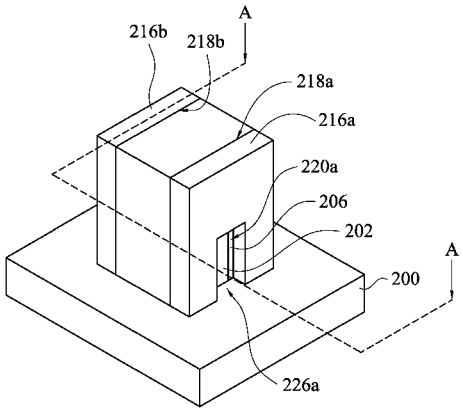
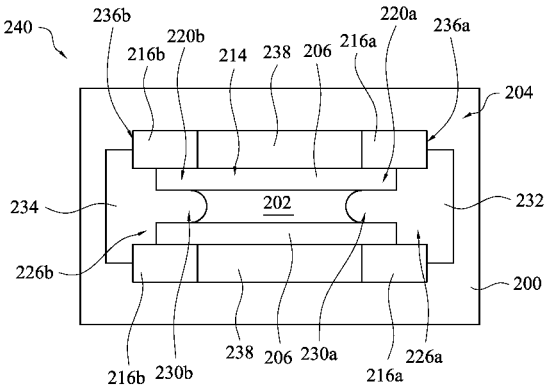
(57) **ABSTRACT**

A FinFET includes a substrate, a fin structure, a dielectric layer, a metal gate, two spacers, a source and a drain. The fin structure is disposed on the substrate. The dielectric layer is disposed on the fin structure and covers two opposite side surfaces of the fin structure. The dielectric layer includes two first portions protruding from the side surfaces of the fin structure, such that two opposite first recesses are formed in the dielectric layer. The metal gate is disposed on a second portion of the dielectric layer which is sandwiched between the first portions. The spacers are disposed on the first portions of the dielectric layer and protrude from the first portions of the dielectric layer respectively, such that two second recesses are formed in the spacers. The source and drain are respectively disposed in the first recesses and the second recesses on the substrate.

20 Claims, 10 Drawing Sheets





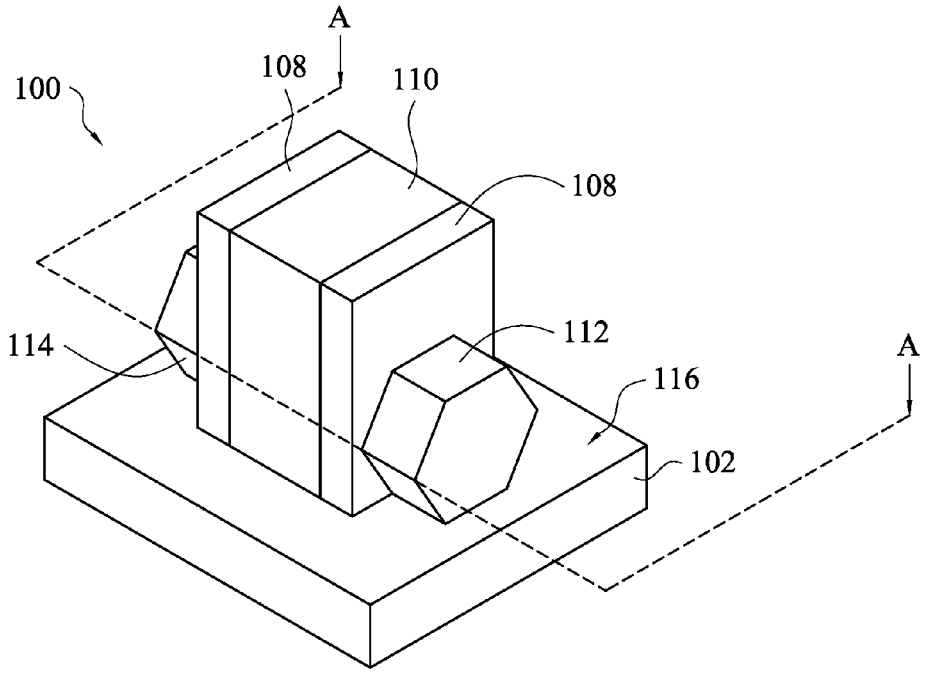
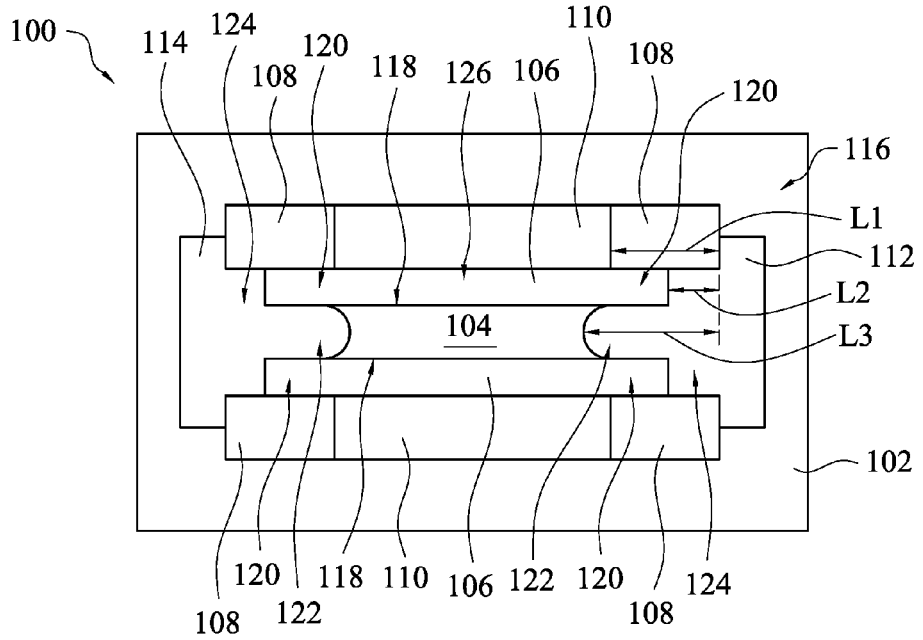

A
100
108
110
108
114
112
116
A
102

FIG. 1A


100
114
124
108
120
118
126
106
110
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120
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L1
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L3
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120
122
118
110
106
122
120
108
124

FIG. 1B

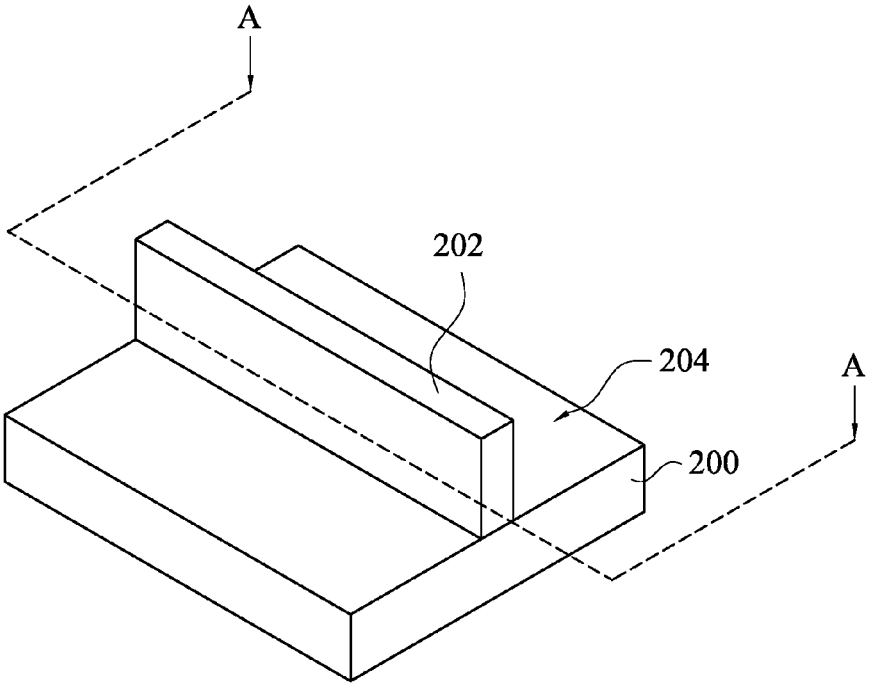


FIG. 2A

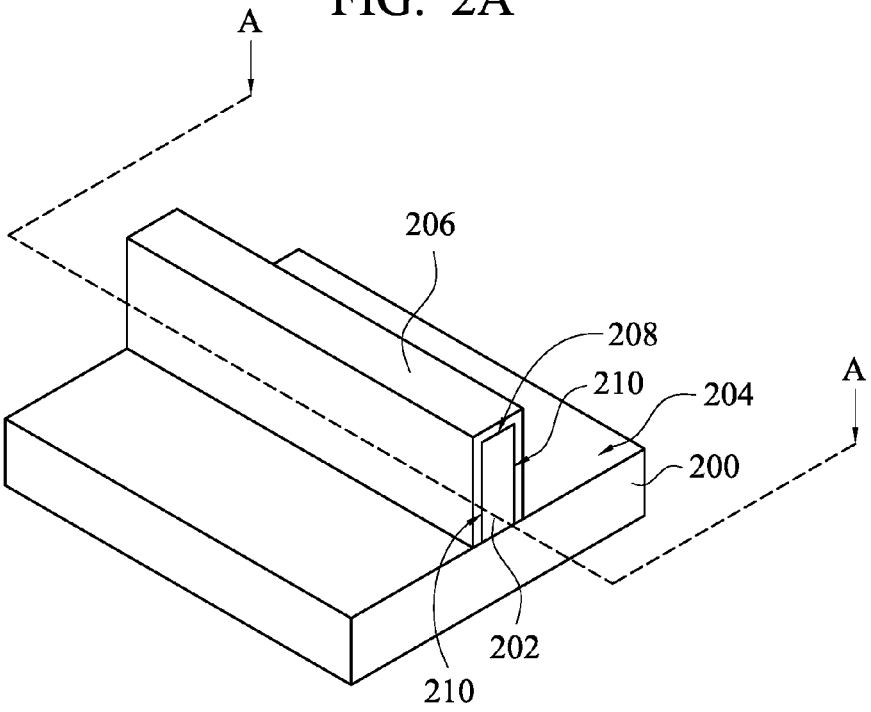


FIG. 2B

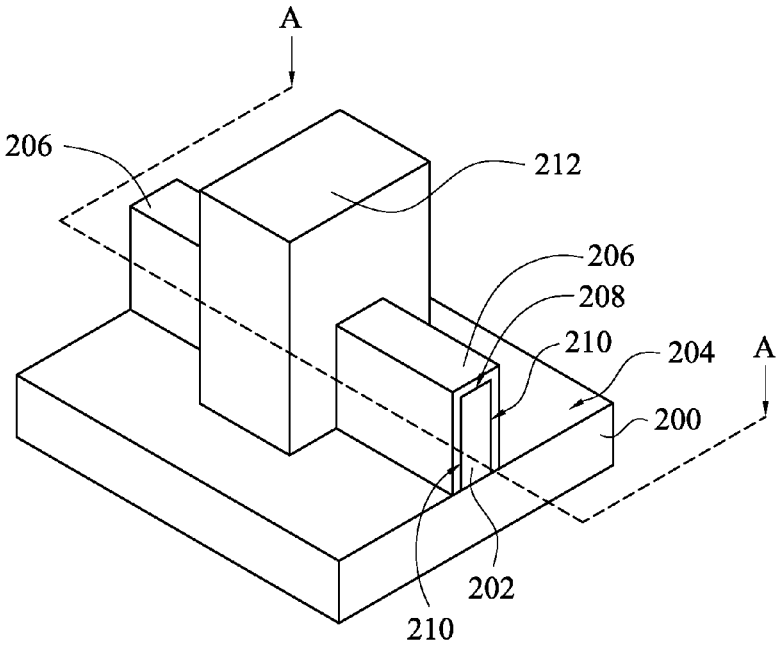

A
206
212
206
208
210
204
A
200
202
210

FIG. 2C

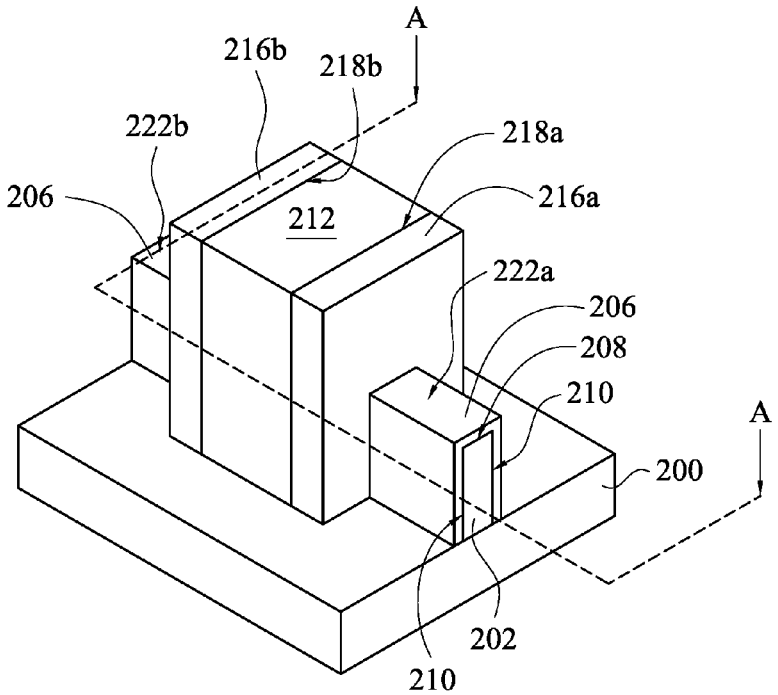

A
216b
218b
222b
218a
206
216a
212
222a
206
208
210
A
200
202
210

FIG. 2D

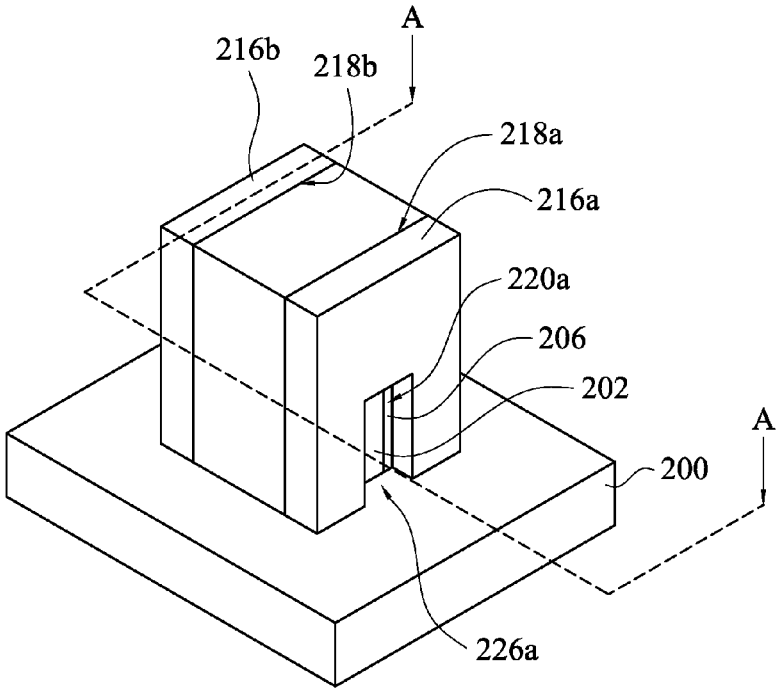

A
216b
218b
218a
216a
220a
206
202
A
200
226a

FIG. 2E

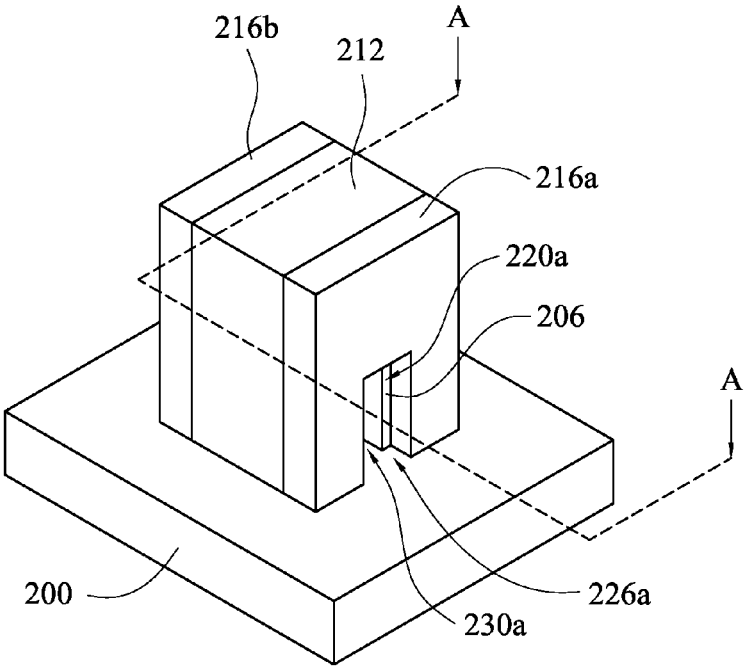

216b
212
A
216a
220a
206
A
200
226a
230a

FIG. 2F

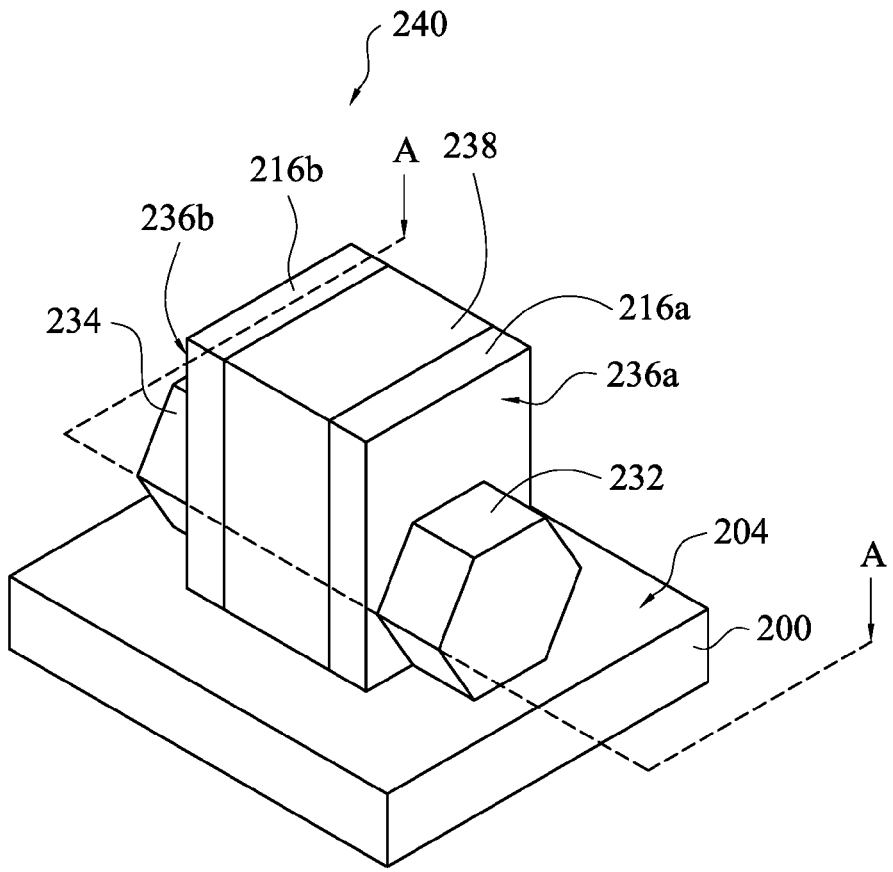


FIG. 2G

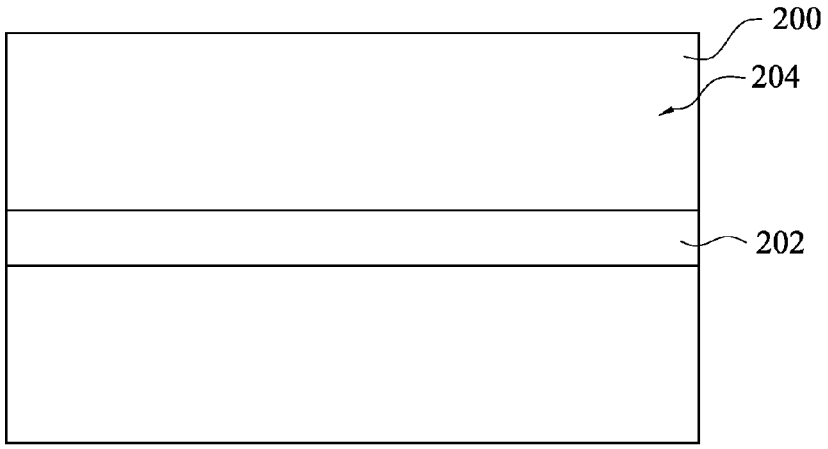


FIG. 3A

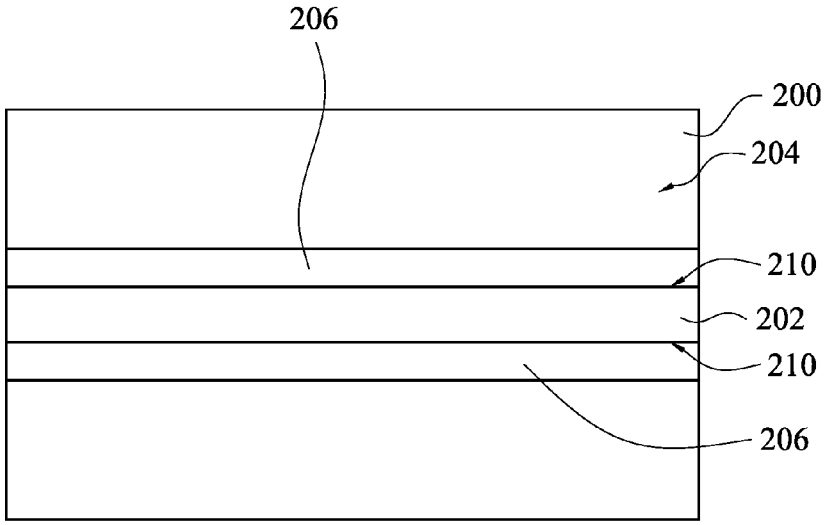


FIG. 3B

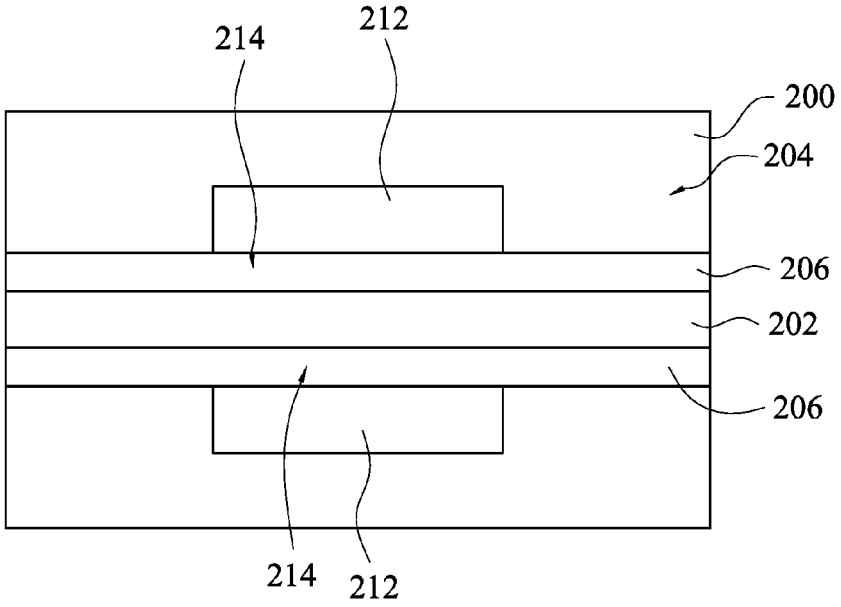
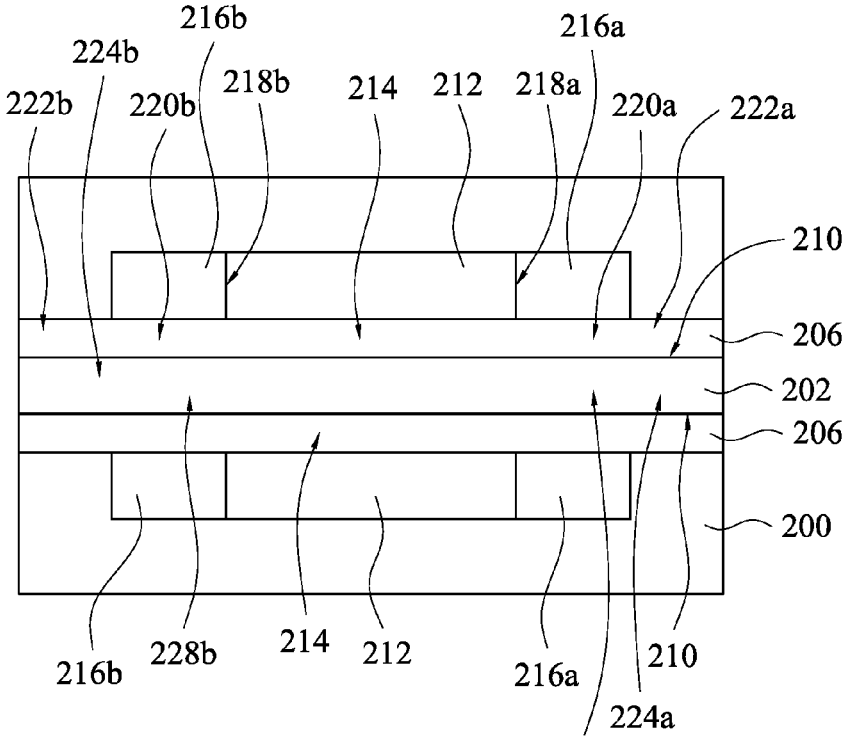

214
212
200
204
206
202
206
214
212

FIG. 3C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224b
222b
220b
218b
214
212
218a
216a
220a
222a
210
206
202
206
200
216b
228b
214
212
216a
210
224a
228a

FIG. 3D

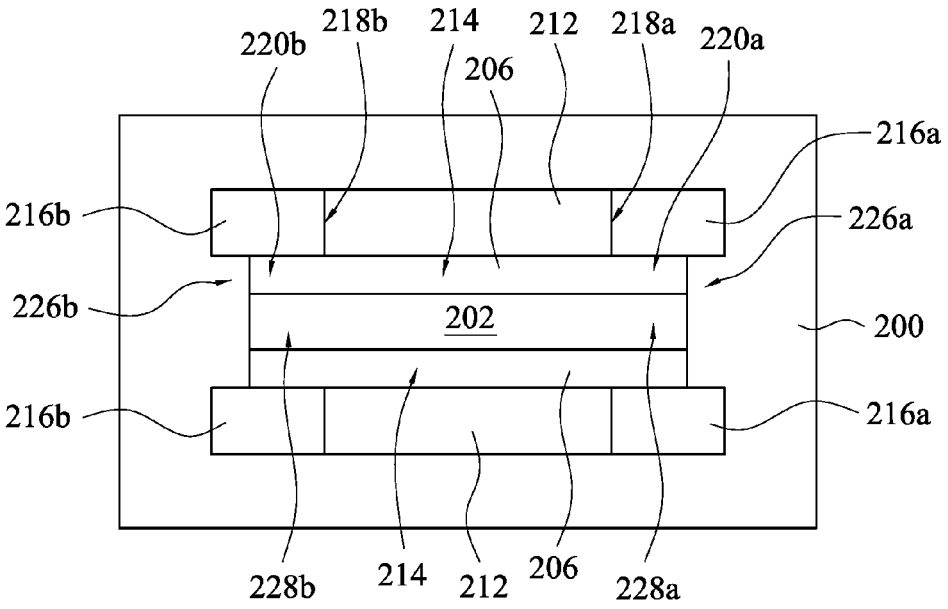

220b
218b
214
212
218a
220a
206
216a
216b
226a
226b
202
200
216b
216a
228b
214
212
206
228a

FIG. 3E

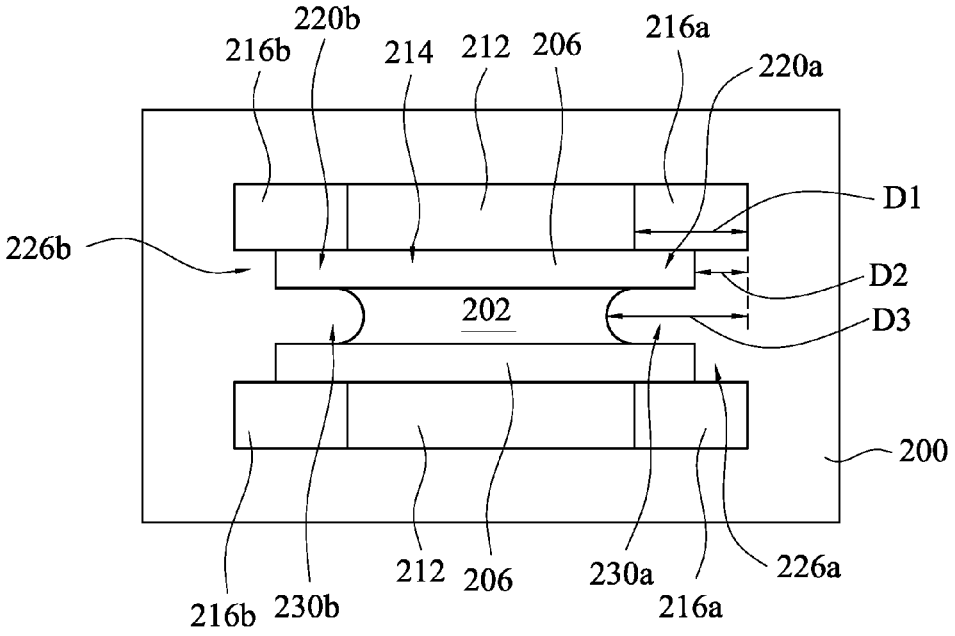
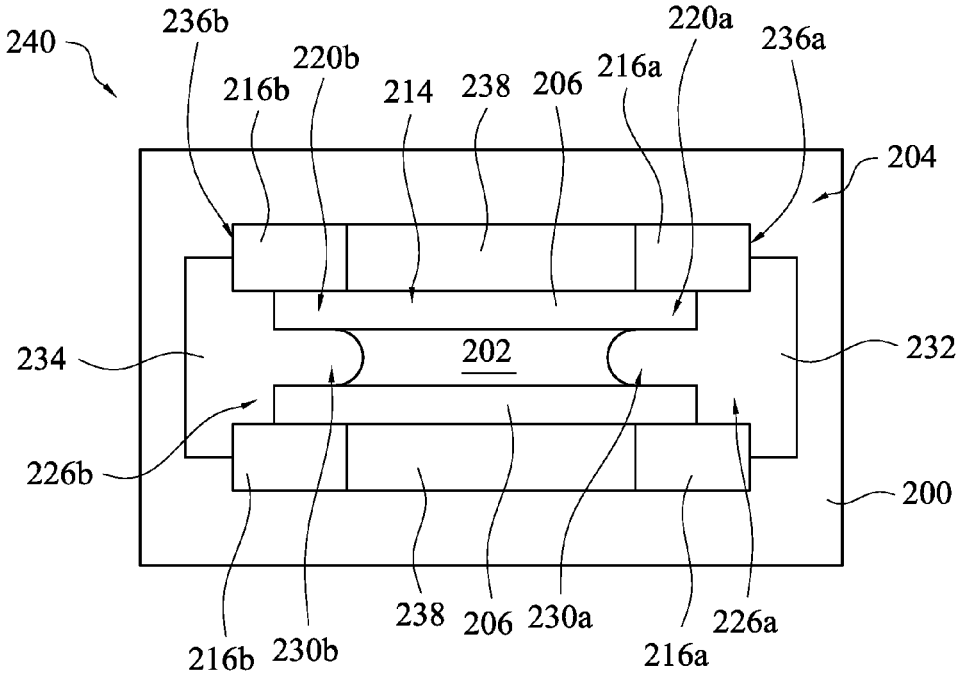

220b
216b
214
212
206
216a
220a
D1
226b
D2
202
D3
200
216b
230b
212
206
230a
216a
226a

FIG. 3F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236b
220b
216b
214
238
206
216a
220a
236a
204
234
202
232
226b
200
216b
230b
238
206
230a
216a
226a

FIG. 3G

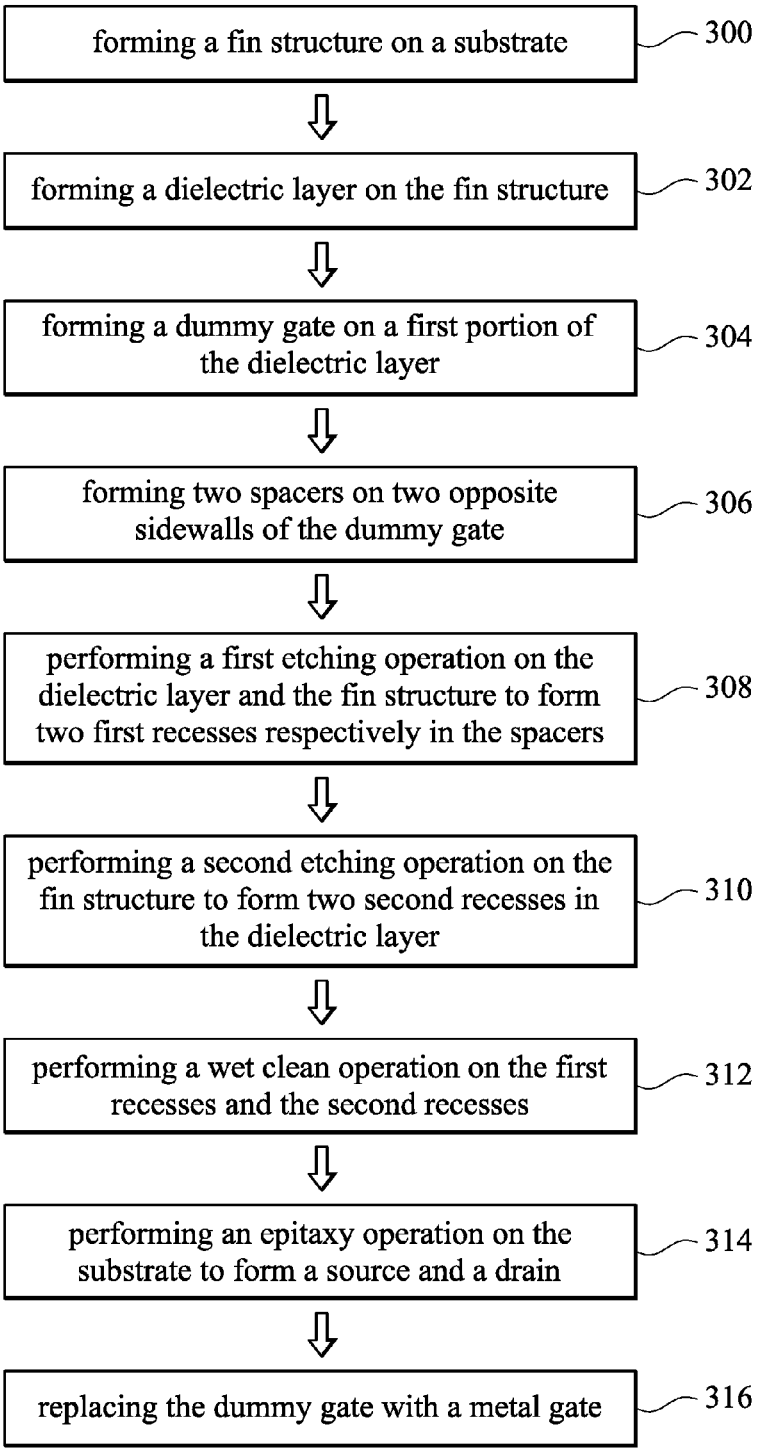
forming a fin structure on a substrate
300
forming a dielectric layer on the fin structure
302
forming a dummy gate on a first portion of the dielectric layer
304
forming two spacers on two opposite sidewalls of the dummy gate
306
performing a first etching operation on the dielectric layer and the fin structure to form two first recesses respectively in the spacers
308
performing a second etching operation on the fin structure to form two second recesses in the dielectric layer
310
performing a wet clean operation on the first recesses and the second recesses
312
performing an epitaxy operation on the substrate to form a source and a drain
314
replacing the dummy gate with a metal gate
316

FIG. 4

SOURCE AND DRAIN PROCESS FOR FINFET

BACKGROUND

The semiconductor integrated circuit (IC) industry has experienced rapid growth. In the course of the IC evolution, functional density (defined as the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased. A scaling down process generally provides benefits by increasing production efficiency and lowering associated costs. But, such scaling down has increased the complexity of processing and manufacturing ICs. For these advances to be realized, similar developments in IC manufacturing are needed.

For example, as the semiconductor IC industry has progressed into nanometer technology process nodes in pursuit of higher device density, higher performance, and lower costs, challenges from both fabrication and design have resulted in the development of three-dimensional (3D) devices such a fin-like field effect transistors (FinFETs). However, conventional FinFET devices and methods of fabricating the FinFET devices have not been entirely satisfactory in every aspect.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1**A is schematic three-dimensional diagram of a FinFET in accordance with various embodiments.

FIG. **1**B is schematic top view of the FinFET taken along line A-A of FIG. **1**A.

FIG. **2**A through FIG. **2**G are three-dimensional diagrams of intermediate stages showing a method for manufacturing a FinFET in accordance with various embodiments.

FIG. **3**A through FIG. **3**G are schematic top views of the FinFET taken along line A-A of FIG. **2**A through **2**G respectively.

FIG. **4** is a flow chart of a method for manufacturing a FinFET in accordance with various embodiments.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact.

Terms used herein are only used to describe the specific embodiments, which are not used to limit the claims appended herewith. For example, unless limited otherwise, the term "one" or "the" of the single form may also represent

the plural form. The terms such as "first" and "second" are used for describing various devices, areas and layers, etc., though such terms are only used for distinguishing one device, one area or one layer from another device, another area or another layer. Therefore, the first area can also be referred to as the second area without departing from the spirit of the claimed subject matter, and the others are deduced by analogy. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

In a typical FinFET replacement polysilicon gate (RPG) technology with a high-k metal gate last (HKMG) process, an operation of removing of a portion of a fin structure and a portion of a dielectric layer covering the fin structure needs a high over-etching amount of the fin structure and the dielectric layer, thereby enlarging a process window for each of sequential deposition process of a high-k dielectric layer and a metal gate, thus enhancing a performance of the FinFET. However, the high over-etching amount of the dielectric layer shortens a portion of the dielectric layer that is used for blocking a dummy gate which covers a portion of the dielectric layer and the underlying fin structure, such that an extrusion path is decreased to result in footing of the dummy gate, and thus causing a metal gate extrusion issue.

Embodiments of the present disclosure are directed to providing a FinFET and a method for manufacturing the FinFET, in which a first etching operation is performed on a fin structure and a dielectric layer covering the fin structure to recess the fin structure and the dielectric layer, so as to form two first recesses respectively in two spacers which cover the dielectric layer and the fin structure, and then a second etching operation is performed on the fin structure to further recess the fin structure to form two second recesses in the dielectric layer, in which the seconds respectively communicate with the first recesses. Thus, portions of the dielectric layer used for blocking a dummy gate are lengthened, the dummy gate covering the dielectric layer and the fin structure and being sandwiched between the spacers, such that each extrusion path is increased, thereby enhancing the yield of the FinFET.

Referring to FIG. **1**A and FIG. **1**B, FIG. **1**A is schematic three-dimensional diagram of a FinFET in accordance with various embodiments, and FIG. **1**B is schematic top view of the FinFET taken along line A-A of FIG. **1**A. In some embodiments, a FinFET **100** includes a substrate **102**, a fin structure **104**, a dielectric layer **106**, a metal gate **110**, two spacers **108**, a source **112** and a drain **114**. The fin structure **104**, the dielectric layer **106**, the metal gate **110**, the spacers **108**, the source **112** and the drain **114** are disposed on the substrate **102**.

The fin structure **104** is disposed on the substrate **102**. In some exemplary examples, the fin structure **104** is formed by recessing the substrate **102**, and thus the fin structure **104** protrudes from a recessed surface **116** of the substrate **102**, and the fin structure **104** and the substrate **102** are formed from the same material. The substrate **102** and the fin structure **104** may be composed of a single-crystalline semiconductor material or a compound semiconductor material. For example, silicon, germanium or glass may be used as a material of the substrate **102** and the fin structure **104**. In some exemplary examples, the substrate **102** and the fin structure **104** are composed of silicon.

Referring to FIG. **1**B again, the dielectric layer **106** is disposed on the fin structure **104** and covers two opposite side surfaces **118** of the fin structure **104**. The dielectric layer **106** includes two first portions **120**, in which the first portions **120** disposed at two opposite ends of the dielectric layer **106**. A cross-section of each of the first portions **120** is in an inverted U-shape. Each of the first portions **120** of the dielectric layer **106** protrudes from the side surfaces **118** of the fin structure **104** to form a first recess **122** in the dielectric layer **106**. Thus, the first recesses **122** are opposite to each other. In some examples, the fin structure **104** and the dielectric layer **106** are formed from different materials, such that the dielectric layer **106** has an etching selectivity with respect to the fin structure **104** during an operation of etching the fin structure **104**. For example, the fin structure **104** may be formed from silicon, and the dielectric layer **106** may be formed from silicon oxide.

Referring to FIG. **1**A and FIG. **1**B, the metal gate **110** is disposed on a second portion **126** of the dielectric layer **106**. In the dielectric layer **106**, the second portion **126** is adjacent to the first portions **120**, in which the first portions **120** are located at two opposite ends of the second portion **126**, such that the second portion **126** is sandwiched between the first portions **120**. A cross-section of the metal gate **110** is in an inverted U-shape.

As shown in FIG. **1**A and FIG. **1**B, the spacers **108** are respectively disposed on the first portions **120** of the dielectric layer **106**. A cross-section of each of the spacers **108** is in an inverted U-shape. The spacers **108** respectively protrude from the first portions **120** of the dielectric layer **106** which are covered by the spacer **108**, so as to form two second recesses **124** in the spacers **108**. The second recesses **124** correspondingly communicate with the first recesses **122**. In some examples, the spacers **108** and the fin structure **104** are formed from different materials, such that the spacers **108** have an etching selectivity with respect to the fin structure **104** during an operation of etching the fin structure **104**. In some exemplary examples, the spacers **108**, the dielectric layer **106** and the fin structure **104** are formed from different materials. For example, the spacers **108** may be formed from silicon nitride, while the fin structure **104** may be formed from silicon, and the dielectric layer **106** may be formed from silicon oxide.

As shown in FIG. **1**B, the fin structure **104** is further recessed to form the first recesses **122**, such that a length L**1** of each spacer **108** is greater than a length L**2** of each second recess **124**, and a length L**3** of a combination of the first recess **122** and the corresponding second recess **124** is greater than the length L**1** of each spacer **108**. In some exemplary examples, the length L**1**, the length L**2** and the length L**3** are within a range from 0.5 Å to 100 Å.

As shown in FIG. **1**A and FIG. **1**B, the source **112** is disposed in one of the first recess **122** and the corresponding second recess **124** on the substrate **102**, and protrudes from the second recess **124**. In addition, the drain **114** is disposed in the other one of the first recess **122** and the corresponding second recess **124** on the substrate **102**, and protrudes from the second recess **124**. In some examples, the source **112** and the drain **114** may extend through the recessed surface **116** into the substrate **102**. For example, each of the source **112** and the drain **114** may include an epitaxy layer. In some exemplary examples, the source **112** and the drain **114** are formed from silicon germanium (SiGe).

Referring to FIG. **1**B again, the first recesses **122** are respectively formed in the first portions **120** of the dielectric layer **106**, such that extrusion paths of the metal gate **110** are increased with the existence of the first portions **120** of the dielectric layer **106**, and thus the metal gate **110** can be effectively blocked by the first portions **120** of the dielectric layer **106**, thereby enhancing the yield of the FinFET **100**.

Referring to FIG. **2**A through FIG. **2**G and FIG. **3**A through FIG. **3**G, FIG. **2**A through FIG. **2**G are three-dimensional diagrams of intermediate stages showing a method for manufacturing a FinFET in accordance with various embodiments, and FIG. **3**A through FIG. **3**G are schematic top views of the FinFET taken along line A-A of FIG. **2**A through **2**G respectively. As shown in FIG. **2**A and FIG. **3**A, a substrate **200** is provided. In some examples, the substrate **200** may be optionally recessed to form a fin structure **202** on a surface **204** of the substrate **200** by using, for example, a photolithography process and an etching process.

In the operation of recessing the substrate **200**, a portion of the substrate **200** is removed. In such examples, the fin structure **202** is composed of a portion of the substrate **200**, such that the fin structure **202** is formed from a material the same as that of the substrate **200**. The substrate **200** and the fin structure **202** may be composed of a single-crystalline semiconductor material or a compound semiconductor material. In some examples, silicon, germanium or glass may be used as a material of the substrate **200** and the fin structure **202**. In some exemplary examples, the substrate **200** and the fin structure **202** are formed from silicon.

As shown in FIG. **2**B and FIG. **3**B, a dielectric layer **206** is formed on a top surface **208** and two opposite side surfaces **210** of the fin structure **202**. In the fin structure **202**, the side surfaces **210** are connected to two opposite edges of the top surface **208**. For example, the side surfaces **210** may extend along an extending direction of the fin structure. Thus, a cross-section of each of the dielectric layer **206** is in an inverted U-shape. For example, the dielectric layer **206** may be formed by using a deposition process or a thermal oxidation process. The deposition process may be a chemical vapor deposition (CVD) process or a plasma-enhanced chemical vapor deposition (PECVD) process. In some examples, the fin structure **202** and the dielectric layer **206** are formed from different materials, such that the dielectric layer **206** has an etching selectivity with respect to the fin structure **202** during an operation of etching the fin structure **202**. For example, the fin structure **202** may be formed from silicon, and the dielectric layer **206** may be formed from silicon oxide.

As shown in FIG. **2**C and FIG. **3**C, a dummy gate **212** is formed on a first portion **214** of the dielectric layer **206**. In some exemplary examples, the dummy gate **212** extends from one of the side surfaces **210** to the other one of the side surfaces **210** through the top surface **208** of the fin structure **202**, such that a cross-section of the dummy gate **212** is in an inverted U-shape. In some examples, the dummy gate **212** is formed by using a deposition process and an etching process. The deposition process may be a chemical vapor deposition process or a plasma-enhanced chemical vapor deposition process, for example. In some exemplary examples, the dummy gate **212** is formed from polysilicon.

As shown in FIG. **2**D and FIG. **3**D, two spacers **216***a* and **216***b* are respectively formed on two opposite sidewalls **218***a* and **218***b* of the dummy gate **212**. In some examples, an operation of forming the spacers **216***a* and **216***b* includes forming the spacers **216***a* and **216***b* on two second portions **220***a* and **220***b* of the dielectric layer **206** respectively, and exposing two third portions **222***a* and **222***b* of the dielectric layer **206**. In the dielectric layer **206**, the second portion **220***a* is located between the first portion **214** and the third portion **222***a*, and the second portion **220***b* is located

between the first portion **214** and the third portion **222***b*. For example, the second portions **220***a* and **220***b* are closely adjacent to opposite sides of the first portion **214** respectively, and the third portions **222***a* and **222***b* are closely adjacent to the second portions **220***a* and **220***b* respectively.

As shown in FIG. **2**D, each of the spacers **216***a* and **216***b* extends from one of the side surfaces **210** to the other one of the side surfaces **210** through the top surface **208** of the fin structure **202**, such that a cross-section of each of the spacers **216***a* and **216***b* is in an inverted U-shape. For example, the spacers **216***a* and **216***b* are formed by using a deposition process and an etching process. The deposition process may be a chemical vapor deposition process or a physical vapor deposition (PVD) process, for example. The etching process may be an etching back process. In some examples, the spacers **216***a* and **216***b* and the fin structure **202** are formed from different materials, such that the spacers **216***a* and **216***b* have an etching selectivity with respect to the fin structure **202** during an operation of etching the fin structure **202**. In some exemplary examples, the spacers **216***a* and **216***b*, the dielectric layer **206** and the fin structure **202** are formed from different materials. For example, the spacers **216***a* and **216***b* may be formed from silicon nitride, while the fin structure **202** may be formed from silicon, and the dielectric layer **206** may be formed from silicon oxide.

Referring to FIG. **3**D, a first etching operation is performed on the dielectric layer **206** and the fin structure **202** to remove the third portions **222***a* and **222***b* and a portion of each of the second portions **220***a* and **220***b* of the dielectric layer **206**, and two first portions **224***a* and **224***b* of the fin structure **202** underlying the third portions **222***a* and **222***b* and the portions of the second portions **220***a* and **220***b* of the dielectric layer **206**. As shown in FIG. **2**E and FIG. **3**E, after the first etching operation is completed, the spacers **216***a* and **216***b* respectively protrude from the first portions **220***a* and **220***b* of the dielectric layer **206**, so as to form two first recesses **226***a* and **226***b* in the spacers **216***a* and **216***b* respectively. In some examples, the first etching operation is a high bias etching operation. The first etching operation may be performed by using a dry etching technique.

Referring to FIG. **3**D and FIG. **3**E simultaneously, a second etching operation is performed on the fin structure **202** to remove two second portions **228***a* and **228***b* of the fin structure **202** which are respectively adjacent to the first portions **224***a* and **224***b* of the fin structure **202**. As shown in FIG. **2**F and FIG. **3**F, after the second etching operation is completed, the remaining second portions **220***a* and **220***b* of the dielectric layer **206** protrude from two opposite ends of the fin structure **202** to respectively form second recesses **230***a* and **230***b* in the dielectric layer **206**. The second recesses **230***a* and **230***b* correspondingly communicate with the first recesses **226***a* and **226***b*. In some examples, the second etching operation is a high selectivity etching operation, and the dielectric layer **206** has an etching selectivity with respect to the fin structure **202** during the second etching operation. Thus, a cross-section of each of the second portions **220***a* and **220***b* of the dielectric layer may be in an inverted U-shape after the second etching operation is completed. The second etching operation may be performed by using a dry etching technique.

Referring to FIG. **3**F again, with a two-step etching process, the fin structure **202** is further recessed to form the second recesses **230***a* and **230***b* during the second etching operation, such that a length D**1** of each of the spacers **216***a* and **216***b* is greater than a length D**2** of each of the first recesses **226***a* and **226***b*, and a length D**3** of a combination of the first recess **226***a* and the second recess **230***a* or a combination of the first recess **226***b* and the second recess **230***b* is greater than the length D**1** of each of the spacers **216***a* and **216***b*. In some exemplary examples, the length D**1**, the length D**2** and the length D**3** are within a range from 0.5 Å to 100 Å.

By using a two-step etching process, the second recesses **230***a* and **230***b* are respectively formed in the second portions **220***a* and **220***b* of the dielectric layer **206**, such that extrusion paths of the dummy gate **212** are increased with the existence of the second portions **220***a* and **220***b* of the dielectric layer **206**, and thus the dummy gate **212** can be effectively blocked by the second portions **220***a* and **220***b* of the dielectric layer **206**.

In some examples, after the second etching operation is completed, a wet clean operation may be optionally performed on the first recesses **226***a* and **226***b* and the second recesses **230***a* and **230***b* to remove particles, products and/or contaminants from the first recesses **226***a* and **226***b* and the second recesses **230***a* and **230***b*. During the wet clean operation, the dummy gate **212** can be effectively protected by the second portions **220***a* and **220***b* of the dielectric layer **206**, thereby preventing the dummy gate **212** from extruding.

As shown in FIG. **2**G and FIG. **3**G, a source **232** may be formed in the first recess **226***a* and the second recess **230***a* on the substrate **200**, and a drain **234** may be formed in the first recess **226***b* and the second recess **230***b* on the substrate **200**. For example, the source **232** may be formed to fill the first recess **226***a* and the second recess **230***a* and protrude from the spacer **216***a*, such that the source **232** may cover a portion of an outer surface **236***a* of the spacer **216***a* and a portion of the surface **204** of the substrate **200**. The drain **234** may be formed to fill the first recess **226***b* and the second recess **230***b* and protrude from the spacer **216***b*, such that the drain **234** may cover a portion of an outer surface **236***b* of the spacer **216***b* and a portion of the surface **204** of the substrate **200**. In some examples, an operation of forming the source **232** and the drain **234** is performed by using an epitaxy process. In some exemplary examples, each of the source **232** and the drain **234** is formed to include a silicon germanium (SiGe) layer.

Referring to FIG. **2**F and FIG. **2**G simultaneously, after the source **232** and the drain **234** are completed, the dummy **212** are replaced with a metal gate **238** to complete a FinFET **240**. In some examples, an operation of replacing the dummy gate **212** includes removing the dummy gate **212** to form a recess between the spacers **216***a* and **216***b* and expose the first portion **214** of the dielectric layer **206**, and forming the metal gate **238** fill the recess and cover the first portion **214** of the dielectric layer **206**. For example, an operation of removing the dummy gate **212** may be performed using a dry etching technique or a wet etching technique. An operation of forming the metal gate **238** may be performed by using a deposition process and a patterning process, in which the deposition process may be a chemical vapor deposition process or a physical vapor deposition process, and the patterning process may include a chemical mechanical polishing process.

Referring to FIG. **4** with FIG. **2**A through FIG. **2**G and FIG. **3**A through FIG. **3**G, FIG. **4** is a flow chart of a method for manufacturing a FinFET in accordance with various embodiments. The method begins at operation **300**, where a substrate **200** is provided. In some examples, the substrate **200** may be optionally recessed to form a fin structure **202** on a surface **204** of the substrate **200** by using, for example, a photolithography process and an etching process. In the

operation of recessing the substrate **200**, a portion of the substrate **200** is removed. In such examples, the fin structure **202** is composed of a portion of the substrate **200**, such that the fin structure **202** is formed from a material the same as that of the substrate **200**. In some examples, silicon, germanium or glass may be used as a material of the substrate **200** and the fin structure **202**.

At operation **302**, as shown in FIG. **2**B and FIG. **3**B, a dielectric layer **206** is formed on a top surface **208** and two opposite side surfaces **210** of the fin structure **202**. In the fin structure **202**, the side surfaces **210** are connected to two opposite edges of the top surface **208**. For example, the dielectric layer **206** may be formed by using a deposition process or a thermal oxidation process. The deposition process may be a chemical vapor deposition process or a plasma-enhanced chemical vapor deposition process. The fin structure **202** and the dielectric layer **206** are formed from different materials, such that the dielectric layer **206** has an etching selectivity with respect to the fin structure **202** during an operation of etching the fin structure **202**.

At operation **304**, as shown in FIG. **2**C and FIG. **3**C, a dummy gate **212** is formed on a first portion **214** of the dielectric layer **206** by using, for example, a deposition process and an etching process. The deposition process may be a chemical vapor deposition process or a plasma-enhanced chemical vapor deposition process. In some exemplary examples, the dummy gate **212** extends from one of the side surfaces **210** to the other one of the side surfaces **210** through the top surface **208** of the fin structure **202**, such that a cross-section of the dummy gate **212** is in an inverted U-shape. In some exemplary examples, the dummy gate **212** is formed from polysilicon.

At operation **306**, as shown in FIG. **2**D and FIG. **3**D, two spacers **216***a* and **216***b* are respectively formed on two opposite sidewalls **218***a* and **218***b* of the dummy gate **212** by using for example, a deposition process and an etching process. The deposition process may be a chemical vapor deposition process or a physical vapor deposition process. The etching process may be an etching back process. In some examples, an operation of forming the spacers **216***a* and **216***b* includes forming the spacers **216***a* and **216***b* on two second portions **220***a* and **220***b* of the dielectric layer **206** respectively, and exposing two third portions **222***a* and **222***b* of the dielectric layer **206**. In the dielectric layer **206**, the second portion **220***a* is located between the first portion **214** and the third portion **222***a*, and the second portion **220***b* is located between the first portion **214** and the third portion **222***b*. For example, the second portions **220***a* and **220***b* are closely adjacent to opposite sides of the first portion **214** respectively, and the third portions **222***a* and **222***b* are closely adjacent to the second portions **220***a* and **220***b* respectively, such that the second portion **220***a* is sandwiched between the first portion **214** and the third portion **222***a*, and the second portion **220***b* is sandwiched between the first portion **214** and the third portion **222***b*.

Referring to FIG. **2**D again, each of the spacers **216***a* and **216***b* extends from one of the side surfaces **210** to the other one of the side surfaces **210** through the top surface **208** of the fin structure **202**, such that a cross-section of each of the spacers **216***a* and **216***b* is in an inverted U-shape. In some examples, the spacers **216***a* and **216***b* and the fin structure **202** are formed from different materials, such that the spacers **216***a* and **216***b* have an etching selectivity with respect to the fin structure **202** during an operation of etching the fin structure **202**. In some exemplary examples, the spacers **216***a* and **216***b*, the dielectric layer **206** and the fin structure **202** are formed from different materials. For example, the spacers **216***a* and **216***b* may be formed from silicon nitride, the fin structure **202** may be formed from silicon, and the dielectric layer **206** may be formed from silicon oxide.

At operation **308**, as shown in FIG. **3**D, a first etching operation is performed on the dielectric layer **206** and the fin structure **202** to remove the third portions **222***a* and **222***b* and a portion of each of the second portions **220***a* and **220***b* of the dielectric layer **206**, and two first portions **224***a* and **224***b* of the fin structure **202** underlying the third portions **222***a* and **222***b* and the portions of the second portions **220***a* and **220***b* of the dielectric layer **206**. In some examples, the first etching operation is a high bias etching operation. The first etching operation may be performed by using a dry etching technique. As shown in FIG. **2**E and FIG. **3**E, after the first etching operation is completed, the spacers **216***a* and **216***b* respectively protrude from the first portions **220***a* and **220***b* of the dielectric layer **206**, so as to form two first recesses **226***a* and **226***b* in the spacers **216***a* and **216***b* respectively.

At operation **310**, referring to FIG. **3**D and FIG. **3**E simultaneously, a second etching operation is performed on the fin structure **202** to remove two second portions **228***a* and **228***b* of the fin structure **202** which are respectively adjacent to the first portions **224***a* and **224***b* of the fin structure **202**. As shown in FIG. **2**F and FIG. **3**F, after the second etching operation is completed, the remaining second portions **220***a* and **220***b* of the dielectric layer **206** protrude from two opposite ends of the fin structure **202** to respectively form second recesses **230***a* and **230***b* in the dielectric layer **206**. The second recesses **230***a* and **230***b* respectively communicate with the first recesses **226***a* and **226***b*. In some examples, the second etching operation is a high selectivity etching operation, and the dielectric layer **206** has an etching selectivity with respect to the fin structure **202** during the second etching operation. Thus, a cross-section of each of the remaining second portions **220***a* and **220***b* of the dielectric layer may be in an inverted U-shape. The second etching operation may be performed by using a dry etching technique.

At operation **312**, referring to FIG. **2**F and FIG. **3**F again, after the second etching operation is completed, a wet clean operation may be optionally performed on the first recesses **226***a* and **226***b* and the second recesses **230***a* and **230***b* to remove particles, products and/or contaminants from the first recesses **226***a* and **226***b* and the second recesses **230***a* and **230***b*. During the wet clean operation, the dummy gate **212** can be effectively protected by the second portions **220***a* and **220***b* of the dielectric layer **206**, thereby preventing the dummy gate **212** from extruding.

At operation **314**, as shown in FIG. **2**G and FIG. **3**G, a source **232** may be formed in the first recess **226***a* and the second recess **230***a* on the substrate **200**, and a drain **234** may be formed in the first recess **226***b* and the second recess **230***b* on the substrate **200** by using an epitaxy process. For example, the source **232** may be formed to fill the first recess **226***a* and the second recess **230***a* and protrude from the spacer **216***a*, such that the source **232** may cover a portion of an outer surface **236***a* of the spacer **216***a* and a portion of the surface **204** of the substrate **200**. The drain **234** may be formed to fill the first recess **226***b* and the second recess **230***b* and protrude from the spacer **216***b*, such that the drain **234** may cover a portion of an outer surface **236***b* of the spacer **216***b* and a portion of the surface **204** of the substrate **200**. In some exemplary examples, each of the source **232** and the drain **234** is formed to include a silicon germanium layer.

At operation **316**, referring to FIG. **2**F and FIG. **2**G simultaneously, after the epitaxy process is completed, the dummy **212** are replaced with a metal gate **238** to complete a FinFET **240**. In some examples, an operation of replacing the dummy gate **212** includes removing the dummy gate **212** to form a recess between the spacers **216***a* and **216***b* and expose the first portion **214** of the dielectric layer **206**, and forming the metal gate **238** fill the recess and cover the first portion **214** of the dielectric layer **206**. For example, an operation of removing the dummy gate **212** may be performed using a dry etching technique or a wet etching technique. An operation of forming the metal gate **238** may be performed by using a deposition process and a patterning process, in which the deposition process may be a chemical vapor deposition process or a physical vapor deposition process, and the patterning process may include a chemical mechanical polishing process.

In accordance with an embodiment, the present disclosure discloses a method for manufacturing a FinFET. In this method, a fin structure is formed on a substrate. A dielectric layer is formed on a top surface and two side surfaces of the fin structure, in which the side surfaces are connected to two opposite edges of the top surface, and the fin structure and the dielectric layer are formed from different materials. A dummy gate is formed on a first portion of the dielectric layer. Two spacers are respectively formed on two opposite sidewalls of the dummy gate. An operation of forming the spacers includes forming the spacers respectively on two second portions of the dielectric layer and exposing two third portions of the dielectric layer, in which each of the second portions of the dielectric layer is located between the first portion and one of the third portions of the dielectric layer. A first etching operation is performed on the dielectric layer and the fin structure to remove the third portions and a portion of each of the second portions of the dielectric layer, and two first portions of the fin structure underlying the third portions and the portions of the second portions of the dielectric layer, thereby forming two first recesses respectively in the spacers. A second etching operation is performed on the fin structure to remove two second portions of the fin structure which are respectively adjacent to the first portions of the fin structure, thereby forming two second recesses in the dielectric layer, in which the second recesses respectively communicate with the first recesses.

In accordance with another embodiment, the present disclosure discloses a method for manufacturing a FinFET. In this method, a fin structure is formed on a substrate. A dielectric layer is formed on a top surface and two side surfaces of the fin structure, in which the side surfaces are connected to two opposite edges of the top surface, and the fin structure and the dielectric layer are formed from different materials. A dummy gate is formed on a first portion of the dielectric layer. Two spacers are respectively formed on two opposite sidewalls of the dummy gate. An operation of forming the spacers includes forming the spacers respectively on two second portions of the dielectric layer and exposing two third portions of the dielectric layer, in which each of the second portions of the dielectric layer is located between the first portion and one of the third portions of the dielectric layer. A first etching operation is performed on the dielectric layer and the fin structure to remove the third portions of the dielectric layer, a portion of each of the second portions of the dielectric layer, and two first portions of the fin structure underlying the third portions of the dielectric layer and the portions of the second portions of the dielectric layer, thereby forming two first recesses respectively in the spacers. A second etching operation is performed on the fin structure to remove two second portions of the fin structure which are respectively adjacent to the first portions of the fin structure, thereby forming two second recesses in the dielectric layer, wherein the second recesses respectively communicate with the first recesses. A wet clean operation is performed on the first recesses and the second recesses. An epitaxy operation is performed on the substrate to form a source in one of the first recesses and one of the second recesses on the substrate, and to form a drain in the other one of the first recesses and the other one of the second recesses on the substrate.

In accordance with yet another embodiment, the present disclosure discloses a FinFET. The FinFET includes a substrate, a fin structure, a dielectric layer, a metal gate, two spacers, a source and a drain. The fin structure is disposed on the substrate. The dielectric layer is disposed on the fin structure and covers two opposite side surfaces of the fin structure, in which the dielectric layer includes two first portions protruding from the side surfaces of the fin structure, such that two first recesses are formed in the dielectric layer, and the first recesses are opposite to each other. The metal gate is disposed on a second portion of the dielectric layer, in which the second portion is sandwiched between the first portions of the dielectric layer. The spacers are disposed on the first portions of the dielectric layer respectively, in which the spacers respectively protrude from the first portions of the dielectric layer, such that two second recesses are formed in the spacers. The source is disposed in one of the first recesses and one of the second recesses on the substrate. The drain is disposed in the other one of the first recesses and the other one of the second recesses on the substrate.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method for manufacturing a FinFET, the method comprising:

forming a fin structure on a substrate;

forming a dielectric layer on a top surface and two side surfaces of the fin structure, wherein the side surfaces are connected to two opposite edges of the top surface, and the fin structure and the dielectric layer are formed from different materials;

forming a dummy gate on a first portion of the dielectric layer;

forming two spacers respectively on two opposite sidewalls of the dummy gate, wherein an operation of forming the spacers comprises forming the spacers respectively on two second portions of the dielectric layer and exposing two third portions of the dielectric layer, wherein each of the second portions of the dielectric layer is located between the first portion and one of the third portions of the dielectric layer;

performing a first etching operation on the dielectric layer and the fin structure to remove the third portions and a portion of each of the second portions of the dielectric

layer, and two first portions of the fin structure underlying the third portions and the portions of the second portions of the dielectric layer, thereby forming two first recesses respectively in the spacers; and

performing a second etching operation on the fin structure to remove two second portions of the fin structure which are respectively adjacent to the first portions of the fin structure, thereby forming two second recesses in the dielectric layer, wherein the second recesses respectively communicate with the first recesses.

2. The method of claim **1**, wherein an operation of forming the fin structure forms the fin structure from silicon, and an operation of forming the dielectric layer forms the dielectric layer from silicon oxide.

3. The method of claim **1**, wherein the operation of forming the spacers forms the spacers from silicon nitride.

4. The method of claim **1**, wherein an operation of forming the dummy gate forms the dummy gate from polysilicon.

5. The method of claim **1**, the method further comprising performing a wet clean operation on the first recesses and the second recesses after the second etching operation is completed.

6. The method of claim **1**, the method further comprising performing an epitaxy operation on the substrate to form a source in one of the first recesses and one of the second recesses on the substrate, and to form a drain in the other one of the first recesses and the other one of the second recesses on the substrate after the second etching operation is completed.

7. The method of claim **6**, wherein the epitaxy operation forms the source and the drain each of which comprises a silicon germanium (SiGe) layer.

8. The method of claim **6**, the method further comprising replacing the dummy gate with a metal gate after the epitaxy operation is completed.

9. A method for manufacturing a FinFET, the method comprising:

forming a fin structure on a substrate;

forming a dielectric layer on a top surface and two side surfaces of the fin structure, wherein the side surfaces are connected to two opposite edges of the top surface, and the fin structure and the dielectric layer are formed from different materials;

forming a dummy gate on a first portion of the dielectric layer;

forming two spacers respectively on two opposite sidewalls of the dummy gate, wherein an operation of forming the spacers comprises forming the spacers respectively on two second portions of the dielectric layer and exposing two third portions of the dielectric layer, wherein each of the second portions of the dielectric layer is located between the first portion and one of the third portions of the dielectric layer;

performing a first etching operation on the dielectric layer and the fin structure to remove the third portions of the dielectric layer, a portion of each of the second portions of the dielectric layer, and two first portions of the fin structure underlying the third portions of the dielectric layer and the portions of the second portions of the dielectric layer, thereby forming two first recesses respectively in the spacers;

performing a second etching operation on the fin structure to remove two second portions of the fin structure which are respectively adjacent to the first portions of the fin structure, thereby forming two second recesses in the dielectric layer, wherein the second recesses respectively communicate with the first recesses;

performing a wet clean operation on the first recesses and the second recesses; and

performing an epitaxy operation on the substrate to form a source in one of the first recesses and one of the second recesses on the substrate, and to form a drain in the other one of the first recesses and the other one of the second recesses on the substrate.

10. The method of claim **9**, wherein an operation of forming the fin structure forms the fin structure from silicon, and an operation of forming the dielectric layer forms the dielectric layer from silicon oxide.

11. The method of claim **9**, wherein the operation of forming the spacers forms the spacers from silicon nitride.

12. The method of claim **9**, wherein an operation of forming the dummy gate forms the dummy gate from polysilicon.

13. The method of claim **9**, wherein the epitaxy operation is performed to form the source and the drain each of which comprises a silicon germanium (SiGe) layer.

14. The method of claim **9**, wherein an operation of forming the fin structure is performed by recessing the substrate.

15. The method of claim **9**, the method further comprising replacing the dummy gate with a metal gate after the epitaxy operation is completed.

16. A FinFET comprising:

a substrate;

a fin structure on the substrate;

a dielectric layer which is disposed on the fin structure and covers a top surface and two opposite side surfaces of the fin structure, wherein the dielectric layer comprises two first portions protruding from the side surfaces of the fin structure such that two first recesses are formed in the dielectric layer, each of the first recesses is surrounded by the dielectric layer and the substrate, and the first recesses are opposite to each other;

a metal gate on a second portion of the dielectric layer, wherein the second portion is sandwiched between the first portions of the dielectric layer;

two spacers on the first portions of the dielectric layer respectively, wherein the spacers respectively protrude from the first portions of the dielectric layer such that two second recesses are formed in the spacers;

a source which is disposed in one of the first recesses and one of the second recesses on the substrate; and

a drain which is disposed in the other one of the first recesses and the other one of the second recesses on the substrate.

17. The FinFET of claim **16**, wherein the fin structure is formed from silicon, and the dielectric layer is formed from silicon oxide.

18. The FinFET of claim **16**, wherein the spacers are formed from silicon nitride.

19. The FinFET of claim **16**, wherein the source and the drain are formed from silicon germanium.

20. The FinFET of claim **16**, wherein each of the source and the drain comprises an epitaxy layer.

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