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Zhang et al.

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(54) **FIN FIELD EFFECT TRANSISTOR (FINFET) DEVICE AND METHOD FOR FORMING THE SAME**

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H01L 21/306	(2006.01)
H01L 29/165	(2006.01)

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CPC ***H01L 29/7851*** (2013.01); ***H01L 21/30604*** (2013.01); ***H01L 21/76224*** (2013.01); ***H01L 29/0847*** (2013.01); ***H01L 29/6653*** (2013.01); ***H01L 29/66795*** (2013.01); ***H01L 29/7848*** (2013.01); *H01L 29/165* (2013.01)

(58) **Field of Classification Search**

CPC H01L 29/66795

See application file for complete search history.

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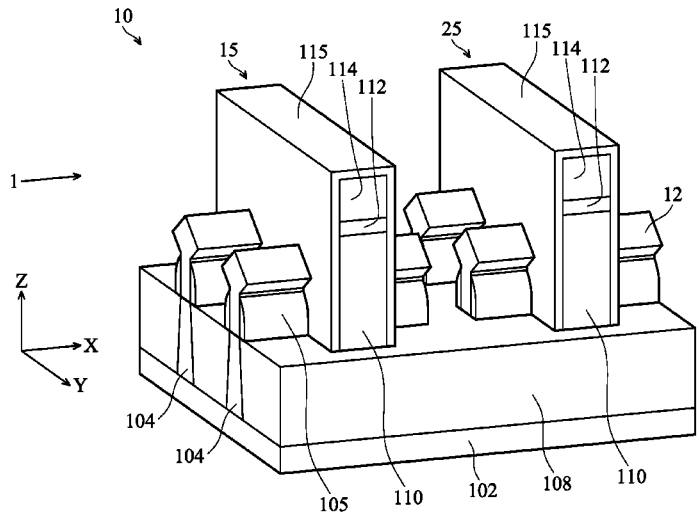
(57) **ABSTRACT**

A fin field effect transistor (FinFET) device structure and method for forming FinFET device structure are provided. The FinFET structure includes a substrate and a fin structure extending above the substrate. The FinFET structure includes an epitaxial structure formed on the fin structure, and the epitaxial structure has a first height. The FinFET structure also includes fin sidewall spacers formed adjacent to the epitaxial structure. The sidewall spacers have a second height and the first height is greater than the second height, and the fin sidewall spacers are configured to control a volume and the first height of the epitaxial structure.

19 Claims, 11 Drawing Sheets



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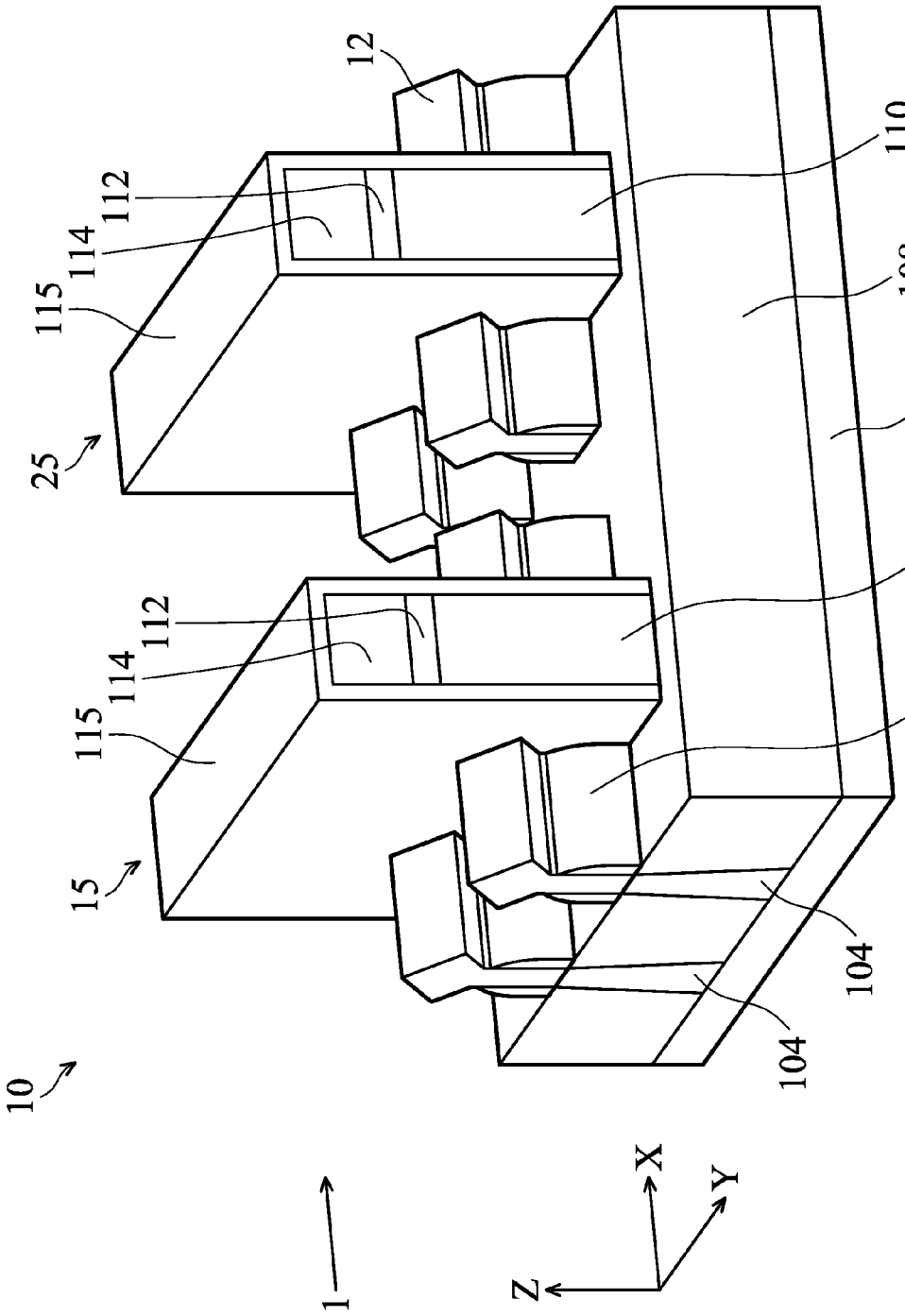
12
110
112
114
115
108
102
25
110
112
114
115
105
15
104
104
10
1
X
Y
Z

FIG. 1

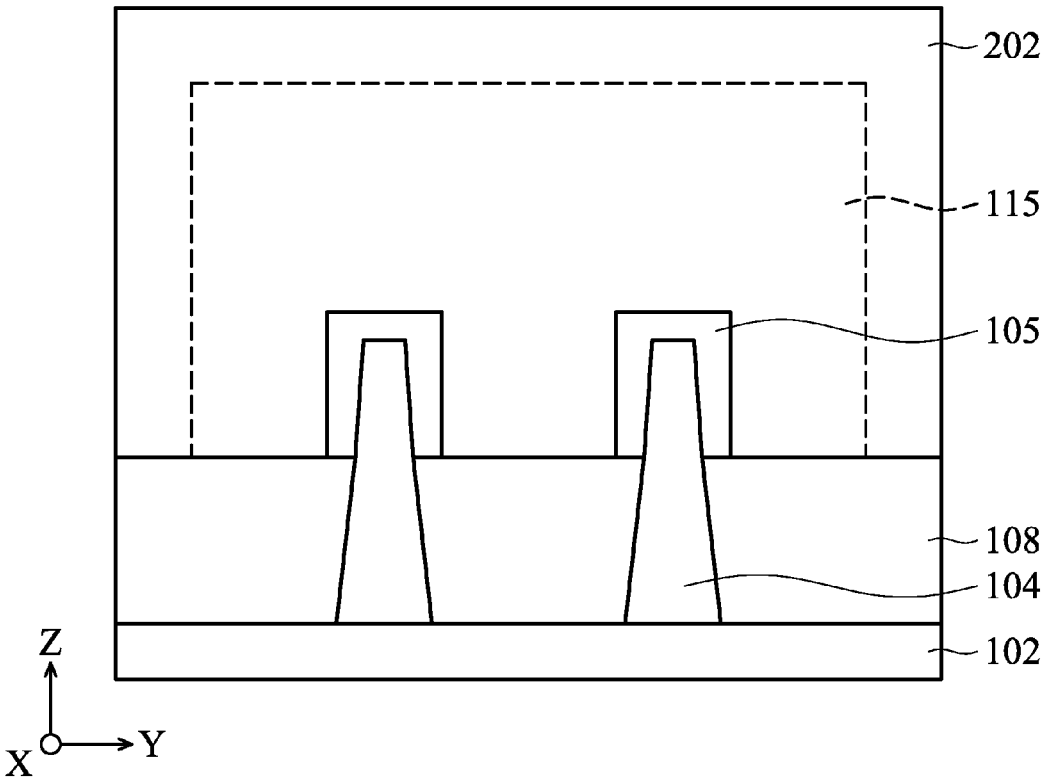

FIG. 2A

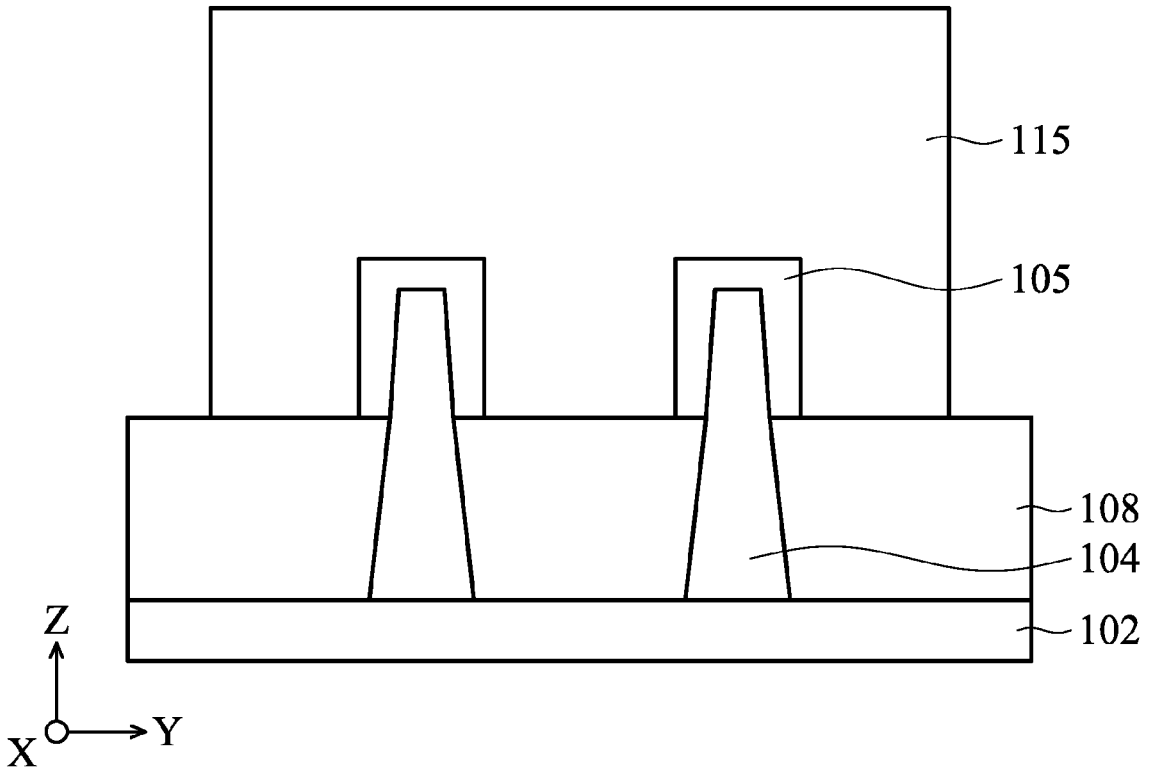

FIG. 2B

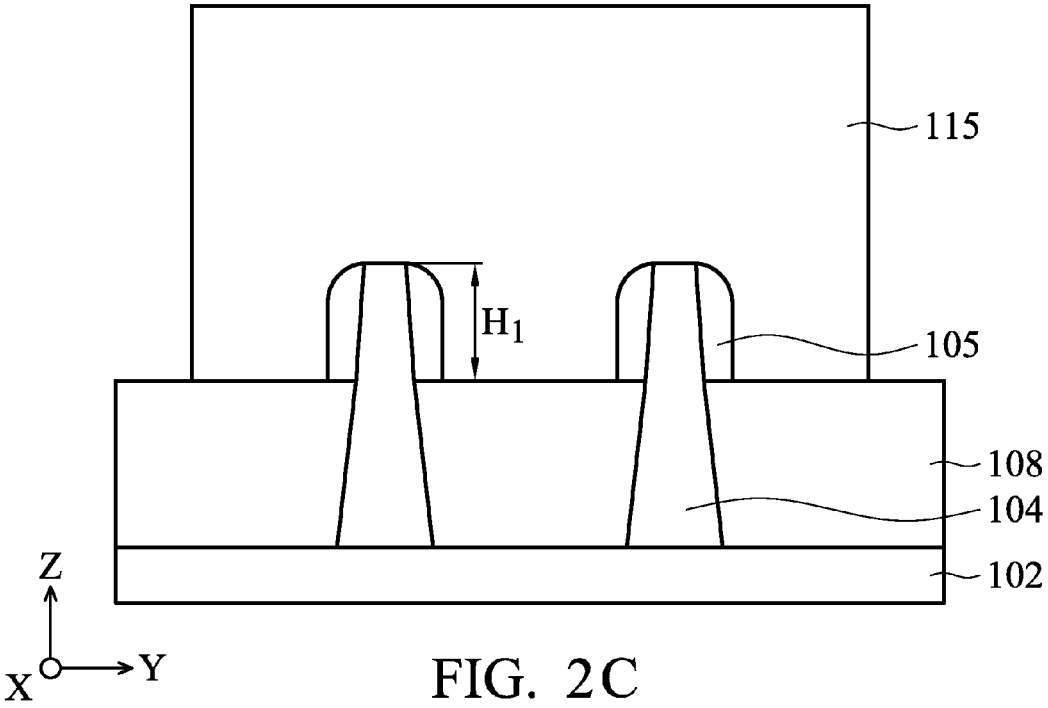

FIG. 2C

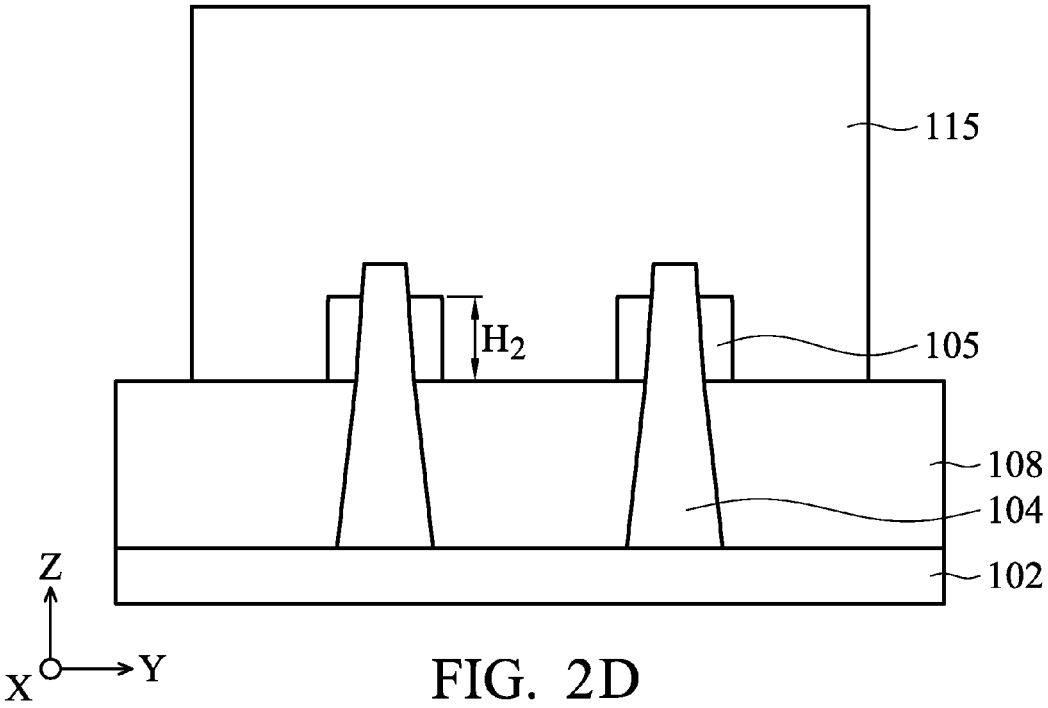

FIG. 2D

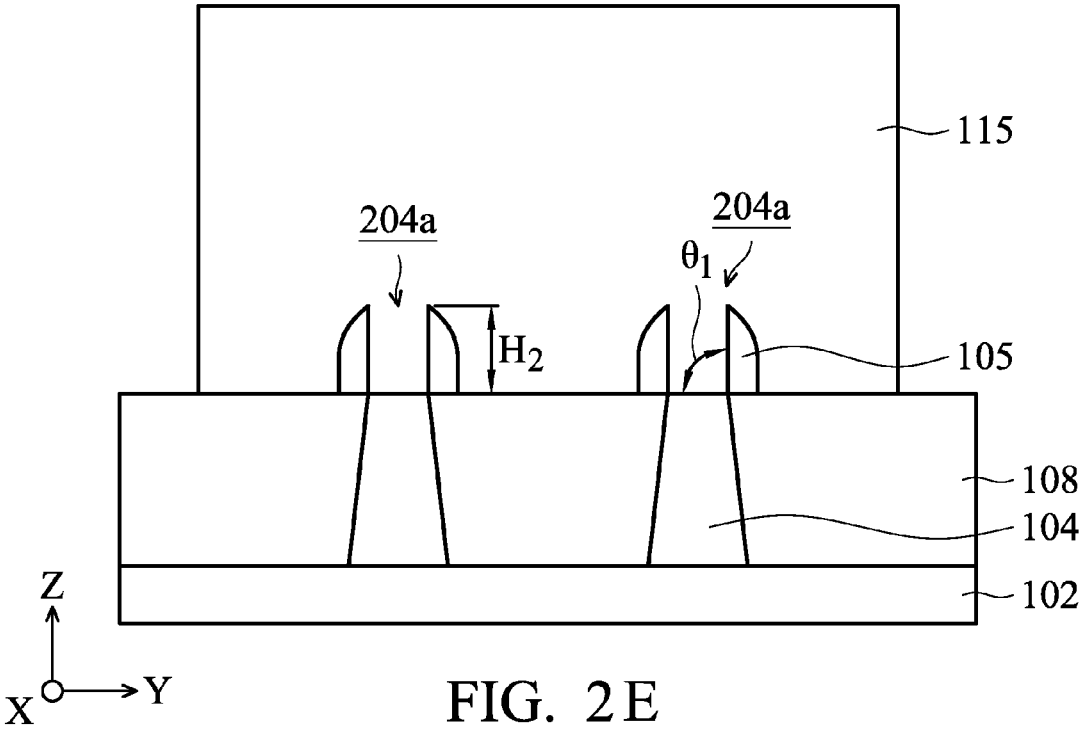
115
204a
204a
θ1
H2
105
108
104
102
Z
Y
X

FIG. 2E

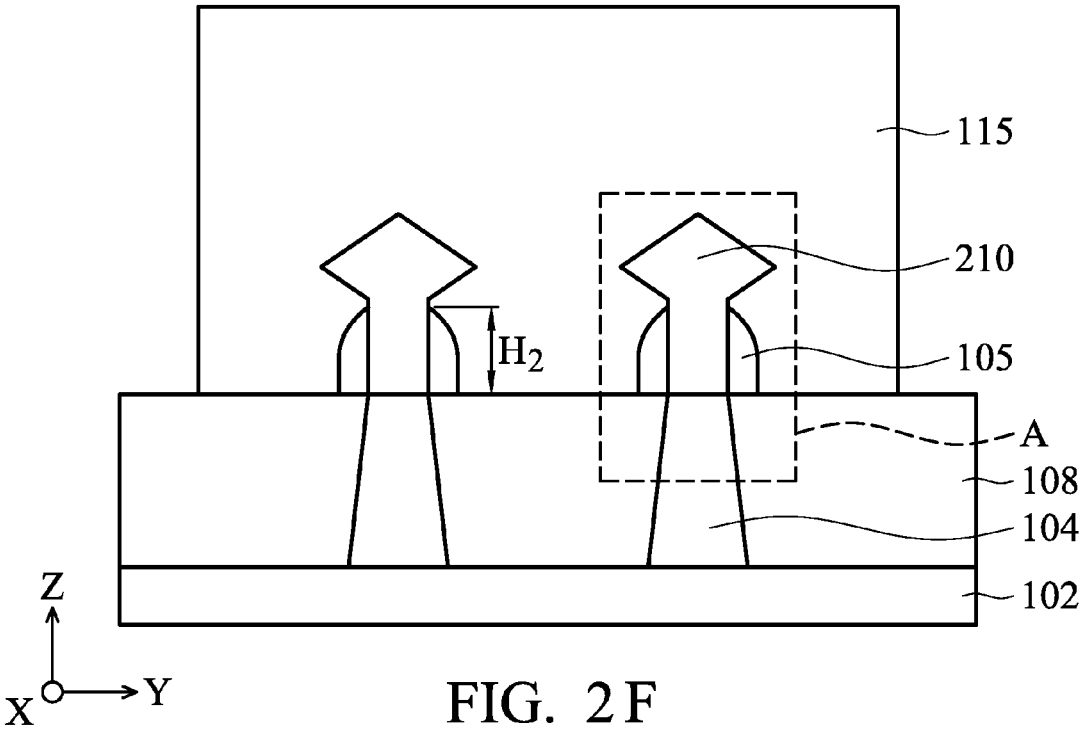
115
210
H2
105
A
108
104
102
Z
Y
X

FIG. 2F

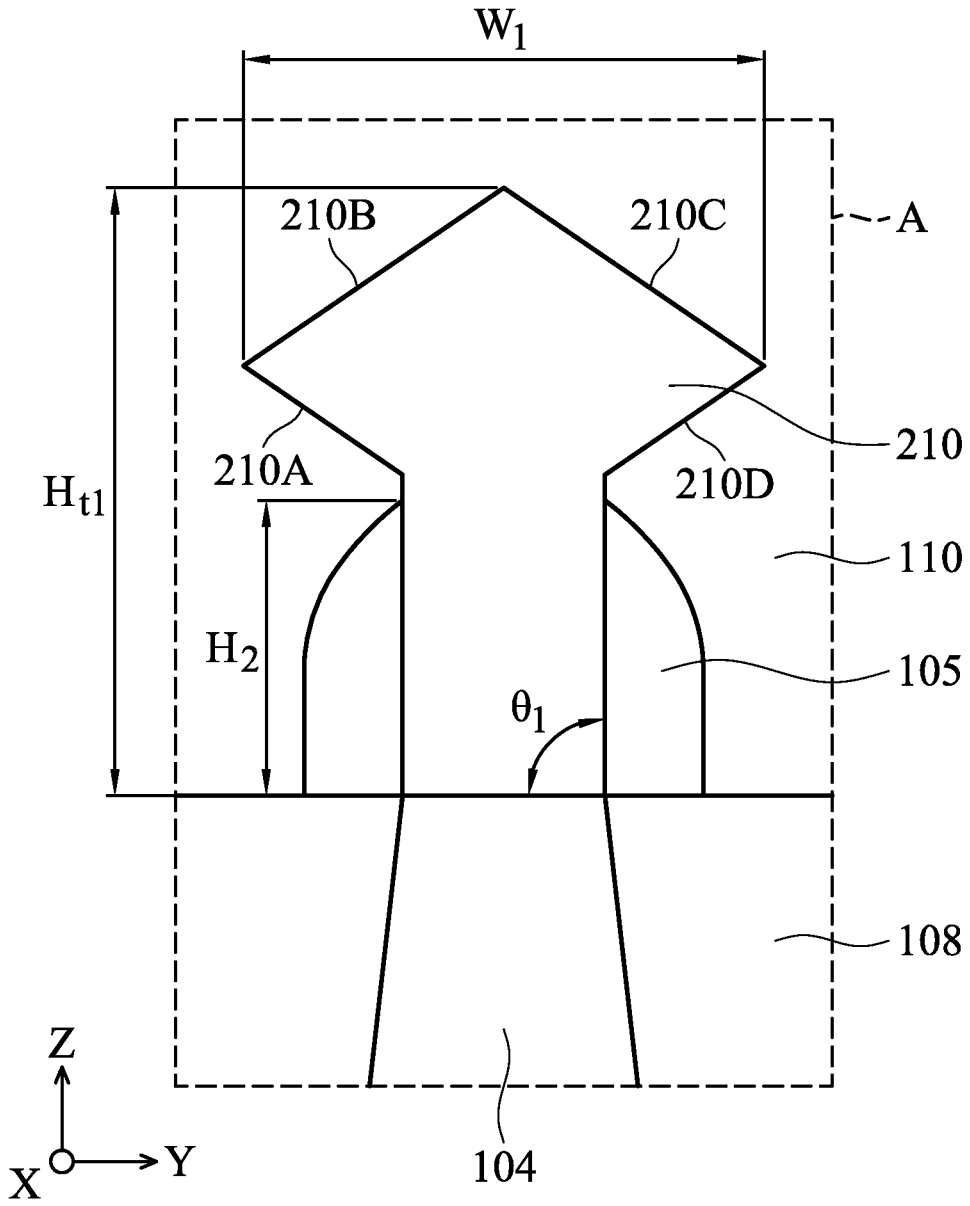

FIG. 2G

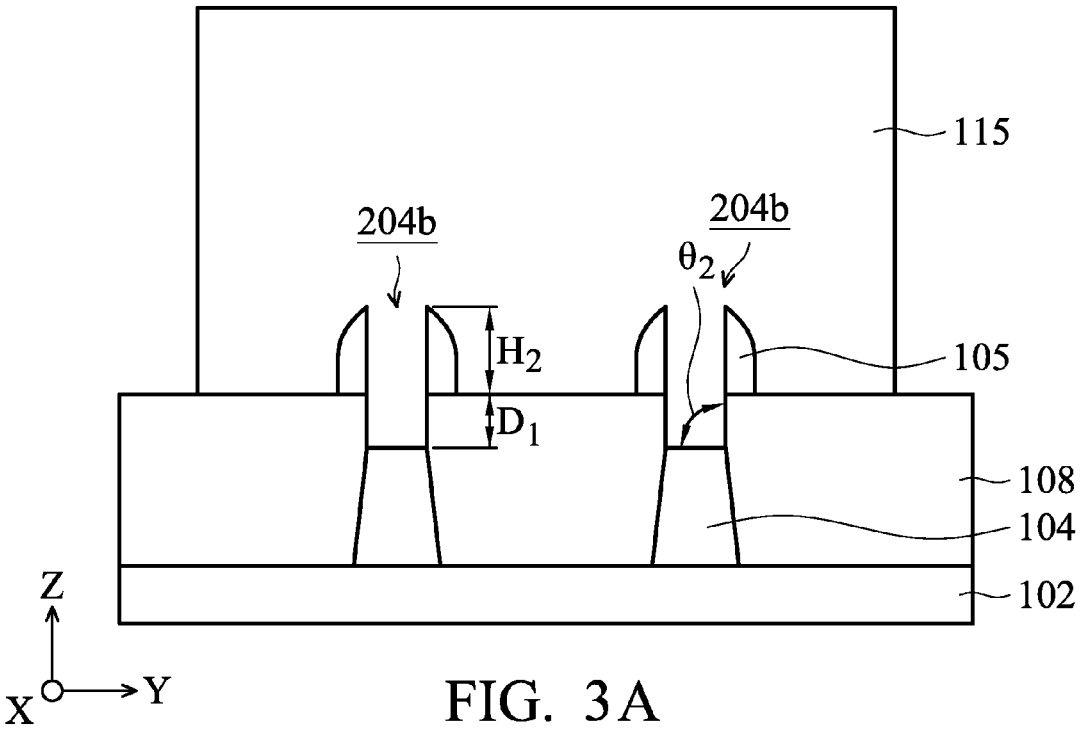
115
204b
204b
θ2
H2
105
D1
108
104
102
Z
X
Y

FIG. 3A

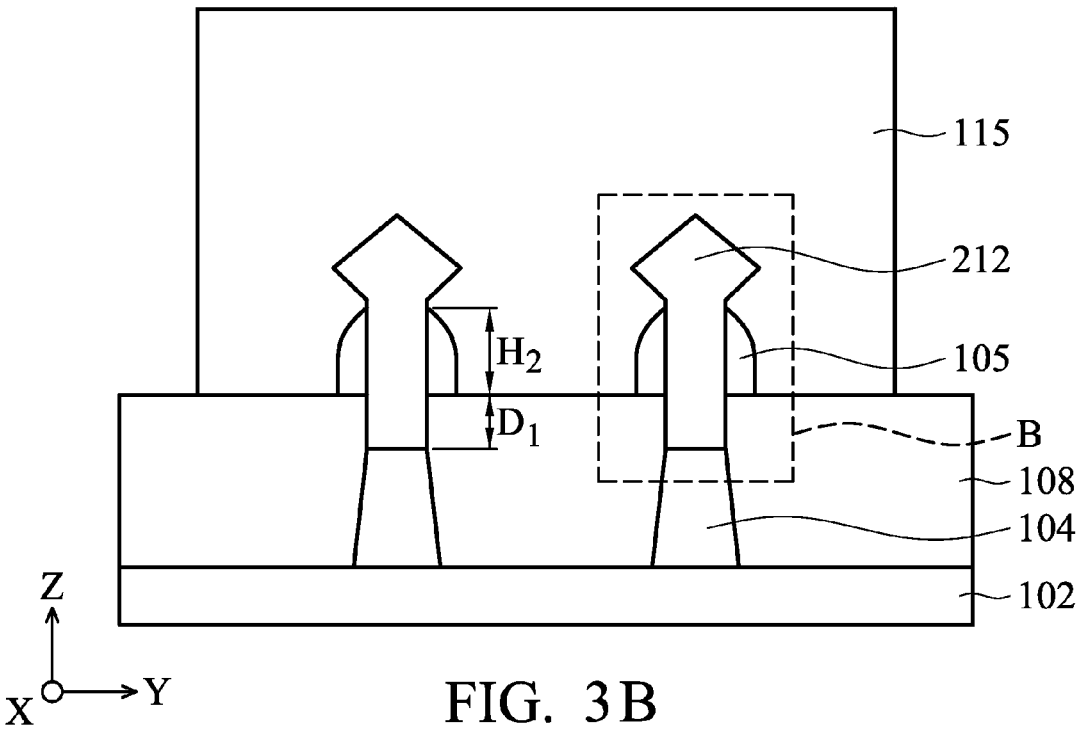
115
212
H2
105
D1
B
108
104
102
Z
X
Y

FIG. 3B

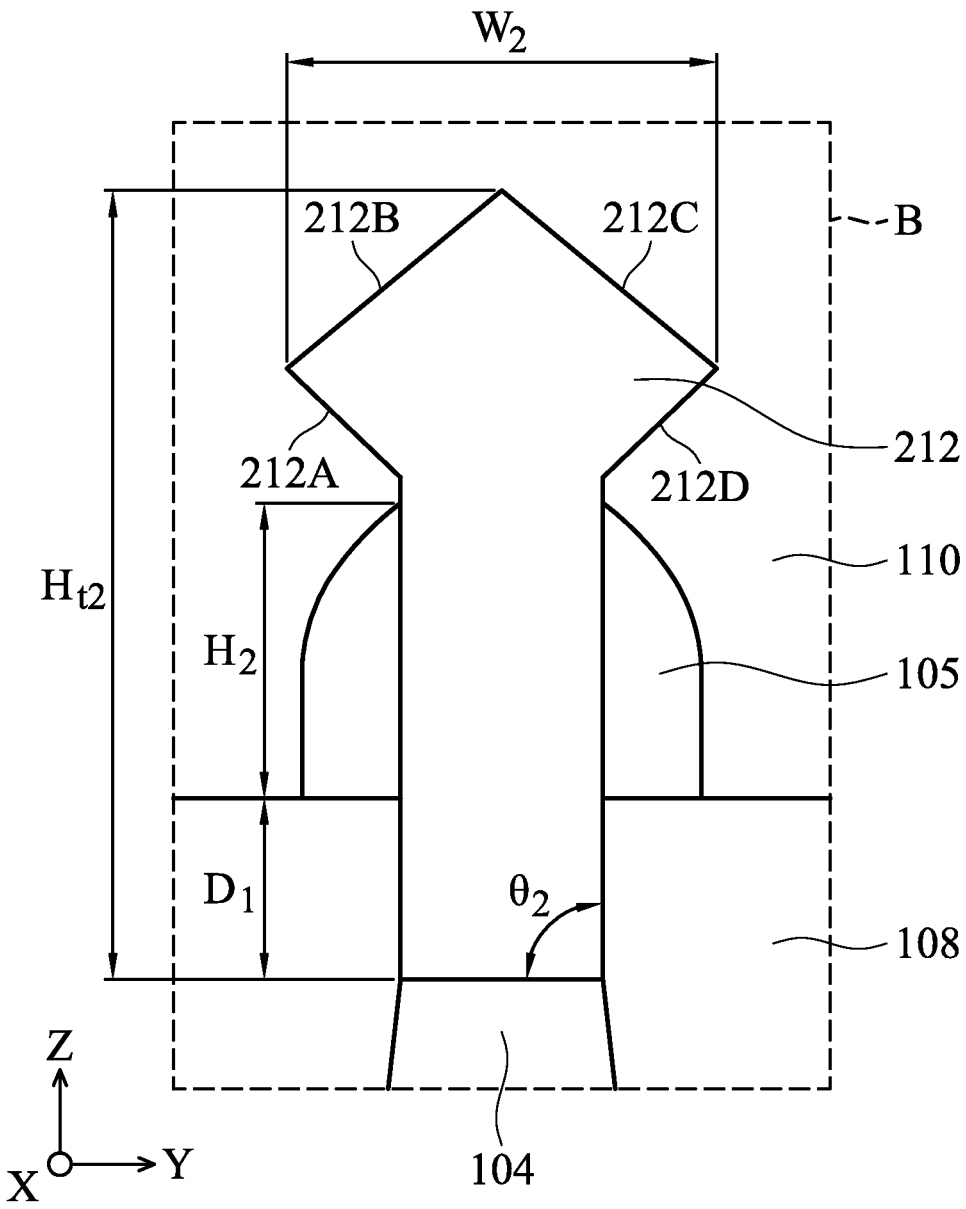

FIG. 3C

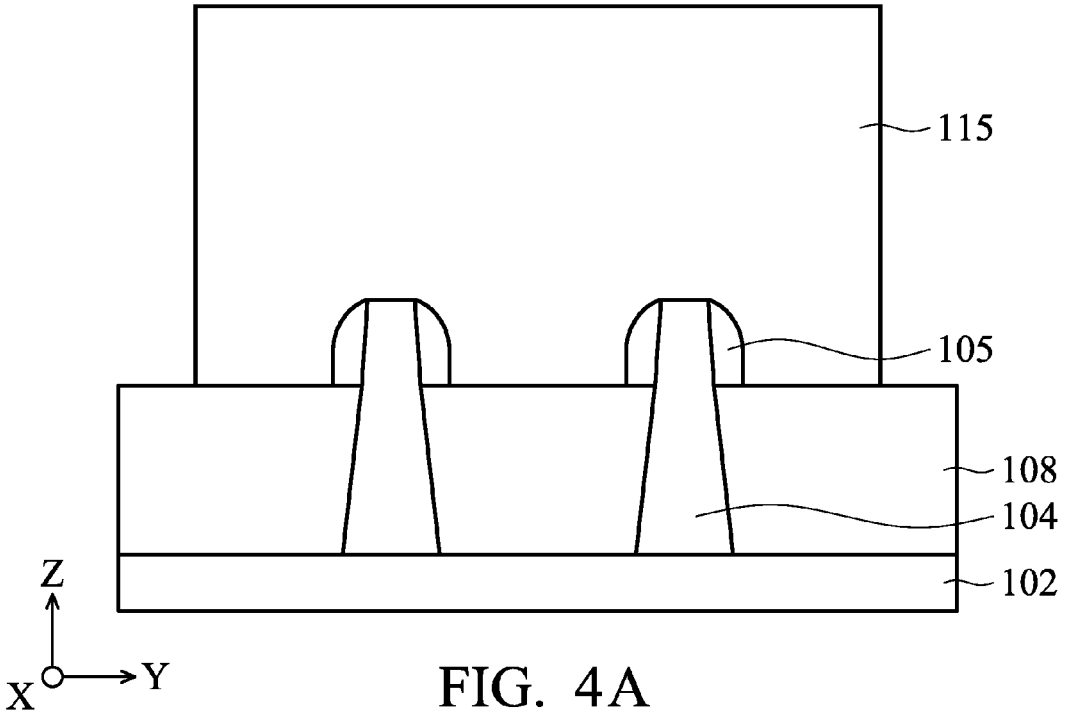

FIG. 4A

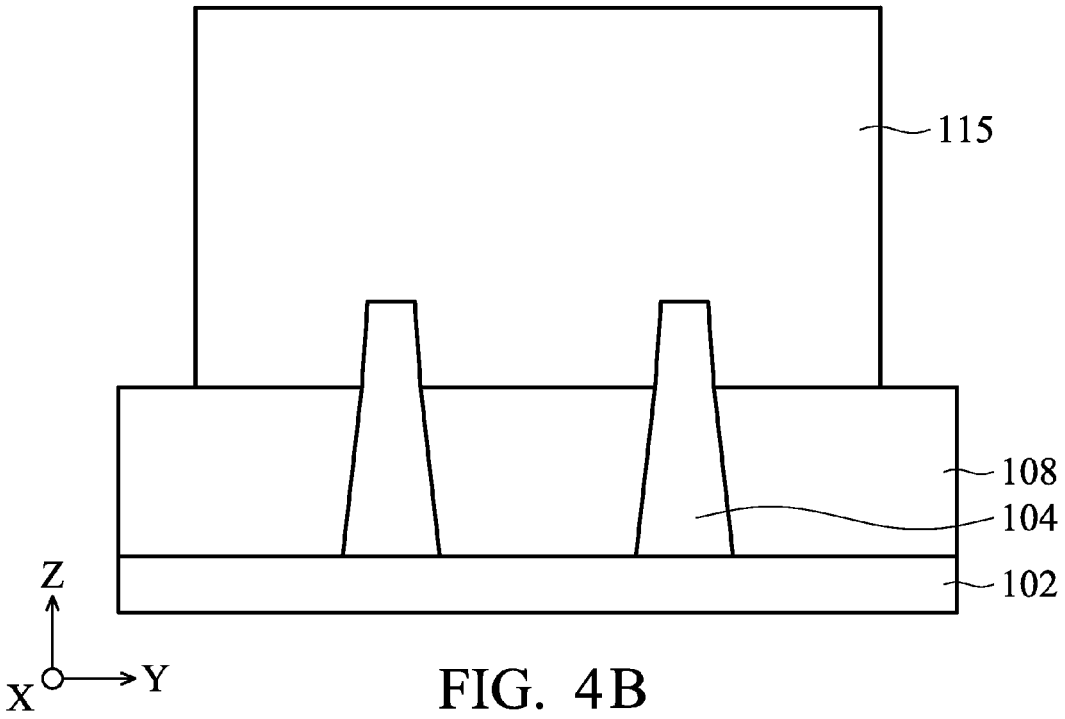

FIG. 4B

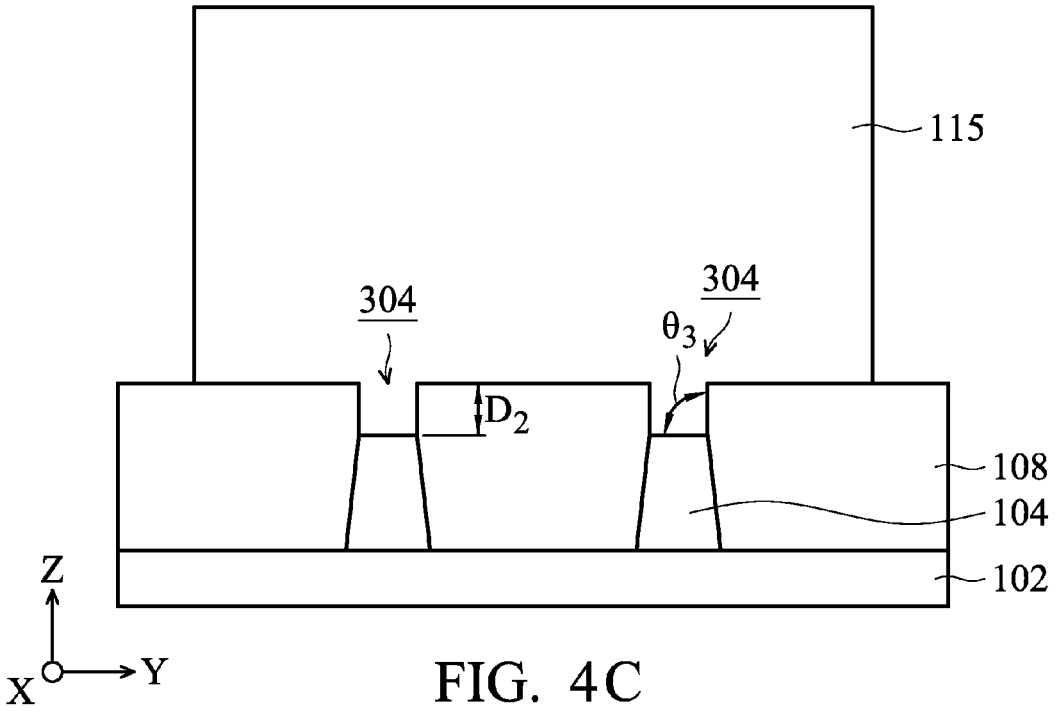

FIG. 4C

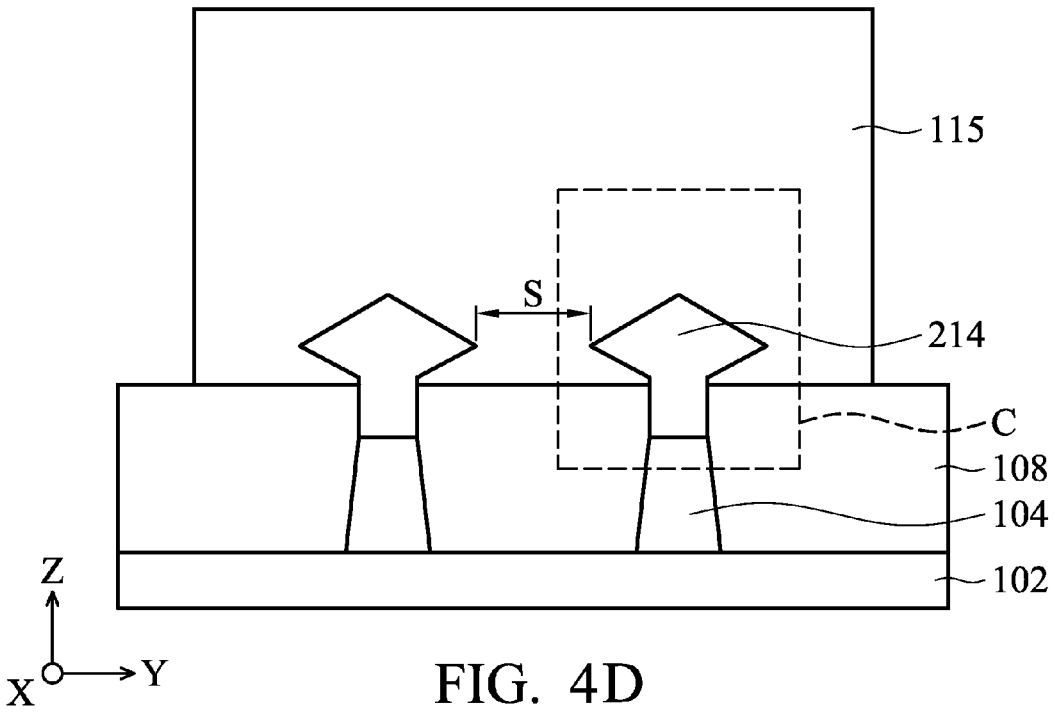

FIG. 4D

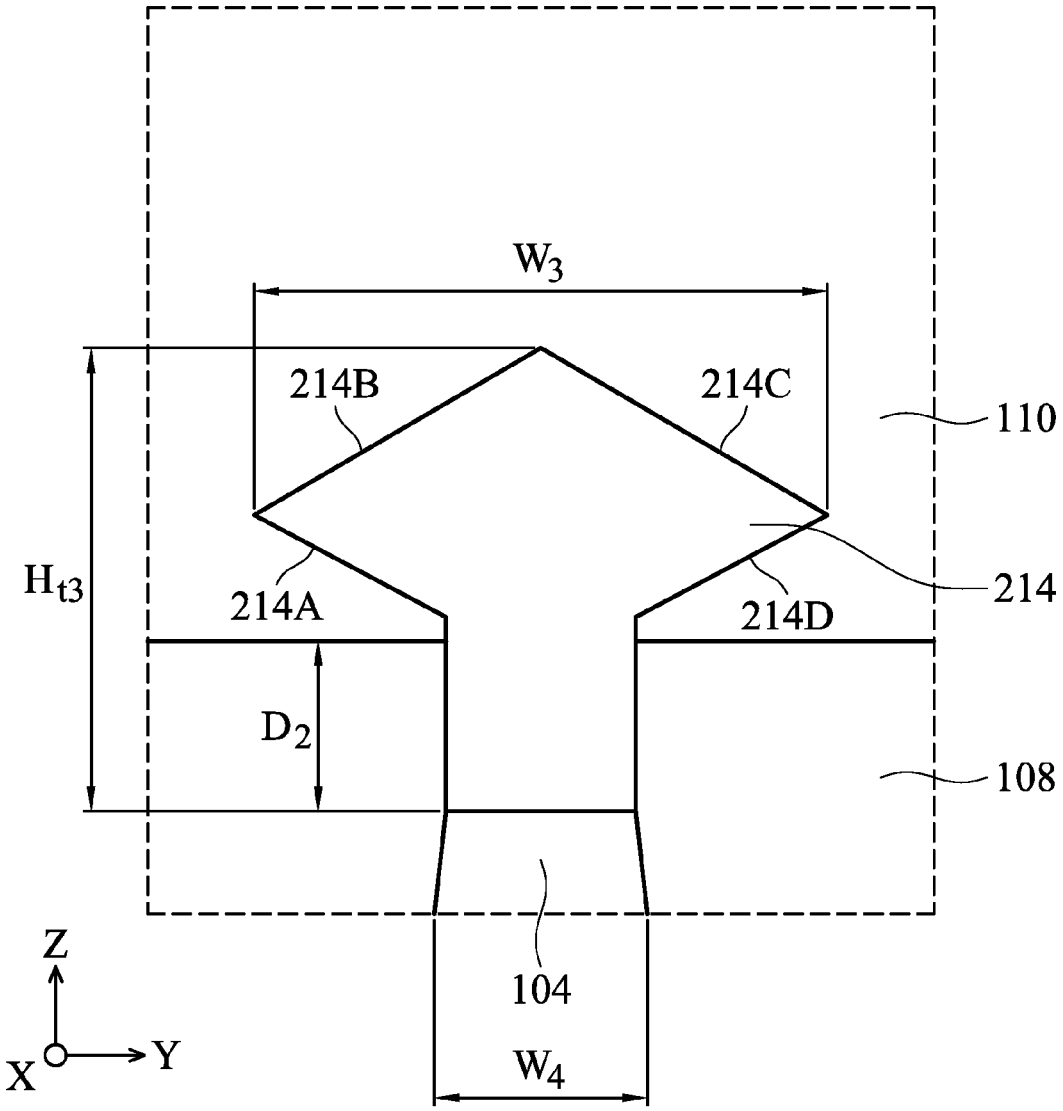

FIG. 4E

FIN FIELD EFFECT TRANSISTOR (FINFET) DEVICE AND METHOD FOR FORMING THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to the following co-pending an commonly assigned patent applications: U.S. patent application Ser. No. 14/517,209, filed on Oct. 17, 2014 and entitled "Fin field effect transistor (FinFET) device and method for forming the same", U.S. Patent Application No. 62/075,015, filed on Nov. 4, 2014 and entitled "Fin field effect transistor (FinFET) device and method for forming the same", and U.S. patent application Ser. No. 14/609,088, filed on Jan. 29, 2015 and entitled "Fin field effect transistor (FinFET) device and method for forming the same."

BACKGROUND

Semiconductor devices are used in a variety of electronic applications, such as personal computers, cell phones, digital cameras, and other electronic equipment. Semiconductor devices are typically fabricated by sequentially depositing insulating or dielectric layers, conductive layers, and semiconductive layers of material over a semiconductor substrate, and patterning the various material layers using lithography to form circuit components and elements thereon. Many integrated circuits are typically manufactured on a single semiconductor wafer, and individual dies on the wafer are singulated by sawing between the integrated circuits along a scribe line. The individual dies are typically packaged separately, in multi-chip modules, or in other types of packaging, for example.

As the semiconductor industry has progressed into nanometer technology process nodes in pursuit of higher device density, higher performance, and lower costs, challenges from both fabrication and design issues have resulted in the development of three-dimensional designs, such as the fin field effect transistor (FinFET). FinFETs are fabricated with a thin vertical "fin" (or fin structure) extending from a substrate. The channel of the FinFET is formed in this vertical fin. A gate is provided over the fin. Advantages of the FinFET may include reducing the short channel effect and higher current flow.

Although existing FinFET devices and methods of fabricating FinFET devices have been generally adequate for their intended purpose, they have not been entirely satisfactory in all aspects.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** shows a perspective representation of a fin field effect transistor (FinFET) device structure, in accordance with some embodiments of the disclosure.

FIGS. **2A-2F** show side views of various stages of forming a fin field effect transistor (FinFET) device structure, in accordance with some embodiments of the disclosure.

FIG. **2G** is an enlarged representation of region A of FIG. **2F**, in accordance with some embodiments of the disclosure.

FIGS. **3A-3B** show side views of various stages of forming a fin field effect transistor (FinFET) device structure, in accordance with some embodiments of the disclosure.

FIG. **3C** is an enlarged representation of region B of FIG. **3B**, in accordance with some embodiments of the disclosure.

FIGS. **4A-4D** show side views of various stages of forming a fin field effect transistor (FinFET) device structure, in accordance with some embodiments of the disclosure.

FIG. **4E** is an enlarged representation of region C of FIG. **4D**, in accordance with some embodiments of the disclosure.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Some variations of the embodiments are described. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. It is understood that additional operations can be provided before, during, and after the method, and some of the operations described can be replaced or eliminated for other embodiments of the method.

Embodiments for forming a fin field effect transistor (FinFET) device structure are provided. FIG. **1** shows a perspective representation of a fin field effect transistor (FinFET) device structure **10**, in accordance with some embodiments of the disclosure. The FinFET device structure **10** includes a N-type FinFET device structure (NMOS) **15** and a P-type FinFET device structure (PMOS) **25**.

The FinFET device structure **10** includes a substrate **102**. The substrate **102** may be made of silicon or other semiconductor materials. Alternatively or additionally, the substrate **102** may include other elementary semiconductor materials such as germanium. In some embodiments, the substrate **102** is made of a compound semiconductor such as silicon carbide, gallium arsenic, indium arsenide, or indium phosphide. In some embodiments, the substrate **102** is made of an alloy semiconductor such as silicon germanium, silicon germanium carbide, gallium arsenic phosphide, or gallium indium phosphide. In some embodiments, the substrate **102** includes an epitaxial layer. For example, the substrate **102** has an epitaxial layer overlying a bulk semiconductor.

The FinFET device structure **100** also includes one or more fin structure **104** (e.g., Si fins) that extend from the substrate **102**. The fin structure **104** may optionally include germanium (Ge). The fin structure **104** may be formed by using suitable processes such as photolithography and etching processes. In some embodiments, the fin structure **104** is etched from substrate **102** using dry etch or plasma processes.

In some other embodiments, the fin structure **104** can be formed by a double-patterning lithography (DPL) process. DPL is a method of constructing a pattern on a substrate by dividing the pattern into two interleaved patterns. DPL allows enhanced feature (e.g., fin) density.

An isolation structure **108**, such as a shallow trench isolation (STI) structure, is formed to surround the fin structure **104**. In some embodiments, a lower portion of the fin structure **104** is surrounded by the isolation structure **108**, and an upper portion of the fin structure **104** protrudes from the isolation structure **108**, as shown in FIG. **1**. In other words, a portion of the fin structure **104** is embedded in the isolation structure **108**. The isolation structure **108** prevents electrical interference or crosstalk.

The FinFET device structure **100** further includes a gate stack structure including a gate electrode **110** and a gate dielectric layer (not shown). The gate stack structure is formed over a central portion of the fin structure **104**. In some other embodiments, multiple gate stack structures are formed over the fin structure **104**.

In some other embodiments, the gate stack structure is a dummy gate stack and is replaced later by a metal gate (MG) after high thermal budget processes are performed.

The Gate dielectric layer (not shown) may include dielectric materials, such as silicon oxide, silicon nitride, silicon oxynitride, dielectric material(s) with high dielectric constant (high-k), or combinations thereof. Examples of high-k dielectric materials include hafnium oxide, zirconium oxide, aluminum oxide, hafnium dioxide-alumina alloy, hafnium silicon oxide, hafnium silicon oxynitride, hafnium tantalum oxide, hafnium titanium oxide, hafnium zirconium oxide, the like, or combinations thereof.

The gate electrode **110** may include polysilicon or metal. Metal includes tantalum nitride (TaN), nickel silicon (NiSi), cobalt silicon (CoSi), molybdenum (Mo), copper (Cu), tungsten (W), aluminum (Al), cobalt (Co), zirconium (Zr), platinum (Pt), or other applicable materials. Gate electrode **110** may be formed in a gate last process (or gate replacement process). In some embodiments, the gate stack structure includes additional layers, such as interfacial layers, capping layers, diffusion/barrier layers, or other applicable layers.

The gate stack structure is formed by a deposition process, a photolithography process and an etching process. The deposition process include chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), high density plasma CVD (HDPCVD), metal organic CVD (MOCVD), remote plasma CVD (RPCVD), plasma enhanced CVD (PECVD), plating, other suitable methods, and/or combinations thereof. The photolithography processes include photoresist coating (e.g., spin-on coating), soft baking, mask aligning, exposure, post-exposure baking, developing the photoresist, rinsing, drying (e.g., hard baking). The etching process includes a dry etching process or a wet etching process. Alternatively, the photolithography process is implemented or replaced by other proper methods such as maskless photolithography, electron-beam writing, and ion-beam writing.

FIGS. **2**A-**2**F show side views of various stages of forming a fin field effect transistor (FinFET) device structure, in accordance with some embodiments of the disclosure. FIGS. **2**A-**2**F show side views taken along arrow **1** of FIG. **1** and arrow **1** is parallel to the X-axis.

Referring to FIG. **2**A, a first hard mask layer **112** is formed on the gate electrode **110**, and a second hard mask layer **114** is formed on the first hard mask layer **112**. In some embodiments, the first hard mask layer **112** is made of silicon oxide, silicon nitride, silicon oxynitride, or other applicable materials. In some embodiments, the second hard mask layer **114** is made of silicon oxide, silicon nitride, silicon oxynitride, or other applicable materials.

Gate sidewall spacers **115** are formed on the opposite sidewalls of the gate electrode **110**, fin sidewall spacers **105** are formed on the opposite sidewalls of the fin structure **104**. Afterwards, a bottom anti-reflective coating (BARC) layer **202** is formed on the gate sidewall spacers **115**. The BARC layer **202** is used under a photoresist layer for enhancing pattern transfer to the hard mask layers **112**, **114** during a patterning process. In some embodiments, when an implantation process is performed on N-type FinFET device structure (NMOS) **15**, the BRAC **202** and a photoresist (not shown) which is formed on the BRAC **202** are formed on the gate electrode **110** to cover the gate electrode **110** in the P-type FinFET device structure (PMOS) **25**.

Afterwards, the photoresist (not shown) and BRAC **202** are removed by an etching process as shown in FIG. **2**B, in accordance with some embodiments of the disclosure. The etching process may be a dry etching process or a wet etching process. In some embodiments, a first dry etching process is operated at a pressure in a range from about 3 mtorr to about 50 mtorrr. In some embodiments, the gas used in the first dry etching process includes methane (CH_4), nitrogen (N_2), helium (He), oxygen (O_2) or combinations thereof. In some embodiments, the first dry etching process is operated by a power in a range from about 50 W to about 1000 W. In some embodiments, the first dry etching process is operated at a temperature in range from about 20° C. to about 80° C.

After the BRAC **202** is removed, a portion of the gate sidewall spacers **115** and a portion of the fin sidewall spacers **105** are removed as shown in FIG. **2**C, in accordance with some embodiments of the disclosure. More specifically, a top portion of the gate sidewall spacers **115** is removed to expose the second hard mask layer **114**. A top portion of the fin sidewall spacers **105** is removed to expose the fin structure **104**.

In some embodiments, when the gate sidewall spacers **115** and the fin sidewall spacers **105** are made of silicon nitride, a second etching process is performed to remove the silicon nitride. In some embodiments, the second etching process is a second dry etching process and is operated at a pressure in a range from about 3 mtorr to about 50 mtorrr. In some embodiments, the gas used in the second dry etching process includes fluoromethane (CH_3F), difluoromethane (CH_2F_2), methane (CH_4), argon (Ar), hydrogen bromide (HBr) nitrogen (N_2), helium (He), oxygen (O_2) or combinations thereof. In some embodiments, the second dry etching process is operated by a power in a range from about 50 W to about 1000 W. In some embodiments, the second dry etching process is operated at a temperature in range from about 20° C. to about 70° C.

After the second dry etching process, each of the fin sidewall spacers **105** has a first height H_1. In some embodiments, the first height H_1 is in a range from about 0.1 nm to about 100 nm.

After the portion of the gate sidewall spacers **115** and the portion of the fin sidewall spacers **105** are removed, a portion of the remaining fin sidewall spacers **105** is removed as shown in FIG. **2**D, in accordance with some embodiments of the disclosure. The upper portions of the fin sidewall spacers **105** are removed by a third etching process. The third etching process may be a dry etching process or a wet etching process.

In some embodiments, the third etching process is a third dry etching process and is operated at a pressure in a range from about 3 mtorr to about 50 mtorrr. In some embodiments, the gas used in the third dry etching process includes fluoromethane (CH_3F), difluoromethane (CH_2F_2), methane (CH_4), argon (Ar), hydrogen bromide (HBr) nitrogen (N_2), helium (He) or oxygen (O_2) or combinations thereof. In some embodiments, the third dry etching process is operated by a power in a range from about 50 W to about 1000 W. In some embodiments, the third dry etching process is operated at a temperature in range from about 20° C. to about 70° C.

After the third dry etching process, the height of the fin sidewall spacers **105** is reduced from the first height H_1 to a second height H_2. In some embodiments, the second height H_2 is in a range from about 0.1 nm to about 90 nm.

It should be noted that the second height H**2** of the fin sidewall spacers **105** is critical to an epitaxial structure (such as epitaxial structure **210** in FIG. **2**F). The height and volume of the epitaxial structure are affected by the second height H**2** of the fin sidewall spacers **105**. In other words, the fin sidewall spacers **105** are configured to control the volume and the height of the epitaxial structure **210**.

After the third dry etching process, a portion of the fin structure **104** is removed as shown in FIG. **2**E, in accordance with some embodiments of the disclosure. The fin structure **104** is removed by an etching process, such as a dry etching process or a wet etching process.

As shown in FIG. **2**E, a top surface of the remaining fin structure **104** is level with a top surface of the isolation structure **108**. A trench **204***a* is formed by recessing a portion of the fin structure **104** which is located above the isolation structure **108**. The sidewalls of the trench **204***a* are vertical parallel to each other. In some embodiments, an angle θ_1 between the sidewall of trench **204***a* and a top surface of the fin structure **104** is about 90 degrees.

After the portion of the fin structure **104** is removed, an epitaxial structure **210** is formed in the trenches **204***a*, as shown in FIG. **2**F, in accordance with some embodiments of the disclosure

The epitaxial structure **210** includes source/drain epitaxial structure. In some embodiments, when an N-type FET (NFET) device is desired, the source/drain epitaxial structures include an epitaxially growing silicon (epi Si) Alternatively when a P-type FET (PFET) device is desired, epitaxial source/drain structures include an epitaxially growing silicon germanium (SiGe).

FIG. **2**G is an enlarged representation of region A of FIG. **2**F, in accordance with some embodiments of the disclosure. As shown in FIG. **2**G, the epitaxial structure **210** has a rhombus-like upper portion and a column-like lower portion. The rhombus-like upper portion of the epitaxial structure **210** has four facets **210**A, **210**B, **210**C and **210**D. Each facet has a (111) crystallographic orientation. The column-like lower portion of the epitaxial structure **210** has a bottom surface and sidewalls adjoined to the bottom surface. An angle θ_1 between the bottom surface and the sidewalls is about 90 degrees. In addition, the bottom surface of the column-like lower portion of the epitaxial structure **210** is substantially level with a top surface of the isolation structure **108**.

As shown in FIG. **2**G, the epitaxial structure **210** has a height H_{t1} and a width W_1. In some embodiments, the height H_{t1} is in a range from about 10 nm to about 300 nm. If the height H_{t1} is too great, the electric resistance will become lower. If the height H_{t1} is too small, the electric resistance becomes higher to impact device speed. In some embodiments, the width W_1 is in a range from about 10 nm to about 100 nm. If the width W_1 is too great, the epitaxial structure **210** may merge with neighbor one and cause short circuit effect. If the width W_1 is too small, a contact window for contacting with the epitaxial structure **210** will become narrow, and therefore the circuit effect may be broken.

In addition, a ratio (H_{t1}/H_2) of the height H_{t1} of the epitaxial structure **210** to height H_2 of the fin sidewall spacers **105** is in a range from about 1.5 to about 10. If the ratio is too small, fin sidewall can't have effective support to EPI height and cause short EPI structure.

FIGS. **3**A-**3**B show side views of various stages of forming a fin field effect transistor (FinFET) device structure, in accordance with some embodiments of the disclosure.

As shown in FIG. **3**A, in some embodiments, a top surface of the remaining fin structure **104** is lower than a top surface of the isolation structure **108**. A trench **204***b* is formed by recessing a portion of the fin structure **104** which is located below the isolation structure **108**. In some other embodiments, an angle θ_2 between the sidewall of trench **204***b* and a top surface of the fin structure **104** is about 90 degrees. The trench **204***b* extends from a top surface of the isolation structure **108** to a depth D_1 in a range from about 0.1 nm to about 50 nm.

After the portion of the fin structure **104** is removed, an epitaxial structure **212** is formed in the trenches **204***b*, as shown in FIG. **3**B, in accordance with some embodiments of the disclosure. The epitaxial structure **212** includes source/drain epitaxial structure. In some embodiments, when an N-type FET (NFET) device is desired, the source/drain epitaxial structures include an epitaxially growing silicon (epi Si). Alternatively, when a P-type FET (PFET) device is desired, epitaxial source/drain structures include an epitaxially growing silicon germanium (SiGe).

FIG. **3**C is an enlarged representation of region B of FIG. **3**B, in accordance with some embodiments of the disclosure. As shown in FIG. **3**C, the epitaxial structure **212** has a rhombus-like upper portion and a column-like lower portion. The rhombus-like upper portion of the epitaxial structure **212** has four facets **212**A, **212**B, **212**C and **212**D. Each facet has a (111) crystallographic orientation. The column-like lower portion of the epitaxial structure **212** has a bottom surface and sidewalls adjoined to the bottom surface. An angle θ_2 between the bottom surface and the sidewalls is about 90 degrees. In addition, the bottom surface of the column-like lower portion of the epitaxial structure **212** is lower than a top surface of the isolation structure **108**.

As shown in FIG. **3**C, the epitaxial structure **212** has a height H_{t2} and a width W_2. The height H_{t1} is smaller than height H_{t2}, and the width W_1 is greater than width W_2. In some embodiments, the height H_{t2} is in a range from 15 nm to about 150 nm. In some embodiments, the width W_2 is in a range from about 10 nm to about 100 nm.

The epitaxial structures **210** and an epitaxial structure **212** independently include single element semiconductor material such as germanium (Ge) or silicon (Si); or compound semiconductor materials, such as gallium arsenide (GaAs), aluminum gallium arsenide (AlGaAs); or semiconductor alloy, such as silicon germanium (SiGe), gallium arsenide phosphide (GaAsP).

The epitaxial structures **210** and **212** are formed by an epi process. The epi process may include a selective epitaxial growth (SEG) process, CVD deposition techniques (e.g., vapor-phase epitaxy (VPE) and/or ultra-high vacuum CVD (UHV-CVD)), molecular beam epitaxy, or other applicable epi processes.

The epitaxial structures **210** and **212** may be doped or undoped in-situ during the epi process. For example, the epitaxially grown SiGe epitaxial structure may be doped with boron; and the epitaxially grown Si epitaxial structure may be doped with carbon to form a Si:C epitaxial structure, phosphorous to form a Si:P epitaxial structure, or both carbon and phosphorous to form a SiCP epitaxial structure. The doping may be achieved by an ion implantation process, plasma immersion ion implantation (PIII) process, gas and/or solid source diffusion process, or another suitable process. The epitaxial structures **210** and **212** may further be exposed to annealing processes, such as a rapid thermal annealing process.

If the epitaxial structures **210** and **212** are not doped in-situ, a second implantation process (i.e., a junction implant process) is performed to dope the epitaxial structure **210** and **212**.

The fin structure **104** includes a channel region (not shown) surrounded or wrapped by gate electrode **110**. The lattice constants of the epitaxial structure **210** and **212** are different from the substrate **102**, the channel region are stained or stressed to enable carrier mobility of the FinFET device structure and enhance the FinFET device structure performance.

It should be noted that the volume and the heights H_{t1}, H_{t2} of the epitaxial structure **210** and **212** are controlled by adjusting the height H_2 of the fin sidewall spacers **105** and/or depth D_1. Once the volume and the heights H_{t1}, H_{t2} of the epitaxial structure **210** and **212** are well controlled, the performance of the FinFET device structure is further improved. For example, the device mobility (Id_Sat) will gain when the FinFET device structure is improved.

FIGS. **4**A-**4**D show side views of various stages of forming a fin field effect transistor (FinFET) device structure, in accordance with some embodiments of the disclosure. FIG. **4**E is an enlarged representation of region C of FIG. **4**D, in accordance with some embodiments of the disclosure. FIGS. **4**A-**4**D show side views taken along arrow **1** of FIG. **1** and the arrow **1** is parallel to X-axis direction.

Referring to FIG. **4**A, the gate sidewall spacers **115** are formed on the opposite sidewalls of the gate electrode **110**, the fin sidewall spacers **105** are formed on the opposite sidewalls of the fin strutcure **104**.

Afterwards, the fin sidewall spacers **105** are completely removed as shown in FIG. **4**B, in accordance with some embodiments of the disclosure. As a result, the top surface and a portion of the sidewalls of the fin structure **104** are exposed. No fin sidewall spacers **105** are formed on the fin structure **104**.

After the fin sidewall spacers **105** are completely removed, a portion of the fin structure **104** is removed as shown in FIG. **4**C, in accordance with some embodiments of the disclosure. As a result, a trench **304** is formed by recessing a portion of the fin structure **104**.

The trench **304** has a depth D_2 which is below the isolation structure **108**. In some embodiments, the depth D_2 is in a range from about 0.1 nm to about 50 nm. In some embodiments, an angle θ_3 between the sidewall of trench **304** and a top surface of the fin structure **104** is about 90 degrees.

After the portion of the fin structure **104** is removed, an epitaxial structure **214** is formed in the trench **304** and on the fin structure **104** as shown in FIG. **4**D, in accordance with some embodiments of the disclosure.

The epitaxial structure **214** includes single element semiconductor material such as germanium (Ge) or silicon (Si); or compound semiconductor materials, such as gallium arsenide (GaAs) or aluminum gallium arsenide (AlGaAs); or semiconductor alloy, such as silicon germanium (SiGe) or gallium arsenide phosphide (GaAsP).

The epitaxial structure **214** is formed by an epi process. The epi process may include a selective epitaxial growth (SEG) process, CVD deposition techniques (e.g., vapor-phase epitaxy (VPE) and/or ultra-high vacuum CVD (UHV-CVD)), molecular beam epitaxy, or other suitable epi processes.

Like epitaxial structure **210** and **212**, the epitaxial structure **214** has a rhombus-like upper portion and a column-like lower portion. The rhombus-like upper portion of the epitaxial structure **214** has four facets **214**A, **214**B, **214**C and **214**D. Each facet has a (111) crystallographic orientation.

It should be noted that, compared with FIGS. **2**G and **3**C, no fin sidewall spacers are formed adjacent to the epitaxial structure **214** in FIG. **4**E. Therefore, the volume and the height of the epitaxial structure **214** are controlled by adjusting the depth of the trench **304** (shown in FIG. **4**C). In addition, because no fin sidewall spacers inhibit the growth of the epitaxial structure **214**, the epitaxial structure **214** is prone to growing in the direction of the X-axis. Therefore, the width W_3 of the epitaxial structure **214** is greater than the width W_4 of the fin structure **104**.

The epitaxial structure **214** has a height H_{t3} and a width W_3. The height H_{t3} of the epitaxial structure **214** is less than height H_{t2} of the epitaxial structure **212**, and the width W_2 of the epitaxial structure **212** is greater than width W_3 of the epitaxial structure **214**. In addition, the height H_{t3} of the epitaxial structure **214** is less than height H_{t1} of the epitaxial structure **210**, and the width W_1 of the epitaxial structure **210** is greater than width W_3 of the epitaxial structure **214**.

Referring to FIG. **4**D again, a spacing S between two adjacent epitaxial structure **214** is in a range from about 0.1 nm to about 100 nm. In some embodiments, the width W_3 of the epitaxial structure **214** is in a range from about 10 nm to about 100 nm. In some embodiments, the height H_{t3} of the epitaxial structure **214** is in a range from about 10 nm to about 300 nm. In some embodiments, the ratio (H_{t3}/W_3) of the height to the width of the epitaxial structure **214** is in a range from about 0.1 to about 10.

Afterwards, The FinFET device structure may continue to undergo other processes to form other structures or devices. In some embodiments, metallization includes vertical interconnects, such as conventional vias or contacts, and horizontal interconnects, such as metal lines. The various interconnection features may implement various conductive materials including copper, tungsten, and/or silicide.

Embodiments for forming fin field effect transistor (FinFET) device structure are provided. The FinFET device structure includes a fin structure extending above the substrate and an epitaxial structure formed on the fin structure. In some embodiments, the fin sidewall spacers are formed adjacent to the epitaxial structure. The fin sidewall spacers are configured to control a volume and the height of the epitaxial structure. In some other embodiments, no fin sidewall spacers are formed adjacent to the epitaxial structure, the volume and the height of the epitaxial structure are controlled by adjusting the depth of a trench which is formed by recessing a top portion of the fin structure. Once the volume and the height of the epitaxial structure are controlled, the performance of the FinFET device structure is further improved.

In some embodiments, a fin field effect transistor (FinFET) device structure is provided. The FinFET structure includes a substrate and a fin structure extending above the substrate. The FinFET structure includes an epitaxial struc-

ture formed on the fin structure, and the epitaxial structure has a first height. The FinFET structure also includes fin sidewall spacers formed adjacent to the epitaxial structure. The sidewall spacers have a second height and the first height is greater than the second height, and the fin sidewall spacers are configured to control a volume and the first height of the epitaxial structure.

In some embodiments, a fin field effect transistor (FinFET) device structure is provided. The FinFET structure includes a substrate and a fin structure extending above the substrate. The FinFET structure also includes an isolation structure formed on the substrate, and the fin structure is embedded in the isolation structure. The FinFET structure further includes a first epitaxial structure formed on the fin structure, an interface between the first epitaxial structure and the fin structure is below a top surface of the isolation structure, and no fin sidewall spacers are formed adjacent to the first epitaxial structure.

In some embodiments, a method for forming a fin field effect transistor (FinFET) device structure is provided. The method includes providing a substrate and forming a fin structure above the substrate. The method also includes forming a gate stack structure over a central portion of the fin structure and forming gate sidewall spacers on a top surface and sidewalls of the gate stack structure and forming fin sidewall spacers on a top surface and sidewalls the fin structure. The method further includes removing a top portion of gate sidewall spacers and a top portion of the fin sidewall spacers to expose a top portion of the gate stack structure and a top portion of the fin structure. The method includes removing a portion of the fin sidewall spacers, and the fin sidewall spacers have a second height. The method further includes recessing a portion of the fin structure to form a trench. The method also includes epitaxially growing a epitaxial structure from the trench, and the epitaxial structure is formed over the fin structure, and the epitaxial structure has a first height and the first height is greater than the second height.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A fin field effect transistor (FinFET) device structure, comprising:

a substrate;

a fin structure extending above the substrate;

an epitaxial structure formed on the fin structure, wherein the epitaxial structure has a first height, and the epitaxial structure comprises a rhombus-like upper portion and a column-like lower portion;

fin sidewall spacers formed adjacent to the epitaxial structure, wherein the fin sidewall spacers have a second height and the first height is greater than the second height, and wherein the rhombus-like upper portion is entirely above a top of the fin sidewall spacers, and a junction between the rhombus-like upper portion and the sidewall of the column-like lower portion is higher than a peak of the fin sidewall spacers, and a bottom surface of the column-like lower portion is leveled with a bottom surface of the fin sidewall spacers.

2. The fin field effect transistor (FinFET) device structure as claimed in claim **1**, further comprising:

a gate stack structure is formed over a central portion of the fin structure, wherein the epitaxial structure formed adjacent to the central portion of the fin structure.

3. The fin field effect transistor (FinFET) device structure as claimed in claim **1**, wherein the second height is in a range from about 0.1 nm to about 100 nm.

4. The fin field effect transistor (FinFET) device structure as claimed in claim **1**, further comprising:

an isolation structure, wherein the fin structure is embedded in the isolation structure.

5. The fin field effect transistor (FinFET) device structure as claimed in claim **4**, wherein a bottom surface of the epitaxial structure is level with a top surface of the isolation structure.

6. The fin field effect transistor (FinFET) device structure as claimed in claim **1**, wherein the epitaxial structure extends from the top surface of the isolation structure to a depth in a range from about 0.1 nm to about 50 nm.

7. The fin field effect transistor (FinFET) device structure as claimed m claim **1**, wherein the epitaxial structure comprises a source/drain structure.

8. The fin field effect transistor (FinFET) device structure as claimed in claim **1**, wherein the column-like lower portion has a bottom surface and sidewalls adjoined to the bottom surface and an angle between the bottom surface and the sidewalls is about 90 degrees.

9. A fin field effect transistor (FinFET) device structure, comprising:

a substrate;

a fin structure extending above the substrate;

an isolation structure formed on the substrate, wherein the fin structure is embedded in the isolation structure;

a first epitaxial structure formed on the fin structure, wherein the first epitaxial structure comprises a rhombus-like upper portion and a column-like lower portion, the column-like lower portion has a bottom surface and a sidewall adjoined to the bottom surface, an angle between the bottom surface and the sidewall is about 90 degrees, a junction between the rhombus-like upper portion and the sidewall of the column-like lower portion is above the top surface of the isolation structure such that the rhombus-like upper portion is entirely located above the top surface of the isolation structure; and

fin sidewall spacers formed adjacent to the first epitaxial structure, wherein a peak of the fin sidewall spacers is higher than a bottom surface of the column-like lower portion and lower than the junction.

10. The fin field effect transistor (FinFET) device structure as claimed in claim **9**, wherein the first epitaxial structure extends from the top surface of the isolation structure to a depth in a range from about 0.1 nm to about 50 nm.

11. The fin field effect transistor (FinFET) device structure as claimed in claim **9**, further comprising:

a gate stack structure is formed over a central portion of the fin structure; and gate sidewall spacers formed adjacent to the gate stack structure.

12. The fin field effect transistor (FinFET) device structure as claimed in claim **9**, further comprising:

a second epitaxial structure adjacent to the first epitaxial structure, wherein a spacing between the first epitaxial structure and the second epitaxial structure is in a range from about 0.1 nm to about 100 nm.

13. The fin field effect transistor (FinFET) device structure as claimed in claim **9**, wherein the rhombus-like upper portion has four facets, each of the four facets has a (111) crystallographic orientation, two of the four facets joining the sidewall of the column-like lower portion, and the four facets are entirely located above the top surface of the isolation structure.

14. The fin field effect transistor (FinFET) device structure as claimed in claim **9**, wherein the fin structure has a first width, the first epitaxial structure has a second width and the second width is greater than the first width.

15. The fin field effect transistor (FinFET) device structure as claimed in claim **1**, wherein the first height is in a range from about 10 nm to about 300 nm, and the epitaxial structure has a first width in a range from about 10 nm to about 100 nm.

16. The fin field effect transistor (FinFET) device structure as claimed in claim **1**, wherein a ratio of the first height to the second height is in a range from about 1.5 to about 10.

17. The fin field effect transistor (FinFET) device structure as claimed in claim **1**, wherein the lattice constants of the epitaxial structure are different from that of the substrate.

18. The fin field effect transistor (FinFET) device structure as claimed in claim **9**, wherein the first epitaxial structure has a height in a range from about 10 nm to about 300 nm and a width in a range from about 10 nm to about 100 nm.

19. The fin field effect transistor (FinFET) device structure as claimed in claim **9**, wherein a ratio of the height to the width of the first epitaxial structure is in a range from about 0.1 to about 10.

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