

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-01265
U.S. Patent No. 8,993,384 B2

**DECLARATION OF JOSEPH C. MCALEXANDER III REGARDING
PATENT OWNER'S PRELIMINARY RESPONSE FOR *INTER PARTES*
REVIEW OF U.S. PATENT NO. 8,993,384**

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TABLE OF EXHIBITS

Exhibit	Description
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4 th ed. 2000)
2003	<i>Curriculum Vitae</i> of Joseph C. McAlexander III
2101	Website: Foundries to Grow Faster than Integrated Circuits in 2016 (https://marketrealist.com/2015/12/foundries-grow-faster-integrated-circuits-2016/)
2102	Website: Ranked: Semiconductor Foundries by Revenue Share (www.visualcapitalist.com/ranked-semiconductor-foundries-by-revenue-share/)
2103	Website: US Patent No. 8,993,384 B2 – Semiconductor device and fabrication method thereof – Google Patents (https://patents.google.com/patent/US8993384B2/en?q=8993384#citedBy)
2104	Declaration of Paul Ahern Regarding Patent Owner’s Request for Discretionary Denial of Institution

I. Qualifications

1. I am a Registered Professional Engineer (#79454) and the President of M^cAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 53 years and am a named inventor on 31 U.S. patents and a number of foreign patents, many of which are directly related to the design and operation of transistors and circuits incorporating transistors, including control, addressing, comparing and sensing, and fabrication.

2. My skills and experience are in areas of circuit design and analysis, device and board fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing,

- analysis, and control involved use of mechanical calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;
- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
 - provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and
 - designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

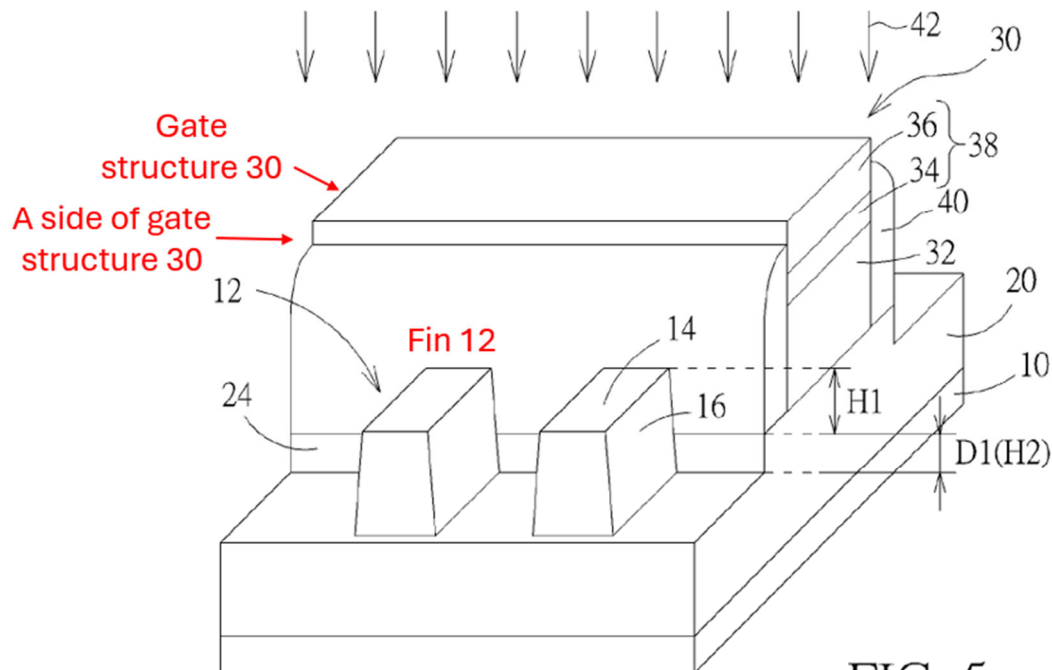
3. Because of my background, training, and experience, I am qualified as an expert to opine on the challenged patent. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, which is submitted as Exhibit 2003.

II. Overview

4. Each of the two asserted grounds in the Petition fails to disclose multiple limitations of the challenged claims of U.S. Patent Number 8,993,384 (“the ’384 patent”).

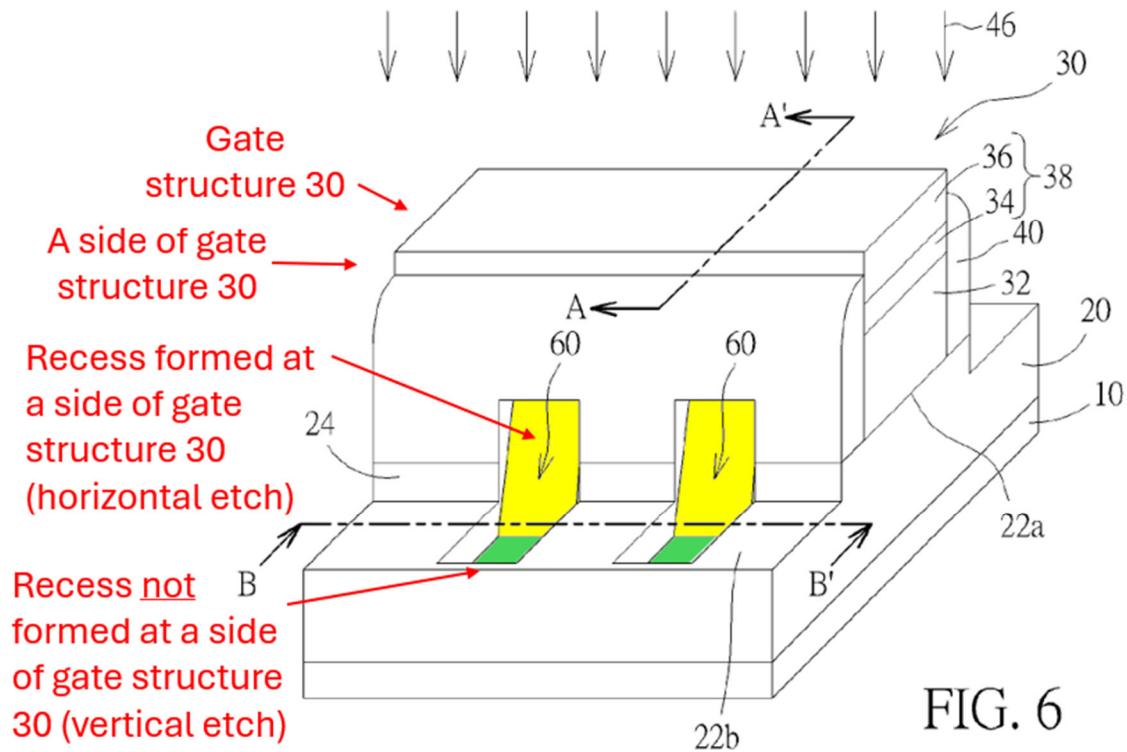
5. For example, the claims recite a transistor fabrication method in which a recess is formed in a “fin structure” specifically “at a side of the gate structure.” The side of the gate structure is a vertical wall, as shown below, and so, as the patent explains, to form the recess in the “at a side of the gate structure” means to etch the fin structure horizontally, *e.g.*, to etch the fin structures 12 horizontally into the spacers 40 toward the gate structure 30. Ex. 1001, 5:55-60. As clearly evidenced by Figures 5 and 6 below, horizontal etching occurs through the sidewall spacers 40 toward the vertical sides of the gate structure 30, thus creating a recess 60:

Before recess is created in the fin:



Ex. 1001, Fig. 5 (annotated).

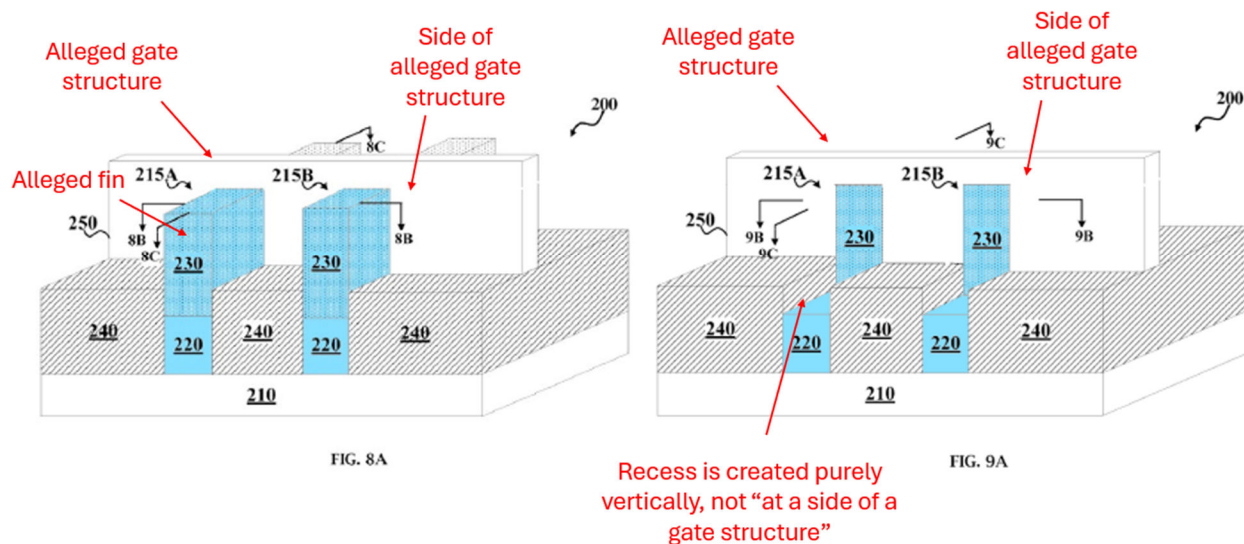
After recess is created in the fin:



Ex. 1001, Fig. 6 (annotated).

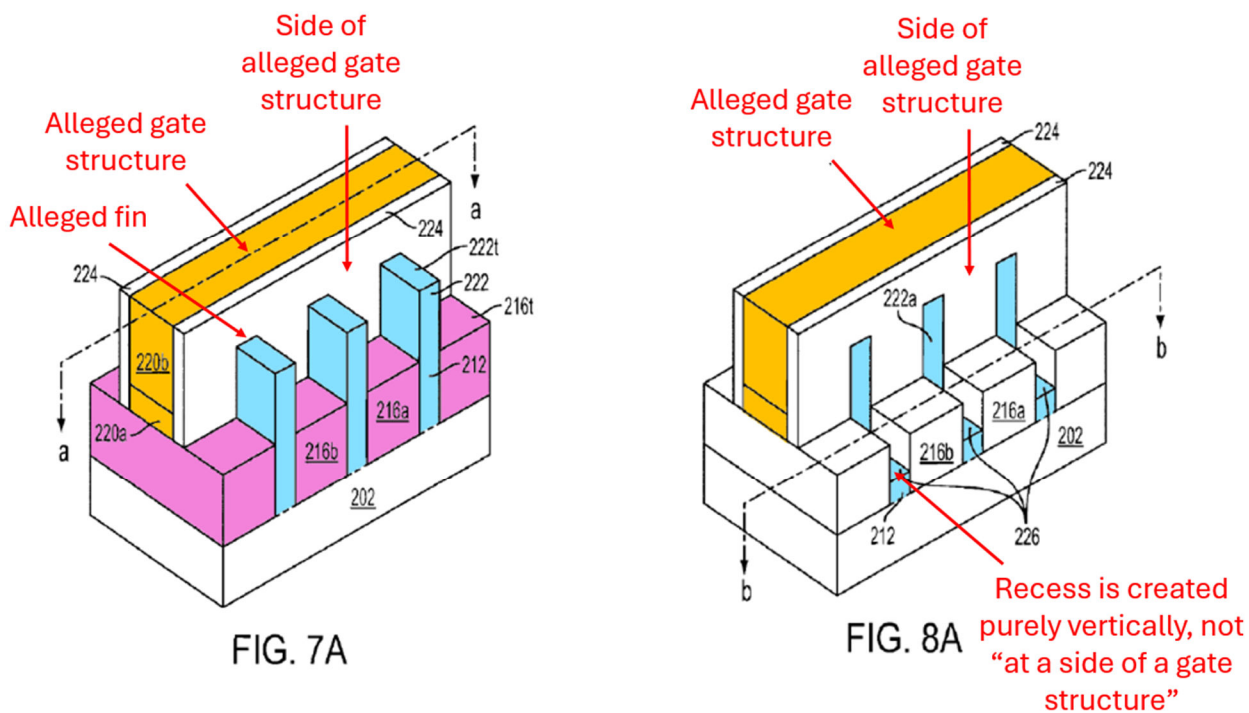
6. None of the asserted prior art forms a recess at the side of the gate structure. The prior art forms exclusively a vertical recess, without the required horizontal component being created:

Xu (Ground 1):



Ex. 1004, Figs. 8A and 9A (annotated).

Lin (Ground 2):



Ex. 1005, Figs. 8A and 9A (annotated).

7. Further, Xu (Ground 1) fails to describe etching both the isolation structure (item 20 in the '384 patent figures above) and forming a recess in the fins. Instead, it describes two embodiments. As explained below, the two methods are incompatible with one another in Xu, and a POSITA would not perform both steps, as required by the claims. Even if one were to perform both steps, in the hypothetical created by Petitioner, there is no reason that one etch would be lower than the other, as required by the claims, which require that the recess in the fins be formed to a lower depth than that to which the isolation structure was etched. The Petition relies on two separate embodiments, with no relationship to one another, and no reason why one etch would be lower than the other.

III. Materials Considered

8. In preparing this declaration, I have reviewed the Petition and the declaration of Petitioner's expert, as well as the materials that they cite, including the asserted prior art.

IV. Understanding Of The Law

9. In preparing and expressing my opinions and considering the subject matter of the challenged patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

A. Claim Construction

10. I understand that the scope of a patent is defined by its claims. I understand that a claim can be:

- a. a method claim, which covers a process/activity, or
- b. an apparatus claim, which covers a physical machine, etc.

11. I understand that the first step in determining the validity of a claim is for the claim to be properly construed. I have been further advised that, in an inter partes review proceeding, the claims of a patent are typically given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the claims and the patent disclosure (specification).

12. I further understand that an inventor can provide special definitions for specific claim term(s) within the patent. However, any special definition for a claim term must be set forth in the specification with reasonable clarity and precision.

B. Invalidity

13. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim, as a whole, would have been obvious to a POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an inter partes review proceeding is by a preponderance of the evidence.

14. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in the art. I have been informed and understand that a prior art reference should be viewed as a whole.

15. I have been informed that in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious.

16. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one is to consider certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that for such objective evidence to be relevant to the non-obviousness of claim, however, there must be a causal relationship (called a

“nexus”) between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

17. I have also been informed and understand that, when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that the prior art must create a reasonable expectation of success in producing the claimed subject matter.

V. Semiconductor Transistor Technology Primer

18. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (*e.g.*, fin) transistors; and (3) common process steps for creating transistors.

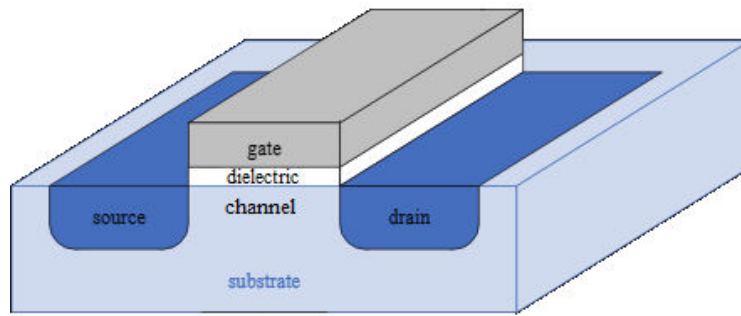
A. Basic Transistor Components

19. Today’s semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). Ex. 2002 at 1-2. Where earlier tube devices used a vacuum to

control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. Ex. 2002 at 3.

20. One type of transistor typically used in an integrated circuit (or “chip”) is a “field effect transistor,” or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. Ex. 2002 at 29-34. In a conductor (*e.g.*, a metal), electric current can flow freely. Ex. 2002 at 29. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. Ex. 2002 at 30. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. Ex. 2002 at 31-34.

21. The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See, e.g.*, Ex. 2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.

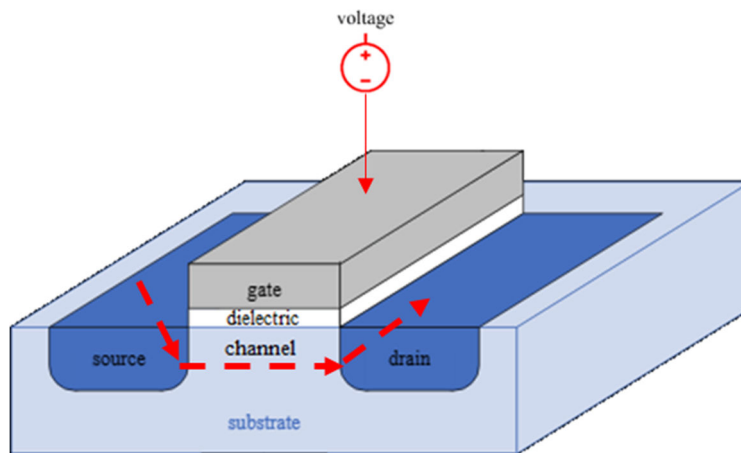


See, e.g., Ex. 2002 at 510-511.

22. The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). Ex. 2002 at 26-28, 427-28. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). Ex. 2002 at 510-511.

23. The gate is a conductor located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. Ex. 2002 at 510-511. When a voltage is applied to the gate, the dielectric prevents the flow of current from the gate to the channel, but the applied voltage results in the creation of a “field effect” in the channel. Ex. 2002 at 510-511. This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). Ex. 2002 at 510-511.

24. As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping source-to-drain electrical current.

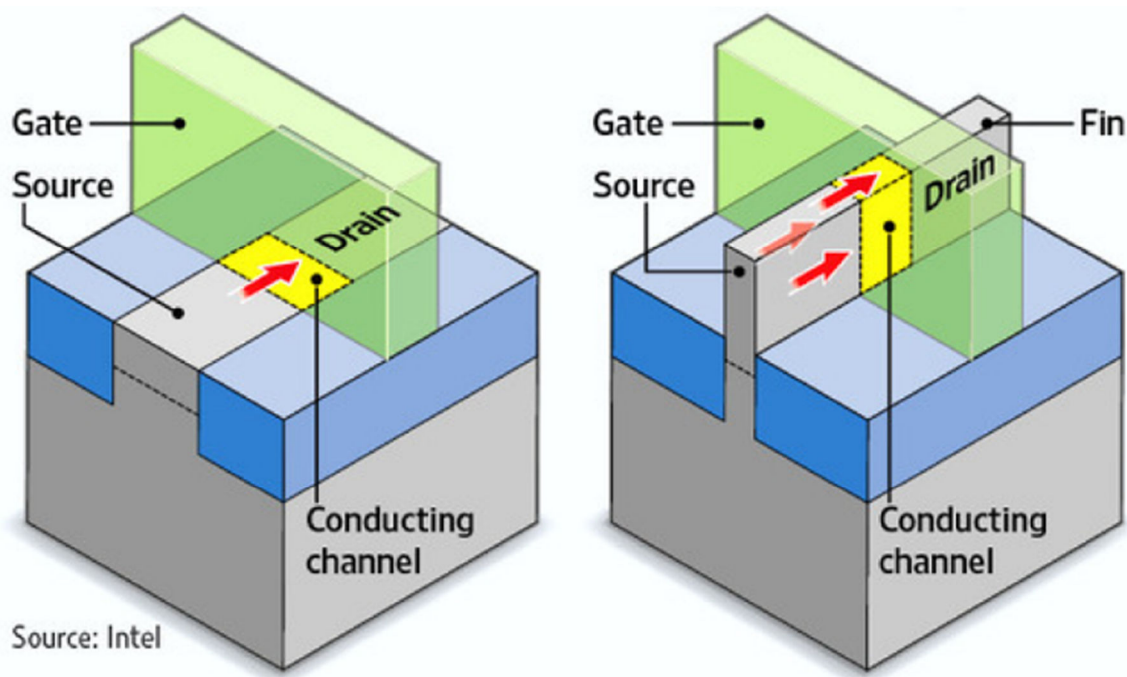


B. Planar vs. Three-Dimensional Transistors

25. Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more on a chip has been consistent and widespread in industry. This desire led to the development of a new type of transistor, a “FinFET.”

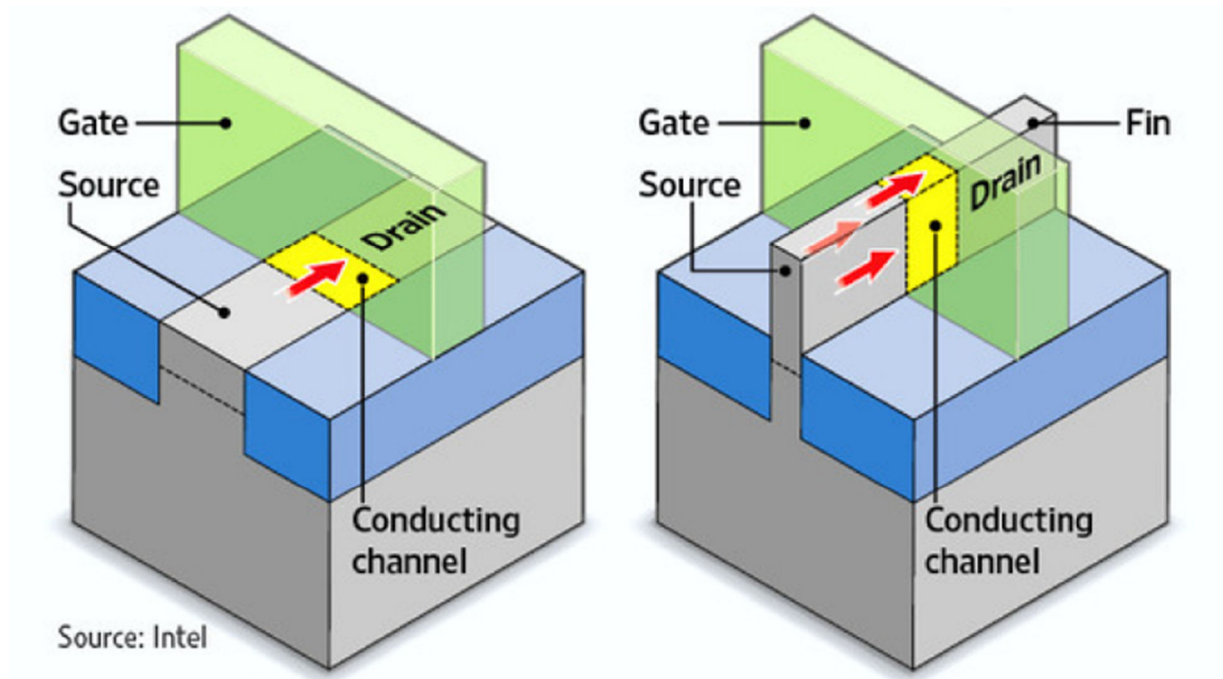
26. The simplified illustrative FET transistors illustrated in the previous section all feature a gate structure built on a flat semiconductor substrate; in other words, a “planar” FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors.

27. In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



28. In contrast, as illustrated below in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. In the resulting fin field

effect transistor (“FinFET”), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.



29. Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip compared to that of the planar transistor. In addition, because FinFETs typically leak less current than planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip.

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

30. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging.

31. In the first stage, the semiconductor material itself is created. Ex. 2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. Ex. 2002 at 13.

32. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” Ex. 2002 at 13-14. A wafer acts as a semiconductor substrate on and in which transistors may be formed.

33. The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. Ex. 2002 at 14. Thousands of integrated circuits can be formed on the substrate of a single wafer. Ex. 2002 at 14.

34. In the packaging stage, the wafer is separated into individual chips. Ex. 2002 at 14-15.

2. The Wafer Fabrication Stage

35. The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in the wafer's substrate. Ex. 2002 at 14. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). See Ex. 2002 at 29-31, 71. For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning.

36. **Layering** is the operation used to add thin layers to the semiconductor substrate. Ex. 2002 at 72. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. Ex. 2002 at 72.

37. For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. Ex. 2002 at 72.

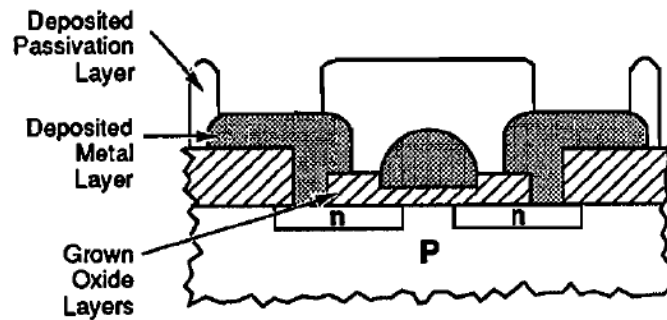


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

38. **Patterning** is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. Ex. 2002 at 72-73. This creates a pattern on the wafer surface. Ex. 2002 at 72-73.

39. The patterning may result in one or more holes in the layered material or one or more remaining islands of material. Ex. 2002 at 72-73. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

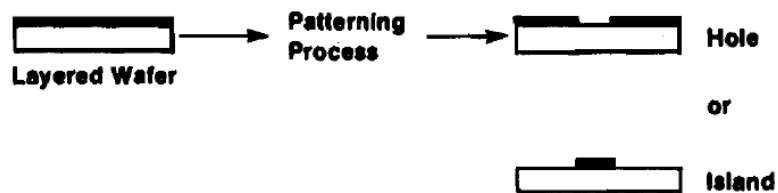


Figure 4.7 Patterning.

40. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

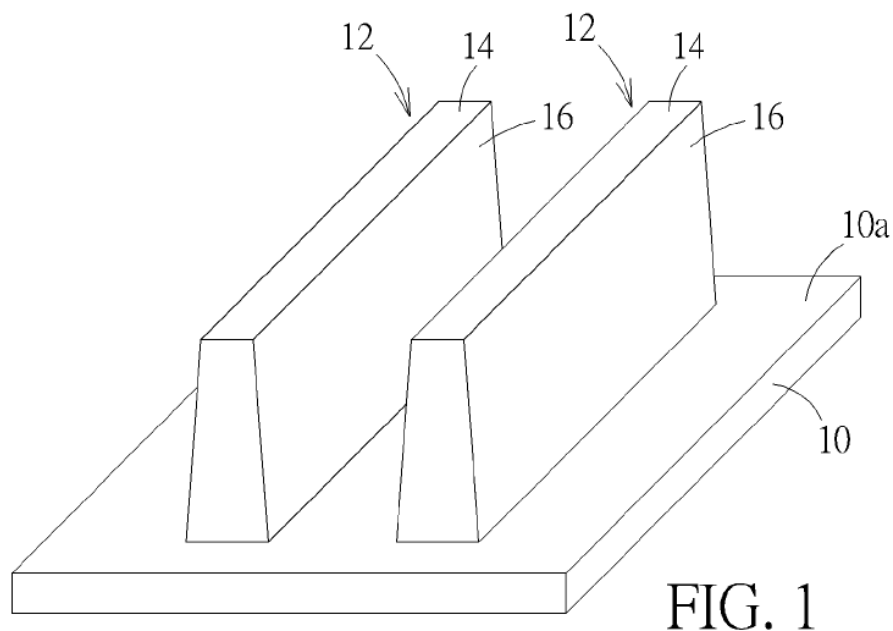
Ex. 2002 at 73.

VI. The Challenged '384 Patent

41. The '384 patent “generally relates to the field of semiconductor devices, and more particularly to a semiconductor device with an epitaxial structure and a fabrication method thereof.” Ex. 1001, 1:6-10. Specifically, the patent states that “[c]rystal strain technology is becoming more and more attractive as a means for getting better performances in the field of MOS transistor fabrication. Putting a strain on a semiconductor crystal alters the speed at which charges move through that crystal.” *Id.*, 1:20-25. The patent identifies weaknesses in the prior art in that “how to prevent the formation of the defects inside the epitaxial layer is an important issue” because “defects inside the epitaxial layer reduce the stress required to be

imposed onto the corresponding channel region.” *Id.*, 1:36-42. The described invention is designed to solve those issues. *Id.*, 1:45-2:31.

42. The patent describes “forming a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces,” for example in Figure 1, depicting substrate 10 and fins 12:



Ex. 1001, claim 1; Fig. 1.

43. The patent further describes “forming an isolation structure to surround the fin structure” and “forming a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure, and covering a portion of the isolation structure,” shown for example in Figure 2, depicting isolation structure 20 and gate structure 30:

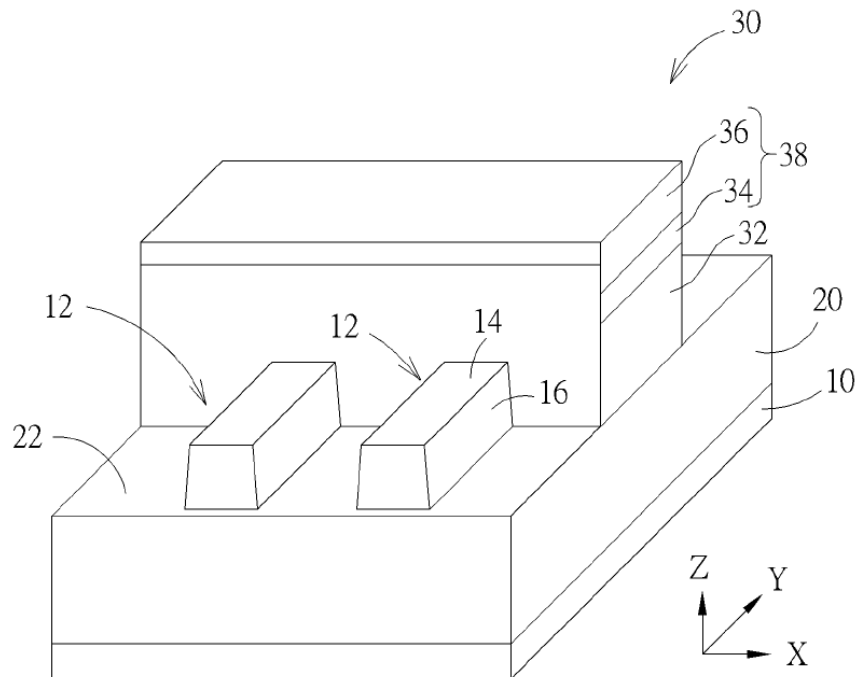


FIG. 2

Ex. 1001, claim 1; Fig. 2.

44. After forming the gate structure, the inventors form a spacer on the sidewall of the gate structure: “[a]fter the formation of the gate structure, a spacer 40 is formed on the sidewalls of the gate structure 30.” *Id.*, 5:6-8.

45. The patent also describes “after the step of forming the gate structure, etching the isolation structure exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth,” for example as shown in the transition from Figure 3 to Figure 5.

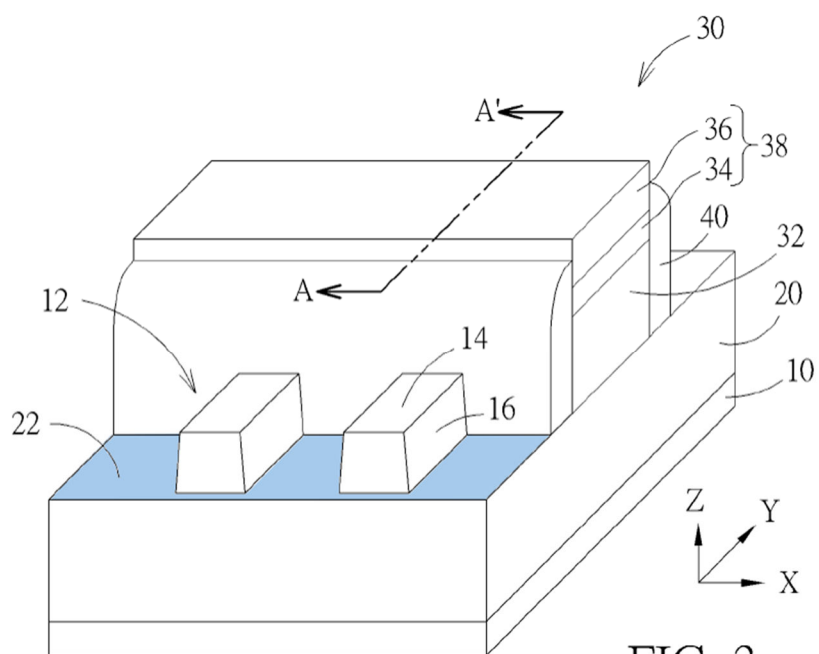


FIG. 3

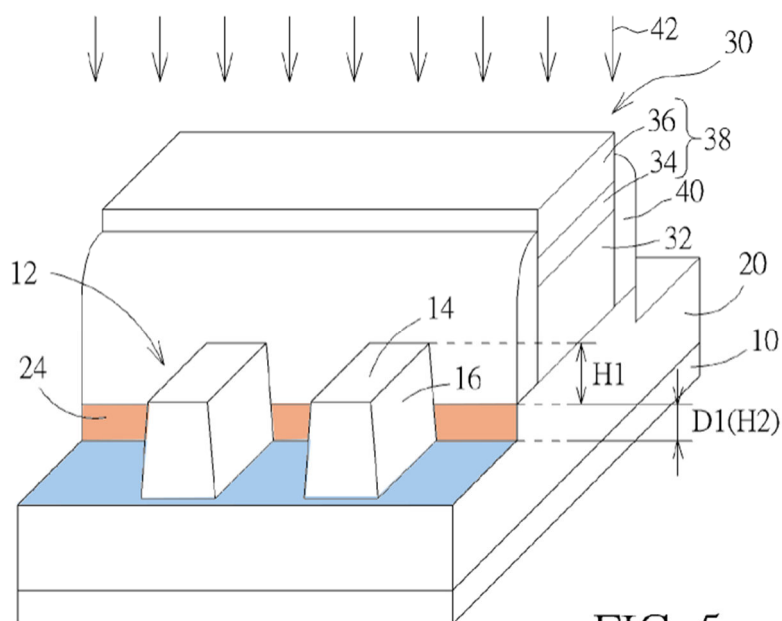
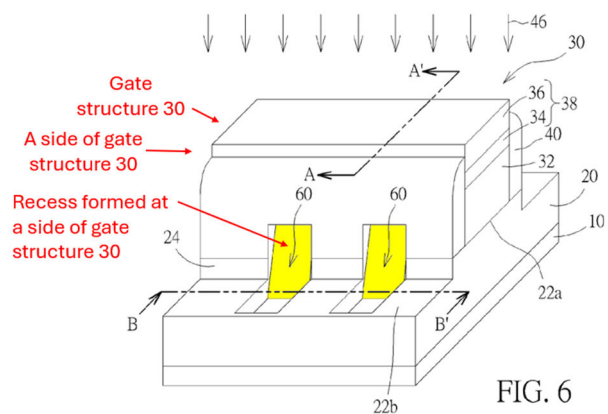
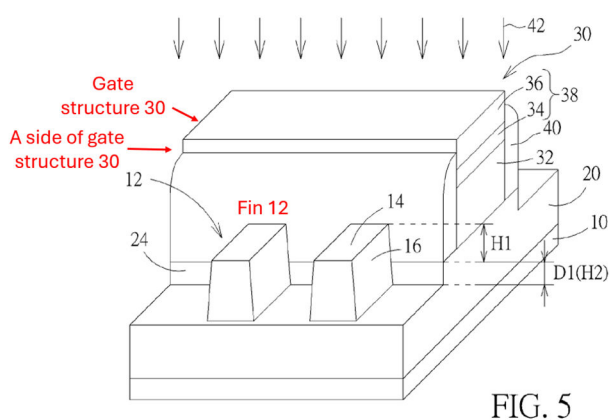


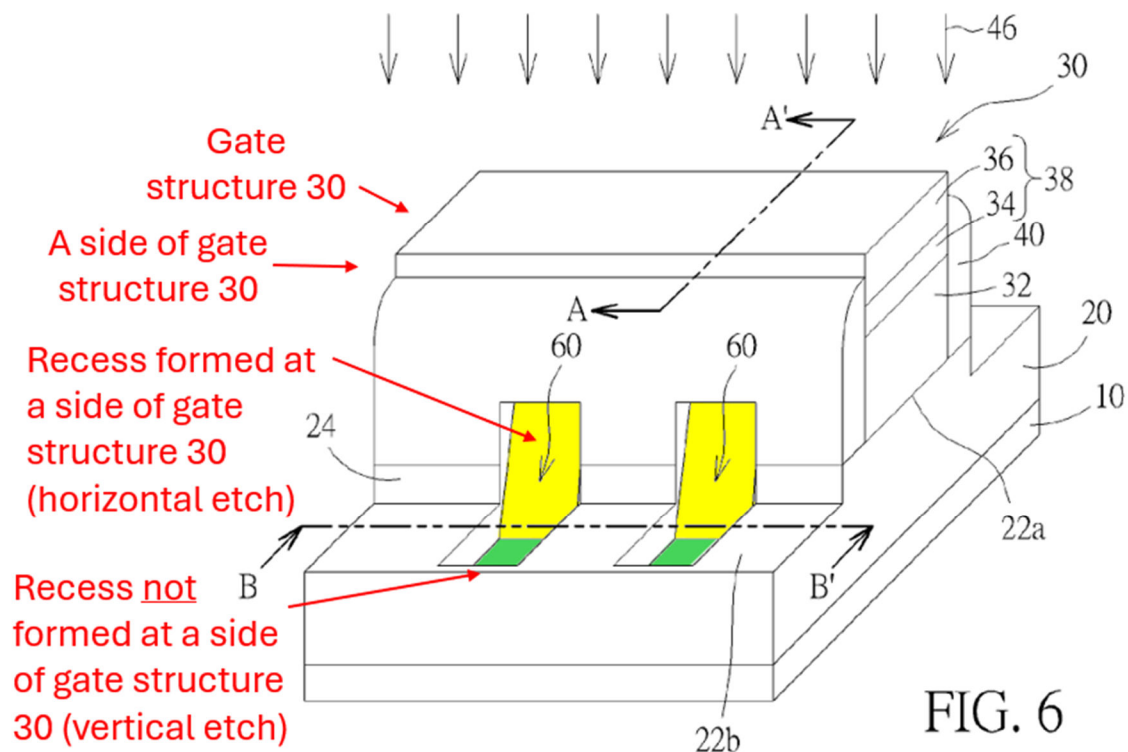
FIG. 5

Ex. 1001, claim 1, Figs. 3 and 5 (annotated).

46. The patent then describes the next step, forming a recess in fins 12, which is claimed as “forming a recess in the fin structure at a side of the gate structure.” Ex. 1001, claim 1. The claims thus establish two key things about the recess: (1) in what and (2) where the recess is created. The claims specify that the recess is created (1) in the fin structure, “a recess in the fin structure,” and (2) “at a side of the gate structure.” *Id.* This is further shown in Figures 5 (before etching to create the recess) and 6 (after etching to create the recess). *Id.*, Figs. 5 and 6. On the left below, Figure 5 shows the gate structure, the claimed side of the gate structure (a vertical wall), and the fin, before recess creation. On the right below, Figure 6 shows the gate and side of gate structure, and the recess in the fin and, and in particular, as annotated in yellow, the recess being “at a side of the gate structure,” which is the vertical wall of the gate. In particular, as annotated in yellow, the recess has a horizontal component that causes it to be “at a side of the gate structure.”



Ex. 1001, Figs. 5-6 (annotated). To further clarify, in the annotations below, the yellow recess area was created “at a side of the gate structure,” whereas the green part of the recess was not; it was purely a vertical component of the etch:



Ex. 1001, Fig. 6 (annotated). The yellow recess must exist according to the claims.

The recess cannot purely comprise the green (vertical) portion.

47. The specification confirms this by stating that the etch extends horizontally, in the example below, in the direction under the spacers 40 and the gate structure 30, and does not only etch vertically:

As shown in FIG. 6 to FIG. 8, a second etching process 46 is carried out to *etch the fin structures 12 under the gate structure 30 and the spacers 40*. After the etching process, a recess 60 may be formed in each fin structure 12 at *at least one side of the gate structure 30*.

Ex. 1001, 5:55-60 (emphasis added). This quote directly ties together the concept of etching horizontally to the formation of the recess “at at least one side of the gate structure 30,” which is the claim language, in that the former is what causes the latter.

48. Thus, at least part of the etch must extend horizontally and the recess must be formed at least partly horizontally, not just vertically, which would not be at a side of the gate structure, since the side of the gate structure is a vertical wall. As explained below, none of the asserted prior art discloses or renders obvious this limitation, nor does the Petition argue that it does, as each reference lacks the horizontal (yellow) etch direction of the recess.

49. The patent also explains that “a bottom surface of the recess has a second depth, and the second depth is deeper than the first depth,” *i.e.*, the depth to which the isolation structure was etched. Ex. 1001, 2:10-13, claim 1.

50. These innovative aspects of the invention are embodied in all challenged claims via claim 1, which recites:

1. A fabrication method for a semiconductor device, comprising:

forming a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;

forming an isolation structure to surround the fin structure;

forming a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure, and covering a portion of the isolation structure;

after the step of forming the gate structure, *etching the isolation structure* exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth;

forming a recess in the fin structure at a side of the gate structure; and

forming an epitaxial layer to fill up the recess, wherein *a bottom surface of the recess has a second depth, and the second depth is deeper than the first depth.*

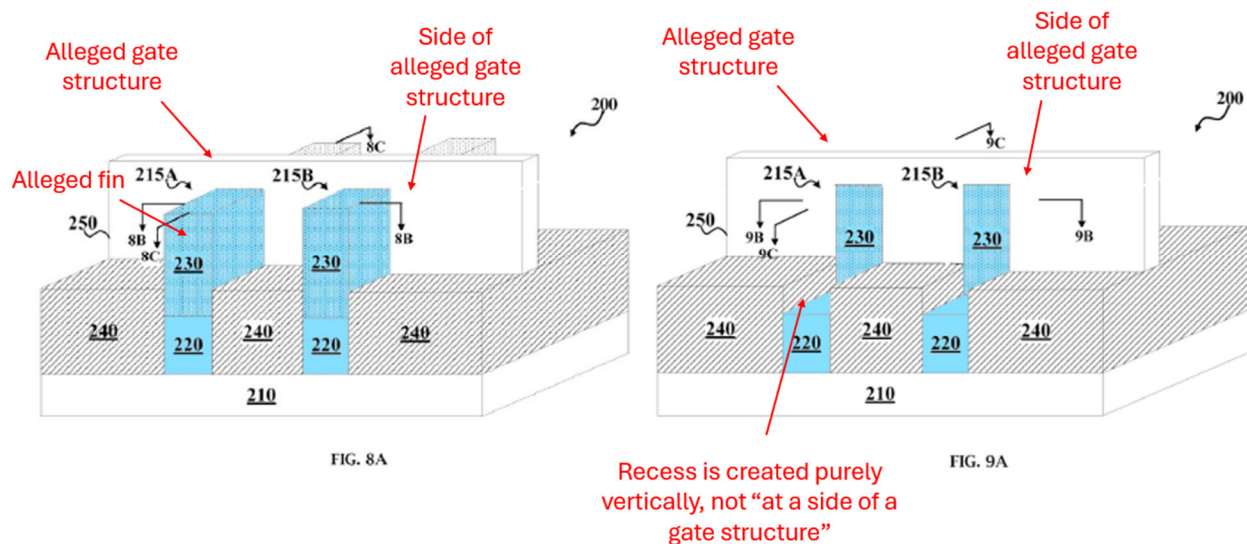
Ex. 1001, claim 1.

VII. ANALYSIS OF THE GROUNDS

A. Ground 1

1. Ground 1 Fails To Establish “Forming A Recess In The Fin Structure At A Side Of The Gate Structure” (Element 1[e])

51. As explained above in Section VI, the recess formed in the fin must extend at least in the horizontal direction in order to be a recess “at a side of the gate structure.” Ex. 1001, claim 1. Ground 1 fails to disclose that feature. In Xu, as the Petition concedes, the etching of the fin to create the alleged recess is purely vertical and has no horizontal component, and therefore, is not formed “at a side of the gate structure”:



Pet., 23 (annotated). Indeed, as seen above, some amount of item 230, the top part of the fin, remains, confirming that the etch did not extend horizontally. The specification confirms that the etch is only vertical as well, stating that “the fin

portions 220 may be etched into the substrate 210,” which is located directly below the fin, as seen in Figures 8A-9A. Ex. 1004, 8:36-37.

52. The Petition does not rely on Brask to supplement Xu for this element. Pet., 21-26.

2. Ground 1 Fails To Establish Both “Etching The Isolation Structure” And “Forming A Recess In The Fin Structure”

53. As the Petition concedes, there is no disclosure in Xu of a process, embodiment, or structure created by both “etching the isolation structure” and “forming a recess in the fin structure,” which are both requirements of all claims. Pet., 20-26. The Petition argues that Figures 1-6 constitute a first embodiment in which an isolation structure is etched, and that Figures 7-11A constitute a second embodiment in which a recess in the fin structure is formed. Pet., 20-26. Xu itself refers to these two embodiments as distinct approaches and different methods. Ex. 1004, 1:49-58 (“FIG. 1 is a flow chart of *a method* for fabricating a fin-like field effect transistor (FinFET) device according to aspects of the present disclosure”; “FIG. 7 is a flow chart of *another method* for fabricating a FinFET device according to aspects of the present disclosure.”).

54. The Petition’s rationale “to combine the fin-recessing step [of the second embodiment] with Xu’s first embodiment” is that it would “achieve and optimize strain” in the first embodiment. Pet. 23-24. But that only relates to the

second and third embodiments, Figures 7-11C and 12-16C respectively, as they refer to “FinFET devices 200 and 400,” discussed in those embodiments. Ex. 1004, 15:56-60. And Xu states that “controlling source and drain trench depth (for example, d1 and d2) for the epi source and drain features, strain for both PMOS and NMOS FinFET devices can be achieved and optimized.” Ex. 1004, 58-60; Pet. 23-24. The Petition’s argument is that changing depth of a trench in a fin can impact channel strain.

55. However, the first embodiment, Figures 1-6, describes a different and incompatible method of achieving strain from that of the second (and third) embodiment that the Petitioner seeks to add to the first embodiment, one that has no fin trench, and so the optimization methods of the second (and third) embodiments are inapplicable. In the first embodiment, starting with Figure 2, the isolation structure is etched to arrive at Figure 3:

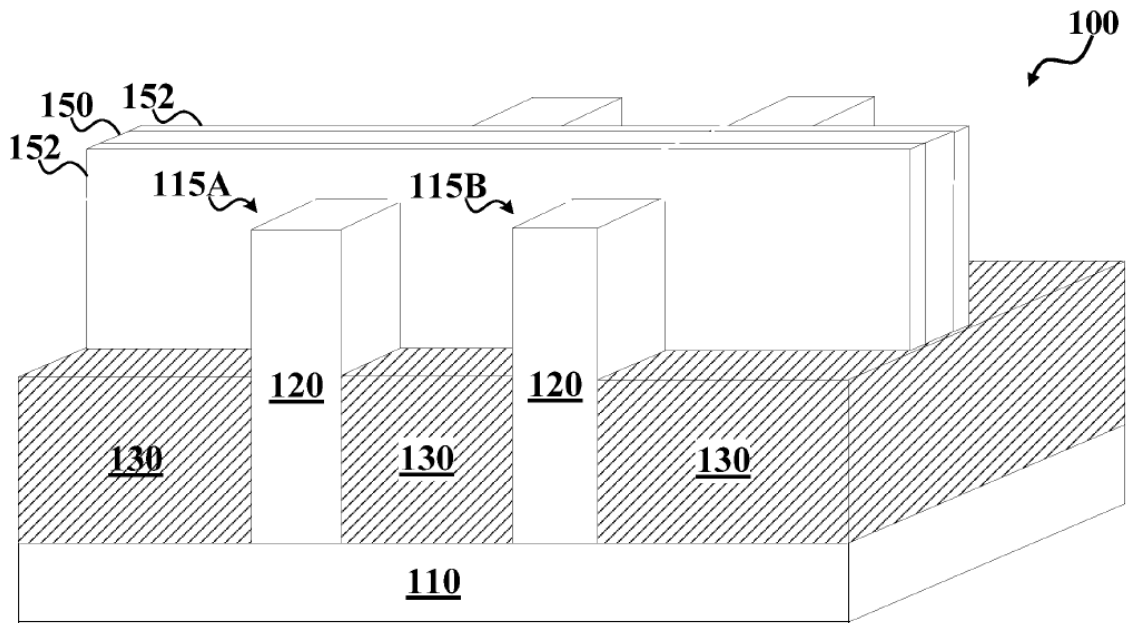


FIG. 2

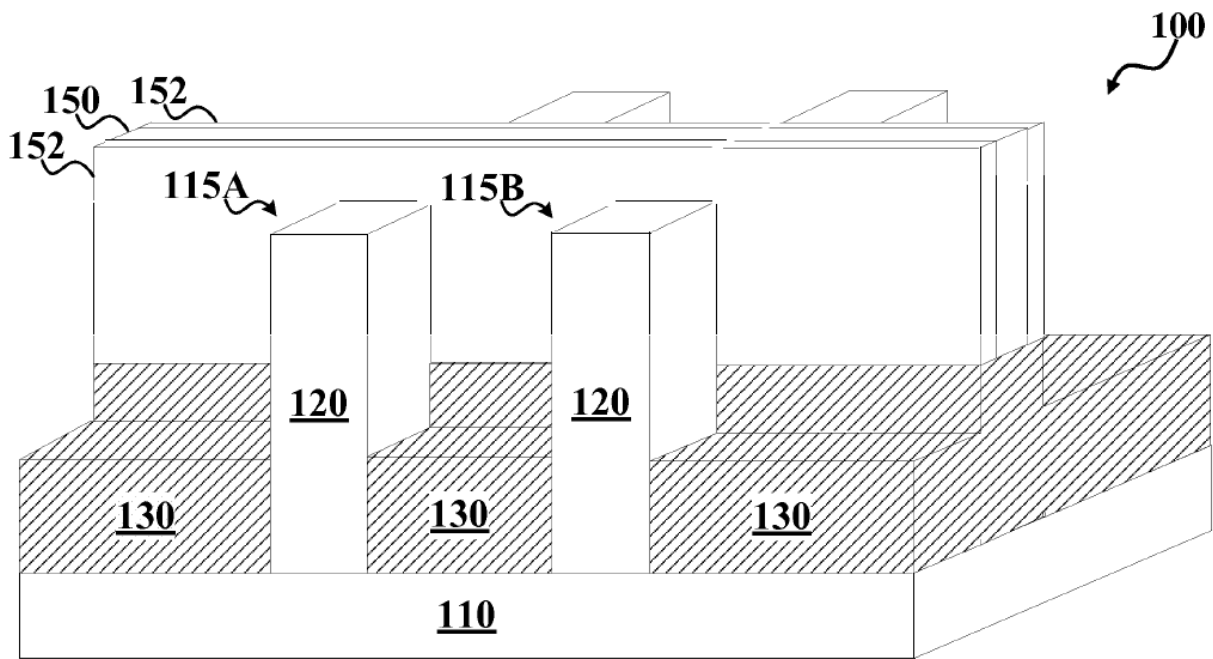


FIG. 3

Ex. 1004, Figs. 2 and 3. Then, “a fin template 135 is formed on exposed portions of the fins 120.” *Id.*, 5:1-2.¹

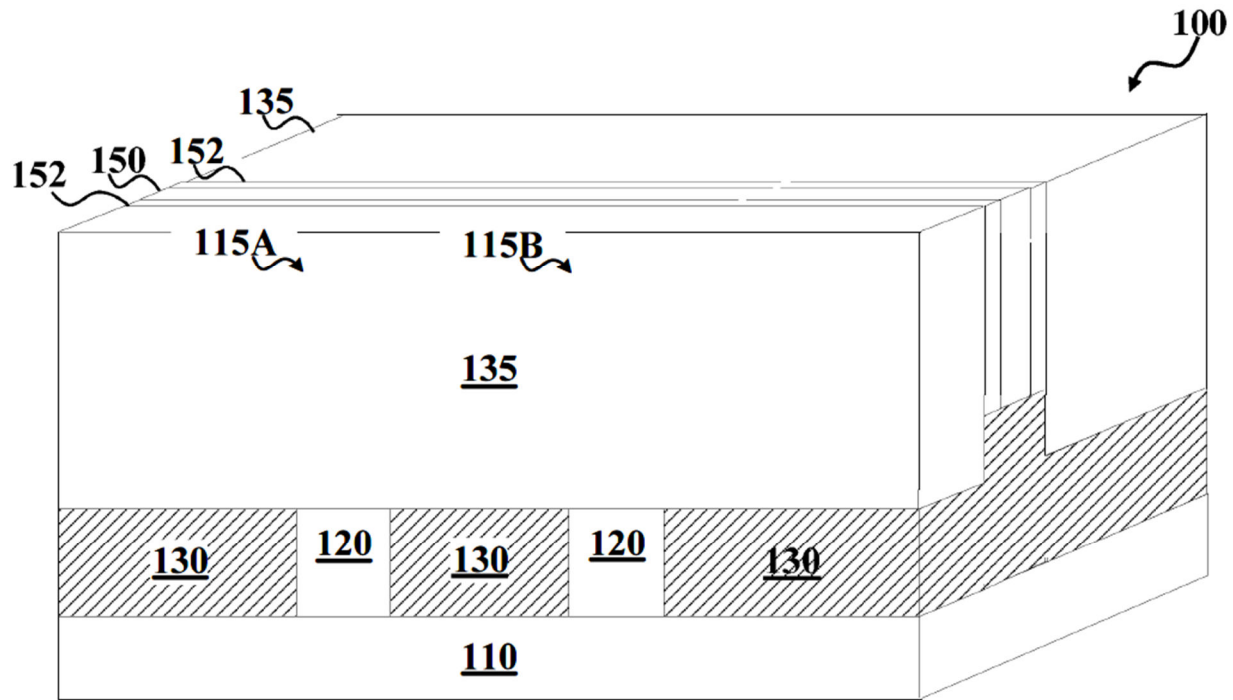


FIG. 4

Id., Fig. 4. Then, in Figure 5, “a process is performed to recess the fin template 135” from what is shown in Figure 4:

¹ In Xu’s embodiments that include a fin template 135, the isolation structures 130 do not actually isolate the fins 120, since the fin template 135 electrically connects them together. *See* Ex. 1004, 6:28-31.

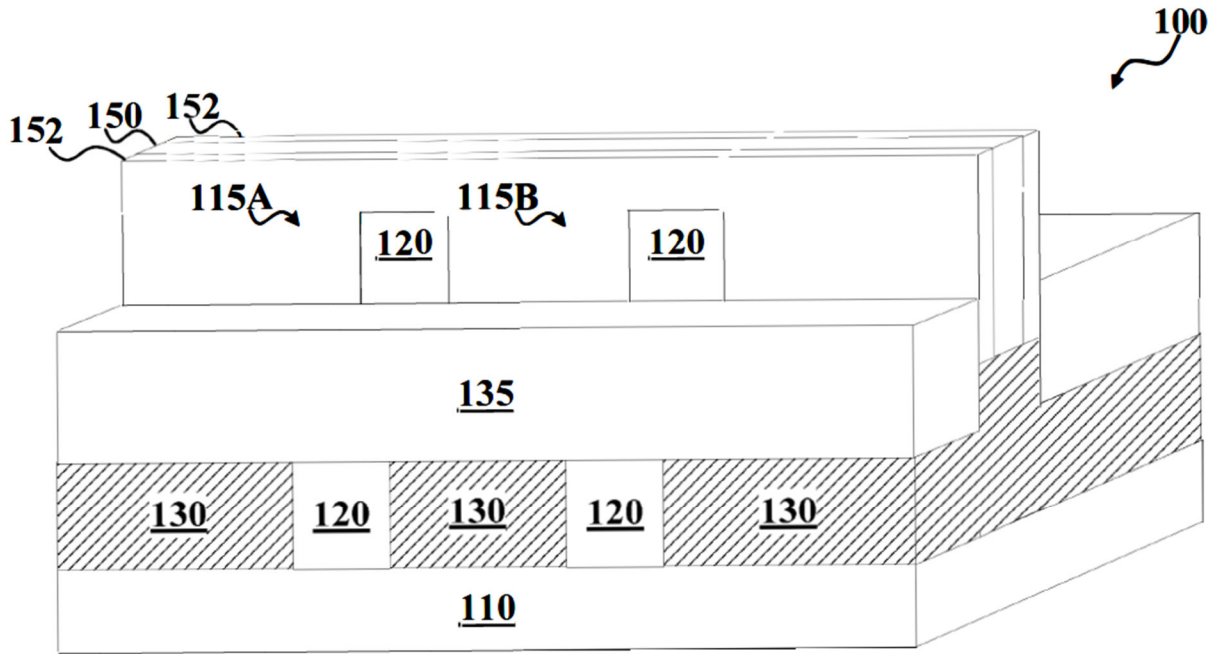


FIG. 5

Id., 5:34-35; Fig. 5. Specifically, “[t]he fin template 135 is etched back sufficiently to expose the channels of the fin structures 115A and 115B,” as illustrated in FIG. 5. *Id.*, 5:43-45; Fig. 5. As Xu states, “[t]his ensures that later-formed raised source and drain features (semiconductor material 160) ***can effectively introduce strain*** into the channels of the fins structures 115A and 115B.” *Id.*, 5:45-47.

56. This process, as shown above, removes part of the fin structure, but notably, as the Petition concedes, it does not meet the claim requirement to “form[] a recess in the fin structure at a side of the gate structure.” Pet. 20-26.

57. Then, in Figure 6, “a semiconductor material 160 is epitaxially grown over the fin template 135. In the depicted embodiment, a semiconductor material is

epi grown on the exposed fin template 135 in the source and drain regions of the fin structures 115A and 115B”:

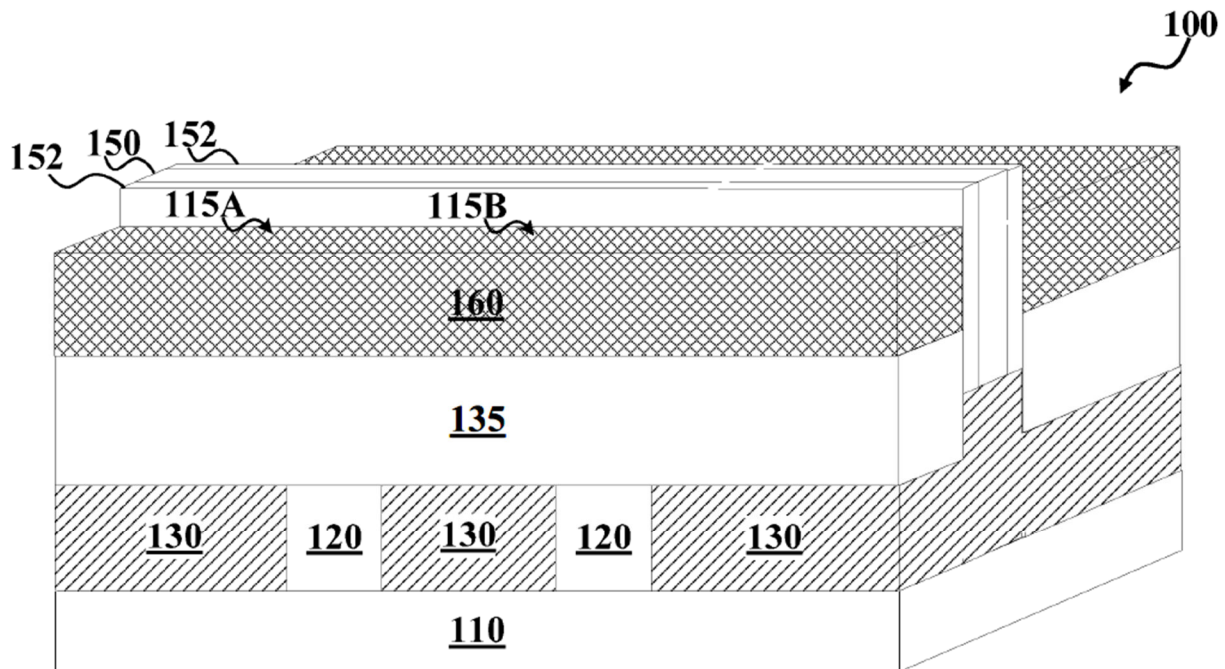


FIG. 6

Ex. 1004, 5:49-53; Fig. 6. Explaining what was alluded to with regard to Figure 5 above, Xu explains that “[t]he epi grown semiconductor material 160 *generates channel strain* for the fin structures 115A and 115B.” *Id.*, 5:53-55 (emphasis added). As Xu states, therefore, the semiconductor material 160 generates channel strain, not the depth of the trench, which does not exist in the first embodiment.

58. Thus, the first embodiment has a different method from the second and third regarding how to introduce channel strain, a method that does not benefit from

the alleged modification and is incompatible with the proposed modifications. Given that fact, a POSITA would not be motivated to combine embodiments and perform both claimed steps.

3. Even If Ground 1 Establishes Both “Etching The Isolation Structure” And “Forming A Recess In The Fin Structure,” It Fails To Disclose “The Second Depth Is Deeper Than The First Depth”

59. The claim requires that the fin recess is created to a depth greater than that to which the isolation structure is etched. Ex. 1001, Claim 1. Xu does not disclose that requirement, even in the alleged modification combining different aspects of different embodiments, which a POSITA would not be motivated to do, as explained above. The Petition argues that, when combining the first and second embodiments of Xu, which a POSITA would not do, as explained above, “the second depth is necessarily ‘deeper than the first depth.’” Pet., 30. Not so. The Petition cobbles together two embodiments, one that etches a fin without concern as to the height of the surrounding isolation structure (second embodiment) and one that etches an isolation structure, without concern as to the height of the neighboring fin. There is nothing to suggest that, even if a POSITA were to combine both steps, one etch would go down further than the other. Petitioner’s expert provides no rationale, simply repeating what the Petition states. Ex. 1003 ¶¶ 101-102. It is simply

hindsight to state that one would necessarily reach a further depth than the other, and specifically that the fin recess would be at a greater depth.

B. Ground 2

1. Ground 2 Fails To Establish “Forming A Recess In The Fin Structure At A Side Of The Gate Structure” (Element 1[e])

60. As explained above in Section VI, the recess formed in the fin must extend at least in the horizontal direction in order to be a recess “at a side of the gate structure.” Ground 2 fails to disclose that feature. In Lin, as the Petition concedes, the etching of the fin to create the alleged recess is purely vertical and has no horizontal component, and therefore, is not formed “at a side of the gate structure”:

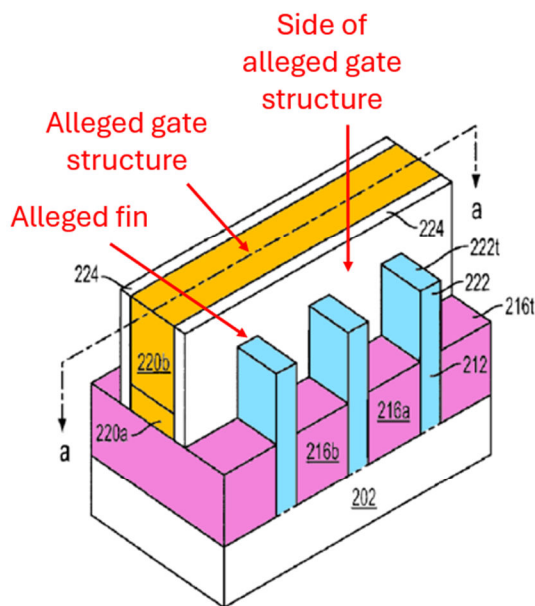


FIG. 7A

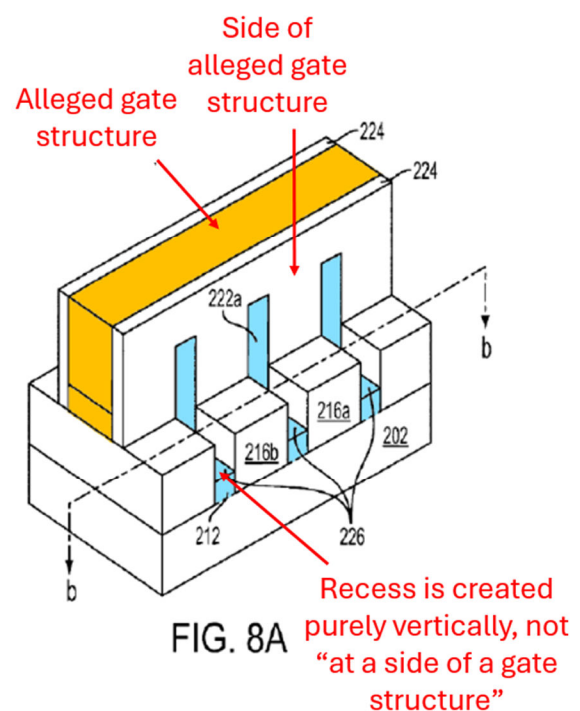
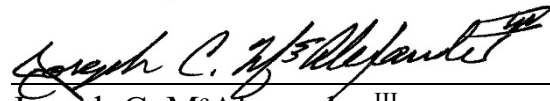


FIG. 8A

Pet., 59-60 (annotated). As the Petition cites, Lin specifically states that “[t]he portion of the semiconductor fin 212 [blue] *not covered by the gate stack 220* [gold] and spacers 224 formed thereover are recessed to form a recessed portion 226 of the fin 212 [blue].” Pet. 59 (citing Ex. 1005 ¶ 30) (emphasis added). That is, the etch does not extend horizontally and there is thus no fin recess at “*a side of the gate structure.*”

61. The Petition does not rely on Brask to supplement Lin for this element. Pet. 69-71.

Dated: October 17, 2025



Joseph C. McAlexander III