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Transcript of Jack Lee, Ph.D.

Date: February 26, 2026

Case: Taiwan Semiconductor Manufacturing Co. Ltd. -v- Marlin Semiconductor Ltd. (PTAB)

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Phone: 888.433.3767

Email: transcripts@planetdepos.com

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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING
COMPANY, LTD.,

Petitioner,

vs.

CASE NO: IPR2025-01265

MARLIN SEMICONDUCTOR, LTD., U.S. Patent No. 8,993,384

Patent Owner.

* * * * *

Deposition of JACK LEE, PH.D., taken on
behalf of the Defendants, via Zoom videoconference,
commencing on the 26th day of February, 2026, at the
hour of 8:01 a.m. PT, before Jillian Doctor, CSR No.
14603, pursuant to Notice of Taking Deposition.

A P P E A R A N C E S

FOR THE PETITIONER:

JONES DAY
1221 Peachtree St NE, #400
Atlanta, Georgia 30361
BY: Stephen Bradley, Esquire
Sbradley@jonesday.com

FOR THE PATENT OWNER:

MINTZ, LEVIN, COHN, FERRIS, GLOVSKY AND
POPEO, P.C.
777 Brickell Avenue, Suite 500
Miami, Florida 33131
BY: Reza Dokhanchy, Esquire
Rdokhanchy@mintz.com

VIDEOGRAPHER:

Harut Akopyan

TECHNICIAN:

Leyhbert Sharp

ALSO PRESENT:

JILLIAN DOCTOR, RPR, CRR
COURT REPORTER

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I N D E X

WITNESS	EXAMINATION	PAGE
JACK LEE	BY MR. DOKHANCHY	5

* * * * *

EXHIBITS FOR IDENTIFICATION

Exhibit 2004	48
What is Step Coverage	

Transcript of Jack Lee, Ph.D.
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1	THE TECHNICIAN: All right, everybody. Good	08:01:36
2	morning and thank you for attending this proceeding	08:01:43
3	remotely, which we anticipate will run smoothly.	08:01:45
4	Please remember to speak slowly and do your best not	08:01:49
5	to talk over one another. And please be aware we are	08:01:52
6	recording this proceeding via Zoom just for back-up	08:01:55
7	purposes only.	08:01:57
8	Any off-the-record discussions should be had	08:01:59
9	away from the computer. And just remember to mute	08:02:02
10	your microphone for those conversations. Please have	08:02:05
11	your video enabled to help our court reporter identify	08:02:07
12	who is speaking.	08:02:10
13	I apologize in advance for any	08:02:12
14	technical-related interruptions for the videographer.	08:02:14
15	You may proceed. Thank you.	08:02:16
16	THE VIDEOGRAPHER: Thanks, Leyhbert.	08:02:18
17	Stand by for video.	08:02:21
18	THE TECHNICIAN: Sure.	08:02:22
19	THE VIDEOGRAPHER: Here begins Media	08:02:23
20	Number 1 in the videotaped deposition of Dr. Jack Lee	08:02:36
21	in the matter of Taiwan Semiconductor Manufacturing	08:02:41
22	Co., LTD versus Marlin Semiconductor, LTD in the	08:02:47
23	United States Patent and Trademark Office before the	08:02:53
24	Patent Trial -- excuse me -- before the Patent Trial	08:02:57
25	and Appeal Board. Case Number: IPR 2025-01265.	08:03:04

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1	Today's date is February 26, 2025. The time	08:03:12
2	on the video monitor is 8:03 a.m. Pacific time.	08:03:16
3	The remote videographer today is Harut	08:03:22
4	Akopyan representing Planet Depos. All parties of	08:03:24
5	this video deposition are attending remotely.	08:03:28
6	Would counsel please voice-identify	08:03:31
7	themselves and state whom they represent, starting	08:03:33
8	with the taking attorney.	08:03:35
9	MR. DOKHANCHY: Reza Dokhanchy from Mintz	08:03:36
10	Levin on behalf of the patent owner.	08:03:40
11	MR. BRADLEY: Stephen Bradley from Jones Day	08:03:41
12	on behalf of petitioner.	08:03:44
13	THE VIDEOGRAPHER: The court reporter today	08:03:49
14	is Jill Doctor representing Planet Depos. The witness	08:03:51
15	will now be sworn.	08:03:57
16	JACK LEE, PH.D.,	
17	having been first duly sworn,	
18	was examined and testified as follows:	
19	EXAMINATION	
20	BY MR. DOKHANCHY:	
21	Q. Good morning, Dr. Lee.	08:04:13
22	A. Good morning.	08:04:15
23	Q. Have you been deposed before?	08:04:16
24	A. Yes.	08:04:17
25	Q. About how many times?	08:04:18

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1	A.	I don't recall. Probably, like, 50 times or	08:04:19
2		more. I don't remember now.	08:04:28
3	Q.	Okay. So you're very familiar with the	08:04:29
4		process.	08:04:31
5		The main thing I would ask is that you and I	08:04:32
6		do not speak over each other so that the court	08:04:35
7		reporter can take down everything we say.	08:04:38
8		Is that okay with you?	08:04:40
9	A.	Yes.	08:04:40
10	Q.	Is there any reason you cannot provide	08:04:42
11		truthful and accurate testimony today?	08:04:45
12	A.	No.	08:04:46
13	Q.	All right. Can you tell me about your	08:04:49
14		experience with semiconductor device manufacturing,	08:04:54
15		starting with your education?	08:04:57
16	A.	So I have been in this semiconductor	08:04:59
17		business since 1979 or so, when I was a undergraduate	08:05:10
18		student at UCLA. And since then I've worked in the	08:05:23
19		semiconductor industry from 1979 part-time, to 1984	08:05:36
20		full-time for several years at the TRW	08:05:51
21		Microelectronics Center.	08:06:04
22		And I also received my master degree, in	08:06:04
23		addition to my bachelor degree, in electrical	08:06:10
24		engineering in 1980. And subsequently, a master	08:06:14
25		degree also from UCLA in 1981.	08:06:24

1	Then I got my PhD degree in electrical	08:06:31
2	engineering from UC Berkeley, working under my	08:06:37
3	advisor, Professor Chenming Hu, who is considered the	08:06:47
4	father of FinFETs.	08:06:56
5	And my focus of research included 3D	08:07:01
6	structures such as FinFET, gated-all-around structure,	08:07:09
7	fabrication processes, characterization and modeling	08:07:14
8	device, physics, and replacement gate process, strain	08:07:20
9	engineering.	08:07:35
10	Q. What is --	08:07:41
11	A. In 1980 --	08:07:42
12	Q. Sorry. Go ahead. I thought you were done.	08:07:43
13	A. Oh.	08:07:46
14	In 1988, I joined the University of Texas in	08:07:46
15	the department of electrical and computer engineering,	08:07:51
16	focusing on the research that I talked about just a	08:07:58
17	minute ago. We have a cleanroom -- Class 100	08:08:02
18	cleanroom. And my student and I fabricate many, many	08:08:11
19	devices, including FinFET, gate-all-around devices,	08:08:16
20	strain engineering devices.	08:08:22
21	I graduated over 40 PhD students and have	08:08:27
22	published over 600 journal papers and conference	08:08:32
23	proceedings. And have nine patents. I also	08:08:36
24	coauthored eight books and book chapters.	08:08:42
25	And I've been elected to be the fellow of	08:08:46

1	IEEE, which is the Society for Electrical Engineering	08:08:52
2	and Electronics Engineering.	08:08:58
3	I was -- I had also been the distinguished	08:09:01
4	lecturer for IEEE Electron Devices Society.	08:09:05
5	In addition to my research, I also provide	08:09:13
6	short course. Of course, at UT not only do research,	08:09:18
7	but I also teach a -- teach courses, including a	08:09:24
8	graduate-level semiconductor device course.	08:09:29
9	In addition to university work, I also teach	08:09:33
10	short courses, continuing education short courses, and	08:09:42
11	consult with company regarding the -- not only	08:09:47
12	teaching the courses with two engineers, but also they	08:09:58
13	bring their problems to the course, and we discuss	08:10:01
14	about it. And I travel worldwide to conduct these	08:10:04
15	courses, including China, Korea, Taiwan, Israel,	08:10:11
16	Ireland, England, and Scotland, and all over US.	08:10:22
17	So that's -- these are my highlight of my	08:10:28
18	experience in semiconductor.	08:10:34
19	Q. Thank you.	08:10:35
20	You mentioned the TRW Microelectronics	08:10:38
21	Center.	08:10:44
22	A. Yes.	08:10:44
23	Q. What is that? Or what was that?	08:10:45
24	A. It was -- TRW is focused on building	08:10:47
25	communication -- at least in my division,	08:10:58

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1 communication chips for aerospace industry. It's 08:11:00
2 located in El Segundo, California. Actually, the 08:11:06
3 division I worked in was Redondo Beach, California. 08:11:18
4 At that point, my area was focusing on 08:11:22
5 high-speed devices. High-speed transistor program. 08:11:26
6 Q. And your work at TRW related to bipolar 08:11:36
7 devices. 08:11:40
8 Is that right? 08:11:41
9 A. That's right. In those days, bipolar was a 08:11:42
10 main course -- main (Indiscernible) for high-speed 08:11:54
11 applications. 08:12:03
12 Since then I also -- even though that was my 08:12:03
13 focus, my -- at the TRW Microelectronics Center, I 08:12:07
14 also helped them develop the MOS transistors devices. 08:12:16
15 And -- but other than that, my PhD, my master degree, 08:12:25
16 and my research and teaching in -- as a faculty at 08:12:35
17 University of Texas at Austin focused on so-called 08:12:45
18 MOSFET, M-O-S-F-E-T. 08:12:52
19 And -- which is what FinFETs and -- 08:12:56
20 so-called gate-all-around FinFET transistors is. 08:13:03
21 Q. And once you finished your PhD in 1988, it 08:13:15
22 appears you went straight into academia. 08:13:19
23 Is that correct? 08:13:22
24 A. Yes. Prior to my -- prior to my graduation 08:13:23
25 from University of California at Berkeley, I was 08:13:31

1 already teaching courses at Berkeley with my own TA, 08:13:37
2 teaching assistant. 08:13:46
3 And I enjoyed teaching, and I also enjoy 08:13:47
4 university environment, research environment in the 08:13:54
5 university, so I decided to go into academia. And in 08:14:01
6 four years, I -- I was promoted from assistant 08:14:07
7 professor to associate professor level. And then 08:14:12
8 another four years, I was promoted to full professors. 08:14:17
9 Q. And since 1988 you have been in academia and 08:14:22
10 you have not returned to industry. 08:14:27
11 Is that correct? 08:14:29
12 A. Since 1988, I was in academia; but as I 08:14:30
13 mentioned before, I have connection with industry, you 08:14:40
14 know, all this time that I was in academia know me 08:14:50
15 that I receive funding from industry. I collaborated 08:14:57
16 with -- with industrial partners to do research. We 08:15:00
17 exchange devices and sometimes we receive wafers from 08:15:07
18 industry partially fabricated, and then we put in our 08:15:19
19 device and then send it back and going back and forth. 08:15:24
20 So although I did not return to industry 08:15:28
21 full-time, I work with industry partners, engineers, 08:15:34
22 and even management in various role, including giving 08:15:45
23 short courses and doing consulting, and collaborative 08:15:56
24 research. 08:16:05
25 Q. Since 1988, you have not been employed by a 08:16:06

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1	company; correct?	08:16:10
2	A. I guess I don't know what exactly you mean	08:16:12
3	by employed. I do consult with the industry and teach	08:16:25
4	short courses to particular companies, so -- but I'm	08:16:33
5	not a full-time employee of any industry or companies.	08:16:38
6	Q. And you haven't been a full-time employee of	08:16:44
7	any industrial company since 1988; correct?	08:16:48
8	A. That is -- that is correct. I'm not -- I	08:16:53
9	have not been a full-time employee of industrial	08:16:57
10	company; although, I work with industrial company	08:17:06
11	very, you know -- in various, you know,	08:17:16
12	collaborations, consulting, teaching courses.	08:17:24
13	So I have been involved tightly with	08:17:27
14	industrial companies during my tenure as a faculty at	08:17:31
15	the University of Texas at Austin.	08:17:38
16	Q. Do you have any experience as an employee in	08:17:40
17	the industry working on FinFETs?	08:17:49
18	A. As I mentioned, I was not an employee of any	08:17:52
19	companies since 1988. And FinFET does not -- was not	08:18:05
20	discovered or invented until mid or late 1980 or	08:18:18
21	1990s.	08:18:28
22	Q. Great.	08:18:28
23	MR. DOKHANCHY: Let's make available	08:18:36
24	Exhibit 1003, if we could, please.	08:18:38
25		08:18:38

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1	BY MR. DOKHANCHY:	08:18:38
2	Q. Dr. Lee, this is your declaration in this	08:18:41
3	matter. I understand you do not have paper copies.	08:18:45
4	Is that right?	08:18:48
5	A. No.	08:18:48
6	THE TECHNICIAN: And do you want to mark	08:18:50
7	that as Exhibit No. 1?	08:18:54
8	MR. DOKHANCHY: No. So we'll just use the	08:18:57
9	premarked numbering. So that exhibit has been	08:19:00
10	premarked as Exhibit 1003 --	08:19:03
11	THE TECHNICIAN: Okay.	08:19:05
12	MR. DOKHANCHY: -- so we'll just continue	08:19:06
13	with that numbering.	08:19:08
14	THE TECHNICIAN: Stand by. Give me just one	08:19:09
15	second.	08:19:11
16	And Exhibit Number 2003 is available now.	08:19:18
17	MR. DOKHANCHY: Sorry. 1003. Not 2003.	08:19:23
18	THE TECHNICIAN: Yeah. That's what I said,	08:19:27
19	1003, just in case.	08:19:29
20	MR. DOKHANCHY: Sorry.	08:19:31
21	THE TECHNICIAN: No worries. My accent.	08:19:32
22	BY MR. DOKHANCHY:	08:19:51
23	Q. And, Dr. Lee, if you can try to access the	08:19:51
24	download link that's in the chat, see if you can	08:19:54
25	download Exhibit 1003 and let me know.	08:19:57

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1	A.	I'm sorry. I don't see it on the chat.	08:20:01
2	THE TECHNICIAN:	Remember the link we share	08:20:04
3		earlier where you open the document, you'll be able to	08:20:07
4		see it. It's the same link. And I can send it again.	08:20:10
5		Let me send it again in the chat box.	08:20:13
6	THE WITNESS:	Oh.	08:20:15
7	THE TECHNICIAN:	I just shared the link one	08:20:17
8		more time.	08:20:19
9	THE WITNESS:	Oh, I got it. Okay. Thank	08:20:23
10		you.	08:20:25
11	THE TECHNICIAN:	No problem.	08:20:27
12	THE WITNESS:	Oops. It said this folder is	08:20:29
13		empty. Hold on one second.	08:20:33
14	THE TECHNICIAN:	Press F5 to refresh your	08:20:39
15		browser.	08:20:45
16	THE WITNESS:	Is it possible to download	08:20:49
17		from that?	08:20:51
18	THE TECHNICIAN:	Yeah.	08:20:53
19	THE WITNESS:	Okay. Got it. I see that.	08:20:57
20	THE TECHNICIAN:	Are you able to see -- I'm	08:21:15
21		sorry. Just for clarification, are you able to see	08:21:17
22		the document that I just shared?	08:21:19
23	THE WITNESS:	Yes. I download it now.	08:21:21
24		Thank you.	08:21:22
25	THE TECHNICIAN:	Okay.	08:21:23

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1	MR. DOKHANCHY: And then can we also add to	08:21:25
2	that folder Exhibit 1001, and 1004, 1005, and 1006, so	08:21:27
3	Dr. Lee can access them?	08:21:39
4	THE VIDEOGRAPHER: Yes, sir. You said 1001,	08:21:41
5	1004, 1005, 1006?	08:21:44
6	MR. DOKHANCHY: Yes.	08:21:48
7	THE TECHNICIAN: One second. They're	08:22:00
8	uploading now.	08:22:01
9	And they're available now.	08:22:02
10	BY MR. DOKHANCHY:	08:22:03
11	Q. So, Dr. Lee, we'll be discussing at least	08:22:04
12	these exhibits, just so -- I just want to make sure	08:22:06
13	you have them and can see them.	08:22:11
14	1001 is the '384 patent, the patent at issue	08:22:14
15	here; 1003 we already discussed is your declaration;	08:22:18
16	1004 is the Xu reference; 1005 is the Lin reference;	08:22:22
17	and 1006 is the Brask reference.	08:22:25
18	So as we're going, you should have access to	08:22:28
19	those. And let me know if, for any reason, you don't.	08:22:31
20	A. Can you give me one second? Thank you.	08:22:35
21	So I downloaded 1001, 1003, 1004, 1005, and	08:22:47
22	1006.	08:22:53
23	Q. Great.	08:22:55
24	A. Is that all you have so far at this point?	08:22:56
25	Q. Yes.	08:22:58

1	A.	Okay. Thank you.	08:22:59
2	Q.	All right. If you could open Exhibit 1001,	08:23:00
3		the '384 patent.	08:23:06
4	A.	Yes.	08:23:09
5	Q.	I just want to direct --	08:23:10
6	A.	I got it.	08:23:13
7	Q.	I want to direct you to the claims that I	08:23:13
8		have some questions about.	08:23:16
9		So if you go down to Page 12 of 13 in	08:23:17
10		Exhibit 1001, you'll see the claims starting with	08:23:24
11		claim one.	08:23:27
12		Let me know if you see that?	08:23:30
13	A.	I see that.	08:23:33
14	Q.	And I have some questions about Claim 8 in	08:23:34
15		particular. And I'll read Claim 8 so we're on the	08:23:40
16		same page.	08:23:44
17		That is, "The fabrication method according	08:23:45
18		to Claim 7, wherein a step for forming the spacer	08:23:47
19		comprises: Depositing a material layer to conformally	08:23:51
20		cover the gate structure and the fin structure, and	08:23:55
21		etching the material layer until the isolation	08:23:58
22		structure is exposed."	08:24:01
23		Do you see that?	08:24:03
24	A.	Yes.	08:24:04
25	Q.	All right. Now, if you could open up your	08:24:06

1	declaration, Exhibit 1003.	08:24:11
2	A. Hold on one second. Sorry.	08:24:16
3	Okay.	08:24:22
4	Q. If you scroll down to internal Page 59, you	08:24:23
5	have a Section 8 where you discuss Claim 8. And in	08:24:36
6	the --	08:24:40
7	A. Yes.	08:24:41
8	Q. -- PDF Page 65.	08:24:41
9	A. Yes.	08:24:43
10	Q. Let me know when you're there.	08:24:44
11	Okay. Are you there, Dr. Lee?	08:24:49
12	A. Hold on one second. Sorry. I apologize.	08:24:51
13	So this is Page 60 on the PDF?	08:25:09
14	Q. 65. And the number at the bottom of the	08:25:15
15	page will say 59, the internal page.	08:25:18
16	A. Oh, okay. Sorry. Thank you. 59.	08:25:21
17	Okay. Got it.	08:25:32
18	Q. And you see here the heading that starts	08:25:33
19	with Claim 8?	08:25:37
20	A. Yes.	08:25:39
21	Q. Okay. And in this section, you are	08:25:41
22	discussing the Xu reference and your opinion that the	08:25:47
23	Xu reference invalidates Claim 8 of the '384 patent.	08:25:53
24	Is that right?	08:25:59
25	A. That's right.	08:25:59

1	Q.	Okay. And part of your argument revolves	08:26:03
2		around, as you say in Paragraph 115, "Xu discloses	08:26:09
3		that spacers 152 may be formed by depositing a silicon	08:26:14
4		nitride layer"; correct?	08:26:21
5	A.	That is correct.	08:26:22
6	Q.	And you agree that Xu does not disclose any	08:26:22
7		particular method of depositing a silicon nitride	08:26:33
8		layer; correct?	08:26:37
9	A.	So in Column 6, Xu says that the spacers may	08:28:09
10		include multi-layer structure, such as multi-layer	08:28:19
11		structure including silicon nitride and silicon oxide	08:28:23
12		layer. A spacer of formed by a suitable process to a	08:28:28
13		suitable thickness. Spacer may be formed by	08:28:33
14		depositing silicon nitride layer and then dry etching	08:28:38
15		the layer to form the spacer, as illustrated in	08:28:43
16		Figure 2.	08:28:47
17		So although Xu did not -- does not say	08:28:51
18		specifically what deposition -- specifically what	08:29:04
19		deposition method is used to deposit silicon nitride	08:29:13
20		layer, however, the description in Column 4 strongly	08:29:19
21		indicate that a person of ordinary skill would	08:29:39
22		understand that it would be obvious that the	08:29:46
23		depositing silicon nitride would conformally cover the	08:29:48
24		gate structure, followed by etching of the silicon	08:29:55
25		nitride to form the spacer.	08:30:03

1	Q.	Okay. And to support your opinion that a	08:30:05
2		person of skill in the art would have known that the	08:30:14
3		silicon nitride would be laid conformally, in	08:30:16
4		Paragraph 116, you point to a reference numbered	08:30:21
5		Exhibit 1025.	08:30:25
6		Do you see that?	08:30:26
7	A.	Yes.	08:30:27
8	Q.	Here, let's go to the Xu reference.	08:30:28
9		Can you open Exhibit 1004, please?	08:30:55
10	A.	Yes.	08:31:01
11	Q.	And please turn to Figure 1. Let me know	08:31:01
12		when you're there.	08:31:19
13	A.	Okay. Figure 1.	08:31:30
14	Q.	And so Figure 1 is a flow diagram for the	08:31:32
15		embodiment of Xu that you referred to in Column 6;	08:31:39
16		right? Excuse me. Column 4. Well, and also	08:31:44
17		Column 6.	08:31:54
18	A.	Sorry. Hold on one second. The Column 4,	08:31:55
19		we just read about the spacer. I believe that it is	08:33:19
20		referred to not just Figure 1, but also Figure 2 to 6	08:33:25
21		that provide various prospective views of the FinFET.	08:33:31
22	Q.	Correct. My question was, Figure 1 is a	08:33:34
23		flow diagram that relates to Figures 2 through 6.	08:33:39
24		And if you need some reference, you can look	08:33:46
25		at Column 1, Lines 49 through 53.	08:33:49

1	A.	Yes.	08:34:00
2	Q.	And so Figure 1 is a flow diagram	08:34:01
3		corresponding to Figures 2 through 6, which is the	08:34:09
4		embodiment that you pointed to in Columns 4 and 6 for	08:34:15
5		this issue; correct?	08:34:19
6	A.	Did you say Figure 2 to 6, right, not 3 to	08:34:20
7		6?	08:34:29
8	Q.	Correct.	08:34:29
9	A.	Okay. Yes. Yeah, Figure 1 is the flow	08:34:30
10		diagram. And Figure 2 to 6 illustrate the -- what the	08:34:33
11		FinFET structure looked like.	08:34:47
12	Q.	Okay. Nothing in Figure 1 discusses the	08:34:50
13		process for forming spacers 152; correct?	08:34:56
14	A.	Yeah, I think Figure 1 is just a very	08:35:01
15		high-level summary of the process flow; however, the	08:35:38
16		specifications provide a lot more details.	08:35:50
17		And as we read previously, that this -- in	08:35:54
18		Column 4 of Xu discuss about how the spacers are	08:36:07
19		formed, how they were etched.	08:36:14
20	Q.	Right. My question is just that Figure 1	08:36:26
21		does not discuss the process for forming spacers 152.	08:36:34
22		Do you agree with that?	08:36:40
23	A.	Again, Figure 1 is really high-level	08:36:41
24		summary. In fact, it doesn't talk much -- doesn't say	08:37:11
25		anything about the spacers. So I think a person of	08:37:14

1	ordinary skill in the art reading the patent would not	08:37:20
2	take Figure 1 out of context about the -- the process,	08:37:25
3	because the specification definitely provide a lot	08:37:38
4	more detail.	08:37:41
5	But to answer your question, yes, Figure 1	08:37:42
6	does not say the process related to forming the	08:37:44
7	spacers. And, however, as I mentioned that, the	08:37:54
8	details are provided in the specifications.	08:38:00
9	Q. And in Figures 2 through 6, spacers 152 are	08:38:06
10	present; correct?	08:38:16
11	A. That's correct. That spacer is labeled 152	08:38:18
12	in Figure 1 through -- 2 to 6.	08:38:41
13	Q. There is no depiction of the before and	08:38:46
14	after regarding the creation of spacers 152 as	08:38:55
15	described in Column 4 that you pointed me to earlier;	08:39:01
16	correct?	08:39:06
17	A. When you say before and after, what do you	08:39:06
18	mean by that?	08:39:37
19	Q. Maybe I can ask you a different way.	08:39:38
20	So you pointed me to a process in Column 4	08:39:45
21	for creating the spacers 152.	08:39:48
22	My question --	08:39:50
23	A. Yes.	08:39:51
24	Q. -- is simply, there is no depiction of that	08:39:51
25	process; right? And what I mean is that in the first	08:39:55

1	figure, the spacers are already there.	08:39:58
2	MR. BRADLEY: Objection. Form.	08:40:02
3	THE WITNESS: When you say the first figure,	08:40:03
4	do you mean Figure 2?	08:40:08
5	BY MR. DOKHANCHY:	08:40:09
6	Q. Yes.	08:40:09
7	A. Mm-hmm. Yes. In Figure 2, the spacer is	08:40:09
8	already indicated as Label Number 152.	08:40:18
9	Again, that figure is one thing, and the	08:40:30
10	descriptions of the spacer formations has a lot more	08:40:38
11	detail in the specification.	08:40:48
12	Q. Right. I'm just asking about the figures.	08:40:52
13	I understand your position that there is a description	08:41:01
14	of the process in the specification. I just want to	08:41:03
15	make sure we're in agreement on this point.	08:41:09
16	So the question is, there is no depiction in	08:41:11
17	the figures of the process described in Column 4 for	08:41:14
18	creating the spacers 152; correct?	08:41:20
19	MR. BRADLEY: Objection. Form.	08:41:25
20	THE WITNESS: So there is no depictions of	08:41:27
21	what the device looked like prior to the spacer	08:41:37
22	formation in Figure 2 to 6. Figure 2 to 6 show the	08:41:42
23	device which has already had the spacer formed using a	08:41:54
24	suitable process followed by a dry etching of a layer	08:42:08
25	to form the spacer, as illustrated in Figure 2.	08:42:25

1	BY MR. DOKHANCHY:	08:42:32
2	Q. And your contention is that a person of	08:42:34
3	skill in the art would know that the silicon nitride	08:42:38
4	layer described as being laid down at some point	08:42:43
5	before Figure 2 would be a conformal layer; correct?	08:42:50
6	A. This is spacer technology has been around	08:42:56
7	for many, many years.	08:43:09
8	What is that? I'm sorry.	08:43:12
9	And the fact that Xu mentioned that the	08:43:15
10	spacer are deposit -- are formed by depositing a	08:43:28
11	silicon nitride layer and then dry etching to form the	08:43:36
12	spacer, a person of ordinary skill in the art reading	08:43:41
13	this would understand that the silicon nitride is	08:43:47
14	deposited conformally, covering the gate structure.	08:43:53
15	Because the dry etching is an isotropic etch, and it	08:44:03
16	is a method of choice in forming the spacer.	08:44:15
17	So in order for it to form the spacers, in	08:44:29
18	general, by 2013, the materials such as silicon	08:44:35
19	nitride were typically formed by depositing using	08:44:47
20	conformal deposition. And it is a very standard	08:44:52
21	process.	08:44:59
22	Conformal means that they follow the contour	08:45:01
23	of the step. And using very conventional chemical	08:45:05
24	vapor depositions such as low-pressure deposition --	08:45:17
25	low-pressure chemical depositions or plasma-enhanced	08:45:21

1	depositions, those are the widely used deposition	08:45:25
2	process which form a conformal deposition. This is	08:45:35
3	then subsequently followed by a dry etching, which is	08:45:42
4	an isotropic or sometimes called the directional etch.	08:45:54
5	So if you can imagine that the silicon	08:46:00
6	nitride is formed conformally, allowing the gate	08:46:04
7	structure. So, therefore, the vertical distance on	08:46:12
8	top of the gate and on top of the wafers will be less	08:46:17
9	than the vertical distance right next to the gate	08:46:22
10	because the gate is a tall structure.	08:46:30
11	So when you do a directional etch, it will	08:46:32
12	etch the silicon nitride on top of the gate and also	08:46:37
13	on top of the wafer, what you leave behind is a	08:46:43
14	silicon nitride layer on the sidewall of the gate.	08:46:48
15	And Xu explicitly say that dry etching is used to etch	08:47:01
16	the silicon nitride layer to form the spacer.	08:47:10
17	So it is very clear that in order for -- to	08:47:15
18	form that spacer using dry etching silicon nitride, is	08:47:21
19	and must be formed conformally on the gate structure.	08:47:30
20	Q. A dry etch does not have to be anisotropic,	08:47:38
21	correct, it could be a dry isotropic etch; right?	08:47:52
22	MR. BRADLEY: Objection. Form.	08:47:56
23	THE WITNESS: Dry etch depends on how the	08:47:57
24	dry etching is done, but typically, dry etching is a	08:48:05
25	process which would primarily be anisotropic.	08:48:12

1	Now, of course, one can design it in such a	08:48:25
2	way that it still have some isotropic component, but	08:48:33
3	in general, especially forming the spacers, the	08:48:38
4	purpose of dry etching is primarily result in	08:48:47
5	anisotropic etch, meaning directional etch, at very	08:48:57
6	little isotropic component.	08:49:02
7	BY MR. DOKHANCHY:	08:49:08
8	Q. The Xu reference does not say one way or	08:49:08
9	another whether its dry etch is isotropic,	08:49:11
10	anisotropic, or something in between.	08:49:17
11	Is that correct?	08:49:20
12	A. I don't think Xu need to say anything about	08:49:21
13	forming the spacer, whether it's isotropic or	08:49:39
14	anisotropic. A person of ordinary skill in the art	08:49:45
15	understanding the formation of spacer would	08:49:49
16	immediately understand that the dry etching to form	08:49:56
17	the spacer, that the dry etching of the silicon	08:50:00
18	nitride layer is -- is a anisotropic etching method.	08:50:06
19	Q. Xu does not say that its dry etch is	08:50:16
20	anisotropic; correct?	08:50:23
21	A. Xu does not say dry etching is anisotropic	08:50:26
22	in Column 4, but it doesn't need to because it's well	08:50:32
23	understood that it is anisotropic etching to form the	08:50:37
24	spacer.	08:50:43
25	A person of ordinary skill in the art	08:50:45

1	working in the semiconductor industry -- and spacer	08:50:47
2	formation has been around probably since 1980s -- is	08:50:51
3	well understood that the method to form the spacer is	08:50:57
4	by etching the silicon nitride layer by dry etching,	08:51:04
5	which is an anisotropic etch method.	08:51:12
6	Q. Spacers of this type can and have been	08:51:19
7	formed with isotropic etches; agreed?	08:51:26
8	A. So a person of ordinary skill in the art	08:51:31
9	would understand that the spacer formation step which	08:53:01
10	is depositing a conformal material and then etching	08:53:07
11	onto -- the nitride on top of the wafers, in other	08:53:15
12	words, until the isolation structure is exposed. And	08:53:22
13	that is the conventional spacer formation process	08:53:28
14	using anisotropic etch back.	08:53:34
15	Isotropic etch will remove material from	08:53:43
16	vertical direction at the same -- at substantially the	08:53:48
17	same grade as horizontal surface in the horizontal	08:53:54
18	direction, and it will not leave a well-defined spacer	08:54:01
19	as described in Claim 8.	08:54:07
20	So I don't recall any isotropic etching	08:54:12
21	being used to form standard spacer such as in the	08:54:24
22	FinFET. In long time back in 1980s so-called LDD	08:54:35
23	device, lightly doped drain device.	08:54:44
24	So if you ask me, have spacer ever been	08:54:48
25	formed using isotropic etch, in the mainstream CMOS	08:54:50

1	and FinFET, the answer is no. Not for LDD device.	08:55:00
2	Not for self-aligned silicide. Not for source drain	08:55:06
3	alignment. Not for spacer formations.	08:55:11
4	So there has been other process such as	08:55:22
5	reflow base part -- spacer, but those are not	08:55:26
6	isotropic etch-back process to form the spacer in any	08:55:31
7	sense.	08:55:40
8	Q. What is a reflow base spacer?	08:55:42
9	A. Well, that is a very old process. So the	08:55:49
10	reflow base process -- reflow base spacer formed by,	08:56:19
11	first, you still deposit a conformal material, and	08:56:26
12	then you heat the wafer above the certain temperature	08:56:31
13	called softening temperature. And you allow the	08:56:40
14	material to reflow, and you leave behind the material	08:56:52
15	along the vertical etch.	08:56:57
16	That's the highlight description of what is	08:57:00
17	a reflow based. So the detail is that you first form	08:57:07
18	material conformal deposition such as nitride or	08:57:14
19	phosphatidic gas, so-called EPSG. And then you do a	08:57:28
20	thermal reflow.	08:57:34
21	And when you do the reflow above the	08:57:37
22	softened temperature, the material will soften and	08:57:51
23	flows. And it will thin on the flat horizontal region	08:57:56
24	and accumulate at the corner and vertical edge due to	08:58:05
25	surface tension. And the result is that the material	08:58:09

1	remain thicker -- thicker along the sidewall of a	08:58:12
2	structure such as a gate.	08:58:24
3	So this is -- this is -- gives rise to	08:58:27
4	spacer-like structure, but reflow base is not a very	08:58:31
5	good method. And it's very rare for modern CMOS	08:58:35
6	because, you know, imagine that you're relying on the	08:58:45
7	material to reflow, the dimensional control is very	08:58:49
8	poor, and you also have rounded edge, which that's not	08:58:54
9	help for nanoscale device. And, therefore, it's very	08:59:01
10	difficult to scale below nanoscale dimensions.	08:59:07
11	So that is why reflow-based spacer is not	08:59:15
12	used anymore. But that was one of those that appears	08:59:23
13	in research-type journal papers and research lab, but	08:59:30
14	I don't think it ever implemented in standard CMOS	08:59:41
15	industrial, practical applications.	08:59:49
16	Q. And why would it be important for the reflow	08:59:52
17	method for the deposition to be conformal if the	09:00:00
18	heating step is going to reflow the layer anyways?	09:00:06
19	A. Well, even though the material has to be	09:00:13
20	reflowed, you still have to have started out with some	09:00:18
21	material sticking to the sidewall of the structure,	09:00:22
22	and also on the top. It's not like you can just put	09:00:28
23	it on the top and it will reflow completely. Yeah.	09:00:34
24	So, you know, you still need -- it's not	09:00:40
25	like reflow would just -- if you just deposit it on	09:00:43

1	the isolation, it's not going to reflow up to the --	09:00:47
2	up to the sidewall at all.	09:00:51
3	Q. Mm-hmm.	09:00:54
4	A. Yeah.	09:00:56
5	Q. But you would agree, it wouldn't need to be	09:00:56
6	strictly conformal, in that, this process wouldn't	09:00:59
7	require the deposited layer to be the same thickness	09:01:04
8	on the sidewall and the top? You're just saying that	09:01:07
9	there needs to be some thickness on the sidewall;	09:01:12
10	correct?	09:01:16
11	MR. BRADLEY: Objection. Form.	09:01:16
12	THE WITNESS: You know, to tell you the	09:01:26
13	truth, you ask me something that I did not address in	09:01:49
14	my reply -- in my declaration. And -- but -- so I'm	09:01:56
15	not really prepared to answer these questions, but	09:02:06
16	the -- to tell you the answer, is that the -- it does	09:02:13
17	not have to be strictly -- for reflow-based process,	09:02:32
18	it does not have to be strictly conformal deposition;	09:02:36
19	however, it does require the material to be	09:02:44
20	distributed on all the surfaces.	09:02:56
21	But if the initial film is slightly thicker	09:03:09
22	on the horizontal surface or somewhat longer form,	09:03:17
23	reflow would still cause some redistribution. So as a	09:03:21
24	result, the spacer formation will still form driven by	09:03:36
25	surface tension rather than sidewall using anisotropic	09:03:41

1	etch-back such as the conventional way of forming	09:03:50
2	spacer.	09:03:55
3	But in any case, obviously we're not here to	09:04:00
4	talk about reflow-based spacer process.	09:04:04
5	BY MR. DOKHANCHY:	09:04:08
6	Q. Okay. Well, let's talk about the methods	09:04:08
7	you did opine on in your report.	09:04:12
8	Can you explain what low-pressure CVD is?	09:04:14
9	A. I think I might have talked about that. Let	09:04:18
10	me see.	09:04:36
11	Q. So Paragraph 116 that -- where we were	09:04:42
12	looking at earlier is where you discuss the concept in	09:04:45
13	relation to Claim 8.	09:04:48
14	A. Right. No, I'm trying to see whether I	09:04:50
15	discussed that during the technology background.	09:04:58
16	Let's see. Let me search for it.	09:05:17
17	So, first, let's talk about what is CVD,	09:05:27
18	right. CVD is chemical vapor deposition. It is a	09:05:34
19	process where you deposit a thin film, such as silicon	09:05:40
20	nitride, on the substrate by introducing reactive	09:05:43
21	gases that are chemically reacted or chemically	09:05:47
22	decomposed on the wafer to form solid material. Okay.	09:05:55
23	So, for example, silicon nitride -- silane,	09:06:06
24	SiH ₄ , if you put in silane in the chamber, it will	09:06:09
25	associate to silicon and hydrogen. Then silicon will	09:06:16

1	condense and deposit on the surface. But if you put	09:06:22
2	that on silane and phosphine -- sorry -- silane and	09:06:33
3	ammonia, that would react -- the silane would react	09:06:39
4	with ammonia to form silicon nitride. Silane is SiH_4 ,	09:06:59
5	ammonia is NH_3 , and silicon nitride is Si_3N_4 .	09:07:08
6	So if you add -- the chemical reaction is	09:07:14
7	when you have three SiH_4 plus four NH_3 , it will form	09:07:17
8	Si_3N_4 -- Si_3N_4 , which is nitride, plus 12 hydrogen as	09:07:30
9	a by-product. So silane is supplying the silicon	09:07:38
10	component, and ammonia, NH_3 , will supply the nitrogen	09:07:43
11	component, and the by-product is the hydrogen gas.	09:07:50
12	Okay. So that's what CVD is. Low-pressure	09:08:06
13	CVD is low-pressure chemical vapor deposition. Low	09:08:11
14	pressure means that it's below the atmospheric	09:08:19
15	pressure, usually about ten, 200, maybe even 1,000,	09:08:27
16	maybe more. And the temperature, depending on the	09:08:31
17	process, around 500 to 900 degrees C, it could be	09:08:34
18	either a single wafer process or etch furnace-type or	09:08:38
19	furnace-base batch process. Okay.	09:08:45
20	The low pressure means that the gas molecule	09:08:55
21	is -- is not so close together. And so what it means	09:09:04
22	is that the mean free path of gas molecule is	09:09:15
23	increased. And because the mean free path is	09:09:24
24	increased, that would create a uniform -- a good	09:09:31
25	uniformity across the wafer. And that -- and that	09:09:37

1	would result in conformality of the film, even in a	09:09:45
2	high aspect ratio structure.	09:09:51
3	So the low-pressure CVD will give you --	09:09:56
4	it's known to give you so-called a good step coverage,	09:10:04
5	meaning a conformal deposition.	09:10:07
6	And you also can have plasma-enhanced CVD	09:10:13
7	that is -- that the energy is coming from the plasma	09:10:22
8	rather than thermal energy as in the low pressure CVD	09:10:29
9	so that you can achieve deposition at lower	09:10:36
10	temperature, but what it means is that the pressure is	09:10:40
11	usually higher, and such that the conformality is not	09:10:46
12	as good as low pressure CVD.	09:10:53
13	And in the old days, before these two type	09:11:00
14	of processes invented, usually you use atmospheric	09:11:03
15	pressure CVD. And the pressure is high, the	09:11:09
16	temperature is high, conformality is usually poor, but	09:11:12
17	those are the older oxide deposition film. Deposition	09:11:17
18	process.	09:11:22
19	Does that answer your question?	09:11:30
20	Q. Yes, it does, you know, I think for the time	09:11:31
21	being.	09:11:34
22	Although, when you're referring to the	09:11:34
23	conformality being poor --	09:11:39
24	A. I'm not -- I'm saying that the old process	09:11:43
25	is poor. The LPCVD process is excellent.	09:11:46

1 Q. What are the -- some of the older processes? 09:11:51
2 Is there an acronym besides CVD that you're referring 09:11:55
3 to? 09:11:59
4 A. Well, I'm talking about atmospheric -- I'm 09:11:59
5 focusing on chemical vapor deposition. Atmospheric 09:12:04
6 deposition -- atmospheric pressure CVD would result in 09:12:10
7 a conformality not as good as low-pressure CVD. 09:12:16
8 Are you asking me about even other process? 09:12:30
9 Q. Yeah, exactly. I'd like to get your full 09:12:34
10 sense of what the available processes were to deposit 09:12:37
11 silicon nitride around the time of the Xu reference. 09:12:41
12 So we've established LPCVD, PECVD, and 09:12:46
13 atmospheric pressure CVD. 09:12:52
14 My question is, what other methods besides 09:12:55
15 CVD would have been available to deposit silicon 09:13:00
16 nitride in the Xu reference? 09:13:04
17 A. Around that time, Xu -- let's see. Which is 09:13:06
18 in 2010 was filed, and this issue in 2015. There 09:13:25
19 might be many other deposition process, but it will be 09:13:39
20 silly for anyone to use older technology to form the 09:13:44
21 spacer other than LPCVD, which is very common, 09:13:49
22 reliable process. 09:13:56
23 And so you're asking me whether there are 09:13:58
24 other deposition of silicon nitride process? 09:14:37
25 Q. Correct. 09:14:40

1 A. Well, I think that the -- a POSITA 09:15:21
2 understanding the deposition of silicon nitride 09:15:24
3 process around 2010, 2015 would just think of 09:15:27
4 conventional CVD, meaning LPCVD or plasma-enhanced 09:15:36
5 CVD, and LPCVD give you a better conformality. And 09:15:45
6 they would not think of other deposition process such 09:15:50
7 as PE -- AP, atmospheric pressure CVD process. 09:15:55
8 Q. What other processes besides LPCVD, PECVD, 09:16:05
9 and APCVD, were available in 2010 to deposit silicon 09:16:15
10 nitride? 09:16:22
11 A. There is also another -- another process, 09:16:22
12 which is called the ALD silicon nitride, which stand 09:16:25
13 for atomic layer deposition, which is an advanced thin 09:16:33
14 film deposition technique that would grow material one 09:16:55
15 atomic layer at a time. And it is very 09:16:58
16 well-controlled, well -- excellent conformality, and 09:17:12
17 had very good thickness control, excellent 09:17:22
18 conformality because of the self-limiting surface 09:17:27
19 reaction type. 09:17:32
20 So one can use that, but in general, not -- 09:17:35
21 this is mainly used for the gate oxide, the high-K 09:17:55
22 dielectric, but in -- what is it? 2010, 2015? 09:18:08
23 Around that time, Xu, in general, is used 09:18:16
24 LPCVD or PECVD silicon nitride. 09:18:23
25 ALD was not generally used and not required 09:18:29

1 because the feature size were larger than what it is 09:18:32
2 today. And LPCVD provides sufficient conformality. 09:18:36
3 And throughput is more important in manufacturing, and 09:18:44
4 so that would favor CVD. 09:18:57
5 Imagine if you do ALD, right, one atomic 09:19:00
6 layer at a time. Yes, it is very precise, very 09:19:06
7 conformal, very well atomic layer, you know, CDD 09:19:10
8 control, critical dimension control, but the drawback 09:19:19
9 is that it is a much slower process. 09:19:23
10 So in the year where Xu patent was filed and 09:19:28
11 issued, the method of choice for depositing silicon 09:19:37
12 nitride is LPCVD silicon nitride or PECVD silicon 09:19:46
13 nitride, followed by anisotropic etch-back, that would 09:19:53
14 result in spacer forming on the sidewall of the gate. 09:19:58
15 Q. Does atmospheric pressure CVD have any 09:20:02
16 advantages over PECVD or LPCVD? For example, cost, 09:20:09
17 complexity, speed, or anything else? 09:20:15
18 MR. BRADLEY: Objection. Form. 09:20:21
19 THE WITNESS: The problem with atmospheric 09:20:22
20 CVD, the -- the control of the process is very poor. 09:20:54
21 So even for those dimension around 2013, which is, 09:21:12
22 like, 22 nanometer, technology now would not be 09:21:23
23 sufficient. So that's why APCVD is rare for spacer, 09:21:28
24 because it just does not provide the sufficient 09:21:36
25 conformality and uniform thickness and having control 09:21:41

1 etch-back. And also that -- because the -- it is done 09:21:50
2 in an atmospheric, there is a lot of contaminations. 09:22:00
3 Are there any advantage? I don't -- at top 09:22:04
4 of my head, I don't see any advantages. When -- 09:22:08
5 unless -- unless you're working in the research lab, 09:22:14
6 you can't afford LPCVD or PECVD. But in general, all 09:22:21
7 manufacturing have PECVD and LPCVD process. 09:22:29
8 Yeah, I don't see any advantage other than 09:22:37
9 many -- lots of disadvantage of using APCVD process to 09:22:40
10 form spacer. 09:22:46
11 BY MR. DOKHANCHY: 09:22:48
12 Q. So you wouldn't agree that APCVD is less 09:22:49
13 complex than PECVD and LPCVD. 09:22:52
14 Is that what you're saying? 09:22:59
15 MR. BRADLEY: Objection. Form. 09:23:00
16 THE WITNESS: Well, I don't understand what 09:23:01
17 you mean by less complex. 09:23:03
18 For the process engineers around the time of 09:23:08
19 the Xu reference, all these processes are not complex 09:23:16
20 at all. And so I wouldn't say that APCVD have the 09:23:26
21 advantage of simplicity because by the time 2010, 09:23:37
22 2015, LPCVD is such a conventional process. It's -- 09:23:47
23 one of ordinary skill in the art would not consider 09:23:57
24 that as complex at all. In fact, they would consider 09:24:00
25 that as fairly straightforward and simple process. 09:24:07

1	BY MR. DOKHANCHY:	09:24:15
2	Q. That's fine. My question was different.	09:24:15
3	I'm comparing APCVD to LPCVD.	09:24:17
4	Simply by virtue of the fact that you don't	09:24:24
5	need to create a vacuum, you would agree that APCVD is	09:24:26
6	simpler and less complex, setting aside whether you	09:24:30
7	think LPCVD in the abstract is complex or not; right?	09:24:35
8	A. Well, creating a vacuum is simply require a	09:24:40
9	pump. Okay. It's not -- it's not complicated.	09:24:47
10	And --	09:24:53
11	Q. That's not required in APCVD; right?	09:24:53
12	A. No. Because it's atmospheric. But one have	09:24:58
13	to consider the advantages and disadvantages. And,	09:25:05
14	yeah, no vacuum pump is required. That doesn't mean	09:25:10
15	that it is so complicated to add a vacuum pump.	09:25:15
16	Q. I understand. That's not the question I'm	09:25:27
17	asking you.	09:25:30
18	So similarly, APCVD does not require	09:25:31
19	introduction of plasma into the process the way that	09:25:34
20	plasma-enhanced CVD requires and is, thus, simpler in	09:25:40
21	that regard, too; correct?	09:25:46
22	A. Well, more importantly, LPCVD actually	09:25:49
23	provide advantage of better conformality compared to	09:25:53
24	PECVD. So that's why in general for the spacer	09:26:01
25	application in 2010/2015, that LPCVD is used because	09:26:03

1 of a good conformality. 09:26:09

2 And so I'm not sure why anyone would use 09:26:13

3 APCVD. It's like you driving a car with auto 09:26:23

4 steering. And you say, "Well, if I go back to 09:26:38

5 Model T, it doesn't have auto steering," would be much 09:26:44

6 simpler. Would be ironic to think that, "Oh, let's -- 09:26:47

7 let's use Model T kind of car because it's almost 09:26:53

8 simpler." It doesn't have a -- it doesn't have auto 09:26:57

9 steering, it doesn't have fuel injection. It's just 09:27:01

10 idiotic to think that, "Yeah, let's use the cheaper 09:27:08

11 one, simpler." 09:27:12

12 So that's the analogy that one would see 09:27:19

13 that in terms of choosing the appropriate CVD process 09:27:22

14 for the spacer application. 09:27:28

15 Q. Okay. And I know we've been going almost an 09:27:35

16 hour and a half, so I just have one more question on 09:27:38

17 this point. 09:27:41

18 We've mentioned LPCVD, APCVD, PECVD, ALD. 09:27:42

19 What other methods of depositing silicon 09:27:50

20 nitride were available in 2010 to 2015? 09:27:52

21 A. First of all, like I said, that those are 09:27:55

22 the -- LPCVD -- are the, you know, process of choice. 09:28:15

23 So you're asking me that by around that time, what 09:28:51

24 other methods, other than APCVD, LPCVD, and PECVD. 09:28:57

25 Well, I already talk about atomic layer 09:29:09

1	deposition.	09:29:15
2	Q. Yeah. So my question is, other than those	09:29:28
3	four, what were the other options?	09:29:30
4	A. So there are other, you know, if you look at	09:29:33
5	textbook about fabrication, there are other	09:29:45
6	processing, but those are not suitable for this	09:29:51
7	application of silicon nitride for conformal spacer	09:29:58
8	application.	09:30:02
9	For example, there is high-density plasma	09:30:04
10	CVD is a plasma base using very high ionic density.	09:30:07
11	And the advantage is that it can fill very high aspect	09:30:16
12	ratio trench, but it's more common for oxide, not for	09:30:21
13	nitride.	09:30:27
14	There is also physical vapor deposition,	09:30:32
15	PVD, but that's rarely used for nitride application.	09:30:36
16	There is also MOCVD, metal organic CVD, but	09:30:45
17	that's not used for CMOS applications, mostly used for	09:30:53
18	III-V application.	09:31:00
19	I mean, again, I was not preparing to answer	09:31:04
20	these questions. I'm more focusing on the IPR, so --	09:31:10
21	I mean, there are other applications, other methods	09:31:21
22	that go on and on. Epitaxial, but that's not used for	09:31:27
23	CVD process -- that's not used for spacer application.	09:31:33
24	Spin-on nitride, but that's very poor process for	09:31:41
25	thickness control and density control.	09:31:48

1	I mean, there is thermal nitridation that's	09:31:51
2	used for very, very thin silicon nitride process, not	09:32:04
3	used for spacer application.	09:32:08
4	So to answer your question, is that for a	09:32:10
5	person of ordinary skill in the art looking at the	09:32:13
6	choices, it's really limited to LPCVD and PECVD for	09:32:15
7	silicon nitride spacer deposition process around 2010,	09:32:26
8	2015. And it's -- and LPCVD would have a little	09:32:31
9	better conformality compared to PECVD.	09:32:39
10	Q. All right. Why don't we take a ten-minute	09:32:47
11	break.	09:32:50
12	A. Okay. Thank you.	09:32:50
13	THE VIDEOGRAPHER: Going off the record at	09:32:51
14	9:32 a.m.	09:32:54
15	(OFF THE RECORD AT 9:32 a.m. PT.)	09:32:54
16	(ON THE RECORD AT 9:42 a.m. PT.)	09:42:41
17	THE VIDEOGRAPHER: We're back on record at	09:42:23
18	9:42 a.m.	09:42:40
19	BY MR. DOKHANCHY:	09:42:41
20	Q. Dr. Lee, let's go back to your declaration,	09:42:43
21	Paragraph 116 that we've been looking at. Regarding	09:42:47
22	Claim 8. Let me know when you've got that up.	09:42:52
23	A. Yep. Yes.	09:42:55
24	Q. And as we just talked about, in this time	09:42:56
25	period, some deposition methods were more suitable for	09:43:01

1	different applications, for example, you expressed	09:43:09
2	some deposition methods that were really only used for	09:43:14
3	gate oxides and not spacers; correct?	09:43:19
4	A. Yeah. Yes. That's right, depending on what	09:43:25
5	material -- what application you want to use, there is	09:43:31
6	usually an appropriate or more suitable deposition	09:43:36
7	process.	09:43:39
8	Q. And the claim at issue here requires	09:43:40
9	depositing a material layer to conformally cover	09:44:11
10	specifically the gate structure and the fin structure.	09:44:14
11	Do you see that in Claim 8?	09:44:17
12	A. Yes.	09:44:19
13	Q. And you point in Paragraph 116 to	09:44:20
14	Exhibit 1025.	09:44:30
15	MR. DOKHANCHY: So let's go ahead and share	09:44:31
16	that exhibit, please, so Dr. Lee can download it.	09:44:32
17	Exhibit 1025.	09:44:37
18	THE TECHNICIAN: Stand by, please.	09:44:38
19	And Exhibit Number 1025 is available now.	09:44:49
20	BY MR. DOKHANCHY:	09:44:54
21	Q. Dr. Lee, are you able to access	09:44:54
22	Exhibit 1025?	09:44:56
23	A. One second, please.	09:44:57
24	Q. Do you have the exhibit, Dr. Lee?	09:46:51
25	A. Yes. Is this the excerpt from Stanley Wolf?	09:46:54

1	Q.	Yes.	09:47:03
2	A.	Yes.	09:47:08
3	Q.	Okay. And then we saw in your declaration,	09:47:09
4		you rely on this exhibit for the argument that PECVD	09:47:20
5		and LPCVD were obvious methods for depositing silicon	09:47:26
6		nitride over the gates and the fins.	09:47:26
7		And my question to you is, Exhibit 1025	09:47:28
8		doesn't say anything about depositing anything over	09:47:32
9		gates or fins specifically; correct?	09:47:38
10	A.	I'm sorry. Let me take a look at this.	09:47:43
11		Okay?	09:47:56
12	Q.	Okay.	09:47:56
13	A.	So your question is that, does this exhibit	09:48:18
14		specifically discuss deposit -- deposition --	09:48:21
15	Q.	On top of gates or on top of fins.	09:48:30
16		MR. BRADLEY: Objection. Form.	09:48:34
17		THE WITNESS: On top of gates or on top of	09:48:35
18		fins?	09:48:47
19		BY MR. DOKHANCHY:	09:48:47
20	Q.	Yes. That's the question.	09:48:48
21	A.	Okay. It's been a while that I look at	09:48:49
22		this. Let me take a look.	09:48:51
23		I think this exhibit discussed deposition on	09:50:21
24		surfaces, such as wafer surfaces, substrate surfaces,	09:50:25
25		and even talk about the chain-to-wall surfaces. And,	09:50:32

1	you know, obviously, the top of the fins is a -- is	09:50:42
2	a -- is part of the substrate surfaces or wafer	09:50:55
3	surface. The gate -- deposit on the gate, the gates	09:51:00
4	are also part of the substrate surfaces and wafer	09:51:07
5	surfaces.	09:51:15
6	So it might not have discussed,	09:51:16
7	specifically, deposition on top of the fins and on top	09:51:22
8	of the gate. A person of ordinary skill in the art	09:51:30
9	would understand that the general discussion of CVD	09:51:35
10	mechanism, such as gas transport, absorption, surface	09:51:42
11	reaction, and deabsorption, and deposition of silicon	09:51:49
12	nitride or silicon oxide, CVD, and step coverage, and	09:51:54
13	whether it's surface reaction limited or mass	09:52:02
14	transport limited regime, and talk about conformal	09:52:06
15	deposition behavior. All of that is applied to the	09:52:09
16	deposition on top of the gate, on the sidewall of the	09:52:19
17	fins, on the gate electrode, or any modern 3D	09:52:22
18	structures.	09:52:28
19	So that's why I cite this exhibit, because a	09:52:30
20	person of ordinary skill in the art reading this would	09:52:39
21	understand that this learning or this teaching from	09:52:43
22	Exhibit 1025 would apply to deposition on top of the	09:52:54
23	fins, on the sidewall of the fins, on top of the gate,	09:53:02
24	on the sidewall of the gate, or on top and around on	09:53:10
25	any surfaces of any modern three-dimensional	09:53:15

1	structure.	09:53:23
2	Q. All right. And your declaration points to a	09:53:28
3	few specific pages that I want to take a look at.	09:53:34
4	A. Okay.	09:53:38
5	Q. In particular, you cite Page 298, noting	09:53:39
6	conformal coverage for PECVD of silicon nitride films.	09:53:48
7	So I want to go to Page 298 --	09:53:58
8	A. Okay.	09:54:01
9	Q. -- of Exhibit 1025.	09:54:01
10	A. One second, please.	09:54:05
11	Q. Okay.	09:54:06
12	A. Which --	09:54:11
13	Q. And -- sorry. Go ahead.	09:54:12
14	A. No, go ahead.	09:54:14
15	Q. So on Exhibit 1025 at page -- this is	09:54:16
16	internal Page 298, I want to ask what you're pointing	09:54:20
17	to for that statement. I believe you're pointing to	09:54:26
18	Table 16-2 and the row labeled "Step coverage."	09:54:29
19	Is that correct? Or are you pointing to	09:54:38
20	something else?	09:54:40
21	A. Which -- okay. Oh, there is one place that	09:54:41
22	shows that low-pressure CVD and PECVD has excellent	09:55:42
23	conformal deposition.	09:55:52
24	THE VIDEOGRAPHER: I'm sorry to interrupt.	09:55:55
25	Dr. Lee, would you mind moving your device	09:55:57

1 just slightly higher? Because it's almost cutting off 09:56:00
2 your eyes. 09:56:03
3 THE WITNESS: I'm sorry. Sorry. 09:56:04
4 Is it better? 09:56:06
5 THE VIDEOGRAPHER: Yes. Thank you. 09:56:08
6 BY MR. DOKHANCHY: 09:56:09
7 Q. And so if you look at the headings in 09:56:14
8 Table 16-2, the one on the left says HTCVD-NP, and the 09:56:17
9 one on the right says PECVD-LP. 09:56:24
10 And so which one of those is PECVD? Which 09:56:30
11 one is LPCVD? 09:56:39
12 A. I think that the right column will -- would 09:56:41
13 include -- let me think. Let me talk -- let me think. 09:57:08
14 Sorry. It has been a while that I seen this. Give me 09:57:15
15 one moment, please. 09:57:18
16 Q. Dr. Lee, would it be helpful if I reasked 10:01:52
17 the question? 10:01:55
18 A. No. I hear your question. You say that -- 10:01:57
19 are you asking me whether Table 16.2 discuss LPCVD? 10:02:00
20 Q. Yeah, I can point you to a page a few 10:02:09
21 earlier. It's 296. 10:02:14
22 A. 296. 10:02:17
23 Q. In the bottom right, about three quarters of 10:02:18
24 the way down, it says Table 16-2 compares the 10:02:27
25 properties of LPCVD and PECVD. 10:02:31

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1 A. Wait. What page are you -- 296? 10:02:35

2 Q. 296, bottom right. 10:02:38

3 A. Right. 10:02:42

4 Q. About ten lines up from the bottom. 10:02:42

5 A. Right. 10:02:45

6 Q. It points out that Table 16-2, the one we 10:02:46

7 were just looking at, compares properties of LPCVD and 10:02:50

8 PECVD. 10:02:53

9 A. Right. 10:02:53

10 Q. And so my question for you is, which one is 10:02:54

11 which? Because I see some different terminology used 10:02:57

12 in the headings. 10:03:02

13 So the question is, in Table 16-2, which 10:03:04

14 process is LPCVD and which process is PECVD? 10:03:08

15 A. Oh, I see your question now. 10:03:12

16 You notice that below what you just said, it 10:03:14

17 says that LPCVD silicon nitride is the most common 10:03:22

18 deposited by reacting dichlorosilane and ammonia at 10:03:26

19 temperature 700 to 800 in hot-wall reactor according 10:03:34

20 to the overall reactions. Okay. 10:03:39

21 So the -- so this is around 700 to 10:03:44

22 800 degrees C. And so the left-hand column, I 10:03:50

23 believe, is the LPCVD nitride process. And it's also 10:03:59

24 called high temperature process because PECVD -- 10:04:08

25 because the energy is coming from plasma, the 10:04:14

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1 temperature can be reduced to 400 -- or, here, it says 10:04:17
2 300. 10:04:24
3 So I believe that in Table 2 -- Table 16.2, 10:04:25
4 the left-hand column is the -- is the LPCVD oxide -- 10:04:32
5 LPCVD nitride. 10:04:43
6 Q. Okay. And if you look at the first row 10:04:44
7 under the heading, there is a line that says 10:04:49
8 composition. 10:04:51
9 Can you see that? 10:04:52
10 A. Yes. 10:04:53
11 Q. And in the left column, we see silicon 10:04:53
12 nitride Si₃N₄, as you said earlier; correct? 10:05:00
13 A. Yep. 10:05:05
14 Q. In the right column, we see SixNyHz, and I 10:05:06
15 believe you would call that silicon hydrazine. 10:05:17
16 Is that right? 10:05:22
17 A. Well, all that means is that they contain 10:05:23
18 hydrogen. And I was -- I'm not sure what you just 10:06:03
19 said. I would say that it's hydrogenated silicon 10:06:16
20 nitride. That's usually what I would call that, 10:06:22
21 hydrogenated silicon nitride. And that's because 10:06:28
22 plasma-enhanced CVD has -- result in a lot more 10:06:31
23 hydrogen compared to LPCVD. 10:06:41
24 Q. Okay. Is hydrogenated silicon nitride the 10:06:46
25 same thing as silicon nitride? 10:06:56

1 A. What do you mean by -- obviously, one has 10:06:58
2 more silicon -- one has contained silicon-hydrogen 10:07:15
3 bond, nitrogen-hydrogen bond. I'm talking about 10:07:27
4 hydrogenated silicon nitride, which typically result 10:07:31
5 from plasma-enhanced CVD. 10:07:36
6 So that material contains silicon-hydrogen 10:07:39
7 bond, nitrogen-hydrogen bond. And the hydrogen 10:07:45
8 content probably have, you know, quite a bit, maybe, I 10:07:54
9 don't know, 10 percent to 30 percent. 10:07:57
10 Q. Yeah, I mean, that is my question. 10:08:06
11 So you agree that hydrogenated silicon 10:08:08
12 nitride and silicon nitride are not the same thing? 10:08:13
13 A. Again, what do you mean by the same thing? 10:08:18
14 It is... 10:08:27
15 Q. Well, it's a pretty simple question. 10:08:42
16 They're either the same or they're not. 10:08:44
17 So are they the same? Or are they 10:08:47
18 different? 10:08:49
19 A. Well, obviously they're not the same because 10:08:49
20 silicon -- you know, the former is different. 10:08:51
21 Obviously, they're not the same thing. 10:08:56
22 But on the other hand, if you ask me whether 10:08:59
23 hydrogenated silicon nitride can be used for the 10:09:02
24 spacer application. And the answer is yes, it can be 10:09:08
25 and actually routinely used for sidewall spacer. 10:09:11

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1 And so it's a very interesting question when 10:09:18
2 you say whether they're the same thing. That's such a 10:09:27
3 non technical term, so I wouldn't know how to answer 10:09:32
4 that. 10:09:36
5 The formula is different. The process is 10:09:41
6 different. So obviously, they're not -- well, I 10:09:43
7 wouldn't even go there when you ask a question like 10:09:51
8 whether they're the same thing. 10:09:55
9 But if you ask whether silicon -- PECVD 10:09:56
10 nitride can be applied for spacer -- it's applicable 10:10:04
11 to spacer application, and the answer is yes. Not 10:10:09
12 only it can be, but it will routinely be used for 10:10:13
13 spacer at the sidewall of a structure such as gate 10:10:16
14 structure. 10:10:22
15 Q. Okay. Can we go ahead and introduce a new 10:10:22
16 exhibit. And it's going to be Exhibit 2004. 10:10:29
17 (DEPOSITION EXHIBIT NUMBER 2004 10:10:29
18 WAS MARKED FOR IDENTIFICATION.) 10:10:34
19 MR. DOKHANCHY: And for the tech, it's 10:10:34
20 Number 01. The title, What is Step Coverage. 10:10:38
21 THE TECHNICIAN: Okay. Thank you, sir. And 10:10:43
22 that's going to be marked as Exhibit 2004? 10:10:49
23 MR. DOKHANCHY: Correct. 10:10:53
24 THE TECHNICIAN: Okay. One second, please. 10:10:54
25 THE WITNESS: I'm sorry. I do not see it 10:11:37

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1 yet. 10:11:39
2 THE TECHNICIAN: No, I'm uploading it right 10:11:40
3 now. 10:11:42
4 Okay. You should be able to see it now, 10:11:54
5 Exhibit Number 2004. 10:11:57
6 BY MR. DOKHANCHY: 10:12:08
7 Q. Let me know if you're able to see that 10:12:08
8 exhibit, Dr. Lee. 10:12:10
9 A. One second, please. 10:12:11
10 Okay. It's a 16-page document. 10:12:49
11 Is that right? 10:12:55
12 Q. Yes. That's right. 10:12:55
13 A. Okay. 10:13:01
14 Q. And you see this is from a furnace 10:13:01
15 manufacturer, Kintek. 10:13:04
16 Have you ever heard of them? 10:13:06
17 A. I don't recall directly. 10:13:08
18 Q. Okay. You see in the title here, the 10:13:11
19 article is talking about step coverage in PECVD? 10:13:14
20 Do you see that? 10:13:21
21 A. The title is "What is Step Coverage in 10:13:22
22 PECVD, and Why is It Important" -- 10:13:27
23 Q. Yeah. 10:13:31
24 A. -- "Ensure Uniform Thin-Film Deposition for 10:13:32
25 Reliability." 10:13:35

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1 Is that what you mean? 10:13:36

2 Q. Yes. 10:13:37

3 A. Yeah. 10:13:38

4 Q. I just want to make sure we're all looking 10:13:39

5 at the same thing. 10:13:41

6 If you could scroll down to the bottom of 10:13:43

7 Page 2, there is a heading that says "The Role of 10:13:48

8 Plasma in Aiding Deposition." 10:13:52

9 A. Yes. 10:13:54

10 Q. And it says, "Unlike purely thermal 10:13:54

11 processes, PECVD uses a plasma to create reactive 10:13:58

12 chemical species at lower temperatures. This has a 10:14:03

13 mixed effect on step coverage." 10:14:07

14 Do you agree with that statement? 10:14:10

15 MR. BRADLEY: Objection. Scope. 10:14:16

16 THE WITNESS: First of all, I hate to read 10:14:18

17 one sentence and take one sentence out of context. So 10:14:42

18 if you give me one moment, please. 10:14:47

19 BY MR. DOKHANCHY: 10:14:50

20 Q. Sure thing. Take your time. 10:14:51

21 A. This is Exhibit 2004; right? Yeah. 10:15:45

22 So the way I see this -- it says that -- 10:16:57

23 after what you just wrote -- after the sentence you 10:17:10

24 just read, the subsequent sentence says that, "The 10:17:13

25 plasma create a high concentration of reactive 10:17:20

1 radicals, which can improve the depositions on -- in 10:17:24
2 shadow regions. However, it also can -- it also 10:17:29
3 create an electric field that can accelerate ion 10:17:34
4 toward the substrate, leading to more a directional, 10:17:38
5 line-of-sight deposition that can worsen the shadowing 10:17:43
6 effect. The key is to balance these competing 10:17:49
7 mechanism." Okay? 10:17:56
8 So it's basically saying that there is two 10:17:58
9 competing effect. One is the radical-driven chemistry 10:18:05
10 that the plasma increases the radical density, and the 10:18:16
11 radicals diffuse relatively uniformly or 10:18:23
12 isotropically, and that can help to reach a sidewall 10:18:32
13 and recess regions. 10:18:37
14 The other competing effect is what they call 10:18:39
15 the ion bombardment. That can reduce the conformality 10:18:42
16 because of the plasma create or form an electric field 10:18:46
17 that can accelerate the ions normal to the substrate 10:18:56
18 as what they call the line-of-sight or quasi 10:19:06
19 line-of-sight component. And -- which can increase 10:19:13
20 the shadowing effect. However, PECVD is still a 10:19:15
21 surface reaction-driven CVD process, not a ballistic 10:19:26
22 physical vapor deposition process. Not like ballistic 10:19:37
23 vapor -- physical vapor deposition. 10:19:43
24 The ion contribution is really a fact of fin 10:19:50
25 density and surface reactions, but the deposition 10:19:54

1 itself is -- is really a chemical -- chemically 10:19:58
2 driven, not ion bombardment. 10:20:08
3 So I believe that I agree with this 10:20:19
4 statement, however, I would say that the -- to some 10:20:21
5 degree, because plasma-enhance CVD deposition remains 10:20:28
6 chemically driven. So ion bombardment, although, does 10:20:35
7 have some electric field effect; however, it is a 10:20:40
8 secondary effect so that it doesn't really influence 10:20:47
9 the conformality very much. 10:20:52
10 But to answer your question whether that 10:20:56
11 statement is true or not, one that you take into 10:21:01
12 account to understand that, yeah, there is some effect 10:21:06
13 and there is some balancing. But in general, the 10:21:09
14 concern about the electric field effect is not really 10:21:16
15 that important. 10:21:20
16 So to answer your question, is that PECVD 10:21:22
17 deposition process still have very good conformality 10:21:29
18 even though it point to the fact that plasma-enhanced 10:21:33
19 could create electric field that might cause shadowing 10:21:37
20 effect and, therefore, might reduce conformality. But 10:21:42
21 that ion bombardment effect is negligible compared to 10:21:47
22 the radical-driven chemistry. 10:21:58
23 Do you understand what I'm saying? 10:22:00
24 Q. I think so. 10:22:01
25 Just so we can get on the same page, what 10:22:03

1 are shadowing effects? 10:22:06

2 A. Well, what they are saying is that there is 10:22:08

3 a line-of-sight deposition. So if you have a gate 10:22:10

4 like this right here standing up, if there is, indeed, 10:22:14

5 a line-of-sight deposit, then this gate will create a 10:22:17

6 shadowing. And you would deposit out here, not right 10:22:24

7 next to the gate. That's, in general, what it means 10:22:28

8 by shadowing effect. 10:22:32

9 Q. Okay. And that's the decreased conformality 10:22:33

10 that you talked about? 10:22:38

11 A. That the -- the paragraphs discuss about 10:22:41

12 that might reduce conformality. But once again, you 10:22:46

13 know, these effects are there, but, you know, which 10:22:52

14 one dominates? But that -- the electric field effect 10:23:00

15 that cause line-of-sight deposition, those are -- that 10:23:04

16 is much less of a issue compared to chemistry-driven 10:23:08

17 deposition. 10:23:15

18 So in short, I think that the 10:23:15

19 plasma-enhanced CVD, a person of ordinary skill in the 10:23:21

20 art would understand that that still give you a very 10:23:25

21 good conformal deposition and good step coverage. 10:23:29

22 Q. If you scroll down a little further, there 10:23:37

23 is another heading that says Key Influencing Factors. 10:23:41

24 Do you see that? 10:23:45

25 A. Right. Yes. 10:23:46

1 Q. And in this section, the authors are 10:23:47
2 discussing the few -- what they call key parameters 10:23:51
3 for achieving good step coverage using PECVD. And 10:23:56
4 they mention -- 10:24:02
5 A. Yes. 10:24:03
6 Q. -- pressure, temperature, precursor gas 10:24:03
7 chemistry, plasma power and frequency. 10:24:07
8 Is that right? 10:24:10
9 A. Yes. 10:24:11
10 Q. Do you agree that those are factors that can 10:24:12
11 impact whether or not the PECVD process is truly 10:24:18
12 conformal? 10:24:23
13 MR. BRADLEY: Objection. Form. 10:24:30
14 THE WITNESS: You're saying that -- 10:24:32
15 obviously -- let's see. 10:25:11
16 You know, obviously that in any process 10:26:37
17 recipe, there are many parameters: Pressure, 10:26:42
18 temperature, precursor gas chemistry, plasma power and 10:26:47
19 frequency. These are all well-established knobs that 10:26:53
20 affect step coverage and conformality. That's well 10:27:03
21 known. And -- because those influence the transport 10:27:06
22 of reactants to serve as mobility the sticking 10:27:15
23 probability and ion directionality. 10:27:27
24 So to answer your question whether I agree 10:27:34
25 with that -- with -- that those are the important 10:27:39

1 parameters that affect conformality, the answer is, 10:27:46
2 yes; but a person of ordinary skill in the art would 10:27:52
3 understand how to adjust these parameters to create a 10:27:58
4 good, conformal deposition. 10:28:07
5 BY MR. DOKHANCHY: 10:28:14
6 Q. Okay. In your declaration, you did not 10:28:15
7 address any of the factors listed here on Page 3 of 10:28:19
8 Exhibit 2004; correct? 10:28:22
9 A. Where are you looking at in my IPR 10:28:27
10 declaration? 10:28:36
11 Q. So the same place we've been looking, 10:28:38
12 Paragraph 116. 10:28:41
13 A. Okay. 10:28:45
14 Q. But -- you can feel free to point me 10:28:45
15 elsewhere, but that's the section where you're 10:28:47
16 discussing silicon nitride being deposited by these 10:28:51
17 techniques, including PECVD. 10:28:57
18 And my question to you is, you did not 10:29:02
19 analyze any of the key influencing factors that 10:29:05
20 determined whether or not the step coverage is 10:29:11
21 conformal in PECVD in your declaration; correct? 10:29:14
22 A. You know, I believe that a person of 10:29:20
23 ordinary skill in the art reading my IPR declaration 10:29:32
24 and looking at the exhibit that I provide will draw a 10:29:36
25 conclusion that Xu prior art satisfy and meet the 10:29:44

1 limitation of Claim 8. 10:29:59
2 Q. Dr. Lee -- 10:30:03
3 A. But may I answer the question? 10:30:04
4 Q. Yeah, I'm asking you to answer the question. 10:30:06
5 The question was, you didn't -- 10:30:08
6 A. Yes. 10:30:10
7 [Simultaneous speaking.] 10:30:10
8 BY MR. DOKHANCHY: 10:30:10
9 Q. -- factors, did you? 10:30:10
10 A. My answer is that I don't think I need to 10:30:13
11 reiterate all the details of the exhibit onto my IPR 10:30:23
12 declaration. 10:30:33
13 A person of ordinary skill in the art would 10:30:36
14 understand that to improve conformality, one would 10:30:39
15 increase the pressure so that you have less 10:30:47
16 line-of-sight problem, increase the substrate 10:30:50
17 temperature so you can increase the atoms' mobility 10:30:57
18 and thickness evening out, and choose the chemistry so 10:31:04
19 that you can have a more concentrated penetration 10:31:09
20 around the gate. And then the plasma, would choose it 10:31:18
21 to have lower power plasma, and adjust it so that it 10:31:23
22 reduce the ion bombardment directionality and also the 10:31:31
23 frequency to -- so that you have lower ion energy. 10:31:36
24 So those are the knobs that a person of 10:31:42
25 ordinary skill in the art would understand. And I -- 10:31:46

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1 that's why I provide this exhibit in my declaration 10:31:52
2 that a person of ordinary skill in the art looking at 10:31:57
3 the -- looking at my IPR declaration and looking at 10:32:02
4 the exhibits would understand that -- the optimal way 10:32:11
5 to achieve good, conformal deposition. 10:32:21
6 Q. All right. Now I'd like an actual answer to 10:32:25
7 my question. I've been pretty patient letting you 10:32:28
8 answer however you want, but I need an actual answer. 10:32:32
9 [Simultaneous speaking.] 10:32:35
10 MR. BRADLEY: Reza, he's answering to the 10:32:35
11 best of his ability. 10:32:38
12 MR. DOKHANCHY: I don't need your 10:32:39
13 commentary, Steve. 10:32:41
14 BY MR. DOKHANCHY: 10:32:42
15 Q. Dr. Lee, you did not address any of the 10:32:43
16 factors listed as key influencing factors in 10:32:45
17 Exhibit 2004 in your declaration; correct? 10:32:50
18 MR. BRADLEY: Objection. Asked and 10:32:52
19 answered. 10:32:53
20 BY MR. DOKHANCHY: 10:33:02
21 Q. You may answer, Dr. Lee. 10:33:03
22 Dr. Lee, what is your answer to my question? 10:33:45
23 A. I am thinking about it, because... 10:33:48
24 So in those paragraphs below the -- Claim -- 10:34:06
25 within the Claim 8, Paragraph 115 to 119. In summary, 10:35:31

1 basically, I indicated that PECVD silicon nitride are 10:35:47
2 well-known prior to provide conformal step coverage 10:35:52
3 over FinFET topology -- topography, by including the 10:35:57
4 vertical gate sidewall in the fin structure. 10:36:06

5 And although I did not cite all the detailed 10:36:10
6 optimizations and precise control over certain 10:36:21
7 parameters, such as pressure, temperature, precursor 10:36:27
8 gas chemistry, and plasma power and frequency, a 10:36:34
9 person of ordinary skill in the art reading my IPR 10:36:37
10 declaration and reading the cited exhibit in that -- 10:36:43
11 in that -- in those paragraph would understand that 10:36:49
12 the conclusion is that Xu does provide a discussion of 10:36:56
13 PECVD silicon nitride in such detail to meet the 10:37:09
14 limitations of Claim 8. 10:37:16

15 And you're the lawyer; you tell me whether I 10:37:19
16 need to re -- you know, rewrite all of the details of 10:37:30
17 my exhibit, how to achieve conformality into my IPR. 10:37:37
18 That would be -- make the IPR declaration be, you 10:37:45
19 know, at least double the size. 10:37:50

20 So answer your question, no, I did not 10:37:53
21 need -- I did not specify all the details of pressure, 10:37:56
22 temperature, precursor gas chemistry, plasma power and 10:38:01
23 frequency, but I don't think I need to. 10:38:07

24 Q. Okay. If you scroll down further in 10:38:09
25 Exhibit 2004, you'll see a heading Understanding the 10:38:14

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1 Trade-Offs on Page 4. Let me know when you get there. 10:38:18
2 A. Yes. 10:38:32
3 Q. Okay. And in this section, the reference is 10:38:32
4 saying, "Optimizing for perfect step coverage," 10:38:35
5 meaning conformality, "does not come without costs. 10:38:40
6 Engineers must balance conformality against other 10:38:44
7 critical manufacturing metrics." 10:38:48
8 Do you agree with that? 10:38:50
9 A. Look, any engineering problem is like 10:38:53
10 juggling a number of ball at the same time. There is 10:39:03
11 always a trade-off. So -- 10:39:07
12 Q. And sometimes in doing that trade-off, you 10:39:23
13 may find other things more important than achieving 10:39:25
14 conformality. 10:39:29
15 That's what they're saying here; right? 10:39:30
16 A. Where are you reading? 10:39:33
17 Q. Under the heading Understanding the 10:39:37
18 Trade-Offs. 10:39:42
19 A. Right. 10:39:42
20 Q. They are talking about the trade-offs that 10:39:43
21 you must consider when deciding whether conformality 10:39:48
22 is important enough to overcome the downsides. And 10:39:55
23 that you may not necessarily pursue conformality at 10:40:02
24 all costs; right? 10:40:07
25 A. Well, it depends on your priority. Depends 10:40:08

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1 on your priority. If your priority is excellent step 10:40:19
2 coverage, yes, it might result in slower deposition 10:40:25
3 break. But that is what engineers do. They look at 10:40:31
4 what is the Number 1 priority that we need to achieve. 10:40:39
5 And for the spacer application, you need 10:40:44
6 conformal deposition. And so if it result in the 10:40:46
7 slower deposition rate, so be it. But, yeah, there is 10:40:53
8 always engineering -- that's what I teach in my class. 10:40:59
9 Engineering is, basically, learning how to deal with 10:41:04
10 trade-off. 10:41:08
11 But in this case where you form -- you want 10:41:09
12 to form a good spacer, you need a conformal 10:41:16
13 deposition. So that's the goal. Yeah. There is -- 10:41:21
14 understanding the trade-off is something that an 10:41:28
15 engineer, a POSITA, would always consider. 10:41:33
16 Q. And you've said that you need a conformal 10:41:40
17 layer, and so if there is a slower deposition rate, so 10:41:47
18 be it. 10:41:51
19 Earlier, you said there is a method called 10:41:53
20 atomic layer deposition that provides excellent 10:41:57
21 conformality but is so slow that people don't use it. 10:42:01
22 So it's not always that you pursue 10:42:08
23 conformality regardless of deposition rate. 10:42:11
24 Is that fair? 10:42:14
25 A. That's not fair. 10:42:15

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1 MR. BRADLEY: Objection. 10:42:16

2 BY MR. DOKHANCHY: 10:42:17

3 Q. Okay. So you do always -- 10:42:17

4 A. Wait, wait. Can I answer your question? 10:42:19

5 Q. Yes. 10:42:24

6 A. You asked me a question; can I answer your 10:42:24

7 question? 10:42:27

8 Q. Please do. 10:42:27

9 A. You said is it fair. Okay? 10:42:27

10 Depends on the application. Okay? Atomic 10:42:29

11 layer deposition is extremely conformal and is 10:42:32

12 extremely well thickness control. Okay? So, 10:42:38

13 therefore, when you deposit a ultra thin layer, such 10:42:44

14 as high-K dielectric layer, which is about 1 nanometer 10:42:49

15 or 1 to 3-nanometer thick, you need extremely well 10:42:56

16 control on the thickness. And not for the 10:43:03

17 conformal -- conformality. That is really mainly for 10:43:07

18 the thickness control. 10:43:12

19 On the other hand, that for spacer 10:43:15

20 applications, yes, conformality is important. And the 10:43:18

21 thickness is much thicker than that of the gate oxide, 10:43:25

22 and, therefore, the conformal -- conformality that can 10:43:33

23 be achieved using LPCVD or PECVD is good enough use 10:43:40

24 for that application. 10:43:49

25 You don't need ALD because ALD is really, 10:43:52

1 primarily, for thickness control for ultra-thin 10:43:58
2 dielectric thickness. We're not talking about that. 10:44:03
3 So it really depends on your application, which 10:44:06
4 process to use. 10:44:10
5 And I'm not saying that, oh, I didn't use -- 10:44:11
6 I think you misunderstand my earlier comment that 10:44:15
7 ALD -- ALD process give you a good -- very good -- 10:44:20
8 excellent conformality. That is true, but I'm not 10:44:26
9 saying that, oh, we don't use it for thick -- for 10:44:29
10 spacer application because it's too slow, because it's 10:44:38
11 not necessary. It's not necessary to have a precise 10:44:43
12 thickness control such as in the application of high-K 10:44:47
13 dielectric application. 10:44:59
14 Do you understand? 10:45:00
15 Q. I do. I understand very well, actually. 10:45:01
16 So why is it -- well, withdraw the question. 10:45:04
17 For those same reasons, you may decide, as 10:45:09
18 an engineer when you're designing a system and you're 10:45:15
19 depositing silicon nitride, that you are not willing 10:45:19
20 to suffer the slower deposition rate of PECVD. And 10:45:22
21 you may value deposition rate more highly and decide 10:45:27
22 that you don't need that level of conformality. 10:45:32
23 Isn't that true, too? 10:45:35
24 A. If you -- by optimizing the process, you are 10:45:37
25 having a trade-off. Some might have higher 10:45:47

1 deposition -- deposition rate and conformality might 10:45:50
2 not be as good, and some have a very good conformality 10:45:55
3 but the deposition rate might be slower. It really 10:45:59
4 depends on -- that's how optimization work. Yeah. 10:46:03
5 So there are trade-offs. And there are 10:46:08
6 specification that you need, what kind of conformality 10:46:12
7 you need. And as long as you meet the conformality 10:46:17
8 specifications, I -- you might be able to adjust the 10:46:21
9 density of the -- and the plasma conditioned so that 10:46:26
10 you have a sufficiently high deposition rate. 10:46:33
11 So these are all well understood by process 10:46:38
12 engineer. It's nothing new. It's not -- it's not so 10:46:42
13 complex, you make it seem like. 10:46:47
14 Q. Okay. And the next trade-off in this 10:46:49
15 article is film quality. And the article states, "An 10:46:55
16 aggressive process designed solely for coverage might 10:47:01
17 produce a film that is too stressed, leading to 10:47:04
18 cracking or delamination later on." 10:47:07
19 Do you agree with that? 10:47:11
20 A. So -- well, the process conditioned that 10:47:12
21 enhanced PECVD step coverage can increase the 10:49:04
22 intrinsic film stress due to densification and ion 10:49:16
23 bombardment effects, and intrinsic stress is a 10:49:23
24 controllable process variable. So a person of 10:49:34
25 ordinary skill in the art, an engineer, would 10:49:37

1 routinely optimize the deposition parameter to achieve 10:49:42
2 acceptable conformality while maintaining the fin 10:49:48
3 stress within a reliable level. 10:49:57
4 So, yeah, it is well known that because 10:50:06
5 of -- to achieve very high conformality, you might 10:50:11
6 need a higher ion bombardment, meaning higher power, 10:50:19
7 it is higher plasma density, higher substrate 10:50:27
8 temperature, and so on and so forth. And that could 10:50:31
9 increase your fin stress, but it's not like someone 10:50:34
10 who just blindly increasing all these variables 10:50:39
11 without worrying about -- that you don't need that 10:50:44
12 certain amount of conformality, you just need a 10:50:50
13 sufficient amount of conformality. 10:50:55
14 So everything is trade-off. And you have 10:50:57
15 all these knobs to play with. One would adjust these 10:51:02
16 knobs to achieve the material, the layer that you 10:51:09
17 deposit to meet all the specification: Conformality, 10:51:14
18 reliability, fin stress, and so on and so forth. 10:51:22
19 Q. Okay. What is the sufficient level of 10:51:27
20 conformality if you were going to use PECVD in the Xu 10:51:32
21 reference? 10:51:39
22 A. Well, first of all, neither Xu or -- I don't 10:51:40
23 think '384 reference define what conformality 10:52:39
24 percentage term. Whether it's 70 percent, 90 percent, 10:52:43
25 or so, there is no qualitative step coverage metrics 10:52:46

1 that's disclosed. And neither is the claim. Claim 8 10:52:51
2 doesn't say what percentage, what conformality number 10:52:55
3 that you need. 10:53:00
4 And so what is sufficient conformality mean 10:53:03
5 in Xu? That the -- it will be -- it is sufficient if 10:53:06
6 the epitaxial -- if the material formed consistently 10:53:15
7 along the exposed gate surface and fin surface, it 10:53:23
8 will result in a channel region with intended strain 10:53:27
9 profile, the gate would wrap around the intended 10:53:34
10 portion of the fin, and there is no void or defects in 10:53:40
11 the films that would compromise electrical 10:53:48
12 performance. So those are the key objective of Xu. 10:53:58
13 And so if you develop a process so that you 10:54:01
14 can satisfy those aspects, then there is -- the 10:54:08
15 conformality is sufficient. 10:54:17
16 Q. All right. 10:54:19
17 A. But that -- how much is it? Well, it 10:54:23
18 depends on what is the particular technology node, how 10:54:29
19 tall is the gate, how tall is the fins, and what is 10:54:32
20 dimensions. There is all kinds of parameters one need 10:54:41
21 to consider. But as long as you were able to achieve 10:54:44
22 the goals that you need, then the conformality is 10:54:47
23 sufficient. 10:54:53
24 Q. Okay. And you didn't discuss any of the 10:54:54
25 trade-offs that we looked at in Exhibit 2004 regarding 10:55:01

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1 conformality versus other considerations that an 10:55:08
2 engineer must consider in your declaration; correct? 10:55:13
3 MR. BRADLEY: Objection. Form. 10:55:20
4 THE WITNESS: My job -- my understanding of 10:55:21
5 my IPR declaration is to prove that Xu disclosures 10:55:26
6 meets the claim limitation of Claim 8. I don't 10:55:36
7 think -- so I think I did that. 10:55:47
8 A person of ordinary skill in the art would 10:55:50
9 understand that all these trade-offs, all these knobs 10:55:52
10 that one needs to turn, is not the object of my IPR 10:56:00
11 declaration. 10:56:07
12 BY MR. DOKHANCHY: 10:56:07
13 Q. I'm not hearing an answer to my question, so 10:56:16
14 I'll ask it again. 10:56:18
15 A. I believe I answered it. I did not need to 10:56:19
16 do that. 10:56:21
17 Q. And you didn't do that; correct? 10:56:22
18 A. I did not need to do that, so, therefore, I 10:56:23
19 don't need to do that. And I didn't do that. I 10:56:27
20 didn't need to discuss all the trade-off, all the ion 10:56:29
21 line-of-sight, all the aggressive process designed. 10:56:34
22 What I do -- what I did is to prove that 10:56:46
23 Xu's disclosure satisfied the claim limitation of 10:56:51
24 Claim 8, and I did that. All the extra stuff that you 10:56:56
25 asked me, I don't think I need to do that, and, 10:57:01

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1 MR. BRADLEY: It's 68 of the PDF. 62 is the 11:31:25
2 number at the bottom. 11:31:31
3 THE WITNESS: Yep. Okay. 11:31:41
4 BY MR. DOKHANCHY: 11:31:42
5 Q. All right. And I don't know if you have the 11:31:43
6 claim up, but why don't I just set some context. 11:31:47
7 Claim 9 says, "The fabrication method 11:31:51
8 according to Claim 1, further comprising: Depositing 11:31:54
9 an interlayer dielectric to surround the gate 11:31:56
10 structure, removing the gate structure to leave a 11:31:59
11 trench, forming a gate dielectric layer to conformally 11:32:02
12 cover a sidewall and bottom of the trench, and forming 11:32:07
13 a conductive layer to fill up the trench." 11:32:10
14 Do you see that as Claim 9? 11:32:13
15 A. Yes. 11:32:15
16 Q. Okay. So I want to go to your analysis on 11:32:16
17 elements as you've labeled them, 9b and 9c. 11:32:24
18 So -- well in 9a, we can see when we're on 11:32:29
19 Page 62, you reference the disclosure in Xu of the 11:32:36
20 gate-last process. Paragraph 121. 11:32:39
21 Do you see that? 11:32:42
22 A. 121. Yes. 11:32:43
23 Q. And in terms of removing the gate structure 11:32:48
24 to leave a trench, if you go -- starting at 11:32:54
25 Paragraph 125, the process that you are saying is 11:32:57

1 disclosed to a POSITA is that the gate-last process -- 11:33:04
2 this is Paragraph 126, "The gate-last process of Xu 11:33:11
3 uses a dummy gate as the initial structure, which is 11:33:15
4 subsequently removed." 11:33:17
5 And then you say at the top of Page 65, "A 11:33:19
6 POSITA would have further understood that removing the 11:33:23
7 gate structure 152 -- annotated in gold below -- of Xu 11:33:26
8 would leave a trench between the spacers 152." 11:33:32
9 Is that right? 11:33:36
10 A. Right. 11:33:37
11 Q. So the trench you're identifying is once 11:33:38
12 you've removed 150 in Figure 2 of Xu, the walls of the 11:33:42
13 spacers on the sides and the substrate on the bottom 11:33:48
14 constitute or define a trench. 11:33:53
15 Is that the right trench? 11:33:55
16 A. You could say that, yes. 11:33:57
17 Q. Okay. And then the next step in 9c is 11:33:59
18 forming a gate dielectric layer to conformally cover a 11:34:04
19 sidewall and the bottom of the trench. 11:34:09
20 And you say in Paragraph 128, "A POSITA 11:34:11
21 would have found -- excuse me -- would have understood 11:34:16
22 and found obvious that the gate dielectric layer is 11:34:20
23 deposited conformally to cover a sidewall and the 11:34:24
24 bottom of the trench in a gate-last process." 11:34:27
25 And so my initial question is, what is the 11:34:34

1 purpose of a gate dielectric in MOSFET, FinFET -- 11:34:40
2 well, I'll just restate the question. 11:34:47
3 What is the purpose of a gate dielectric? 11:34:49
4 A. In MOSFET or FinFET? Or both? 11:34:51
5 Q. Let's say in the device of Xu, what is the 11:35:02
6 purpose of the gate dielectric? 11:35:07
7 A. Well, the primary purpose is to electrically 11:35:09
8 insulate the gate from the channel, and thereby 11:35:20
9 allowing the gate to capacitively couple to the channel. 11:35:25
10 So without it, the gate -- the gate current would flow 11:35:34
11 directly into the channel, and the device will short 11:35:40
12 and lose the field effect control. 11:35:44
13 MOSFET stand for metal-oxide-semiconductor 11:35:50
14 field-effect transistor. So the way it works is 11:36:00
15 simply using the electric field across the gate 11:36:02
16 dielectric to turn on or turn off the channel. So 11:36:07
17 without the gate dielectric, you would not have a 11:36:13
18 transistors such as MOSFET or FinFET. 11:36:19
19 Q. And so that use that you're talking about 11:36:25
20 comes from the gate dielectric being vertically 11:36:29
21 positioned below the gate and above the substrate. 11:36:34
22 Is that right? 11:36:37
23 A. Can you repeat that? Vertically? 11:36:38
24 Q. Yeah. 11:36:44
25 The gate dielectric, to achieve the purpose 11:36:45

1 dielectric layer was nonconformal, meaning it only 11:38:14
2 deposited horizontally and not on the vertical 11:38:21
3 sidewalls of the spacers; right? 11:38:26
4 A. You're talking about depositing onto the 11:38:28
5 trench -- 11:38:32
6 Q. Correct? 11:38:32
7 A. -- after the gate -- sacrificial gate is 11:38:33
8 removed. 11:38:36
9 Yeah, ideally, you don't need the gate 11:38:37
10 dielectric on the sidewall of the spacers. In fact, 11:38:40
11 in some process, you don't have the gate dielectric on 11:38:47
12 the sidewall, but that's a different story. 11:39:00
13 Q. So -- 11:39:04
14 [Simultaneous speaking.] 11:39:04
15 BY MR. DOKHANCHY: 11:39:07
16 Q. What mechanisms or deposition techniques 11:39:07
17 would have been usable to accomplish that sort of 11:39:12
18 deposition, where the gate dielectric is only on the 11:39:17
19 flat, horizontal portion above the substrate and not 11:39:22
20 on the sidewalls? 11:39:31
21 A. It's not the process; it's the process 11:39:32
22 sequence. In some process sequence, you deposit the 11:39:35
23 gate dielectric first, and then put down the dummy 11:39:39
24 gate. So you have the gate dielectric and then the 11:39:48
25 dummy gate and then you form the spacer. And then you 11:39:51

1 remove the dummy gate, so now you already have the 11:39:54
2 gate dielectric on the bottom. Then you put down the 11:39:57
3 real gate. 11:40:00
4 Q. Okay. 11:40:01
5 A. Whereas in some process, you put down the 11:40:02
6 dummy gate, for example, polysilicon gate. And then 11:40:07
7 you build a sidewall and then build a spacer. And 11:40:12
8 then you fabricate or source drain region, which is at 11:40:15
9 high temperature. 11:40:21
10 After you form the source drain region, then 11:40:23
11 you remove the dummy gate. And now you need to put 11:40:25
12 down the high-K dielectric, the gate insulator. And 11:40:29
13 in order to fill the bottom -- in order to have the 11:40:37
14 gate dielectric go into the trench, right, the high 11:40:40
15 aspect ration trench, you need a CVD process or ALD 11:40:48
16 process so that you would have a conformal deposition. 11:40:52
17 In that case, you would have the dielectric on the 11:40:55
18 bottom, as well as the sidewall of the spacers. 11:40:58
19 Q. Would it be possible to deposit in that 11:41:02
20 method and not have a conformal deposition, meaning a 11:41:09
21 process where the gate dielectric is not laid on the 11:41:13
22 sidewalls of the spacers? 11:41:19
23 A. The side -- the gate dielectric has to be -- 11:41:21
24 the gate dielectric is a extremely critical element in 11:41:27
25 the entire process. And -- so you need a very good 11:41:36

1 deposition process. So the best is the ALD, which 11:41:41
2 give you a very precise control of the thickness and 11:41:48
3 precise of the composition. 11:41:51
4 You could use sputtering, which is a 11:41:54
5 directional deposition. Then in that case, you could 11:41:57
6 have a thin layer of gate dielectric at the bottom 11:42:01
7 because it's directional deposition and not at the 11:42:07
8 sidewall. But sputtering is not a high quality -- 11:42:11
9 would not result in a high-quality gate dielectric. 11:42:20
10 And also, not only that is a poor quality, 11:42:24
11 but also very poor control of the thickness. So 11:42:26
12 that's why it's not being used. 11:42:29
13 You should take my class. This is what I 11:42:40
14 teach in my industrial class. 11:42:44
15 Q. It does sound interesting, I'll give you 11:42:45
16 that. 11:42:48
17 A. It sounds -- I sense a little bit of 11:42:50
18 sarcasm. 11:42:54
19 Q. No, not at all. Not at all. I do think 11:42:55
20 it's interesting. 11:42:58
21 A. Okay. 11:42:59
22 Q. Okay. So -- okay. Actually, I think we're 11:43:00
23 fine on that one. 11:43:08
24 Let's go to the Lin reference. 11:43:09
25 Can -- 11:43:14

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1 A. It's uploaded? 11:43:15
2 Q. Yeah, I believe so. It's Exhibit 1005. 11:43:16
3 A. Okay. 11:43:20
4 THE TECHNICIAN: Yeah. 1005 is available. 11:43:23
5 BY MR. DOKHANCHY: 11:43:26
6 Q. Okay. So let's go to your analysis in 11:43:48
7 Ground 2 of the Lin and the Brask reference. 11:43:51
8 Brask is also available, but first let's 11:43:56
9 orient ourselves in your declaration around 11:44:01
10 Paragraph 180, I believe it is. 11:44:06
11 A. Okay. Which is on Page -- 11:44:09
12 Q. It's a little further down, actually. It's 11:44:12
13 187. And that's on PDF 106 or internal Page 100. 11:44:15
14 A. Yep. 11:44:23
15 Q. We may need to bounce around a little bit. 11:44:24
16 Lin uses a gate-first approach. 11:44:44
17 Is that right? And you can look at 11:44:47
18 Paragraph 180, if that's helpful. 11:44:53
19 A. Yes. Lin -- the first sentence, Lin 11:44:55
20 discloses a gate-first fabrication process. 11:45:01
21 Q. And that means that the gate is created and 11:45:04
22 it is not removed, in contrast with the gate-last 11:45:13
23 approach; correct? 11:45:17
24 A. That is -- in a sense, yes, that's correct. 11:45:19
25 Q. There is no sacrificial gate and there is no 11:45:25

1 dummy gate in the Lin reference; correct? 11:45:29

2 A. That's what it means by gate-first, yes. 11:45:32

3 There is not -- it's not a gate-last process, which 11:45:34

4 has a dummy gate or also called a sacrificial gate. 11:45:37

5 Q. The gate-first approach has certain 11:45:44

6 advantages over a gate-last approach. 11:45:51

7 Do you agree? 11:45:54

8 A. Like I said, there is some advantages and 11:45:56

9 disadvantages in every engineering problem. 11:46:02

10 Q. And what are some advantages of a gate-first 11:46:08

11 approach? 11:46:14

12 A. So one of the important things to fabricate, 11:46:14

13 whether it's MOSFET or FinFET, you need -- after you 11:46:29

14 form the gate, you need to source drain to align 11:46:37

15 the -- source drain region to align with the edge of 11:46:42

16 the gate. Okay. 11:46:49

17 And so in a gate-first process, which is a 11:46:54

18 very simple integration, you put down the gate and 11:47:15

19 then you implant the source and strain because by 11:47:22

20 implanting -- implant means that you basically 11:47:30

21 bombarded the entire wafer with, let's say, 11:47:35

22 phosphorus. Okay. And that the -- because the gate 11:47:42

23 act as a shadowing, it blocks the implant, and, 11:47:49

24 therefore, the source drain will only implant at the 11:47:54

25 edge next to the edge of the gate. 11:47:58

1 So right off the bat, you have a perfect 11:48:01
2 cell -- so-called self-align process. Okay. 11:48:07
3 Unfortunately, since 19 -- since 2007 when we have 11:48:14
4 high-K metal gate process, metal gate melt at 11:48:21
5 600 degrees C or so, 600 or 650. For example, 11:48:27
6 aluminum. 11:48:33
7 In that case, after you put that on aluminum 11:48:34
8 and you implant the source and strain -- but in order 11:48:37
9 to activate the source and strain, you need 11:48:42
10 temperature much higher than 650 degrees C. Worse, if 11:48:46
11 you use strained silicon where you want to grow a 11:48:52
12 silicon-germanium source drain, you need even higher 11:48:55
13 temperature. 11:49:00
14 So, therefore, that would result in the 11:49:01
15 gate -- the metal gate basically disintegrate or melt. 11:49:08
16 Okay. So that wouldn't work. So, therefore, we use 11:49:13
17 the gate-last process. We use a dummy gate, which is 11:49:18
18 made of polysilicon. 11:49:22
19 Polysilicon is a polycrystalline silicon 11:49:24
20 which is made of silicon. And silicon doesn't melt 11:49:31
21 until over 1200 degrees C. So, therefore, you took 11:49:35
22 down the dummy gate, and then you do all the process 11:49:39
23 to form a source drain, and there can be high 11:49:41
24 temperature, that's fine. Now what you do is, you 11:49:45
25 need to take out the dummy gate and put down the real 11:49:48

1 gate. 11:49:52

2 The process is a little more complicated 11:49:52

3 because you need to still make sure that the final 11:49:54

4 gate is perfectly aligned with the source drain. So, 11:49:58

5 therefore, you put down a -- deposit a insulator, and 11:50:04

6 planarize it by CMP, chemical mechanical polishing. 11:50:09

7 And then after you planarize it, then you take out the 11:50:15

8 dummy gate and then you put down the real gate. 11:50:22

9 So it would require a number of -- number of 11:50:25

10 extra steps in order to achieve the -- in order to 11:50:30

11 achieve the self-align process. 11:50:36

12 So gate-first is simpler, but it wouldn't 11:50:40

13 stand -- it would not survive -- survive the high 11:50:45

14 temperature of the source drain process. Gate-last is 11:50:53

15 good because it can form a self-align and the gate 11:50:59

16 would still work, would not melt, but the process 11:51:10

17 complexity is much more than the gate-first process. 11:51:13

18 Q. So at some point in the development of 11:51:18

19 semiconductor manufacturing techniques, gate-first was 11:51:28

20 the -- I don't know if you would say the only method 11:51:33

21 or the dominant method. And then at some point, your 11:51:37

22 assertion is that that changed to gate-last. 11:51:42

23 Is that correct? 11:51:45

24 A. Well, if you go back in history, it's -- 11:51:46

25 actually, it was gate-last process first. If you go 11:51:52

1 back in 1970, before you were born, you first form -- 11:51:56
2 use a (indiscernible) to form the gate. And then you 11:52:10
3 develop the source drain, and then you put down 11:52:12
4 aluminum as the gate. But that required aligning of 11:52:16
5 the aluminum gate to the source drain because the 11:52:20
6 alignment might not be perfect, so you have to ensure 11:52:26
7 there are some overlap. 11:52:30
8 So this is not a self-align process. If it 11:52:31
9 is not self-aligned, it create a lot of overlap, which 11:52:36
10 creates so-called parasitic pass events, which means 11:52:39
11 that it is not desirable. 11:52:44
12 So then in 19 -- early 19 -- late 1970s and 11:52:46
13 early 1980s, we start using polysilicon gate as the -- 11:52:52
14 as the gate. Polysilicon gate either dopant with anti 11:52:58
15 dopant or P-type dopant because this polysilicon is -- 11:53:06
16 can withstand high temperature. 11:53:10
17 And at the same time, the advent of ion 11:53:12
18 implantations, in other words, you can basically 11:53:16
19 inject ions vertically, 0-degree, into the substrate. 11:53:20
20 When that was developed, now we can have a 11:53:27
21 self-aligned process, very simple, very easy to 11:53:33
22 achieve. 11:53:36
23 By 2007, at 45-nanometer technology, at that 11:53:38
24 point we say, hey, we cannot use polysilicon gate 11:53:44
25 anymore because of all kinds of disadvantage. We use 11:53:52

1 metal gate. But metal cannot withstand high 11:53:54
2 temperature. So, therefore, we say best use gate-last 11:53:58
3 for a process. 11:54:02
4 So I think in short, that's the progressions 11:54:03
5 over the years. 11:54:07
6 Q. So it was really the desire to move away 11:54:08
7 from polysilicon gates to metal gates that spurred the 11:54:12
8 use of a gate-last process? 11:54:20
9 A. That is correct. Well, not only the 11:54:22
10 polysilicon -- moving away from polysilicon gate. 11:54:27
11 More importantly, it's moving away from SiO₂, the gate 11:54:33
12 dielectric. Because if you can imagine, the gate 11:54:38
13 dielectric is important because the gate is the one 11:54:47
14 that control whether the transistors turn on and off. 11:54:49
15 So in order to have very high efficient 11:54:54
16 transistor, the gate oxide thickness needs to be very 11:54:56
17 thin. Okay. So over the year, we've been scaling 11:55:01
18 down from 1,000 angstroms in 1970s down to 12 11:55:04
19 angstroms in 19 -- in 2000 or so. 2001, 2002. 11:55:09
20 And 10 angstrom is only, like, 5 monolayer 11:55:16
21 of SiO₂. Electron can easily tunnel through the 11:55:20
22 insulator. In other words, it's no longer an 11:55:25
23 insulator, and, therefore, we need to -- we need to 11:55:29
24 replace that with something else. 11:55:33
25 The something else is so-called high-K 11:55:35

1 dielectric. The reason high-K dielectric works better 11:55:39
2 is because it has higher K. K means dielectric 11:55:43
3 constant. Having a high K means I can have a thicker 11:55:50
4 dielectric, thicker insulator, and, still, the gate 11:55:53
5 can couple to the channel very efficiently. 11:55:57
6 So that is the reason why -- but high-K -- 11:55:59
7 high-K dielectric doesn't work well with the 11:56:03
8 polysilicon. It only works well with metal gate. So 11:56:09
9 that's the reason why we use metal gate. Plus other 11:56:14
10 reasons. 11:56:17
11 Q. Okay. Are you familiar with the concept of 11:56:17
12 design rules? Is that a term that has meaning to you 11:56:35
13 in terms of semiconductor device design and the notion 11:56:40
14 that gate-last has more restrictive design rules than 11:56:46
15 gate-first? 11:56:52
16 A. Yeah. Design rule is basically a set of 11:56:53
17 geometrical -- geometric restriction or constraint 11:56:58
18 that a circuit designer must follow so that a chip 11:57:04
19 layout -- so that a chip layout can be reliably 11:57:11
20 manufactured on a specific semiconductor process. 11:57:17
21 In other words, let's say you want to build 11:57:19
22 a chip. And you send it to a foundry. And a foundry 11:57:23
23 would say that, "Look, the metal line cannot be too 11:57:28
24 close to the polysilicon line. The metal to metal 11:57:31
25 cannot be too close." And those are the so-called 11:57:35

1 design rules. 11:57:39

2 So your question is? 11:57:42

3 Q. Do you agree that the gate-last approach has 11:57:54

4 more restrictive design rules, and the gate-first 11:57:58

5 approach results in greater freedom in circuit design? 11:58:03

6 MR. BRADLEY: Objection. Form. 11:58:07

7 THE WITNESS: You can't really compare the 11:58:09

8 two because one is for -- gate-first was used for 11:58:28

9 65-nanometer technology node and early -- and late -- 11:58:44

10 and earlier. And one is used for 45-nanometer 11:58:48

11 technology node and beyond. 11:58:54

12 So, therefore, it's hard to compare because 11:58:59

13 you are talking about different technology node, you 11:59:17

14 know, when you go from 45 -- from 65-nanometer 11:59:21

15 technology node to 45-nanometer technology node. 11:59:25

16 Technology node, obviously, will be more restrictive. 11:59:29

17 So I'm not sure if that question make any 11:59:35

18 sense at all. 11:59:38

19 BY MR. DOKHANCHY: 11:59:38

20 Q. Yeah, I'm not talking across different 11:59:42

21 technology nodes. I'm talking about, let's say -- and 11:59:44

22 you can correct me if this hypothetical doesn't make 11:59:50

23 sense. 11:59:53

24 But let's take a given technology node 11:59:54

25 where, all else equal, if you could use gate-first or 11:59:56

1 gate-last. 12:00:01
2 And -- 12:00:02
3 A. I see. 12:00:03
4 Q. -- my question is, for that technology node, 12:00:04
5 there would be more restrictive design rules in 12:00:07
6 implementing the gate-last process, and greater 12:00:12
7 freedom and fewer design rules when implementing a 12:00:16
8 gate-first process? 12:00:20
9 A. There still is a lot of nuance about that. 12:00:21
10 So, for example, the gate-last process might -- design 12:00:45
11 rule might be more restrictive because you have a 12:00:51
12 narrow -- very narrow gate spacing. And you need to 12:00:59
13 have the metal -- to -- the dummy gate to be removed 12:01:07
14 and then refielded. And then you also have CMP 12:01:12
15 dishing risk. 12:01:17
16 So the foundry, the TSMC, for example, or 12:01:18
17 Samsung, would often impose a stricter minimum gate 12:01:22
18 spacing and density balancing rule. And, therefore, 12:01:27
19 it might have a little more restrictive in terms of 12:01:32
20 layout density, and -- but the gate-first can also be 12:01:36
21 more constrained, interestingly, because the thermal 12:01:44
22 stability would limit the metal stack options. The 12:01:52
23 work function tuning might be -- flexibility might be 12:01:55
24 lower. 12:01:59
25 So in other words, you saying that -- let's 12:02:00

1 say, 45-nanometer technology node, you agree that 12:02:04
2 polysilicon cannot use any -- cannot be used anymore, 12:02:08
3 so both are using, let's say, titanium nitride. But 12:02:12
4 if you use gate-first process, then the -- you 12:02:17
5 would -- the material -- the foundry might limit 12:02:21
6 the -- what kind of work -- what kind of material you 12:02:27
7 can use for the gate and what kind of -- which result 12:02:32
8 in what kind of threshold voltage that are allowed in 12:02:44
9 the process. 12:02:51
10 So design rule is not just for layout, but 12:02:52
11 also talk about a threshold voltage and what kind of 12:02:55
12 resistance that the gate would have and so on and so 12:03:00
13 forth. 12:03:03
14 So once again, it's really -- there is 12:03:04
15 really a lot of trade-off. So it's not -- it's not 12:03:09
16 really fair to say that, well, the gate-last process 12:03:14
17 tends to have more restrictive design rule than 12:03:18
18 gate-first. But, you know, in general, yes, there is, 12:03:21
19 but at the same time, there is not. 12:03:26
20 Q. Okay. I think that makes sense. 12:03:29
21 A. Yeah. 12:03:36
22 Q. So in the time frame of the Lin reference, 12:03:37
23 when it was filed -- which was 2010 also. 12:03:47
24 A. Well, 2010. 12:03:56
25 Q. The possibility of using a gate-last 12:03:58

1 approach would have been known. 12:04:03
2 That's what you say; right? 12:04:04
3 A. Oh, yeah. 2000 -- 2007, a 45-nanometer 12:04:06
4 technology node entail -- was -- at that time, was one 12:04:16
5 of the first one that developed gate-last process. 12:04:19
6 High-K metal gate. And, therefore, by 2010, many 12:04:23
7 companies already been using gate-last process. 12:04:31
8 Q. Can you think of a reason that the inventors 12:04:34
9 who worked at TSMC would not have known about the 12:04:42
10 ability to use a gate-last process? 12:04:47
11 A. Like I said, there is a lot of trade-off. 12:04:49
12 Perhaps the better question would be, can 12:05:16
13 you think of a reason why the lawyer who drafted this 12:05:30
14 patent didn't know anything about gate-first -- 12:05:34
15 gate-last process. Maybe -- it's drafted by a lawyer, 12:05:38
16 so perhaps they didn't know about it. I don't know. 12:05:45
17 I mean, to -- technically -- technically, 12:05:47
18 that -- the focus is really on -- emphasizing in 12:06:01
19 strain engineering and strain template formation. So 12:06:09
20 that's why they have the rounded insulating layer. So 12:06:16
21 that's the emphasis. 12:06:20
22 And by using a gate-first process, you 12:06:21
23 eliminate the complexity of dummy gate process steps. 12:06:27
24 And -- using the CMP as well as the complexity of 12:06:31
25 filling the trench. And since the focus is on the 12:06:42

1 channel material, epitaxial source drain region, and 12:06:44
2 stress engineering, that it will be much simpler to 12:06:50
3 use a gate-first process and avoid the introduction of 12:06:55
4 replacement gate process that is not really related to 12:07:04
5 the claim invention. 12:07:08
6 So -- but by that time, an engineer would 12:07:12
7 have known that a gate-last process is what was 12:07:17
8 widespread, but, you know, I don't know -- I can't 12:07:25
9 read their mind, why they choose to use the gate-first 12:07:33
10 process. But perhaps it's simpler, more sufficient 12:07:42
11 for the disclosed structure, and thereby avoiding the 12:07:49
12 complexity of the replacement gate process. That's -- 12:07:54
13 like I said, I can't read the inventor's mind or the 12:07:59
14 attorney who drafted the patent. 12:08:07
15 Q. Okay. That's actually all I have, pending 12:08:10
16 any cross -- well, redirect; in which case, I may have 12:08:18
17 some recross. 12:08:24
18 That is all my questions for you, Dr. Lee. 12:08:25
19 MR. BRADLEY: Okay. Why don't we take a 12:08:28
20 break, and then -- ten minutes. And then we can go 12:08:30
21 back on the record to see if we have any. 12:08:33
22 MR. DOKHANCHY: That's fine. So it's 12:08 12:08:36
23 my time. 12:18, which I guess is 2:18 your time, 12:08:39
24 Dr. Lee? 12:08:44
25 THE WITNESS: That's right, yeah. 12:08:46

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1 THE VIDEOGRAPHER: We're going off the 12:08:47
2 record at 12:08 p.m. 12:08:48
3 (OFF THE RECORD AT 12:08 p.m. PT.) 12:08:48
4 (ON THE RECORD AT 12:17 p.m. PT.) 12:17:35
5 THE VIDEOGRAPHER: We're back on record at 12:17:24
6 12:17 p.m. 12:17:35
7 MR. BRADLEY: We have no further questions. 12:17:36
8 We reserve the right to read and sign. 12:17:41
9 MR. DOKHANCHY: Okay. We can wrap it up, 12:17:44
10 then. Thank you, Dr. Lee. 12:17:45
11 THE WITNESS: Thank you, Reza. 12:17:47
12 Thank you, Steve. 12:17:49
13 THE VIDEOGRAPHER: This marks the end of the 12:17:51
14 deposition of Dr. Jack Lee. We're going off the 12:17:53
15 record at 12:17 p.m. 12:17:56
16 THE VIDEOGRAPHER: Mr. Bradley, do you need
17 the video?
18 MR. BRADLEY: Just the transcript is fine.
19 (Whereupon, the deposition concluded at 12:17 p.m.
20 PT.)
21
22
23
24
25

1 DECLARATION

2

3 I hereby declare I am the deponent in the within
4 matter; that I have read the foregoing deposition and
5 know the contents thereof; and I declare that the same
6 is true of my knowledge except as to the matters which
7 are therein stated upon my information or belief, and
8 as to those matters, I believe them to be true.

9 I declare under the penalties of perjury that the
10 foregoing is true and correct.

11 Executed this _____ day of _____,
12 20____, _____.

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1 C E R T I F I C A T E

2 I, Jillian Doctor, the undersigned Certified
3 Shorthand Reporter, holding a valid and current
4 license issued by the State of California, do hereby
5 certify:

6 I do hereby certify that JACK LEE, PH.D., the
7 witness whose deposition is hereinbefore set forth,
8 was duly sworn by me before the commencement of such
9 deposition and that such deposition was taken before
10 me and is a true record of the testimony given by such
11 witness.

12 I further certify that the adverse party,
13 PETITIONER, was represented by counsel at the
14 deposition.

15 I further certify that the deposition of
16 JACK LEE, PH.D., occurred via Zoom on 26, February,
17 2026 commencing at 8:01 a.m. PT to 12:17 p.m. PT.

18 I further certify that I am not related to
19 any of the parties to this action by blood or
20 marriage, I am not employed by or an attorney to any
21 of the parties to this action, and that I am in no way
22 interested, financially or otherwise, in the outcome
23 Of this matter.

24

25

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1 I am neither of counsel nor of kin to the parties
2 to the action, nor am I in anywise interested in the
3 result of said cause.

4

5 IN WITNESS WHEREOF, I have hereunto set my
6 Hand this 26 day of February, 2026.

7

8

9

Jillian Doctor

10

11 JILLIAN DOCTOR, RPR,
CERTIFIED REALTIME REPORTER

12

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