

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-01265
U.S. Patent No. 8,993,384 B2

**SECOND DECLARATION OF JOSEPH C. MCALEXANDER III
REGARDING PATENT OWNER'S RESPONSE FOR *INTER PARTES*
REVIEW OF U.S. PATENT NO. 8,993,384**

TABLE OF CONTENTS

	<u>Page</u>
I. Qualifications	1
II. Overview	2
III. Materials Considered.....	15
IV. Understanding Of The Law.....	15
A. Claim Construction.....	15
B. Invalidity	16
V. Semiconductor Transistor Technology Primer	18
VI. The Challenged '384 Patent	26
VII. Analysis Of The Grounds.....	36
A. Grounds 1A And 1B Fail To Disclose Or Render Obvious The Challenged Claims	36
1. Xu Fails To Disclose Or Render Obvious “Forming An Isolation Structure To Surround The Fin Structure” (Element 1[b]).....	36
a. Xu’s Alleged Isolation Structure Does Not Surround A Fin	36
2. Xu Fails To Disclose Or Render Obvious “Forming A Recess In The Fin Structure At A Side Of The Gate Structure” (Element 1[e]).....	42
3. Xu Fails To Disclose Or Render Obvious “Etching The Isolation Structure” And “Forming A Recess In The Fin Structure”	44
4. Even If Ground 1 Establishes Both “Etching The Isolation Structure” And “Forming A Recess In The Fin	

Structure,” It Fails To Disclose “The Second Depth Is Deeper Than The First Depth”	50
5. Xu Fails To Disclose Or Render Obvious “Forming An Epitaxial Layer To Fill Up The Recess” (Element 1[f]).....	51
6. Xu Fails To Disclose Or Render Obvious Claim 8	54
7. Xu Fails To Disclose Or Render Obvious Claims 4 And 9.....	60
8. Ground 1B Fails To Render Obvious Claims 4 And 9.....	63
B. Grounds 2A And 2B Fail To Disclose Or Render Obvious The Challenged Claims	65
1. Lin Fails To Disclose Or Render Obvious “Forming An Isolation Structure To Surround The Fin Structure” (Element 1[b]).....	65
2. Lin Fails To Disclose Or Render Obvious “Forming A Recess In The Fin Structure At A Side Of The Gate Structure” (Element 1[e]).....	66
3. Ground 2B Fails To Render Obvious Claims 4 And 9.....	68

I. Qualifications

1. I am a Registered Professional Engineer (#79454) and the President of McAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 53 years and am a named inventor on 31 U.S. patents and a number of foreign patents, many of which are directly related to the design and operation of transistors and circuits incorporating transistors, including control, addressing, comparing and sensing, and fabrication.

2. My skills and experience are in areas of circuit design and analysis, device and board fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing,

analysis, and control involved use of mechanical calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and
- designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

3. Because of my background, training, and experience, I am qualified as an expert to opine on the challenged patent. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, which is submitted as Exhibit 2003.

II. Overview

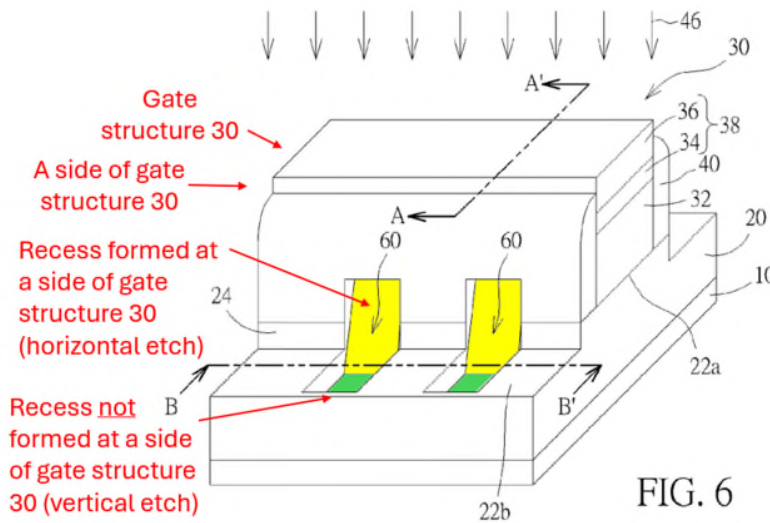
4. None of Petitioner's presented grounds anticipates or renders obvious claims 1-9 of U.S. Patent No. 8,993,384 ("the '384 Patent"). Petitioner's presented grounds fail for multiple reasons.

Before recess is created in the fin:



3

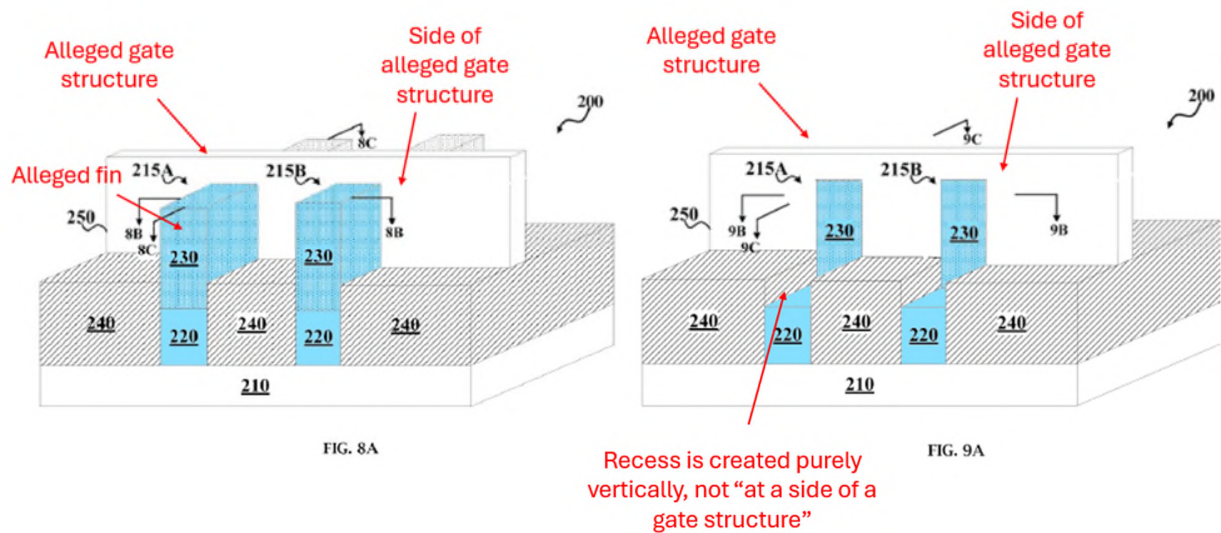
After recess is created in the fin:



Ex. 1001, Fig. 6 (annotated).

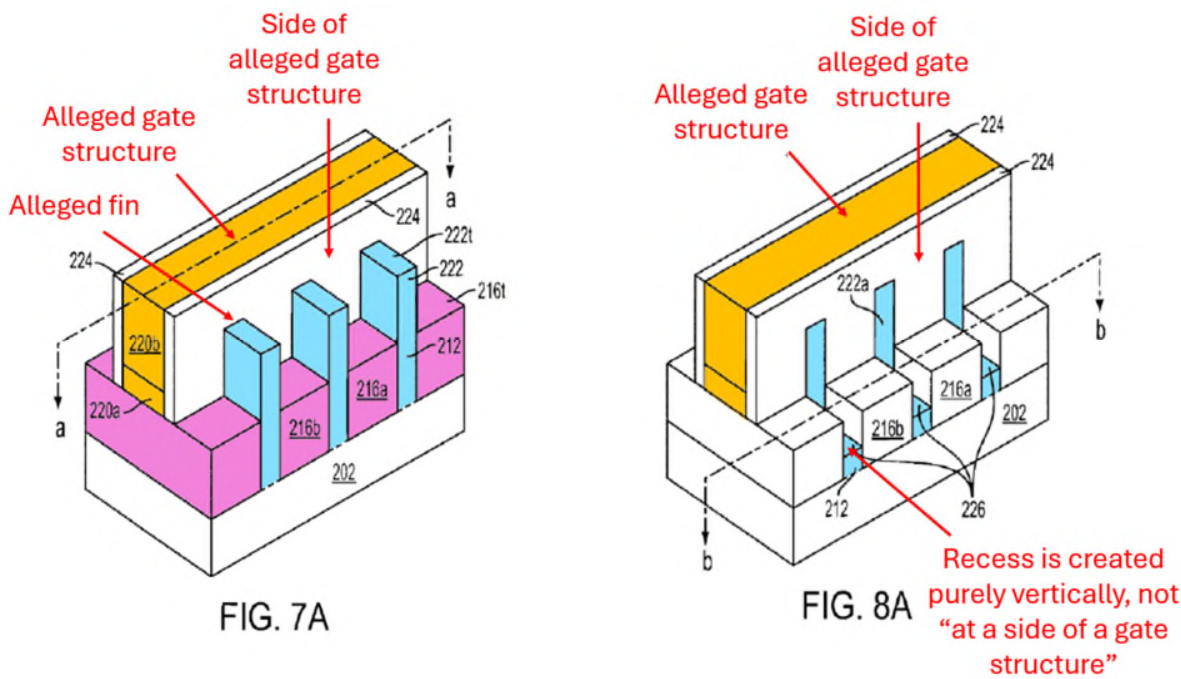
6. But none of the asserted prior art operates that way. The prior art forms exclusively a vertical recess, without the required horizontal component being created:

Xu (Ground 1):



EX1004-Xu, Figs. 8A and 9A (annotated).

Lin (Ground 2):



EX1005-Lin, Figs. 8A and 9A (annotated).

7. Further, Xu (Ground 1) fails to describe etching both the isolation structure (item 20 in the '384 patent figures above) and forming a recess in the fins. Instead, it describes two embodiments, each of which does one of the two, for the same purposes as one another, being redundant to each other. As explained below, the two methods are incompatible with one another in Xu, and a POSITA would not perform both steps, as required by the claims. And in any event, even if one were to perform both steps, in the hypothetical created by Petitioner, there is no reason that one etch would be lower than the other, as required by the claims, which require that the recess in the fins be formed to a lower depth than that to which the isolation structure was etched. The Petition relies on two separate embodiments, with no relationship to one another, and no reason why one etch would be lower than the other.

8. All grounds also fail to disclose or render obvious an isolation structure surrounding a fin structure. Neither of the Petition's primary references (Xu for Grounds 1A and 1B, Lin for Grounds 2A and 2B) describes such an isolation structure. An important feature of the '384 patent's claimed semiconductor device is that the isolation structure surrounds the fin structure on all four sides, thereby completely isolating the fin structure. That the isolation structure surrounds the fin structures is confirmed by the '384 patent's specification, which explains that "a

lower portion of each fin structure is **embedded** in the isolation structure 20,” indicating that the isolation structure covers all four sides of each fin structure. EX1001 at 3:61-62 (emphasis added). This is further confirmed by the ’384 patent’s figures, which consistently illustrate the isolation structure 20 covering all four sides of the fin structures 12:

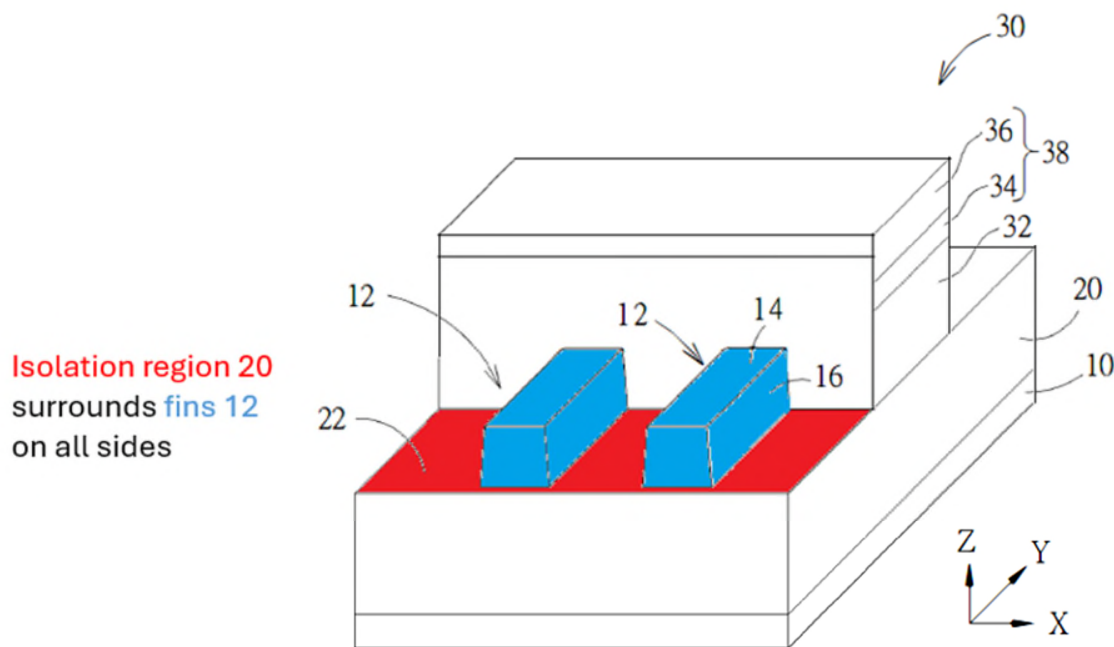


FIG. 2

EX1001 at Fig. 2 (annotated); *see also id.* at Figs. 3, 5.

9. In contrast, in Xu, “isolation features 130” do not surround the fin structures on all four sides of the fins 120, and thus do not “surround” the fins as claimed, but rather only cover two sides of the fins 120:

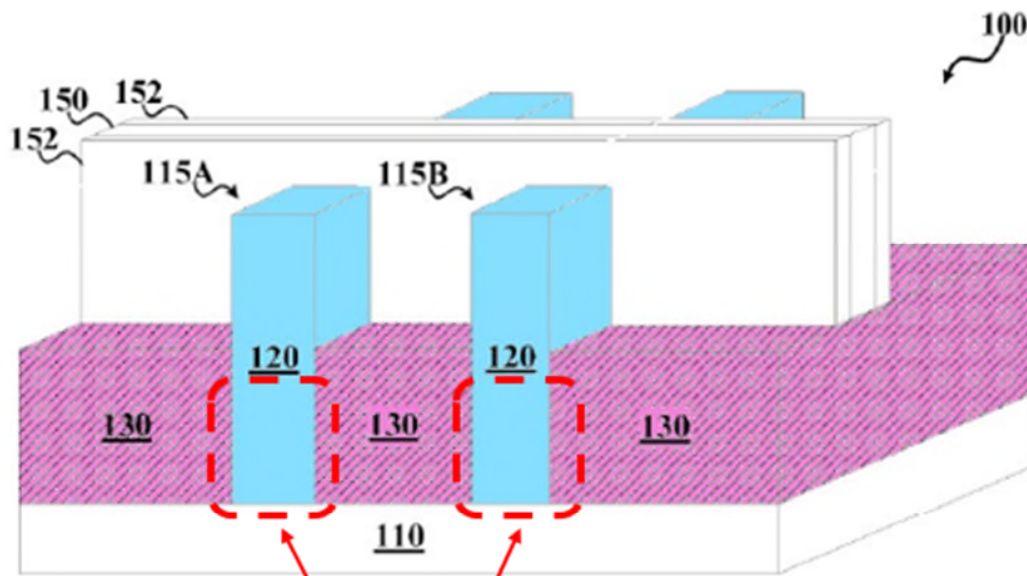


FIG. 2

Alleged isolation
structure 130
(magenta) does not
“surround” fins 120
(blue)

Pet., 18 (showing annotated EX1004-Xu, Fig. 3, further annotated here).

10. Although Xu states that “[i]solation features 130 . . . surround the fin structures 115A and 115B” (EX1004-Xu at 3:54-56), a POSITA would have understood that Xu’s usage of the term “surround” is inconsistent with that term as required by the claimed semiconductor device. Moreover, even if Xu’s isolation features 30 are interpreted as “surrounding” fins 120, Xu’s isolation features

nevertheless do not surround Xu's "fin structure" because, unlike the '609 patent's claimed semiconductor device, Xu's device merges its fins together into a single, merged "fin structure." Xu explains that a "fin template 135 is formed by merging together the fins 120 of the FinFET device 100." EX1004-Xu at 5:2-4. A "semiconductor material is epitaxially grown by an epi process until the fins 120 of the fin structures 115A and 115B are merged together to form the fin template 135." *Id.* at 5:8-10.

11. Xu's Figure 4 illustrates the merging together of fins 120 to form fin template 135:

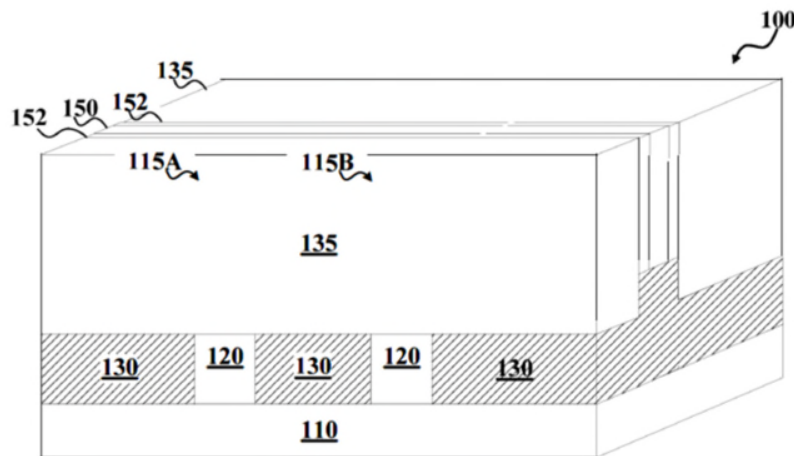


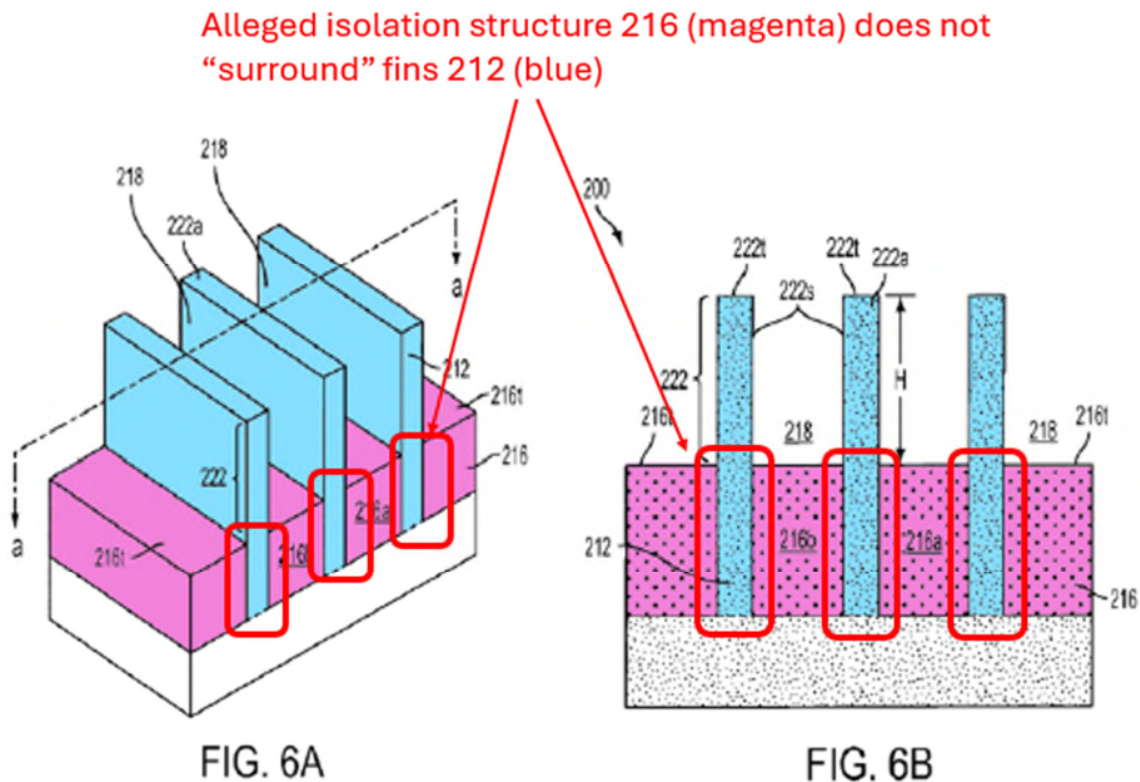
FIG. 4

Id. at Fig. 4. 58.

12. As shown in Figure 4 above, Xu's fin template 135 is disposed on top of isolation features 130. As such, Xu's "isolation features 130" do not surround its

fin structure because it does not enclose any side of the merged fin structure, e.g., the part made up of fin template 135.

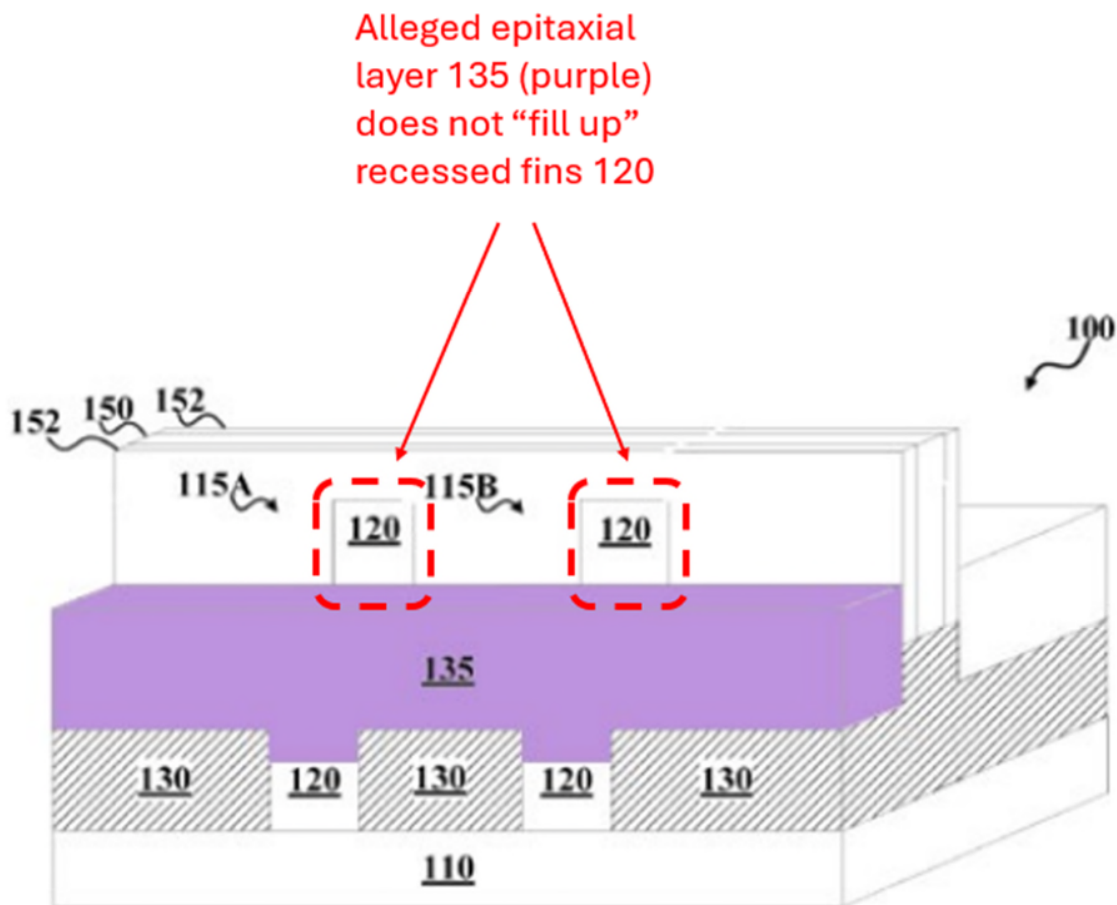
13. Similarly, in Lin, the alleged isolation structure (insulation regions 216) does not surround the fins 212 on all four sides, and thus do not “surround” the fins as claimed, but rather are separate and distinct structures that each cover only one side of each fin:



Pet., 64-65 (showing annotated EX1005-Lin, Figs. 6A and 6B, further annotated here).

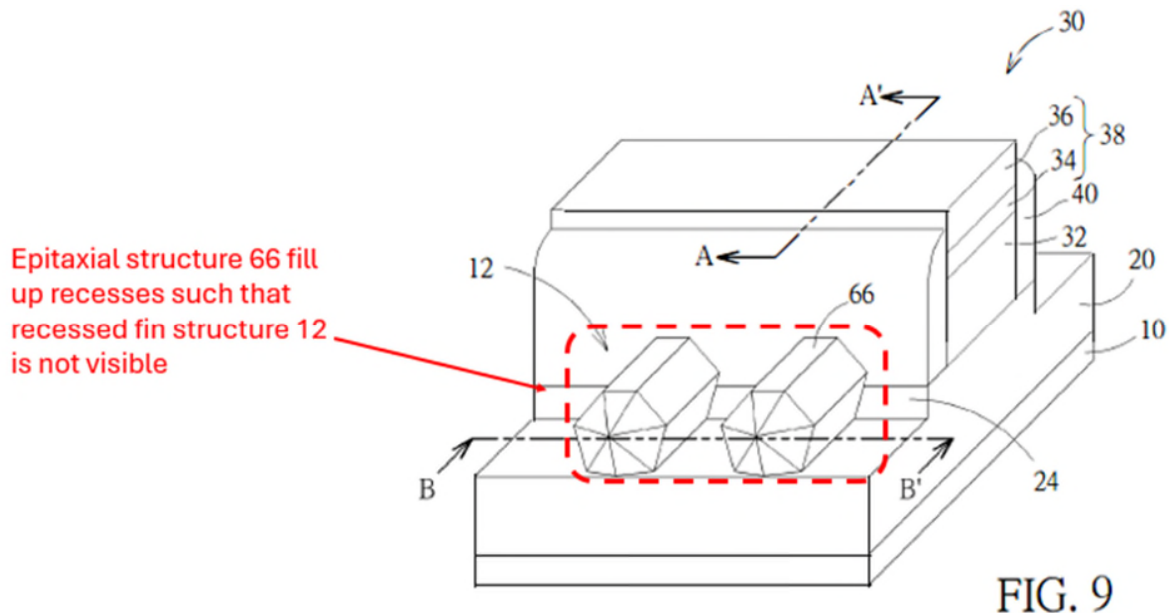
14. Even if the separate insulation regions could be considered a single “isolation structure,” they clearly do not surround the fins.

15. Further, Xu (Ground 1) fails to disclose or render obvious “forming an epitaxial layer to fill up the recess.” As shown in the figure below (annotated and modified in the Petition), Xu’s “fin template 135” does not fill up the recesses, as the fin template does not extend to the top of the alleged recessed fin 120:



Pet., 18 (showing annotated and modified figure, further annotated here).

16. As shown, the alleged epitaxial layer does not extend vertically to the top of the recess, as evidenced by the fact that the tops of the fins 120 are visible over the top of the fin template 135. This is in contrast with the '384 patent, in which the epitaxial structures 66 completely fill up the recessed fin structure 12, as evidenced by the epitaxial structures completely covering the exposed portions of the fin structure such that the fin structure is not visible:



EX1001, Fig. 9 (annotated).

17. Further, Xu (Ground 1) fails to disclose or render obvious that “a step for forming the spacer comprises [] depositing a material layer to conformally cover the gate structure and the fin structure,” as required by claim 8. Xu’s entire disclosure regarding forming a spacer is that “spacers 152 may be formed by

depositing a silicon nitride layer,” without elaborating further. EX1004-Xu, 4:46-49. The Petition alleges that a “POSITA would have understood and found obvious that the deposited silicon nitride layer would conformally cover the gate structure and the fin structure as recited in claim 8.” Pet., 36. This argument requires several leaps of logic, none of which are supported by Xu or any other evidence. The Petition argues one method, plasma-enhanced chemical vapor deposition (PECVD), would be chosen by a POSITA to deposit silicon nitride in Xu, but it fails to sufficiently support why. Pet., 36-37. The Petition argues that it was desirable to use PECVD because it is conformal, which is circular and based on hindsight based on the claim language. Moreover, as Petitioner’s expert admitted, there were non-conformal methods of depositing silicon nitride at the time, which resulted in certain benefits, such as a faster deposition rate and avoidance of strain on the material layer that could destroy the layer. EX2005-Lee-Dep at 28:5-32:7. And the Petition fails to justify why a POSITA would value whatever level of conformality PECVD could provide, at the cost of reduced speed and increased strain. Neither the Petition nor Petitioner’s expert analyzed any of these trade-offs, nor any reason why any arbitrary level of conformality would be needed or beneficial in Xu, or even what that level would be. Moreover, as Petitioner’s expert admitted, there are certain factors that make PECVD conformal, and certain factors that make PECVD non-conformal, and

the Petition and expert declaration are completely silent on those considerations and how they would affect what the appropriate method was for Xu. EX2005-Lee-Dep at 54:10-55:4, 57:15-58:23. Thus, there is no reason or motivation to modify or combine Xu with any particular deposition technique (much less a conformal deposition technique), which the Petition's argument entirely hinges on.

18. Finally, all grounds fail to disclose or render obvious claims 4 and 9. These claims recite a specific "replacement metal gate (RMG)" process for replacing a dummy gate structure with a replacement metal gate. Xu's entire disclosure regarding such a replacement process is that the gate structure may be formed "in a gate first or gate last process." EX1004-Xu, 4:13-14. Even if the Petition is correct that a gate last process is an RMG process, it still does not explain why a POSITA would have been motivated to implement the specific RMG process recited in claims 4 and 9. For example, a POSITA would have known that not every gate-last process includes replacing a gate dielectric layer, as required by claim 9. Thus, Xu's mere disclosure of a "gate last process" does not render obvious the specific steps of the claimed RMG process. For Grounds 1B and 2B, the Petition relies on combinations including the Brask reference but fails to provide a motivation to combine Brask with either Xu or Lin. The mere fact that Xu discloses a "gate last process" is insufficient to motivate implementing the specific gate last process disclosed in

Brask. The Petition's stated rationales would apply to any gate last process, rather than the specific gate last process disclosed in Brask. Moreover, Lin specifically calls for a gate first process, as admitted by the Petition. The Petition fails to provide a sufficient rationale that a POSITA would have been motivated to contradict Lin's express disclosure of a gate first process to instead implement a gate last process.

III. Materials Considered

19. In preparing this declaration, I have reviewed the Petition and the declaration of Petitioner's expert, as well as the materials that they cite, including the asserted prior art. I have also reviewed the documents cited herein, including the transcript of the February 26, 2026, deposition of Petitioner's expert, Dr. Jack Lee.

IV. Understanding Of The Law

20. In preparing and expressing my opinions and considering the subject matter of the challenged patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

A. Claim Construction

21. I understand that the scope of a patent is defined by its claims. I understand that a claim can be:

- a. a method claim, which covers a process/activity, or
- b. an apparatus claim, which covers a physical machine, etc.

22. I understand that the first step in determining the validity of a claim is for the claim to be properly construed. I have been further advised that, in an inter partes review proceeding, the claims of a patent are typically given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the claims and the patent disclosure (specification).

23. I further understand that an inventor can provide special definitions for specific claim term(s) within the patent. However, any special definition for a claim term must be set forth in the specification with reasonable clarity and precision.

B. Invalidity

24. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim, as a whole, would have been obvious to a POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an inter partes review proceeding is by a preponderance of the evidence.

25. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in the art. I have been informed and understand that a prior art reference should be viewed as a whole.

26. I have been informed that in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are

apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious.

27. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one is to consider certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that for such objective evidence to be relevant to the non-obviousness of claim, however, there must be a causal relationship (called a “nexus”) between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

28. I have also been informed and understand that, when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that

the prior art must create a reasonable expectation of success in producing the claimed subject matter.

V. Semiconductor Transistor Technology Primer

29. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (*e.g.*, fin) transistors; and (3) common process steps for creating transistors.

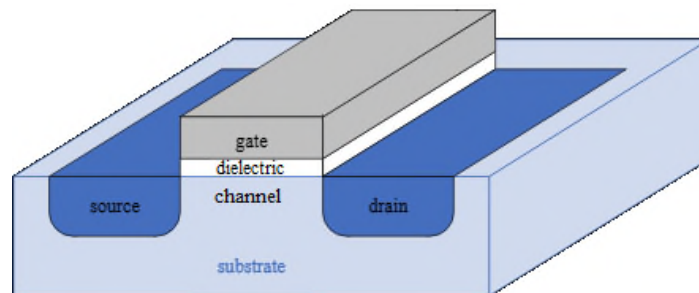
A. Basic Transistor Components

30. Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). EX2002 at 1-2. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. EX2002 at 3.

31. One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. EX2002 at 29-34. In a conductor (*e.g.*,

a metal), electric current can flow freely. EX2002 at 29. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. EX2002 at 30. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. EX2002 at 31-34.

32. The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See, e.g.*, EX2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



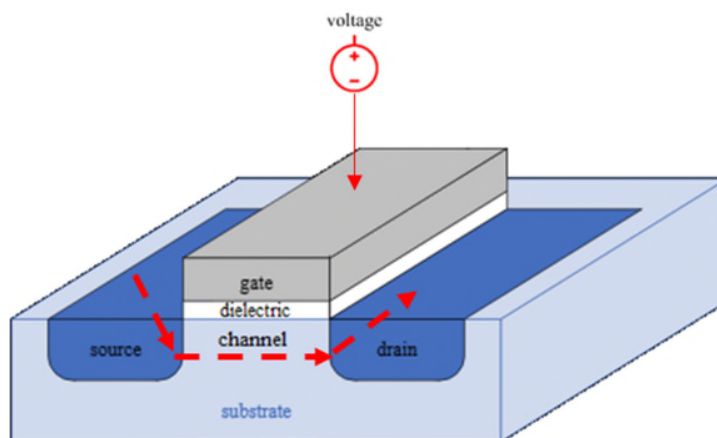
See, e.g., EX2002 at 510-511.

33. The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). EX2002 at 26-28, 427-28. The channel is a region under the gate

and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). EX2002 at 510-511.

34. The gate is a conductor (or semiconductor) located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. EX2002 at 510-511. When a voltage is applied to the gate, the dielectric prevents the “flow of charge” (current) between the gate and the channel, but the applied voltage results in the creation of a “field effect” in the channel. EX2002 at 510-511. This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). EX2002 at 510-511.

As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current.



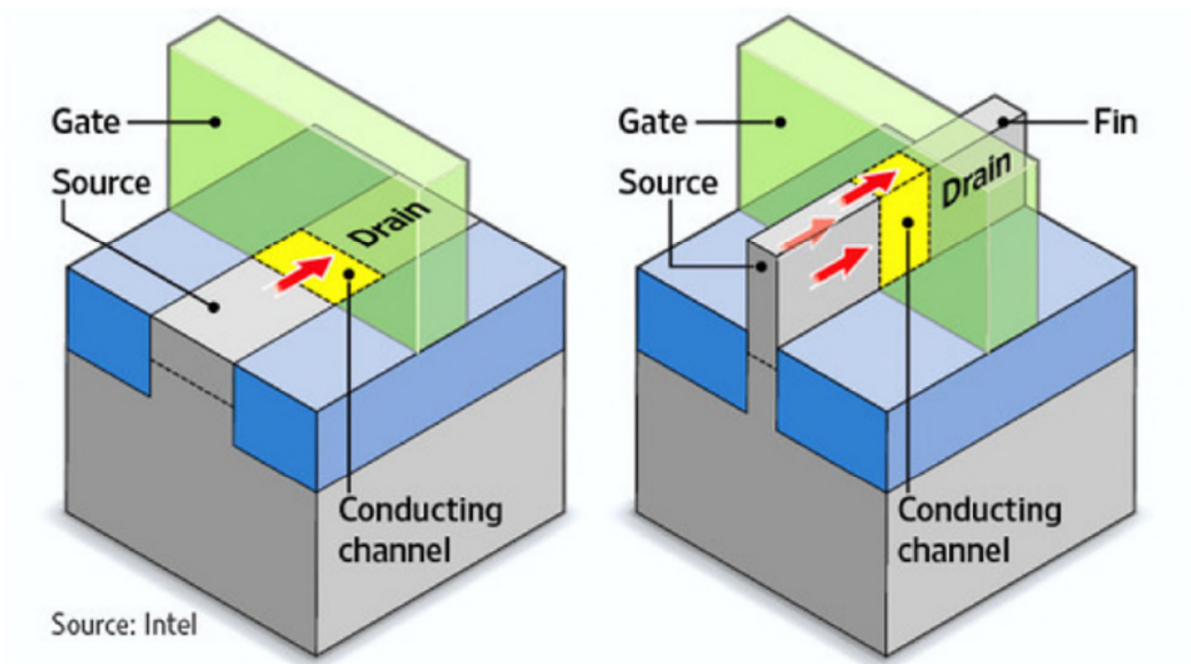
See, e.g., EX2002 at 510-511 (annotated).

B. Planar vs. Three-Dimensional Transistors

35. Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more transistors on a chip has been consistent and widespread in industry. This desire led to the development of a new type of transistor, a “FinFET.”

36. The simplified illustrative FET transistors illustrated in the previous section all feature a gate structure built on a flat semiconductor substrate; in other words, a “planar” FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors.

37. In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



38. In contrast, as illustrated above in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. In the resulting fin field effect transistor (“FinFET”), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.

39. Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip compared to that of the planar transistor. In addition, because FinFETs typically leak less current than

planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip.

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

40. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging.

41. In the first stage, the semiconductor material itself is created. EX2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. EX2002 at 13.

42. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” EX2002 at 13-14. A wafer acts as a semiconductor substrate on and in which transistors may be formed.

43. The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. EX2002 at 14. Thousands of integrated circuits can be formed on the substrate of a single wafer. EX2002 at 14.

44. In the packaging stage, the wafer is separated into individual chips. EX2002 at 14-15.

2. The Wafer Fabrication Stage

45. The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer's substrate. EX2002 at 14. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). See EX2002 at 29-31, 71. For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning.

46. **Layering** is the operation used to add thin layers to the semiconductor substrate. EX2002 at 72. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. EX2002 at 72.

47. For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor

structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. EX2002 at 72.

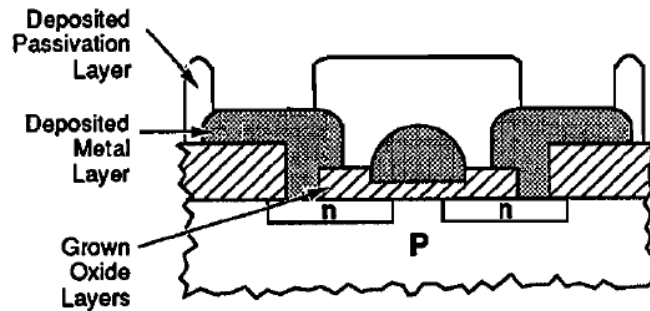


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

48. **Patterning** is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. EX2002 at 72-73. This creates a pattern on the wafer surface. EX2002 at 72-73.

49. The patterning may result in one or more holes in the layered material or one or more remaining islands of material. EX2002 at 72-73. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

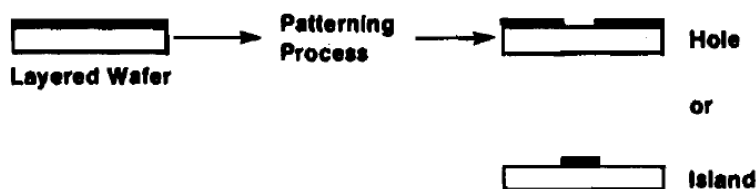


Figure 4.7 Patterning.

50. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

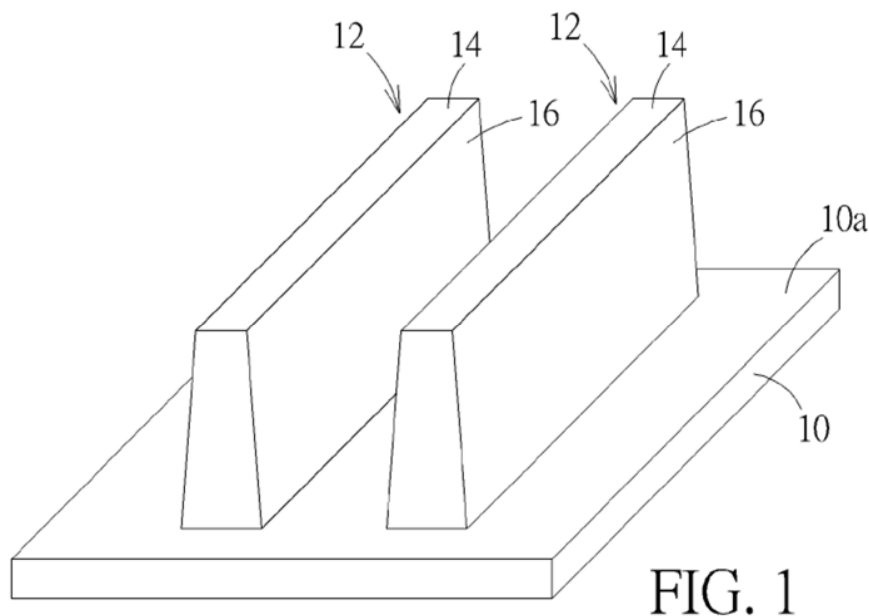
EX2002 at 73.

VI. The Challenged '384 Patent

51. The '384 patent “generally relates to the field of semiconductor devices, and more particularly to a semiconductor device with an epitaxial structure and a fabrication method thereof.” EX1001, 1:6-10. Specifically, the patent states that “[c]rystal strain technology is becoming more and more attractive as a means for getting better performances in the field of MOS transistor fabrication. Putting a strain on a semiconductor crystal alters the speed at which charges move through that crystal.” *Id.* 1:20-25. The patent identifies weaknesses in the prior art in that “how to prevent the formation of the defects inside the epitaxial layer is an important issue” because “defects inside the epitaxial layer reduce the stress required to be

imposed onto the corresponding channel region.” *Id.*, 1:36-42. The described invention is designed to solve those issues. *Id.*, 1:45-2:31.

52. The patent describes “forming a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces,” for example in Figure 1, depicting substrate 10 and fins 12:



EX1001, claim 1, Fig. 1.

53. The patent further describes “forming an isolation structure to surround the fin structure” and “forming a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure, and covering a portion of the isolation structure,” shown for example in Figure 2, depicting isolation structure 20 and gate structure 30:

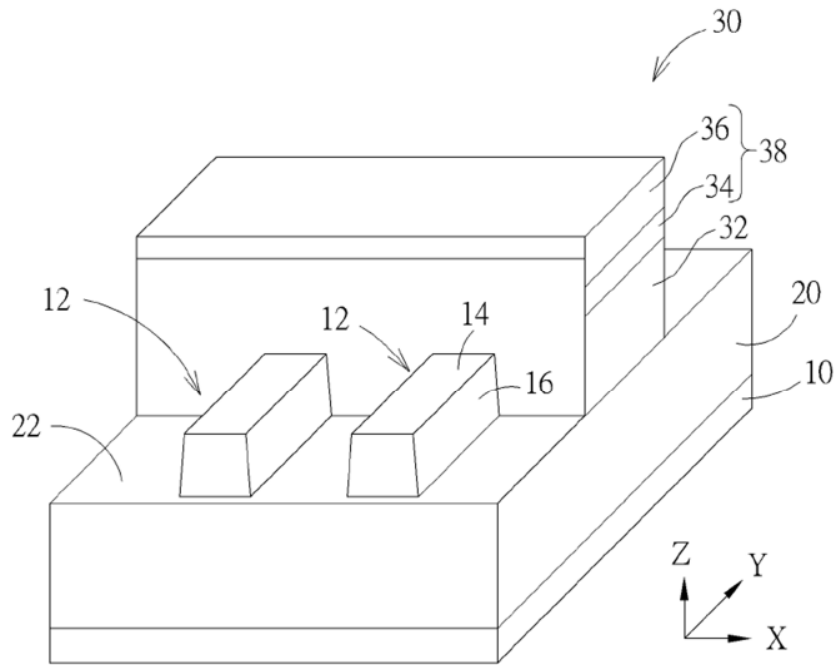


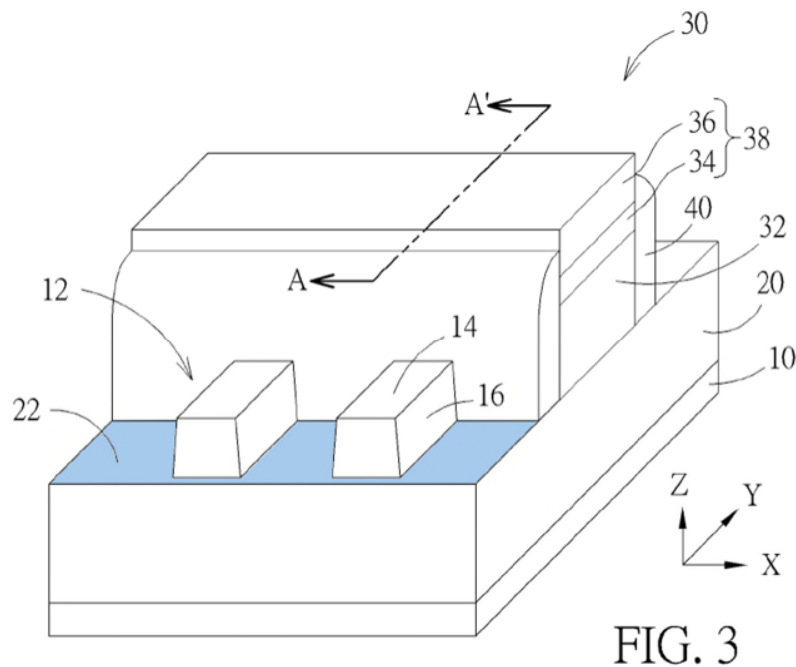
FIG. 2

EX1001, claim 1, Fig. 2.

54. As shown, “[a]t this stage, a lower portion of each fin structure 12 is **embedded** in the isolation structure 20.” *Id.* at 3:61-62 (emphasis added). That is, as clearly shown in Fig. 2, the isolation structure fully surrounds each side of the lower portion of each fin structure. Forming the isolation structure to fully surround the fin structures in this manner is important in order to fully isolate each fin structure, preventing unwanted contact and electrical interaction and thereby ensuring that each fin structure operates independently without interference.

55. After forming the gate structure, the inventors form a spacer on the sidewall of the gate structure: “[a]fter the formation of the gate structure, a spacer 40 is formed on the sidewalls of the gate structure 30.” EX1001, 5:6-8.

56. The patent also describes “after the step of forming the gate structure, etching the isolation structure exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth,” for example as shown in the transition from Figure 3 to Figure 5.



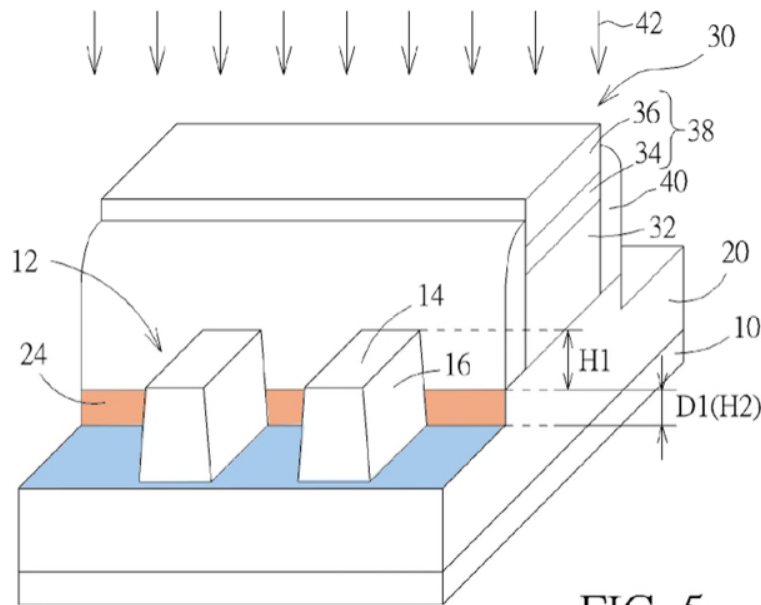


FIG. 5

EX1001, claim 1, Figs. 3 and 5 (annotated).

57. The patent then describes the next step, forming a recess in fins 12, which is claimed as “forming a recess in the fin structure at a side of the gate structure.” EX1001, claim 1. The claims thus establish two key things about the recess: (1) in what and (2) where the recess is created. The claims specify that the recess is created (1) in the fin structure, “a recess in the fin structure,” and (2) “at a side of the gate structure.” EX1001, claim 1. This is further shown in Figures 5 (before etching to create the recess) and 6 (after etching to create the recess). *Id.*, Figs. 5 and 6. On the left below, Figure 5 shows the gate structure, the claimed side of the gate structure (a vertical wall), and the fin, before recess creation. On the right below, Figure 6 shows the gate and side of gate structure, and the recess in the fin

and, and in particular, as annotated in yellow, the recess being “at a side of the gate structure,” which is the vertical wall of the gate. In particular, as annotated in yellow, the recess has a horizontal component that causes it to be “at a side of the gate structure.”

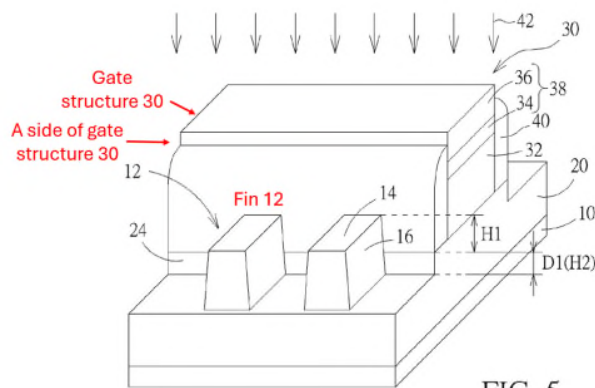


FIG. 5

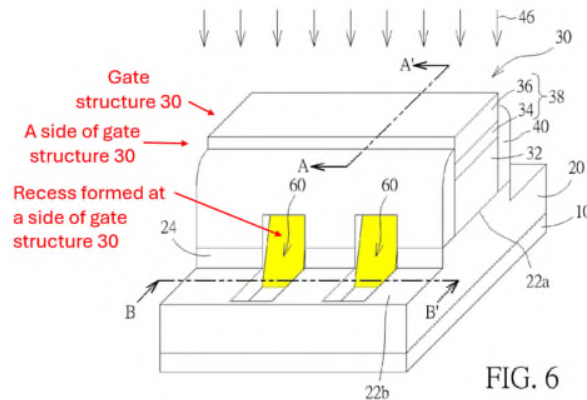
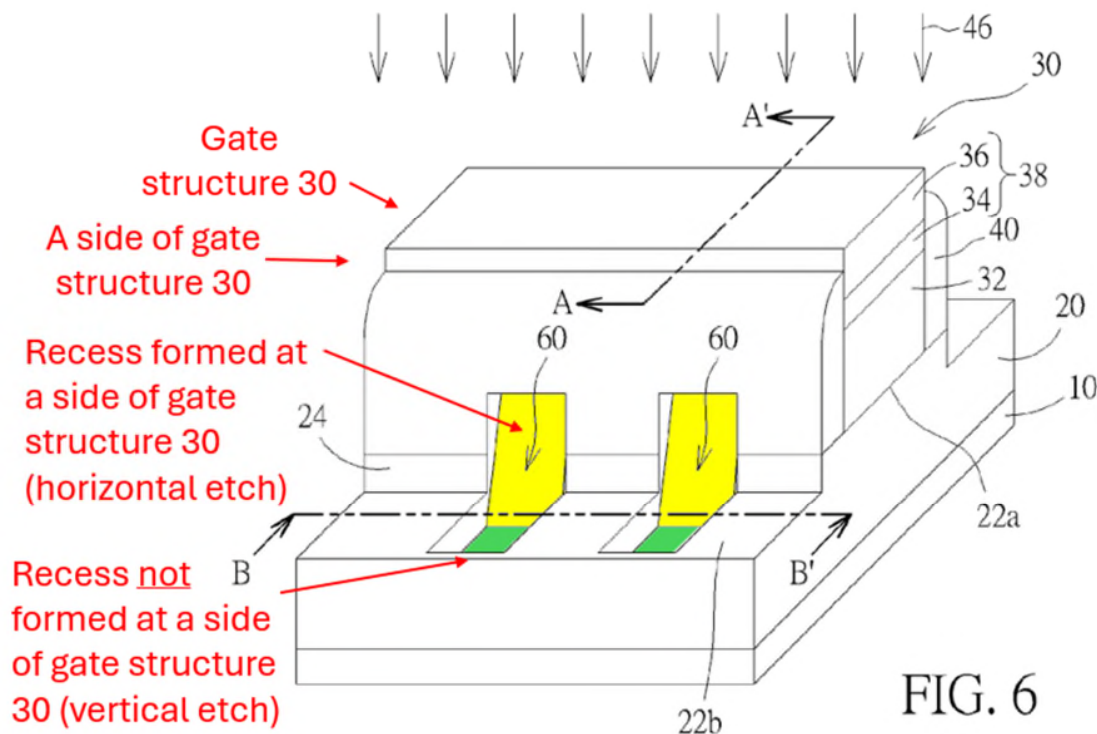


FIG. 6

EX1001, Figs. 5-6 (annotated).

58. To further clarify, in the annotations below, the yellow recess area was created “at a side of the gate structure,” whereas the green part of the recess was not; it was purely a vertical component of the etch:



EX1001, Fig. 6 (annotated).

59. The yellow recess must exist according to the claims. The recess cannot purely comprise the green (vertical) portion. The specification confirms this by stating that the etch extends horizontally, in the example below, in the direction under the spacers 40 and the gate structure 30, and does not only etch vertically:

As shown in FIG. 6 to FIG. 8, a second etching process 46 is carried out to **etch the fin structures 12 under the gate structure 30 and the spacers 40**. After the etching process, a recess 60 may be formed in each fin structure 12 at **at least one side of the gate structure 30**.

EX1001, 5:55-60 (emphasis added).

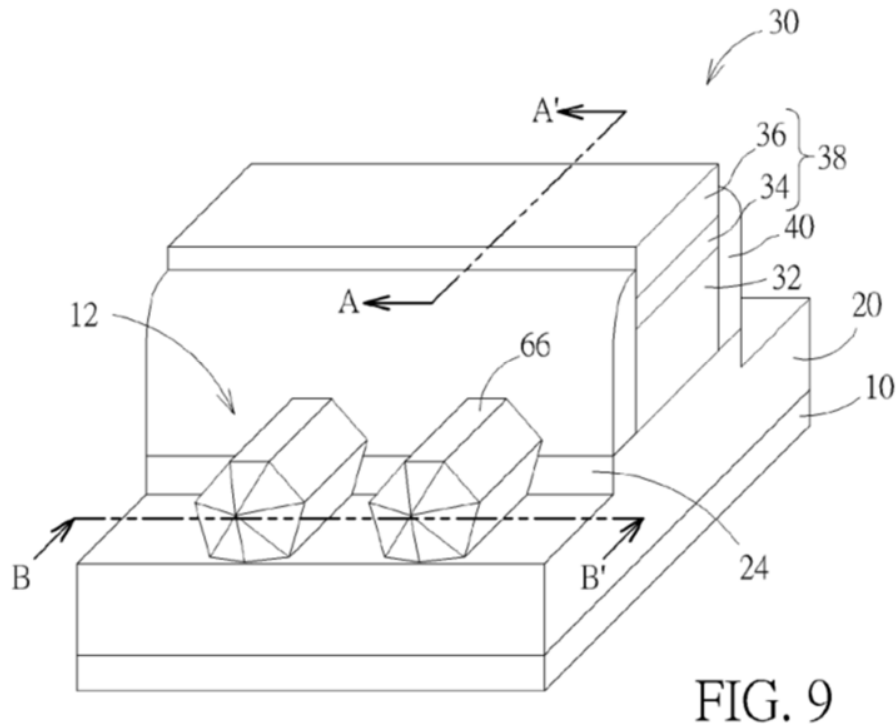
60. The above quote directly ties together the concept of etching horizontally to the formation of the recess “at at least one side of the gate structure 30,” which is the claim language, in that the former is what causes the latter.

61. Thus, at least part of the etch must extend horizontally and the recess must be formed at least partly horizontally, not just vertically, which would not be at a side of the gate structure, since the side of the gate structure is a vertical wall. As explained below, none of the asserted prior art discloses or renders obvious this limitation, nor does the Petition argue that it does, as each reference lacks the horizontal (yellow) etch direction of the recess.

62. The patent also explains that “a bottom surface of the recess has a second depth, and the second depth is deeper than the first depth,” *i.e.*, the depth to which the isolation structure was etched. EX1001, 2:10-13, claim 1. Moreover, because the isolation structure 20 fully surrounds the fin structures on all four sides, when the fin structures are etched down to form recesses 60, the isolation structure 20 fully surrounds the recesses 60, as can be seen in Fig. 6 above.

63. Finally, “FIG. 9 is a schematic perspective view showing the semiconductor device after the formation of an epitaxial layer.” EX1001 at 6:38-40.

Figure 9 illustrates an embodiment of a semiconductor device formed through the claimed fabrication method:



Id. at Fig. 9.

64. “As shown in FIG. 9 . . . an epitaxial growth process . . . maybe carried out in order to grow an epitaxial structure [66] in each corresponding recess 60.” *Id.* at 6:43-48. “[E]ach epitaxial structure 66 may completely cover the bottom surface 68 and sidewalls 70 of the corresponding recess 60.” *Id.* at 6:48-50. Because the isolation structure 20 surrounds the recesses 60 on all four sides, when the epitaxial structures 66 are formed in the recesses 60, the isolation structure 20 also fully surrounds the epitaxial structures 66, as can be seen in Fig. 9 above. This

beneficially ensures that the epitaxial structures are structurally separate and isolated, preventing unwanted contact and electrical interaction and thereby ensuring that each fin structure operates independently without interference. Moreover, “through etching the isolation structure 20 at two sides of the gate structure 30, the epitaxial structure 66 may be formed with a desired height (also called depth) and without any void defects.” EX1001 at 8:1-4. Thus, the ’384 patent’s isolation structure provides an improvement over prior-art semiconductor devices by mitigating defects associated with epitaxial structures.

65. These innovative aspects of the invention are embodied in all challenged claims via claim 1, which recites:

A fabrication method for a semiconductor device, comprising:

forming a fin structure, protruding from a surface of a substrate, wherein the

fin structure comprises a top surface and two side surfaces;

forming an isolation structure to surround the fin structure;

forming a gate structure, overlaying the top surface and the two side surfaces

of a portion of the fin structure, and covering a portion of the isolation

structure;

after the step of forming the gate structure, ***etching the isolation structure*** exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth;

forming a recess in the fin structure at a side of the gate structure; and

forming an epitaxial layer to fill up the recess, wherein a bottom surface of the recess has a second depth, and the second depth is deeper than the first depth.

EX1001, claim 1.

VII. Analysis Of The Grounds

A. Grounds 1A And 1B Fail To Disclose Or Render Obvious The Challenged Claims

1. Xu Fails To Disclose Or Render Obvious “Forming An Isolation Structure To Surround The Fin Structure” (Element 1[b])

a. Xu’s Alleged Isolation Structure Does Not Surround A Fin

66. The Petition alleges that Xu’s “isolation features 130” (the alleged isolation structure) surround the “fins 120.” Pet., 17-18. However, as shown in the figure below (annotated in the Petition), Xu’s “isolation features 130” do not surround the fin structures on all four sides of the fins 120, but rather only cover two sides of the fins 120:

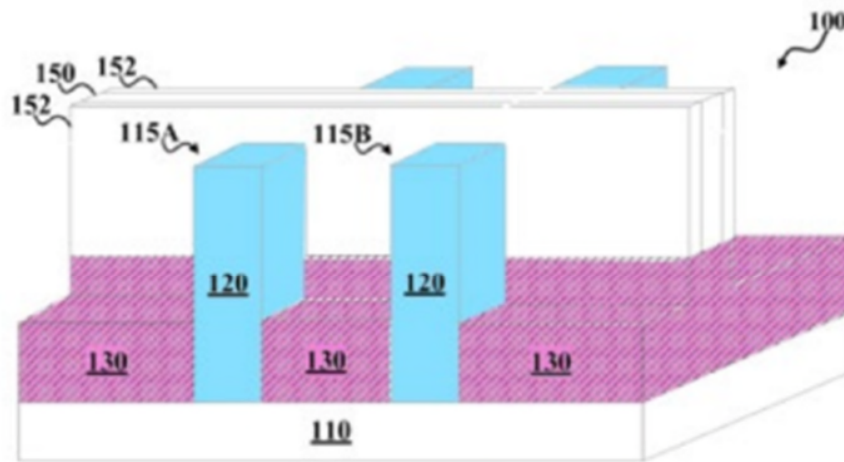


FIG. 3

Pet., 18 (showing annotated EX1004-Xu, Fig. 3).

67. This is in contrast with the challenged claims, which require that the “isolation structure . . . **surrounding** the fin structure.” As explained above in Section VI, an important feature of the '384 patent's claimed method is that the isolation structure surrounds the fin structure on all four sides, thereby completely isolating the fin structures and the epitaxial structures formed on the fin structures. That the isolation structure surrounds the fin structures is confirmed by the '384 patent's specification, which explains that “a lower portion of each fin structure is **embedded** in the isolation structure 20,” indicating that the isolation structure covers all four sides of each fin structure. EX1001 at 3:61-62 (emphasis added). This is further confirmed by the '384 patent's figures, which consistently illustrate the

isolation structure 20 covering all four sides of the fin structures 12, not merely two of the sides as in Xu:

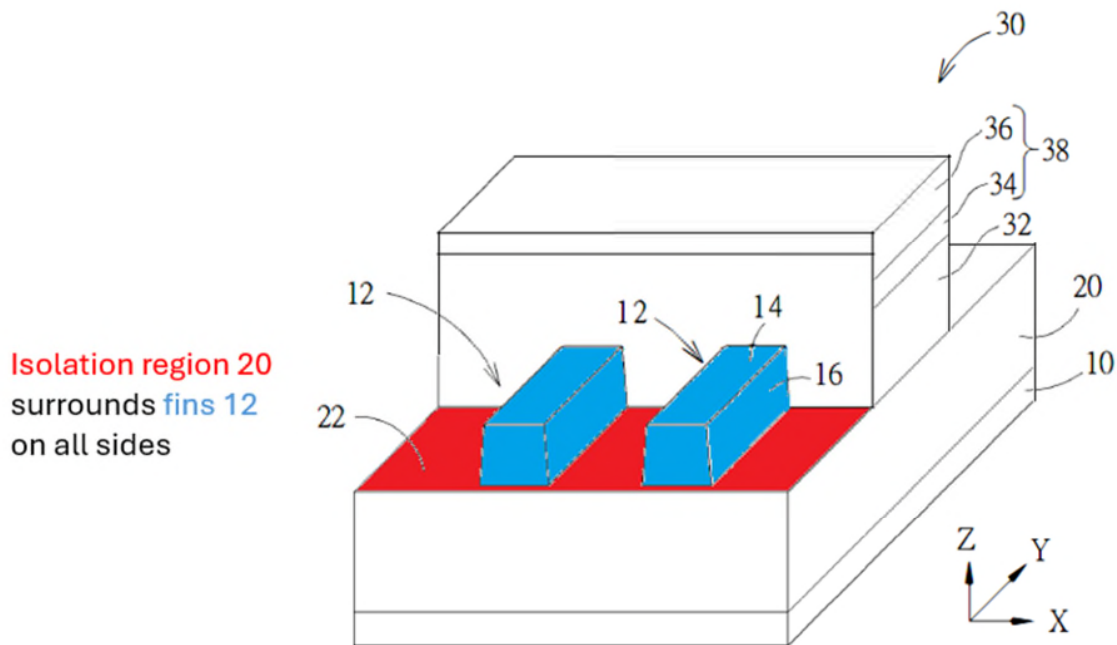


FIG. 2

EX1001 at Fig. 2 (annotated); *see also id.* at Figs. 3, 5.

68. Moreover, the figures also illustrate that the isolation structure 20 surrounds all four sides of the etched down fin structures (recesses 60) and the epitaxial structures 66 formed over the etched down fin structures:

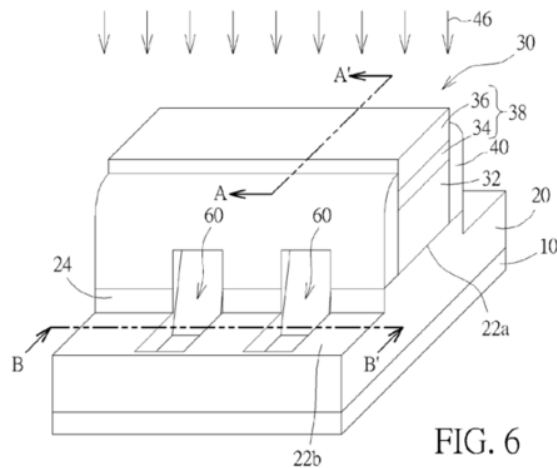


FIG. 6

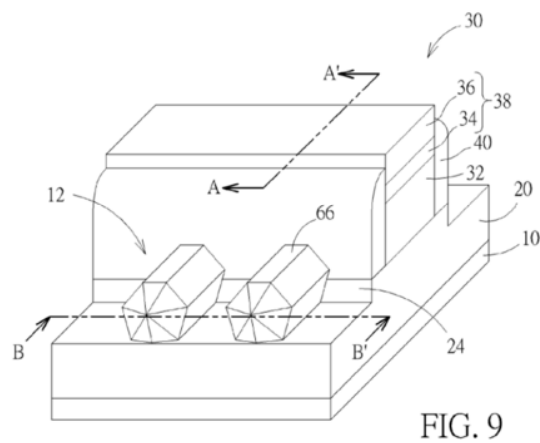


FIG. 9

EX1001 at Figs. 6 and 9.

69. Thus, a POSITA would have understood that, in the claimed method, the isolation structure surrounds the fin structure on all four sides. See EX2006 (“surround” means “to enclose on all sides”).

70. In contrast, Xu’s “isolation features 130” do not surround the fin structures as required by the challenged claims. Although Xu states that “[i]solation features 130 . . . surround the fin structures 115A and 115B,” (EX1004-Xu at 3:54-56) a POSITA would have understood that Xu’s usage of the term “surround” is inconsistent with the claimed method. That passage in Xu describes Xu’s Figure 2, which shows that isolation features 130 do not, in fact, surround the fin structures but rather only cover two sides of each fin:

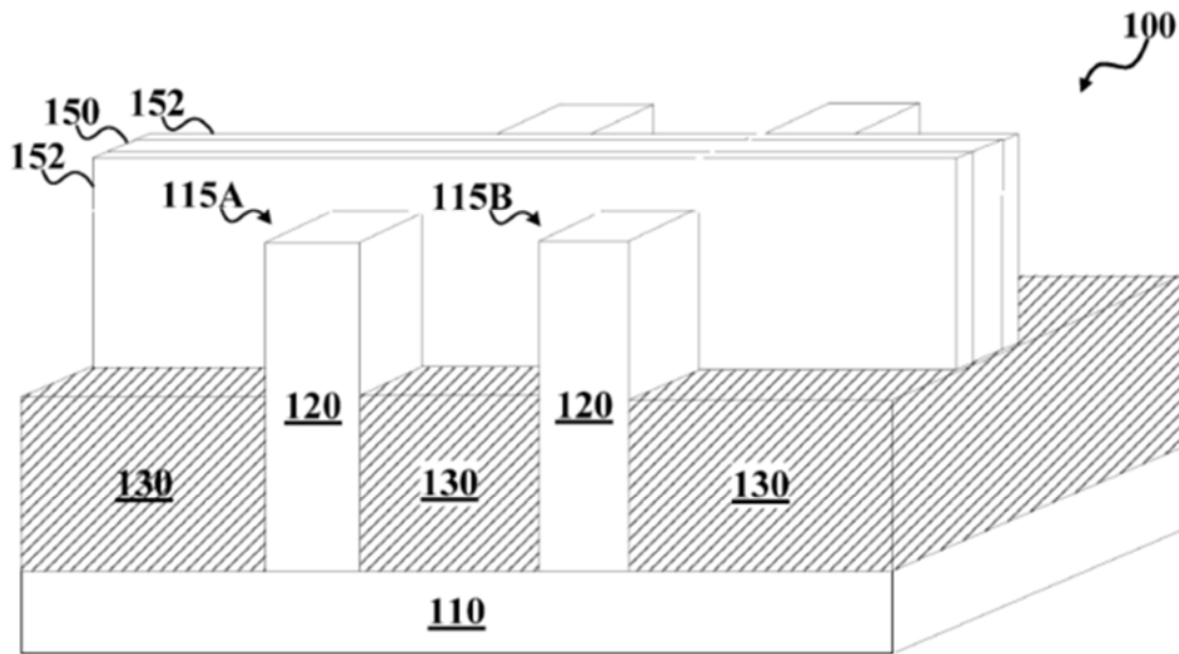


FIG. 2

EX1004-Xu at Fig. 2.

71. In contrast to the '384 patent's figures, which all illustrate the isolation structure surrounding the fin structures, all of Xu's figures consistently illustrate "isolation features 130" as covering only two sides of the fins 120. EX1004-Xu at Figs. 2-6, 8A-C, 9A-C, 10A, 11A, 13A, 14A, 15A, 16A.

b. Xu's Alleged Isolation Structure Does Not Surround Xu's Merged Fin Structure

72. Moreover, Xu fails to disclose or render obvious this limitation for an additional reason. Even if Xu's isolation features 30 are interpreted as

“surrounding” fins 120, Xu’s isolation features nevertheless do not surround Xu’s “fin structure” because unlike the ’384 patent, Xu’s device merges its fins together into a single, merged “fin structure.” For example, Xu explains that a “fin template 135 is formed by merging together the fins 120 of the FinFET device 100.” EX1004-Xu at 5:2-4. A “semiconductor material is epitaxially grown by an epi process until the fins 120 of the fin structures 115A and 115B are merged together to form the fin template 135.” *Id.* at 5:8-10. Xu’s Figure 4 illustrates the merging together of fins 120 to form fin template 135:

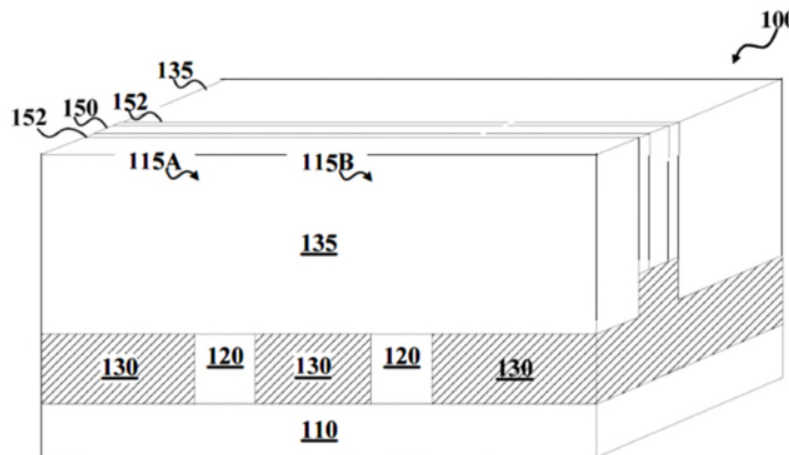


FIG. 4

Id. at Fig. 4.

73. Xu explains that “[t]hough the fins 120 and fin template 135 are depicted separately, it is understood that ‘fin template’ can refer to the newly grown epi semiconductor material alone (depicted as fin template) or the newly grown epi

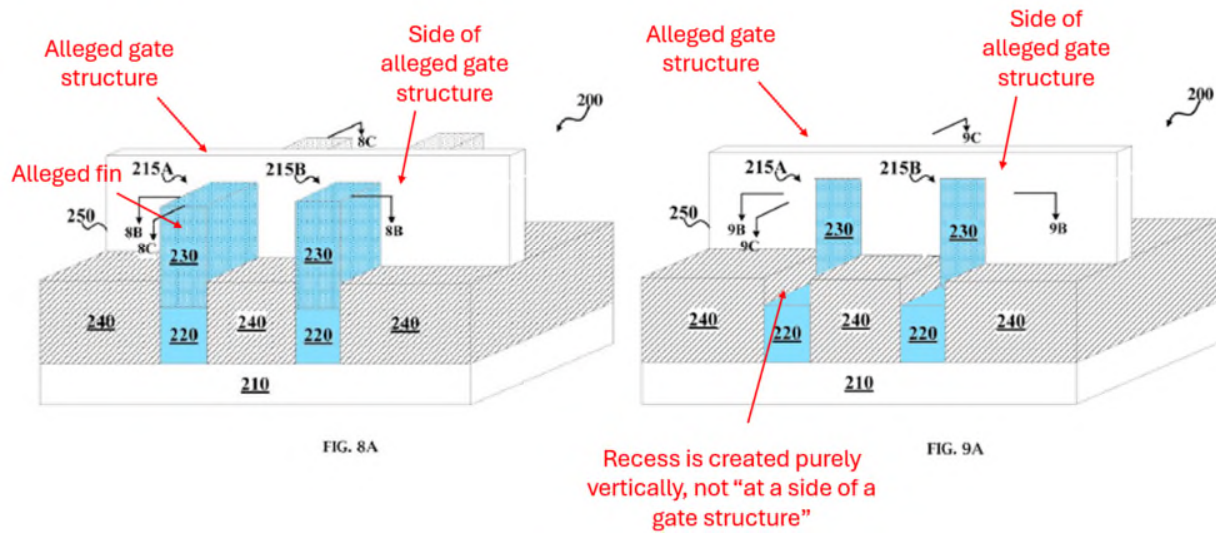
semi-conductor material combined with the initial fins (depicted as fins 120). *Id.* at 5:28-33. Thus, a POSITA would have understood that Xu's device's "fin structure" includes both fins 120 and fin template 135, which merges adjacent fin structures 115A and 115B.

74. As shown in Figure 4 above, Xu's fin template 135 is disposed on top of isolation features 130. As such, Xu's "isolation features 130" do not surround its fin structure because it does not enclose *any* side of the merged fin structure, *e.g.*, the part made up of fin template 135.

75. Accordingly, Xu does not disclose "an isolation structure . . . surrounding the fin structure, as required by all challenged claims." The Petition also alleges that Xu renders obvious this limitation but does not provide any explanation or analysis on this point. Pet. at 16-17. Thus, Ground 1A fails.

2. Xu Fails To Disclose Or Render Obvious "Forming A Recess In The Fin Structure At A Side Of The Gate Structure" (Element 1[e])

76. As explained above in Section 29, the recess formed in the fin must extend at least in the horizontal direction in order to be a recess "at a side of the gate structure." EX1001, claim 1. Ground 1 fails to disclose that feature. In Xu, as the Petition concedes, the etching of the fin to create the alleged recess is purely vertical, and has no horizontal component, and therefore is not formed "at a side of the gate structure":



Pet. 23 (annotated).

77. Indeed, as seen above, some amount of item 230, the top part of the fin, remains, confirming that the etch did not extend horizontally. The specification confirms that the etch is only vertical as well, stating that "the fin portions 220 may be etched into the substrate 210," which is located directly below the fin, as seen in Figures 8A-9A. EX1004-Xu at 8:36-37.

78. The Petition does not rely on Brask to supplement Xu for this element. Pet. 21-26. Thus, the Petition fails to establish disclosure of the element and the Petition should be denied.

3. Xu Fails To Disclose Or Render Obvious “Etching The Isolation Structure” And “Forming A Recess In The Fin Structure”

79. As the Petition concedes, there is no disclosure in Xu of a process, embodiment, or structure created by both “etching the isolation structure” and “forming a recess in the fin structure,” which are both requirements of all claims. Pet., 20-26. The Petition argues that Figures 1-6 constitute a first embodiment in which an isolation structure is etched, and that Figures 7-11A constitute a second embodiment in which a recess in the fin structure is formed. Pet., 20-26. Xu itself refers to these two embodiments as distinct approaches and different methods. EX1004-Xu, 1:49-58 (“FIG. 1 is a flow chart of *a method* for fabricating a fin-like field effect transistor (FinFET) device according to aspects of the present disclosure”; “FIG. 7 is a flow chart of *another method* for fabricating a FinFET device according to aspects of the present disclosure.”).

80. The Petition’s rationale “to combine the fin-recessing step [of the second embodiment] with Xu’s first embodiment” is that it would “achieve and optimize strain” in the first embodiment. Pet. 23-24. But that only relates to the second and third embodiments, Figures 7-11C and 12-16C respectively, as they refer to “FinFET devices 200 and 400,” discussed in those embodiments. EX1004-Xu, 15:56-60. And Xu states that “controlling source and drain trench depth (for example, d1 and d2) for the epi source and drain features, strain for both PMOS and

NMOS FinFET devices can be achieved and optimized.” EX1004-Xu, 58-60; Pet. 23-24. The Petition’s argument is that changing depth of a trench in a fin can impact channel strain.

81. However, the first embodiment, Figures 1-6, describes a different and incompatible method of achieving strain from that of the second (and third) embodiment that the Petitioner seeks to add to the first embodiment, one that has no fin trench, and so the optimization methods of the second (and third) embodiments are inapplicable. In the first embodiment, starting with Figure 2, the isolation structure is etched to arrive at Figure 3:

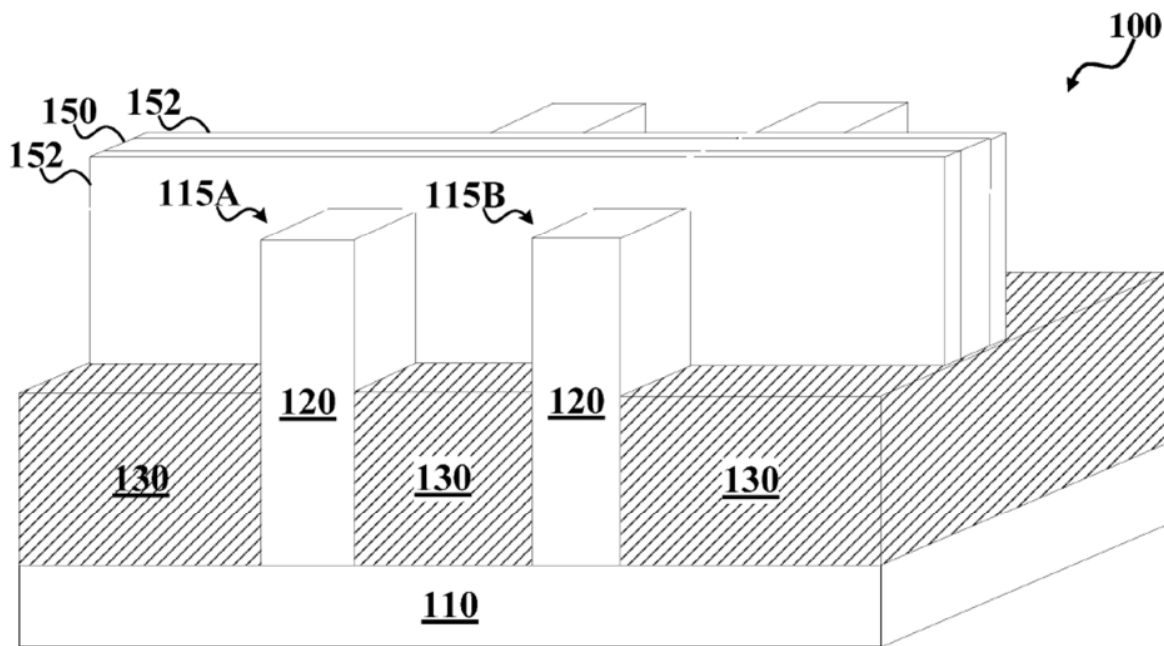


FIG. 2

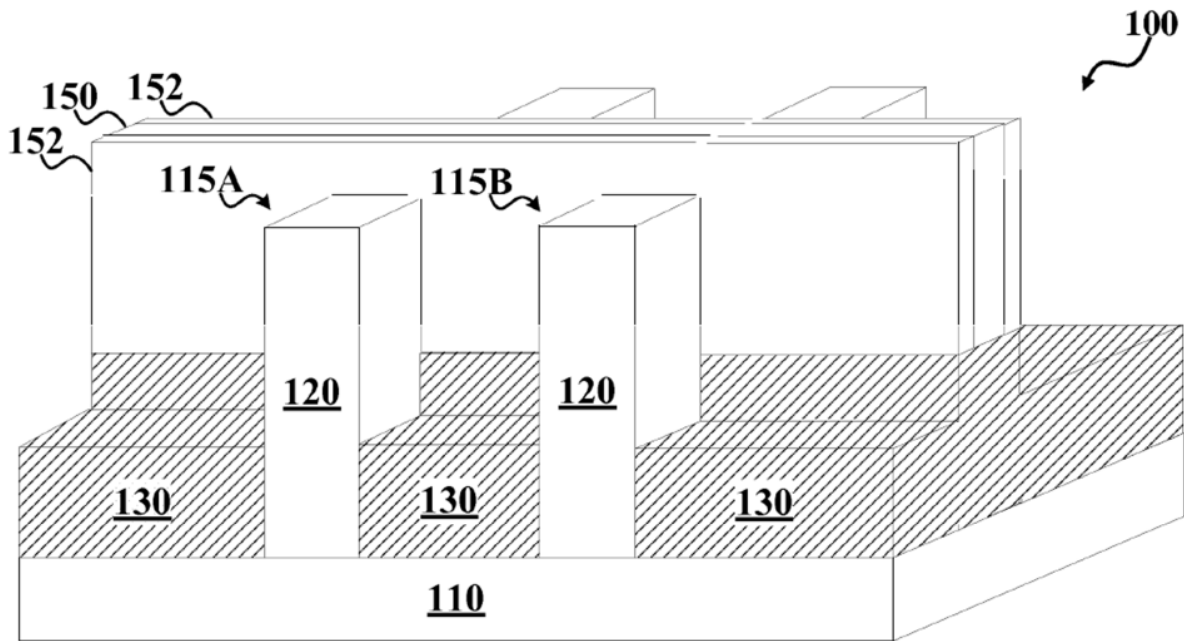


FIG. 3

EX1004-Xu, Figs. 2 and 3. Then, “a fin template 135 is formed on exposed portions of the fins 120.” *Id.*, 5:1-2.

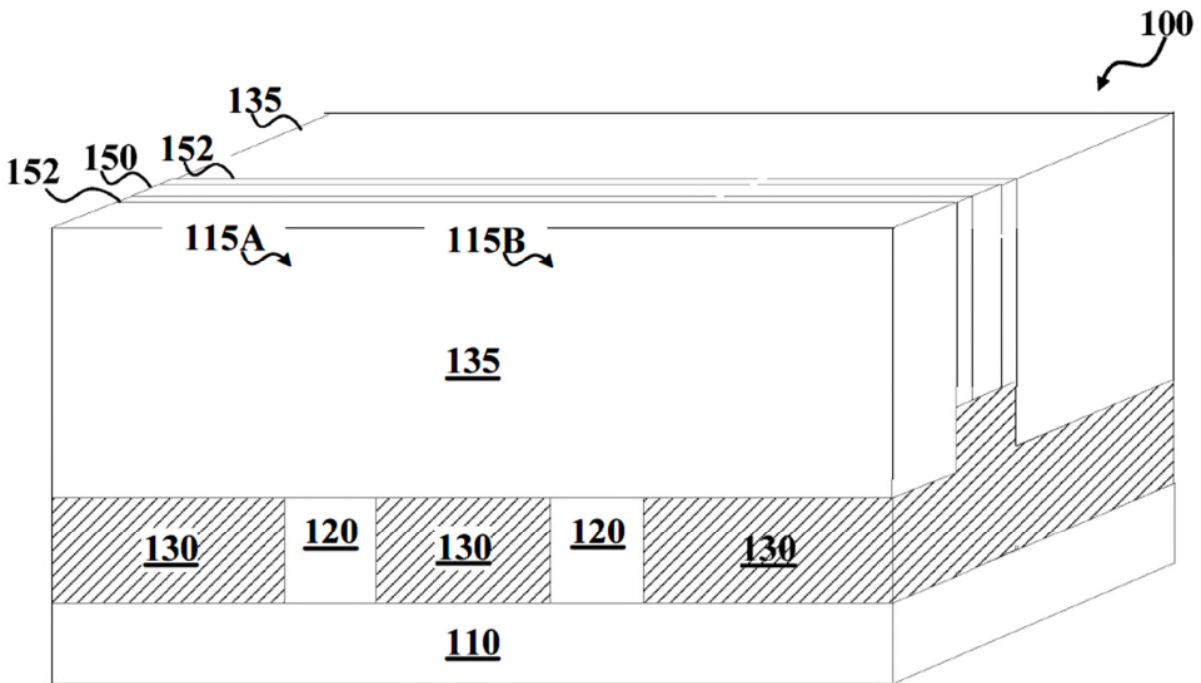


FIG. 4

Id., Fig. 4.

82. Then, in Figure 5, “a process is performed to recess the fin template 135” from what is shown in Figure 4:

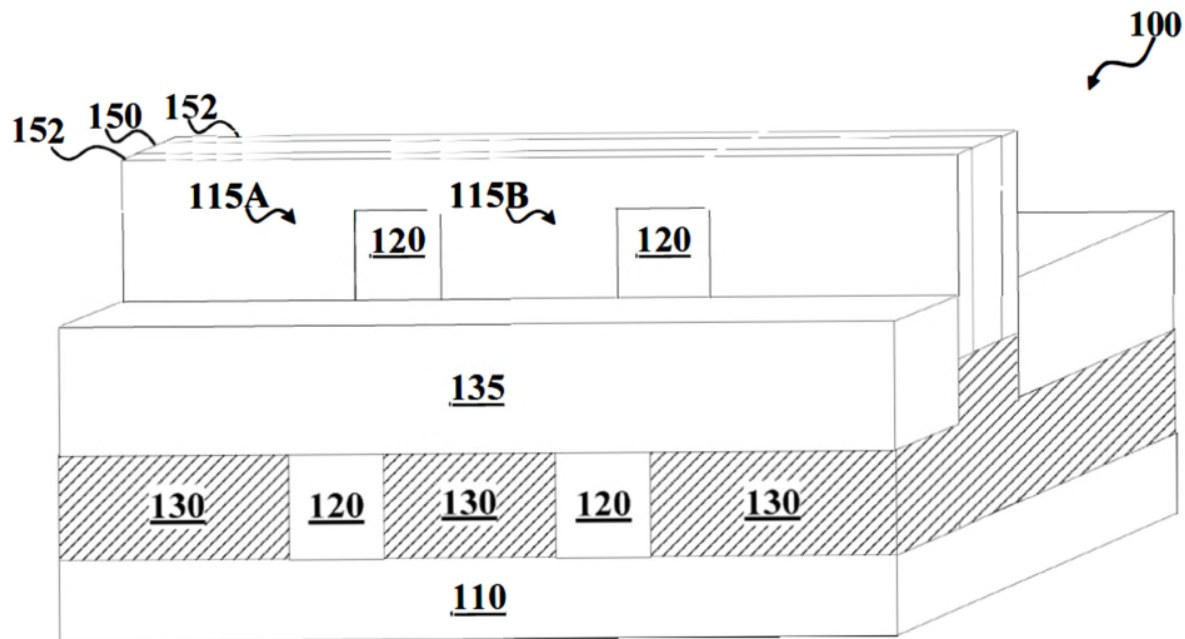


FIG. 5

Id., 5:34-35, Fig. 5.

83. Specifically, “[t]he fin template 135 is etched back sufficiently to expose the channels of the fin structures 115A and 115B,” as illustrated in FIG. 5. *Id.*, 5:43-45; Fig. 5. As Xu states, “[t]his ensures that later-formed raised source and drain features (semiconductor material 160) **can effectively introduce strain** into the channels of the fins structures 115A and 115B.” *Id.*, 5:45-47.

84. This process, as shown above, removes part of the fin structure, but notably, as the Petition concedes, it does not meet the claim requirement to “form[] a recess in the fin structure at a side of the gate structure.” Pet. 20-26.

85. Then, in Figure 6, “a semiconductor material 160 is epitaxially grown over the fin template 135. In the depicted embodiment, a semiconductor material is epi grown on the exposed fin template 135 in the source and drain regions of the fin structures 115A and 115B”:

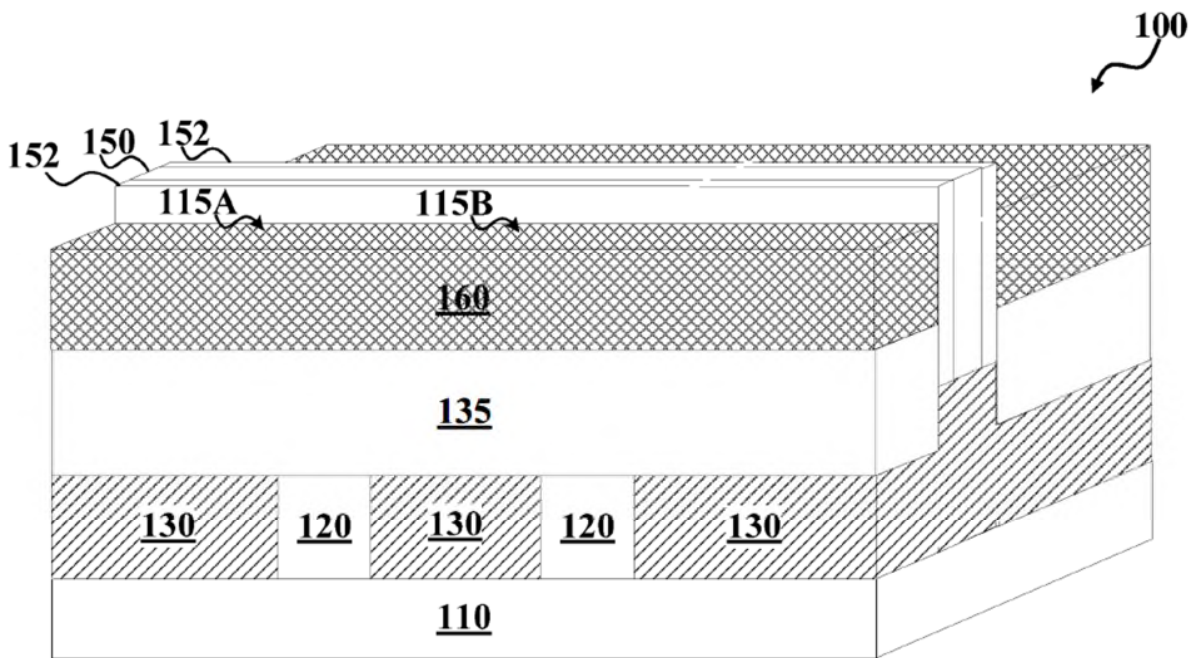


FIG. 6

EX1004-Xu, 5:49-53; Fig. 6.

86. Explaining what was alluded to with regard to Figure 5 above, Xu explains that “[t]he epi grown semiconductor material 160 ***generates channel strain*** for the fin structures 115A and 115B.” *Id.*, 5:53-55 (emphasis added). As Xu

therefore states, the semiconductor material 160 generates channel strain, not the depth of the trench, which does not exist in the first embodiment.

87. Thus, the first embodiment has a different method from the second and third regarding how to introduce channel strain, a method that does not benefit from the alleged modification and is incompatible with the proposed modifications. Given that fact, a POSITA would not be motivated to combine embodiments and perform both claimed steps.

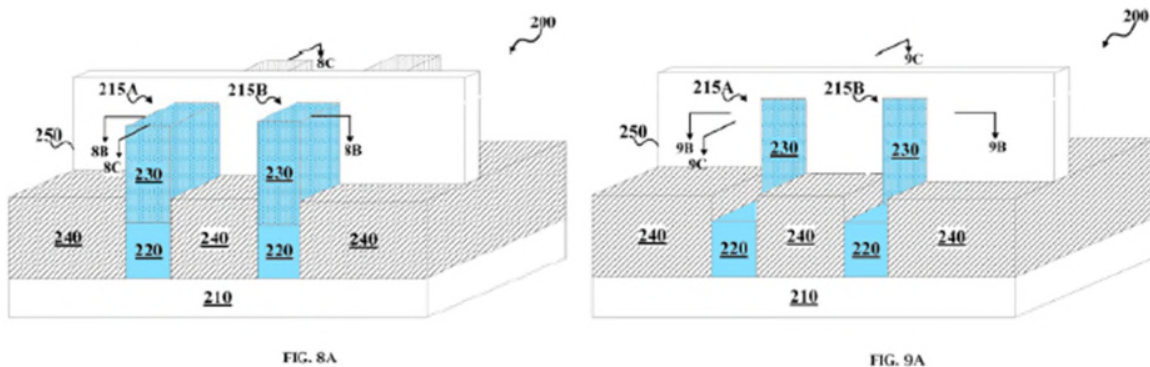
4. Even If Ground 1 Establishes Both “Etching The Isolation Structure” And “Forming A Recess In The Fin Structure,” It Fails To Disclose “The Second Depth Is Deeper Than The First Depth”

88. The challenged claims require that the fin recess is created to a depth greater than that to which the isolation structure is etched. EX1001, Claim 1. Xu does not disclose that requirement, even in the alleged modification combining different aspects of different embodiments, which a POSITA would not be motivated to do, as explained above. The Petition argues that, when combining the first and second embodiments of Xu, which a POSITA would not do, as explained above, “the second depth is necessarily ‘deeper than the first depth.’” Pet., 30. Not so. The Petition cobbles together two embodiments, one that etches a fin without concern as to the height of the surrounding isolation structure (second embodiment) and one that etches an isolation structure, without concern as to the height of the neighboring

fin. There is nothing to suggest that, even if a POSITA were to combine both steps, one etch would go down further than the other. Petitioner's expert provides no rationale, simply repeating what the Petition states. EX1003 ¶¶ 101-102. It is simply hindsight and attorney argument to state that one would necessarily reach a further depth than the other, and specifically that the fin recess would be at a greater depth.

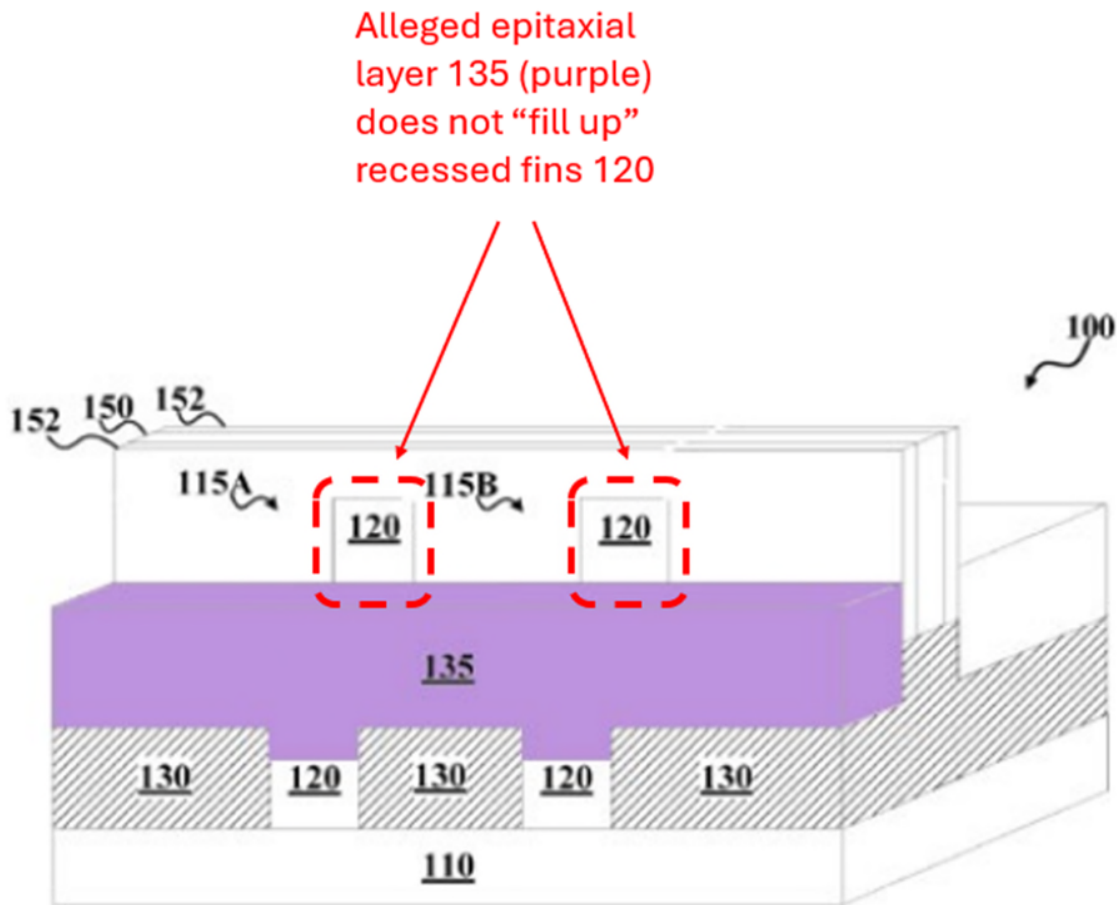
5. Xu Fails To Disclose Or Render Obvious “Forming An Epitaxial Layer To Fill Up The Recess” (Element 1[f])

89. The Petition alleges that Xu's “fin template 135” (the alleged epitaxial layer) fills up the recesses. Pet., 27-29. As with other elements, the Petition improperly combines different aspects of different embodiments. However, even in the alleged modification, Xu's “fin template 135” does not “fill up the recess,” as required by the challenged claims. The Petition alleges that Xu discloses the “a recess in the fin structure at the side of the gate structures, as shown in Figures 8A and 9A”:



Pet., 22-23 (annotated EX1004-Xu, Figs. 8A and 9A).

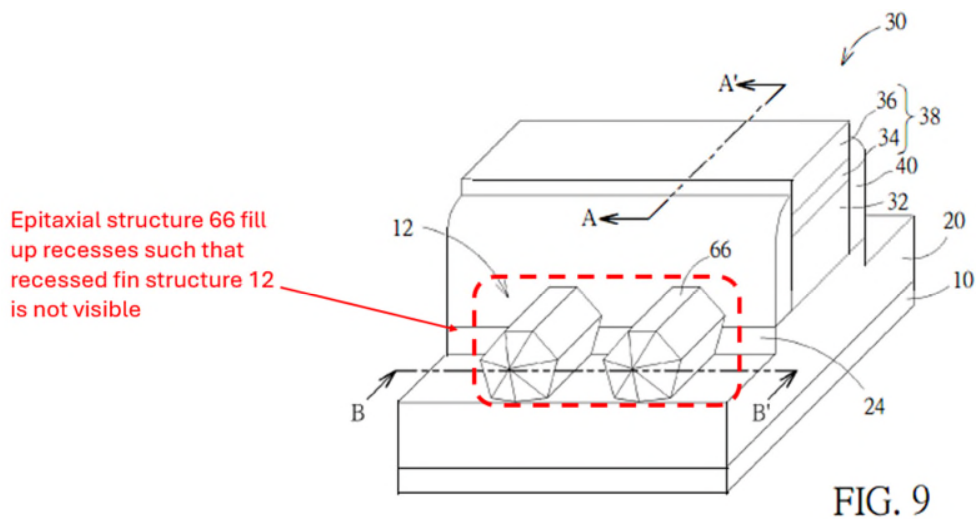
90. As shown, the Petition's alleged recess (colored in blue above) includes the exposed portions of the fin under the gate structure. *Id.* However, as shown in the figure below (annotated and modified in the Petition), Xu's "fin template 135" does not fill up the recesses, as the fin template does not extend to the top of the alleged recess:



Pet., 28 (showing annotated and modified figure, further annotated here).

91. As shown, the alleged epitaxial layer does not extend vertically to the top of the recess, as evidenced by the fact that the tops of the fins 120 are visible over the top of the fin template 135.

92. This is in contrast with the challenged claims, which require the “epitaxial layer to fill up the recess.” The ’384 patent specification explains that “[m]ore precisely, each epitaxial structure 66 may **completely cover the bottom surface 68 and sidewalls 70 of the corresponding recess 60.**” EX1001, 6:48-50 (emphasis added). As shown in Figures 9 and 10 below, this means that epitaxial structures 66 completely fill up the recess 60, such that the non-recessed portions of the fins are covered by the epitaxial structure:



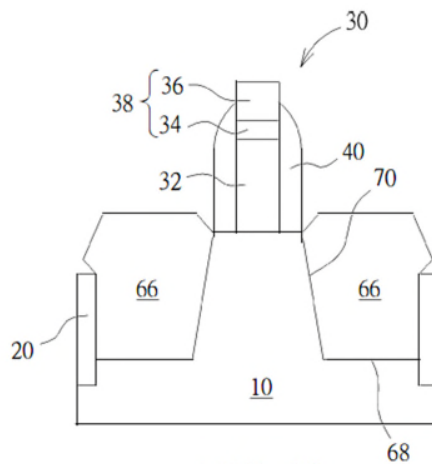


FIG. 10

Id., Figs. 9 (annotated) and 10.

6. Xu Fails To Disclose Or Render Obvious Claim 8

93. Claim 8 recites:

The fabrication method according to claim 7, wherein a step for forming the spacer comprises:

depositing a material layer to conformally cover the gate structure and the fin structure, and

etching the material layer until the isolation structure is exposed.

EX1001, claim 8.

94. Contrary to the Petition's allegations, Xu does not disclose or render obvious claim 8. Xu's entire disclosure regarding forming a spacer is that "spacers 152 may be formed by depositing a silicon nitride layer." EX1004-Xu, 4:46-49. Xu does not elaborate any further, and certainly does not mention anything about "depositing a material layer to conformally cover the gate structure and the fin

structure, and etching the material layer until the isolation structure is exposed.” The Petition does not dispute this.

95. Despite this, the Petition alleges that “[a] POSITA would have understood and found obvious that the deposited silicon nitride layer would conformally cover the gate structure and the fin structure as recited in claim 8.” Pet., 36. The Petition argues that “a POSITA would have understood that . . . material like silicon nitride were typically deposited using conformal deposition techniques such as LPCVD (low-pressure chemical vapor deposition) or PECVD (plasma-enhanced CVD), which were well-known to coat all exposed topographies uniformly.” *Id.* This argument requires several leaps of logic, none of which are supported by Xu or any other evidence.

96. As an initial matter, the Petition fails to set forth any motivation or rationale to use any particular deposition method to form Xu’s spacers. Pet., 36-37. I understand that even in single-reference obviousness grounds, a showing of a suggestion or motivation to modify the teachings of that reference to the claimed invention is required. Here, the Petition uses only conclusory language: “materials like silicon nitride were typically deposited using conformal deposition techniques,” “[a] POSITA therefore would have understood that the deposited SiN layer conformally coats both of these structures before being anisotropically etched to

form spacers,” and “it would have been obvious to a POSITA to simply substitute one of these well-known conformal deposition processes into the method of Xu.” Pet., 36-37. I understand that such conclusory expert testimony is inadequate to support an obviousness determination.

97. Moreover, the Petition is incorrect that Xu’s spacer would inherently be formed using a conformal deposition technique. The Petition argues that it was desirable to use PECVD because it is conformal, which is circular and based on hindsight based on the claim language. Pet., 36. Contrary to the Petition’s allegations, a POSITA would have understood that gate sidewall spacers could be formed using non-conformal deposition/etching techniques, such as chemical mechanical polishing (CMP).

98. A POSITA would have understood that, when selecting a deposition technique: (1) conformality is relative, with certain deposition techniques resulting in more or less conformality than others; and (2) there are tradeoffs between depositing a material conformally and other critical manufacturing metrics. EX2004 at 2, 4-5. Step coverage is a manufacturing metric that defines how uniformly a deposited material conforms to the underlying topography of a substrate. EX2004 at 1. But uniformity comes at a cost. For example, “[t]he process conditions that favor excellent step coverage—such as high pressure and low power—often result

in a slower deposition rate.” EX2004 at 4. Moreover, while PECVD results in step coverage that is more conformal relative to some other techniques, it does not result in 100% conformal step coverage. EX2004 at 5. A POSITA would have understood that other deposition techniques result in better step coverage than PECVD. EX2004 at 5.

99. The Petition’s argument appears to be that Xu’s spacer would be formed using LPCVD or PECVD because it is formed from silicon nitride. Pet., 36-37. However, as Petitioner’s expert admitted, there were non-conformal methods of depositing silicon nitride at the time of the ’384 patent, which resulted in certain benefits, such as a faster deposition speed and avoidance of strain on the layer that could destroy the layer. EX2005-Lee-Dep at 28:5-32:7. The Petition fails to justify why a POSITA would value whatever level of conformality PECVD could provide, at the cost of reduced speed and increased strain. Neither the Petition nor Petitioner’s expert analyzed any of these trade-offs, nor any reason why any arbitrary level of conformality would be needed or beneficial in Xu, or even what that level would be. Pet., 36-37; EX2005-Lee-Dep at 54:10-55:4, 57:15-58:23. Nor do they address any other critical manufacturing metric that would be negatively impacted in achieving such a level of conformality, or why a POSITA would choose a conformal deposition technique in spite of these negative impacts. *Id.* Thus, the Petition fails to provide

any reason or motivation to modify or combine Xu with any particular deposition technique.

100. The Petition relies on Exhibit 1025, which the Petition alleges “describe[s] CVD techniques for conformal deposition of silicon nitride.” Pet., 36. But again, the Petition does not provide any reason or motivation to combine Xu with Exhibit 1025 or any other deposition method. Further, Exhibit 1025 does not in fact describe PECVD to deposit silicon nitride, but rather ***hydrogenated*** silicon nitride:

TABLE 16-2 PROPERTIES OF HIGH-TEMPERATURE-CVD-SILICON-NITRIDE AND PECVD-SILICON-NITRIDE		
Property	HT-CVD—NP 900°C	PE-CVD—LP 300°C
Composition	Si ₃ N ₄	Si ₃ N ₂ H ₂
Si/N ratio	0.75	0.8–1.0
Density	2.8–3.1 g/cm ³	2.5–2.8 g/cm ³
Refractive index	2.0–2.1	2.0–2.1
Dielectric constant	6–7	6–9
Dielectric strength	1 × 10 ⁷ V/cm	6 × 10 ⁴ V/cm
Bulk resistivity	10 ¹³ –10 ¹⁷ ohms/cm	10 ¹³ ohms/cm
Surface resistivity	> 10 ¹³ ohms/square	1 × 10 ¹³ ohms/square
Stress at 23°C on Si	1.2–1.8 × 10 ¹⁰ dyn/cm ² (tensile)	1–8 × 10 ⁹ dyn/cm ² (compressive)
Thermal expansion	4 × 10 ⁻⁴ /°C	> 4 < 7 × 10 ⁻⁴ /°C
Color, transmitted	None	Yellow
Step coverage	Fair	Conformal
H ₂ O permeability	Zero	Low–none
Thermal stability	Excellent	Variable > 400°C
Solution etch rate		
HFB 20–25°C	10–15 Å/min	200–300 Å/min
49% HF 23°C	80 Å/min	1500–3000 Å/min
85% H ₃ PO ₄ 155°C	15 Å/min	100–200 Å/min
85% H ₃ PO ₄ 180°C	120 Å/min	600–1000 Å/min
Plasma etch rate		
70% CF ₄ /30% O ₂ , 150 W, 100°C	200 Å/min	500 Å/min
Na ⁺ penetration	< 100 Å	< 100 Å
Na ⁺ retained in top 100 Å	> 99%	> 99%
IR absorption		
Si–N max	~ 870 cm ⁻¹	~ 830 cm ⁻¹
Si–H minor	—	2180 cm ⁻¹

EX1025 at 298.

101. As shown above, Exhibit 1025 explains that HT-CVD is used to deposit silicon nitride, while PE-CVD (the process that the Petition alleges would be used in Xu) is used to deposit hydrogenated silicon nitride. A POSITA would have understood that hydrogenated silicon nitride is not the same as silicon nitride. Indeed, Petitioner's expert admitted as much during his deposition. EX2005-Lee-Dep at 47:10-48:14. The Petition does not even allege that hydrogenated silicon

nitride could be used to form Xu's spacers and thus does not establish any connection between the PECVD process described in Exhibit 1025 and Xu's spacer formation.

7. Xu Fails To Disclose Or Render Obvious Claims 4 And 9

102. Claim 4 recites: "The fabrication method according to claim 1, wherein the gate structure is a dummy gate structure."

103. Claim 9 recites:

The fabrication method according to claim 1, further comprising:

depositing an interlayer dielectric to surround the gate structure;

removing the gate structure to leave a trench;

forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench; and

forming a conductive layer to fill up the trench.

EX1001, claim 9.

104. Contrary to the Petition's allegations, Xu does not disclose or render obvious the elements of claims 4 and 9. These claims recite a specific "replacement metal gate (RMG)" process for replacing a dummy gate structure with a replacement metal gate. Xu's entire disclosure regarding such a replacement process is that "[t]he gate structure 150, such as the gate electrode, may be formed in a gate first or gate last process." EX1004-Xu, 4:13-14. According to the Petition, the words "gate last process" in Xu apparently disclose every limitation of claims 4 and 9. Pet., 32-33, 38-42. That is a monumental leap that defies logic.

105. Alternatively, the Petition alleges that Xu's disclosure of a "gate last process" renders obvious each element of claims 4 and 9. Pet., 32-33, 38-42. I disagree. The Petition points out that the '384 patent states that "the RMG process and the contact formation process are well-known to those skilled in the art." Pet., 38-39. However, a POSITA would have understood that while an RMG process in general was known at the time of the '384 patent, claim 9 provides a specific series of steps for replacing a dummy gate structure. One of these steps is "forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench." (element 9[c]). On element 9[c], the Petition merely alleges that "a POSITA would have understood" that Xu's gate-last process "includes 'forming a gate dielectric layer to conformally cover the sidewalls and bottom of the trench.'" Pet., 41 (citing only the challenged patent), without any analysis or factual basis. Moreover, a POSITA would have known that not every gate-last process includes replacing a gate dielectric layer. In fact, Petitioner's expert admitted that, in some gate-last process sequences, a gate dielectric layer is deposited first before putting down the dummy gate. EX2005-Lee-Dep, 72:16-73:3. In such a process sequence, during the gate replacement process, no gate dielectric layer is deposited in the trench. *Id.* Thus, the Petition's analysis not only deficient, but also incorrect, in that a POSITA would have actually understood that Xu's "gate-last process" could refer to a process

sequence that does not include “forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench.”

106. Indeed, Petitioner’s expert admitted that “ideally, you don’t need the gate dielectric on the sidewall of the spacers” (EX2005-Lee-Dep, 71:24-72:12), *i.e.*, the sidewall of the alleged trench, indicating that a POSITA would have understood that Xu’s gate-last process does not include “forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench,” as required by claim 9. As shown below, the Petition’s alleged “trench” is defined by Xu’s spacers 152 on the sides and isolation features 130 on the bottom, and is allegedly formed when the gate structure 150 is removed:

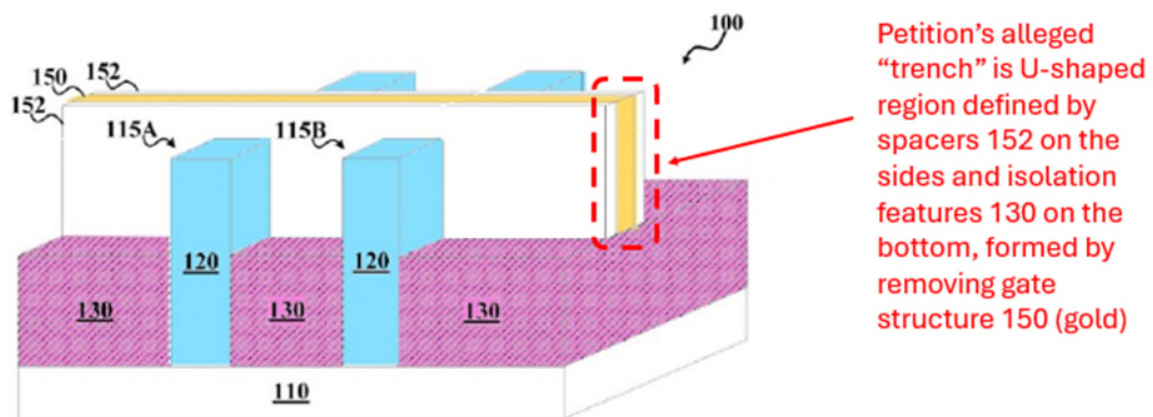


FIG. 2

Pet., 41 (annotated EX1004-Xu Fig. 2, further annotated here).

107. Element 9[c] recites: “forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench.” As Petitioner’s expert conceded, a POSITA would not have been motivated to form a gate dielectric layer to conformally cover a sidewall of the trench, as there is no reason to have the dielectric cover the sidewall. EX2005-Lee-Dep, 71:24-72:12.

8. Ground 1B Fails To Render Obvious Claims 4 And 9

108. The Petition fails to provide any reason or motivation to combine Xu and Brask. The Petition alleges that a POSITA would have been motivated to combine Xu and Brask because:

Xu discloses that the gate structure 150 may be formed in a “gate last process.” EX1004-Xu at 4:13-14. However, Xu does not explicitly disclose implementation details of the gate-last process. Ex. 1003 at ¶ 132. A POSITA therefore would have looked to established prior art, like Brask, for details on gate-last processing in FinFET structures. *Id.*

Pet., 47.

109. But as explained above, a POSITA would have understood that a “gate last process” is a general term that encompasses varying procedures with different steps, including procedures that do not meet the specific steps recited in claims 4 and 9. For example, a POSITA would have known that not every gate-last process

includes replacing a gate dielectric layer. In fact, Petitioner's expert admitted that, in some gate-last process sequences, a gate dielectric layer is deposited first, before putting down the dummy gate. EX2005-Lee-Dep, 72:16-73:3. In such a process sequence, during the gate replacement process, no gate dielectric layer is deposited in the trench. *Id.* Such a gate last process would not include "forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench," as required by claim 9.

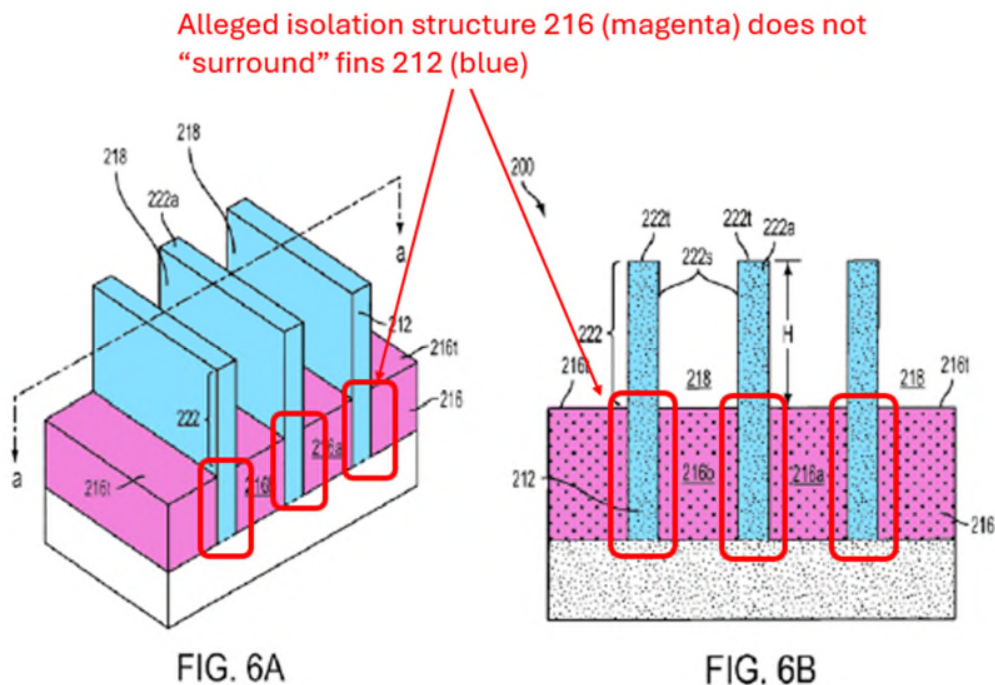
110. Thus, the mere fact that Xu discloses a "gate last process" is insufficient to motivate implementing the specific gate last process recited in claim 9. In fact, Petitioner's expert admitted that "ideally, you don't need the gate dielectric on the sidewall of the spacers" (EX2005-Lee-Dep, 71:24-72:12), *i.e.*, the sidewall of the alleged trench, indicating that a POSITA would **not** have been motivated to "form[] a gate dielectric layer to conformally cover a sidewall and a bottom of the trench," as required by claim 9. And the Petition does not provide any rationale for why a POSITA would want to implement the specific process disclosed in Brask, instead only stating certain benefits that would apply to any gate last process. *See* Pet., 48-49 (stating benefits associated with a gate last process in general). For example, the Petition alleges that a gate last process enables tuning of gate electrode work functions. *Id.* But this only applies to replacing a gate electrode, not a gate dielectric

layer, as required by element 9[c]. Accordingly, the Petition's motivation to combine arguments fail to explain why a person of ordinary skill in the art would have combined elements from Xu and Brask in the way the claimed invention does.

B. Grounds 2A And 2B Fail To Disclose Or Render Obvious The Challenged Claims

1. Lin Fails To Disclose Or Render Obvious “Forming An Isolation Structure To Surround The Fin Structure” (Element 1[b])

111. The Petition alleges that Lin's “insulation regions 216 (the claimed isolation structure) surround the fins 212 as shown in Figures 6A and 6B:



Pet., 64-65 (showing annotated EX1005-Lin, Figs. 6A and 6B, further annotated here).

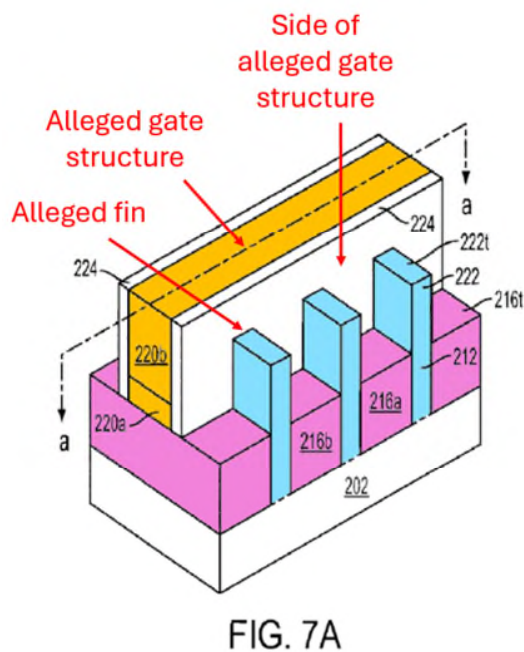
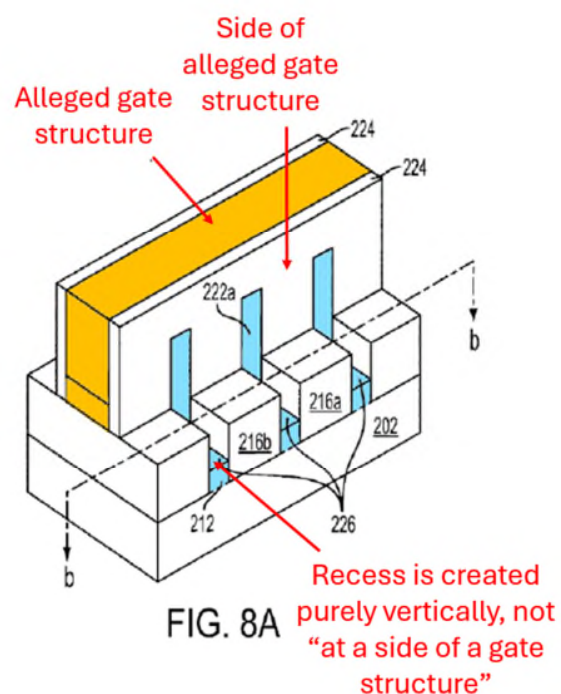
112. However, as shown in the figures above, Lin's insulation regions 216 do not surround the fins 212 on all four sides, but rather only cover two sides of the fins.

113. As explained above in Section VII.A.1 with respect to Xu, a POSITA would have understood that in the '384 patent's claimed fabrication method, the isolation structure is formed such that it surrounds the fin structure on all four sides. See EX2006. In contrast, Lin's insulation regions 216 only cover two sides of the fins. This is apparent from the figures, as well as Lin's description of the insulation regions, which describes "a fin 212 **between** the first and second insulation regions 216a, 216b." EX1005-Lin, ¶[0026] (emphasis added). That is, as illustrated in Lin's Figs. 6A and 6B, insulation regions 216a and 216b are two distinct regions that do not merge, and a fin is between the two regions, such that the insulation regions only cover two sides of the fin. *Id.* This is different from the '384 patent, in which "a lower portion of each fin structure 12 is **embedded** in the isolation structure 20." EX1001 at 3:61-62 (emphasis added). Thus, Lin does not disclose "forming an isolation structure to surround the fin structure," as required by all challenged claims.

2. Lin Fails To Disclose Or Render Obvious "Forming A Recess In The Fin Structure At A Side Of The Gate Structure" (Element 1[e])

114. As explained above in Section VI, the recess formed in the fin must extend at least in the horizontal direction in order to be a recess "at a side of the gate

structure.” Ground 2 fails to disclose that feature. In Lin, as the Petition concedes, the etching of the fin to create the alleged recess is purely vertical, and has no horizontal component, and therefore is not formed “at a side of the gate structure”:



Pet., 59-60 (annotated).

115. As the Petition cites, Lin specifically states that “[t]he portion of the semiconductor fin 212 [blue] *not covered by the gate stack 220 [gold] and spacers 224 formed thereover are recessed to form a recessed portion 226 of the fin 212 [blue].*” Pet. 59 (citing EX1005-Lin, ¶30) (emphasis added). That is, the etch does not extend horizontally and there is thus no fin recess at “*a side of the gate structure.*”

116. The Petition does not rely on Brask to supplement Lin for this element. Pet. 69-71. Thus, the Petition fails to establish disclosure of the element and the Petition should be denied.

3. Ground 2B Fails To Render Obvious Claims 4 And 9

117. The Petition fails to provide a reason or motivation to combine Lin and Brask. The Petition admits that “Lin discloses a ‘gate-first’ fabrication process where the operative metal gate is formed before the source and drain regions of the transistor.” Pet., 79. Despite this, the Petition argues that a POSITA would have been motivated to modify Lin’s gate first process to not use a gate first process, and instead use a gate-last process as disclosed in Brask. Pet., 79-80. This makes no sense, because a POSITA would have understood that a gate-first and gate-last process each have pros and cons. For example, as Petitioner’s expert admitted, the gate-first process beneficially is much simpler, results in “a perfect cell,” and has less restrictive design rules. EX2005-Lee-Dep, 76:10-78:17, 83:4-84:19. The Petition alleges that “[b]y the priority date of the ’384 patent, POSITAs would have understood that gate-first processes would expose the gate structure to the high activation anneal for the junctions thereby degrading performance of the transistor.” Pet., 80. But presumably, the inventors of Lin understood the tradeoffs associated with gate-first versus gate-last processing and specifically chose gate-first. Thus, it

is unclear why a POSITA would choose to contradict Lin's express disclosure of using a gate-first process to instead use the opposite gate-last process.

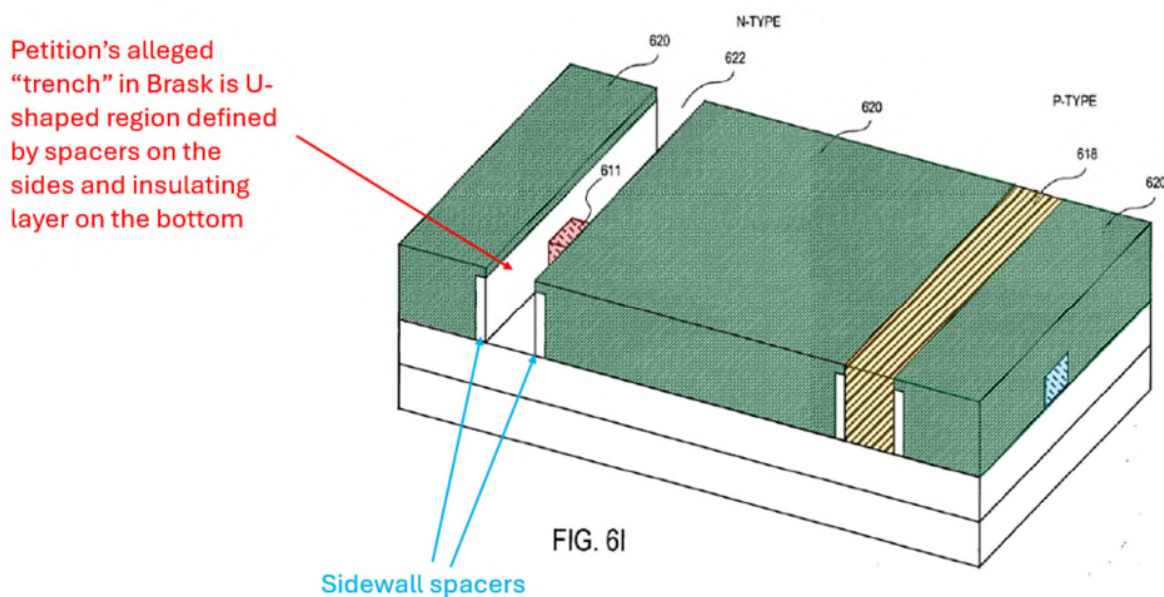
118. The Petition's argues that "by 2013, there was an industry-wide shift from gate first to gate last processing." Pet., 80 (internal quotations omitted). The Petition's logic appears to be that the inventors of Lin used gate-first because it was the prevailing technology at the time but that by 2013, once gate-last was developed, everyone had shifted to gate last and therefore a POSITA would have been motivated to modify Lin to instead use gate last. But this narrative does not hold up under closer inspection. Lin was filed by Petitioner TSMC on October 13, 2010, and specifically discloses only a gate-first process. EX1005-Lin at 1. Xu was filed by Petitioner TSMC less than a month later on November 2, 2010, and discloses both a gate-first and gate-last process. EX1004-Xu at 1. Thus, at the time of Lin's filing, TSMC clearly knew how to implement both gate-first and gate-last processes, and the inventors of Lin still specifically chose to use gate-first only. Moreover, Brask—the reference that the Petition alleges discloses the gate-last process that would be combined with Lin—was filed *nearly seven years before Lin* on December 30, 2003. EX1006-Brask at 1. Thus, the Petition's narrative that gate-last processing did not come about until after Lin was written makes no sense. Indeed, Petitioner's expert admitted that the inventors of Lin would have known about the gate-last

process, yet chose to implement gate-first in their design. EX2005-Lee-Dep at 84:22-86:14.

119. Moreover, even if a POSITA would have been motivated to modify Lin to use a gate-last process instead of a gate-first process, the Petition does not provide any rationale for why a POSITA would have chosen the specific gate-last process recited in claim 9. As explained above, a POSITA would have understood that a “gate last process” is a general term that encompasses varying procedures with different steps, including procedures that do not meet the specific steps recited in claims 4 and 9. For example, a POSITA would have known that not every gate-last process includes replacing a gate dielectric layer. In fact, Petitioner’s expert admitted that in some gate-last process sequences, a gate dielectric layer is deposited first, before putting down the dummy gate. EX2005-Lee-Dep, 72:16-73:3. In such a process sequence, during the gate replacement process, no gate dielectric layer is deposited in the trench. *Id.* Such a gate last process would not include “forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench,” as required by claim 9.

In fact, Petitioner’s expert admitted that “ideally, you don’t need the gate dielectric on the sidewall of the spacers” (EX2005-Lee-Dep, 71:24-72:12), *i.e.*, the sidewall of the alleged trench, indicating that a POSITA would **not** have been

motivated to “form[] a gate dielectric layer to conformally cover a sidewall and a bottom of the trench,” as required by claim 9 and admittedly not disclosed in Lin. As shown below, the Petition’s alleged “trench” in Brask is defined by sidewall spacers on the sides and an insulating layer on the bottom:

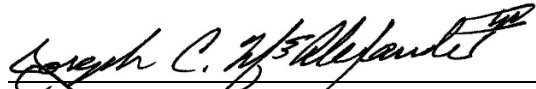


Pet., 86 (annotated EX1006-Brask Fig. 6I, further annotated here).

120. Element 9[c] recites: “forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench.” As Petitioner’s expert conceded, a POSITA would not have been motivated to form a gate dielectric layer to conformally cover a sidewall of the trench, as there is no reason to have the dielectric cover the sidewall. EX2005-Lee-Dep, 71:24-72:12.

121. Moreover, the Petition does not provide any rationale for why a POSITA would want to implement the specific process disclosed in Brask, instead only stating certain benefits that would apply to any gate last process. *See* Pet., 80-81 (stating benefits associated with a gate last process in general). For example, the Petition alleges that a gate last process enables tailoring of gate electrode work functions. *Id.* at 81. But this alleged benefit only applies to replacing a gate electrode, not a gate dielectric layer, as required by element 9[c]. Accordingly, the Petition's motivation to combine arguments fail to explain why a person of ordinary skill in the art would have combined elements from Lin and Brask in the way the claimed invention does.

Dated: March 5, 2026



Joseph C. McAlexander, III