UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-01265
U.S. Patent No. 8,993,384

PETITIONER'S REPLY

Table of Contents

Updated List of Petitioner Exhibits ii
INTRODUCTION 1
I. GROUNDS 1A AND 2A DISCLOSE AND/OR RENDER OBVIOUS FORMING AN ISOLATION STRUCTURE TO SURROUND THE FIN STRUCTURE 2
A. Marlin's "all four sides" requirement is illusory 3
B. Xu meets element 1[b] 6
1. Xu's "fin template" is irrelevant to 1[b] 7
C. Lin meets element 1[b] 8
II. GROUNDS 1A AND 2A DISCLOSE AND/OR RENDER OBVIOUS FORMING A RECESS IN THE FIN STRUCTURE AT A SIDE OF THE GATE STRUCTURE 10
III. GROUNDS 1A, 1B, AND 2B DISCLOSE AND/OR RENDER OBVIOUS CLAIMS 4 AND 9 14
A. Marlin fails to rebut claim 4's obviousness 14
B. Xu in view of the knowledge of a POSITA renders claim 9 obvious 14
C. Xu-Brask renders claim 9 obvious 17
D. Lin-Brask renders claim 9 obvious 19
IV. MARLIN'S REMAINING CHALLENGES ARE UNPERSUASIVE 20
A. Xu's embodiments are compatible and obvious to combine 20
B. The combination meets 1[g] 22
C. Xu meets 1[f] 23
D. Xu meets Claim 8 26
1. Xu discloses and/or renders obvious conformal deposition 26
2. Marlin's evidentiary attacks are meritless 28
V. CONCLUSION 29

Updated List of Petitioner Exhibits

Ex.	Description
1001	U.S. Patent No. 8,993,384 ("'384 patent").
1002	Prosecution History of U.S. Patent No. 8,993,384.
1003	Declaration of Dr. Jack Lee, Ph.D.
1004	U.S. Patent No. 9,166,022 B2 ("Xu").
1005	U.S. Patent 2012/0091538 A1 ("Lin").
1006	U.S. Patent Pub. No. 2005/0148137 A1 ("Brask").
1007	T. Ghani et al, *A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45 Nm Gate Length Strained Silicon CMOS Transistors*, IEEE International Electron Devices Meeting 2003, pp. 11.6.1-11.6.3 (2003).
1008	Excerpts from N. Collaert, *CMOS Nanoelectronics* (2012).
1009	A. Veloso et al., *Gate-Last vs. Gate-First Technology for aggressively scaled EOT Logic/RF CMOS*, Symposium on VLSI Technology – Digest of Technical Papers, pp. 34-35, (2011).
1010	M. Quirk and J. Serda, *Semiconductor Manufacturing Technology Instructor's Manual* (2001) (archived Sep. 28, 2007).
1011	Excerpts from S. P. Muraka et al., *Interlayer Dielectrics for Semiconductor Technologies* (2003).
1012	Excerpts from D. Neaman, *Semiconductor Physics and Devices* (2012).
1013	D. Hisamoto et al., *Folded-channel MOSFET for deep-sub-tenth micron era*, International Electron Devices Meeting 1998 – Technical Digest, pp. 1032-1034, (1998).
1014	X. Huang et al., *Sub 50-nm FinFET: PMOS*, International Electron Devices Meeting 1999 – Technical Digest, pp. 67-70, (1999).
1015	D. Hisamoto et al., *FinFET – a self-aligned double-gate MOSFET scalable to 20 nm*, IEEE Transactions on Electron Devices, Vol. 47, No. 12, pp. 2320-2325 (2000).
1016	J. Markoff, *Intel Increases Transistor Speed by Building Upward*, New York Times (2011).

1017	Intel, *Intel's Revolutionary 22 nm Transistor Technology* (2011).
1018	A. Shimpi, *Intel Announces first 22nm 3D Tri-Gate Transistors, Shipping in 2H 2011*, AnandTech (2011) (archived May 18, 2011).
1019	K. Mistry et al., *A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging*, 2007 IEEE International Electron Devices Meeting, pp. 247-250, (2007)
1020	U.S. Patent No. 7,525,160 B2 ("Kavalieros")
1021	S. Thompson et al., *Key Differences for Process-Induced Uniaxial vs. Substrate-Induced Biaxial Stressed Si and Ge Channel MOSFETs*, Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 221-224 (2004).
1022	C. Auth et al., *45nm High-k + Metal Gate Strain-Enhanced Transistors*, 2008 Symposium on VLSI Technology, pp. 128-129 (2008)
1023	S. Mayuzumi et al., High-Performance Metal/High-k n- and p-MOSFETs With Top-Cut Dual Stress liners Using Gate-Last Damascene Process on (100) Substrates, IEEE Transactions on Electron Devices, Vol. 56, No. 4, pp. 620-626, (2009)
1024	Excerpts from G. May and S. Sze, *Fundamentals of Semiconductor Fabrication* (2004).
1025	Excerpts from S. Wolf, *Microchip Manufacturing*, (2004).
1026	*Curriculum Vitae* of Dr. Jack Lee, Ph.D.
1027	Declaration of Stephen M. Bradley
1028-1100	Intentionally left blank
1101	Hsieh (U.S. Patent No. 8,735,553)
1102	Ching (U.S. Pub. No. 2014/0131776)
1103	Cho (U.S. Patent No. 8,853,037)
1104	Goto (U.S. Pub. No. 2014/0070328)
1105	van Dal (U.S. Pub. No. 2012/0319211)
1106	Liao (U.S. Patent No. 9,812,363)
1107	Chang (U.S. Patent No. 9,570,567)

1108	USPTO Class 257 Schedule
1109	USPTO Class 438 Definitions
1110	Xu-472 (U.S. Pub. No. 2012/0104472)
1111	TSMC Institution Decisions
1112	TSMC FWD Rate
1113	Baker (U.S. Patent No. 8,214,007)
1114	TSMC-Ansys Collaboration Press Release
1115	TSMC-Cadence Press Release
1116	’384 Patent Assignment to Marlin
1117	TSMC Technology Overview
1118	Intentionally Left Blank
1119	CNBC Transcript – US Commerce Secretary Howard Lutnick
1120	Removing Barriers to American Leadership in Artificial
1121	Another Historic Investment Secured Under President Trump
1122	Tsai (U.S. Patent No. 10,263,108)
1123	Zhang (U.S. Patent No. 9,653,605)
1124	Nasdaq – This 1 Number May Ensure TSMC’s Market Dominance
1125	TSMC’s Resurgence: What Lies Ahead for the Architect of AI
1126	Decoding TSMC’s Contribution to the AI and 5G Ecosystem
1127	TSMC Annual Report 2024 (Excerpts)
1128	Yahoo! Finance Article on TSMC Fab 21
1129	Prosecution History of U.S. Patent No. 9,812,363
1130	Prosecution History of U.S. Patent No. 9,570,567
1131	Prosecution History of U.S. Patent No. 10,263,108
1132-1200	Intentionally left blank
1201	Reply Declaration of Dr. Jack Lee
1202	IPR2026-00130, Paper-8, Patent Owner’s Preliminary Response
1203	IPR2026-00130, Paper-9, Notice of Decisions
1204	Transcript of May 14, 2026 Deposition of Joseph C. McAlexander

INTRODUCTION

Failing to identify material deficiencies in the prior art, Marlin takes a kitchen-sink approach, raising numerous unconvincing arguments in the hope that one might land. Each of Marlin's scattershot attempts lacks merit.

First, Marlin's challenges to claim element 1[b] rely on a contrived position that "surround" requires surrounding "on all four sides." Marlin's position is unsupported, contradicted by its own arguments and evidence, and fails to distinguish the prior art in any event. Marlin erroneously attacks the prior art figures for failing to meet its "all four sides" requirement, disregarding disclosures and evidence demonstrating that the prior art meets the claim even under Marlin's improper restriction.

Second, Marlin's challenges to claim element 1[e] import a limitation that has no basis in the claim language or the intrinsic record. Marlin injects a "horizontal" recess requirement into the claim language "forming a recess," then faults the prior art for not satisfying it. The specification and claims confirm that this requirement does not exist. Stripped of this nonexistent constraint, Marlin has no basis to contend Xu and Lin do not meet this element.

Third, claims 4 and 9 recite gate-last process steps that are well-known and conventional in FinFET fabrication. Yet Marlin argues these steps are non-obvious because "other types" of gate-last processing exist. Marlin's argument contravenes

well-settled Federal Circuit precedent and fails to engage with the motivations and rationales detailed in the Petition.

Fourth, Marlin's remaining quibbles with the Xu grounds lack merit. Its contention that Xu's embodiments are "incompatible" ignores the benefits of strain optimization that motivate the combination and fails to rebut Xu's suggestion of combining the embodiments altogether. Its challenge to 1[f] likewise disregards Xu's teachings and hinges on a strained and incorrect interpretation of the alleged recess, which is "fill[ed] up" by Xu's epitaxial layer in multiple ways. And Marlin's challenge to claim 8 further reveals its lack of familiarity with standard FinFET fabrication techniques and the state of the art. Conformal deposition and etching of insulation to form gate spacers were conventional at the relevant time and would have been obvious to those skilled in the art.

As explained below, Marlin's positions are unpersuasive and the Board should find the challenged claims unpatentable.

I. GROUNDS 1A AND 2A DISCLOSE AND/OR RENDER OBVIOUS FORMING AN ISOLATION STRUCTURE TO SURROUND THE FIN STRUCTURE

Relying on Figure 2 of the '384 Patent, Marlin's entire theory on 1[b] rests on the premise that the claim requires isolation structures to surround the fins "on all four sides." POR, 5-9, 34-40 (Xu), 65-66 (Lin). Marlin's position fails. As

explained below, Marlin's interpretation is not only incorrect, but does not distinguish the prior art even if it were right. *See* Ex. 1201, ¶¶10-33.

A. Marlin's "all four sides" requirement is illusory

Marlin (wrongly) faults Xu and Lin for not depicting isolation structures that surround the fin structures on "all four sides." POR, 34-40, 65-66. As Mr. McAlexander admits, however, Marlin bases this requirement on Figure 2's depiction of a "preferred embodiment." Ex. 1204, 74:3-75:13; Ex. 1001, 2:33-35. Reading this figure into the claims "is improper" as a matter of law. *Polaris Innovations Ltd. v. Brent*, 48 F.4th 1365, 1377 (Fed. Cir. 2022).

Marlin cites to the '384 Patent's disclosure that "a lower portion of each fin structure is embedded in the isolation structure 20" as supporting its position. POR, 5. Marlin is wrong. This passage merely contrasts the "lower portion of each fin structure," which is disposed within (*i.e.*, "embedded" in) the isolation structure, with upper portions that extend above the isolation structure to "a first height H1." Ex. 1001, 3:61-64. Both Xu and Lin employ this same configuration and therefore meet 1[b]:

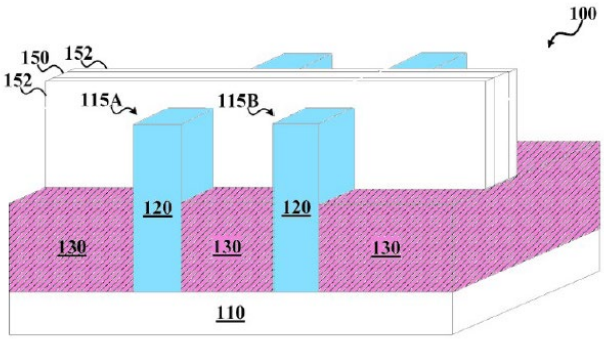


FIG. 2

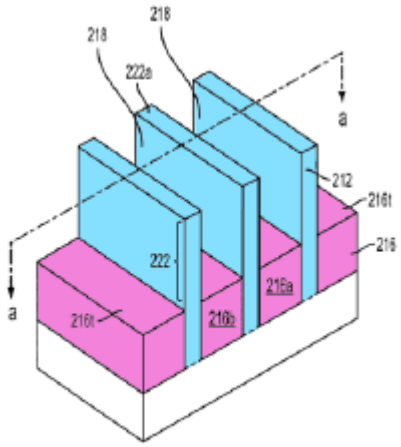


FIG. 6A

Pet., 17, 65.

And while Marlin defines "surround" as "enclose on all sides," Mr. McAlexander admits that the meaning of "surround" depends "on the context." Ex. 2006; Ex. 1204, 32:7-18.

Notably, in the context of the '384 Patent, Marlin and Mr. McAlexander repeatedly use "surround" in a manner inconsistent with Marlin's "all four sides" definition. POR, 19 (describing a gate as "surrounding the fin on the top and two sides"); Ex. 2007, ¶38 (same); Ex. 1204, 33:3-7 (describing a "semicircle of people" as "surrounding" a person). In particular, Marlin alleges "the isolation structure 20 fully surrounds the recesses 60" in the '384 patent figure below, yet only three sides of the recesses are surrounded in the figure:

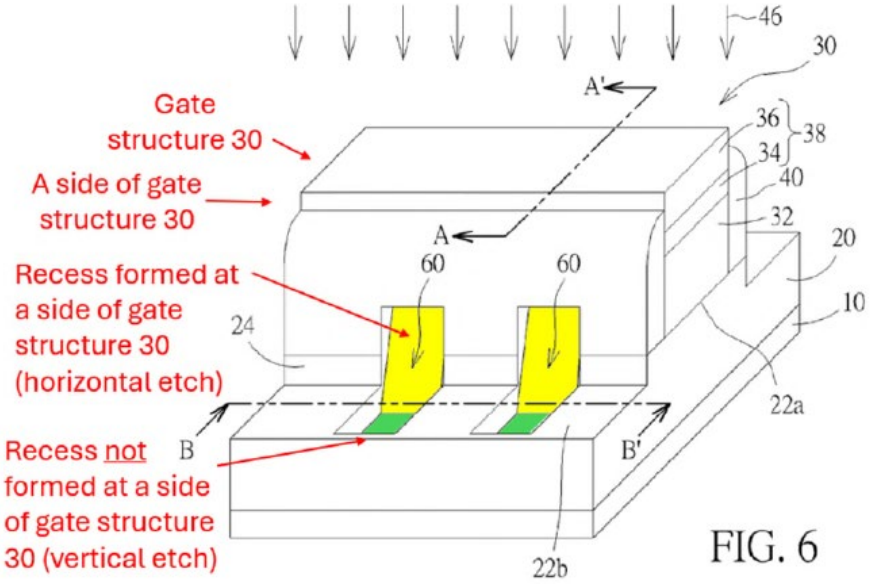


FIG. 6

POR, 30-31. This directly contradicts Marlin's "all four sides" requirement. Ex. 1201, ¶17. Moreover, Marlin's statement that the isolation structure "*fully* surrounds the fin structures on all four sides" (POR, 31)[1], equates its "all four sides" requirement with surrounding "fully." The claims do not include this qualifier (Ex. 1204, 33:25-34:2) and therefore do not require surrounding on all four sides. Ex. 1201, ¶17.

Dr. Lee and Mr. McAlexander agree that one structure may "surround" another on less than all sides. *Id.*, ¶18; Ex. 2007, ¶38. With this understanding, both Xu and Lin clearly disclose and/or render obvious 1[b], as set forth in the Petition. Pet., 17-18, 64-65. Regardless, Xu and Lin meet 1[b] even under Marlin's interpretation, as described below. *See* Ex. 1201, ¶¶19-33.

[1] All emphases added unless otherwise noted.

B. Xu meets element 1[b]

Marlin's lead argument asks the Board to find that Xu's disclosure does not disclose "forming an isolation structure to surround the fin structure." POR, 34-40.[2] Marlin's argument is a non-starter, however, because Xu *expressly* states that its "[i]solation features 130 … ***surround the fin structures*** 115A and 115B." Pet., 17-18; Ex. 1004, 3:54-56. Xu's use of the precise claim term—"surround"—to describe the claimed relationship between the isolation structure and the fin should end the inquiry. Ex. 1001, 8:30; Ex. 1004, 3:54. Notably, Marlin elsewhere acknowledges Xu's isolation structure as "the *surrounding* isolation structure." POR, 48.

Notwithstanding the express teachings in the text of Xu, Marlin argues that "Xu's usage of the term 'surround' is inconsistent with the claimed method," allegedly because Xu Figure 2 shows isolation features that "only cover two sides of each fin." POR, 37. This is factually and legally wrong.

First, Marlin invites error by attempting to limit the textual disclosure of Xu to just the simplified device of the figures. Xu discloses that its figures depict "various perspective views of a FinFET device [] ***in portion*** or entirety, at various stages of fabrication." Ex. 1004, 2:51-53; Pet., 10, 14. And Xu explains that STI

[2] Marlin unsuccessfully attempted this same argument at the pre-institution phase of a related proceeding. *Compare* POR, 34-40 *with* Ex. 1202, 23-29 (POPR presenting same arguments); Ex. 1203 (granting institution).

130 "isolate[s] the fins 120 from each other ***and other not-illustrated circuit*** devices." Ex. 1004, 3:56-58; Pet., 18. A POSITA would have understood Figure 2 as a cross-sectional view showing a "portion" of the isolation structure that "surround[s]" the fin structures. Ex. 1004, 2:51-53, 3:54-56; Ex. 1201, ¶21.

Additionally, Xu clarifies that "Figs. 2-6 have been *simplified* for the sake of clarity to better understand the inventive concepts of the present disclosure." *Id*., 2:57-59. Marlin's elevation of these simplified drawings over the detailed description in the specification is wrong as a matter of law. *See In re Andersen*, 743 F.2d 1578, 1581 (Fed. Cir. 1984) (a "*simplified* schematic" does not outweigh detailed teachings of the prior art) *overruled in-part on other grounds by In re Etter*, 756 F.2d 852, 858-59 (Fed. Cir. 1985).

1. Xu's "fin template" is irrelevant to 1[b]

Marlin's related argument that Xu fails to meet 1[b] because Xu's isolation structure does not surround the "fin template 135" (POR, 38-40) also fails. The claims expressly require "forming an isolation structure to surround the ***fin structure***." Ex. 1001, 8:30. Mirroring the claim language, the Petition asserts Xu's "fin structure[s]," not Xu's "fin template," as the claimed "fin structure." Pet., 16-18. As described above, Xu's STI "surround[s] the fin structures" as claimed. Ex. 1004, 3:54-55.

Undeterred, Marlin asserts that a POSITA would have understood that Xu's "'fin structure' includes both fins and fin template 135." POR, 39-40. The passage Marlin quotes in support refutes this understanding—"it is understood that ***'fin template' can refer to the newly grown epi semiconductor material alone*** … or the newly grown epi semiconductor material combined with the initial fins." Ex. 1004, 5:28-30. Without explanation, Marlin ignores the first option to fabricate a dispute based on the second. POR, 39-40. But even if the later-formed "fin template" could include the "fin structure," that does not mean the earlier-formed "fin structures" can encompass the "fin template," which does not exist when the fin structures and isolation structures are formed. Ex. 1201, ¶¶24-25.

C. Lin meets element 1[b]

Marlin deploys the same flawed strategy against Lin, relying on Lin's drawings to argue the isolation structure does not "surround" the fin structures. POR, 65-66. But Lin, like Xu, discloses that the depicted figures are merely "perspective and cross-sectional views" and "are *simplified* for a better understanding of the inventive concepts of the present disclosure." Ex. 1005, ¶¶14-15. Marlin's treatment of these "simplified" figures as complete representations of Lin's teachings is legally incorrect. *See In re Andersen*, 743 F.2d at 1581.

Lin's detailed description reveals Marlin's error. Lin discloses that some "processes may only be briefly described herein" and that the depicted FinFET "may

be included in a microprocessor, memory cell, and/or other integrated circuit." Ex. 1005, ¶14. A POSITA reading Lin would have understood the figures to depict a cross-section of the whole structure, which provides isolation from fin-to-fin (which alone meets the claim as described below) and from other integrated devices, such that the isolation structures extend around outer edges of each fin. Ex. 1201, ¶27. Indeed, Mr. McAlexander admits that FinFETs like Lin use "shallow trench isolation" to provide this very feature. Ex. 2007, 28:11-20, 77:25-79:3. As, the Petition and Dr. Lee explain, Lin's "isolation region[s]" are "shallow trench isolation." Pet., 74-75; Ex. 1003, ¶¶167-169. A POSITA therefore would have understood Lin's isolation regions to surround the fin structures as claimed. Ex. 1201, ¶¶27-28.

Marlin focuses on Lin's description of the fins as "between" the isolation structures to distinguish the reference. POR, 66. This description, however, is entirely consistent with the '384 Patent, which uses this exact same word to describe the isolation structure in relation to the fin structures. Ex. 1201, ¶30; Ex. 1001, 3:57-58 ("An isolation structure 10 is formed on the substrate ***between each fin structure 12***…).

Regardless, the Petition and Dr. Lee's unrebutted testimony explain why the claimed arrangement would have been obvious to a POSITA. Pet., 65; Ex. 1003,

¶151. Marlin fails entirely to address this point. POR, 65-66 (not addressing obviousness); Ex. 2007, ¶¶111-113 (same).

Notably, Marlin's own arguments demonstrate the obviousness of having the isolation structure surround the fin structure. Ex. 1201, ¶¶31-32. Specifically, Marlin submits that surrounding the fin structures "is important in order to fully isolate each fin structure, preventing unwanted contact and electrical interaction and thereby ensuring that each fin structure operates independently without interference." POR, 26; Ex. 2007, ¶54. This is exactly the reason why surrounding the fin structures with isolation material would have been obvious to a POSITA, and accords with Dr. Lee's declaration (Ex. 1003, ¶151). *See also* Ex. 1201, ¶¶32-33.

II. GROUNDS 1A AND 2A DISCLOSE AND/OR RENDER OBVIOUS FORMING A RECESS IN THE FIN STRUCTURE AT A SIDE OF THE GATE STRUCTURE

Inventing a new claim limitation, Marlin repeats its unpersuasive POPR contention that "the recess formed in the fin must extend at least in the horizontal direction in order to be a recess 'at a side of the gate structure.'" POR, 40, 66; POPR, 22, 31. Marlin's position is legally improper and runs contrary to the patent. This is not required by the claims, nor can Marlin articulate a cogent position on the scope of its non-existent limitation. Ex. 1204, 13:21-17:5.

Rather, Marlin reads this limitation into 1[e] based primarily on a figure from the '384 Patent. POR, 28-31, 41, 66-67; Ex. 1204, 18:3-24. But the '384 Patent

confirms that figures and related portions of the specification describe only a preferred embodiment. *E.g.*, Ex. 1001, 2:33-35, 3:10-12. Marlin's concocted "horizontal" recess requirement is inconsistent with the intrinsic record and legally improper. *Polaris*, 48 F.4th at 1377.

To support its improper restriction, Marlin bifurcates the '384 Patent's recess and argues "the yellow recess area was created 'at a side of the gate structure,' whereas the green part of the recess was not":

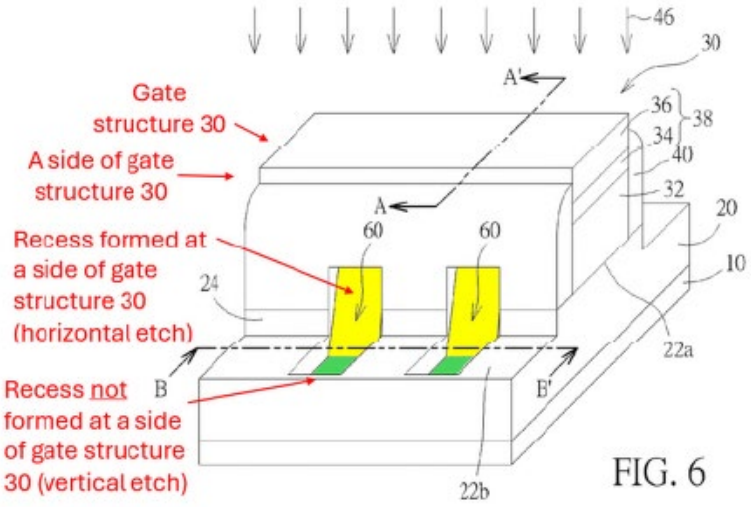


FIG. 6

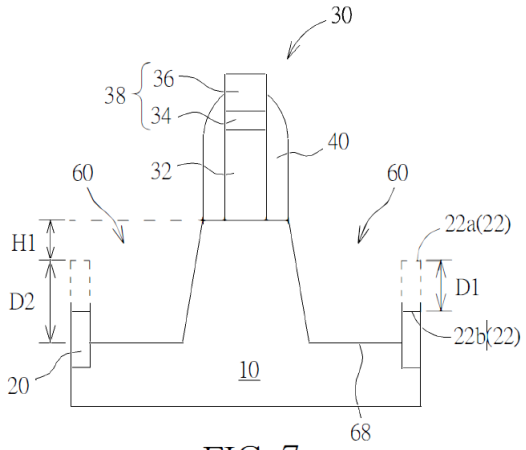
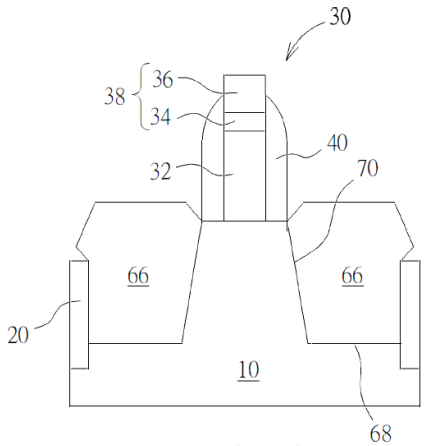
POR, 29-30. Marlin's sole support for doing so is a single passage Marlin claims: (1) "stat[es] that the etch extends horizontally" and (2) "ties together the concept of etching horizontally to the formation of the recess at a side of the gate structure." POR, 30-31. Neither conclusion is warranted.

In full context, this passage states:

> As shown in FIG. 6 to FIG. 8, a second etching process 46 is carried out to etch the fin structure 12 ***under*** the gate structure 30 and the

> spacers 40. After the etching process, a ***recess 60*** may be formed in each fin structure at ***at least one side of the gate structure*** 30. Furthermore, according to this embodiment, ***the ends of the fin structures*** 12 ***at two sides of the gate structure*** 30 may respectively have ***a recess 60***, and ***a bottom surface 68 of the recess*** is preferably ***shallower than a bottom surface of the isolation structure*** 20.

Ex. 1001, 5:55-64. Conspicuously, this does not state "the etch extends horizontally" nor describe any "horizontal" etching or extension. *Id*. To the extent Marlin reads "under" to require a "horizontal" etch, this is nonsensical. Ex. 1201, ¶36. To the contrary, "under" refers to etching down lower than the gate structure and the spacers such that a bottom surface of the recess is "shallower than a bottom surface of the isolation structure." Ex. 1001, 5:60-64; Ex. 1201, ¶36. This is confirmed by the '384 Patent's other figures (including FIG. 7, referenced in this passage) which fail to show any extension beyond the horizontal bounds of the spacers and gate:

'384 Patent, Fig. 7	**'384 Patent, Fig. 10**
 FIG. 7	 FIG. 10

Ex. 1201, ¶39. *See also* Ex. 1201, ¶¶37-38.

Fatally for Marlin, the full passage also expressly describes the "ends of the fin structures" and "bottom surfaces 68 of the recesses" as being "at two sides of the gate structure." Ex. 1001, 5:60-64. This is not an anomaly—the '384 Patent consistently uses the phrase "side[s] of the gate" to refer to the broader source/drain region of the transistor. *Id.*, 6:1-4, 6:29-34, 7:5-16, 8:1-4, 8:9-14. For example, the '384 Patent describes "the top surfaces 22b of the isolation structure ***at two sides of the gate structure***." *Id.*, 7:7-8. As Marlin's own figure shows, 22b (magenta) is located in the same region as Marlin's "green" recesses:

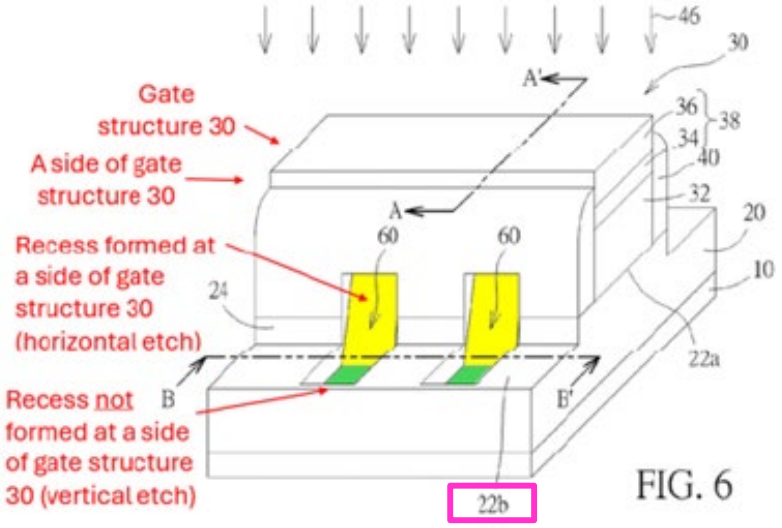


FIG. 6

POR, 29 (modified). The "green" recesses are therefore "at a side of the gate" as claimed, confirming Marlin's "horizontal" recess is not required. Ex. 1201, ¶40.

And because there is no horizontal recess requirement, both Xu and Lin meet this element as set forth in the Petition. Pet., 21-26, 69-72; Ex. 1201, ¶¶34-40.

III. GROUNDS 1A, 1B, AND 2B DISCLOSE AND/OR RENDER OBVIOUS CLAIMS 4 AND 9

Claims 4 and 9 require a "dummy gate" (claim 4) and various well-known, conventional gate-last process steps (claim 9) that were standard by 2013. Ex. 1201, ¶41. Marlin's contentions that these steps are nonetheless non-obvious are unpersuasive.

A. Marlin fails to rebut claim 4's obviousness

As a threshold matter, Marlin and Mr. McAlexander purport to challenge claims 4 and 9, but make no arguments specific to claim 4. POR, 58-64, 68-73; Ex. 2007, ¶¶18, 104-107, 109-110, 117-121. Even when challenging rationales for obviousness, Marlin's arguments are directed only to elements of claim 9.[3] Accordingly, the Petition's arguments and Dr. Lee's opinions that claim 4 is unpatentable remain unrebutted. Pet., 32-33, 50, 83. *See also* Ex. 1201, ¶¶41-43.

B. Xu in view of the knowledge of a POSITA renders claim 9 obvious

Xu specifically discloses using a "gate last process." Ex. 1004, 4:14. As the Petition explains, a POSITA would have understood and found obvious that Xu's disclosure refers to the steps set forth in claim 9. Pet., 38-42. This is particularly true where both the '384 Patent and Marlin's expert acknowledge that each of these

[3] To the extent any of Marlin's general challenges apply to claim 4, these arguments are not persuasive, as described below.

steps were well-known and therefore within the knowledge of a POSITA. Ex. 1001, 7:31-34; Ex. 1204, 66:22-25.

Marlin argues this is not so because only gate last processing "in general was known" and "not every gate-last process includes replacing a gate dielectric layer" as in 9[c]. POR, 59-60. Marlin misses the mark both as to a POSITA's knowledge and obviousness.

The '384 Patent describes a "high-k last replacement metal gate (RMG) process" comprising four specific steps. Ex. 1001, 7:21-29. It then states that "*the* RMG process"—meaning the particular process described and claimed—is "well-known to those skilled in the art." *Id*., 7:31-34. The patent's own inventors thus concede that the specific steps described and claimed were within the general knowledge of a POSITA. Ex. 1201, ¶¶45-46. Dr. Lee's declaration reinforces this understanding. Ex. 1003, ¶¶45-46, 108-110, 120-130.

Against this backdrop, the obviousness of claim 9 is straightforward. Dr. Lee confirms what the patent admits: each claimed step represents a well-known aspect of the "gate last" process described in Xu. Ex. 1201, ¶51. These steps are not merely "well-known" in the abstract, they are specifically known as steps of Xu's "gate last" process and would have been obvious to a POSITA as described in the Petition. Pet., 32-33, 38-42; Ex. 1003, ¶¶108-109, 120-130; Ex. 1201, ¶¶44-51.

Marlin's invocation of other types of gate-last processes as defeating the obviousness of element 9[c] fails for similar reasons. Ex. 1201, ¶47. That "not every gate-last process includes replacing a gate dielectric layer" (POR, 60) is immaterial where the specific claim step is known to a POSITA, as the '384 Patent admits. Ex. 1001, 7:27-28, 7:31-34. Moreover, the Petition explains it was known at the time that multi-gate FETs (like FinFETs) "require[] highly conformal deposition techniques for the … dielectric" (Pet., 41 (quoting Ex. 1008, 16)), highlighting the obviousness of 9[c] in light of this design requirement. Ex. 1201, ¶47.

The testimony Marlin cites does not compel a different conclusion. Dr. Lee did not "concede" that "there is no reason to have the dielectric cover the sidewall." POR, 61. Rather, Dr. Lee explained that whether this step is "need[ed]" depends on "the process sequence." Ex. 2005, 72:9-73:18. Dr. Lee clarified that known process sequences with high aspect ratios "need a CVD or ALD process so that you have a conformal deposition" resulting in "the dielectric on the bottom, as well as the sidewall of the spacers." Ex. 2005, 73:13-18.

If anything, Dr. Lee's testimony shows only that there are "simultaneous advantages and disadvantages" to different types of gate-last processing, but this does not "obviate motivation to combine." *Allied Erecting and Dismantling Co., Inc. v. Genesis Attachments, LLC*, 825 F.3d 1373, 1381 (Fed. Cir. 2016) (quotations omitted). *See also Novartis Pharms. Corp. v. W-Ward Pharms. Int'l Ltd*., 923 F.3d

1051, 1059 (Fed. Cir. 2019) (combination need not "be the preferred, or the most desirable, combination described in the prior art in order to provide motivation … it is thus improper to require [patent challenger] to prove that a [POSITA] would have selected [one option] over other prior art [options].").

C. Xu-Brask renders claim 9 obvious

Marlin does not dispute that Brask discloses every element of these claims. POR, 61-64. Instead, Marlin argues that it would not have been obvious to combine Xu and Brask because other types of gate-last processes exist. POR, 62. But Marlin ignores Brask's express recognition that its disclosed gate-last process "enables tuning of work functions such that performance of the transistor may be 'dramatically improved.'" Pet., 48 (citing Ex. 1006, ¶58). This express disclosure of motivation in Brask defeats Marlin's arguments.

Marlin follows with variations of the same flawed arguments it raises for Ground 1A, each time ignoring Brask's disclosures. Marlin again argues that "gate-last process" is a "general term" encompassing procedures that do not meet 9[c] and there is therefore no motivation to arrive at the claimed process. POR, 62-63. This is even more irrelevant here because Brask discloses the specific process at issue (Pet., 49-56), including 9[c] (*id*., 54), and motivates its combination with Xu (Pet., 47-50).

Marlin again misstates Dr. Lee's testimony to argue that Xu's disclosure of a "gate-last process is insufficient to motivate implementing" the step of 9[c]. POR, 63-64. But as explained above, Dr. Lee's acknowledgement of different types of gate-last processes is no concession and does nothing to obviate the obviousness of the claims. *See Allied Erecting*, 825 F.3d at 1381; *Novartis*, 923 F.3d at 1059. And Marlin fails to account for Brask's express disclosure of a process including the claim element and the Petition's numerous rationales for combining the references, including Brask's disclosure of advantages provided by this process. Pet., 47-50; Ex. 1006, ¶58.

Finally, Marlin argues the Petition relies only on "benefits that would apply to any gate-last process" rather than motivating Brask's specific process. POR, 64. This is incorrect. The Petition relies on the disclosed advantages of Brask's specific process and bolsters this with evidence demonstrating that these advantages were widely known at the relevant time. Pet., 47-49; Ex. 1006, ¶58. Even Mr. McAlexander agrees that the work function tunability resulting from Brask's method is beneficial. Ex. 1204, 68:3-6.

This is nothing like the "generic" motivations to build something "better" or "more efficient" that *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.* deemed "insufficient." 694 F.3d 1312, 1328 (Fed. Cir. 2012). Rather, the Petition explains "precisely how [(Pet., 49-55)] and why [(Pet., 47-50)] a skilled artisan would have

combined the references," thereby demonstrating obviousness. *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 797-98 (Fed. Cir. 2021).

In any event, a POSITA would have understood that Brask's high-temperature protection applies equally to the deposited high-k gate dielectric material. Ex. 1003, ¶¶44 (high-k dielectric material introduced after high-temperature processing), 45 (gate-last process advantageous as "sensitive materials are never exposed to damaging thermal steps"); Ex. 1201, ¶58. A POSITA therefore would have found applying this process to Xu obvious. Ex. 1201, ¶¶52-58.

D. Lin-Brask renders claim 9 obvious

Marlin's challenges to the Lin-Brask combination are equally unavailing. Marlin first argues using a gate-last process in Lin is non-obvious because there are "pros and cons" to gate-first and gate-last approaches. POR, 68-69. As described above, this is wrong as a matter of law—such tradeoffs do not obviate obviousness. *Allied Erecting*, 825 F.3d at 1381; *Novartis*, 923 F.3d at 1059.

Marlin's contention that the Lin inventors' knowledge of gate-last processing supports non-obviousness (POR, 69-70) fares no better. The point is simple: Lin discloses one approach; Brask discloses another with well-recognized advantages. Pet., 79-83. And by the time the '384 Patent was filed, the industry had largely adopted Brask's solution. *Id*., 80. A POSITA considering both references would

have found applying Brask's process to Lin obvious to achieve Brask's expected benefits. Ex. 1201, ¶60.

Moreover, Lin's awareness of gate-last processing merely confirms that both approaches were within a POSITA's knowledge—supporting, rather than defeating the obviousness of applying Brask's known technique to Lin's fabrication method which was ready for improvement. Pet., 81; Ex. 1003, ¶¶180-181.

Marlin follows with the same unconvincing arguments it raises for Grounds 1A and 1B. POR, 70-73. These arguments are unpersuasive and wrong for the reasons stated above. *See* Sections III.B, III.C, *supra*; Ex. 1201, ¶¶59-62.

IV. MARLIN'S REMAINING CHALLENGES ARE UNPERSUASIVE

A. Xu's embodiments are compatible and obvious to combine

Marlin first contends that Xu fails to disclose or render obvious "etching the isolation structure" and "forming a recess in the fin structure" because a POSITA would not combine Xu's first and second embodiments. POR, 42-48 (repeating POPR, 24-31). To the contrary, the Petition establishes that Xu motivates the combination by detailing advantages achieved by the second embodiment (*i.e.*, by controlling recess depth, channel strain "can be achieved and optimized" thereby "independently optimiz[ing] performance of each FinFET device") Pet., 23-24.

Marlin's sole challenge is that Xu's first embodiment introduces channel strain through a different method and therefore "does not benefit from" and "is

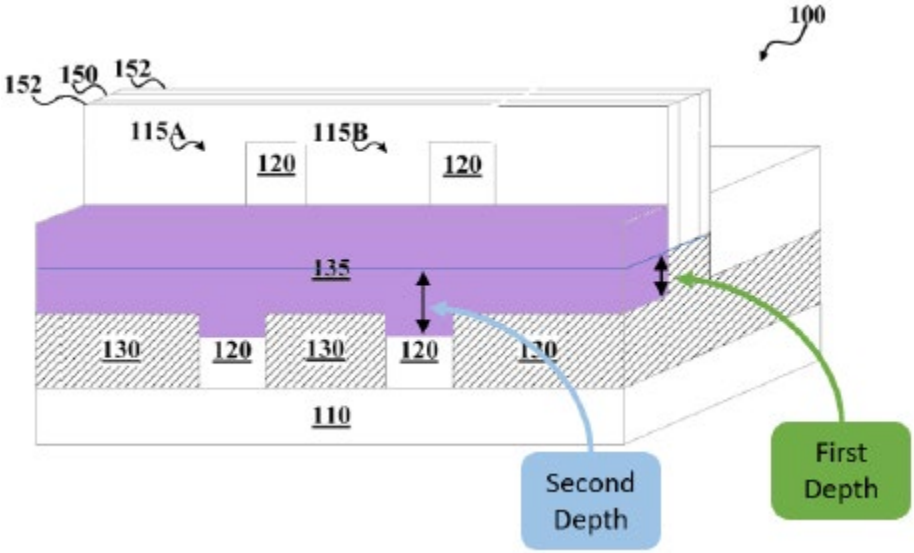
incompatible with" the proposed modification. POR, 46-48. Unsurprisingly, Marlin finds no evidentiary support for this position beyond a *verbatim* statement from Mr. McAlexander, who has no experience with strained transistor design. POR, 48 (citing Ex. 2007, ¶87); Ex. 1204, 88:15-17.

Marlin overlooks a key fact—through Xu's second embodiment, strain is not just achieved, but "optimized" by controlling source and drain depth. Ex. 1004, 15:56-16:2. As Dr. Lee explains, a POSITA "would have been familiar with the goal of imparting and *optimizing* strain … and would have found it obvious to apply [Xu's second embodiment to] Xu's first embodiment in order to *further tailor the strain*." Ex. 1003, ¶90. This expressly motivates the combination, which meets the claim as set forth in the Petition. Pet., 20-26; Ex. 1003, ¶¶84-95; Ex. 1201, ¶¶62-65.

Moreover, the Petition also explains that: (1) Xu's embodiments are not only compatible, but described as used together both in the specification and the claims (Pet., 24-26; Ex. 1003, ¶¶91, 95); and (2) the combination is an obvious application of a known technique (second embodiment) to a fabrication process ready for improvement (first embodiment) (Pet. 25; Ex. 1003, ¶94). Marlin does not rebut these positions. POR, 42-48, Ex. 2007, ¶¶79-87. These unrebutted arguments alone establish obviousness. Pet., 24-26. *See also* Ex. 1201, ¶¶66-67.

B. The combination meets 1[g]

Marlin next argues that it is "hindsight" to arrive at the claimed depth relationship from the combination of Xu's embodiments. POR, 48-49. As the Petition explains, however, Xu's second embodiment forms recesses that extend "to an exposed surface of the fin portion 220" having sidewalls "defined by … isolation features 240." Pet., 30. Combining Xu's embodiments therefore results in the claimed depth relationship, as shown in the figure below, depicting the combination:



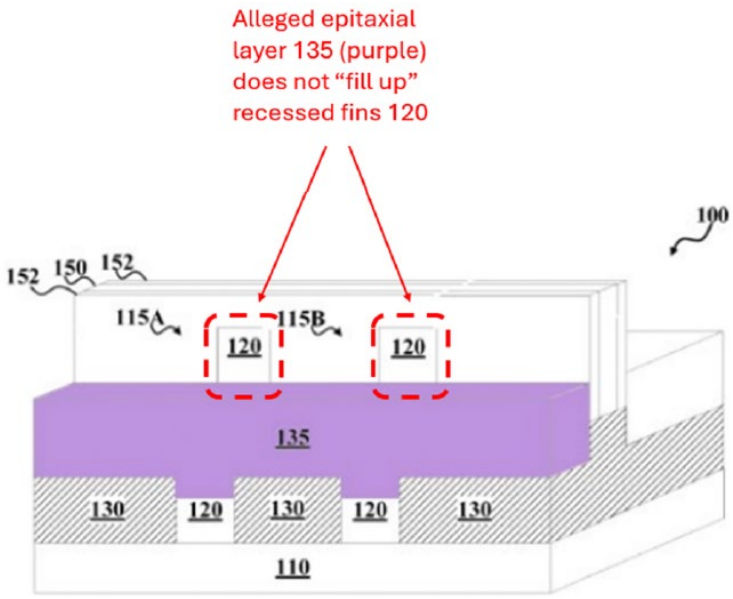
Pet., 31 (depicting Ex. 1004, Fig. 5 (modified)). Marlin argues "[t]here is nothing to suggest … one etch would go down further than the other." POR, 49.

Marlin's position is built upon a false premise—that Xu's second embodiment "etches a fin without concern as to the height of the surrounding isolation structure." *Id.*, 48. However, Xu's teachings directly concern isolation structure height, because Xu's strain optimization results from the depth of the source/drain regions. Pet., 23-

25. Xu's second embodiment achieves this by etching the fins below a top surface of the isolation structure. Pet., 22-23. The resultant depths are not based on hindsight, but a straightforward application of Xu's second embodiment to its first as set forth in the Petition. Pet., 22-26 (describing combination); Pet., 30 (describing structure resulting when combined "as discussed above"); Ex. 1201, ¶¶68-70.

C. Xu meets 1[f]

Referring to modified Figure 5 below, Marlin argues Xu does not satisfy 1[f] because Xu's "'fin template 135' does not fill up the recess, as the fin template does not extend to the top of the alleged recess":



POR, 49-52. Marlin's position contains multiple errors. *See* Ex. 1201, ¶¶70-83.

First, Marlin mischaracterizes the "alleged recess." Ex. 1201, ¶72. As Xu discloses, the recess sidewalls are "defined by … isolation features 240." Ex. 1004,

10:52-53. Mr. McAlexander agrees—conceding there is ***no recess*** formed in the upper portions of the fin (circled red) 120 and explaining that where "the top surface of 120 is lower than the top surface of 130" is what "defines the recess." Ex. 1204, 48:21-50:4, 52:20-53:5. Accordingly, the epitaxial layer need not cover exposed fin portions under the gate to "fill up" Xu's recess, which is defined by the isolation structures. Ex. 1201, ¶75.

Marlin also errs by overlooking Xu's relevant disclosures, which meet the claim in multiple ways, even under Marlin's incorrect interpretation. POR, 50-51; Ex. 1201, ¶77. First, Xu describes forming an epitaxial layer on "exposed portions of the fins" before etching the epitaxial layer to a final height. Pet., 28-29 (citing Ex. 1004, 5:1-2, 11:4-8). The Petition depicts this process with respect to Xu's first embodiment:

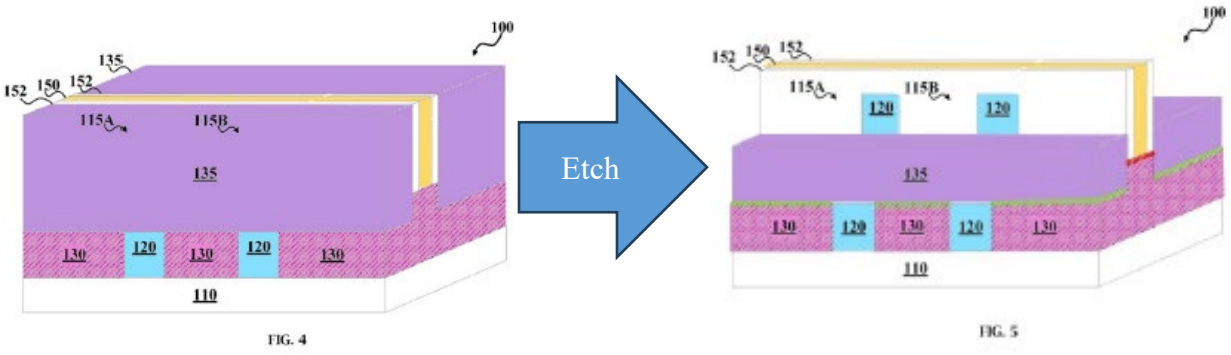


FIG. 4 FIG. 5

Pet., 12-13; Ex. 1201, ¶78. In Figure 4, the epitaxial layer is: (1) formed in the source drain region (Ex. 1004, 5:4-6); and (2) planarized (*id*., 5:26-28). In Figure 5, "an etching process is applied to etch back the fin template 135." *Id*., 5:35-36.

Xu's second embodiment uses a "process similar to that described" in Figure 5. Pet., 27; Ex. 1004, 11:2-4. A POSITA would have understood this to include the steps of forming, planarizing, and etching the epitaxial layer:

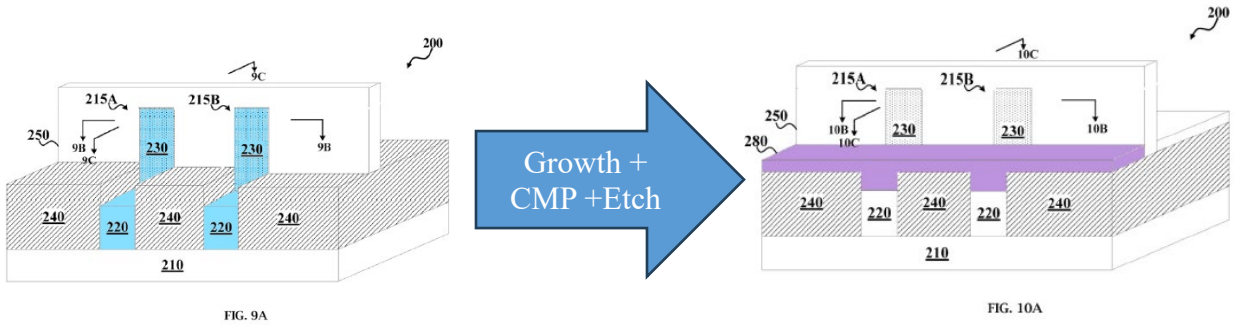


FIG. 9A FIG. 10A

Ex. 1201, ¶79. Prior to the final etching, Xu's "fin template" therefore "completely cover[s] the bottom surface [] and sidewalls [] of the corresponding recess," as Marlin argues is required. *Id*., ¶¶79-83; POR, 51. The claim language does not preclude subsequent processing of the epitaxial layer. Ex. 1001, 8:25-9:6.

Second, Xu's subsequent processing steps confirm that Xu's epitaxial layer meets the claim. After forming the fin template 135/280, Xu discloses that epitaxial semiconductor layer 160/285 is grown thereover to cover exposed sidewalls of the fin and complete the source/drain regions of the device:

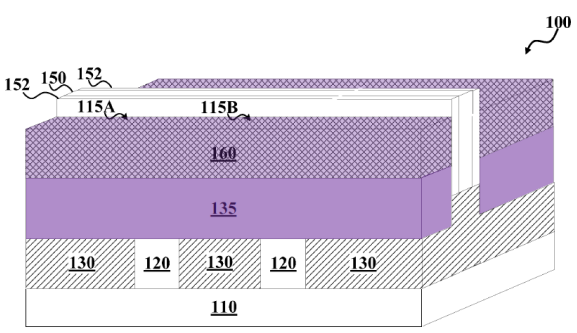


FIG. 6

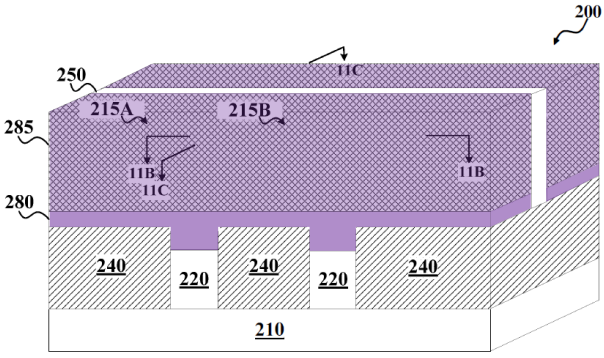


FIG. 11A

Ex. 1004, Fig. 6 (modified), Fig. 11A (modified); Ex. 1201, ¶84. *See also* Pet., 12; Ex. 1003, ¶¶57-59. Xu's epitaxial layer therefore meets 1[f], even under Marlin's interpretation. Ex. 1201, ¶84.

D. Xu meets Claim 8

Finally, Marlin argues that Xu fails to disclose or render obvious "depositing a material layer to *conformally* cover the gate structure and the fin structure." POR, 52-58. The evidence proves otherwise. *See* Ex. 1201, ¶¶85-90.

1. Xu discloses and/or renders obvious conformal deposition

Marlin argues the existence of other types of deposition processes somehow defeats both a POSITA's understanding of Xu's disclosure (POR, 53, 55-56) and the obviousness of using a conformal deposition (POR, 56-57). Both arguments are wrong.

Contrary to Marlin's assertions, a POSITA would have understood Xu's disclosure of "depositing a silicon nitride layer and then dry etching the layer to form the spacers" (Ex. 1004, 4:47-49) as referring to conventional spacer formation

processes that use conformal deposition followed by directional etching. Ex. 1003, ¶¶116-117; Ex. 1201, ¶87. As Dr. Lee testified at length, this technique has long been industry standard. Ex. 2005, 22:2-26:7. This conventionality is demonstrated by the prior art (Ex. 1005, ¶30; Ex. 1006, ¶53) and even the '384 Patent itself, which claims "depositing … conformally" while the specification merely discloses "[a] material layer is deposited … and then an etching process is performed to form the spacers 40" (Ex. 1001, 5:12-15). Marlin's reliance on other types of deposition fails to account for this state of the art, which reflects how a POSITA would understand Xu's disclosure. Ex. 1201, ¶¶87-88.

Regardless, as the Petition explains, depositing Xu's spacer material conformally at least would have been obvious for multiple reasons, including the beneficial coating of "all exposed surfaces uniformly." Pet., 36-37; Ex. 1003, ¶¶115-118. Marlin's arguments to the contrary make the same legal error as with claim 9. The "simultaneous advantages and disadvantages" of different deposition types do not detract from the obviousness of using a conformal deposition. *Allied Erecting*, 825 F.3d at 1381; *Novartis*, 923 F.3d at 1059. This is especially so here, where Marlin's own evidence establishes the advantages and desirability of conformal deposition. Ex. 2004, 2-5; Ex. 1204, 57:14-58:25. Indeed, Marlin's question of "why a POSITA would choose a conformal deposition technique" (POR, 56) is answered by its own exhibit which explains that conformal coating is recommended

for non-planar coating, such as depositing insulation over fin and gate structures. Ex. 2004, 5; Ex. 1201, ¶89.

The Petition separately establishes that substituting Xu's deposition with a conformal process would have been obvious. Pet., 37; Ex. 1003, ¶118. This is a straightforward application of *KSR*: "the simple substitution of one known element for another" is obvious. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007). Marlin does not rebut this argument, beyond casting the Petition as "conclusory." POR, 54. But the Petition's conclusion is supported by Dr. Lee's factual underpinnings, including that both "conformal … and non-conformal depositions … were known in the art" and "a POSITA could have substituted a conformal process into the method of Xu, yielding [] predictable results." Ex. 1003, ¶118. Notably, Mr. McAlexander agrees with these facts (Ex. 1204, 55:5-11, 59:1-60:12) confirming that conformal deposition would have been an obvious substitution. *KSR*, 550 U.S. at 417. *See also* Ex. 1201, ¶90.

2. Marlin's evidentiary attacks are meritless

Marlin further alleges that the Petition's claim 8 arguments lack support (POR, 53-54), but Marlin's case law is inapposite. Dr. Lee provides fact-based testimony, corroborated by Xu's teachings and a scientific textbook. Ex. 1003, ¶¶115-118. This is far different from the scenario in *Apple v. MPH Techs. Oy*, where

"there was no factual support underlying the expert testimony." 28 F.4th 254, 262 (Fed. Cir. 2022).

Finally, Marlin raises a perceived inconsistency—that a Table labeled "PECVD-SILICON-NITRIDE" shows *hydrogenated* silicon nitride—to argue a POSITA would not find the exhibit relevant to Xu's disclosed deposition of "silicon nitride." POR, 57-58. This distinction is immaterial. Skilled artisans would have understood that hydrogenation results from using PECVD to deposit silicon nitride. Ex. 1025, 296; Ex. 1201, ¶91. A POSITA would therefore understand PECVD-SiN as "depositing a silicon nitride layer" (Ex. 1004, 4:47-49) regardless of whether the resulting layer further contains hydrogen. Ex. 1201, ¶91. Moreover, the claim is directed to "depositing … conformally," not to any specific material or deposition process. Ex. 1001, 8:62-63. Exhibit 1025 establishes the conventional and advantageous nature of such depositions for silicon nitride (and other insulators), which a POSITA would have found obvious to use in Xu's method. Ex. 1025, 277, 296-299; Ex. 1201, ¶91.

V. CONCLUSION

For the reasons set forth above and in the Petition, the Board should find the challenged claims of U.S. Patent No. 8,993,384 unpatentable.

Dated: May 28, 2026

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing Petitioner's Reply was served on May 28, 2026 on counsel of record via electronic mail.

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CERTIFICATE OF WORD COUNT UNDER 37 C.F.R. § 42.24(d)

I, the undersigned, do hereby certify that the attached petition contains 5,594 words, as measured by the Word Count function of Microsoft Word, excluding this Certification and the following: Table of Contents, Table of Authorities, List of Exhibits, Mandatory Notices, and Certificate of Service. This is less than the limit of 5,600 words as specified by 37 C.F.R. § 42.24(c)(1).

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