

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD
3 -----
4

5 TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
6 Petitioner,
7 v.
8 MARLIN SEMICONDUCTOR LTD.,
9 Patent Owner.
10 -----

11 Case No. IPR2025-01265
12 U.S. Patent No. 8,993,384
13 -----
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15
16

17 DEPOSITION OF JOSEPH COLBY McALEXANDER, III
18 Conducted via Zoom
19 Thursday, May 14th, 2026
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24 REPORTED BY: GREG S. WEILAND, CSR, RDR, CRR
25 JOB NO.: 8049107

May 14th, 2026

10:03 a.m. Central Daylight Time

Deposition of JOSEPH COLBY

McALEXANDER, III, conducted via Zoom, taken before
GREG S. WEILAND, CSR, RDR, CRR, pursuant to the
applicable rules pertaining to the taking of
depositions, commencing at 10:03 o'clock a.m.
Central Daylight Time, on the 14th day of May, 2026.

1 PRESENT:

2
3 ON BEHALF OF THE PETITIONER:

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1 PRESENT (CONTINUED):

2
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May 14th, 2026

TESTIMONY OF JOSEPH COLBY McALEXANDER, III

PAGE

Examination by Mr. Sauer7

DEPOSITION EXHIBITS

NUMBER	DESCRIPTION	PAGE
Exhibit 1001	United States Patent 8,993,384	61
Exhibit 1004	United States Patent 9,166,022	39
Exhibit 1005	United States Patent Application Publication, US 2012/0091538	75
Exhibit 2003	Curriculum Vitae, Joseph C. McAlexander, III	81
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DEPOSITION EXHIBITS (CONTINUED)

NUMBER	DESCRIPTION	PAGE
Exhibit 2007	Second Declaration of Joseph C. McAlexander III Regarding Patent Owner's Response for Inter Partes Review of U.S. Patent No. 8,993,384	9

REPORTER'S NOTE: All quotations from exhibits are reflected in the manner in which they were read in the record and do not necessarily reflect exact quotes from the source documents nor necessarily match the punctuation.

1 (Witness sworn.)

2 JOSEPH COLBY McALEXANDER, III

3 after being first duly sworn, testified as follows:

4 EXAMINATION

5 BY MR. SAUER:

6 Q. Can you state your full name for the
7 record, please, sir.

8 A. Full name is Joseph Colby McAlexander,
9 III.

10 Q. And you understand you're under oath?

11 A. Yes, I do.

12 Q. Is there any reason that you couldn't
13 testify truthfully today?

14 A. No.

15 Q. And you said you have clean copies of the
16 exhibits in front of you?

17 A. Yes. I actually downloaded them
18 electronically, and I printed each one of them.

19 Q. Okay. So you have paper copies?

20 A. Yes, I do.

21 Q. Any other documents with you?

22 A. No, sir, none.

23 Q. Do you have a cell phone on?

24 A. It's on silent.

25 Q. Do you have any messaging apps running on

1 your cell phone or your computer?

2 A. Standard stuff, but I don't look at it.

3 Q. Okay. If you get a message, you know, and
4 you want to look at it, you need to let me know.

5 Okay?

6 A. I'll do that. But since it's on silent, I
7 won't hear it or see it, so I won't know it came in.

8 Q. Fair enough. You don't have any apps or
9 documents running on your computer other than your
10 conferencing app?

11 A. The conferencing app. I have
12 Windows Explorer so I can electronically look at the
13 documents.

14 Q. Okay. But there's nothing on
15 Windows Explorer now, just the prompt line, the
16 Google? Do you have any information --

17 A. When I say "Windows Explorer," I'm talking
18 about the local Explorer that you use on your
19 computer that gives you access to your computer
20 files. That's the thing that's running.

21 Q. Okay. Fair enough.

22 So I'm fighting a cold, so my voice might
23 get strained by the end of this. So if for some
24 reason you're having trouble understanding me,
25 please let me know.

1 A. That's okay. And if you want to quit
2 early, that's fine too.

3 Q. Let's try not to talk over each other, you
4 know, for the stenographer.

5 A. Agreed.

6 Q. All right. Can you pull out Exhibit 2007,
7 which should be a copy of your second declaration,
8 please.

9 (Exhibit 2007 was marked for
10 identification.)

11 BY MR. SAUER:

12 Q. Let me know when you've got it.

13 A. I have it.

14 Q. And for the record, this should be
15 Exhibit 2007, Marlin Exhibit 2007, which is the
16 second declaration of Joseph C. McAlexander, III.

17 Correct?

18 A. Correct.

19 Q. Did you review this declaration in
20 preparation for your deposition today, sir?

21 A. Yes, I did.

22 Q. And on the last page, is that your
23 signature?

24 A. Yes, dated March the 5th of 2026.

25 Q. Did you write this document?

1 A. I wrote it in coordination with the
2 attorney.

3 Q. I'm going to turn up my volume here just a
4 second.

5 Okay. Let me turn to Paragraph 19, which
6 is on Page 15, please.

7 A. Okay. I have it.

8 Q. Paragraph 19 lists or describes the
9 materials you considered in preparing your
10 declaration; is that correct?

11 A. Correct.

12 Q. Did you consider any materials other than
13 those that you reference in this paragraph?

14 A. I believe this covers the material I
15 reviewed.

16 Q. Have your opinions changed since you
17 signed this declaration?

18 A. No, they have not.

19 Q. Anything you'd like to correct?

20 A. Not that I'm aware of.

21 Q. Okay. If you'd turn to Page 2, please.
22 Are you there?

23 A. Yes, I am.

24 Q. In Section II here, starting on Page 2,
25 you provide an overview of your declaration

1 testimony; is that correct?

2 A. Yes, that's correct.

3 Q. Turn to Page 3, please. Sir, I want to
4 talk first about the overview that you provide here
5 in Paragraphs 5 and 6.

6 Can you just go ahead and read through
7 those by yourself to refresh your memory?

8 A. I've read 5 and 6.

9 Q. Okay. As you state here in Paragraph 5,
10 here in these paragraphs you're addressing claim
11 language that recites "a transistor fabrication
12 method in which a recess is formed in a fin
13 structure specifically at a side of the gate
14 structure"; is that correct?

15 A. Correct.

16 Q. And on Page 4, you have an annotated
17 version of Figure 6 of the '384 patent, right?

18 A. Correct.

19 Q. And this figure illustrates the recesses
20 formed in the fin structure, right?

21 A. That is correct.

22 Q. And the recesses are labeled 60; is that
23 right?

24 A. That is correct.

25 Q. Now, you've colored a portion of the

1 recess yellow and a portion green, right?

2 A. Correct.

3 Q. And then you have annotations here, and
4 the annotations indicate that the yellow-colored
5 portion is a recess that's formed at a side of the
6 gate structure 30 through a horizontal etch.

7 Is that your opinion?

8 A. Correct, yes.

9 Q. And then you have further annotation that
10 indicates that the green-colored portion is a recess
11 that is not formed at the side of the gate structure
12 but that's formed through a vertical etch; is that
13 correct?

14 A. That is correct.

15 Q. So to be clear, is it your opinion, then,
16 that the green-colored portion of the recess is not
17 located at the side of the gate structure? Is that
18 correct?

19 A. Well, in the etch process, I've defined
20 these two as vertical and horizontal.

21 Now, if, for instance, the yellow
22 horizontal was missing in the etch process, it was a
23 vertical etch, anisotropic etch, then that green
24 would only exist at the edge of the sidewall. It
25 would not go back under the sidewall to the gate.

1 The only way it gets back to the gate is because of
2 the horizontal etch on the yellow.

3 So in the end result, you're going to have
4 that lower portion all the way back at the gate, but
5 that's only because of the horizontal etch.

6 Q. So are you saying that the green portion
7 is created with no -- has no horizontal etch
8 component?

9 A. If I separate the two in terms of the
10 horizontal versus the vertical, a vertical etch
11 would only do that vertically and would use the edge
12 of the sidewall oxide as the edge, and so it would
13 only vertically etch from that point down.

14 The green -- at the end result, the
15 bottom, which is labeled green, does reach back up,
16 too, at the gate, but that's only because of the
17 horizontal etch.

18 And, therefore, you will have it extending
19 back, too, at the gate as a result of the horizontal
20 etch, if that makes sense.

21 Q. So I just want to make sure I understand
22 literally.

23 Is it purely a directional component,
24 then, in your mind? In order to be at the side of
25 the gate structure, it has to have a horizontal etch

1 component? Is that what you're saying?

2 A. Yeah, to be -- to be at the gate
3 structure, there has to be a horizontal etch
4 component because the area that's available for just
5 a vertical etch is only at the edge of the sidewall
6 oxide. There's no way to get back to the gate in
7 the direction of the gate unless you have a
8 horizontal etch.

9 Q. Well, I mean, are you saying that it has
10 to be touching the gate structure in order to be at
11 the side of the gate?

12 A. No, it doesn't have to be touching, but it
13 has to be at. And that means it cannot be away
14 from.

15 And in the typical processes that were
16 done that in the art was represented by this patent
17 was that there was not a horizontal piece to this
18 etch. There was a vertical, using just -- it's
19 standard anisotropic etch, so it's etching in the
20 single direction and it's straight down, vertical.

21 Q. What I'm trying to understand, though, is
22 how much horizontal etching is required in your
23 opinion.

24 Does it have to etch all the way to the
25 gate structure?

1 A. No, it doesn't -- excuse me. It
2 doesn't --

3 Q. Sorry. Go ahead. I interrupted. I'm
4 sorry. Can you start over?

5 A. Yeah, I'm not sure who was interrupting
6 who there.

7 There has to be a horizontal etch back
8 toward the gate structure. Now, the claim does not
9 specifically recite a particular amount or how far
10 away or how close or as to exactly at. There's not
11 any claim language limitation there.

12 But certainly there has to be a horizontal
13 etch in order to get the recess necessary to get
14 back toward the gate. Otherwise, the invention has
15 no purpose.

16 Q. So any amount of etching in the direction
17 of the gate structure would be sufficient, then, in
18 your opinion?

19 A. I don't know that I would characterize it
20 as "any amount" because that gets into the area
21 where there's no theory. There's no practical
22 aspect to it.

23 You can't give an exact number because the
24 distance or the dimension, the width of that
25 sidewall oxide, may be variant depending upon the

1 product that it's used in.

2 Secondly, that sidewall oxide may be a
3 multilayer sidewall rather than a single layer, and
4 the etching process may actually require using a
5 change in the etchant itself in order to get back
6 through there.

7 So it's an intentional etch in a
8 horizontal direction and an intentional etch in the
9 vertical direction. Both are required.

10 Q. Okay. So if there's any amount of
11 intentional etch in the direction of the gate
12 structure, would that be sufficient? I'm trying to
13 understand how much etching you need.

14 How close do you need to be in your mind
15 for it to be at the side of the gate?

16 A. Well, to be at -- I'm looking at right now
17 Exhibit 1001, the '384 patent.

18 Q. Sure. Hold on. Just a second.

19 Okay.

20 A. I think, you know, trying to quantify the
21 actual amount, that's not in the claim. Certainly
22 the amount is going to be dependent upon the actual
23 process. The amount that one would go back on a
24 10-nanometer process or a 5-nanometer or a
25 16-nanometer would be very different.

1 But the purpose of this is to get that
2 recess back toward the gate at the gate in such a
3 way that when you fell it with the epi you can then
4 change the strain component on the channel region
5 and the gate region.

6 Q. Let's talk about the process.

7 What type of etching process would you use
8 to do horizontal etching in the direction of the
9 gate?

10 A. It's really -- I would use a reactive-ion
11 type processing. And you can change the etchant
12 gas. You can change the temperature. You can
13 change the concentration. You can change the
14 source. You can change the power that's generated.
15 You can change the substrate voltage.

16 There's a lot of things you can do as
17 variations in the reactive type ion that you use.

18 Q. Is that a wet etching process or a dry
19 etching process?

20 A. Dry etching.

21 Q. So you would use a dry etching process to
22 provide a horizontal edge?

23 A. It would be -- it certainly would be a
24 preferred choice, yes.

25 Q. In your opinion -- if we can turn back to

1 your declaration on Page 4.

2 A. I'm there.

3 Q. Your opinion that the green recess, the
4 green portion of the recess is not at the side of
5 the gate structure, is based on what's shown in
6 Figure 6 of the '384 patent, right?

7 A. It's shown in Figure 6 with a note that
8 the recess not formed at the side of the gate is
9 based upon, in parenthesis, the vertical etch
10 component.

11 Q. But you developed this opinion and these
12 annotations based on Figure 6, correct?

13 Let me ask it this way.

14 Is there anything within the specification
15 of the '384 patent other than Figure 6 that supports
16 your interpretation that a recess at the side of the
17 gate structure requires a horizontal etch?

18 A. Well, I would say the references with
19 regard to Figure 6 through 8, in terms of the
20 process, but with regard to Figure 6 specifically,
21 the specification of column 5 supports that aspect
22 of etching back under the gate and so under the
23 sidewall oxide.

24 So the specification supports that.

25 Q. Is your interpretation based on your

1 understanding of the plain and ordinary meaning of a
2 side of the gate structure? Or are you giving it
3 some special meaning based on the patent?

4 A. I'm not giving it any special meaning.
5 The process is done in such a way that there is
6 etching, and the etching under the sidewall oxide is
7 literally in a horizontal direction.

8 And so the specification supports that.
9 There's nothing disconnected from what the spec
10 teaches versus what some person of skill in the art
11 would understand it to mean.

12 Q. Let's look back at Figure 6 here on
13 Page 4.

14 A. Okay.

15 Q. Would it be clear, as we're talking about
16 this, if I refer to the green-colored portion of the
17 recess as the vertical recess and then the yellow
18 portion as the horizontal recess? Which I
19 understand --

20 A. Yes, that's fine.

21 Q. So the vertical recess here, the green
22 portion in Figure 6, is located within what the
23 patent refers to as the isolation structure, which
24 is labeled 20 on here, right?

25 A. That is correct.

1 Q. And you can see one of the surfaces of the
2 isolation structure in Figure 6 is labeled 22b on
3 the top surfaces.

4 Do you see that?

5 A. Yes, I see that.

6 Q. Would you consider the surface that's
7 labeled 22b to be at a side of the gate structure?

8 A. The 22b is the part of the epitaxial layer
9 that has been etched down lower than the level of
10 the gate.

11 Q. I think 22b is referring to the surface of
12 the isolation structure 20, the top surface of it.

13 A. Yeah, excuse me. Sometimes that is
14 deposited by epi, but the isolation, the isolation
15 structure, that's fine.

16 The 22b represents the top surface of that
17 structure that's outside of the sidewall oxide.
18 That structure, the 22b, does not penetrate back at
19 the gate.

20 Q. So you would not consider that at the side
21 of the gate?

22 A. No. That's at the side of the sidewall
23 oxide.

24 Q. Turn to Page 5, please.

25 A. Okay.

1 Q. So at the top of Page 5 here, you have two
2 annotated drawings under the heading "Xu
3 (Ground 1)."

4 Do you see that?

5 A. Yes, I do.

6 Q. These are color-annotated versions of
7 Figures 8A and 9A of the Xu reference, right?

8 A. Yes, that's correct.

9 Q. And in the annotated version of Xu's
10 Figure 9A here on the right, you've colored the fins
11 blue, correct?

12 A. I did, yes.

13 Q. And this shows the fins after etching,
14 right?

15 A. Well, in Figure 9A, yes.

16 Q. In Figure 9A, yeah.

17 And in this annotated version of Figure 9,
18 you have an annotation here that points to the
19 recess that's formed by etching, and you indicate
20 there that the recess is created purely vertically,
21 not aside a gate structure, correct?

22 A. That's correct.

23 Q. So just to be clear, why in your opinion
24 is the recess in Xu not at the side of the gate
25 structure?

1 A. By the way, I'm looking at -- I'm looking
2 in Xu right now.

3 Q. Sure. Take your time.

4 A. The nature of the design is shown in more
5 detail in Figures 1 through 6. And when you get to
6 Figures 8 and 9, the specification clearly says at
7 Column 7, "Figures 8A through 8C, 9A through 9C, 10A
8 through 10C, and 11A through 11C have been
9 simplified for the sake of clarity."

10 So not all of what one would do in a
11 process such as is shown in Figures 1 through 6 is
12 represented in Figures 8 through the rest.

13 So this, as it's shown in Figure 9A, this
14 etching is back to that big bulk structure, but if
15 you look at the other Figures 1 through 6, it's
16 clear that it's not just a gate itself but there is
17 oxide, there is insulation around that gate as well.
18 And it would necessarily have to be. Otherwise,
19 you'd have a short.

20 Q. So you're saying there's something in
21 between the gate structure and the recess --

22 A. That is correct.

23 Q. -- in actuality?

24 A. That is correct.

25 Q. And is it your opinion, then, that Xu is

1 not at the side of the gate structure because
2 there's no intentional horizontal etching component?

3 A. That is correct, because if you looked at
4 the construct of Figures 8A through to 9A, there's
5 no -- there's nothing that says that any of this
6 etching is other than a vertical etch.

7 Q. I'm sorry. I'm having a little trouble
8 hearing you. It might just be me.

9 Are you able to hear him, okay, Greg?

10 THE STENOGRAPHER: Yes, I can hear him.

11 It's a little soft, but I can hear him.

12 THE WITNESS: I'll speak a little bit
13 louder.

14 BY MR. SAUER:

15 Q. That would be great.

16 So then would rue -- would rue -- would
17 Xu's recess be at the side of the gate structure if
18 it had an intentional etching component, in your
19 opinion?

20 A. If it had -- could you clarify "an
21 intentional etching component"?

22 Q. Right. If the etching that created what's
23 shown in Figure 9A also included a horizontal
24 etching component or a process that etched
25 intentionally horizontally instead of only

1 vertically, would then you consider it to be at the
2 side of the gate structure?

3 A. Well, there's nothing -- there's nothing
4 that I can see clearly that represents that, and so
5 there's not any intention.

6 If there was an intention, you'd see an
7 edge that goes back into that white structure, which
8 I've listed as the side of the alleged gate
9 structure, but there is none.

10 So there is no intentional because there's
11 no representation in the spec or in the figures that
12 such exist.

13 Q. But if there were, then you would consider
14 it to be at the side of the gate structure?

15 A. If there was intentional etching that goes
16 back through that sidewall oxide toward the gate, if
17 that is part of what is covered and suggested, then
18 that's something I would consider. But that's
19 certainly not what is shown.

20 Q. Okay. And then, similarly, here under the
21 heading Lin (Ground 2), you have annotated versions
22 of Figures 7A and 8A of Lin, correct?

23 A. Yes, sir, that's correct.

24 Q. And Figure 8A of Lin shows the fins after
25 etching, correct?

1 A. That is correct.

2 Q. And you've colored the fins blue here, the
3 etched fins blue?

4 A. That is correct.

5 Q. And here, again, your annotations indicate
6 that the recess formed by etching the fins is
7 created vertically, not at a side of the gate
8 structure, right?

9 A. Yes, that's correct.

10 Q. And for Lin, why in your opinion is the
11 recess not at the side of the gate structure?

12 A. There's no showing in Lin of any
13 intentional etching to take that fin back toward the
14 gate at all. It specifically -- the entire focus of
15 Lin is the mechanism by which you can form
16 multilayers of insulation that are tapered. That's
17 what Lin is directed to.

18 And so he has -- he has not given any
19 indication at all that there's any understanding of
20 trying to etch on a horizontal basis to go back in
21 toward the gate. He's literally talking about how
22 to form the fins and the organization of the fins
23 with regard to the insulation that is put alongside
24 of them, between them.

25 Q. So it's not at the side of the gate

1 structure, in your opinion, because there's purely
2 and only vertically etching; is that right?

3 A. That is all that is shown here. His
4 intent, again, was focused on the relationship
5 between the FinFET that is etched and the
6 insulation.

7 Q. Let's turn to Page 18, please.

8 A. I'm there.

9 Q. So here on 18, starting in section -- or
10 in Section V here, which starts on Page 18 of your
11 declaration, you provide a semiconductor transistor
12 technology primer, right?

13 A. Yes, that's correct.

14 Q. And then flipping ahead in this section to
15 Page 21, please.

16 A. I'm there.

17 Q. Here in Subsection B, you have a primer on
18 planar versus three-dimensional transistors, right?

19 A. That's correct.

20 Q. In the first paragraph, Paragraph 35, you
21 explain that integrated circuit chips in modern
22 computer systems are typically composed of millions
23 and even billions of transistors, right?

24 A. Correct.

25 Q. And then on the next page, Page 22, you

1 have a couple example illustrations of transistors.

2 The one on the left is a 2D planar
3 transistor built on a flat silicon substrate, and
4 then the one on the right is an example of a FinFET,
5 right?

6 A. That's correct.

7 Q. Where do these images come from?

8 A. Drawn from -- the source is intel. It's
9 just a document.

10 Q. From the internet or --

11 A. Yes, just internet, yes.

12 Q. What's highlighted in blue?

13 A. I could have drawn these from a lot of
14 different sources. I just picked the one on the
15 internet.

16 Q. So these are typical, commonly known
17 examples?

18 A. That's correct. They're just general
19 examples, block diagrams. They're not to any great
20 detail.

21 Q. Sure. And you've labeled them, but
22 looking at the FinFET, what's the blue layer? Is it
23 an isolation layer?

24 A. That would be an isolation layer, yes.

25 Q. And in the illustration, FinFET shows the

1 source in the drain regions of the fin right at the
2 edge of the structure, same with the gate.

3 So when you place this transistor in a
4 circuit next to other transistors or circuits in the
5 circuit layout, how would you typically isolate the
6 transistor to prevent shorts or interference?

7 A. How would I typically arrange or organize
8 this particular arrangement so that it doesn't
9 interfere with other circuits or other circuits
10 interfere with it? Is that your question?

11 Q. Right. You're saying there's millions and
12 billions of these in a transistor layout, and here,
13 in this example, you see that the edges of the fins
14 come right up against the diagram.

15 So how do you isolate that fin from other
16 circuits and fins?

17 A. Typically, you would use a different
18 isolation technique called shallow trench isolation.
19 So it's a separate exposure to a separate kind of
20 insulation. And that would be one way.

21 The older technology, which would have
22 been used back in the days of the planar transistor,
23 would use what's called a field oxide, and that
24 would be a grown oxide. Today, you'd use a shallow
25 trench most of the time where you actually create a

1 trench, an opening, and then you fill it,
2 epitaxially fill it with an insulation.

3 So it's a different insulator.

4 Q. Different insulator than what you colored
5 in blue? Is that what you mean?

6 A. Correct.

7 Q. And here in Paragraph 38 on this page, the
8 second sentence here, you state that, "In the
9 resulting fin field effect transistor, FinFET, the
10 source and drain regions are formed in opposing
11 regions of the fin, and the gate is wrapped over the
12 fin surrounding the fin on the top and two sides."

13 Right?

14 A. Yes, that's correct.

15 Q. So the gate surrounds the fin on three
16 sides?

17 A. The gate structure surrounds the fin on
18 three sides. Again, this is just a general diagram.

19 There are technologies within FinFET that
20 use what's called a double gate, which they use only
21 the sides and they insulate the top, and there are
22 other transistors that will actually use all three
23 sides.

24 Q. Let's flip ahead to Page 26.

25 A. Okay.

1 Q. Section VI is here starting on Page 26,
2 and in Section VI you describe the challenged '384
3 patent, right?

4 A. That is correct.

5 Q. A couple pages later on Page 28, are you
6 there?

7 A. Yes, I am.

8 Q. On Page 28 in Paragraph 54, you're
9 describing the structure that's shown in Figure 2 of
10 the '384 patent that you've copied here, right?

11 A. That is correct.

12 Q. Here you state, starting on the third line
13 that, "As clearly shown in Figure 2, the isolation
14 structure fully surrounds each side of the lower
15 portion of each fin structure. Forming the
16 isolation structure to fully surround the fin
17 structures in this manner is important in order to
18 fully isolate each fin structure."

19 Right?

20 A. That's correct.

21 Q. Can you explain what you mean by "fully
22 surrounds"?

23 A. Well, if you look, for instance, on
24 Page 29 at Figure 3, I color it in blue, and you can
25 see that that represents the top surface of that

1 insulation layer, but you can see for any given fin,
2 such as Number 14, the one that's labeled as 14-16,
3 if you look at that, you'll see that the blue
4 correspondingly surrounds that portion of the fin on
5 both to the left, the right, and in the front. And
6 the corresponding would occur at the other side of
7 the fin. You'd have the left, right, and rear, the
8 rear facing as you face into or away from the page.

9 So that's a color-coded version that
10 basically I think answers your question with regard
11 to Figure 2.

12 Q. So by "fully surround," you mean it
13 surrounds on four sides?

14 A. Yeah, because you've got the left and the
15 right, and you've got the front and the rear.

16 Q. To your mind, does "fully surround" mean
17 something different than just surround?

18 A. Those words depend upon the context of its
19 use. Sometimes "fully" means totally envelope. So
20 you have to look at the context.

21 Here, you obviously have a recess that
22 occurs, and so it's not totally encompassing all of
23 the fin. But in terms of the level to which you
24 have deposited or grown the particular insulation
25 layer, then the question is, all right, now if I

1 look at the FinFet, the fin itself as compared to
2 the insulation, what's the -- what's the take on how
3 that corresponds?

4 And so here, it's clear that you're
5 surrounding each one of those on both the left, the
6 right, front, and rear.

7 Q. So it depends on context what "surround"
8 means.

9 For example, earlier you used "surround"
10 to mean -- to describe a gate that surrounds three
11 sides. Here you're saying "surround" means fully
12 surround four sides.

13 So "surround" can have different meanings
14 depending on the context?

15 A. It can, and that's the reason why I made
16 that annotation in one of the prior references that
17 used the word "surround," but it had a different
18 meaning because of the different context.

19 Q. Is that the commonly understood meaning of
20 "surround" in your opinion?

21 A. It's what the commonly understood meaning
22 of "surround." The word "surround" is a -- is a
23 term that certainly has to be determined in terms of
24 its scope or its breadth within the context of its
25 use.

1 Q. But you're not giving it a special meaning
2 based on something in the patent?

3 A. No. For instance, if I was giving a
4 lecture and I had a semicircle of people that were
5 in front of me that are surrounding me, that's one
6 thing. They could be totally surrounding me. They
7 could be in the balconies up above.

8 I mean, there's different contexts of what
9 "surround" might mean based on its application and
10 its context.

11 Q. So here, you're determining what
12 "surround" means based on the context of how it's
13 used within the patent or based on what you see in
14 the diagrams of the patent?

15 A. Well, it's based upon looking at you're
16 reading the patent itself and allowing the patent to
17 give me some context, but the context is not
18 different than the plain ordinary meaning.

19 Q. But it's not based on anything in the
20 claim itself? It's based on what you've seen in the
21 specification of the patent, right?

22 A. I say I'm applying the plain ordinary
23 meaning based upon the context of the specification
24 of the patent itself.

25 Q. Sure. The claim doesn't say "fully

1 surround," right?

2 A. No, it does not use the word "fully."

3 Q. Well, let's look back at Page 28 here and
4 Paragraph 54.

5 A. Okay. I'm there.

6 Q. So the last sentence, you say, "Forming
7 the isolation structure to fully surround the fin
8 structures in this manner is important in order to
9 fully isolate each fin structure, preventing
10 unwanted contact and electrical interaction and
11 thereby ensuring that each fin structure operates
12 independently without interference."

13 Right?

14 A. Right.

15 Q. So am I understanding this, what you're
16 saying is that it's important to fully isolate each
17 fin structure to prevent unwanted contact and
18 electrical interaction? That's something that's
19 important in FinFet design?

20 A. I'd say when you look at the end
21 component, yes, that's important.

22 Now, you're going to get different layers
23 of this. For instance, you're going to -- the way
24 the fin is formed, you're going to have isolation
25 structures that correspond in a horizontal direction

1 making sure that any adjacent structures are
2 isolated or it's isolated from adjacent structures.

3 Now, there are going to be subsequent
4 process steps beyond the scope of these patents --
5 of this patent, rather, that goes vertical, the
6 integration when you start to run conductors or
7 capacitive structures that are sitting above it in a
8 multiplayer process. So, you know, there may be
9 other things that are also done in the process
10 before you finish the product.

11 But this particular aspect of surround is
12 based upon the particular insulation and the
13 particular FinFET at this stage.

14 Q. You don't cite anything in support of
15 this, right?

16 A. That's just standard processing.

17 Q. So the standard FinFET designer would
18 understand the importance of isolating the fin
19 structure to prevent unwanted contact and electrical
20 interaction?

21 A. In the general concept, yes.

22 And just to add to that, that way of
23 isolating, there are a number of different ways in
24 which that can be done, but the general context of
25 isolating, yes, that's correct.

1 Q. Still looking at Paragraph 54 here, you
2 include a quotation from the '384 patent the first
3 sentence of the paragraph.

4 Do you see that?

5 A. That's correct.

6 Q. And this portion of the specification is
7 the only portion of the patent specification that
8 you cite to here, right?

9 A. In this paragraph, that's correct.

10 Q. So the quotation says, "At this stage, a
11 lower portion of each fin structure 12 is embedded
12 in the isolation structure 20."

13 Right?

14 A. Correct.

15 Q. And you've highlighted the word
16 "embedded," correct?

17 A. I have.

18 Q. What's the significance of the word
19 "embedded" here? Why did you highlight that?

20 A. I highlighted it primarily because if you
21 take that particular sentence and then you look at
22 the figure, where it says Figure 2, it would add
23 clarity as to what the "embedded" is. It doesn't
24 mean it's totally enveloped by but embedded in. You
25 can see the lower portion, and I specifically refer

1 to that in Paragraph 54, that first sentence, "a
2 lower portion."

3 Q. So are you saying that the isolation
4 structure must fully surround the fins on all four
5 sides because they're embedded in the isolation
6 structure?

7 MR. LU: Object to form.

8 BY MR. SAUER:

9 Q. Go ahead.

10 A. No. I'm saying that in the context of
11 Figure 2, as described by the specification, that
12 it's talking -- the embedded aspect is only talking
13 about in this case the lower portion of the fin
14 structure 12. And so then you can see that the
15 isolation structure 20 does surround at that level,
16 at that lower portion.

17 So it's just -- it's just connecting the
18 dots between what is specified and what is shown in
19 the figure.

20 Q. Okay. Let's go to Page 36, please. Let
21 me know when you're there.

22 A. Okay. I'm there.

23 Q. In Section VII.A, it starts on Page 36,
24 you're addressing Grounds 1A and 1B of the petition,
25 right?

1 A. Yes, that's correct.

2 Q. And Grounds 1A and 1B relate to the Xu
3 reference, right?

4 A. Correct.

5 Q. And your first conclusion here under this
6 section is the heading 1a, which says that "Xu's
7 alleged isolation structure does not surround a
8 fin," correct?

9 A. That is correct.

10 Q. So Page 39 then, let me know when you're
11 there.

12 A. I have Page 39.

13 Q. Page 39, Paragraph 70, you state here --
14 I'm just going to read it -- "In contrast, Xu's
15 isolation features 130 do not surround the fin
16 structures as required by the challenged claims.
17 Although Xu states that isolation features 130
18 surround the fin structures 115 and 115B," you have
19 a citation, "a POSITA would have understood that
20 Xu's use of the term 'surround' is inconsistent with
21 the claimed method. That passage in Xu describes
22 Xu's Figure 2, which shows that isolation features
23 130 do not, in fact, surround the fin structures but
24 rather only cover two sides of each fin."

25 Right? Is that your opinion?

1 A. Yes, sir, that's correct.

2 Q. And then in Paragraph 70, so there's a
3 citation, here you cite to Xu at Column 3, Lines 54
4 to 56, right?

5 A. Yes, that's correct.

6 Q. Let's take a look at Xu, which is
7 Exhibit 1004.

8 (Exhibit 1004 was marked for
9 identification.)

10 BY MR. SAUER:

11 Q. Do you have that?

12 A. I have it, yes. I'm at Column 3.

13 Q. And you recognize -- you recognize
14 Exhibit 1004 as the Xu reference?

15 A. Yes, that's correct.

16 Q. And did you review the Xu reference in
17 preparation for your declaration?

18 A. I did.

19 Q. And do you consider yourself familiar with
20 Xu and its technology?

21 A. Yes.

22 Q. Okay. Let's look at Column 3 where you
23 cited it, Column 3 starting at Line 54, please.

24 A. Okay.

25 Q. So here, Xu states, "Isolation features

1 130, such as a shallow trench isolation, STI,
2 structures, surround the fin structures 115A and
3 115B in the depicted embodiment, the fins 120,
4 isolating the fins from each other and other
5 not-illustrated integrated circuit devices."

6 Right?

7 A. That's what it says, yes.

8 Q. And this is the portion of Xu that you
9 cited in your declaration, right?

10 A. That is correct.

11 Q. And this is referring to Figure 2 of Xu,
12 right?

13 A. That is referring to Figure 2, that is
14 correct.

15 Q. And as you acknowledged in your
16 declaration that we were just talking about, this
17 portion of Xu tells us that the isolation features
18 130 that are shown in Figure 2 surround the fin
19 structures 115 and 1 -- 115A and 115B, right?

20 A. Yes, sir, that's correct.

21 Q. What you don't mention in your declaration
22 is the sentence goes on to explain that the
23 isolation features 130 in Figure 2 are isolating the
24 fins 120 from each other and other not-illustrated
25 integrated circuit devices.

1 Do you see that?

2 A. I see that.

3 Q. So let's look at Figure 2 of Xu.

4 A. Okay. I have it.

5 Q. Figure 2, the isolation features are
6 labeled 130, right?

7 A. That is correct.

8 Q. The fins are labeled 120? Right, 120?

9 A. That's correct.

10 Q. As we were just discussing, the
11 specification tells us that the portion of isolation
12 feature 130 is isolating fins 120 from each other,
13 right?

14 A. Yes, that's correct.

15 Q. That's the portion of 130 that's between
16 the two fins, to be exact, right?

17 A. That is correct.

18 Q. And as we were just discussing also, the
19 specification of Xu also tells us that the isolation
20 features 130 isolates the fins from other
21 not-illustrated integrated circuit devices, correct?

22 A. Yes, that's correct.

23 Q. Doesn't this mean that the isolation
24 feature 130 here in Figure 2 would also extend
25 between the fins 120 and other devices that are

1 outside of the depicted structure?

2 A. It could be. It's not shown.

3 Q. It's not shown?

4 A. It's just a Xu statement. It could be
5 others that are outside. It could be others that
6 are partly inside.

7 Q. But it does tell us that it's this
8 isolation structure 130 that would extend between
9 these fins and those other devices, right?

10 MR. LU: Object to form.

11 THE WITNESS: It doesn't say that it will
12 extend between. It says that it would isolate
13 from.

14 BY MR. SAUER:

15 Q. Okay. But it's the isolation feature 130
16 that would be used to isolate these fins from other
17 not-depicted circuits and devices?

18 A. Again, it's a general statement. There's
19 nothing that supports what that is, where it is, or
20 anything about it.

21 Q. But you would agree that the isolation
22 structure 130 here could be used in that manner,
23 right?

24 A. It can be used in that manner, but there's
25 no specification as to what that is or how. It

1 could be used for isolating structures that are even
2 above. There's no -- there's no information here as
3 to what that is. It's a -- it's a conclusory
4 statement without any support as to how that would
5 be embodied.

6 Q. Well, it's not illustrated in the
7 drawings, right?

8 A. Nor anywhere in the specification.

9 Q. Well, let's look at Column 2.

10 A. Column 2 of Xu? Okay.

11 Q. Starting on Line 57, which is the middle
12 of the paragraph here, it says, "Figures 2 through 6
13 have been simplified for the sake of clarity to
14 better understand the inventive concepts of the
15 present disclosure. Additional features can be
16 added in the FinFET device 100, and some of the
17 features described below can be replaced or
18 eliminated in other embodiments of FinFET device
19 100."

20 Correct?

21 A. Correct.

22 Q. So Figure 2 is a simplified illustrative
23 drawing, right?

24 A. Yes, it's a simplified illustrated
25 drawing, and so you cannot draw any conclusions to

1 how else that would be used or where it would be and
2 what it would be used. You can't draw any
3 conclusions from that.

4 Q. Right. But since it's simplified, that's
5 why it doesn't show all the circuit details, like
6 how the isolation features 130 would isolate those
7 fins from other integrated circuit devices, right?

8 A. Yeah. If you're saying there's no
9 enabling disclosure for how else it would be used,
10 the answer is yes.

11 MR. SAUER: Let's take a ten-minute break
12 so I can get another cup of tea.

13 (Whereupon, a recess was taken
14 from 10:59 a.m. to 11:12 a.m.)

15 MR. SAUER: Go back on the record, please.

16 BY MR. SAUER:

17 Q. All right. Welcome back.

18 Let's go back to your declaration. I'm on
19 Page 51.

20 A. Okay. I'm there.

21 Q. Subsection 5, starting here on Page 51 of
22 your declaration, you discuss your opinion that Xu
23 fails to disclose or render obvious forming an
24 epitaxial layer to fill up the recess, right?

25 A. Correct.

1 Q. And then in the first paragraph, 89, you
2 state that, "The petitioner alleges that Xu
3 discloses a recess in the fin structure at the side
4 of the gate structures as shown in Figures 8A and
5 9A."

6 Right?

7 A. That is correct.

8 Q. And then you included some more
9 color-annotated versions of Figures 8A and 9A of Xu
10 here on Page 51, right?

11 A. Yes, that's correct.

12 Q. And in the color-annotated version of
13 Figure 8A, the blue portions are the fin structures,
14 right?

15 A. Yes, that's correct.

16 Q. And then in the color-annotated version of
17 Figure 9A, the blue-colored portions are the fin
18 structures after etching, right?

19 A. Correct.

20 Q. Sorry. What did you say?

21 A. That is correct, yes.

22 Q. And then on the next page, you've got
23 another annotated figure. It's not labeled, but
24 this is an annotated version of Xu's Figure 5,
25 right?

1 You can verify that if you want.

2 A. Correct.

3 Q. And the purple portion here in this
4 annotation of Figure 5 is an epitaxial layer; is
5 that right?

6 A. It is, yes.

7 Q. And you conclude here in the annotations
8 that the alleged epitaxial layer 135, which is
9 purple, does not fill up recessed fins 120.

10 Right?

11 A. That is correct, the vertical portion of
12 that.

13 Q. Yeah. And you've circled the upper
14 portion of the recessed fins there?

15 A. That is correct.

16 Q. And these are the portions that extend
17 above the epitaxial layer in Figure 5, right?

18 A. That is correct.

19 Q. So looking back at the color-annotated
20 versions of Figures 8 and 9 on the previous page, as
21 we already discussed, it's your opinion that the
22 etching process that forms the recess shown in
23 Figure 9 of Xu is a purely vertical etch, right?

24 A. Correct, for the reasons we discussed
25 before.

1 Q. Yeah. So there's no horizontal etch, in
2 your opinion, going on here, right?

3 A. That is correct.

4 Q. So with no horizontal etch, the only
5 recess in Xu's Figure 9A would be the vertical
6 recess that goes through the isolation feature 240,
7 right?

8 A. You said the isolation feature 240?

9 Q. Yeah. Do you see 240 in Figure 9A?

10 A. Okay, in Figure 9A, yes, that's correct.
11 That would be the only isolation there, correct.

12 Q. The only recess is the vertical recess
13 that goes through that isolation feature 240?

14 A. That is correct.

15 Q. There's no horizontal recess?

16 A. That is correct.

17 Q. So then in Figure 9A, what defines the
18 recess? Isn't it the -- isn't it bounded by the
19 sides of the isolation feature 240?

20 A. The -- the recessed portion, which is the
21 lower part of 120 -- or 220 here, 220, yeah, lower
22 part of 220, they -- basically the 240 isolation is
23 shown between the different fin structures 220.

24 So one fin is isolated in the horizontal
25 direction from another fin.

1 Q. That's not my question.

2 My question is, what's the reason? You're
3 not giving a special meaning to the word "recess"
4 here, are you?

5 A. No, I mean, the 220 --

6 Q. Would you understand -- let me ask it -- a
7 recess, the common meaning of a recess to be a
8 hollow space that's defined within something?

9 A. That's -- that's okay, yeah.

10 Q. That's what Oxford says.

11 A. If Oxford said it, I must agree with you
12 then.

13 Q. Good enough for me, right.

14 So if a recess is a hollow space that's
15 defined within something, what defines the recess
16 here? Isn't it the sides of the isolation feature
17 240?

18 A. The sides of the isolation feature 240
19 that are around that recessed portion 220 on two
20 sides.

21 Q. Okay. Right. So looking back, then, at
22 your annotated version of Figure 5 on the next page,
23 if there's no horizontal etching in Xu, there's no
24 horizontal recess, how are the portions of the fins
25 120 that you've circled here part of a recess?

1 They're not within any hollow portion of anything.

2 A. Well, what that says is the recess --
3 there is no recess in that particular section, in
4 that particular area, because there's no horizontal.
5 But it uses the same number 120 for both the lower
6 and the side, the elevated portion as well as the
7 lower portion.

8 And so the only part of 120 that is
9 recessed, so therefore it's a 120 recess, is only
10 the vertical direction.

11 Q. But isn't the part of 120 that's recessed
12 the vertical direction filled up by the epitaxial
13 layer?

14 A. Well, eventually it's filled up, yes, by a
15 separate -- by a separate epitaxial layer.

16 Q. Well, no. It's filled up in this figure.
17 The recess, as you said, is the part that's bounded
18 by the isolation features 130.

19 That portion -- that recess is filled up
20 here, isn't it?

21 A. Well, I hope so. You're not going to
22 leave a hole in the integrated circuit. After you
23 create the recess, the vertical recess, so 120 now,
24 the top surface of the 120 is lower than the top
25 surface of 130. That defines the recess.

1 Subsequent processing, you're not going to
2 leave a hole in an integrated circuit. There may be
3 other things such as a separate epi 135 that's
4 deposited.

5 Q. Right. So this epi 135 shown here fills
6 up the recess?

7 A. On the top only.

8 Q. It fills up the entire recess. The recess
9 is the portion, the hollow portion defined by the
10 structures 130, right?

11 A. Well, the hollow portion is -- the way in
12 which the hollow portion occurs is a vertical
13 etching of 120. 120, then, the top layer, the top
14 surface is lowered.

15 Q. Uh-huh.

16 A. The boundaries around the edges -- excuse
17 me, on the left and right of 120 here, is still 130.
18 130 bounds it on two sides.

19 But the only thing 135 does, when a
20 subsequent process fills in, it only touches the top
21 surface of 120. Yes, the recess itself will be
22 filled in. You don't leave voids in a circuit.

23 But that particular 135 is a separate
24 structure from the 130, and each one of them --
25 neither one of them surround on all sides the

1 fin 120.

2 Q. Okay. That's fair enough. But the
3 epitaxial layer 135 does fill in the vertical
4 recess, right?

5 A. Yeah, eventually that subsequent process,
6 the 135, will fill it in, sure. Again, you don't
7 want to leave voids in the structure.

8 Q. Okay.

9 A. But just to be clear, since you raised the
10 question, my annotation in Paragraph 90, I referred
11 to 120 as the recessed fins because a portion of
12 them, the vertical portion, is recessed.

13 Q. How is that vertical portion recessed if
14 there's no horizontal -- the portion you have
15 circled here in red is on the sidewall, right? And
16 you've said that there's no horizontal recess.
17 There's no recess within these red circles, is
18 there?

19 A. What I'm referring to is the part of 120
20 that was recessed by virtue of a vertical etch,
21 that -- which is the lower portion. That then
22 labels 120 as recessed.

23 Q. Well, now you're using "recessed" as a
24 verb. But a recess is, as you've acknowledged, is a
25 hollow opening in something, which isn't the

1 portions that are circled here in red.

2 It's the hollow portion that's defined by
3 the isolation structures 130 because of the etching,
4 right?

5 A. The fin 120 is recessed by etching of the
6 fin, not etching of 130. It's etching of the fin.

7 Q. Sure.

8 A. Okay. So --

9 Q. It's recessed to form a recess, you know,
10 at the bottom surface within that 130, right?

11 A. Yeah, you've got an opening or cavity or
12 whatever you want to call it within the 130 portion
13 because you have lowered the fin at that particular
14 place, that location, lower than the surface. So
15 that creates a recess.

16 So, therefore, the 120, that part of 120
17 has been recessed.

18 Q. I think we're in agreement.

19 A. It's not the --

20 Q. But there is no hollow portion formed
21 inside of these red circles, right?

22 A. The part -- again, 120 is a number that's
23 applied to both the vertical and the horizontal
24 portion of this particular fin.

25 So that portion that's in the red dashed

1 square that I have identified is a portion that has
2 not been etched.

3 Q. So there's no hollow recess formed?

4 A. There's no hollow there, no, none
5 whatsoever.

6 Q. We're in agreement. I'll move on.
7 Let's flip over a couple pages to Page 54,
8 please.

9 A. Okay.

10 Q. Excuse me just one second here.
11 Page 54. Here you have Subsection 6.
12 Do you see that starting on Page 54, where
13 you discuss your opinion that Xu fails to disclose
14 or render obvious claim 8, right?

15 A. Correct.

16 Q. Okay. Let's jump ahead two pages, 56, and
17 there's Paragraph 97 on that page.

18 Do you see that?

19 A. Yes, I do.

20 Q. Page 97, you conclude that the petition is
21 incorrect that Xu's spacer would inherently be
22 formed using a conformal coating, and that contrary
23 to the petition's allegations, a POSITA would have
24 understood that gate sidewall spacers could be
25 formed using non-conformal deposition/etching

1 techniques, such as chemical mechanical polishing,
2 CMP.

3 Correct?

4 A. You've correctly read that, yes.

5 Q. CMP is an etching technique, not a
6 deposition technique, right?

7 A. Well, the CMP process, it's rather
8 difficult to etch something that does not exist. So
9 the existing part is the deposition. So you deposit
10 material, and then you do a chemical mechanical
11 polishing etch to etch it back to a planar surface.

12 Q. But the deposition will be done through a
13 different process, right?

14 A. Yeah, the deposition is -- the deposition
15 will be done with a different process than the CMP
16 etch-back.

17 Q. What are some examples of non-conformal
18 deposition processes?

19 A. You can do non-conformal just in
20 variations of the parameters around the etching --
21 excuse me, the deposition process, even in a PECVD.
22 You can change the composition of the materials.
23 You can use one or more gases. You can use them in
24 a sublimation concept. You can use them in the full
25 gaseous state, the atomic type that you're using for

1 the bombardment to be the deposition, the
2 temperature of the substrate, a lot of variations
3 you can do to arbitrate whether something is or is
4 not conformal, even if it's PECVD.

5 Q. Is that commonly known? You don't cite
6 any evidence about the use of non-conformal
7 deposition techniques for sidewall spacers.

8 Is that something that you would say is
9 generally known?

10 A. Yeah, these types of deposition techniques
11 are known.

12 Q. Then in Paragraph 98, you conclude here
13 that a POSITA would have understood that, when
14 selecting a deposition technique, 1, conformality is
15 relative with certain deposition techniques
16 resulting in more or less conformality than others;
17 and, 2, there are tradeoffs between depositing a
18 material conformality [sic] and other critical
19 manufacturing metrics.

20 Right?

21 A. Yes.

22 Q. Sorry. I read that wrong.

23 "2, there are tradeoffs between depositing
24 a material conformally and other critical
25 manufacturing metrics," right?

1 A. Correct.

2 Q. And you cite here to Exhibit 2004 in
3 support of this conclusion, right?

4 A. Correct.

5 Q. Let's pull out Exhibit 2004, take a look
6 at it.

7 (Exhibit 2004 was marked for
8 identification.)

9 BY MR. SAUER:

10 Q. Let me know when you've got it.

11 A. I have it.

12 Q. Did you review this article when you
13 prepared for your declaration -- deposition?

14 A. I did.

15 Q. Did you review it in preparing your
16 declaration?

17 A. I did.

18 Q. Do you consider yourself familiar with the
19 article?

20 A. I do.

21 Q. Do you know when it was published?

22 A. I don't have the information here in front
23 of me, so I don't want to speculate on that.

24 Copyright -- let's see.

25 Q. It has the copyright on it of 2002 --

1 A. Yeah, I saw the copyright date on it.
2 It's way at the back.

3 If all of the rest of the related products
4 and stuff is a part of it, then that's probably the
5 best that we have.

6 Q. Probably around 2002? Would that make
7 sense?

8 A. It does make sense, yes.

9 Q. Let's turn to Page 2.

10 A. I believe that was shown on the last page,
11 Page 16 of 16.

12 Page 2?

13 Q. Yes. Let's look at Page 2 here.

14 You have -- in the third full paragraph
15 here, it says that poor step coverage is
16 non-conformal.

17 Do you see that? Do you agree with that?

18 A. This is on Page 2?

19 Q. Yes.

20 A. That's -- I would say that's generally
21 correct, yes.

22 Q. Page 3, the last paragraph, it goes on to
23 say that in semi conducting -- excuse me, "In
24 semiconductor manufacturing, a seemingly small
25 defect in step coverage can have catastrophic

1 consequences for the entire device."

2 Is that right? Do you agree with that?

3 A. Yes, that's correct.

4 Q. On Page 4, we have a heading here

5 "Maintaining Device Performance."

6 Here it states that, "Modern transistors,
7 like FinFETs, have complex 3D architectures. The
8 gate dielectric must wrap around the transformer's
9 fin with perfect uniformity."

10 Do you agree with that?

11 A. In a perfect world, yes.

12 Q. So it's not typical for --

13 A. Well, you hope that you have products that
14 will cross the way for defect-free, but the chances
15 are zero that that occurs.

16 Q. It's a design goal though?

17 A. That's a good design goal, yes.

18 Q. Okay. Then looking at the next paragraph,
19 do you agree that non-conformal deposition can cause
20 a void or keyhole inside the film?

21 A. That is correct. It can.

22 Q. And those voids are structural weak points
23 that compromise the mechanical integrity of the
24 device; is that right?

25 A. Yes, that's correct.

1 Q. All right. Let's go back to your
2 declaration, then, at Page 56 that we were looking
3 at.

4 In Paragraph 98, you have that article and
5 your citation to it.

6 Am I correct that your position is that
7 there are tradeoffs between conformal deposition
8 techniques and non-conformal deposition techniques?

9 A. Yes, there are, definitely.

10 Q. And were those tradeoffs known in 2013?

11 A. They were known in 2002.

12 Q. At least maybe 2002?

13 A. And even before that.

14 Q. So in the 2013 time frame, you would have
15 known how conformal versus non-conformal depositions
16 would impact the manufacturing process?

17 A. Yes, and they would maybe have different
18 impacts depending upon the process that you're
19 using.

20 Q. What do you mean by that?

21 A. Well, if you have a silicon germanium
22 process or silicon carbide process, you know, the
23 materials that you have that you're constructing and
24 how you're constructing them have a bearing on the
25 conformality or the non-conformality, so the

1 structures themselves, the processes themselves.

2 And as the article had stated, there are a
3 number of different variations, such as pressure,
4 temperature, precursor gas, and plasma power and
5 frequency, according to Page 3 of 16 of
6 Exhibit 2004.

7 Q. That would have been all --

8 A. All of these are variables.

9 Q. Those variables would have been all
10 well-known back in even in 2002 then, right?

11 A. It would be nice that some of them weren't
12 variable, but yes, they were known.

13 Q. All right. Let's move on then to Page 60.
14 Are you there?

15 A. I am there, yes.

16 Q. Here you have Subsection 7, now it starts
17 on this page, and you discuss your opinion that Xu
18 fails to disclose or render obvious claims 4 and 9.

19 Correct?

20 A. Yes, that's correct.

21 Q. On the next page, 61, it's Paragraph 105,
22 a big paragraph.

23 Do you see that?

24 A. I see it.

25 Q. So on, I think, the third line, the third

1 line, you state -- I'll read a little bit of it
2 here. "The petition points out that the '384 patent
3 states that the RMG process and the contact
4 formation process are well-known to those skilled in
5 the art. However, a POSITA would have understood
6 that while an RMG process in general was known at
7 the time of the '384 patent, claim 9 provides a
8 specific series of steps for replacing a dummy gate
9 structure."

10 Is that your opinion?

11 A. That is correct, yes.

12 Q. All right. Let's pull up the patent,
13 Exhibit 1001.

14 (Exhibit 1001 was marked for
15 identification.)

16 BY MR. SAUER:

17 Q. Turn to Column 7. Let me know when you're
18 there.

19 A. Okay. I have the patent, Column 7.

20 Q. Okay. Can you just read this paragraph
21 here starting at Line 21 of Column 7? It starts
22 "After the formation of the above epitaxial
23 structures."

24 Can you read that paragraph to yourself,
25 and let me know when you're done.

1 A. Certainly.

2 All right. I have read the paragraph
3 beginning Column 7, Line 19 to 20.

4 Q. So the paragraph first says that, "After
5 the formation of the above epitaxial structures, the
6 following semiconductor process may be optionally
7 carried out. For example, a high-k last replacement
8 metal gate, RMG, process may be carried out so that
9 the gate structure composed of polysilicon inside
10 may be replaced with a metal gate structure."

11 Right?

12 A. Correct.

13 Q. And then the patent goes on, and it says
14 that, "The RMC process may include the following
15 processes," and then it lists four numbered process
16 steps, right?

17 A. Correct.

18 Q. Take a look at those four numbered process
19 steps.

20 Those four numbered RMG process steps here
21 in this paragraph are identical to the steps that
22 are listed in claim 9; isn't that right?

23 A. I believe that's correct. Let me review
24 that.

25 Correct.

1 Q. So after the patent lists four RMG process
2 steps that are in claim 9 in this paragraph, at the
3 bottom of the same paragraph here, it states, "Since
4 the RMG process and the contact formation process
5 are well-known to those skilled in the art, the
6 detailed description of these is therefore omitted
7 for the sake of clarity."

8 Right? Is that what it says?

9 A. That's what it states, yes.

10 Q. So this sentence comes after and in the
11 same paragraph as the four numbered RMG process
12 steps in that claim 9, right?

13 A. That's the way it's organized, yes.

14 Q. So when the patent says the RMG process is
15 well-known to those skilled in the art, you'd
16 understand it to be referring to the RMG process
17 that's listed right above this in the same
18 paragraph, wouldn't you?

19 A. Yes and no. It is not specifically to
20 that because it says the RMG process. If you look,
21 generally speaking, the RMG process is known, there
22 are different ways in which RMG can be done.

23 But the RMG process is known, that's
24 correct.

25 Q. The RMG process was just described as

1 using those four steps, right? So as an ordinary
2 reader, wouldn't you understand it to be saying that
3 those four steps are known?

4 A. No. Well, those -- the RMG process would
5 be known. But if you go back to Line 24, it says
6 "the RMG process may include the following." It
7 doesn't have to. It may have other things.

8 So the statement that what is listed as
9 these four parameters is a part of the RMG process
10 that they're specifically focused on, but the RMG
11 process, not just those four, but the RMG process is
12 generally known.

13 Q. It says at least these four steps, so
14 maybe there's more steps.

15 But it's telling us that at least those
16 four steps are known, isn't it?

17 A. Well, I'm not discounting the fact that
18 those four steps are known. I'm just saying that
19 the RMG process and the contact formation process,
20 that's a statement of general consideration, and
21 that is true. They are known.

22 Q. Would you -- would you disagree that those
23 four steps were known at the time?

24 A. The RMG process itself in terms of
25 replacing an existing dummy gate with a metal gate,

1 those -- that process generally is known.

2 Q. Using those same steps?

3 A. No. It's just the general process is
4 known.

5 The statement here in this particular four
6 steps that they're talking about that are in the
7 claim requires -- where is it -- forming a gate
8 dielectric layer to conformally cover the sidewalls
9 and bottom of the trench.

10 Now, what that says in this particular
11 process, you are removing the dielectric layer that
12 was under the polygate, polysilicon being one of the
13 dummies.

14 Now, when you put a gate down, such as a
15 dielectric for a gate oxide or a gate dielectric,
16 that is done conformally, and it is also done at a
17 very high temperature so that you get a good
18 density.

19 Now, in this process, they're saying
20 you're putting down a dielectric that's going to be
21 at the base at the bottom of the trench, which is
22 going to be in the sides and the sidewall. Now that
23 new dielectric is going to be a part of the gate
24 dielectric, and yet you're having to put that down
25 at a significantly lower temperature, because if you

1 didn't, you'd melt all the previous structures or
2 you'd displace them or create voids or anomalies.

3 So this particular aspect is something
4 that, in combination, I don't think was known
5 precisely, no, not what is required here, because
6 typically --

7 Q. It doesn't --

8 A. -- the gate replacement process is going
9 to leave the dielectric layer there and remove the
10 polysilicon.

11 Q. It doesn't disclose any of those details
12 of that process that you just told me, does it?
13 Isn't that why it tells us that it's not listing out
14 the details of the process because they're
15 well-known?

16 A. I agree with your statement, but let's
17 qualify it. What that says is each one of these
18 particular aspects is generally known --

19 Q. Okay.

20 A. -- that this is a combination. It's
21 called an improvement claim. It's a combination.

22 Q. I see. So you're saying each of those
23 four steps individually were known but maybe not in
24 that particular order?

25 A. Correct.

1 Q. Okay. Let's go back to your declaration,
2 Page 63.

3 63, are you there?

4 A. I am on Page 63, yes.

5 Q. All right. We've got Subsection 8 here on
6 Page 63, starting on Page 63, where you discuss your
7 conclusions about Ground 1B failing, in your
8 opinion, to render obvious claims 4 and 9, right?

9 A. Correct.

10 Q. And then on the next page, you've got
11 Paragraph 110.

12 Do you see that?

13 A. Yes.

14 Q. Here, you conclude that the mere fact that
15 Xu discloses a gate last process is insufficient to
16 motivate implementing the specific gate last process
17 recited in claim 9.

18 Right?

19 A. Correct.

20 Q. And then towards the bottom of that same
21 paragraph, you state, "For example, the petition
22 alleges that the gate last process enables tuning of
23 gate electrode work functions, but this only applies
24 to replacing a gate electrode, not a gate dielectric
25 layer."

1 Right?

2 A. Yes.

3 Q. I want to explore that a bit.

4 Would you agree that work function
5 tunability is beneficial?

6 A. Yes, it is beneficial.

7 Q. And work function tunability helps to tune
8 the threshold voltage, right?

9 A. It has an impact on that, yes.

10 Q. Okay. Doesn't the gate dielectric
11 material also impact a transistor's threshold
12 voltage?

13 A. It does have a significant impact. That's
14 the reason that you usually put the gate dielectric
15 down early at a higher temperature so that it's more
16 conformal and it's very dense.

17 Q. Okay. Okay. So the only difference
18 between a transistor where the one had a silicon
19 dioxide gate dielectric and the other had a high-k
20 dielectric, the threshold voltage wouldn't be the
21 same in those transistors, right?

22 A. Well, it depends on how you adjust. There
23 are other parameters that go into creating the
24 threshold voltage, but that does have an impact.
25 But you can compensate with other ways in order to

1 even get to the same threshold voltage.

2 Q. Right. Because the gate dielectric is
3 affecting that voltage threshold?

4 A. Correct.

5 Q. So it's tuning the threshold voltage -- is
6 part of tuning the threshold voltage tuning the gate
7 dielectric, amongst other parameters?

8 A. Well, that is part of the choice, but the
9 gate dielectric has already been deposited prior to
10 the dummy polysilicon, so that has already been
11 taken into account. It's not a replacement gate
12 process on the dielectric.

13 Q. Okay. The choice of that gate dielectric
14 and its parameters are part of the process of
15 achieving the threshold voltage that you want at the
16 end of the entire --

17 A. It's a part of it, and it's something you
18 can't avoid. It is a necessary part of it. But
19 that is why you make the choice, and the better of
20 the options is to make that choice at the higher
21 temperature and lower in the level of the process so
22 that it's already done, it's already put in place.
23 And the only thing that you're replacing now in the
24 metal gate is the polysilicon. You remove the gate,
25 not the oxide, not the dielectric.

1 Q. So higher temperature, high-temperature
2 processing can affect the integrity of the gate
3 stack. Wouldn't you agree?

4 A. It does, yes. And if you tried to put in
5 a dielectric that was comparable to the original one
6 at the higher temperature, but you have to use lower
7 temperature, there are a lot of other parameters
8 that have to be taken into account to accomplish
9 that.

10 Q. So high-temperature processing could
11 affect the characteristics of a gate dielectric
12 layer?

13 A. Well, if you're doing -- I'm not sure
14 exactly where you're talking about. The
15 high-temperature process when you're originally
16 forming the gate dielectric under the dummy gate,
17 yes, it's a major factor.

18 Now, if you then subsequent to that start
19 depositing insulators, insulations, polysilicon, you
20 know, even if you replace the polysilicon gate in
21 this structure, in a circuit, polysilicon is also
22 used for connectors, for conductors, between
23 circuits.

24 And so you would not necessarily replace
25 all of those.

1 Now, if you're not replacing all of the
2 polysilicon on the chip, then you've got to consider
3 the fact that you cannot use a high temperature like
4 you put on the original dielectric. You have to use
5 a lower temperature. Otherwise, the temperature
6 will have a negative effect on the circuitry.

7 Q. Okay. Let's look at Lin. Let's go to the
8 next page, 65.

9 A. Okay. I'm there.

10 Q. Here, Section B, starting on this page,
11 you discuss your conclusions about Grounds A -- 2A
12 and 2B, right?

13 A. Yes, sir, that is correct.

14 Q. And those two Grounds 2A and 2B relate to
15 the Lin reference, right?

16 A. That is correct.

17 Q. And the first paragraph, Paragraph 111 of
18 this section, you state that, "The petition alleges
19 that Lin's insulation regions 216 (the claimed
20 insulation structure) surround fins 212 as shown in
21 Figure 6A and 6B."

22 Right?

23 A. Yes, that's correct.

24 Q. And let's look at the next page there on
25 Paragraph 113.

1 You conclude that, starting on the first
2 line, "a POSITA would have understood that in the
3 '384 patent's claimed fabrication method the
4 isolation structure is formed such that it surrounds
5 the fin structure on all four sides. In contrast,
6 Lin's insulation regions 216 only cover two sides of
7 the fins. This is apparent from the figures as well
8 as Lin's description of the insulation regions,
9 which describes a fin 212 between the first and
10 second insulation regions 216a and 216b."

11 Is that your opinion?

12 A. Yes, and the opinions that I've put in
13 here are consistent with what we've already
14 discussed on the Xu reference.

15 Q. Yeah, I just wanted to point out here
16 you've highlighted the word "between" here, right?

17 A. Yeah.

18 Q. Why did you highlight the word "between"?
19 What's the significance of that?

20 A. Well, the only showing is the insulation
21 that is interspersed from one -- between one fin to
22 the next fin to the next fin. That's the only thing
23 that has been described.

24 And that's why I'm saying -- it's on the
25 left and the right side, if you will, but that's the

1 only showing.

2 Q. Right. And it's your opinion that that
3 showing of the insulation between the fins is
4 something different than what's taught in the '384
5 patent?

6 A. Because the '384 patent, in that
7 terminology, that insulation is around four sides in
8 that particular part of the fin structure.

9 Q. Let's look at the terminology. Let's go
10 to the patent again, Exhibit 1001. Column 3,
11 please.

12 A. All right. '384 patent, Column 3.

13 Q. So at the bottom here, starting on
14 Line 55, there's a paragraph.

15 Do you see that?

16 A. Yes, I do.

17 Q. And here, the patent tells us, "Figure 2
18 is a schematic perspective diagram showing the
19 semiconductor device after the formation of a dummy
20 gate structure. An isolation structure 10" -- I
21 think that should be 20.

22 A. It should be 20, yes.

23 Q. "Is formed on the substrate 10 between
24 each fin structure 12 so as to electrically isolate
25 subsequently formed transistors from one another."

1 Did I read that right?

2 A. Yes, you did.

3 Q. Isn't that saying the same thing as Lin
4 about the location of the isolation structure
5 between the fins?

6 A. No, it's not saying the same thing because
7 it's what's referenced to Figure 2. Figure 2, you
8 can see it's all four sides.

9 So does it meet the requirement of
10 between? Yes, it does, but it's more than just
11 between.

12 Q. Based on your interpretation of Figure 2,
13 right?

14 A. Based upon what Figure 2 shows, that's
15 correct.

16 Q. But not based upon anything said here?
17 It's based upon your reading that in connection with
18 your interpretation of what you say is shown in
19 Figure 2, right?

20 A. Well, what is described in the patent
21 specification is a description of the figure. And
22 in this case, it's Figure 2, a schematic perspective
23 diagram of the semiconductor device after formation
24 of the dummy gate structure.

25 So the statement here says that it is

1 between. It is between. So it correctly describes
2 a part of what is shown in Figure 2.

3 Q. But it doesn't say anything about it
4 surrounding all four sides. That conclusion is
5 based on your interpretation of the figure, not the
6 specification description, right?

7 A. Well, the figure shows it on all four
8 sides. It's hard to say I'm interpreting it
9 differently from the spec. I mean, the spec
10 includes the diagram, and the diagram shows it on
11 all four sides.

12 Q. Okay. But it's based on the figure?

13 A. Based on the figure, yes, definitely.

14 Q. Excuse me for a second.

15 I can't shake this cold.

16 A. That's okay. You can move to Texas and
17 join us in the allergy season.

18 Q. It's not an allergy. Somebody gave me
19 something. I wish it was allergies.

20 Okay. Let's move on and look at Lin,
21 which we haven't looked at yet, which is
22 Exhibit 1005, I believe.

23 (Exhibit 1005 was marked for
24 identification.)

25 THE WITNESS: Okay. I have Exhibit 1005.

1 BY MR. SAUER:

2 Q. Are you familiar with Lin?

3 A. Yes.

4 Q. Let's go to Page 13.

5 A. All right. I'm at Page 13.

6 Q. Here there's a Paragraph 14 on this page.
7 Do you see that?

8 Why don't you just go ahead and read that
9 paragraph --

10 A. Yes.

11 Q. -- to yourself, please.

12 A. Yes, I see it.

13 Q. Go ahead and read that paragraph to
14 yourself.

15 A. Okay. I've read it.

16 Q. Okay. So at the end of that paragraph,
17 the bottom half of it, it says, "Figure 2 is a
18 schematic perspective diagram showing the
19 semiconductor device after the formation of a dummy
20 gate structure" -- wait. I'm sorry. I'm reading
21 the wrong thing.

22 A. I was going to ask you where are you
23 reading, please.

24 Q. Wrong quote. That was the quote from the
25 patent.

1 No. At the bottom of Paragraph 14,
2 towards the bottom, it says, here we go, "Also,
3 Figures 1 through 10C are simplified for a better
4 understanding of the inventive concepts of the
5 present disclosure. For example, although the
6 figures illustrate the FinFET 200, it is understood
7 the IC may comprise a number of other devices
8 comprising resistors, capacitors, inductors, fuses,
9 et cetera."

10 Do you see that?

11 A. Yes.

12 Q. So just like Xu that we talked about
13 earlier, Lin is telling us that its transistor
14 drawings are simplified, right?

15 A. Yes.

16 Q. And this includes Figure 6A and 6B that
17 you were addressing in your declaration?

18 A. That is correct. Any questions to this
19 that you would have asked on Xu, I would have the
20 same answer here.

21 Q. So also like Xu, Lin tells us that the
22 full IC would include other devices in addition to
23 the illustrated FinFET?

24 A. For a completed circuit, yeah.

25 Q. And wouldn't the POSITA then recognize

1 that the fins of the FinFET in Lin would also need
2 to be isolated from those devices and structures?

3 A. One would recognize that -- if you use the
4 FinFET technology, you would want to isolate those
5 from other structures, but there's no teaching here
6 as to how that was done. And it could be done by
7 other methods --

8 Q. Methods other than --
9 (Simultaneous speaking.)

10 A. -- such as a separate shallow trench
11 isolation.

12 Q. But it could also be done with the
13 isolation structure that's shown, right?

14 A. There's no teaching of how that would be
15 done.

16 Q. It's feasible?

17 A. An expert can do a lot of stuff, but to
18 the person of skill in the art relegated to what is
19 being taught by the specification, you can only go
20 with what the spec says. And the spec does not show
21 any teaching about anything other than what is shown
22 here, which is how to maintain isolation from one
23 FinFET structure to the next FinFET structure.

24 Q. But, again, the person skilled in the art
25 would know that you'd also want to maintain

1 isolation with the devices on a FinFET, right?

2 A. Which one would typically use an STI or
3 some other approach to make that isolation occur.

4 Q. Let's look at Figure 1.

5 A. Figure 1, okay.

6 Q. You've got it?

7 A. Okay. That's the chart, the flow diagram.

8 Q. Figure 1 shows the process flow diagram
9 for fabricating a FinFET, right?

10 A. That is correct.

11 Q. And the first step, providing a substrate,
12 right?

13 A. Yes.

14 Q. Step 102 is providing a substrate,
15 correct?

16 A. Yes.

17 Q. And the next step, 104, is forming a fin
18 in the substrate, right?

19 A. Right.

20 Q. And the third step labeled 106, is bigger.
21 It says, "Depositing a dielectric material over the
22 substrate and removing the top portion of the
23 dielectric layer to form first and second insulation
24 regions so that the top surfaces of the first and
25 second insulation regions are lower than the top

1 surface of the fin."

2 Right?

3 A. Correct.

4 Q. This dielectric material is the isolation
5 region? It says first and second insulation
6 regions.

7 Wouldn't Step 106 result in the fin being
8 embedded in the dielectric layer?

9 A. No, not necessarily, because they have not
10 in this general flow diagram, which the
11 specification says it is generally applied, but
12 there is more to it than just what's here. There's
13 no statements here as to how one uses masking or
14 double masking or any other thing to isolate
15 structure that you're then depositing this
16 particular insulation.

17 So no, there's no description of that at
18 all.

19 Q. Is the isolation in Lin STI?

20 A. So, therefore, it would not necessarily be
21 embedded, so to speak, on all sides.

22 Q. Is the isolation in Lin STI?

23 A. Is the isolation in STI?

24 Q. I'm sorry, I didn't hear.

25 A. Let's see. This would be 216.

1 I would say not STI. STI, you have to
2 form a trench first, and then you fill the trench.
3 This is etching back an insulator.

4 Q. We've been going another hour. I only
5 have a few more questions.

6 Do you want to plow on, or do you want to
7 take another break?

8 A. You can go forward. I'm okay.

9 Q. Let's just finish up then.

10 Let's look at -- let's pull out your CV,
11 Exhibit 2003.

12 (Exhibit 2003 was marked for
13 identification.)

14 THE WITNESS: Okay. I have it.

15 BY MR. SAUER:

16 Q. 2003 is your CV, right?

17 A. Yes, sir, that's correct.

18 Q. Is it up to date, more or less?

19 A. I like the "more or less" qualifier.

20 Thank you.

21 Q. Yes, it is more or less up to date?

22 A. Yes, it is, more or less.

23 Q. It was submitted in 2025, October of 2025.

24 Anything significant you want to update
25 since then?

1 A. Well, obviously I've added a number of
2 different cases since then.

3 Q. Any relevant experience that you'd want to
4 add?

5 A. Not in terms of -- I mean, I certainly
6 continue to do cases and have cases that are listed
7 here that deal with memory and the technology of
8 memory devices, and, of course, the technology today
9 that I'm dealing with is primarily FinFET.

10 I say the only other thing I would qualify
11 here, it's not directly mentioned because it
12 occurred long ago, but around 2016, I was actually
13 retained by a firm. At that time -- I don't think
14 they exist now, but it was Gerchen Keller, and I did
15 the preliminary analysis on the Lee patent that was
16 FinFET --

17 Q. Okay.

18 A. -- specifically, and that is something
19 that I did the analysis, evaluated the patent,
20 evaluated a number of different semiconductor
21 manufacturers. I did the analysis of the actual
22 products and provided them the information that
23 eventually that was acquired and licensed among a
24 number of different parties.

25 So I did not mention that directly because

1 it's, again, it's, what, eight years, ten years ago.

2 Q. Sure.

3 A. So I've had familiarity with FinFET.

4 Q. Page 11, starting on Page 11 and going on
5 for like 20 pages, you list all the cases that
6 you've been involved with an expert, as an expert,
7 right?

8 A. Yes, sir, that's correct.

9 Q. There's a lot of them.
10 About how many engagements would you say?
11 More than 100?

12 A. Well, I've only listed these in the past,
13 as I said on Page 11, the past seven years, and
14 these are only those that are public, trial,
15 hearing, deposition, or submitted declaration,
16 affidavit, a protective order, something that
17 memorialized it.

18 There are a number of cases beyond the
19 scope of this that I've been retained on that then
20 settled before it goes to any, so I have not done
21 any work on it.

22 Q. Over what period of time? Since when have
23 you been doing this?

24 A. My first venue into this was as an
25 inventor at the ITC defending one of my patents.

1 That was back in 1986.

2 Q. When did you get into expert witnessing
3 though?

4 A. Expert witnessing, I would say circa 1990.

5 Q. You've done quite a number of cases.
6 Do you typically represent the patent
7 owner or petitioner?

8 A. Overall, since 1990, it's been about
9 50/50.

10 Q. Okay. And these cases involve quite a
11 number of different fields of technology.

12 Would you agree?

13 A. Yes, that's correct.

14 Q. I'm just looking through the first
15 several. I see audio/video systems, telecom
16 systems, music jukebox here, video control systems,
17 smart thermostat. It goes on.

18 Would you consider yourself a person of
19 skill in the art for all of these technologies?

20 A. Yes. You know, it depends on the nature
21 of the actual patent itself. For instance, I have a
22 number of engagements in HVAC, but that's the
23 electronic control system. If you want to talk
24 about the actual Freon and that type of thing, no,
25 I'm not an expert on that.

1 But I started my company in 1988 around
2 audio/visual. I designed audio/video and visual
3 system and controls systems and still do.

4 I've also got a number of patents in the
5 Wi-Fi or wireless technology and a number of patents
6 that are used in integrated circuits, including GPS.

7 And so yes, yes, it's an expansive field,
8 but within those particular disciplines, as a
9 registered professional engineer, yes, I do have
10 expertise in them.

11 Q. Have you ever been excluded as an expert
12 in any litigations?

13 A. Never -- I've never been excluded, in
14 other words I could not testify, if that's what you
15 mean. It is -- it is almost -- the way it's
16 organized, the way it shapes out, in any litigation,
17 there are going to be certain parts of the
18 litigation that actually are excluded by the judge,
19 items that might have been relied upon that he is
20 now not allowing to go to the jury.

21 I mean, there's a lot of reasons why
22 certain parts of my potential testimony might be
23 excluded, but I've not been Dauberted.

24 Q. But not because of your qualification as
25 an expert?

1 A. I've never been Dauberted to a point where
2 I cannot testify.

3 Q. So you've never been excluded based on
4 your qualification as an expert is what you're
5 saying?

6 A. No, but I will qualify one area.

7 Q. Okay.

8 A. I mean, just to be up front about it.

9 Q. Sure.

10 A. I had a case a number of years ago. It
11 was a medical catheter case. And that was in the
12 Eastern District of Texas in Beaumont under
13 Judge Clark.

14 I had been retained to represent as an
15 expert the plaintiff in that matter, and I was
16 retained because the previous expert for some reason
17 no longer could continue. I think it was health
18 reasons.

19 So I was joined in late, and I did my
20 work, did the expert work, did the deposition expert
21 report. And then there was a filing to the court by
22 the opposing counsel to exclude me from having any
23 doctrine of equivalents arguments.

24 Q. Okay.

25 A. The judge agreed. Interestingly, I had no

1 DOE arguments in my report or in my deposition.

2 So you have to go look at the fine print
3 to reach a determination, but I've never been
4 excluded to testify.

5 Q. All right. Let's see. Let's look at
6 Page 7 here. You have your education profiled.

7 As part of this, it says you've taught
8 some courses here from 1980 through 1985, right?

9 A. That's correct.

10 Q. Did you ever teach a course on FinFET
11 technology?

12 A. No. No, I did not.

13 Q. Or semiconductor fabrication, more
14 generally?

15 A. Yes, definitely.

16 Q. What was that course?

17 A. Well, this was taught within the
18 companies. In this particular case, it was taught
19 within Texas Instruments to its engineers.

20 Q. Oh, okay.

21 A. And that was done both in Houston as well
22 as Dallas and as well as Singapore.

23 Q. So that was back when you worked at TI,
24 right?

25 A. That's correct.

1 I did continue after that to teach in the
2 other companies I worked with, but predominantly it
3 was within TI or their clients.

4 Q. During your time at TI and during the time
5 you were teaching that course, that was back before
6 1986, right?

7 A. That's correct.

8 Q. FinFETs didn't exist in 1986, right?

9 A. I'm certainly not aware of it.

10 Q. I didn't think so.

11 A. 2000 would be more of the time frame.

12 Q. Have you ever personally designed or
13 fabricated a FinFET?

14 A. No, sir, I have not.

15 Q. Have you ever personally been involved in
16 strained channel transistor design?

17 A. Not in the design, no.

18 Q. You were in the service?

19 A. Correct.

20 Q. Thank you for your service.

21 A. Thank you for recognizing it.

22 MR. SAUER: I don't have any further
23 questions. Pass the witness.

24 MR. LU: All right. Can we go off the
25 record real quick.

1 (Whereupon, a recess was taken
2 from 12:13 p.m. to 12:31 p.m.)

3 MR. LU: We're back on the record.

4 I have no questions at this time. We will
5 reserve the right to review and sign the
6 transcript.

7 Thanks, everyone.

8 (Whereupon, the deposition was
9 concluded at 12:31 p.m.)

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C E R T I F I C A T E

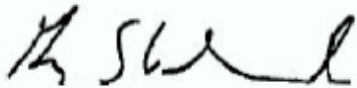
The within and foregoing deposition of the witness, JOSEPH COLBY ALEXANDER, III, conducted via Zoom, was taken before GREG S. WEILAND, CSR, RDR, CRR, commencing at 10:03 o'clock a.m. Central Daylight Time, on the 14th day of May, 2026.

The said witness was first duly sworn and was then examined upon oral interrogatories; the questions and answers were taken down in shorthand by the undersigned, acting as stenographer; and the within and foregoing is a true, accurate and complete record of all the questions asked of and answers made by the aforementioned witness at the time and place hereinabove referred to.

The signature of the witness was not waived and the deposition was submitted to the deponent as per copy of the attached letter.

The undersigned is not interested in the within case, nor of kin or counsel to any of the parties.

Witness my signature on this 15th day of
May, 2026.

A handwritten signature in black ink, appearing to read "G. S. Weiland", is written on a light blue rectangular background.

GREG S. WEILAND, CSR, RDR, CRR
License No. 084-003472

Veritext Legal Solutions
1100 Superior Ave
Suite 1820
Cleveland, Ohio 44114
Phone: 216-523-1313

May 15, 2026

To: Raymond Lu, Esq.

Case Name: Taiwan Semiconductor Manufacturing Company Ltd. v.
Marlin Semiconductor Ltd.

Veritext Reference Number: 8049107

Witness: Joseph Colby McAlexander, III

Deposition Date: 5/14/2026

Dear Sir/Madam:

Enclosed please find a deposition transcript. Please have the witness review the transcript and note any changes or corrections on the included errata sheet, indicating the page, line number, change, and the reason for the change. Have the witness' signature notarized and forward the completed page(s) back to us at the Production address shown above, or email to production-midwest@veritext.com.

If the errata is not returned within thirty days of your receipt of this letter, the reading and signing will be deemed waived.

Sincerely,
Production Department

NO NOTARY REQUIRED IN CA

DEPOSITION REVIEW
CERTIFICATION OF WITNESS

ASSIGNMENT REFERENCE NO: 8049107

CASE NAME: Taiwan Semiconductor Manufacturing
Company Ltd. v. Marlin Semiconductor Ltd.

DATE OF DEPOSITION: 5/14/2026

WITNESS' NAME: Joseph Colby McAlexander, III

In accordance with the Rules of Civil
Procedure, I have read the entire transcript of
my testimony or it has been read to me.

I have made no changes to the testimony
as transcribed by the court reporter.

Date Joseph Colby McAlexander, III

Sworn to and subscribed before me, a
Notary Public in and for the State and County,
the referenced witness did personally appear
and acknowledge that:

They have read the transcript;
They signed the foregoing Sworn
Statement; and
Their execution of this Statement is of
their free act and deed.

I have affixed my name and official seal
this _____ day of _____, 20____.

Notary Public

Commission Expiration Date

DEPOSITION REVIEW
CERTIFICATION OF WITNESS

ASSIGNMENT REFERENCE NO: 8049107

CASE NAME: Taiwan Semiconductor Manufacturing
Company Ltd. v. Marlin Semiconductor Ltd.

DATE OF DEPOSITION: 5/14/2026

WITNESS' NAME: Joseph Colby McAlexander, III

In accordance with the Rules of Civil
Procedure, I have read the entire transcript of
my testimony or it has been read to me.

I have listed my changes on the attached
Errata Sheet, listing page and line numbers as
well as the reason(s) for the change(s).

I request that these changes be entered
as part of the record of my testimony.

I have executed the Errata Sheet, as well
as this Certificate, and request and authorize
that both be appended to the transcript of my
testimony and be incorporated therein.

Date

Joseph Colby McAlexander, III

Sworn to and subscribed before me, a
Notary Public in and for the State and County,
the referenced witness did personally appear
and acknowledge that:

They have read the transcript;
They have listed all of their corrections
in the appended Errata Sheet;
They signed the foregoing Sworn
Statement; and
Their execution of this Statement is of
their free act and deed.

I have affixed my name and official seal
this _____ day of _____, 20____.

Notary Public

Commission Expiration Date

ERRATA SHEET
VERITEXT LEGAL SOLUTIONS MIDWEST
ASSIGNMENT NO: 8049107

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Date _____ Joseph Colby McAlexander, III
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DAY OF _____, 20_____ .

Notary Public

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Federal Rules of Civil Procedure

Rule 30

(e) Review By the Witness; Changes.

(1) Review; Statement of Changes. On request by the deponent or a party before the deposition is completed, the deponent must be allowed 30 days after being notified by the officer that the transcript or recording is available in which:

(A) to review the transcript or recording; and

(B) if there are changes in form or substance, to sign a statement listing the changes and the reasons for making them.

(2) Changes Indicated in the Officer's Certificate. The officer must note in the certificate prescribed by Rule 30(f)(1) whether a review was requested and, if so, must attach any changes the deponent makes during the 30-day period.

DISCLAIMER: THE FOREGOING FEDERAL PROCEDURE RULES ARE PROVIDED FOR INFORMATIONAL PURPOSES ONLY.

THE ABOVE RULES ARE CURRENT AS OF APRIL 1, 2019. PLEASE REFER TO THE APPLICABLE FEDERAL RULES OF CIVIL PROCEDURE FOR UP-TO-DATE INFORMATION.

VERITEXT LEGAL SOLUTIONS

COMPANY CERTIFICATE AND DISCLOSURE STATEMENT

Veritext Legal Solutions represents that the foregoing transcript is a true, correct and complete transcript of the colloquies, questions and answers as submitted by the court reporter. Veritext Legal Solutions further represents that the attached exhibits, if any, are true, correct and complete documents as submitted by the court reporter and/or attorneys in relation to this deposition and that the documents were processed in accordance with our litigation support and production standards.

Veritext Legal Solutions is committed to maintaining the confidentiality of client and witness information, in accordance with the regulations promulgated under the Health Insurance Portability and Accountability Act (HIPAA), as amended with respect to protected health information and the Gramm-Leach-Bliley Act, as amended, with respect to Personally Identifiable Information (PII). Physical transcripts and exhibits are managed under strict facility and personnel access controls. Electronic files of documents are stored in encrypted form and are transmitted in an encrypted

fashion to authenticated parties who are permitted to access the material. Our data is hosted in a Tier 4 SSAE 16 certified facility.

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Inquiries about Veritext Legal Solutions' confidentiality and security policies and practices should be directed to Veritext's Client Services Associates indicated on the cover of this document or at www.veritext.com.