

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,
Petitioner

v.

Marlin Semiconductor Ltd.,
Patent Owner

Case No. – IPR2025-01265
U.S. Patent No. 8,993,384

REPLY DECLARATION OF DR. JACK LEE IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO.
8,993,384

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I, Jack Lee, do hereby declare:

1. My name is Jack Lee. I am making this declaration at the request of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) in the matter of the *Inter Partes* Review of U.S. Patent No. 8,993,384 (“the ’384 Patent”).

2. I am being compensated for my work in this matter at my standard rate of \$680 per hour for such consulting services. My compensation does not depend in any way on the outcome of this proceeding.

3. I have reviewed Marlin’s Patent Owner Response (POR) and the declaration of Mr. Joseph McAlexander in support of Marlin’s POR. I have been asked to provide my responsive opinions.

I. Qualifications

4. My qualifications are set forth in my declaration provided along with the Petition for IPR, submitted as Ex. 1003.

II. Materials Reviewed

5. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field, and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the invention of the ’384 Patent.

6. In forming my opinions herein, I have reviewed and considered the Petition and all associated materials, Marlin’s Patent Owner Preliminary Response

(POPR) and accompanying materials, and Marlin's POR and accompanying materials. I have also reviewed the documents cited herein, including the deposition transcript of Mr. McAlexander.

III. Relevant Legal Standards

7. My understanding of the relevant legal standards is set forth in Ex. 1003.

IV. Person Of Ordinary Skill In The Art

8. My opinion regarding the level of a person of ordinary skill in the art is set forth in Ex. 1003.

V. Summary of Opinions

9. I have reviewed the Patent Owner's Response and Mr. McAlexander's accompanying declaration and disagree with a number of positions therein. I provide my responsive opinions below.

VI. Grounds 1A and 2A Disclose And/Or Render Obvious Forming an Isolation Structure To Surround The Fin Structure.

10. I have reviewed Marlin's arguments and Mr. McAlexander's opinions regarding claim element 1[b] and disagree with their contentions. In my opinion, Xu and Lin disclose and/or render obvious "forming an isolation structure to surround the fin structure."

A. "Surround" does not require surrounding on "all four sides"

11. I disagree with Marlin's contention that "surround" in the claim element requires that the isolation structure surround the fin structure on all four sides. POR,

5-9. I have reviewed the POR and Mr. McAlexander's declaration and deposition testimony and see inconsistencies between Marlin's position and their own use of the term.

12. First, Mr. McAlexander admits that his opinion on "surround" is based on what is shown in Fig. 2 of the '384 Patent. Ex. 1204, 74:3-75:13. I understand this figure and accompanying disclosure is describing a preferred embodiment. Ex. 1001, 2:33-35.

13. Marlin also cites to the '384 Patent's disclosure that "a lower portion of each fin structures is embedded in the isolation structure 20" to support its position. POR, 5. I disagree that a POSITA would understand this disclosure as meaning the isolation structure surrounds the fin structure "on all four sides." Rather, this passage uses "embedded" to distinguish the "lower portion of each fin structure," which is embedded in the isolation structure, from the upper portions that extend out of the isolation structure to "a first height H1." Ex. 1001, 3:61-64. Both Xu and Lin employ this same configuration and therefore meet the claim element, as shown below:

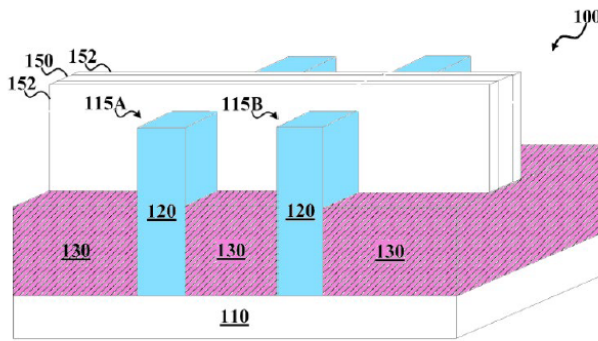


FIG. 2

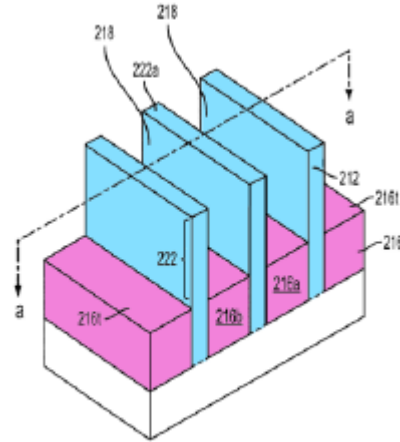
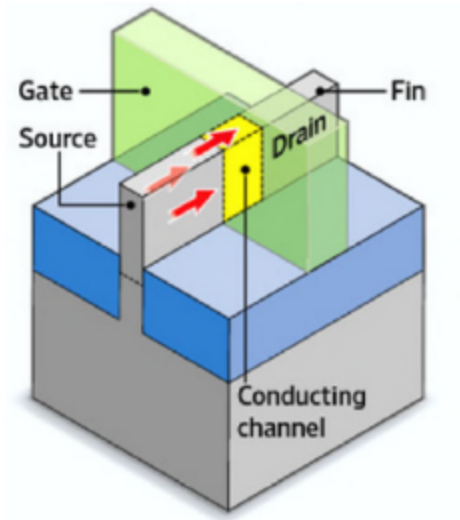


FIG. 6A

POR, 17, 65.

14. I also understand Marlin refers to a dictionary definition of “surround” to support its position. Ex. 2006. In my opinion, however, Marlin and Mr. McAlexander do not use the word “surround” consistently with this definition. Their use of “surround” is also inconsistent with the alleged “all four sides” requirement.

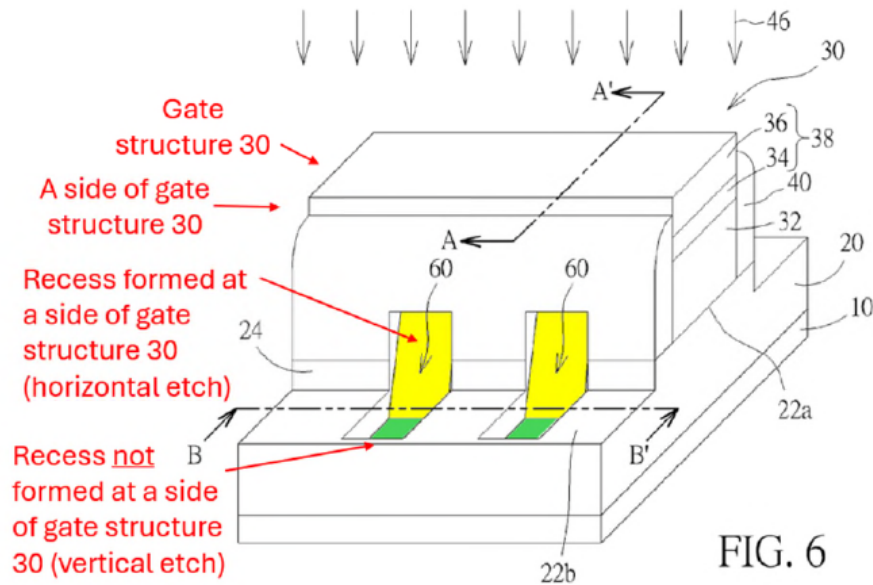
15. For example, referring to the figure below, Marlin and Mr. McAlexander characterize the gate as “wrapped over the fin, surrounding the fin on the top and two sides”:



POR, 19; Ex. 2007, ¶ 38.

16. I have also reviewed Mr. McAlexander’s deposition testimony and am aware that he testified that the meaning of “surround” depends “on the context.” Ex. 1204, 32:7-18. Mr. McAlexander also testified that a group of people in a “semicircle” could be interpreted as surrounding the person in the middle. Neither statement is consistent with a requirement that “surround” requires enclosure on all sides in my opinion.

17. Marlin also alleges that “the isolation structure 20 fully surrounds the recesses 60” in the figure below, yet only three sides of the recesses are surrounded in the figure.



POR, 30-31. In my opinion, this description directly contradicts Marlin’s “all four sides” requirement. Marlin’s use of the phrase “fully surrounds” also contradicts its position and dispels its argument. Marlin states that the isolation structure “fully surrounds the fin structures on all four sides.” POR, 31. In my opinion, this equates its “all four sides” requirement with surrounding the fin structure “fully.” But the claims do not include this qualifier, as Mr. McAlexander admits. Ex. 1205, 33:25-34:2. The claims therefore do not require surrounding on all four sides.

18. To the contrary, a POSITA would have understood that one structure may “surround” another structure on less than all sides. Mr. McAlexander appears to agree based on his description of a gate “surrounding” a fin on three sides. Ex. 2007, ¶38. With this understanding, it is my opinion that Xu and Lin both clearly disclose

and/or render obvious element 1[b]. Regardless, Xu and Lin also meet element 1[b] even under Marlin's interpretation, as described below.

B. Xu meets element 1[b]

19. Xu discloses that “[i]solation features 130, such as shallow trench isolation (STI) structures surround the fin structures 115A and 115B.” Ex. 1004, 3:54-56. Xu uses the precise claim term — “surround”—to describe the claimed relationship and to meet the claim element. Ex. 1001, 8:30; Ex. 1004, 3:54.

20. Marlin's description elsewhere in its response of Xu's isolation structure as “the *surrounding* isolation structure” further confirms my understanding. POR, 48. I disagree with Marlin's attempt to read “surround” out of Xu's specification.

21. Xu discloses that its figures depict “various perspective views of a FinFET device [] in portion or entirety, at various stages of fabrication.” Ex. 1004, 2:51-53. Xu also explains that STI 130 “isolate[s] the fins 120 from each other and other non-illustrated circuit devices.” Ex. 1004, 3:56-58. In my opinion, a POSITA would have understood Figure 2 as a cross-sectional view showing a “portion” of the isolation structure that “surround[s]” the fin structures. Ex. 1004, 2:51-53, 3:56-58.

22. Additionally, Xu clarifies that “Figs. 2-6 have been simplified for the sake of clarity to better understand the inventive concepts of the present disclosure.” *Id.*, 2:57-59. In my opinion, a POSITA would understand this to confirm that the “simplified” figures are not intended to override the specification.

1. Xu’s “fin template” is irrelevant to 1[b]

23. Claim element 1[b] requires “forming an isolation structure to surround the *fin structure*.” Ex. 1001, 8:30. Mirroring the claim language, the Petition asserts Xu’s “fin structure[s]” as the claimed “fin structure”—not the fin template. Pet., 16-18. As described above, Xu’s STI “surround[s] the fin structures” as claimed. Moreover, like the ’384 Patent, Xu later forms an “epitaxial layer” in the source/drain region, including the “fin template.” Ex. 1004, Figs. 4-6, 10A, 11A, 5:1-10, 5:49-68, 10:66-11:11, 11:38-45; Ex. 1001, Fig. 9, 6:38-48. The claims, however, do not require the isolation structure to surround the later-formed “epitaxial layer.”

24. I also disagree with Marlin’s assertion that a POSITA would have understood that Xu’s “‘fin structure’ includes both fins and fin template 135.” POR, 39-40. That assertion is inconsistent with the evidence that Marlin relies upon, which states “it is understood that *‘fin template’ can refer to the newly grown epi semiconductor material alone* ... or the newly grown epi semiconductor material combined with the initial fins.” Ex. 1004, 5:28-30. A POSITA would not disregard the first half of this passage and only consider the combined structure to be the “fin template.” Rather, the patent states that either interpretation is correct.

25. In my opinion, Marlin’s argument is also logically flawed. Even if the later-formed “fin template” could include the “fin structure,” that does not mean the earlier-formed “fin structures” can encompass the “fin template,” which does not

even exist when the fin structures and isolation structures are formed. Ex. 1004, Figs. 2-3.

C. Lin Meets element 1[b]

26. I also disagree that Lin does not disclose element 1[b]. Lin, like Xu, discloses that the depicted figures are merely “perspective and cross-sectional views of the FinFET 200 at various stages of fabrication.” Ex. 1005, ¶ 15. Moreover, Lin also explains that the figures “are simplified for a better understanding of the inventive concepts of the present disclosure.” Ex. 1005, ¶ 14. I do not agree with Marlin’s position that the admittedly “simplified” figures are complete representations of Lin’s teachings.

27. Lin’s detailed description reveals Marlin’s error. Lin discloses that “it is understood that additional processes may be performed before, during, and after” the depicted method “and that some other processes may only be briefly described herein” and that the depicted FinFET “may be included in a microprocessor, memory cell, and/or other integrated circuit.” Ex. 1005, ¶ 14. In my opinion, a POSITA reading Lin would have understood that the figures depict a cross-section of the whole structure. This whole structure provides isolation from fin-to-fin (which alone meets the claim element) and from other integrated devices, such that the isolation structures extend around the outer edges of each fin.

28. This is consistent with the state of the art at the time. As noted in my initial declaration, semiconductor devices comprise “thousands, or even billions of transistors” combined together to form electronic hardware. Ex. 1003, ¶ 35; Ex. 2007, ¶ 35. A POSITA would have understood that the isolation structures of Lin are formed not just to isolate adjacent fins, but to isolate the FinFET from the other components described in Lin that make up a semiconductor device. I also note that Mr. McAlexander stated that FinFET devices would use “shallow trench isolation” to provide this type of surrounding isolation. Ex. 2007, 38:11-29, 77:25-79:3. As described in my previous declaration and in the Petition, Lin’s “isolation region” is an STI structure that is formed using shallow trench isolation (STI) processing—the same “well-known” process described in the ’384 Patent. Ex. 1003, ¶¶ 167-169. This results in lower portions of the fins (blue) being “embedded” in the isolation structure (magenta) just as in the ’384 Patent:

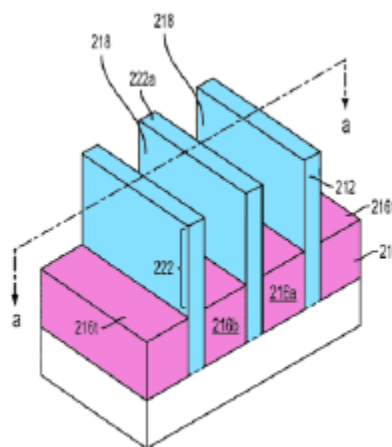


FIG. 6A

Ex. 1005, Fig. 6A (highlighted). STI is conventional and well-known to deposit insulation to surround fins of a FinFET and provide isolation between the fins and from other integrated circuit devices.

29. I also disagree with Marlin's additional arguments regarding Lin and element 1[b].

30. Marlin argues Lin's description of the fins as "between" the isolation structures contrasts with "surround[ing]" the fins as claimed. POR, 66. The '384 Patent, however, uses this exact same word to describe the isolation structure in relation to the fin structures. Ex. 1001, 3:57-58 ("An isolation structure [20] is formed on the substrate *between each fin structure 12...*) (emphasis added). An isolation structure can "surround" and be "between" adjacent fin structures, as the '384 Patent and its description demonstrate. *Id.* In my opinion, Lin's disclosure is therefore entirely consistent with the '384 Patent.

31. Regardless, I maintain that it also would have been obvious to a POSITA for the isolation structures to surround the fin structures. Ex. 1003, ¶ 151. I have reviewed the POR and Mr. McAlexander's declaration and do not find a rebuttal to this point. In my opinion, Marlin cannot provide such a rebuttal given that its arguments support the obviousness of this element.

32. Describing the "preferred embodiment" of the '384 Patent (Ex. 1001, 2:32-35), Marlin submits that fully surrounding the fin structures "is important in

order to fully isolate each fin structure, preventing unwanted contact and electrical interaction and thereby ensuring that each fin structure operates independently without interference.” POR, 26; Ex. 2007, ¶ 54. This is precisely the point I made in my initial declaration when describing the obviousness of the claim element (Ex. 1003, ¶ 151) and evidences why a POSITA would understand and find it obvious for the prior art isolation structures to surround the fin structures. The fact that both Lin and Xu acknowledge their FinFETs may be incorporated into a larger integrated circuit with other devices (Ex. 1004, 3:56-58; Ex. 1005, ¶ 14) underscores this point.

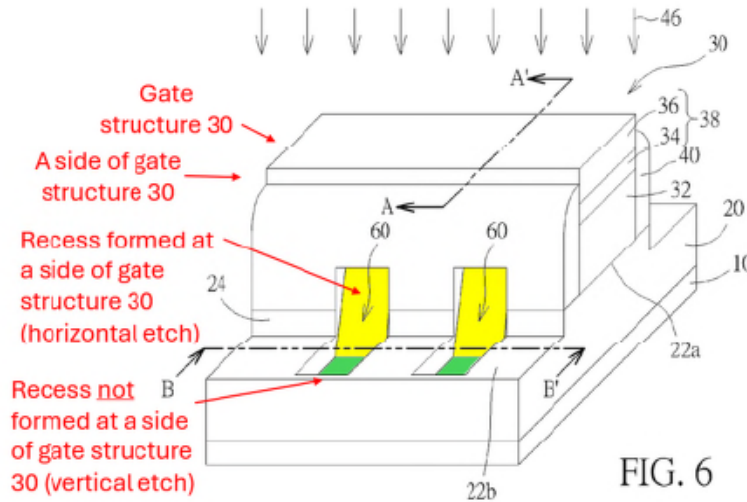
33. The FinFETs disclosed in Xu and Lin would need to be isolated from other devices in the integrated circuit to prevent electrical shorts, leakage paths, and unwanted device-to-device interference, and to promote proper transistor operation. As described above, a POSITA would have understood that the STI structures disclosed by Xu and Lin provide this isolation. In any event, a POSITA would have found such an implementation obvious. Fully surrounding active fin structures with STI was a conventional way to isolate neighboring active regions in integrated circuits, and doing so would have predictably provided the same electrical isolation benefits that Marlin identifies as important. Marlin itself asserts that fully surrounding the fins is important to isolate each fin structure, prevent unwanted contact and electrical interaction, and ensure that each fin operates independently without interference. POR, 26. Those asserted benefits supply a straightforward technical reason why a POSITA

would have understood or found it obvious for the STI in Xu and Lin to surround the fins sufficiently to provide that isolation.

VII. GROUNDS 1A AND 2A DISCLOSE AND/OR RENDER OBVIOUS FORMING A RECESS IN THE FIN STRUCTURE AT A SIDE OF THE GATE STRUCTURE

34. I disagree with Marlin's contention that "the recess formed in the fin must extend at least in the horizontal direction in order to be a recess 'at a side of the gate structure.'" I have reviewed Mr. McAlexander's testimony and do not find that it presents an understandable scope for this proposed limitation. Ex. 1204, 13:21-17:5. In my opinion, the proposed requirement is inconsistent with the '384 Patent.

35. Marlin argues Xu and Lin fail to disclose 1[e] because they do not have a horizontal etch resulting a horizontal recess. But that requirement is not found in the claim language. Instead, Marlin relies primarily on annotations to Figure 6 of the '384 Patent as supporting the alleged limitation. POR, 28-31, 41, 66-67; Ex. 1024, 18:3-24. The '384 Patent, however, discloses that this figure and the related portions of the specification describe only a preferred embodiment. Ex. 1001, 2:33-35, 3:10-12. To arrive at its position, Marlin bifurcates the '384 Patent's recess and argues "the yellow recess area was created 'at a side of the gate structure,' whereas the green part of the recess was not:



POR, 29, 30. Marlin appears to support this with a single passage that Marlin claims:

(1) “stat[es] that the etch extends horizontally” and (2) “ties together the concept of etching horizontally to the formation of the recess at a side of the gate structure.”

POR, 30-31 (citing Ex. 1001, 5:55-60). I disagree with both of these statements.

36. With additional context, the passage Marlin quotes reads:

As shown in FIG. 6 to FIG. 8, a second etching process 46 is carried out to etch the fin structures 12 under the gate structure 30 and the spacers 40. After the etching process, a recess 60 may be formed in each fin structure 12 at at least one side of the gate structure 30. Furthermore, according to this embodiment, the ends of the fin structures 12 at two sides of the gate structure 30 may respectively have a recess 60, and a bottom surface of the recess is preferably shallower than a bottom surface of the isolation structure 20.

Ex. 1001, 5:55-64. This passage does not state “the etch extends horizontally” nor does it describe any “horizontal” etching or extension. It appears Marlin reads “etch the fin structures 12 *under* the gate structure 30 and the spacers 40” to require this horizontal extension. POR, 30-31. This does not make sense. Rather, a POSITA

would understand that “under” in this context refers to the extent of the etch in the vertical direction. Specifically, the sentence beginning with “furthermore” demonstrates that “under” refers to etching down lower than the gate structure and the spacers such that a bottom surface of the recess is “shallower than a bottom surface of the isolation structure.” Ex. 1001, 5:60-64.

37. This is confirmed by the ’384 Patent’s figures. While FIG. 6 depicts some horizontal extension into the *spacer*, it does not depict any horizontal extension into the gate. If “under” required Marlin’s understanding, the recesses would have the same relationship to the gate as to the spacer.

38. Annotated Fig. 7 below explains in greater detail. “Under” means the portion (green) below the surface of both the gate spacers and gate electrode. This is consistent with the ’384 Patent’s description to etch “under” both “the gate structure 30 and spacers 40.” Ex. 1001, 5:55-60. As can be seen in Fig. 7, there is no horizontal extension consistent with Marlin’s interpretation which would be into the red lines (spacers) and blue lines (gate):

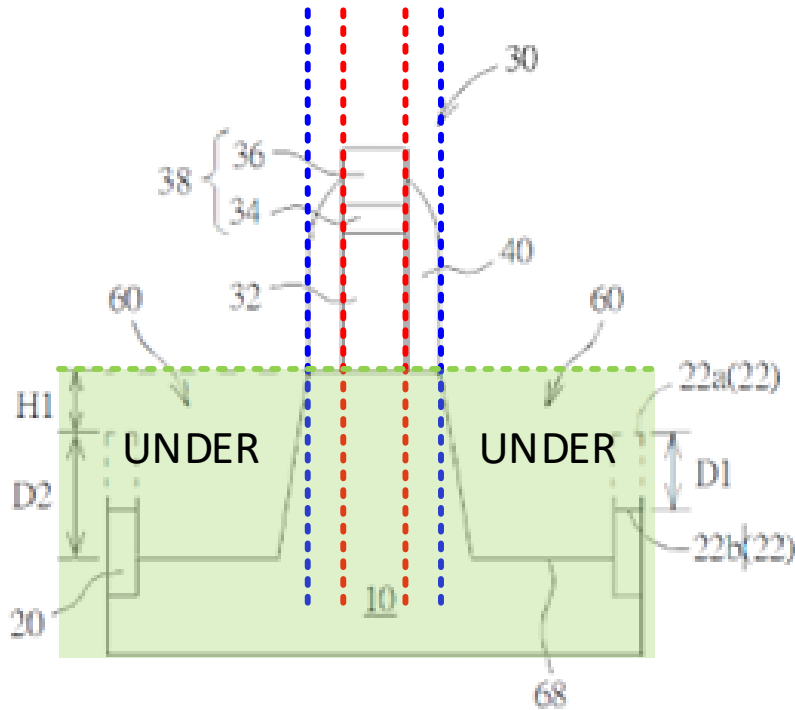
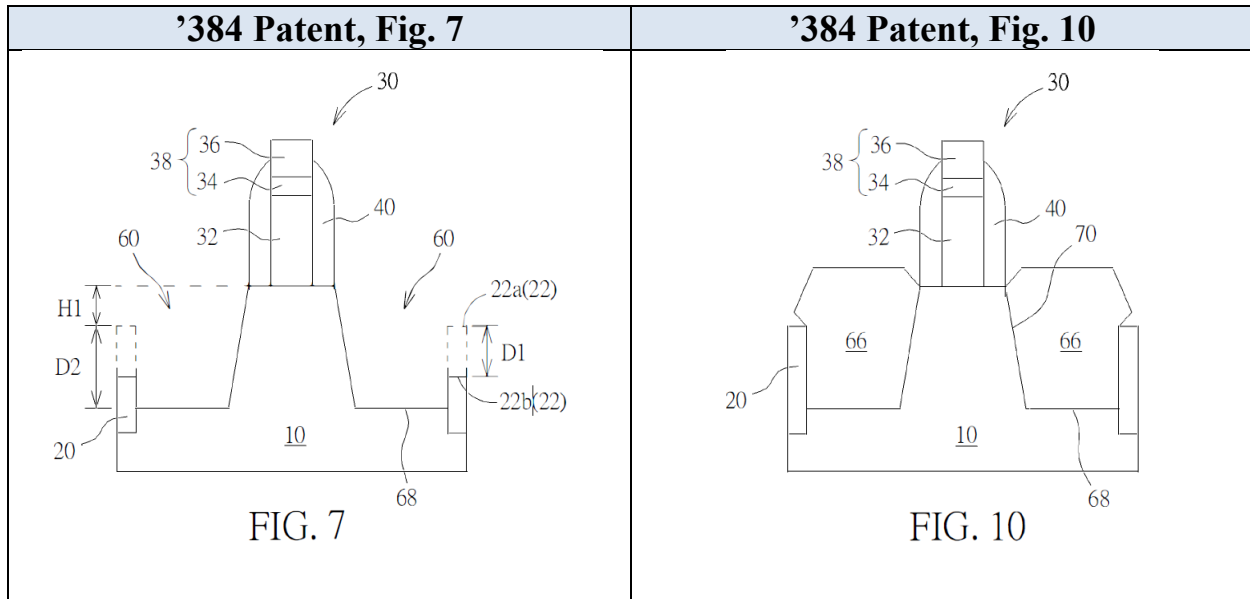


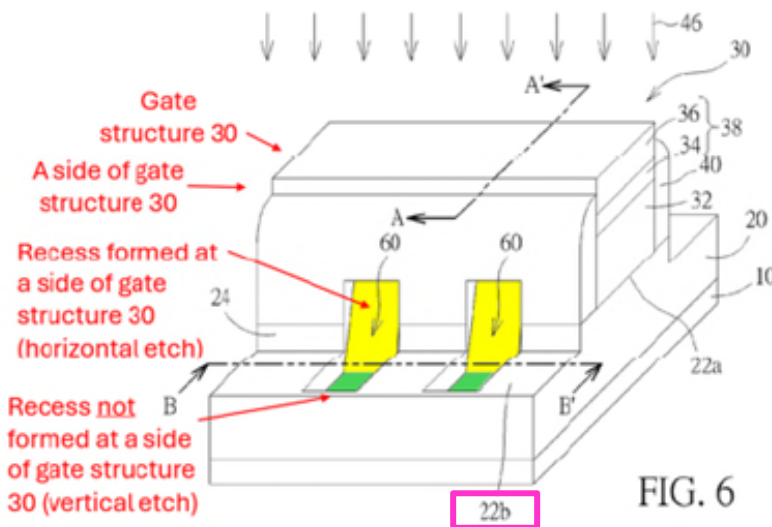
FIG. 7

Ex. 1001, Fig. 7 (annotated). Notably, Fig. 7 is referenced in the passage Marlin relies on which describes “FIG. 6 to FIG. 8,” yet Fig. 7 does not depict the relationship Marlin argues the claim requires.

39. In my opinion, the fact that none of the figures show extension beyond the horizontal bounds of the spacers or gate reinforces that Marlin's position is incorrect. This is evident from Figure 7 and from Figure 10 which fail to show such extension:



40. The passage also expressly describes the “ends of the fin structures” and “bottom surfaces 68 of the recesses” as being “at two sides of the gate structure.” Ex. 1001, 5:60-64. This is not an anomaly—the ’384 Patent consistently uses the phrase “side[s] of the gate” to refer to the broader source/drain region of the transistor. *Id.*, 6:1-4, 6:29-34, 7:5-16, 8:1-4, 8:9-14. For example, the ’384 Patent describes “the top surfaces 22b of the isolation structure at two sides of the gate structure.” *Id.*, 7:7-8. As Marlin’s own figure shows, 22b (magenta) is located in the same region Marlin’s “green” recesses:



POR, 29 (modified). Marlin’s “green” recesses are therefore “at a side of the gate” as claimed, confirming that Marlin’s “horizontal” recess is not required. The same is true for the recesses of Xu and Lin, which are formed in the corresponding source/drain regions at the sides of the gate. Ex. 1004, Fig. 9A; Ex. 1005, Fig. 8A. And because there is no horizontal recess requirement, both Xu and Lin meet this element as set forth in the Petition. Pet., 21-26, 69-72.

VIII. GROUNDS 1A, 1B, AND 2B DISCLOSE AND/OR RENDER OBVIOUS CLAIMS 4 AND 9

41. I disagree with Marlin that the asserted Grounds do not disclose and/or render obvious claims 4 and 9. These claims set forth well-known, conventional replacement metal gate processes or “gate-last” processes that have been used in the art for decades and were standard by 2013. *See* Ex. 1003, ¶ 45 (citing Exs. 1004, 1006, 1022, 1023).

42. I have reviewed Marlin's POR and Mr. McAlexander's declaration and do not find arguments rebutting the obviousness of claim 4, specifically. Marlin's arguments are focused on element 9[c], which relates to forming a gate dielectric to conformally cover a sidewall and a bottom of the trench. POR, 58-64, 68-73; Ex. 2007, ¶¶8, 104-107, 109-110, 117-121. I disagree with those positions.

A. Marlin fails to rebut claim 4's obviousness

43. As described above, Marlin does not mount challenges to claim 4. Marlin only expressly challenges 9[c]. And when challenging rationales for obviousness, Marlin only refutes the obviousness of forming a gate dielectric to conformally cover the sidewalls and a bottom of the trench. The obviousness of the gate structure being a dummy gate structure (as in claim 4) is not specifically challenged.

B. Xu in view of the knowledge of a POSITA renders claim 9 obvious

44. Xu specifically discloses using a "gate last process." Ex. 1004, 4:14. As the Petition explains, a POSITA would have understood and found obvious that Xu's disclosure refers to the steps set forth in claim 9. Pet., 38-42. This is particularly true where both the '384 Patent and Marlin's expert acknowledge that each of these steps was well-known and therefore within the knowledge of a POSITA. Ex. 1001, 7:31-34; Ex. 1204, 66:22-25.

45. I disagree with Marlin’s contention that the Patent merely acknowledges that RMG processes “in general” were well-known. POR, 59. Rather, the patent expressly admits that the particular process described and claimed was “well-known to those in the art.” Ex. 1001, 7:31-34. Marlin’s characterization of the Petition fails to credit this important admission.

46. Specifically, the ’384 Patent describes a “high-k last replacement metal gate (RMG) process” comprising four specific steps. Ex. 1001, 7:21-29. It then states that “*the* RMG process”—meaning the particular process described above — “and the contact formation process are well-known to those skilled in the art.” *Id.*, 7:31-34 (emphasis added). This distinction is critical. The patent’s own inventors conceded that the very steps set forth in claims 4 and 9 were known. Mr. McAlexander also agrees that each claimed step was known. Ex. 1204, 66:22-25. I addressed this understanding of the state of the art and knowledge of a POSITA in my opening declaration. Ex. 1003, ¶¶ 45-46, 108-109, 120-130.

47. Marlin’s arguments related to other types of gate-last processes as rendering the claim non-obvious fail for similar reasons. While a POSITA may have known about these other processes, the ’384 Patent itself confirms that a POSITA would have known about the specific high-k last replacement metal gate process it describes and claims. Additionally, as explained in the Petition, it was known at the time that multi-gate FETs (like FinFETs) “require[] highly conformal deposition

techniques for the ... dielectric.” Pet., 41 (quoting Ex. 1008, 16). In my opinion, this reinforces the obviousness of 9[c]—a POSITA would have found it obvious to “form[] a gate dielectric layer to conformally cover a sidewall and a bottom of the trench” to meet this design requirement which ensures the gate-last process is “compatible with the higher topography” of such devices. Ex. 1001, 9:4-5; Ex. 1008, 16.

48. I disagree that my testimony concedes a POSITA would not have been motivated to form a gate dielectric layer to conformally cover a sidewall of the trench.

49. As my deposition testimony explains, not every gate-last process follows the same sequence. In some gate-last processes, the gate dielectric is formed before the sacrificial gate and remains in place after the sacrificial gate is removed. In other gate-last processes, including high-k-last RMG processes such as the process described in the '384 Patent and disclosed by Brask, the final high-k gate dielectric is formed after the sacrificial gate is removed. In the latter type of process, the high-k dielectric is deposited into the replacement-gate trench. In this type of process, a conformal deposition is typical and results in the dielectric coating exposed surfaces within the trench, including the bottom and sidewalls. Thus, the claimed step of forming a gate dielectric layer to conformally cover a sidewall and a bottom of the trench is consistent with a known high-k-last RMG process, while recognizing that other gate-last flows may retain a previously formed gate dielectric.

50. One reason to use a high-k-last RMG process is to protect the final gate dielectric from earlier high-temperature processing. As my initial declaration explains, in such processes, “the final high-K dielectric and metal gate stack are introduced after all high-temperature processing is complete.” Ex. 1003, ¶ 44. In doing so, “sensitive materials are never exposed to damaging thermal steps.” *Id.*, ¶ 45. This consideration applies to both the metal gate material and the final high-k gate dielectric. The gate dielectric affects important transistor characteristics, including gate capacitance, leakage, reliability, and threshold voltage. Exposing the final gate dielectric to high-temperature processing can alter or degrade the dielectric material and thereby affect device performance, including threshold voltage control.

51. Against this backdrop, the obviousness of claims 4 and 9 is straightforward. Each step in these claims represents a well-known aspect of the “gate-last” processing described in Xu. And as the Petition demonstrates, these steps are not merely “well-known” in the abstract, they specifically known as steps of Xu’s “gate last” process and would have been obvious to a POSITA as described in the Petition. Pet., 32-33, 38-42; Ex. 1003, ¶¶ 108-109, 120.

C. Xu-Brask renders claim 9 obvious

52. I disagree that the Xu-Brask combination fails to render claim 9 obvious.

53. In my opinion, Marlin’s argument ignores Brask’s express recognition that its disclosed gate-last process “enables tuning of work functions such that

performance of the transistor may be ‘dramatically improved.’” Pet., 48 (citing Ex. 1006, ¶ 58). This express disclosure of motivation in Brask demonstrates the obviousness of the claim and rebuts Marlin’s arguments.

54. Marlin’s remaining arguments are similar to those discussed above in Ground 1A. Marlin ignores Brask’s disclosures each time. Marlin again argues that “gate-last process” is a general term encompassing procedures that do not meet 9[c]. POR, 62-63. This is even more irrelevant here because Brask discloses the specific process at issue (Pet., 49-56) and motivates its combination with Xu (Pet., 47-50).

55. Marlin then again argues Xu’s disclosure of “gate-last process is insufficient to motivate implementing” the step of 9[c]. POR, 63. In doing so, Marlin ignores Brask’s disclosure of each element of the claimed process along with the numerous rationales for combining the references set forth in the Petition, including the express advantage acknowledged by Brask. Pet., 47-50; Ex. 1006, ¶ 58.

56. Finally, Marlin argues the Petition relies only on “benefits that would apply to any gate-last process” rather than motivating Brask’s specific process. POR, 64. I disagree. The Petition relies on the disclosed advantages of Brask’s specific process, including protecting sensitive final gate-stack materials from high-temperature processing and enabling better control of gate electrode work functions. The Petition further supports those advantages with evidence showing they were widely known at the relevant time. Pet., 47-49; Ex. 1006, ¶ 58.

57. I am also aware that Mr. McAlexander agrees that work function tunability, including tunability resulting from Brask's method, is beneficial. Ex. 1204, 68:3-6. This further supports my opinion that a POSITA would have found it obvious to apply Brask's process to Xu.

58. In any event, as I described above, a POSITA would have understood that the temperature-protection rationale underlying Brask's gate-last process applies not only to the gate electrode material, but also to the final high-k gate dielectric material in a high-k-last RMG process. Ex. 1003, ¶¶ 44 (high-k dielectric material introduced after high-temperature processing), 45 (gate-last process advantageous as "sensitive materials are never exposed to damaging thermal steps"). In such a process, the final high-k dielectric and metal gate stack are introduced after high-temperature source/drain processing has been completed, thereby avoiding exposure of those sensitive final gate-stack materials to potentially damaging thermal steps. This is relevant because the material properties and interface quality of the high-k gate dielectric can affect transistor characteristics such as leakage, reliability, capacitance, and threshold voltage control.

D. Lin-Brask renders claim 9 obvious

59. I disagree with Marlin's assessment of the Lin-Brask combination for similar reasons.

60. Marlin first argues that using a gate-last process in Lin is non-obvious because there are “pros and cons” to gate-first and gate-last approaches. I disagree. A POSITA would have understood these tradeoffs and found it obvious to use Brask’s gate-last process for the reasons set forth in the Petition. Pet., 79-83. Marlin then asserts that the Petition and my declaration argue that “gate-last processing did not come about until after Lin.” POR, 69-70. I disagree with this characterization. Lin does not disavow gate-last processing. It merely depicts a different process and does not foreclose or warn against the use of gate-last with its method. In my opinion, whether or not the Lin inventors were aware of gate-last processing does not affect whether a POSITA would have found using Brask’s gate-last process to be obvious. The argument presented is simple: Lin chose one approach to gate formation; Brask teaches another approach, one with well-recognized advantages. Pet., 79-83. Moreover, by the time the ’384 Patent was filed, the industry had largely adopted Brask’s solution. *Id.*, 80. A POSITA considering both references would have found it obvious to apply Brask’s process to Lin to achieve Brask’s expected benefits.

61. Even assuming the Lin inventors were aware of gate-last processing, this only confirms a point made in my initial declaration: both approaches were within a POSITA’s knowledge. Ex. 1003, ¶¶ 180-181. This supports my opinion that it would have been obvious to apply Brask’s known technique to Lin’s FinFET fabrication

method, which was ready for improvement through Brask's gate-last processing. *Id.*, ¶ 181.

62. Marlin's further arguments are the same as those raised for Grounds 1A and 1B. I disagree for the reasons stated above.

IX. MARLIN'S REMAINING CHALLENGES ARE UNPERSUASIVE

A. Xu's embodiments are compatible and obvious to combine

63. I disagree with Marlin's contention that Xu fails to disclose or render obvious "etching the isolation structure" and "forming a recess in the fin structure" because Xu's first and second embodiments are "incompatible" and lack a motivation to combine. POR, 42-48; POPR, 24-30. To the contrary, the Petition establishes that Xu motivates the combination by detailing advantages achieved by the second embodiment (*i.e.*, by controlling recess depth, channel strain "can be achieved and optimized," thereby "independently optimiz[ing] performance of each FinFET device"). Pet., 23-24.

64. I disagree with Marlin's response that Xu's first embodiment introduces channel strain through a different method and therefore "does not benefit from" and "is incompatible with" the proposed modification. POR, 46-48. Marlin does not support this contention other than citing a statement from Mr. McAlexander. POR, 48 (citing Ex. 2007, ¶ 87). I have reviewed Mr. McAlexander's deposition and note that he does not have experience in strained channel transistor design. Ex. 1204, 88:15-17.

In my opinion, a POSITA with such experience would understand and find it obvious that Xu's second embodiment is applicable to its first and achieves the benefits of channel strain optimization and tailoring.

65. Marlin's argument overlooks a key fact—through Xu's second embodiment, strain is not just achieved but “optimized” by controlling source and drain depth. Ex. 1004, 15:56-16:2. As stated in my previous declaration, a POSITA “would have been familiar with the goal of imparting and optimizing strain ... and would have found it obvious to apply [Xu's second embodiment to] Xu's first embodiment in order to further tailor the strain.” Ex. 1003, ¶ 90 (citing Exs. 1004, 1005). *See also id.*, ¶ 94 (“applying the recessing of the fins to the first embodiment would have yielded predictable results in enhanced channel strain”). In my opinion, Xu therefore expressly motivates and renders obvious “etching the isolation structure” and “forming a recess in the fin” as claimed. *See* Pet., 20-26; Ex. 1003, ¶¶ 84-95.

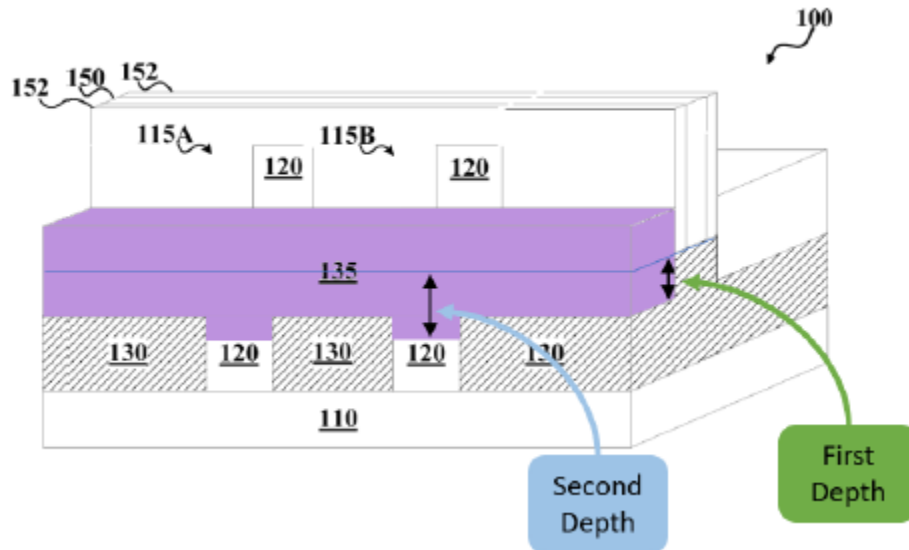
66. Moreover, the Petition also explains that: (1) Xu's embodiments are not just compatible, but described as used together in both the specification and the claims (Pet., 24-26; Ex. 1003, ¶¶ 91, 95); and (2) the combination is merely the application of a known technique (Xu's second embodiment) to a fabrication process ready for improvement (Xu's first embodiment). *See* Pet., 23-24, 26. Marlin does not rebut these points.

67. Indeed, Marlin does not appear to dispute any of the following opinions from my initial declaration: that Xu’s disclosure at 16:5-17:10 describes combining the first and second embodiments in a single fabrication method (Ex. 1003, ¶ 91); that Xu’s claim 19 expressly combines the two embodiments (Ex. 1003, ¶ 95); and the facts confirming that the combination is obvious as applying a known technique to a known method ready for improvement to yield predictable results (Ex. 1003, ¶ 94). In my opinion, these unrebutted facts support the obviousness of combining Xu’s embodiments as described in the Petition and my previous declaration. Pet., 24-26; Ex. 1003, ¶¶ 91-95

B. The combination results in the second depth being deeper than the first depth

68. I disagree that it is “hindsight” to arrive at the claimed depth relationship from the combination of Xu’s embodiments. POR, 48-49. Xu’s second embodiment forms source/drain recesses by removing material from the exposed source/drain portions of the fin structures until the recess extends “to a top, exposed surface of the fin portion 220.” Pet., 30; Ex. 1004, 10:49-56. Xu further explains that the trench sidewalls may be defined by, among other structures, fin portions 220, isolation features 240, remaining fin portion 230 in the channel region, and/or a protective layer. Ex. 1004, 10:49-54. Thus, when Xu’s second-embodiment fin-recessing step is applied with the isolation-etching step of Xu’s first embodiment, the resulting fin recess extends below the etched top surface of the isolation structure, producing the

claimed relationship in which the second depth is deeper than the first depth, as shown in the figure below depicting the combination:



Pet. 31 (depicting Ex. 1004, Fig. 5 (modified)).

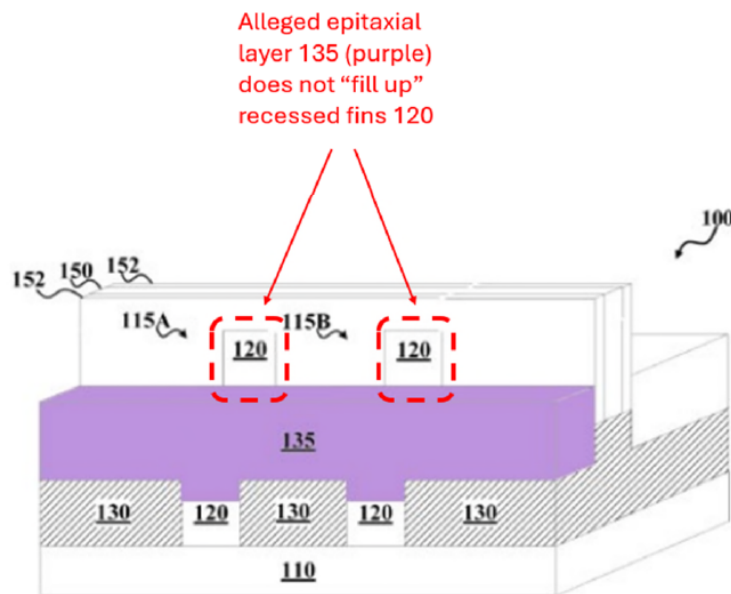
69. Marlin’s contention that “[t]here is nothing to suggest ... one etch would go down further than the other” (POR, 49) is built on a false premise—that Xu’s second embodiment “etches a fin without concern as to the height of the surrounding isolation structure” (*Id.*, 48).

70. In my opinion, this is untrue. Xu’s strain optimization results from controlling the depth of the source/drain regions. *See* Pet., 23-25; Ex. 1003, ¶¶ 89-94, Ex. 1004, 15:56-16:6. Xu’s second embodiment achieves this by etching the fins below a top surface of the isolation structure. *See* Pet., 22-23; Ex. 1003, ¶¶ 87-88; Ex. 1004, 7:58-61, 10:34-36. The resultant depths are not based on hindsight, but a straightforward application of Xu’s second embodiment to its first in the manner set

forth in the Petition. *See* Pet., 22-26 (describing combination); Pet., 30 (describing structure resulting when combined “as discussed above”).

C. Xu meets 1[f]

71. Referring to modified Fig. 5 below, Marlin argues Xu does not satisfy 1[f] because Xu’s “fin template does not fill up the recesses, as the fin template does not extend to the top of the alleged recess:”



POR, 49-52. I disagree with Marlin’s argument.

72. First, Marlin mischaracterizes the “alleged recess.” Marlin excerpts the image below and treats the blue-highlighted regions as defining the entire alleged recess, rather than recognizing that the Petition used the blue highlighting to identify the fin structures.

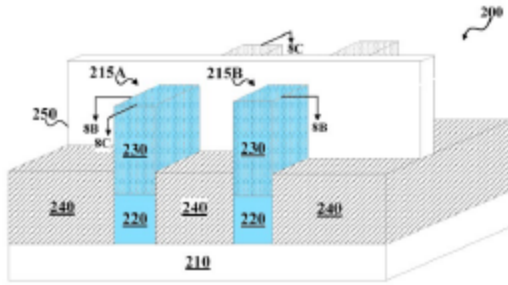


FIG. 8A

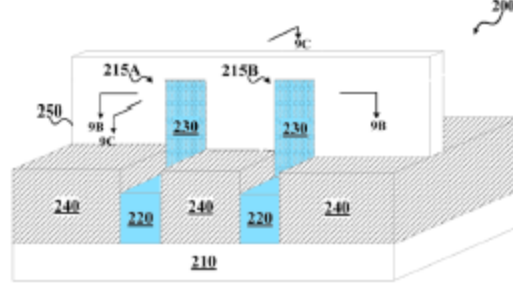


FIG. 9A

Ex. 1004, Fig. 8A, Fig. 9A (highlighted). But as Xu discloses, the recess sidewalls are “defined by ... isolation features 240,” which bound the recess as shown in Fig. 9A above.

73. Specifically, Xu explains that the resulting trench sidewalls may be defined by fin portions 220, *isolation features 240*, remaining fin portion 230 in the channel region, and/or a protective layer. Ex. 1004, 10:49-54.

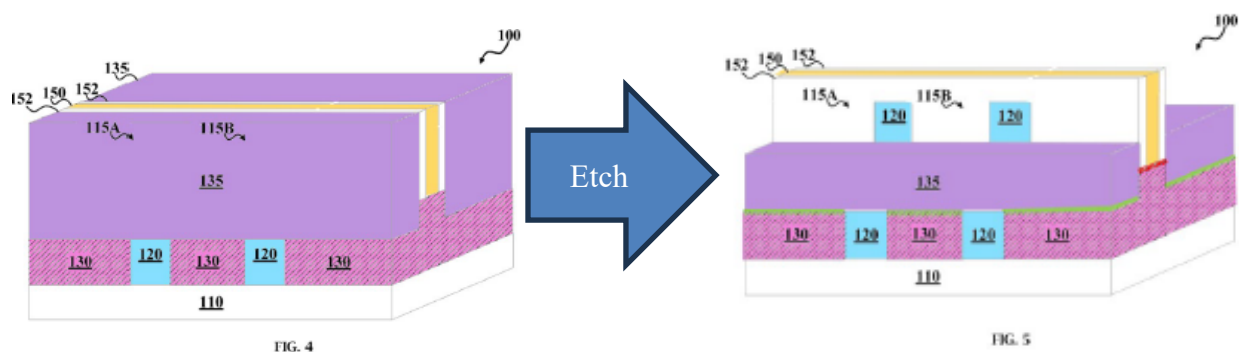
74. I have read Mr. McAlexander’s deposition testimony and understand that he agrees that, in the context of the modified Fig. 5, above, there is no recess formed in the support portions of the fin (circled red) and that “the top surface of 120 is lower than the top surface of 130. That defines the recess.” Ex. 1204, 48:21-50:4. I also understand Mr. McAlexander’s position to be that the recess in Xu is purely vertical, meaning there is no recess where the vertical portions of the fin remain under the gate. *Id.*

75. Consistent with this understanding, the later-formed epitaxial layer need not fully cover every exposed portion of the fin portion under the gate in order to “fill up” Xu’s recess, which is defined by the isolation structures.

76. I also disagree that the claim requires the epitaxial layer to “completely fill up” the recess in the manner Marlin suggests. Claim 1 recites “forming an epitaxial layer to fill up the recess,” not “completely fill up the recess.” In my opinion, a POSITA would understand “fill up” and “completely fill up” to have different meanings, and would not import a complete-fill requirement into the claim absent claim language requiring it.

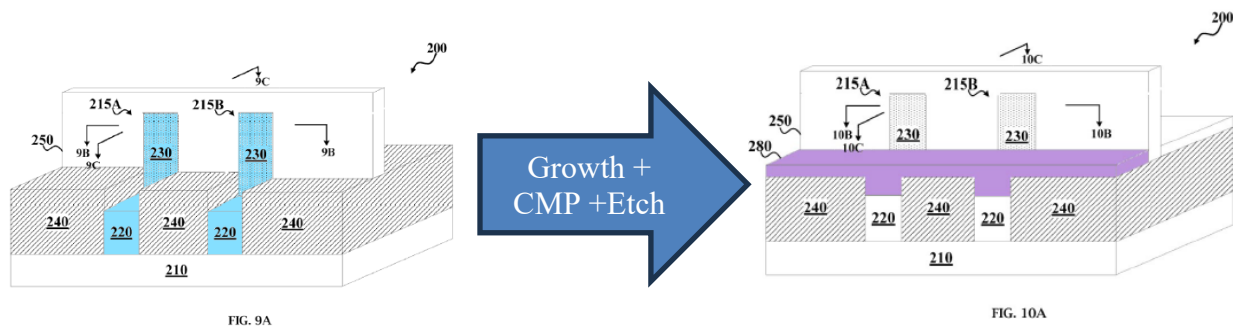
77. In my opinion, Marlin’s position also fails to consider Xu’s relevant teachings, which meet the claim in multiple ways.

78. First, Xu’s embodiments describe forming an epitaxial layer on “exposed portions of the fins” before etching the epitaxial layer to a final height. *See* Pet., 28-29 (citing Xu, 5:1-2, 11:4-8). The Petition depicts this with respect to Xu’s first embodiment:



Pet., 12-13. In Figure 4, the epitaxial layer is: (1) formed in the source drain region (Ex. 1004, 5:4-6); and (2) planarized (*id.*, 5:26-28). In Figure 5, “an etching process is applied to etch back the fin template 135.” *Id.*, 5:35-36.

79. The Petition further explains that Xu’s second embodiment uses a “process similar to that described” in Figure 5. Pet., 27. A POSITA would have understood this to include the steps of forming, planarizing, and etching the epitaxial layer:



Ex. 1004, Figs. 9A-10A (modified). Prior to the final etching, Xu’s “fin template” therefore “completely cover[s] the bottom surface [] and sidewalls [] of the corresponding recess,” as Marlin argues is required. *Id.*; POR, 51. The claim language does not preclude subsequent processing of the epitaxial layer. Ex. 1001, 8:25-9:6.

80. Furthermore, Xu’s second embodiment describes forming template 280 by epitaxially growing semiconductor material on the exposed fin portions in the source/drain regions. Ex. 1004, 11:4-8.

81. A POSITA would understand that this epitaxial growth occurs on exposed crystalline semiconductor surfaces. Thus, to the extent a crystalline sidewall of the remaining SiGe channel portion 230 is exposed at the source/drain recess, that exposed SiGe sidewall could also serve as a nucleation or growth surface. Accordingly, the regrowth would not necessarily be limited to vertical growth from only the horizontal top surface of 220; it could also proceed from exposed SiGe surfaces of 230, while still being described by Xu as growth on the exposed source/drain portions of the fins.

82. Xu identifies epitaxial growth techniques, including molecular beam epitaxy, of the same general type described in the '384 Patent for growing the epitaxial material. Ex. 1001, 6:43-46 (“molecular beam epitaxy (MBE) process”); Ex. 1004, 11:10 (“molecular beam epitaxy”). A POSITA would have understood that such epitaxial growth processes are not limited to growth from horizontal surfaces, but may grow from exposed crystalline semiconductor surfaces, including exposed sidewall surfaces.

83. Any material difference, *i.e.*, that 230 is SiGe and 220 is Si, may affect growth rate, interface strain, composition, and defect formation, but it would not preclude growth from an exposed SiGe sidewall. A POSITA therefore would have understood that Xu’s fin template can fill the source/drain recess when formed, thereby meeting claim element 1[f]’s requirement of “forming an epitaxial layer to

fill up the recess.” The claim language does not preclude subsequent processing, including later etch-back or further epitaxial growth. Ex. 1001, 8:25-9:6.

84. Second, Xu’s subsequent processing steps confirm that both embodiments meet 1[f]. After recessing the fin template 135/280, Xu discloses that epitaxial semiconductor layer 160/285 is grown over the fin template to cover exposed sidewalls of the fin and complete the source/drain regions of the device:

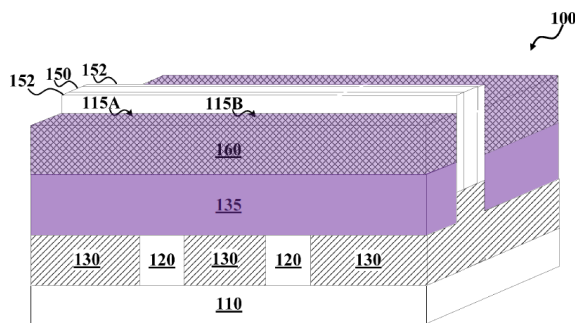


FIG. 6

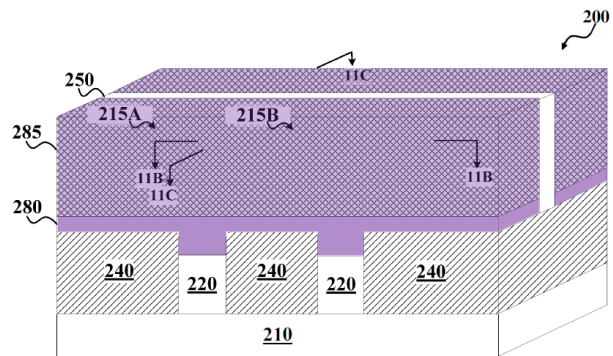


FIG. 11A

Ex. 1004, Fig. 6 (modified)); Ex. 1004, 11A (modified). *See also* Pet., 12; Ex. 1003, ¶¶ 57-59. The same is true in Xu’s second embodiment and the resulting combination. Ex. 1004, Fig. 11A, 11:34-50. This further confirms that Xu meets 1[f], even under Marlin’s restrictive interpretation.

D. Xu meets claim 8

85. I disagree that Xu fails to disclose and/or render obvious “depositing a material layer to conformally cover the gate structure and the fin structure.” POR, 52-58.

86. Xu discloses “spacers [] may be formed by depositing a silicon nitride layer and then dry etching the layer to form the spacers.” Ex. 1004, 4:47-49. As the Petition explains, a POSITA would have: (1) understood this as describing standard FinFET processing techniques that conformally deposit silicon nitride to form gate spacers (Pet., 36-37); (2) found it obvious to use conformal deposition based on its well-understood benefits (*id.*); and (3) at least found it obvious to substitute a conformal deposition process into Xu’s method, to the extent Xu’s method is found not to use one (*id.*, 37). I disagree with Marlin’s arguments to the contrary.

1. Xu discloses and/or renders obvious conformal deposition

87. A POSITA would have understood Xu’s disclosure of “depositing a silicon nitride layer and then dry etching the layer to form the spacers” (Ex. 1004, 4:57-59) as referring to conventional spacer formation processes that use conformal deposition followed by directional etching to arrive at a gate spacer. As explained in my initial declaration, the claimed spacer-formation steps were common and conventional by 2013. Ex. 1003, ¶¶ 116-117. A POSITA would have understood Xu’s disclosure as describing the standard spacer-formation sequence: first depositing a dielectric layer over the gate/fin topography, and then anisotropically etching the layer so that material is removed from horizontal surfaces while remaining on the vertical sidewalls to form spacers. Because the purpose of this process is to leave spacer material on sidewalls, the deposited layer must provide sufficient coverage of those

sidewalls. Thus, conformal or substantially conformal deposition followed by anisotropic etching was not merely one possible way to form gate spacers; it was the standard and well-known approach for forming sidewall spacers in 2013.

88. Marlin's reliance on other types of deposition fails to account for how gate sidewall spacers were ordinarily formed in semiconductor processing. The disclosures in Lin and Brask confirm the conventionality of this process, as does Ex. 1025, relied upon in my initial declaration. *Id*; Ex. 1005, ¶ 30 (describing this process for spacer formation); Ex. 1006, ¶ 53 (same). The '384 Patent also demonstrates this conventionality. The '384 Patent, claims "depositing ... conformally" but the specification merely states that "[a] material is deposited ... and then an etching process is performed to form the spacers 40." Ex. 1001, 5:12-15.

89. Similar to that described above with respect to different types of gate-last processing, I also disagree that the existence of non-conformal depositions or depositions with greater conformality than LPCVD and PECVD would lead a POSITA to understand Xu in a different way or make the claimed steps any less obvious. For example, the Petition explains that depositing Xu's spacer material conformally at least would have been obvious for multiple reasons, including the beneficial coating of "all exposed surfaces uniformly." Pet., 36-37; Ex. 1003, ¶¶ 115-118. This is especially so here, where even the evidence Marlin submits establishes the advantages and desirability of conformal deposition. Ex. 2004, 2-5. I have

reviewed this exhibit and find that it consistently describes the benefits of conformal deposition, particularly in the claimed scenario involving non-planar surfaces. As such, Marlin's question of "why a POSITA would choose a conformal deposition technique" is answered by its own exhibit which establishes that conformal coating is recommended for non-planar coating, as is the case when depositing insulation over fin and gate structures. Ex. 2004, 5. Notably, Mr. McAlexander also acknowledges these advantages. Ex. 1204, 57:14-58:25.

90. The Petition separately establishes that substituting Xu's deposition—to the extent not already conformal—with a conformal process would have been obvious. Pet., 37; Ex. 1003, ¶ 118. As stated in my initial declaration, a POSITA would have been aware of both conformal and non-conformal deposition techniques and would have known and found it obvious to substitute a conformal technique into Xu's method, to the extent not already conformal. Ex. 1003, ¶¶ 116-118. A conformal deposition process would have predictably provided more uniform coverage over the non-planar gate and fin topography, including vertical sidewalls and recessed regions. That uniform coverage is particularly useful for forming gate sidewall spacers because the subsequent anisotropic etch removes material from horizontal surfaces while leaving material on vertical sidewalls. A POSITA therefore would have understood that improved sidewall coverage would help form spacers with more controlled thickness and continuity, reduce the risk of thin spots or discontinuities, and provide

a predictable spacer structure for later source/drain processing. Accordingly, substituting a conformal deposition technique into Xu's spacer-formation process would have been a straightforward use of a known deposition technique to obtain predictable and beneficial results.

2. Marlin's evidentiary attacks are meritless

91. I also disagree with Marlin's position regarding Exhibit 1025. Exhibit 1025 broadly describes CVD techniques for depositing silicon nitride films and identifies LPCVD and PECVD as standard approaches. Ex. 1025, at 270, 296. Although Table 16-2 identifies the PECVD film as hydrogenated silicon nitride, that distinction does not defeat the relevance of Exhibit 1025. A POSITA would have understood that PECVD silicon nitride is commonly written as SiN or SiN:H because PECVD nitride films are typically non-stoichiometric and can incorporate hydrogen from the plasma deposition chemistry. Ex. 1025, 296. That does not mean PECVD is not a silicon nitride deposition process; rather, it reflects a known property of PECVD silicon nitride films. A POSITA would have understood that the hydrogenation does not place PECVD-SiN outside the category of "silicon nitride," but instead results from using PECVD to deposit the silicon nitride. A POSITA would therefore understand PECVD-SiN as "depositing a silicon nitride layer" (Ex. 1004, 4:57-59) regardless of whether the resulting layer further contains hydrogen. Moreover, claim 8 does not require LPCVD, PECVD, or stoichiometric Si₃N₄. It requires depositing a

material layer to conformally cover the gate structure and fin structure. Exhibit 1025 establishes the conventional and advantageous nature of such conformal depositions for silicon nitride (and other insulators), which a POSITA would have known and found obvious to use in Xu's method. Ex. 1025, 277, 296-299.

X. Conclusion

92. As set forth above, and in my initial declaration, it is my opinion that the Challenged Claims of the '384 Patent are unpatentable based on the prior art for the reasons set forth above and in my initial declaration.

93. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

94. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to account for new information as it becomes available to me.

95. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false

statements and the like so made are punishable by fine or imprisonment, or both, under
Section 1001 of Title 18 of the United States Code.

Date: May 27, 2026

By: 

Jack Lee, Ph. D.