

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

RADIAN MEMORY SYSTEMS, LLC,
Patent Owner.

Case IPR2025-01266
Patent 11,544,183

EXHIBIT 2020

DECLARATION OF DR. MARK JONES

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I. INTRODUCTION

1. My name is Mark Jones. I have been retained as an expert witness to provide my independent opinion in regard to the matters at issue in *inter partes* review of U.S. Patent No. 11,544,183 (“the ’183 patent”) in IPR2025-001266. I have been retained by Radian Memory Systems, LLC (“Radian” or “Patent Owner”), the Patent Owner in this proceeding. Petitioner is Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (“Samsung” or “Petitioner”).

2. I am being compensated \$750 per hour for my time spent working in connection with this case. My compensation is in no way related to the outcome of this litigation. If called as a witness, I would testify as to the statements and opinions contained in this report.

3. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

II. QUALIFICATIONS

4. I graduated summa cum laude from Clemson University in 1986 with a B.S. in Computer Science and a minor in Computer Engineering, while holding a National Merit Scholarship and the R. F. Poole Scholarship. I graduated from Duke University in 1990 with a Ph.D. in Computer Science, while holding the Von Neumann Fellowship.

5. Upon graduation, I joined the Department of Energy at its Argonne National Laboratory facility. While at the Department of Energy, I received the IEEE Gordon Bell Prize.

6. In 1994, I joined the Computer Science faculty at the University of Tennessee. While at the University of Tennessee, I received a CAREER Award from the National Science Foundation.

7. In 1997, I joined the Electrical and Computer Engineering faculty at Virginia Tech. I was cited multiple times on the College of Engineering's Dean's List for teaching.

8. In 2021, I became a Professor Emeritus of Electrical and Computer Engineering at Virginia Tech.

9. During my academic career, my teaching included courses on computer architecture and computer organization. These classes frequently covered topics specific to storage systems and more specifically to flash storage systems—including, for example, the division of responsibility for storage management between software and hardware on a host system and software and hardware on an embedded controller. My research has also at times involved the integration of flash storage into various computer architectures.

10. In addition to the activities, education, and professional experience listed above, I have been involved in research projects that contribute to my expertise

relating to this report. While at Virginia Tech, for example, I was a primary or co-investigator on government and industrial research grants and contracts in excess of five million dollars.

11. A detailed record of my professional qualifications is set forth in the attached Exhibit A, which is my *curriculum vitae*, including a list of publications, awards, research grants, and professional activities. My *curriculum vitae* also lists the matters in which I have served as an expert.

III. BASES OF OPINION

12. In the course of conducting my analysis and forming my opinions, I have reviewed materials including those listed below:

- i. The Petition filed by Petitioner in IPR2025-01266,
- ii. U.S. Patent No. 11,544,183 (“’183 Patent”) (Ex. 1001);
- iii. The prosecution history of the ’183 Patent (Ex. 1002);
- iv. The Declaration of Dr. Heiner Litz in IPR2025-01266 (Ex. 1003) (the “Litz Declaration” or “Litz-Decl.”);
- v. U.S. Patent No. 9,239,781 (“Ellis”) (Ex. 1004);
- vi. U.S. Pub. No. 2012/0096217 (“Son”) (Ex. 1005);
- vii. U.S. Pat. Pub. No. 2011/0271032 (“Yamada”) (Ex. 1006);
- viii. U.S. Pat. No. 7,739,444 (“Sinclair”) (Ex. 1007);
- ix. U.S. Pat. Pub. 2012/0284587 (“Yu”) (Ex. 1008);

- x. U.S. Pat. No. 7,409,489 (“Sinclair II”) (Ex. 1009);
- xi. U.S. Pat. Pub. No. 2008/0189485 (“Jung”) (Ex. 1010);
- xii. Nick McKeown et al, OpenFlow: Enabling Innovation in Campus Networks (Ex. 1011);
- xiii. The exhibits and other documents cited herein.

IV. APPLICABLE LEGAL STANDARDS

A. Level Of Ordinary Skill In The Art

13. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan,” or by the acronyms “POSA,” “POSITA” or “PHOSITA,” as of the time of the invention. I understand that the ’183 patent issued on January 3, 2023, and that it claims priority to Provisional Application No. 61/757,464, which was filed on January 28, 2013.

14. I have been told that the person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. I am instructed that “relevant” means relevant to the challenged claims of the ’183 patent.

15. I understand that factual indicators of the level of ordinary skill in the art include the various prior art approaches employed, the types of problems encountered in the art, the rapidity with which innovations are made, the

sophistication of the technology involved, and the educational background of those actively working in the field. I understand that, in assessing the level of skill of a person of ordinary skill in the art, one should consider the type of problems encountered in the art, the prior solutions to those problems found in the prior art references, the rapidity with which innovations are made, the sophistication of the technology, the level of education of active workers in the field, and my own experience working with those of skill in the art at the time of the invention.

16. In this case, Dr. Litz has asserted in his declaration that a person of ordinary skill in the art as of the time of the '183 patent would have had "at least a Bachelor of Science degree in electrical engineering, or an equivalent field, and at least three years of experience with SSDs or other flash memory devices." Ex. 1003 [Litz-Decl.] ¶ 43. Petitioner adds that "[m]ore education can supplement practical experience and vice versa." Pet., 6.

17. For the purposes of this declaration, I accept Dr. Litz's proposed qualifications of a POSITA as further qualified by Petitioner. I exceed this skill level and thus, by Petitioner's terms, I have the "qualification and experience necessary to assess the '183 patent based on the perspective of a POSA." Pet., 6. I reserve the right to revisit the issue of the level of knowledge of the POSITA should the Petition be instituted.

18. As further discussed below, my opinions as stated in this declaration are valid even if the Board adopts a somewhat higher or somewhat lower level of ordinary skill in the art than proposed. For example, as will be discussed throughout my report, even a person with the level of knowledge or experience described by Dr. Litz or adopted by the Board as described above would not have a reasonable expectation of success in implementing certain aspects of the proposed combination as of the priority date of the '183 patent.

19. In this report, the absence of an expressed opinion about any section or paragraph of the Petition or Dr. Litz's declaration, does not indicate my agreement with the section or paragraph.

B. My Understanding Of Legal Standards

20. When considering the '183 patent and stating my opinions, I rely on the following legal standards as described to me by the attorneys for Radian.

21. I understand that a patent claim is unpatentable if the claimed invention was anticipated by a prior art reference or would have been obvious to a person of ordinary skill in the art at the time of the purported invention.

22. I understand that anticipation requires that every limitation of the claim at issue be disclosed, either expressly or under principles of inherency, in a single prior art reference.

23. I understand that inherency may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. Instead, it must be proven that the claim limitation not expressly found in the reference necessarily follows from what is found there.

24. I understand that an obviousness analysis involves comparing a claim to the prior art to determine whether the claimed invention would have been obvious to a person of ordinary skill in the art at the time of the invention in view of the prior art and in light of the general knowledge in the art as a whole. I also understand that obviousness is ultimately a legal conclusion based on underlying facts of four general types, all of which must be considered: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) any objective indicia of non-obviousness.

25. I also understand that obviousness may be established under certain circumstances by combining or modifying the teachings of the prior art. Specific teachings, suggestions, or motivations to combine any first prior art reference with a second prior art reference can be explicit or implicit, but must have existed before the date of purported invention. I understand that prior art references themselves may be one source of a specific teaching or suggestion to combine features of the prior art, but that such suggestions or motivations to combine art may come from the knowledge that a person of ordinary skill in the art would have had.

26. I understand that a reference may be relied upon for all that it teaches, including uses beyond its primary purpose, but also including teachings that lead away from the invention. I understand that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, although the mere disclosure of alternative designs does not teach away.

27. I further understand that whether there is a reasonable expectation of success in combining references in a particular way is also relevant to the analysis.

28. I understand that it is improper to use hindsight to combine references or elements of references to reconstruct the invention using the claims as a guide. My analysis of the prior art is made from the perspective of a person of ordinary skill in the art at the time of the invention.

29. I am not offering any legal opinions in this declaration nor am I qualified to do so. I only consider such legal standards in framing my opinions and conclusions as well as placing assertions made by Petitioner in the Petition into the proper context. Additionally, from a subject matter perspective, I understand that the petitioner always has the burden of persuasion regarding a challenge of patentability of an invention under an inter partes review.

V. CLAIMS AND GROUNDS AT ISSUE

30. I understand that Petitioner has challenged the claims of the '183 patent as follows (Pet., 1):

- Claims 1, 2, 8, 10-14, 18, 20 based on obviousness over Ellis and Son (Ground I);
- Claims 6, 9, 17, 19 based on obviousness over Ellis, Son, and Yamada (Ground II);
- Claims 1, 2, 8, 10-14, 18, 20 based on obviousness over Sinclair, Yu, and Son (Ground III);
- Claims 6, 9, 17, 19 based on obviousness over Sinclair, Yu, Son, and Jung (Ground IV).

VI. OPINIONS

A. Petitioner's Ellis Combinations

31. I have reviewed Petitioner's Grounds I-II, which rely upon the combination of Ellis and Son. Pet. 6-41.

32. I understand that Petitioner's Ground II challenges dependent claims only, and incorporates Petitioner's Ground I (without modification) for all aspects of the underlying independent claims. *See, e.g.*, Pet., 34 (incorporating Petitioner's challenge to dependent claim 2 in Ground I into Ground II's challenge to claim 6), 37 (incorporating Petitioner's challenge to claim 1 in Ground I into Ground II's

challenge to claim 9); 41 (similar for the remaining Ground II challenges). Similarly, all of Petitioner's Ground I challenges incorporate Petitioner's Ground I challenge to claim 1 without modification. *See, e.g.*, Pet., 30 (claim 13 incorporating claim 1 argument); *see also, e.g.*, Pet. 30 (challenging dependent claims 14, 18, and 20 simply by reference to claims 2, 8, and 10), 22, 25, 26 (challenging claims 2, 8, and 10, which depend from claim 1, by incorporating and assuming the validity of Petitioner's challenge to claim 1). For these reasons, I focus on Petitioner's Ground I challenge to independent claim 1.

1. Petitioner Does Not Show A Motivation To Combine.

33. Petitioner argues that “a POSA would have been motivated to incorporate Son's teaching regarding (i) additional forms of superblock metadata and (ii) the sharing of superblock metadata with a host for purposes of memory management” into Ellis, Pet., 9, or “to combine Son's host functionality with the system described in Ellis.” Pet., 10. I do not agree.

34. Indeed, because Petitioner largely describes its combination in the context of individual claim limitations (and not a single coherent system), it is difficult to discern exactly what Petitioner is arguing that a POSITA would be motivated to do.

35. In one instance, for example, Petitioner relies upon “additional forms of superblock metadata” from Son for an argument that its combination of Ellis and

Son teaches the claimed memory controller with logic to receive the claimed “write request.” *See* Pet., 14-15. In doing so, Petitioner blends characteristics of Ellis’s “host system,” Son’s “SSD module,” and the controllers that these systems employ, without fully addressing which responsibilities would be undertaken by which elements of its combination.

36. Petitioner cites disclosures relating to Son’s “SSD module,” for example, but never states that its combination would contain a copy of both Ellis’s “host system” and a copy of Son’s “SSD module” within its “host”—or that functionalities performed by Ellis’s controller in Ellis’s system would be entirely replaced by functionalities inspired by Son’s “SSD module” in Petitioner’s combination. And in suggesting, for example, that a POSITA would be motivated by to add “additional types of metadata” to Ellis, Pet., 14, does not by itself address *which* functions of Ellis would be retained in the combined system, and which would be modified in view of Son.

37. Petitioner makes various arguments about the alleged motivation for its combination of Ellis and Son in connection with the claimed “logic to send the host the information indicating extent of page utilization,” Pet., 16-17, and the claimed “logic to receive an erasure request from the host.” Pet., 18. In both situations, it is apparent to Petitioner that Ellis’s system does not disclose a controller with a host that satisfies these limitations. In this situation, Petitioner repeatedly cites the

following disclosure in Ellis in support of its argument that it would nevertheless be obvious to modify aspects of Ellis:

The functional units in the memory controller 104 can work individually and independently of the other functional units. For illustrative purposes, the memory controller 104 is described by operation of the memory controller 104 with the host system 108 and the memory array 106. ***It is understood that the memory controller 104, the host system 108, and the memory array 106 can operate any of the modules and functions of the memory controller 104.***

Ex. 1004 [Ellis] 4:58-65; *see* Pet. 17, 18 (citing this disclosure in connection with claim limitations); *see also* Pet. 10, 33 (citing this disclosure in connection with motivation to combine).

38. I understand that the same passage appears verbatim, or near verbatim, in a number of other patents filed by the same entity that filed Ellis.¹ A POSITA

¹ *See, e.g.*, Ex. 2021 [U.S. Patent No. 8,949,689] 4:32-39; Ex. 2022 [U.S. Patent No. 9,021,231] 4:60-67; Ex. 2023 [U.S. Patent No. 9,098,399] 4:66-5:6; Ex. 2024 [U.S. Patent No. 9,123,445] 4:43-49; Ex. 2025 [U.S. Patent No. 9,170,941] 9:29-37; Ex. 2026 [U.S. Patent No. 9,183,137] 4:58-65; Ex. 2027 [U.S. Patent No. 9,244,519] 6:41-49; Ex. 2028 [U.S. Patent No. 9,543,025] 6:3-10; Ex. 2029 [U.S. Patent No. 9,671,962] 4:58-65; Ex. 2030 [U.S. Patent No. 10,546,648] 4:49-56.

would recognize this type of statement as the kind of language that is commonly used in patent applications to indicate that a patent disclosure is not necessarily limited to the specifics of the examples that it discusses. This statement does suggest that any particular modification of the system expressly disclosed in Ellis would be desirable. In particular, this passage does not motivate Petitioner's proposed modifications of Ellis with Son.

39. A POSITA would understand that in any functioning system of flash management, architectural choices relating the roles of host and controller are not made arbitrarily, and these choices are not made arbitrarily in Ellis or in Son. This background knowledge of the POSITA is also reflected in claims of the '183 patent, which recite functionalities of the claimed "memory controller" and "host," and specific interchanges of information between them, at length. *See, e.g.*, Ex. 1001 ['183] cl. 1. And Ellis and Son are very different in how they assign responsibilities between a memory controller and a host.

40. Ellis expressly places almost all of the work of flash management—*e.g.*, directing logical read and write operations to specific physical units of memory, managing erase operations, and performing maintenance tasks such as wear leveling and garbage collection—within Ellis's "controller." *See, e.g.*, Ex. 1004 [Ellis] 15:45-50 (describing "logical-to-physical mapping" being "performed by the block control module 306" within Ellis's memory controller); 4:66-5:3 (locating the "block

control module 306” and “memory access module 308” within Ellis’s memory controller); 11:58-62 (locating a “program-erase count” within the “block control module 306” within Ellis’s memory controller); 12:51-55 (locating “recycling operations” within the “memory access module 308” within Ellis’s memory controller), 14:21-24 (locating “remapping of . . . unusable blocks” within the “memory access module” within Ellis’s memory controller).

41. Son expressly assigns the management of similar tasks to a component called an “SSD module,” in what Petitioner occasionally identifies as a “host” in Son. *See, e.g.*, Ex. 1005 [Son] [0039] (locating “a wear count” in Son’s “superblock table 350”), [0033] (describing Son’s superblock table within “management data structures maintained by an SSD module”), [0038] (describing “an FLBA to PLBA mapping table” among the structures maintained by its “SSD module”); *see also* Pet. 17 (locating the “SSD module” inside what Petitioner describes as a “host” in Son), 19 (referring to the “SSD module [(host)]”) (parentheses in original).

42. A POSITA would recognize that Ellis and Son are not merely alternative ways of allocating responsibility for flash management, but potentially conflicting architectures. In any practical system, many of the design choices made in Ellis and Son would be mutually exclusive: a system that handles garbage collection, wear leveling, and other flash-specific processes within its controller (as

in Ellis) generally would not *also* expose those aspects for direct handling by software on a host (as in Son), for example.

43. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown that a POSITA would have been motivated to combine Ellis and Son as Petitioner proposes.

2. Petitioner Does Not Show That Its Ellis Combinations Render Obvious “logic to receive a write request from a host via the host interface, the write request accompanied by an address that designates a specific one of the subdivisions.”

44. Claim 1 requires a “*memory controller* comprising ... logic to receive a write request from a *host* via the *host interface*, the write request accompanied by an address that designates a specific one of the subdivisions.” Petitioner identifies Ellis’s controller as the claimed “memory controller,” Ellis’s “host interface” as the claimed “host interface,” and Ellis’s “host system” as the claimed “host.” *See, e.g.,* Pet., 14; *see also* Pet., 12-13. Petitioner argues that Ellis teaches this limitation, and that Son does. I do not agree with either argument.

- a) *Ellis Does Not Disclose Or Render Obvious A Write Request “from a host . . . accompanied by an address that designates a specific one of the subdivisions.”*

45. Again, Petitioner identifies Ellis’s host system as the claimed “host,” and Ellis’s controller as the claimed “memory controller.” Petitioner also identifies a write request in Ellis as the claimed “write request,” with Ellis’s “super blocks” as

the claimed “subdivisions.” Pet., 14-15. For the claimed “address that designates a specific one of the subdivisions,” Petitioner identifies “super block identification (ID) values” described in Ellis. *See, e.g.*, Pet. 14-15 (quoting Ex. 1004 [Ellis] 10:27-32).

46. Petitioner argues that a “write address [in Ellis] *necessarily must* identify or reference a superblock ID value” (*i.e.*, what Petitioner identifies as an “address that designates a specific one of the subdivisions”). Pet., 14-15.

47. The claim, of course, does not recite a write request *identifying* or *referencing* a specific one of the subdivisions, but “a write request from a host . . . the write request *accompanied by* an address that designates a specific one of the subdivisions.” Petitioner’s cited disclosures do not show any write request from Ellis host system to be *accompanied by* any “superblock ID value.”

48. In a portion of Ellis that Petitioner cites in support of its argument, Ellis states that “Actions including host writes, recycling operations, or erasing of blocks can be performed on a set of the erase blocks 408 included within one of the super blocks 502 as a single unit,” Ex. 1004 [Ellis] 8:4-7; *see also* Pet., 14 (citing Ex. 1004 [Ellis] 7:64-8:7). But I do not see how this disclosure supports Petitioner’s point. When Ellis says that actions “can be performed on a set of erase blocks . . . as a single unit,” this does not specify *how* these actions are performed; in particular, this

does not disclose any specifics about the structure of a write request from Ellis's host to Ellis's controller.

49. Petitioner's argument rests on a statement that a "write address" in Ellis "necessarily must identify or reference a superblock ID value," Pet., 14-15—a contention that Petitioner follows with the bracketed claim language "accompanied by an address that designates a specific one of the subdivisions." Pet., 14-15.

50. The argument implied by this juxtaposition—that a POSITA would understand that a write request from the host in Ellis *necessarily must* be "accompanied by" a superblock ID value, because the request may ultimately result in a write operation that identifies or references specific superblocks—is not true. A POSITA would understand, for example, that a write request received by Ellis's controller from Ellis's host could be directed to a range of *logical* addresses, with Ellis's controller tasked with converting logical addresses to physical addresses upon receipt of the request. These logical addresses may not correspond to any physical addresses when the request is received by the controller. In such a situation, any relevant superblock ID values would be identified at the controller only *after* the request was received from the host and physical addresses were assigned by Ellis's controller as a part of carrying out the request. A POSITA would not understand such a write request to have been "accompanied by" something that Ellis's controller only generates after it has received that request.

51. This difference—host write requests contain logical addresses, not superblock IDs—is perhaps obscured by Petitioner’s ambiguous phrase ‘write address,’ Pet., 14—a phrase that invites confusion between logical and physical addresses, and hence confusion between what the alleged “write request from [the] host” in Ellis is “accompanied by,” on the one hand, and what Ellis’s controller might later create or identify, on the other.

52. Ellis contains many disclosures suggesting that its “host system” would be unaware of any “superblock ID values” associated with the data it is storing. Ellis expressly refers to “superblock ID values” (among other examples of “metadata” maintained in Ellis’s system) as “non-host related information.” Ex. 1004 [Ellis] 10:21-32. Ellis describes its “metadata” (which includes “superblock ID values”) as stored on its controller, and as managed by the “block control module 306,” which is a component of Ellis’s controller. *Id.*, 10:3-20, 4:67-5:3. Ellis describes a “logical-to-physical (L2P) tabling system within the runtime volatile memory” of its controller, *id.*, 12:3-14, 3:39-42, 4:4-8 (locating volatile memory within Ellis’s controller), and “logical-to-physical mapping of ... host data within the memory devices 110” as “non-host related information” stored on its controller. *Id.* 10:25-27. Ellis states, *specifically in connection with a host sending a write request to its controller*, that “The host system 108 can request the memory controller 104 for reading, writing, and deleting data from or to *a logical address space* of a storage

device or the memory sub-system 102 that includes the memory array 106,” Ex. 1004 [Ellis] 3:25-28.

53. From these and many other disclosures in Ellis, a POSITA would understand write requests originating in Ellis’s host would specify, at most, logical addresses that indicate locations in the host’s logical address space (*e.g.*, addresses corresponding to a file-system or OS-level views of storage, not physical locations in flash memory). A POSITA would understand Ellis’s super block “ID values,” by contrast, specify physical locations in flash memory. To the extent that such “ID values” are used at all in handling a write request in Ellis’s system, they would be generated at Ellis’s controller. Ellis’s controller is the component in Ellis’s system tasked with translating logical addresses to physical ones, and with assigning physical addresses for logical addresses that have not previously been written to.

54. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown that Ellis teaches the claimed “logic to receive a write request from a host”

- b) *Son Does Not Render Obvious A Write Request “from a host . . . accompanied by an address that designates a specific one of the subdivisions” In Petitioner’s Combination.*

55. In arguing that its combination teaches a write request “from a host . . . accompanied by an address that designates a specific one of the subdivisions,”

Petitioner separately argues that “[t]o the extent Ellis does not teach this limitation, a POSA would be motivated to combine its teaching with Son.” Pet., 15.

56. Pointing to “write requests” in Son’s system, Petitioner states that “write requests [*in Son*] include an assigned file system logical block address (‘FLBA’) which is associated with a ‘superblock address.’” *Id.* (quoting Son). But Petitioner does not relate this disclosure about write requests *in Son’s system* to write requests received by the “memory controller” in its combination. Petitioner generally suggests that the controller in its combination is a modified version of the controller in Ellis. *See, e.g.*, Pet., 10 (describing the combination as “incorporat[ing] the additional forms of superblock metadata described in Son into the system described in Ellis” and “combin[ing] Son’s host functionality with the system described in Ellis”). Petitioner does not connect how Son’s FLBA being “associated with” a “superblock address” in Son would teach that a write request to the controller in its modified system would be “accompanied by” a superblock ID value.

57. Petitioner’s reference to “combin[ing] Son’s host functionality with the system described in Ellis,” Pet., 10, does not inform the POSITA of how write requests would be structured in the combined system. Petitioner suggests that they would “incorporate the additional forms of superblock metadata described in Son,” Pet., 10, and because write requests from Ellis’s host to Ellis’s unmodified controller are not accompanied by “super block ID values,” presumably Petitioner is proposing

that these “additional forms of superblock metadata” would include super block ID values. Yet Petitioner also points to Son and notes that “Son teaches a ‘write request’ accompanied by an FLBA designating a superblock address.” Pet., 15. In Son, “FLBAs” only “designate” superblock addresses in the sense that “mapping tables” at Son’s SSD module associate them with superblock addresses. *See, e.g.*, Ex. 1005 [Son], ¶¶ [0038] (noting that a “mapping table” in Son’s Figure 3B “associates each FLBA ... with a super block address”), [0034] (locating the mapping tables at Son’s “SSD module”). Petitioner does not argue or show that these mapping tables are on the host in its combination.

58. Petitioner’s analogy to Son’s FLBAs thus presents the same problem as Petitioner’s argument about Ellis. While Petitioner describes the combination of Ellis and Son at a high level, in terms of adding “additional forms of superblock metadata” and “the sharing of superblock metadata with a host” to Ellis, *see* Pet., 9-11, this does not say that Son’s “mapping tables” (or Ellis’s logical-to-physical mapping functionality) would exist on the host of the combined system. In the absence of such a modification, in the combined system, a write request from the host would presumably still be resolved to a “superblock ID value” at the controller, as it is in Ellis.

59. If Petitioner is proposing to augment the host in the combined system with the logical-to-physical mapping *function* of Son’s SSD module—a proposal

that is far from clear in Petitioner’s vague reference to adding “additional forms of superblock *metadata* described in Son” to the host system of Ellis, Pet., 10—then Petitioner does not explain how or whether the memory controller in Ellis, which *also* maintains logical-to-physical mapping information (and which Ellis also refers to as “metadata,” Ex. 1004 [Ellis] 10:21-27), would be modified as to be compatible with this new host functionality.

60. It does not appear, for example, that Petitioner proposes that Ellis’s controller plays *no* role in managing Son’s “superblock metadata” (whether Ellis’s or Son’s) in Petitioner’s combination. In connection with other claim limitations, for example, Petitioner argues that because “in Ellis, the superblock metadata is updated by the controller,” that “[i]n the combined system *the additional superblock metadata described in Son* would also be updated by the controller.” Pet., 15. Yet in Son, it is Son’s SSD module—not Son’s memory controller, and not a component that Petitioner analogizes to any controller in the combination—that is tasked with updating Son’s superblock-level metadata. *See, e.g.*, Ex. 1005 [Son] [0050]-[0055] (describing Son’s “SSD module” as updating various mapping tables, including how to “associate the FLBA [of a write operation] with [a] newly selected PLBA,” during a write operation). Petitioner does not indicate how these distinct approaches would be reconciled.

61. In any event, a POSITA would recognize a change of this sort to represent a fundamental change in the operating principles of the system—with implications far beyond simply what “metadata” accompanies a write request. As one example, a POSITA would recognize that if a host and a memory controller were **both** maintaining logical-to-physical addressing information for the same memory, the system would need some way of synchronizing their activity (*e.g.*, to avoid the host and controller potentially operating upon different logical-to-physical mappings for the same memory). Designing, specifying, and validating that mechanism would be a substantial undertaking, potentially impacting not just the “metadata” exchanged between components, but the command set used by the host, on-media data structures in both components, and scheduling policies in both components. A POSITA would not view such a hybrid system as a minor variant of a host-centric system like Son or a controller-centric system like Ellis.

62. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown that their proposed Ellis combinations render obvious “logic to receive a write request from a host via the host interface, the write request accompanied by an address that designates a specific one of the subdivisions.”

3. Petitioner Does Not Show That Its Ellis Combinations Render Obvious “logic to send the host the information indicating extent of page utilization of the specific one of the subdivisions and an address corresponding to the specific one of the subdivisions.”

63. Claim 1 additionally requires “logic to send the host the information *indicating extent of page utilization* of the specific one of the subdivisions and an address corresponding to the specific one of the subdivisions.”

64. Petitioner identifies Ellis’s “host system” as the claimed “host” and asserts that Ellis’s disclosure of “control or status information” sent from the controller to the host encompasses the sending of superblock-level metadata, including valid page counts. *See, e.g.,* Pet., 14 (citing Ex. 1004 [Ellis] 4:46-50 in identifying the “host interface” in Ellis with the claimed host interface, and the “host system” in Ellis with the claimed “host”), *id.* (citing Ex. 1004 [Ellis] 14:25-34 for a “write operation . . . for host write data from the host system 108” in connection with the claimed “write request from a host”); *id.*, 16 (arguing that Ellis discloses sending “valid page count” statistics for a single “super block” to Ellis’s “host system”).

65. As I will discuss in further detail below, Ellis does not disclose transmitting superblock-specific metadata (let alone valid-page counts) to its host system. Similarly, while Petitioner attempts to supplement Ellis by citing the operation of Son’s “SSD module,” Petitioner ignores that in Son, the “SSD module” *itself* generates and updates the information that Petitioner says a host would request

from a controller in its combination. Without further information about Petitioner's proposed combination, it is unclear how Petitioner's combination would operate as to satisfy the limitation. For these reasons, in my opinion the limitation is not shown.

- a) *Ellis Does Not Disclose Or Render Obvious Sending "information indicating extent of page utilization of [a] specific one of [its] subdivisions" To The Alleged "host" In Petitioner's Combinations.*

66. Ellis states that its controller may send "control or status information generated by the memory controller 104 to the host system 108." Ex. 1004 [Ellis] 4:51-53. Citing this disclosure, Petitioner argues that "Ellis therefore teaches 'logic to send the host [] information.'" Pet., 16. To further argue that Ellis teaches "information *indicating extent of page utilization* of [a] specific one of the subdivisions," Petitioner points to "NAND statistics" maintained for individual "super blocks" in Ellis by Ellis's memory controller. Pet., 16.

67. Ellis's memory controller is not what Petitioner identifies as a "host." Ellis does not disclose that its "NAND statistics" are shared with Ellis's host system, Ellis does not disclose any reason why its memory controller would share these statistics with its host system.

68. To address this issue, Petitioner points to a disclosure in Ellis of "control and status information" being sent to its host system. Petitioner and Dr.

Litz argue that this “control and status information” includes NAND statistics. Pet., 16. I do not agree.

69. Ellis nowhere discloses *any* transmission of “super block”-level information from Ellis’s memory controller to Ellis’s “host system.” Ellis does not disclose transmitting such information as part of Ellis’s “control and status information” (as Petitioner argues, Pet., 16), and Ellis does not disclose transmitting such information as part of any other communication from Ellis’s controller to Ellis’s host system. In particular, Ellis nowhere discloses sending “valid page count” statistics for a single “super block” to Ellis’s “host system” (as Petitioner argues, Pet., 16).

70. A POSITA would also recognize that Ellis nowhere discloses any action taken by its host system that would require or even advantageously be able to use “valid page count” statistics for a single “super block.” Such statistics, for example, might be relevant to garbage collection operations, but Ellis’s host is not involved in managing garbage collection in Ellis. Petitioner does not identify any function of Ellis’s unmodified host that would use this information.

71. Petitioner argues that “Ellis teaches that the control and status information” (which Ellis describes its controller sending to its host at 4:51-53) “is stored as metadata.” Pet., 16. But the cited disclosure in Ellis does not say this. Ellis nowhere refers to its “control and status information” as “metadata,” or

suggests that its “control and status information” includes “metadata.” Ellis expressly and repeatedly describes “metadata” as “*non-host related* information,” *see, e.g.*, Ex. 1004 [Ellis] 10:21, 10:25, 10:28, and a POSITA would recognize from these disclosures that Ellis’s “metadata”—a category that includes the “NAND statistics” identified by Petitioner, Pet., 16—is *not* sent to Ellis’s “host system.”

72. Ellis describes “logical-to-physical mapping information of the host data within the memory devices 110” as an example of “metadata,” for example, and a POSITA would understand that this information is exclusively maintained by the controller in Ellis, and is not sent to Ellis’s “host system.” Ellis’s other examples of “metadata,” such as “logical block address (LBA) information, [and] super block identification (ID) values” cited by Petitioner (Pet., 16-17), are also not sent to Ellis’s “host system.”

73. Petitioner nevertheless refers to these examples as “stored ‘control and status’ metadata *sent to the host*.” Pet., 16 (citing Ex. 1004 [Ellis] 10:27-32, 12:26-41). Again, however, this is not what Ellis says. The cited portions of Ellis only show that refers to LBA information and super block identification values as examples of “metadata.” Ellis nowhere describes this information as “‘control and status’ metadata,” and Ellis nowhere describes anything else as “control and status metadata.” Similarly, Ellis nowhere says that any of what it describes as “metadata” is, as Petitioner states here, “sent to the host” (Pet., 16).

74. Petitioner states that “Ellis describes instances where the controller sends the host ‘metadata’ showing the ‘valid state of data stored within the one of the superblocks.’” Pet., 16 (quoting Ex. 1004 [Ellis] 12:34-37). I do not agree. The portion of Ellis cited by Petitioner states in full:

During portions of drive operations such as but not limited to drive initialization, the metadata pages 508 can be used to restore a host logical to physical mapping of data and a valid state of data stored within the one of the super blocks 502.

Ex. 1004 [Ellis] 12:34-37.

75. This disclosure does not teach sending Ellis’s “metadata” to Ellis’s “host.” A POSITA would understand Ellis’s reference to the use of the “metadata pages 508” to “restore a host logical to physical mapping” to refer to operations that take place entirely within Ellis’s controller, where Ellis stores its logical-to-physical mapping information. Ex. 1004 [Ellis] 10:24-27 (referring to “logical-to-physical mapping information of the host data within the memory devices” as “non-host related information”). Ellis discloses no reason why updating or “restor[ing]” this information would involve, let alone require, sending any of this information to Ellis’s host.

76. A POSITA would understand Ellis’s “control and status information” to include summary information appropriate for a host system that is not itself

responsible for flash management. Such information could potentially include high-level endurance statistics, such as an estimated life left computed from program/erase cycle totals or averages, high-level error statistics (e.g. read error counts), temperature alerts, and the like.

77. What such exemplary types of information have in common is that they relate to the “control and status” of the *drive as a whole*, not to the management of individual “super blocks.” At the time of the invention, the exposure of drive-level summary information to the host was common in systems that, like Ellis, delegated most of the responsibility for flash management to the memory controller. But there would be no reason for a memory controller in such a system to report information at finer levels of granularity to the host, because the host in such a system—not being tasked with flash management—has no use for such information.

78. For at least these reasons, in my opinion, Petitioner and Dr. Litz do not show that Ellis teaches the claimed “logic to send the host the information indicating extent of page utilization.”

- b) *Son Does Not Render Obvious Sending “information indicating extent of page utilization of [a] specific one of [its] subdivisions” To The Alleged “host” In Petitioner’s Combinations.*

79. In another attempt to argue that its combination teaches sending the claimed “information indicating extent of page utilization,” Petitioner identifies

disclosures in Son suggesting that Son's "SSD module" may query Son's "controller" for information such as "the number of free, valid and/or invalid pages in each candidate superblock" in Son. *See, e.g.,* Pet., 17-18 (quoting, e.g., Ex.1005 [Son] [0047]).

80. By describing disclosures about Son's "SSD module" as if they are teachings about the claimed "host," *see, e.g.,* Pet., 17 ("Son teaches that the SSD is managed by a host which is comprised of an 'SSD module'"), *Id.* ("Son teaches that the host may acquire superblock metadata stored in flash memory"), 18 ("The host may query page utilization"), Petitioner appears to regard the "host system" of Ellis as interchangeable with the "SSD module" of Son. But a POSITA would not generally recognize the capabilities of Son's "SSD module" to be interchangeable with those of Ellis's "host system."

81. As one example, Petitioner argues that Son's "SSD module" might require "information indicating the extent of page utilization" "in order to perform operations such as 'garbage collection and wear leveling'" in Son. Pet., 18 (quoting Ex. 1005 [Son] [0017]). As Petitioner recognizes, however, garbage collection and wear leveling in Son are performed by Son's "SSD module." In Ellis, by contrast, garbage collection and wear leveling are performed by Ellis's **controller**, and not by Ellis's "host system."

82. A POSITA would generally recognize that a flash memory system such as Ellis would perform garbage collection and wear leveling—a point that Petitioner’s expert would appear to acknowledge, *see, e.g.*, Ex. 1003 [Litz-Decl.] ¶ 33 (describing garbage collection in section entitled “Technology Background and State of the Art” as a feature of managing solid-state drives), 35 (in the same section, describing wear leveling as “essential” in flash management). And Ellis expressly discloses, for example, that its controller keeps track of numbers of valid pages, program/erase cycles, and the like—inputs that a POSITA would understand to be important to garbage collection or wear leveling (again, as Petitioner’s expert generally acknowledges; *see* Ex. 1003 [Litz-Decl.] ¶¶ 33-34 (describing the general role of “valid blocks” in garbage collection), 35 (discussing the limited number of P/E cycles in connection with wear leveling)).

83. Although Ellis does not employ the term “garbage collection,” Ellis expressly describes its “memory access module” (which resides within Ellis’s controller, Ex. 1004 [Ellis] 4:67-5:3) as performing “recycle operations” for reasons “including freeing space and wear leveling,” Ex. 1004 [Ellis] 16:4-13), and a POSITA would recognize that garbage collection involves “freeing space.” Because Ellis never discloses any role for its host system in performing such operations (or in accessing or updating any of the relevant inputs), a POSITA would understand

that flash garbage collection and wear leveling operations in Ellis are performed exclusively by Ellis's controller, without involvement of Ellis's host.

84. Thus, Petitioner's supposed inspiration for sending "information indicating extent of page utilization" to the host in the combination is information that Ellis's "host system" plays no role in receiving or using.

85. Petitioner does not propose that the modified Ellis host in its combination would entirely take over garbage collection and wear leveling operations in the combination. Petitioner states only that Son teaches "the benefit of *sharing information* with the host in order to perform memory management functions," Pet., 17.

86. It is unclear whether Petitioner suggests that the modified host would perform garbage collection and wear leveling. This type of modification is arguably hinted at by Petitioner's argument that Son's use of data relevant to garbage collection and wear leveling teaches "send[ing] the host the information indicating extent of page utilization" in the combined system. But Petitioner does not expressly identify this (or anything else) as a reason for sending this information to the host in the combined system.

87. If Petitioner were to propose that Ellis's modified host either share or completely take over garbage collection or wear leveling responsibilities in the combination, this would not be a minor modification of Ellis. Such a modification

would go far beyond simply what types of “metadata” exist in Ellis’s system. A POSITA would recognize such an expansion of the role of Ellis’s host to raise other unanswered questions of system design. Petitioner does not address, for example, what would happen with garbage collection and wear leveling *as already performed in Ellis’s controller* in the combination. (If Petitioner were proposing that the modified Ellis host would exclusively manage these operations, for example, Petitioner does not explain why Ellis’s controller would still be tasked with managing and updating the inputs to these operations, if its only role in these operations is to send that information to the host.)

88. For at least these reasons, in my opinion, Petitioner and Dr. Litz do not show that its Ellis combinations teach sending the host the claimed “information indicating extent of page utilization.”

4. Petitioner Does Not Show That Its Ellis Combinations Render Obvious “an erasure request from the host . . . the erasure request accompanied by the address corresponding to the specific one of the subdivisions” (Grounds I-II, All Challenged Claims).

89. Claim 1 additionally requires “an erasure request from the host ... the erasure request accompanied by the address corresponding to the specific one of the subdivisions.” In my opinion, Petitioner does not show that this limitation is taught by its Ellis combinations.

- a) *Petitioner Does Not Show “an erasure request from [a] host . . . the erasure request accompanied by the address corresponding to the specific one of the subdivisions” In Ellis.*

90. Petitioner argues that “Ellis teaches that ***the host or controller*** may request ‘erasing of blocks . . . within one of the super blocks 502 as a single unit.’” Pet., 18 (quoting Ex. 1004 [Ellis] 8:2-7 and citing Ex. 1004 [Ellis] 4:58-65). I do not agree with Petitioner.

91. Ellis does disclose that sets of erase blocks in “super blocks” of its system may be managed “as a single unit.” *See, e.g.*, Ex. 1004 [Ellis] 8:4-7 (“Actions including host writes, recycling operations, or erasing of blocks can be performed on a set of the erase blocks 408 included within one of the super blocks 502 as a single unit”). But this disclosure does not say that Ellis’s ***host*** issues requests to erase specific blocks or super blocks.

92. Petitioner’s use of the phrase “host or controller” does not derive from any disclosure of Ellis’s host system initiating erase requests (let alone such a request “accompanied by” what Petitioner identifies as an “address corresponding to the specific one of the subdivisions”). In arguing that “Ellis teaches that ***the host or controller*** may request ‘erasing of blocks . . . ,’” Pet., 18, Petitioner is quoting from a disclosure about Ellis’s ***controller only***. For the “host” aspect of its assertion, Petitioner appears to be relying upon Ellis’s column 4 disclosure (previously

discussed in Section VI.A.1) to interpret a disclosure about Ellis's controller as a teaching about Ellis's host.

93. Again, however, Ellis's column 4 disclosure states generally "that the memory controller 104, the host system 108, and the memory array 106 can operate any of the modules and functions of the memory controller 104." Ex. 1004 [Ellis] 4:58-65. This high-level language does not say anything specific about host-issued erase requests.

94. Petitioner further argues that "Ellis teaches host erase requests may be sent, via the 'host interface,' to the 'memory controller,' which has 'logic' to process those commands." Pet., 18. Again, however, Petitioner does not identify any host-initiated erase operations in Ellis. The phrase "host erase request" does not appear in Ellis, and the cited disclosures concern only general aspects of Ellis's system—not erase requests, let alone "host erase requests." *Compare* Pet., 18 (citing Ex. 1004 [Ellis] 4:46-50, 3:38-45, 20:40-44) *with* Ex. 1004 [Ellis] 4:46-50 ("The host interface unit 208 allows the host system 108 of FIG. 1 to interface and interact with the memory controller 104. The host interface unit 208 can include a host interface 218 to provide communication mechanism between the host interface unit 208 and the host system 108"), 3:38-45 (describing Ellis's Figure 2, an "exemplary hardware block diagram of the memory controller 104"), 20:40-44 ("Functions or operations of the memory controller 104 as described above can be implemented with the

control unit 202 of FIG. 2, the storage unit 204 of FIG. 2, the memory interface unit 206 of FIG. 2, the host interface unit 208 of FIG. 2, or a combination thereof”²).

95. For at least these reasons, in my opinion, Petitioner and Dr. Litz do not show how Ellis discloses or renders obvious “an erasure request from the host” in Petitioner’s combination.

b) *Petitioner Does Not Show That Any “erasure request from [a] host” Assumed To Exist In Ellis Would Be “accompanied by [an] address corresponding to the specific one of the subdivisions.”*

96. Assuming for the sake of argument that Ellis teaches host-initiated erase requests (which Petitioner has not established), Petitioner does not show that such a request would be “**accompanied by** the address corresponding to the specific one of the subdivisions” (which Petitioner identifies as a “super block ID value” in Ellis). Pet., 19 (emphasis in original).

97. Petitioner states that “[a] POSITA would understand that, for erasures to be carried out on a superblock as a single unit, the erasure request **must** be

² Each of the components 202, 204, 206, and 208 of Figure 2 is contained within Ellis’s memory controller. *See, e.g.*, Ex. 1004 [Ellis] 3:38-39 (“Referring now to FIG. 2, therein is shown an exemplary hardware block diagram of the memory controller 104.”)

accompanied by an address corresponding to ‘superblock ID value.’” Pet., 18-19. I do not agree.

98. When Ellis expressly discloses its “host system” requesting operations, Ellis speaks in terms of its host’s logical addressing, *see, e.g.*, Ex. 1004 [Ellis] 3:25-28 (“The host system 108 can request the memory controller 104 for reading, writing, and deleting data from or to *a logical address space* of a storage device or the memory sub-system 102 that includes the memory array 106”); *see also id.*, 5:21-23 (“The term ‘logical’ refers to *non-physical* and thus does not represent the physical configuration of the memory devices 110”), *cf. id.*, 7:65-66 (“The super blocks 502 are defined as groups of the erase blocks 408”), while it only speaks of “super block identification (ID) values,” as resident in data structures stored on and maintained by Ellis’s controller. *See id.*, 10:21-32.

99. A POSITA would understand that host requests in Ellis could have the ultimate effect of “super blocks” being erased as single units without the request itself being accompanied by any “superblock ID value” from Ellis’s host. A POSITA would recognize, for example, that if Ellis’s host were to send a hypothetical command to erase an entire drive, or to erase the contents of a given range of a logical addresses, such a request would have the ultimate effect of erasing superblocks even though it could be carried out without being accompanied by the superblock ID value of any superblock implicated by the request. A POSITA would

understand Ellis's controller to be capable of generating the superblock ID values relevant to such a request without the host providing them.

100. Ellis refers to its super block ID values as “non-host related information,” which a POSITA would recognize as a teaching that this information, though used internally by Ellis's controller, is not shared with Ellis's host. *See, e.g.,* Ex. 1004 [Ellis] 10:24-30. In particular, a POSITA would not understand Ellis to teach that its host necessarily has access to any super block ID values, let alone that its host necessarily sends any hypothetical erase command with an accompanying super block ID value.

c) *Son Does Not Render Obvious The Claimed “erasure request from [a] host” In Petitioner’s Combination.*

101. As an alternative argument for why its combinations teach the claimed “logic to receive an erasure request from a host,” Petitioner turns to Son for what Petitioner terms “additional implementation details for host initiated erase commands.” Pet., 19. Petitioner's arguments center upon disclosures relating to Son's “SSD module.” Pet., 19-20.

102. As discussed above, however, Petitioner does not explain why a POSITA would regard every capability of Son's “SSD module” as a capability of Ellis's “host system.” To the extent that Petitioner is arguing that Son's “SSD module” would satisfy any claim limitation in its combination that Ellis's “host

system” does not, *see, e.g.*, Pet., 19 (stating that in Son, “***the SSD module [(host)]*** initiates the deletion operation,” quoting Son at [0059]) (emphasis and parenthetical assertion in original), Petitioner does not supply enough information about how the combination would work to show why this would be the case.

103. Petitioner also does not explain why a host-initiated erase operation inspired by Son would be “accompanied by” what Petitioner appears to identify as an “address corresponding to ... [a] ... subdivision” in Son. Petitioner states that in Son, “‘the SSD module [(host)] initiates [a] deletion operation’ by issuing ‘an ‘explicit command ... in association with a particular FLBA,’ to the controller,” and that “[t]he delete command [in Son] with FLBA sent to the controller designates a ‘superblock address’ and a ‘PLBA,’” Pet., 19 (quoting Son), where Petitioner sets the term “superblock address” in boldface.

104. But as I observed above, Son’s “FLBAs” only resolve to superblock addresses in Son in the sense that tables in Son’s host-side SSD module associate them with superblock addresses. *See* Section VI.A.2.b)VI.A.2.b). In Ellis, the analogous functionality of logical-to-physical address translation occurs ***at the controller***. Without further specification of how Petitioner’s combination is supposed to operate, it is not clear how a host-initiated erase request inspired by Son’s “FLBAs” could be “accompanied by” a super block ID value.

105. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown has not shown that its Ellis combinations render obvious “an erasure request from the host . . . the erasure request accompanied by the address corresponding to the specific one of the subdivisions.”

B. Petitioner’s Sinclair Combinations

106. Petitioner’s Sinclair-based challenges rest on Petitioner’s analysis of claim 1 in view of its combination of Sinclair, Yu, and Son (“Ground III”). *See, e.g.*, Pet., 62, 66, 69 (Petitioner’s Ground IV challenges, to dependent claims only, incorporating Petitioner’s Ground III challenges to independent claims), 52, 55 (referring Petitioner’s Ground III arguments regarding dependent claims to Petitioner’s arguments regarding independent claim 1). Accordingly, I focus on Petitioner’s Ground III challenge to claim 1.

1. Petitioner Does Not Show A Motivation To Combine.

107. Petitioner never describes its combination of Sinclair, Son, and Yu in express terms. Petitioner states, for example, that “a POSA would incorporate Son’s teaching regarding implementation details for superblock metadata and commands, to the metablock metadata and commands in Sinclair.” Pet., 45. This does not specify which features of Son are incorporated into Sinclair, or how Sinclair is modified. The challenged claims, after all, do not recite abstract “metadata and commands,” of course; they recite a “memory controller,” and a “host,” and—across

multiple claim limitations—logic for various kinds of specific exchanges of information between these components, including

- “logic to receive a write request from a host via the host interface, the write request accompanied by an address that designates a specific one of the subdivisions,”
- “logic to send the host the information indicating extent of page utilization of the specific one of the subdivisions and an address corresponding to the specific one of the subdivisions,”
- “logic to receive an erasure request from the host, via the host interface, the erasure request accompanied by the address corresponding to the specific one of the subdivisions.”

108. Petitioner’s proposal to alter Sinclair’s with “details for superblock metadata and commands” is vague, and does not motivate any particular way of creating a combined system that satisfies the claim.

109. The question of how a POSITA would be motivated to form Petitioner’s Sinclair combinations is not answered by Petitioner repeatedly incorporating arguments about Ellis and Son by reference. *See, e.g.*, Pet., 47 (arguing that “To the extent Sinclair does not teach this limitation, a POSA would be motivated to incorporate the additional variants of superblock metadata disclosed in Son. As discussed for Ground I, Claim 1[c], Son teaches the claimed page utilization

metadata,” where “Ground I” is an Ellis ground). Petitioner also attempts to motivate its combination with Yu by reference. *See, e.g.,* Pet., 50 (arguing that “to apply the teaching of Yu to the combined system [of Sinclair and Son], a POSA would understand that the information sent by the controller to the host in connection with the S.M.A.R.T. command must include a superblock or metablock address, as described for Ground I, Claim 1[d]-[f],” where “Ground I” is an Ellis combination that does not include Sinclair or Yu). Such arguments do not address the differences between Sinclair and Ellis, let alone clarify exactly how Petitioner would propose to modify Sinclair by Son and Yu, or why a POSITA would be motivated to do so.

110. All of this makes it difficult to discern what Petitioner is proposing that a POSITA would be motivated to do. Accordingly, in my opinion, Petitioner and Dr. Litz have not shown that a POSITA would be motivated to modify Sinclair in the way proposed by Petitioner.

2. Petitioner Does Not Show That Its Sinclair Combinations Render Obvious “logic to receive a write request from a host via the host interface, the write request accompanied by an address that designates a specific one of the subdivisions” (Grounds III-IV, All Challenged Claims).

111. Claim 1 recites a “memory controller” with “logic to receive a write request from a host via the host interface, the write request accompanied by an address that designates a specific one of the subdivisions.” Petitioner identifies the claimed “memory controller” with the controller within *e.g.* the “memory system 2”

of Sinclair's Figure 1 (which Sinclair also calls the "memory"), and the claimed "host" with the "host system 1" in Sinclair's Figure 1 (which Sinclair also calls its "host"). *See* Pet. 46; *see also* Ex. 1007 [Sinclair], Figure 1, 6:54 (referring to the "memory 2" of Figure 1), 7:25-37 (referring to the "host 1" of Figure 1). Petitioner identifies write commands sent from Sinclair's host to Sinclair's controller as the claimed "write requests," *see* Pet., 47, and Sinclair's "metablocks" as the claimed "subdivisions." *See, e.g.,* Pet., 46.

- a) *Sinclair Does Not Disclose The Claimed "write request from a host . . . accompanied by an address that designates a specific one of the subdivisions."*

112. Petitioner does not show that what Petitioner identifies as the claimed "write request from a host" in Sinclair is "accompanied by an address that designates a specific one of the subdivisions" as required by claim 1. Petitioner states: "Sinclair teaches that [its] controller has logic to receive host write commands accompanied by '**logical addresses assigned by the host**,'" Pet., 47-48 (citing Ex. 1007 [Sinclair] 13:9-12, 12:20-30), and that "[t]he logical addresses accompanying the write request **are converted by the controller** to 'physical addresses within a metablock,' *e.g.,* a metablock address designating a specific one of the subdivisions." Pet., 48 (quoting Ex. 1007 [Sinclair] 13:11-12).

113. Petitioner thus acknowledges that in the context of the "write requests" it identifies in Sinclair, it is Sinclair's **controller**, not Sinclair's **host**, that generates

what it identifies as the claimed “address designating a specific one of the subdivisions” (what Petitioner calls a “physical address[] within a metablock,” or “metablock address”). Pet., 48 (citing Ex. 1007 [Sinclair], 13:4-12, 12:20-30).

114. Petitioner nevertheless argues:

Thus, Sinclair teaches that the controller has “logic to receive a write request from a host via the host interface, the write request accompanied by an address that designates a specific one of the subdivisions.”

Pet. 48. I do not agree.

115. Petitioner’s expert offers a slightly different formulation of Petitioner’s argument:

Sinclair teaches that the host issues write requests with an address that designates a metablock: “When the host writes data to the memory system, the controller converts the logical addresses assigned by the host to physical addresses within a metablock.” [Sinclair] 13:9-15. Therefore, a POSA would understand that Sinclair discloses a controller which may receive a write request from the host, where that host includes a logical address; and a POSA would further understand that the logical address—upon conversion to a physical address—designates a metablock.

Ex. 1003 [Litz-Decl.] ¶ 199.

116. Even taking Petitioner’s identification of the claimed “subdivisions” with Sinclair’s superblocks for granted for purposes of argument, to any extent that Petitioner’s expert Dr. Litz is taking the position that write commands in Sinclair are “accompanied by” Petitioner’s alleged “address that designates a specific one of the subdivisions” in the sense of claim 1, I disagree.

117. Dr. Litz states that write commands from Sinclair’s host provide logical addresses. As one example, Dr. Litz quotes Sinclair to the effect that “When the host writes data to the memory system, the controller converts the *logical addresses assigned by the host* to physical addresses within a metablock,” Ex. 1003 ¶ 199 (quoting Ex. 1007 [Sinclair] 13:9-15) (emphasis added). As another example, he states that “Sinclair discloses a controller which may receive a write request from the host, *where that host includes a logical address*,” Ex. 1003 ¶ 199 (emphasis added). The same passage acknowledges that Sinclair’s memory controller receives these write commands.

118. These disclosures show that the thing that “designates a specific one of the subdivisions” in Petitioner’s identification—a metablock address—is generated at Sinclair’s controller after a request is received. Such a thing cannot accompany the request.

119. Dr. Litz also expressly recognizes the role of Sinclair’s memory controller in *converting* logical addresses (such as those from write commands

received from Sinclair’s host) into metablock addresses. In a passage that I have already quoted once (but now with different added emphasis), Dr. Litz quotes Sinclair to the effect that “When the host writes data to the memory system, *the controller* converts the logical addresses assigned by the host to physical addresses within a metablock,” Ex. 1003 ¶ 199 (quoting Ex. 1007 [Sinclair] 13:9-15) (emphasis added). Dr. Litz does not explain how what Petitioner identifies as a “write request from a host”—a command containing a logical address that the controller converts to a metablock address—could be said to be “accompanied by” something that the controller (the recipient of the alleged request) has to generate upon receiving the request.

120. To be clear, Dr. Litz does not use the claim language “accompanied by” in this paragraph of his declaration, Ex. 1003 ¶ 199, and it is not clear to me if Dr. Litz even takes this position. But to any extent that he does, I disagree. A POSITA would not understand a write command directed by Sinclair’s host to Sinclair’s controller to be “accompanied by” a metablock address that the controller generates upon receiving the command. Here, the understanding of the POSITA is consistent with a plain English understanding of the term “accompanied by,” and nothing in the knowledge of POSITA would displace the plain meaning of this term in this context.

121. There are reasons beyond the plain meaning of “accompanied by,” why a POSITA would not understand a write request from a host to be “accompanied by” the address of a metablock that is written to as a result of the request.

122. As one example, even though Sinclair’s logical addresses may ultimately resolve to physical addresses, a POSITA would understand that this correspondence may not always be known in advance of a write command. In both Sinclair and other systems, a POSITA would recognize that a host may issue a write request over a large logical address range at a time when only a small amount of free physical space is available. In such situations, a POSITA would recognize that garbage collection or related maintenance operations may need to take place before the write command can be completed. In such situations, the physical locations that ultimately impacted by the write command may only be determined *after* the command has issued, and indeed, after any requisite maintenance operations are complete.

123. Sinclair expressly refers this situation when it says that “[a]n example of where execution of a host command can be delayed is where there are not enough pre-erased metablocks in the erased block pool to store all the data that the host wants to write into the memory and data consolidation or garbage collection is needed first to clear one or more metablocks of valid data, which can then be erased.” Ex. 1007 [Sinclair] 14:27-32. A POSITA would recognize that in this situation, the

host providing the write command does not know which metablocks will be implicated by the logical addresses that it seeks to write to. A POSITA would further understand that such metablocks would be determined by Sinclair's controller, during or after any necessary data consolidation or garbage collection.

124. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown how Sinclair teaches the claimed "write request from a host ... the write request accompanied by an address that designates a specific one of the subdivisions" in its combination.

b) *Sinclair Does Not Render Obvious The Claimed "“write request from a host ... the write request accompanied by an address that designates a specific one of the subdivisions” In Petitioner’s Combinations.*

125. As an alternative to arguing from disclosures of Sinclair, Petitioner offers the following argument:

To the extent Sinclair does not teach this limitation, a POSITA would be motivated to incorporate the teaching from Son regarding write requests associated with a particular superblock, as discussed supra for Ground I, Claim 1[c].

Pet., 48. I do not agree.

126. Ground I is an Ellis ground, not a Sinclair ground, and Petitioner does not explain what similarities between Ellis and Sinclair would lead a POSITA to modify Sinclair by Son in a way that parallels how Petitioner would propose to

modify Ellis by Son. Similarly, as explained above, Petitioner also did not show that POSITA would be motivated to combine Ellis with Son in the way that Petitioner proposes. Even if Petitioner had motivated its Ellis combinations, however, without further explanation from Petitioner, I would not understand how any such motivation would apply to a modification of Sinclair.

127. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown that Petitioner’s Ellis combination renders obvious “logic to receive a write request from a host via the host interface, the write request accompanied by an address that designates a specific one of the subdivisions.”

3. Petitioner Does Not Show That Its Sinclair Combinations Render Obvious “logic to send the host the information indicating extent of page utilization of the specific one of the subdivisions and an address corresponding to the specific one of the subdivisions.”

128. Claim 1 additionally requires “a memory controller comprising ... logic to send the host the *information indicating extent of page utilization* of the specific one of the subdivisions and *an address corresponding to the specific one of the subdivisions*.” Petitioner identifies Sinclair’s controller as the claimed “memory controller,” *see, e.g., Pet.*, 46, a host interacting with Sinclair’s memory controller as the claimed “host,” *see, e.g., id.*, Sinclair’s “amount of valid data” and/or “number of pages of unprogrammed capacity” (or “additional variants of superblock metadata disclosed in Son”) for the claimed “information indicating extent of page

utilization,” *see, e.g., id.*, 47, one of Sinclair’s “metablocks” for the claimed “specific one of the subdivisions,” *id.*, and a “metablock address” in Sinclair for the claimed “address corresponding to the specific one of the subdivisions.” *Id.*, 48.

129. Petitioner does not argue that Sinclair’s memory controller comprises “logic to send the host the information *indicating extent of page utilization* of the specific one of the subdivisions and an address corresponding to the specific one of the subdivisions.” Indeed, Sinclair does not disclose its memory controller sending its host what Petitioner identifies as the claimed “information” for any metablock in Sinclair, let alone sending such “information” alongside what Petitioner identifies as the claimed “address corresponding to [a] specific one of the subdivisions.”

130. For a mechanism by which a modified Sinclair controller could hypothetically send the items that Petitioner has identified to the host, Petitioner turns to Yu. *See generally* Pet., 48-49. Petitioner states that Yu discloses “S.M.A.R.T. commands,” which are a mechanism by which the host *in Yu* can query a memory controller *in Yu* for “‘important data from the [controller]’ including ‘health information,’ ‘wear,’ ‘wear-leveling count,’ ‘bad block, and other flash memory management’ responsibilities.” Pet., 49 (quoting Ex. 1008 [Yu] [0064] & claim 6). Petitioner argues that Yu “teaches the use of a ‘page status table,’ as well as other metrics representing page utilization,” and by analogy with what it has already identified in Sinclair, argues that a POSITA would understand that Sinclair’s

host and controller could use what Petitioner terms “Yu’s S.M.A.R.T. functionality” for its host to query the controller for, and for the controller to then send, what the claim recites. *See, e.g.*, Pet. 49-50.

131. Petitioner argues that “[a] POSITA would understand, in order to implement Yu’s S.M.A.R.T. functionality in the combined system of Sinclair and Son, that the S.M.A.R.T. information sent to the host would include the combined system’s metablock-level metadata such as page utilization.” Pet., 49-50 (citing Ex. 1003 [Litz-Decl.] ¶ 207). As support for this argument Petitioner cites Dr. Litz, who cites disclosures in Yu for propositions such as “Yu also teaches the maintenance of page utilization data” and “[a] POSA would understand that the page status table [as in Yu] represents page utilization.” Ex. 1003 [Litz-Decl.] ¶ 207.

132. These disclosures do not support Petitioner’s point, however. These statements do not, for example, disclose that Yu ever returns its “page status table,” or information from its “page status table,” in response to a “S.M.A.R.T. command” in Yu’s own system. Petitioner does not explain why an implementation of what it terms “Yu’s S.M.A.R.T. functionality” in a modification of another reference would be inspired by a feature that is not present in an unmodified version of Yu.

133. Petitioner further argues:

Also, to apply the teaching of Yu to the combined system, a POSA would understand that the information sent by the controller to

the host in connection with the S.M.A.R.T. command ***must include*** a superblock or metablock address, as described for Ground I, Claim 1[d]-[f].

Pet., 50 (citing Ex. 1003 [Litz-Decl.] ¶ 207).

134. Petitioner cites Dr. Litz for this point, but the cited paragraph 207 does not support this point. *See* Ex. 1003 [Litz-Decl.] ¶ 207. In the paragraph immediately preceding the one cited by Petitioner, Dr. Litz says that “a POSITA would rely on metablock-level metadata where that includes an address corresponding to the specific one of the subdivisions so that the information is useful to the host.” Ex. 1003 [Litz-Decl.] ¶ 206. But even if one presumes that a feature might be “useful” to a host of a hypothetical system, it does not generally follow that an implementation of that system “must include” that feature. And Dr. Litz does not provide any other basis for Petitioner’s argument. Accordingly, Petitioner identifies no support for its assertion about what a S.M.A.R.T. command in Petitioner’s Sinclair combination “must include.”

135. Petitioner’s citation to “Ground I, Claim 1[d]-1[f]” in support of this argument about “the teaching of Yu” does not support Petitioner’s point either. Petitioner’s Ground I does not involve Yu or Sinclair. In particular, Petitioner’s Ground I does not address why a response to a Yu S.M.A.R.T. command in

Petitioner's Ground IV combination would necessarily include a "superblock or metablock address" in a modified version of Sinclair's system.

136. For at least these reasons, in my opinion, Petitioner and Dr. Litz do not show that its Sinclair combinations render obvious "logic to send the host the information indicating extent of page utilization of the specific one of the subdivisions and an address corresponding to the specific one of the subdivisions."

4. Petitioner Does Not Show That Its Sinclair Combinations Render Obvious "an erasure request from the host . . . the erasure request accompanied by the address corresponding to the specific one of the subdivisions."

137. Claim 1 recites "an erasure request from the host ... the erasure request accompanied by the address corresponding to the specific one of the subdivisions." Petitioner contends that "Sinclair teaches that the host issues, and the controller has logic to receive, 'delete' or erasure commands." Pet., 50 (citing Ex. 1007 [Sinclair] 21:50-57, 27:61-28:12). But Sinclair does not teach that any such erasure commands are accompanied by what Petitioner alleges to be an "address corresponding to the specific one of the subdivisions," which the challenged claims require. Petitioner identifies the claimed "address" with an "address designating a single metablock" in Sinclair. Pet., 50. But Petitioner does not show why any host-issued erasure request in Sinclair would include such a thing.

138. Petitioner cites Sinclair’s discussion of inserting new data in a file, where the updated file is stored as a new file and “[t]he old file is then deleted by the host, and the system may respond by reclaiming the logical address space assigned to the old file is stored, the data of which are now obsolete.” *See* Pet. 50 (citing Ex. 1007 [Sinclair] 21:50-57). This does not disclose Sinclair’s host using metablock addresses relating to where the file was stored (or where the file will be stored), let alone disclose Sinclair’s host issuing an erasure request “accompanied by” an specifying an address corresponding to a metablock.

139. When a file is deleted within a file system, a host typically updates structures such as file allocation tables (FATs) or other records to indicate that a file is no longer in use and that its logical addresses are free for reassignment. A POSITA would understand that such operations typically occur at the level of the file system or a logical address space that is visible to the host, but do not generally entail any action at the level of physical management of flash memory. (In fact, the physical data of a deleted file in a system like Sinclair would typically remain resident in the flash medium until the controller, at some later time, decides that erasing the space is beneficial. *See, e.g.*, Ex. 1007 [Sinclair] 12:20-30.)

140. Sinclair’s statement that when an “old file is then deleted by the host, [] the system may respond by reclaiming the logical address space assigned to the old file” is consistent with this general understanding. A POSITA would not

understand “reclaiming the logical address space assigned to the old file” to involve the erasure by Sinclair’s controller of the physical blocks that formerly corresponded to the logical address space occupied by the old file.

141. Petitioner also cites Ex. 1007 [Sinclair] 27:61-28:12, which is a general enumeration of circumstances in Sinclair’s system in which “data may become obsolete,” where such circumstances include “a file is deleted by a host” or “data within a file is deleted by a host.” *Id.*, 28:1-2.

142. Again, however, Petitioner does not explain how Sinclair’s host deleting a *file* would relate to Sinclair’s host allegedly sending erasure requests “accompanied by the address corresponding to the specific one of the subdivisions” (where Petitioner identifies the claimed “subdivisions” with Sinclair’s “metablocks”).

143. In Sinclair’s system, the translation from logical addresses to physical addresses is generally performed by Sinclair’s controller with a logical address as an input. There would be no reason for Sinclair’s host to send metablock addresses to a controller capable of generating that information. Sinclair expressly explains that “[t]he controller of the memory system will typically change the physical block into which any particular logical block is mapped but *this is not known to the host* and does not affect its assignment of addresses of file data to the logical blocks.” Ex.

1007 [Sinclair] 18:43-47. A POSITA would understand from this disclosure that Sinclair's host does not translate between logical addresses and physical addresses.

144. Petitioner also argues that this limitation is shown by incorporating its arguments about its Ellis/Son combination by reference. Pet., 51. But I do not see how simply citing these arguments about a modification of Ellis would show that the limitation would be present in Petitioner's proposed modification of Sinclair.

145. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown that Petitioner's Sinclair combinations render obvious "an erasure request from the host . . . the erasure request accompanied by the address corresponding to the specific one of the subdivisions."

VII. CONCLUSION

146. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required, I will appear for cross-examination within the United States during the time allotted.

147. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are believed by me to be true, and that all statements herein were and are made with the

knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Respectfully submitted,

Dated: October 20, 2025

A handwritten signature in black ink, appearing to read 'Dr. Mark Jones', written over a light blue rectangular background.

Dr. Mark Jones

Exhibit A

**GENERAL
INFORMATION****Home Address:**

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US Citizen Born March 15, 1965 in Newport News, VA
Residence history: Newport News VA; Redlands CA; Dallas TX;
 Blacksburg VA; Clemson SC; Durham NC; Chicago IL;
 Knoxville TN; Blacksburg VA, Yukon OK

**PROFESSIONAL
EXPERIENCE**

Professor Emeritus of Electrical and Computer Engineering, Virginia Tech,
2021-present

Professor, Department of Electrical and Computer Engineering, Virginia Tech,
8/97-2021

Chief Technology Advisor, *Ocean Tomo, LLC*, August 2013 to December 2013.

Professor, Department of Computer Science, University of Tennessee, 8/93-7/97

Assistant Computer Scientist, Mathematics and Computer Science Division,
Argonne National Laboratory, Chicago, IL, 6/90 to 7/93.

EDUCATION

Ph.D., Duke University, Computer Science, May 1990.

B.S., Clemson University, Computer Science, summa cum laude, May 1986.

**RECOGNITION
AND AWARDS**

Virginia Bioinformatics Faculty Fellow
1st prize and Honorable Mention at AOL-CIT Research Day
Virginia Tech College of Engineering Dean's List for Teaching
NSF CAREER Award
University of Tennessee Science Alliance Award
Atanasoff Best Paper Award
Gordon Bell Prize
Von Neumann Fellowship
R. F. Poole Scholarship
National Merit Scholar

**EXPERT
TESTIMONY**

Blackboard v. Desire2Learn
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving Internet-based educational
software employing role-based access control
Testified: Jury trial (infringement and validity), injunction hearing,
contempt hearing, and deposition (4 times)

TechRadium v. Blackboard
United States District Court for the Eastern District of Virginia

United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving network-based emergency notification systems
Testified: Preliminary injunction hearing and deposition

Computer Associates v. Digex
Circuit Court for Prince George's County Maryland
Overview: Contract dispute involving enterprise management systems
Testified: Jury trial and deposition

Computer Associates v. Retired Persons Services
United States District Court for the Eastern District of Virginia
Overview: Contract dispute involving enterprise management systems
Testified: Deposition

DVSI v. University of Phoenix and Walden University
United States District Court for the Eastern District of Virginia
Overview: Patent infringement case involving network-based educational software employing digital rights management
Testified: Deposition (3 days)

VirnetX v. Microsoft
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving VPN software in Microsoft Windows and Microsoft's Unified Communications software
Testified: Jury trial (infringement and validity) and deposition (3 days)

TechRadium v. Twitter
United States District Court for the Southern District of Texas
Overview: Patent infringement case involving network-based notification systems
Testimony: Deposition

Bedrock Computer Tech v. Softlayer et al
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving data structures in the Linux operating system's network stack
Testimony: Jury trial v. Google (infringement and validity), Jury trial v. Yahoo (infringement and validity) and deposition (3 days)

CEATS v. Continental Airlines et al
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving Web-based interactive seat maps
Testimony: Jury trial (infringement and validity) and deposition (2 days)

VirnetX v. Cisco et al
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving secure communications, VPNs, and Voice-over-IP
Testimony: Jury trial v. Apple (infringement and validity), Jury trial v. Cisco (validity), and deposition (3 days), 2nd jury trial v. Apple (infringement), 3rd jury trial v. Apple (infringement), 4th jury trial v. Apple (infringement), 5th jury trial v. Apple

Summit6 v. Research In Motion et al
United States District Court for the Northern District of Texas

Overview: Patent infringement case involving network-based photo uploading tools on smartphones and web browsers

Testimony: Jury trial v. Samsung (infringement and validity) and deposition (3 days)

Ericsson v. Samsung

International Trade Commission

Overview: Patent infringement case involving Java technology and touchscreen technology on smartphones

Testimony: Deposition

AT Engine Controls LTD. v. Goodrich Corp and Goodrich Pump & Engine Control Systems, Inc.

United States District Court for the District of Connecticut

Overview: Trade secret case involving an embedded computing system design for helicopter engine control

Testimony: Deposition

SmartFlash LLC. v. Apple, et. al.

SmartFlash LLC. v. Samsung, et. al.

United States District Court for the Eastern District of Texas

Overview: Patent infringement case involving digital rights management and content distribution

Testimony: Jury trial v. Apple (infringement and validity) and deposition (4 days)

Unwired Planet v. Apple

United States District Court for the Northern District of California

Overview: Patent infringement case involving several technologies related to mobile devices

Testimony: Deposition (3 days); technology tutorial presentation to the Court

Facebook v. Rembrandt Social Media

Patent Trial and Appeal Board

Overview: Validity of a patent in the area of a web-based diary system

Testimony: Deposition

Motorola Mobility v. Intellectual Ventures

Patent Trial and Appeal Board

Overview: Validity of a patent in the area transmitting and browsing preformatted information

Testimony: Deposition

Summit6 v. Apple et al

United States District Court for the Northern District of Texas

Overview: Patent infringement case involving network-based photo uploading tools on smartphones and web browsers

Testimony: Deposition

EMC v. Pure Storage et al

United States District Court for the District of Delaware

Overview: Patent infringement case involving memory systems

Testimony: Deposition and jury trial (infringement and validity)

Parallel Networks v. IBM

United States District Court for the District of Delaware

Overview: Patent infringement case involving web servers and load balancing
Testimony: Deposition (2 days)

Parallel Networks v. Microsoft

United States District Court for the District of Delaware

Overview: Patent infringement case involving web servers and load balancing
Testimony: Deposition (2 days) and jury trial (infringement and validity)

Microsoft and IBM v. Parallel Networks

Patent Trial and Appeal Board

Overview: Validity of a patent related to web servers and load balancing
Testimony: Deposition

adidas v. Under Armour

United States District Court for the District of Delaware

Overview: Patent infringement case involving fitness tracking
Testimony: Deposition

BMC Software v. ServiceNow

United States District Court for the Eastern District of Texas

Overview: Patent infringement case involving enterprise management software
Testimony: Deposition

Ericsson v. TCL

United States District Court for the Eastern District of Texas

Overview: Patent infringement case involving Java technology and security on smartphones

Testimony: Deposition (3 days) and jury trial (infringement)

REM v. Square

United States District Court for the Eastern District of Missouri

Overview: Intellectual property case involving credit card readers for smartphones

Testimony: Deposition

AARC v. Chrysler et al

United States District Court for the District of Columbia

Overview: Intellectual property case involving car infotainment systems
Testimony: Deposition

Spex Technologies v. Apricorn

United States District Court for the Central District of California

Overview: Patent infringement case involving secure memory devices
Testimony: Deposition, Jury trial

United States Conference of Mayors v. Great-West Life Annuity Insurance Co.

United States District Court for the District of Columbia

Overview: Contract dispute
Testimony: Deposition and jury trial

Tecsec, Inc. v. Adobe Systems Inc. and Oracle (listed as IBM, et.al.).

United States District Court for the Eastern District of Virginia

Overview: Patent infringement case involving secure object technology
Testimony: Adobe: Deposition and jury trial (infringement and validity); Oracle (deposition)

Egenera, Inc. v. Cisco Systems, Inc.

United States District Court for the District of Massachusetts

Overview: Patent infringement case involving an architecture for a processing platform

Testimony: Deposition, bench trial, and jury trial

Unified Patents v. Sound View Innovations

Patent Trial and Appeal Board

Overview: Validity of a patent related to concurrency control

Testimony: Deposition

Hulu v. Sound View Innovations

Patent Trial and Appeal Board

Overview: Validity of a patent related to concurrency control

Testimony: Deposition

Grace and Potter. v. Apple Inc.

United States District Court for the Northern District of California

Overview: Class action case involving FaceTime

Testimony: Deposition

HTC v. Ericsson

United States District Court for the Eastern District of Texas

Overview: Patent licensing related to cellular standards

Testimony: Deposition

Windy City.Innovations v. FaceBook, Inc..

United States District Court for the Northern District of California

Overview: Patent infringement case involving an architecture for a messaging platform

Testimony: Deposition

Hulu v. Sound View Innovations

Patent Trial and Appeal Board

Overview: Validity of a patent related to real time systems

Testimony: Deposition

Citrix Systems, Inc. v. Avi Networks, Inc..

United States District Court for the District of Delaware

Overview: Patent infringement case involving network devices

Testimony: Deposition

Rovi v. Comcast

International Trade Commission

Overview: Patent infringement case set top boxes

Testimony: Deposition, Trial

Seven Networks v. Apple

United States District Court for the Eastern District of Texas

Overview: Patents related to mobile device push-based communication

Testimony: Deposition

Match Group, LLC v. Bumble Trading Inc.

United States District Court for the Western District of Texas

Overview: Patents related to online dating apps

Testimony: Deposition

SAS Institute Inc. v. World Programming Limited, et. al.
United States District Court for the Eastern District of Texas
Overview: Copyright and patents related to statistical software
Testimony: Deposition, Bench trial

Allscripts Healthcare, LLC v. Decision Resources Group,
United States District Court for the District of Massachusetts
Overview: Contract dispute
Testimony: Deposition, jury trial

Clear Imaging v. Samsung
United States District Court for the Eastern District of Texas
Overview: Patents related to image processing
Testimony: Deposition

Nokia v. Lenovo
International Trade Commission
Overview: Patents related to video encoding
Testimony: Deposition

Dish Network v. Sound View Innovations
Patent Trial and Appeal Board
Overview: Validity of a patent related to scheduling for QoS
Testimony: Deposition

Dish Network v. Sound View Innovations
Patent Trial and Appeal Board
Overview: Validity of a patent related real-time multimedia applications
Testimony: Deposition

RFCyber v. Samsung
United States District Court for the Eastern District of Texas
Overview: Patents related to secure payment systems
Testimony: Deposition

RightQuestion LLC v. Samsung
United States District Court for the Eastern District of Texas
Overview: Patents related to hardware-based authentication
Testimony: Deposition

Daedalus Blue, LLC v. MicroStrategy Inc.
United States District Court for the Eastern District of Virginia, Norfolk
Division
Overview: Patent infringement case involving business intelligence software
Testimony: Deposition

Seven Networks v. Motorola Mobility LLC,
United States District Court for the Eastern District of Texas
Overview: Patents related to mobile device communication methods
Testimony: Deposition

HID Global Corp. v. Vector Flow Inc. and Ajay Jain, Vikrant Ghai, and
Shailendra Sharma
United States District Court for the District of Delaware
Overview: Patents related to security monitoring

Testimony: Deposition and Trial

YouToo Technologies, LLC, v. Twitter, Inc.

United States District Court for the Northern District of Texas Dallas Division

Overview: Patents related to video

Testimony: Deposition (2 days) and jury trial

Constellation Designs, LLC v. LG Electronics, Inc., LG Electronics USA, Inc.,
and LG Electronics Alabama, Inc.

U.S. District Court, Eastern District of Texas, Marshall Division

Overview: Patents related to digital communication systems

Testimony: Deposition and Trial

Ryan Hardin, et al. v. Samsung Electronics Co., LTD., et al.

U.S. District Court, Eastern District of Texas, Marshall Division.

Overview: Patents related to geofencing

Testimony: Deposition

Xerox, ACS Transport Solutions, Conduent and New Jersey Transit v.

Bytemark, Inc.

Patent Trial and Appeal Board

Overview: Validity of a patent related to mobile ticketing

Testimony: Deposition

Motista LLC v. Ernst and Young LLP

Arbitration Proceedings

Overview: Matters related to trade secrets

Testimony: Hearing

Inovalon v. Komodo Health

Arbitration Proceedings

Overview: Matters related to trade secrets and breach of contract

Testimony: Hearing

Alacritech, Inc. v. Dell Inc. et al

U.S. District Court, Eastern District of Texas, Marshall Division

Overview: Patents related to network interface devices

Testimony: Deposition

RFCyber v. Apple

United States District Court for the Western District of Texas

Overview: Patents related to secure payment systems

Testimony: Deposition

K. Mizra LLC v. Hewlett Packard Enterprise Co and Aruba Networks LLC

U.S. District Court, Eastern District of Texas, Marshall Division

Overview: Patents related to network security

Testimony: Deposition

Carbyne v. Apple

United States District Court for the Western District of Texas

Overview: Patents related to hardware-based authentication

Testimony: Deposition

Radian Memory Systems LLC, v. Samsung Electronics Co., LTD., et al.

U.S. District Court, Eastern District of Texas, Marshall Division.

Overview: Patents related to flash memory controllers

Testimony: Deposition

Leo Riot, et al. v. Apex Trader Funding Inc., et al.

United States District Court for the Western District of Texas, Austin Division.

Overview: Matters related to trade secrets, copyrights, and breach of contract

Testimony: Deposition

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RESEARCH GRANTS NASA, "Phase II: Integrated Sensors for the Evaluation of Structural Integrity of Inflatable Habitats," with NanoSonic, \$180,000, 9/25/17-9/24/19.

NSF, "SCH: INT: Collaborative Research: Smart Wearable Systems to Support and Measure Movement in Children With and Without Mobility Impairments," \$326,658, 10/1/17-9/30/21.

NASA, "Integrated Sensors for the Evaluation of Structural Integrity of Inflatable Habitats," with NanoSonic, \$35,000, 9/1/2016-8/31/17.

NSF, "SHB: Small: Collaborative Research: Electronic textiles for ambulatory health monitoring," \$306,083, 7/1/2011-6/30/2014.

DARPA, "RECE," With BBN, \$30,000, 4/16/09-10/16/09.

NSF, "Investigating a Novel Embedded Processor Architecture for Electronic Textiles in Wearable and Pervasive Computing," \$220,000, 12/1/08-11/30/10.

NSF, "Fundamental Algorithms to Enable the Simulation of Multi-Scale Biological Systems," \$200,000, 9/1/07-8/31/10.

AFRL, "Phase II: Amorphous Soft-Core Processor for Hardware Anti-Tamper," ~\$230,000, 11/1/06-10/31/08.

Intel, "E-Textile Rug for Gait Analysis, People Tracking and Emergency Directions," \$15,000, 6/1/06-12/31/06.

Carilion, "Quantitative Measurement and Modeling of Early Events in Influenza Pathogenesis," \$20,000, 7/1/05-6/30/06.

AFRL, "Phase I: Wearable Computer for Enhanced Situation Awareness," \$30,000, 5/1/06-1/1/07.

AFRL, "Phase I: Amorphous Soft-Core Processor for Hardware Anti-Tamper," \$35,000, 1/1/06-11/1/06.

MDA, "Phase I: Secure Software Platform for Real-Time Software Anti-Tamper," \$29,994, 6/1/06-11/1/06.

National Science Foundation (NSF), "CRI", (e-textiles equipment), ~\$80,000, 8/05-7/07.

Harris Corporation, "Exploiting the Reconfigurability of a Software-Defined Radio Platform," \$161,070, 9/1/05-6/30/06.

DARPA, "Phase I: Technology for Trusted Circuits," \$31,000, 3/1/05-9/15/05.

Harris Corporation, "Partial Reconfiguration Support for the Harris Programmable Modem Platform," \$73,448, 12/01/04-6/30/05.

NSF, "Phase I: An Electronic Textile System for Gait Analysis", \$33,000, 1/1/2005-6/30/2005.

Office of Naval Research (ONR). "AWINN." \$452,300, 12/20/04-7/31/06.

Office of Secretary of Defense, "Phase II: Reconfigurable Processor Technology for Software Protection," SBIR Subcontract with Luna Innovations, \$237,581, 6/04-5/06.

NSF, REU Supplement to ITR: Tailor-Made: Design of e-Textile Architectures for Wearable Computing, NSF, \$12,000, 6/1/2005 – 8/31/2005.

Office of Secretary of Defense, "Phase I: Reconfigurable Processor Technology for Software Protection," SBIR Subcontract with Luna Innovations, \$33,000, 8/03-2/04.

National Science Foundation (NSF), "ITR: Tailor-Made: Design of e-Textile Architectures for Wearable Computing", \$399,000, 8/02-8/06.

NSF, REU Supplement to above grant, \$10,000.

NSF, REU Supplement to above grant, \$6,000.

NSF, "A Toolbox of Scalable Algorithms and Software for Advanced Scientific Computing Applications", \$300,000, 4/03-4/06.

Defense Advanced Research Projects Agency (DARPA). Computational Fabrics, \$217,000, 3/01-12/02. Subcontract from ISI/University of Southern California.

Office of Naval Research (ONR). Secure Configurable Radio. \$751,000, 4/00-4/04.

NSF, SUCCEED, \$33,000, 9/1/01-8/31/02.

National Science Foundation (NSF). Parallel unstructured mesh algorithms, Amount: \$145,023, 10/99-9/02.

DARPA, Development of algorithms and software for the control of distributed, dynamic sensor networks, Amount \$411,625, 6/99-6/02.

DARPA, Subcontract with USC/ISI. Development of algorithms and runtime software for systems of configurable computers, Amount \$160,000, 10/00-10/01.

Department of Energy, Development of algorithms and software for massively parallel architectures, Amount: \$145,000, 12/98-11/01.

DARPA, Development of Java-based tools and applications for fast, flexible run-time reconfiguration of configurable computing devices, Amount: \$345,574, 9/99-9/01.

DARPA, Development of an application programming interface, algorithms, and applications for run-time reconfiguration on novel adaptive computing architectures, Amount: \$250,000, 6/99-6/01.

Lockheed-Martin/Sanders, A Wireless Link for Remote Telemetry of Compact Airborne System, \$125,000, 5/00-4/01.

DARPA, Development of algorithms and runtime software for systems of configurable computers, Amount \$169,792, 11/99-10/00.

National Security Agency (NSA), Software for the translation of JBits FPGA programs to EDIF programs, Amount \$75,000, 9/99-7/00.

DARPA, Construction of an API & applications for the control of distributed systems of configurable computing nodes, Amount \$162,886, 9/98-10/99.

NSF, Career Award: Parallel algorithms and software for unstructured mesh computations, Amount: \$125,881, 7/96-7/99.

Air Force Research Laboratory, Research and development of an Internet-based, interactive, decision making program, Amount: \$97,425, 11/97-5/99.

NSF, Equipment funding for a 16-node cluster of configurable computers, Amount: \$85,000, 12/97-12/98.

NSF, Scientific applications in a distributed computing environment, Amount: \$318,807, 7/95-7/98.

NSF, Equipment funding for an ATM-based cluster of workstations, Amount, \$100,000, 1/96-12/96.

NSF, Workshop organized at Argonne National Laboratory, Amount, \$10,000, 1996.

PATENTS

Inventor, United States Patent No. 8,473,754, Hardware-Facilitated Secure Software Execution Environment.

SOFTWARE

SLAAC/ACS API (4/99): Software for the control of complex systems of configurable computing nodes and high-speed networks. This code has been distributed to the ACS community. Developed in Configurable Computing Laboratory with Peter Athanas.

BlockSolve (4/93 & 1/96): Software for solving large sparse linear systems on distributed memory architectures. This code has been distributed via netlib and ANL ftp and has been accessed by several hundred people as of 4/4/99. Developed at Argonne National Laboratory with Paul Plassmann.

LANZ (10/90): Software for solving the generalized eigenproblem on shared memory architectures. This code has been distributed via netlib and NASA and has been accessed by over 10,000 people as of 4/4/99. Developed at Duke University and Argonne National Laboratory with Merrell Patrick.

TEACHING

Computer Programming

RESPONSIBILITIES

ECE 5574, *Advanced Software Development for CAE*
ECE 4574, *Large-Scale Software Development for Engineering Systems*
ECE 3574, *Applied Software Design*
ECE 2574, *Data Structures*
ECE 1574, *Engineering Problem Solving with C++*
Computer Simulation and Modeling
CS 371, *Numerical Analysis*
CS 594, *Computational Modeling*
Computer Network, Architecture, and Organization
ECE 2504, *Introduction to Computer Engineering*
CS 594, *Internetworking with TCP/IP*
ECE 4504, *Computer Organization*
ECE 4534, *Design of Embedded Systems*
ECE 5504 (formerly ECE 5515), *Computer and Network Architectures*
ECE Special Studies: *Configurable Computing*, E-Textiles
ECE 5984, *Java-Based Configurable Computing*
ECE 6504, *Applications of Parallel and Distributed Computing*, TV course.
CS 530, *Computer Systems Organization*
CEO of DISC, a student-run virtual corporation, for Fall 1998 and Spring 1999.
