UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE Technology Group Co., Ltd.,
Petitioner,
v.
Paneltouch Technologies LLC,
Patent Owner.

U.S. Patent No. 11,126,025
Original Issue Date: September 21, 2021
Title: IN-CELL TOUCH PANEL

Case No. IPR2025-01267

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,126,025 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42 *et seq.*

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,126,025 (the "'025 patent")
1002	Prosecution History of U.S. Patent No. 11,126,025
1003	Declaration of Richard A. Flasck, M.S. ("Flasck Decl.")
1004	*Curriculum Vitae* of Richard A. Flasck, M.S. ("Flasck C.V.")
1005	U.S. Patent Application Publication No. 2016/0224155 A1 ("Kim")
1006	U.S. Patent Application Publication No. 2017/0192568 A1 ("Kim II")
1007	U.S. Patent Application Publication No. 2018/0113541 A1 ("Xie")
1008	U.S. Patent Application Publication No. 2019/0294273 A1 ("Yoshida")
1009	Japanese Patent Application No. 2018-058356 and Certified Translation ("Translation")
1010	U.S. Patent No. 3,824,003
1011	Willem den Boer, *Active Matrix Liquid Crystal Displays: Fundamentals and Applications* (Elsevier 2005)
1012	U.S. Patent No. 4,582,395
1013	Excerpt from *Wiley Electrical and Electronics Engineering Dictionary* (2004)
1014	Redline comparing Claims 10 and 18 of U.S. Patent No. 11,126,025
1015	U.S. Patent Application Publication No. 2016/0054627 A1

CHALLENGED CLAIM LISTING

Claim	Limitation No.	Limitation
1	[1-PRE]	An in-cell touch panel having an image display area made up of pixels arranged in a first direction and a second direction intersecting the first direction, the in-cell touch panel comprising:
	[1-A]	transistors and pixel electrodes respectively provided in the pixels;
	[1-B]	common electrodes arranged in the first direction and the second direction, respectively facing one or more of the pixel electrodes and provided separately from each other;
	[1-C]	gate lines that extend along the first direction and supply gate signals to the transistors respectively;
	[1-D]	data lines that extend along the second direction and supply data signals to the transistors respectively;
	[1-E]	touch lines that extend along the second direction and are each connected to a corresponding one of the common electrodes; and
	[1-F]	a first bridge line laterally bridging two of the segment electrodes adjacent in the second direction across one of the division areas,
	[1-G]	wherein each common electrode has segment electrodes divided with a division area on the gate line,
	[1-H]	segment electrodes included in one of the common electrodes are connected by at least one of the touch lines,
	[1-I]	the first bridge line and each of the two of the segment electrodes are connected via a contact hole, and

Claim	Limitation No.	Limitation
	[1-J]	the first bridge line extends in the second direction so as to overlap with the segment electrodes included in the one of the common electrodes, and be connected to the segment electrodes included in the one of the common electrodes.
2	2	The in-cell touch panel according to claim 1, wherein the first bridge line is formed in a different layer from the common electrode.
3	3	The in-cell touch panel according to claim 1, wherein the first bridge line is formed in a same layer as the touch line.
4	4	The in-cell touch panel according to claim 1, wherein the contact hole overlaps with the gate line in a planar view.
5	5	The in-cell touch panel according to claim 1, wherein the contact hole does not overlap with the data line in a planar view.
6	6	The in-cell touch panel according to claim 1, wherein the first bridge line overlaps with the data line in a planar view.
8	[8-PRE]	The in-cell touch panel according to claim 1, wherein
	[8-A]	two of the common electrodes adjacent in the second direction are separated from each other with the separation area on the gate line,
	[8-B]	the in-cell touch panel includes a second bridge line laterally bridging the two of the common electrodes adjacent in the second direction across the separation area, and
	[8-C]	the second bridge line is not electrically connected to any of the two of the common electrodes.
9	9	The in-cell touch panel according to claim 1, wherein a plurality of the first bridge lines are provided in the one of the common electrodes.

Claim	Limitation No.	Limitation
10	[10-PRE]	An in-cell touch panel having an image display area made up of pixels arranged in a first direction and a second direction intersecting the first direction, the in-cell touch panel comprising:
	[10-A]	transistors and pixel electrodes respectively provided in the pixels;
	[10-B]	common electrodes arranged in the first direction and the second direction, respectively facing one or more of the pixel electrodes and provided separately from each other;
	[10-C]	gate lines that extend along the first direction and supply gate signals to the transistors respectively;
	[10-D]	data lines that extend along the second direction and supply data signals to the transistors respectively;
	[10-E]	touch lines that extend along the second direction and are each connected to a corresponding one of the common electrodes; and
	[10-F]	a dummy touch line extending along the second direction, formed in a same layer as the touch lines, and not electrically connected to any of the common electrodes,
	[10-G]	wherein each common electrode has segment electrodes divided with a division area on the gate line,
	[10-H]	segment electrodes included in one of the common electrodes are connected by at least one of the touch lines,
	[10-I]	wherein the touch lines are connected one-by-one with the common electrodes arranged in the second direction among the common electrodes,
	[10-J]	two of the common electrodes adjacent in the first direction are separated from each other with a separation area on the data line, and

Claim	Limitation No.	Limitation
	[10-K]	the dummy touch line is provided in the separation area.
11	[11-A]	The in-cell touch panel according to claim 10, wherein a fixed voltage is applied to the dummy touch line, and
	[11-B]	the fixed voltage is a common voltage to be applied to the common electrode.
14	14	The in-cell touch panel according to claim 10, wherein a width of the dummy touch line is smaller than a distance between the dummy touch line and the common electrode.
17	17	The in-cell touch panel according to claim 10, wherein the dummy touch line is offset from any of the common electrodes in a planar view.
18	[18-PRE]	An in-cell touch panel having an image display area made up of pixels arranged in a first direction and a second direction orthogonal to the first direction, the in-cell touch panel comprising:
	[18-A]	transistors and pixel electrodes respectively provided in the pixels;
	[18-B]	common electrodes arranged in the first direction and the second direction, respectively facing one or more of the pixel electrodes and provided separately from each other;
	[18-C]	gate lines that extend along the first direction and supply gate signals to the transistors respectively;
	[18-D]	data lines that extend along the second direction and supply data signals to the transistors respectively;
	[18-E]	touch lines that extend along the second direction and are each connected to a corresponding one of the common electrodes; and

Claim	Limitation No.	Limitation
	[18-F]	a dummy touch line that extends along the second direction, is formed in a same layer as the touch lines, and is electrically isolated from any of the common electrodes,
	[18-G]	wherein each touch line is connected with a corresponding one of the common electrodes arranged in the second direction,
	[18-H]	two of the common electrodes adjacent in the first direction are separated from each other with a separation area on the data line as, and
	[18-I]	the dummy touch line is provided in the separation area.

I. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42, Petitioner respectfully requests *inter partes* review ("IPR") of Claims 1-6, 8-11, 14, 17, and 18 ("Challenged Claims") of U.S. Patent No. 11,126,025 (the "'025 patent"). The Challenged Claims recite an in-cell touch panel with (1) common electrodes divided into segment electrodes and/or (2) a dummy touch line between common electrodes. The '025 patent suggests that these features prevent: distortions in the capacitance of the common electrodes, and electric fields from causing unintended rotation of the display's liquid crystals. But in-cell touch panels with these exact solutions to these exact problems were already known, described, and patented prior to the '025 patent's alleged invention.

Petitioner requests that the PTAB institute trial and find the Challenged Claims unpatentable for the reasons set forth herein.

II. 37 C.F.R. § 42.8(B): MANDATORY NOTICES

A. 37 C.F.R. § 42.8(b)(1): Notice of Real Parties-in-Interest

BOE Technology Group Co., Ltd. ("BOE" or "Petitioner") is the real party-in-interest. No other parties exercised or could have exercised control over this Petition; no other parties funded or directed this Petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

B. 37 C.F.R. § 42.8(b)(2): Notice of Related Matters

To the best knowledge of Petitioner, the '025 patent has been involved in the following matters:

Case Name	Filed
Paneltouch Technologies LLC v. BOE Technology Group Co., Ltd., No. 2:25-cv-00245-JRG (E.D. Tex.)	February 28, 2025

C. 37 C.F.R. § 42.8(b)(3) and (4): Notice of Counsel and Service Information

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Petitioner submits a Power of Attorney with this Petition. Please address all correspondence to lead counsel. Petitioner consents to service by email at the email addresses listed above.

D. Fee for Inter Partes Review

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington & Sutcliffe LLP: 15-0665.

III. REQUIREMENTS FOR IPR

This Petition complies with all requirements under 37 C.F.R. § 42.104 for IPR.

A. § 42.104(a): Grounds for Standing

The ’025 patent is available for IPR. Petitioner is not barred or estopped from requesting IPR. This Petition is timely filed under 35 U.S.C. § 315(b).

B. § 42.104(b): Identification of Challenge

Under 37 C.F.R. §§ 42.104(b) and 42.22, Petitioner requests that the Board institute IPR on the Challenged Claims of the ’025 patent and cancel those claims as unpatentable.

1. § 42.104(b)(1): Challenged Claims

Petitioner challenges Claims 1-6, 8-11, 14, 17, and 18 of the ’025 patent.

2. § 42.104(b)(2): The Prior Art and Statutory Grounds

The ’025 patent is a post-AIA patent. The application for the ’025 patent claims priority to foreign applications JP 2019-035692 and JP 2019-035902, both of which were filed on February 28, 2019. For purposes of this Petition, Petitioner does not challenge that claim to priority, as the following references qualify as prior art to the ’025 patent under the earliest potential effective filing date.

The relied-upon references are prior art to the ’025 patent as follows:

Patent/Publication	Prior Art Date	Prior Art	Ex.
U.S. Patent Application Publication No. 2016/0224155 A1 ("Kim"), published on August 4, 2016	October 14, 2015	102(a)(1) and (2)	1005
U.S. Patent Application Publication No. 2017/0192568 A1 ("Kim II"), published on July 6, 2017	December 30, 2015	102(a)(1) and (2)	1006
U.S. Patent Application Publication No. 2019/0294273 A1 ("Yoshida"), published on September 26, 2019	March 26, 2018	102(a)(2)	1008

Below are the statutory grounds on which the claims are challenged:

Ground Number	Ground
1	Claims 1-3, 6 and 9 are obvious under 35 U.S.C. § 103 (post-AIA) ("obvious") over Kim alone and in combination with Kim II
2	Claims 4, 5 and 8 are obvious over Kim in combination with Kim II and Yoshida
3	Claim 18 is obvious over Yoshida alone
4	Claims 10, 11, 14 and 17 are obvious over Yoshida in combination with Kim II

None of these references were before the Examiner during prosecution of the '025 patent.

3. Level of Ordinary Skill in the Art

A POSITA at the time of the alleged invention would have had at least a bachelor's degree in electrical engineering, physics, or a similar discipline, along with 2-3 years of display and touch panel technology experience. Ex. 1003 ¶35. Relevant experience can substitute for education and vice versa. *Id.*

4. § 42.104(b)(5): Evidence Supporting Challenge

The Declaration of Richard A. Flasck (Ex. 1003) and other supporting evidence in the Exhibit List are filed herewith. Mr. Flasck's background and qualifications, and the information provided to him, are discussed in Exhibit 1003.

IV. TECHNOLOGY BACKGROUND

The structure of active matrix liquid crystal displays (AMLCDs) has been known for decades. Ex. 1003 ¶¶40-46; *see also* '025 patent, 1:17-18 (admitting "liquid crystal display device having both a touch function and a display function ha[d] been developed"). The general structure and components of such panels were well known, including panels with "a plurality of gate lines extending in the row direction, a plurality of data lines extending in the column direction, a pixel electrode provided in each of the plurality of pixels, a plurality of common electrodes (counter electrodes) provided facing the plurality of pixel electrodes, and signal lines connected to the common electrodes as touch lines" that could "sense the touch position" based on a "change in capacitance" were prior art. '025

patent, 1:40-53. All prior art discussed in this Petition describes such a panel having these same conventional components.

In such conventional AMLCD panels, each pixel includes liquid crystal material, a transistor, and a pixel electrode that applies a voltage to configure the liquid crystals and control how much light can shine through the pixel. In prior art, non-touch LCD panels, a common electrode is provided across all the pixels to apply a common default voltage to each pixel. Each transistor exists at the intersection of a horizontal gate line and a vertical data line. The voltages are set for each pixel, row by row, in a synchronized process wherein a gate signal is sent through a specific row's gate line to turn on that row's transistors, while specific data voltages are sent through the plurality of data lines for the pixels of that row. This process, which takes microseconds per row, repeatedly cycles through each row to provide a constantly updating image. Ex. 1003 ¶44.

For in-cell[1] touch-detecting LCD panels (like those at issue in this Petition), the single common electrode is instead divided into an array of separate electrodes (i.e. touch electrodes) that can also detect touch inputs through a touch line via

[1] The '025 patent admits such "in-cell" devices—which incorporate the touch sensors into the LCD itself—were prior art. '025 patent, 1:35-37; Ex. 1003 ¶¶50-53.

mutual capacitance sensing. Ex. 1003 ¶¶47-51; *see* ’025 patent, 1:41-53.

V. THERE EXISTS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

As explained below, the Challenged Claims recite an admittedly conventional in-cell touch panel with certain additional characteristics aimed at solving particular problems that lead to “degradation of image quality” in situations where “common electrodes” *i.e.*, touch electrodes, are provided over a plurality of pixels. ’025 patent, 2:14-17, 2:32-25. By 2019, others had already discovered and solved these problems.

The references discussed in this Petition describe the exact same types of in-cell touch panel devices as the ’025 patent, including the claimed pixels, common electrodes, data lines, gate lines, and touch lines, configured precisely as recited in the claims. This similarity confirms that the art was populated with several patents showing it was common in the art to provide modest design tweaks to the well-known basic touch panel design. Accordingly, because the references describe similar devices with minor adjustments to solve known problems with the conventional design, a POSITA would have had significant confidence that the teachings in this area could be readily combined with great success, and would have been highly motivated to do so to avoid the problems that had already been recognized and solved in the prior art.

A. Summary of the ’025 Patent

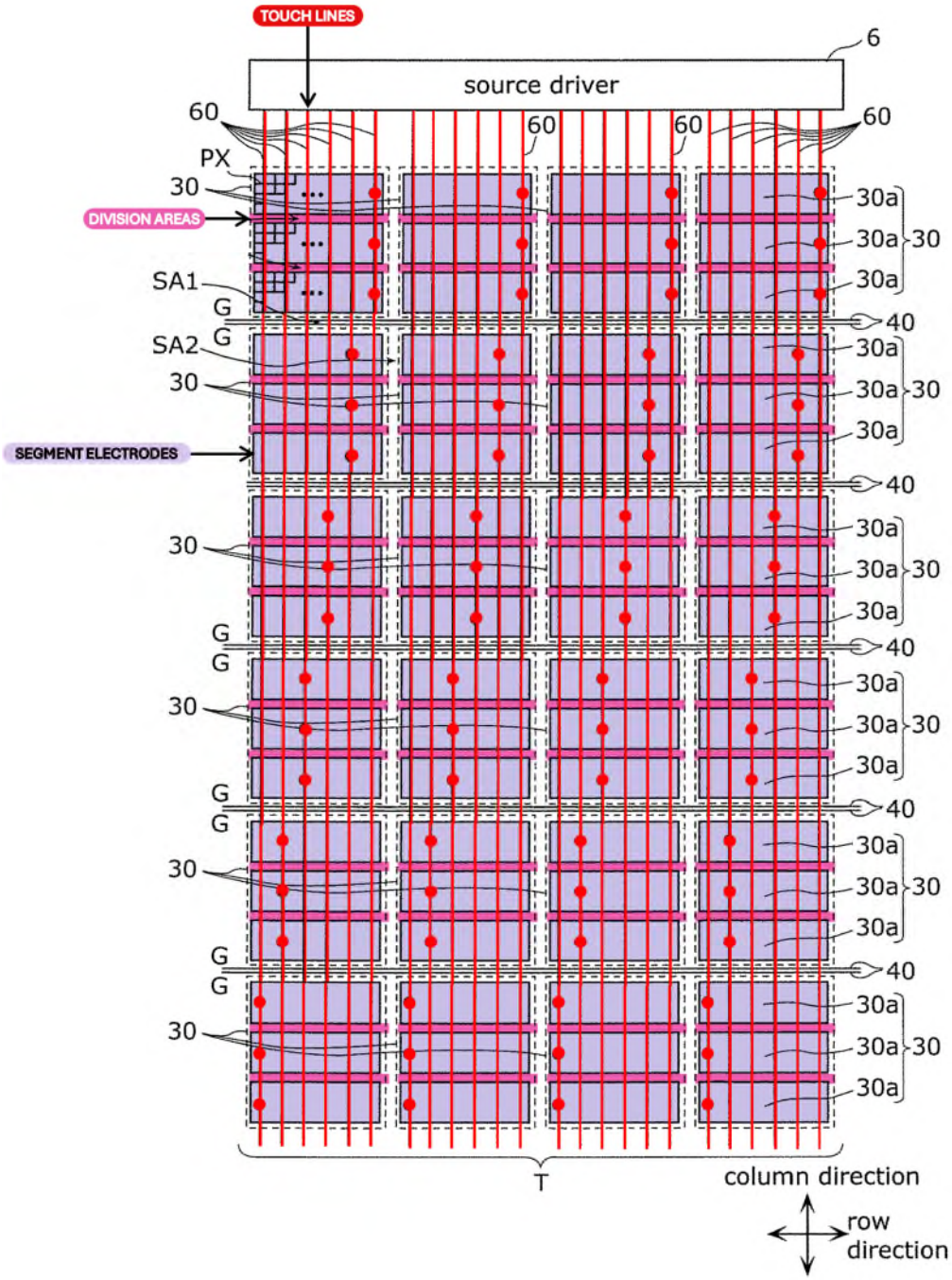
The ’025 patent relates to “in-cell” LCD touch panels with the touch detecting functionality built into the liquid crystal display itself. ’025 patent, 1:32-37. The ’025 patent describes the ordinary structure of such panels with “a plurality of gate lines extending in the row direction, a plurality of data lines extending in the column direction, a pixel electrode provided in each of the plurality of pixels, a plurality of common electrodes (counter electrodes) provided facing the plurality of pixel electrodes, and signal lines connected to the common electrodes as touch lines.” ’025 patent, 1:40-47.

The ’025 patent purports to solve two different problems with such conventional, in-cell touch panels. First, the ’025 patent observes that separate common electrodes (*i.e.*, touch electrodes) formed across several pixels and overlaping the gate lines running horizontally between pixel rows causes capacitance imbalances that degrades image quality. ’025 patent, 1:65-2:13. The patent proposes further dividing each common electrode into a plurality of segment electrodes with gate lines running between discrete segments electrodes. *Id.* 2:46-53; 16:48-56. The patent further describes connecting the segment electrodes of each common electrode with bridge lines that allow the segments to act as one common electrode without covering the gate line. *Id.* 17:16-47.

Figure 3[2] depicts an embodiment showing the common electrodes 30 divided into three (purple) segment electrodes 30a each. Each common electrode 30 is connected a specific (red) touch line 60, which connects to each segment electrode 30a within each common electrode 30. The (pink) spaces between the segment electrodes 30a within a common electrode are labeled DA for "division area." *Id.* 11:19-30. Although not depicted, the '025 patent explains that there are horizontal gate lines present in that division area between segment electrodes. *Id.* 7:20-23.

[2] All figures presented in this Petition have been annotated for illustrative purposes.

FIG.3



'025 patent, Fig. 3.

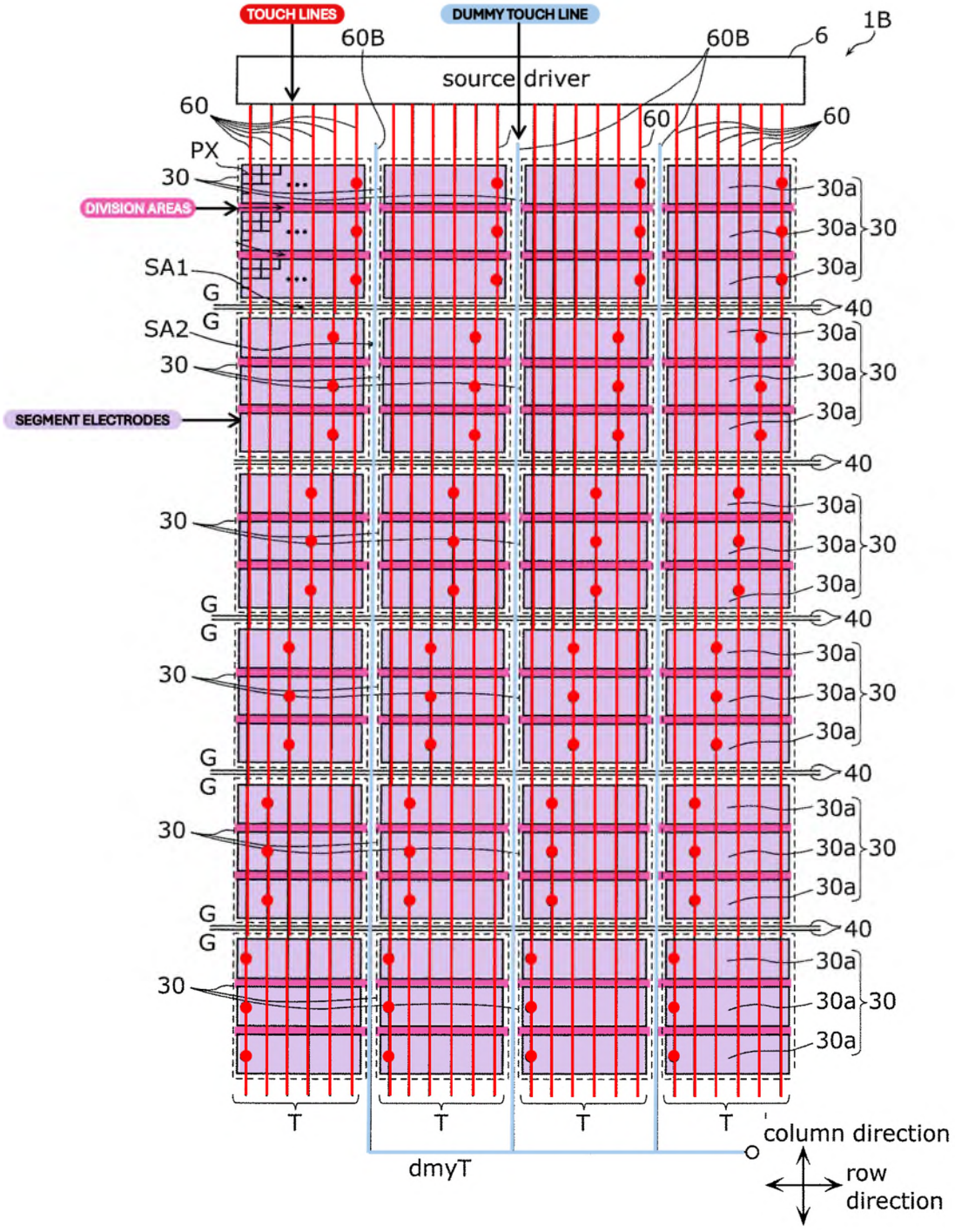
While not depicted in Figure 3, the '025 patent also describes "first bridge

lines 80" which "extend[] in the column direction so as to overlap with each of the plurality of segment electrodes 30a included in one common electrode 30, and is connected to each of the plurality of segment electrodes 30a included in the concerned one common electrode 30." '025 patent, 18:57-63.[3]

The second problem that the '025 patent sought to solve concerned the data line located in the gap between two common electrodes, which generates an electric field that can unintentionally rotate the liquid crystals and degrade image quality. '025 patent, 2:18-31. To solve this problem, a dummy touch line is provided over the data line in the separation area to shield the liquid crystals from the data line's field. '025 patent, 2:54-3:9; 22:10-14. These (blue) dummy touch lines 60B can be seen in Figure 14 below:

[3] Figure 12 purports to depict the first bridge lines 80, but includes a mistake, as it shows them spanning a single segment electrode while connecting in multiple places on a particular segment electrode, which is not how the bridge lines are described in the text.

FIG.14



'025 patent, Fig. 14; Ex. 1003 ¶¶54-62.

B. Prosecution History

The ’025 patent stems from U.S. Application No. 16/784,806, which claims priority to foreign applications JP2019-035692 and JP2019-035902.

Independent claims 1 and 20 (issued as claim 18) of the original application as filed omitted the concept of bridge lines. Ex. 1002 at 107-111 (U.S. Patent Application Publication No. 2020/0278571 A1, claims 1, 20 (published Sept. 3, 2020)).[4] Dependent claim 2 recited the bridge line limitations, with dependent claim 10 adding that they overlap the segment electrodes in a given common electrode. *Id.* (claims 2, 10).

On March 3, 2021, the Examiner issued a non-final rejection, allowing pending claim 20, and noting that pending claims 9 through 19 would be allowable if recited in independent form. Ex. 1002 at 227 (*Office Action*, March 3, 2021). Claim 1 was rejected as obvious over U.S. Patent Application Publication No. 2019/0196638 to Tominaga in view of U.S. Patent Application Publication No. 2008/0068516 to Mori. *Id*. at 229. Claims 2-8 were rejected under the same

[4] United States as Application No. 16/784,806 (“’806 Application”) was filed on February 7, 2020, published as U.S. Patent Application Publication No. 2020/0278571 A1, which included original claims 1-20, and issued as the ’025 patent.

combination, further in view of U.S. Patent Application Publication No. 2018/0120997 to Moon. *Id*. at 231.

In response, the applicant cancelled pending claims 2 and 10 and incorporating their requirements into claim 1. Ex. 1002 at 255 (*Office Action Response*, June 1, 2021). The applicant also amended pending claim 12 to recite the segment electrodes and dummy touch line limitations. *Id.* at 252, 255. The examiner allowed the claims on June 11, 2021. Ex. 1002 at 260-61 (*Notice of Allowance*, June 11, 2021); '025 patent, 1:45; Ex. 1003 ¶¶63-67.

C. Claim Construction

The Board construes claims under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*) and its progeny to have their plain and ordinary meaning in light of the specification. 415 F.3d at 1315-17. The Board only construes claim terms when necessary to resolve the controversy. *See, e.g.*, *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper 11 at 16 (PTAB Aug. 14, 2015).

Petitioner proposes one claim term for construction, discussed below:

1. "dummy touch line"

The term "dummy touch line" appears in Challenged Claims 10-11, 14, 17, and 18. The claims recite where the dummy touch line must be, in what direction it must extend, and to what it must not be connected. *See, e.g.*, Claims 10-11. A

construction is necessary because the claim provides no guidance to distinguish a "dummy touch line" from other lines. Petitioner therefore proposes "dummy touch line" be construed to mean "a line that does not carry a touch signal."

Consistent with the plain and ordinary meaning of "dummy," a POSITA would construe the term "dummy touch line" to refer to a line is non-functional as a touch line—essentially a fake touch line. Ex. 1003 ¶¶70-72; s*ee* Ex. 1013 (*Wiley Electrical and Electronics Engineering Dictionary* (2004)) at 3 (defining "dummy" as "[a] non-operational component, device, or piece of equipment which can be connected or installed as if it were a working component, device, or piece of equipment").

The '025 patent uses the term "dummy touch line" in this manner. For example, the specification explains "dummy touch line 60B" "does not contribute to detection of a touch position." '025 patent, 19:39-43; 20:5-6 (same).

VI. THE PRIOR ART

A. Kim

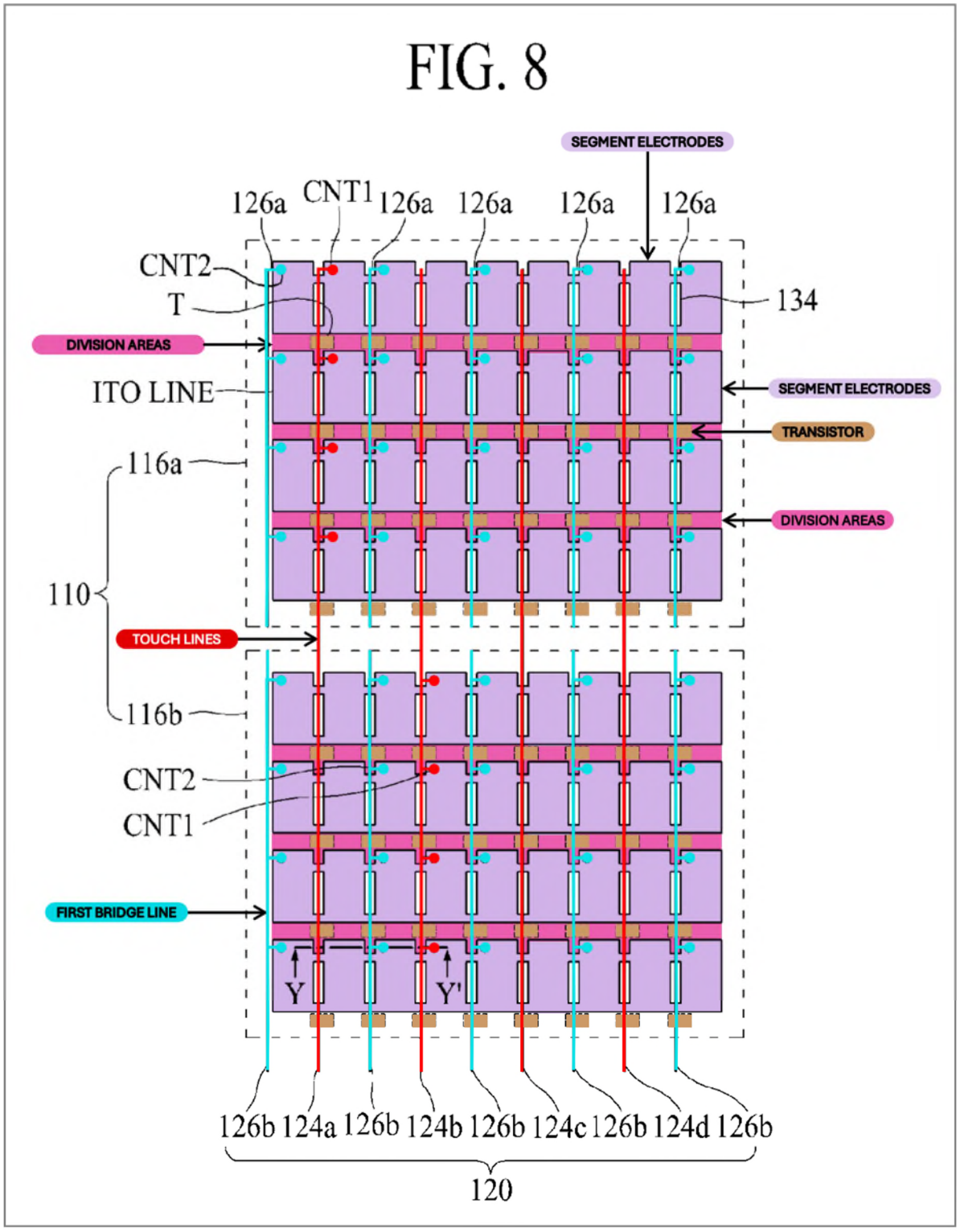
Kim is a published patent application entitled "Touch Display Apparatus." Kim at (54). Kim was published August 4, 2016, and claims priority to two Korean patent applications filed in 2015. Kim at (43), (30). Kim therefore is prior art to the '025 patent under at least 35 U.S.C. § 102(a)(1); Ex. 1003 ¶¶73-78.

Like the ’025 patent, Kim describes an in-cell type “touch sensitive display apparatus.” Kim at Abstract. Kim recognizes that image quality is degraded by the load deviation of touch electrodes found in prior art touch panels. Kim at [0017]-[0019]. Accordingly, Kim’s design “reduces a load deviation of a touch electrode, thereby enhancing image quality.” Kim at [0023].

Kim teaches two embodiments, both of which are modifications to the conventional touch panel including pixels, data lines, gate lines, common electrodes, and touch lines, depicted in Kim’s Figure 4. *See* Kim at [0074] (pixels), [0075] (gate lines and data lines), [0076] (common electrodes) and [0078] (touch lines). The two embodiments differ only regarding the structure of their common electrodes. Kim at [0099], [0117].

For Kim’s second embodiment, its common electrodes are made up of segments—“each touch electrode 110 includes multiple touch electrode lines made from ITO (ITO Line).” Kim at [0118]; Fig. 7. Like the ’025 patent, these ITO lines are linked together by “connecting lines” *i.e.*, bridge lines “that connect[] different ITO lines of a touch electrode 110 to each other.” Kim at [0120]. “By connecting together different ITO lines, the connecting lines 126 reduces an internal load deviation of each of the touch electrodes 110, and a load deviation between the plurality of touch electrodes 110 is reduced.” *Id.*

Kim's Figure 8 depicts this embodiment, showing two common electrodes made up of four (purple) ITO lines, *i.e.*, segment electrodes, each separated by (pink) gaps, *i.e.*, division areas, overlapping the (brown) thin film transistors, each common electrode is connected to a (red) touch signal line, and each ITO line within a common electrode is connected to the others via a (cyan) connecting/bridge line:


FIG. 8
SEGMENT ELECTRODES
126a
CNT1
126a
126a
126a
126a
CNT2
T
134
DIVISION AREAS
ITO LINE
SEGMENT ELECTRODES
TRANSISTOR
116a
DIVISION AREAS
110
TOUCH LINES
116b
CNT2
CNT1
FIRST BRIDGE LINE
Y
Y'
126b 124a 126b 124b 126b 124c 126b 124d 126b
120

Kim, Fig. 8.

B. Kim II

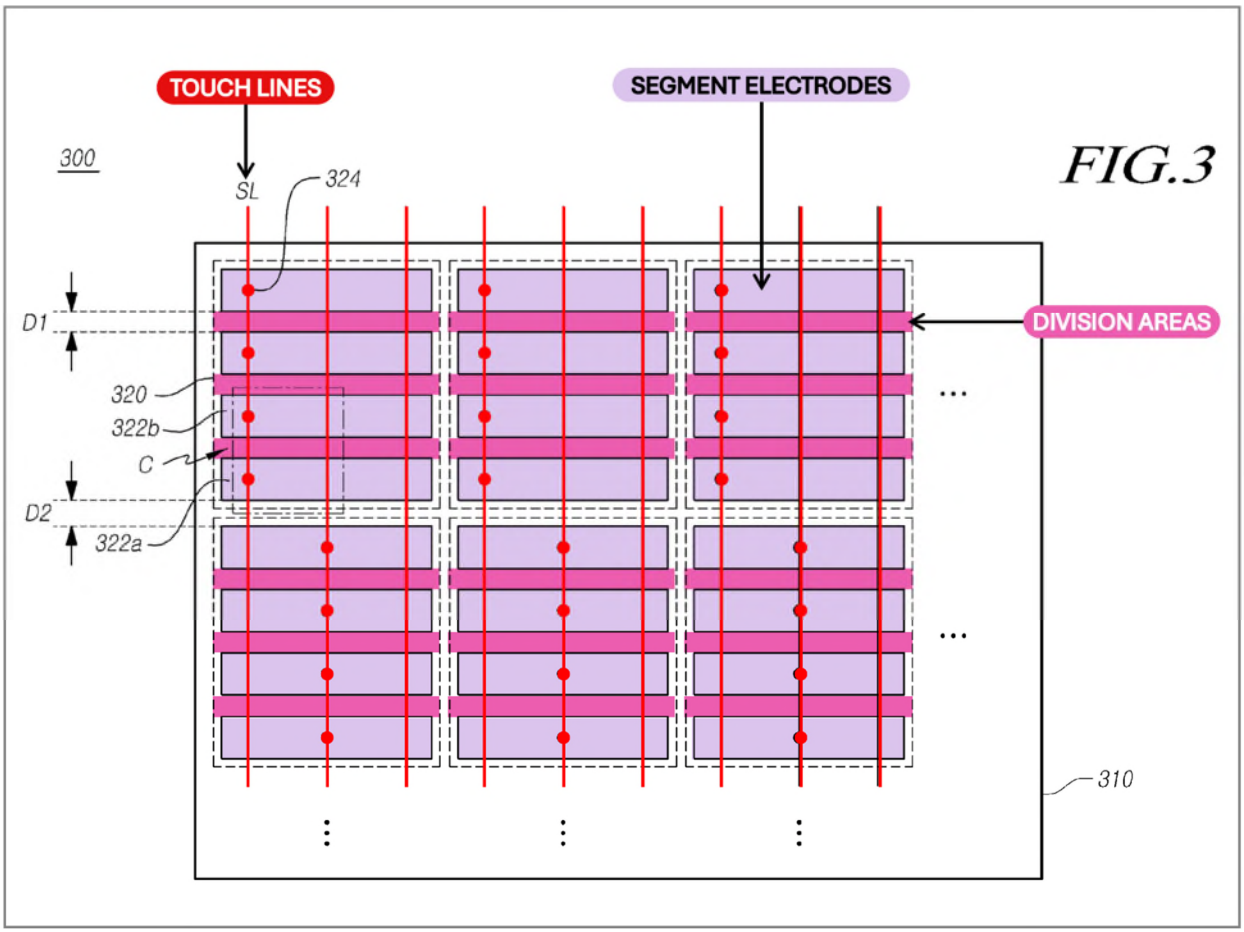
Kim II is a published patent application entitled "Touch-Integrated Display Device." Kim II at (54). Kim II was published July 6, 2017, and claims priority to a Korean patent application filed in 2015. Kim II at (43), (30). Kim II therefore is prior art under at least 35 U.S.C. § 102(a)(1). Ex. 1003 ¶¶79-83.

Kim II had the same applicant as Kim,[5] and also relates to in-cell touch panel technology, *i.e.*, "a touch-integrated display device in which a touch electrode is positioned inside a display panel." Kim II at [0003]. Kim II notes that in "conventional display panel[s]," large common electrodes overlaying multiple pixels cause capacitance issues that can distort the gate-source voltage of transistors (*i.e.*, the voltage needed to turn on the transistor) based on their location relative to the edge of the common electrode, which may hinder functionality of the gate activation process and cause display defects. Kim II at [0016]-[0017]. Like the '025 patent, Kim II prevents this by dividing its touch electrodes into rows of common voltage electrodes, with the gate lines running through the division areas between those rows. Kim II at [0018]-[0020], claims 5, 14. "By positioning the separation space 510 on the gate line GL, a capacitance of the gate electrode 518 may be decreased and the transistor TR may be driven at an increased speed."

[5] *See* Kim and Kim II at (71) (listing "LG Display Co., Ltd." as the applicant).

Kim II at [0090].

Figure 3 shows Kim II's common electrodes segmented into (purple) rows 322, with (pink) division areas between them. Kim II's Figure 5 embodiment (which builds upon Figure 3) shows that this division area is on the gate line. Kim II at [0090]. Figure 3 also shows that each touch electrode is connected to a particular (red) sensing line SL.



Kim II, Fig. 3.

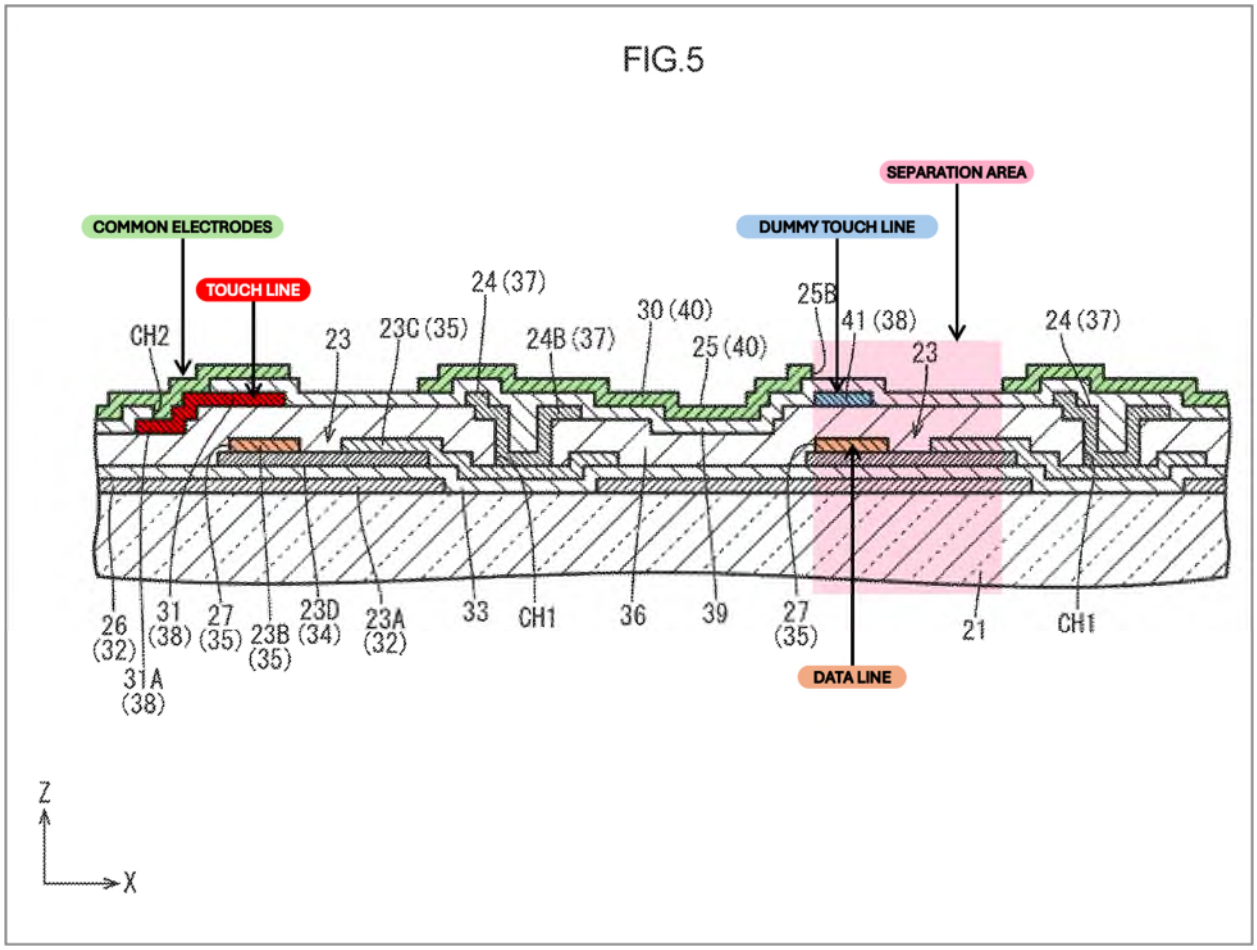
C. Yoshida

Yoshida is a U.S. Patent Application entitled "Position Input Device." Yoshida at (54). It was published September 26, 2019 and claims priority to Japanese Application JP2018-058356, which was filed on March 26, 2018. Yoshida at (43), (30). A certified copy of Japanese Application JP2018-058356 was provided to the U.S. Patent Office, and a certified translation of that application is included herewith as Exhibit 1009. Yoshida was filed within 12 months of the date that its Japanese counterpart was filed in Japan, and while its Japanese counterpart was still pending. Yoshida at (22); Translation at pg. 3, [Date Submitted/Filed in Japan]. Yoshida's Japanese counterpart lists the same inventor as Yoshida. Translation at pg. 3, [Name]. Yoshida also properly identified its Japanese counterpart in its application. 35 U.S.C. §§ 119(a), (b)(1). Yoshida therefore meets the "ministerial requirements" to claim priority to its Japanese counterpart. *See Penumbra, Inc. v. RapidPulse, Inc.*, IPR2021-01466, Paper 34 (PTAB March 10, 2023) at 32; Ex. 1003 ¶¶84-91.

Yoshida's Japanese counterpart also "describes the subject matter" relied upon in Yoshida as prior art. *Id.*; 35 U.S.C. § 102(d). As is evident from the Translation, Yoshida's Japanese counterpart includes the same subject matter as Yoshida, with only minor differences in paragraph numbering and wording that are likely attributable to translator discretion. *See* Ex. 1003 ¶¶85-87. Parallel citations

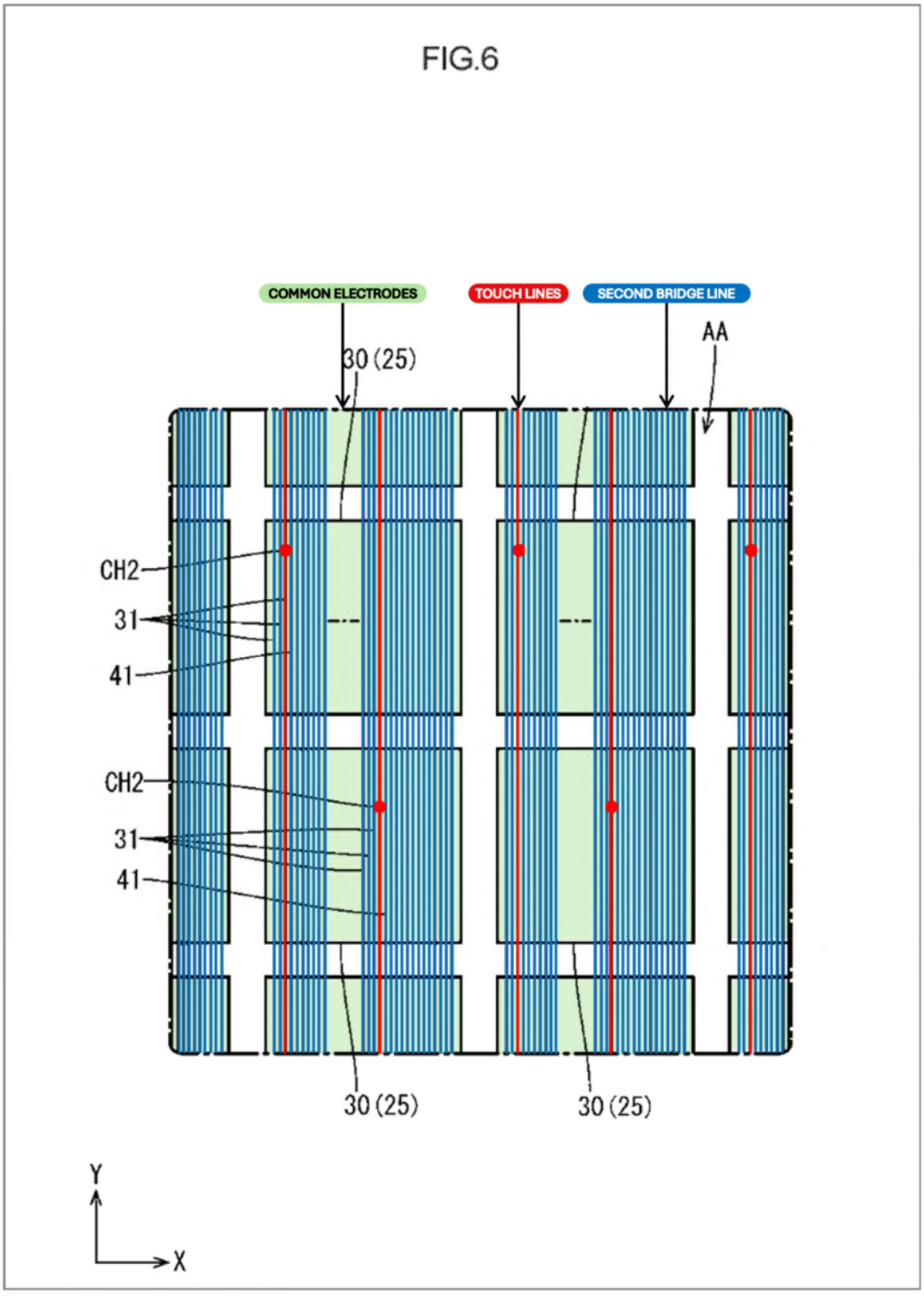
to both Yoshida and the Translation are provided throughout this Petition to demonstrate this common material. *See Penumbra,* IPR2021-01466, Paper 34 at 32-35 (establishing a reference as prior art based on entitlement to earlier references based on the same showing). Yoshida is therefore prior art under 35 U.S.C. § 102(a)(2).

As with the other references discussed in this Petition, Yoshida discloses an in-cell touch panel device using horizontal gate lines, vertical data lines, touch electrodes, and touch lines. Yoshida at [0028]; Translation at [0016]. Yoshida also discloses "spare touch lines" that can be connected to a touch electrode to replace a faulty touch line. Yoshida at [0035]; Translation at [0023]. Like the claimed dummy touch lines, these (blue) spare touchlines 41 can be in the (pink) area between (green) common electrodes 30 so that they overlap the (orange) source (data) line 27. Yoshida at [0035], [0038]; Translation at [0023], [0026]. This is depicted from a cross-sectional view in Figure 5:



Yoshida, Fig. 5; *see also* Translation, Fig. 5. Further, for its third embodiment, Yoshida explains that these spare touch lines positioned between common electrodes can be supplied by a "terminal portion 55" with "the same common signal supplied to the common electrode." Yoshida at [0062], [0065]; *see also* Translation at [0050], [0053]. This, Yoshida explains, helps stabilize this area, which is otherwise exposed to potentially destabilizing electric fields between the common and pixel electrodes. *Id.*

Yoshida also explains that some of its (blue) spare touchlines can overlap the touch electrodes, as shown in Figure 6:



Yoshida, Fig. 6; Translation at Fig. 6.

VII. THE CHALLENGED '025 PATENT CLAIMS ARE UNPATENTABLE OVER THE PRIOR ART

A. GROUND 1: Claims 1-3, 6, and 9 Are Obvious in View of Kim and Kim II.

Kim, alone and in combination with Kim II, discloses and renders obvious every limitation of '025 patent Claims 1-3, 6 and 9. This ground relies on Kim's second embodiment, which does not expressly describe having a "division area" between segment electrodes "on the gate line" as claimed. As explained below, a POSITA would nonetheless find it obvious that the division area is on, or would be obvious to place on, the gate line based Kim's first embodiment, which does describe the gate line being in the "division area," and which would be understood to have the same underlying structure as Kim's second embodiment. Ex. 1003 ¶¶97, 130-134. A POSITA would also have been motivated to combine Kim and Kim II's teachings regarding the several benefits to positioning the division area on the gate line in in-cell touch panel products. Ex. 1003 ¶¶98, 135-145. A detailed discussion of the motivation to combine these references is provided in the analysis below.

1. Independent Claim 1

Claim 1 is obvious in view of Kim alone and combined with Kim II.

a) [1-PRE]

To the extent that the preamble is limiting, Kim teaches, or at least renders

obvious, the preamble. Kim discloses an "*in-cell touch panel*,"[6] as a "touch sensitive display apparatus." Kim at Abstract, [0007] ("a touch sensor [that] is built into a liquid crystal panel in the in-cell touch type").

Kim further explains that its touch panel has "*an image display area made up of pixels arranged in a first direction and a second direction intersecting the first direction.*" Kim describes its "touch sensitive panel" as including "a liquid crystal layer" that includes a "plurality of pixels" arranged in a "matrix type," *i.e.*, arranged in rows and columns. Kim at [0072]-[0074]; Ex. 1003 ¶¶100-103.

For purposes of this claim mapping, the "*first direction*" will refer to horizontal rows and the second "*second direction*" will refer to vertical columns relative to the orientation of Kim's figures.

b) [1-A]

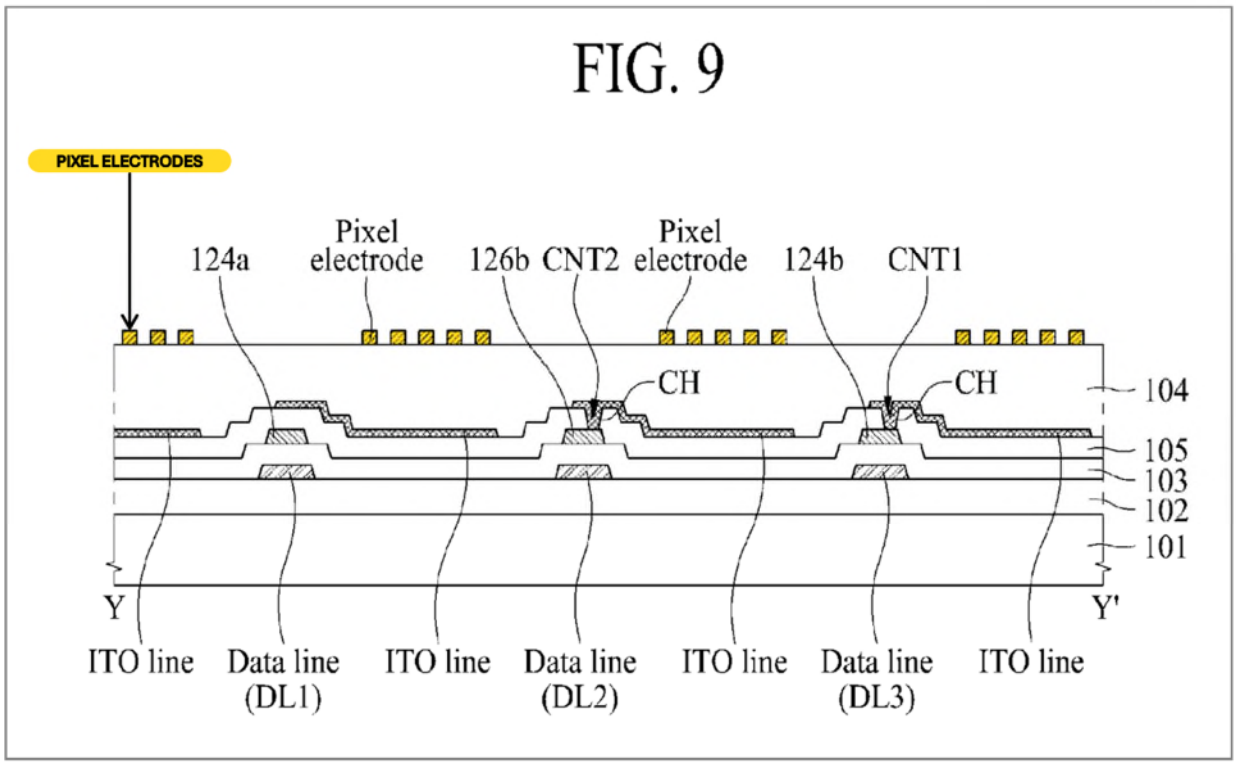
Kim teaches, or at least renders obvious, "*transistors and pixel electrodes respectively provided in the pixels*." Because Kim teaches a panel having an LCD display, a POSITA would understand it necessarily includes pixels provided with transistors and pixel electrodes. Ex. 1003 ¶104. Kim expressly teaches that each pixel has a "thin film transistor," or "TFT." Kim at [0036]. These TFTs form an array and are arranged in a matrix that corresponds to the pixels. Kim at [0074],

[6] Text in red italics indicates verbatim claim language throughout.

[0075]; *see also* [0112] ("For example, as illustrated in FIG. 6, each of the plurality of slits 114 may be disposed in an area where a thin film transistor (TFT) T driving a corresponding pixel P is disposed."); Ex. 1003 ¶105.

Kim further teaches "*pixel electrodes respectively provided in the pixels*." Specifically, Kim teaches "[t]he plurality of pixels may be defined by a plurality of data lines and a plurality of gate lines which intersect each other. A TFT [*i.e.*, a transistor], a pixel electrode, and a storage capacitor (Cst) may be disposed in each of a plurality of areas defined by intersections of the data lines and the gate lines." Kim at [0075]; Ex. 1003 ¶¶106-107.

These forked pixel electrodes (yellow) can be seen in Kim's Figure 9:



Kim. Fig. 9.

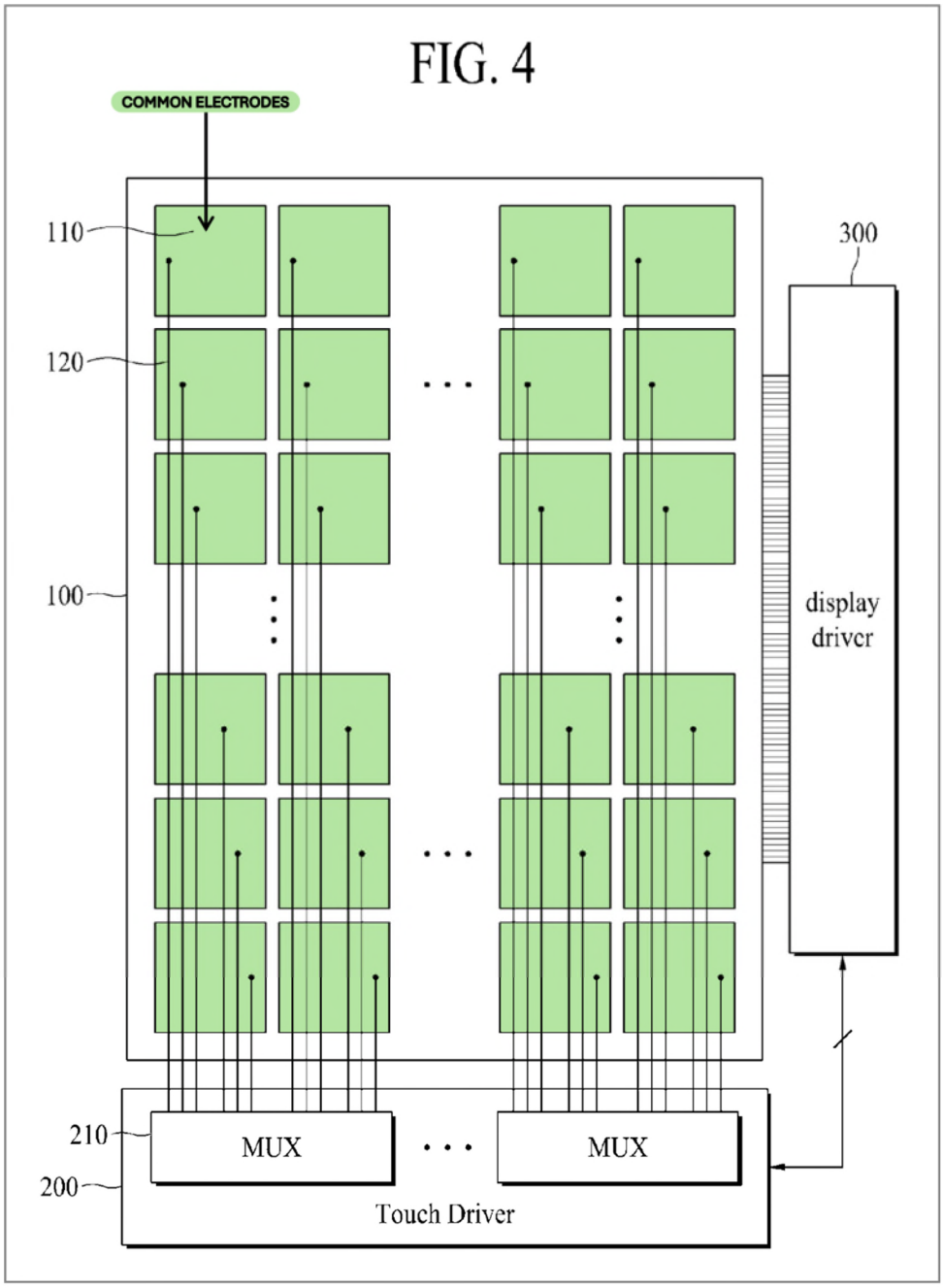
c) [1-B]

Kim teaches, or at least renders obvious "*common electrodes arranged in the first direction and the second direction, respectively facing one or more of the pixel electrodes and provided separately from each other*." Kim teaches that its touch panel includes a plurality of "common electrode[s]" that "may be used as the touch electrode[s]." Kim at [0076]. Kim explains that these common electrodes are supplied a common voltage (Vcom) via the touch signal lines, thus rendering them common electrodes. Kim at [0080], Ex. 1003 ¶¶108-109.

Kim's common electrodes are "*arranged in both the first and second direction*": "For example, twenty touch electrodes 110 are disposed in a horizontal direction, and thirty-two touch electrodes 110 are disposed in a vertical direction in the touch sensitive panel, namely, a total of 640 touch electrodes 110 are disposed in the touch sensitive panel 100." Kim at [0077]; Ex. 1003 ¶110.

Kim's common electrodes "*respectively fac[e] … the pixel electrodes.*" Kim explains that "the plurality of touch electrodes 110" may be provided "by patterning the common electrodes in units of pixels," with each pixel containing a pixel electrode. Kim at [0076]; *See also* Kim at [0078] ("Each touch electrode 110 is shared by a respective block of pixels (not shown) and serves as the display electrode for the respective block of pixels."); Ex. 1003 ¶111.

Finally, Kim teaches that the (green) touch electrodes 110 are "*provided separately from each other*," as depicted in Kim's Figure 4, below:



Kim, Fig. 4; *see also* Figs. 7 and 8 (depicting the second embodiment's separate common electrodes); Ex. 1003 ¶112.

d) [1-C]

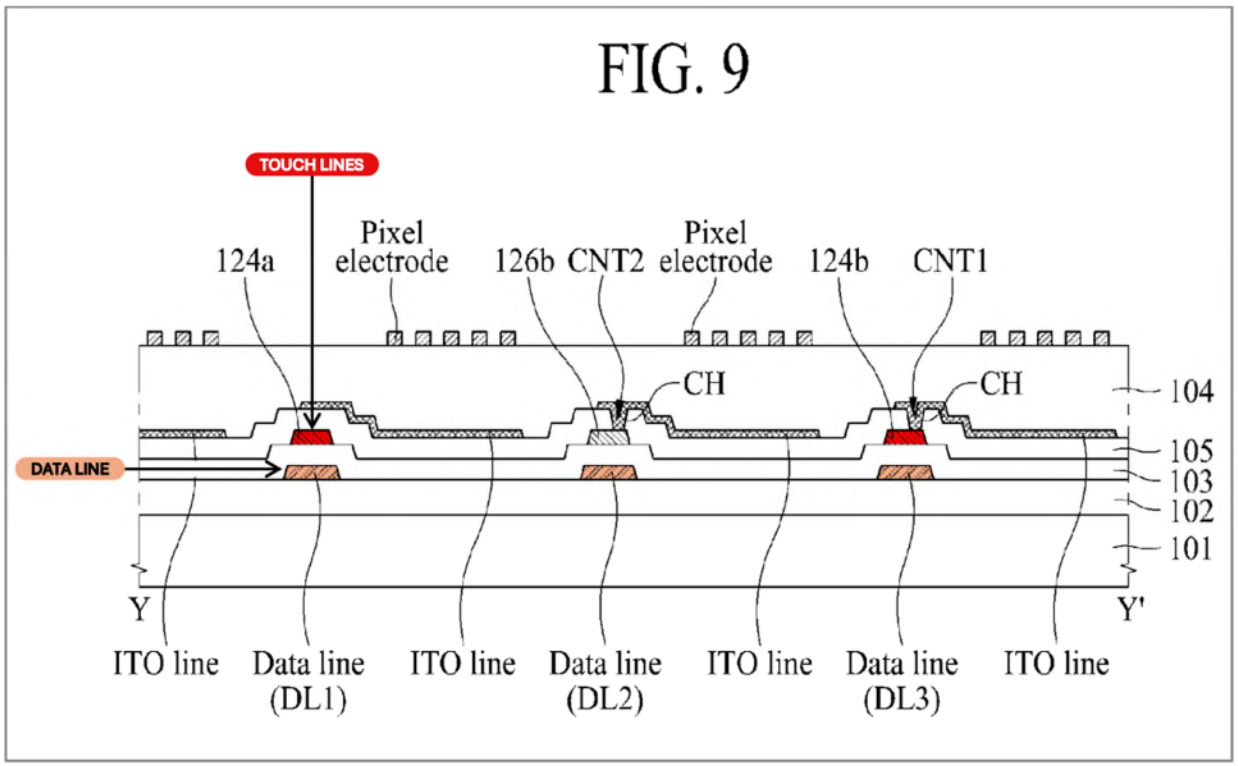
Kim teaches, or at least renders obvious, "*gate lines that extend along the first direction and supply gate signals to the transistors respectively*."

Kim teaches that its gate lines "*supply gate signals to the transistors respectively*." Kim explains that "[t]he gate driver may sequentially supply the gate driving signal to the plurality of gate lines included in the liquid crystal panel during the display period in one frame period" and that these gate signals are provided to the "TFT" *i.e.*, transistor "included in each of the plurality of pixels." Kim at [0089]; Ex. 1003 ¶¶113-114.

Kim also teaches, or at least renders obvious, that its gate lines "*extend along the first direction*," *i.e.* horizontal. Horizontal gate lines have been a conventional part of the LCD design for decades, so a POSITA would understand that the gate lines extend in the first direction. Ex. 1003 ¶¶115-118. Kim teaches that the gate lines intersect with the data lines. Kim at [0075]. Because, as explained below, the data lines run vertically, a POSITA would understand that the gate lines must run horizontally. *Id.*; *see also* Kim at [0114] (explaining that the substantially similar Figure 6 embodiment depicts two unit touch electrodes adjacent to each other along the necessarily horizontal gate line).

e) [1-D]

Kim teaches, or at least renders obvious, "*data lines that extend along the second direction and supply data signals to the transistors respectively*." Ex. 1003 ¶¶119-122. Kim teaches expressly that its touch signal lines "*extend along the second direction*," i.e., vertically (Kim at [0118], Figs. 4, 7 and 8), and teaches that its data lines are parallel to the touch lines. Specifically, Kim's Figure 9 shows a cross-sectional view of Kim's second embodiment, and the (orange) data lines extending in the direction parallel to the vertical touch signal lines (shown in red) discussed generally below. Figure 9 therefore demonstrates that the data lines likewise extend along the claimed, vertical "*second direction*."



Kim, Fig. 9; *see also* [0145] (stating that "data lines oriented in the same direction as the touch signal lines 120"); [0114]-[0115] (explaining that bridges B2 can bridge over the data lines). Kim teaches that its touch panel includes data lines that intersect with the gate lines and therefore extend in the "*second direction*." Kim at [0075] (describing pixel areas as being defined by "intersections of the data lines and the gate lines."). Ex. 1003 ¶¶121-122.

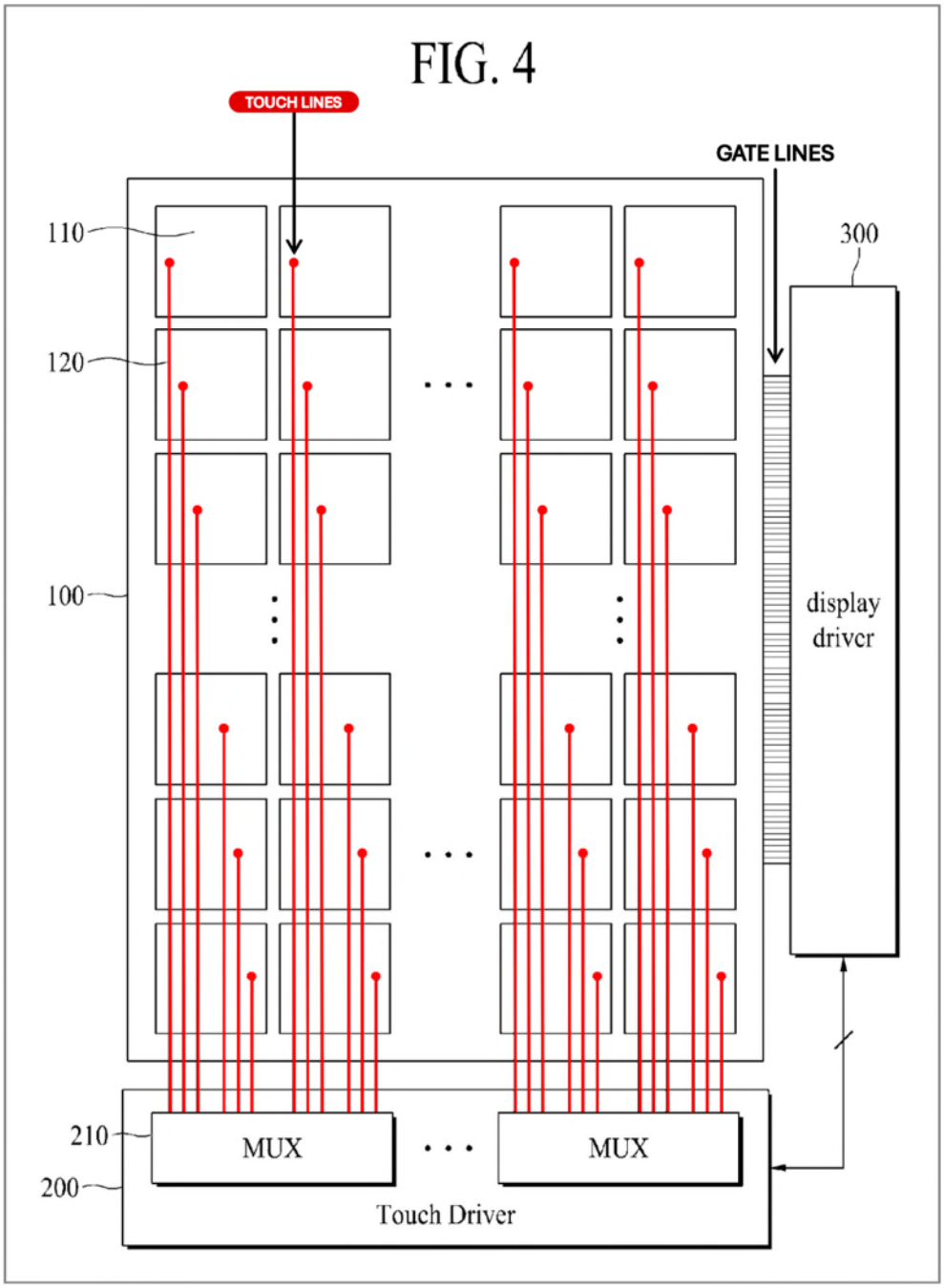
Kim makes clear that this intersection occurs at the transistor (*id.*) and further explains that these data lines provide "*data signals to the transistors respectively*," as the claim requires. Kim at [0090] (explaining that data lines carry data voltages to the TFT); Ex. 1003 ¶120.

f) [1-E]

Kim teaches and renders obvious "*touch lines that extend along the second direction and are each connected to a corresponding one of the common electrodes.*" Kim teaches that "[e]ach of the touch electrodes 110" *i.e.*, common electrodes "may be connected to a corresponding channel of the touch driver 200 through a corresponding touch signal line 120 among a plurality of touch signal lines 120." Kim at [0078]; Fig. 4. Kim further discloses that each touch line may be "*connected to a corresponding one*" of the touch electrodes. *See* Kim at [119] (explaining that "each of the plurality of touch electrodes 110 may be connected to one or more touch signal lines 120 through a plurality of first contacts CNT1 at different locations"); *see also* Fig. 4 (showing each touch line connecting to a corresponding one touch electrode).[7]

Kim further teaches that these touch signal lines "*extend along the second direction*," *i.e.*, vertically (Kim at [0118]) and shows these (red) lines in Figure 4, below:

[7] For Kim's second embodiment, certain of these touch signal lines are referred to as "touch signal lines 124." Kim at [0118]; Fig. 7 (showing touch line 124a and 124b connecting to only one of the two depicted touch electrodes); Fig. 8 (same).

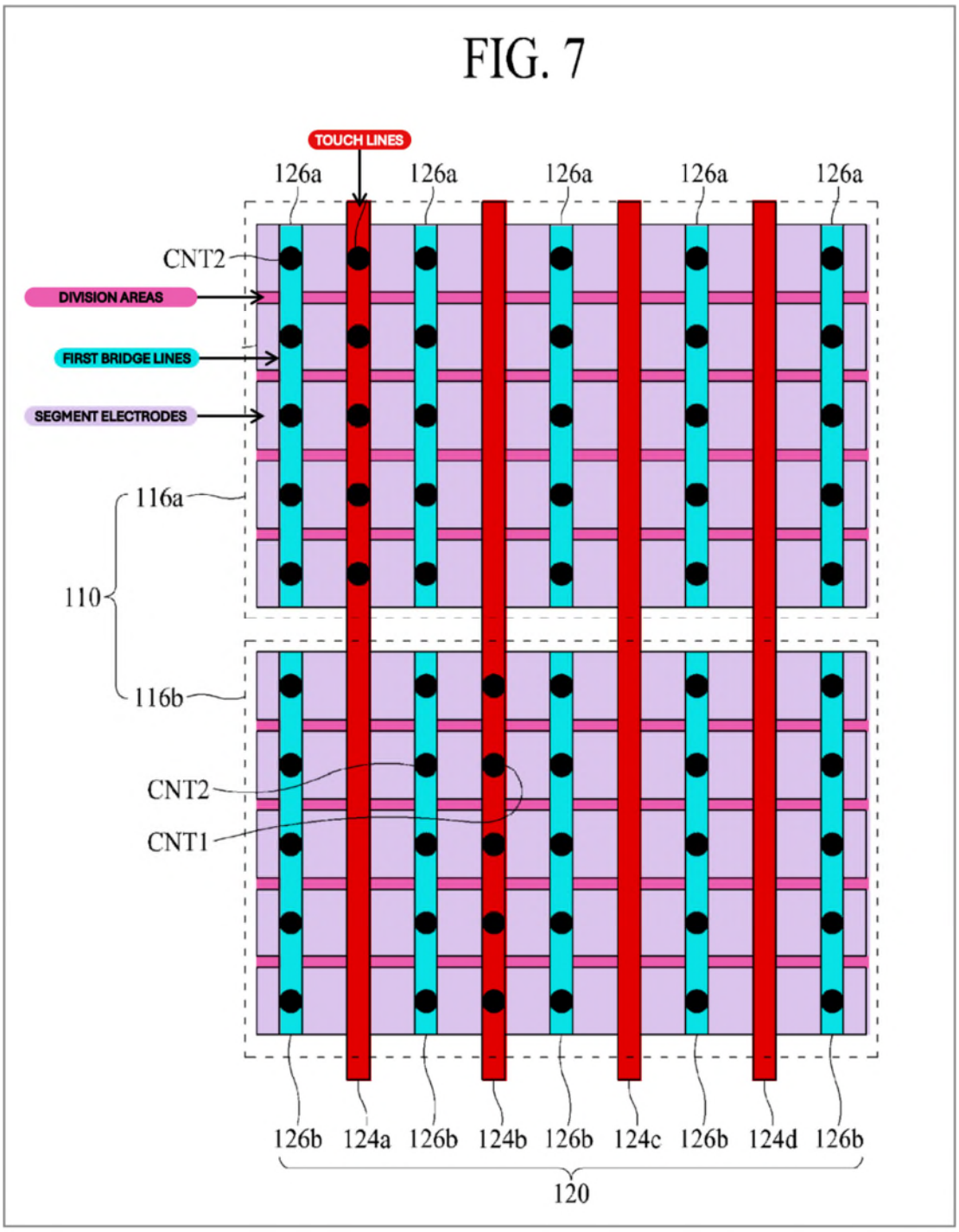


Kim, Fig. 4; *see also* Figs. 7 and 8 (showing vertical touch signal lines 124); [0145] (touch lines extend in the same direction as data lines); Ex. 1003 ¶¶123-125.

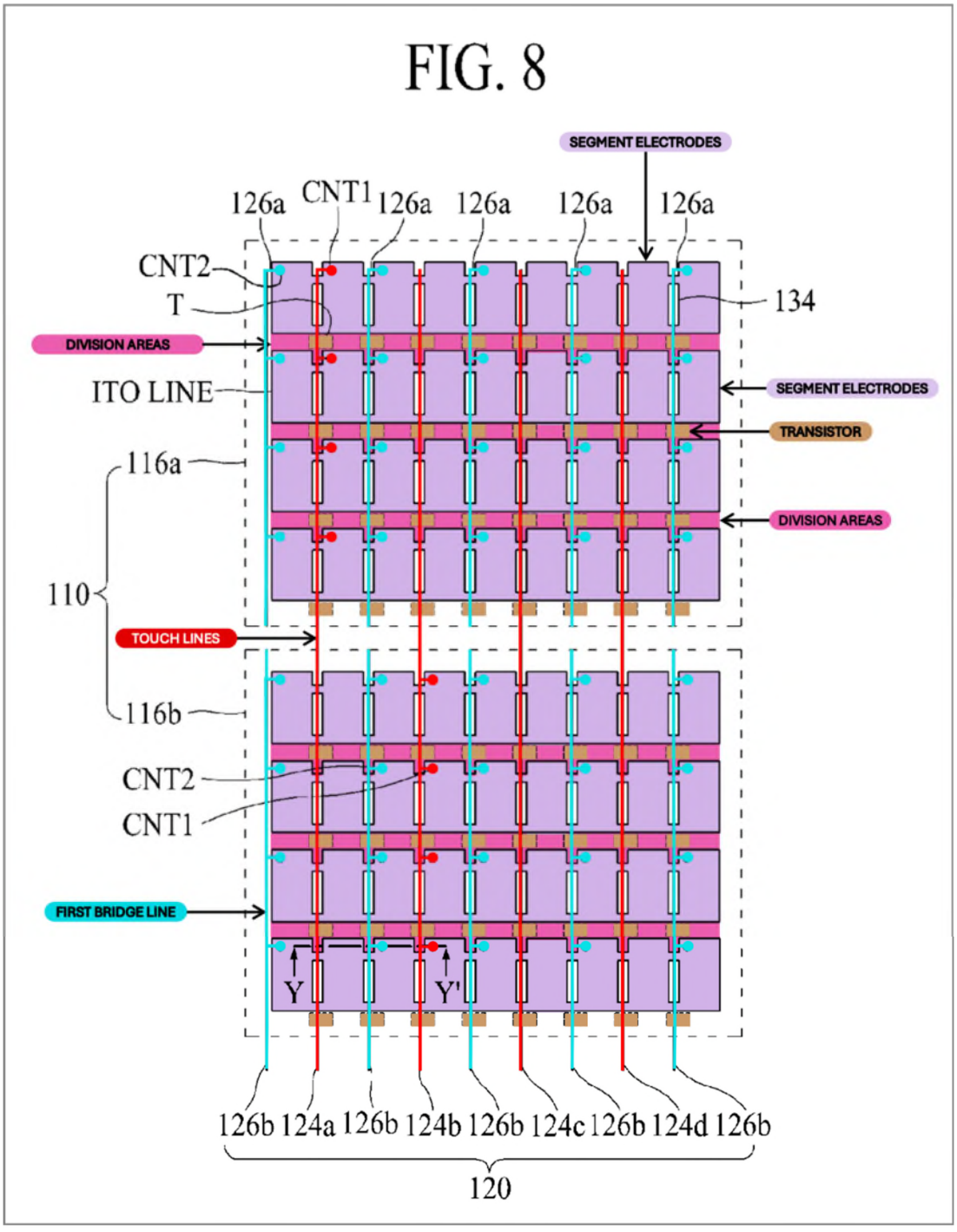
g) [1-F] and [1-G]

Kim both alone and in combination with Kim II teaches and renders obvious "*a first bridge line laterally bridging two of the segment electrodes adjacent in the second direction across one of the division areas, wherein each common electrode has segment electrodes divided with a division area on the gate line*."

Focusing on the "wherein" clause, Kim teaches "common electrodes" having "segment electrodes" divided with a "division area." In Kim's second embodiment, the "touch electrodes 110" *i.e.*, common electrodes, are divided into "multiple touch electrode lines made from ITO (ITO Line)," each of which corresponds to the claimed "*segment electrode*." Kim at [0118], [0142]. These "ITO lines extend in the horizontal direction and are parallel to each other," *Id.*; *see also* Fig. 7. These (purple) ITO lines are set apart from one another by a small distance, *i.e.*, a (pink) division area.



Kim, Fig. 7. Figure 8 depicts these elements in greater detail.



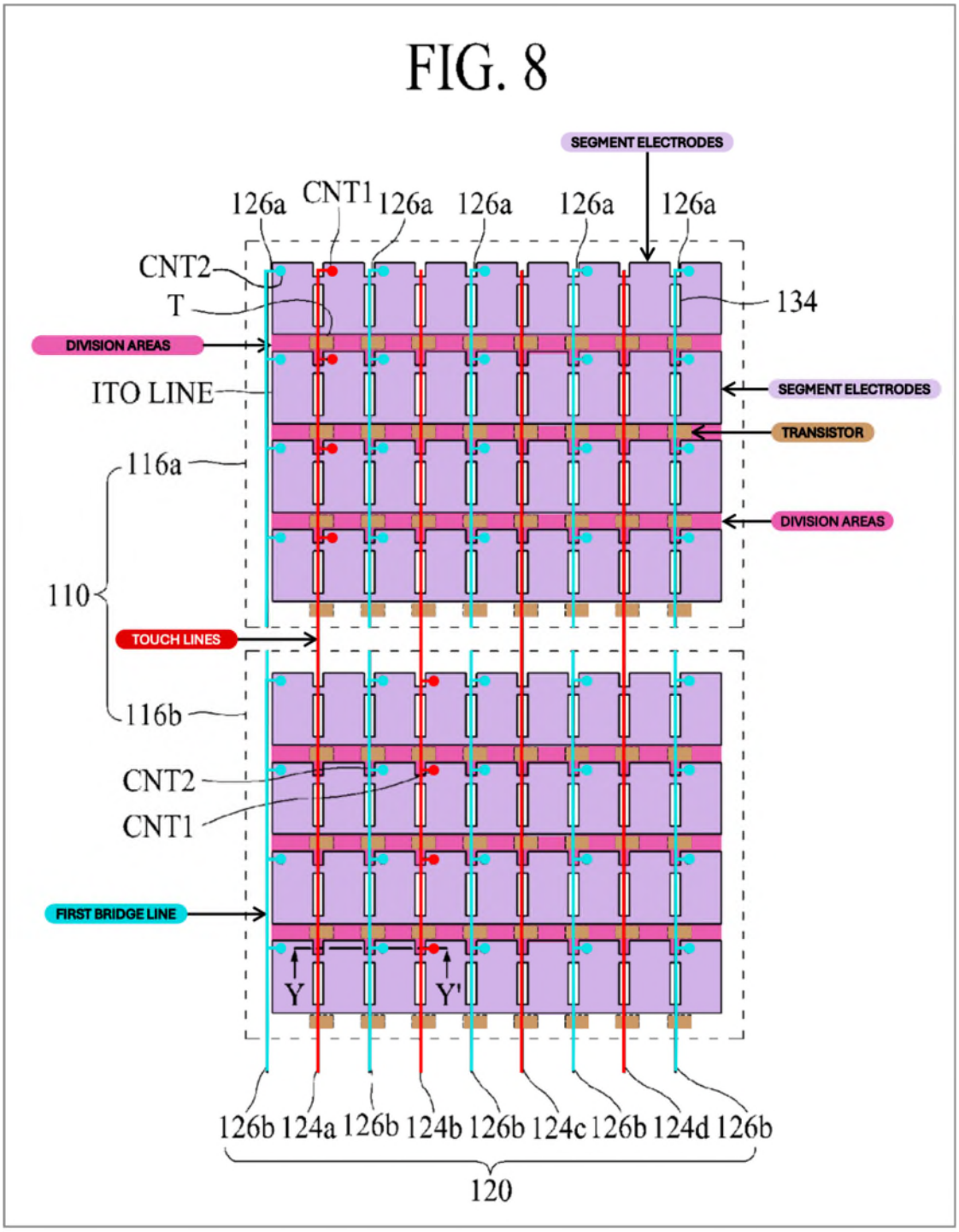
Kim, Fig. 8; Ex. 1003 ¶¶126-127.

Kim further teaches "*a first bridge line laterally bridging two of the segment electrodes adjacent in the second direction across one of the division areas*." Specifically, Kim teaches "connecting lines 126," which Kim describes as "a line of conductive material that connects different ITO lines of a touch electrode 110 to each other." Kim at [0120]. These "connecting lines 126 extend in a vertical direction and are perpendicular to and intersect the ITO lines" *i.e.*, the segment electrodes. Kim at [0118]. The "connecting lines" therefore "*laterally bridge*" at least two of the segment electrodes in the "*second direction*," *i.e.*, vertically crossing the division areas between segment electrodes. *See* Kim at [0120]. Figures 7 and 8 depict several (cyan) connecting lines 126 crossing the (pink) division area between (purple) ITO lines to laterally bridge adjacent ITO lines. Ex. 1003 ¶128.

Finally, Kim alone and in combination with Kim II teaches, or at least renders obvious, that the "*division areas*" between segment electrodes being "*on the gate line*." Ex. 1003 ¶¶129-145.

First, in Kim's second embodiment, a POSITA would understand, or at least find obvious, that the division areas between segment electrodes are on the gate line. As explained above, Kim teaches that its gate lines run horizontally and supply signals to Kim's transistors. *See supra* Section VII.A.1.c. Kim further

teaches, in connection with its second embodiment, that the (brown) transistors are in the (pink) division area:

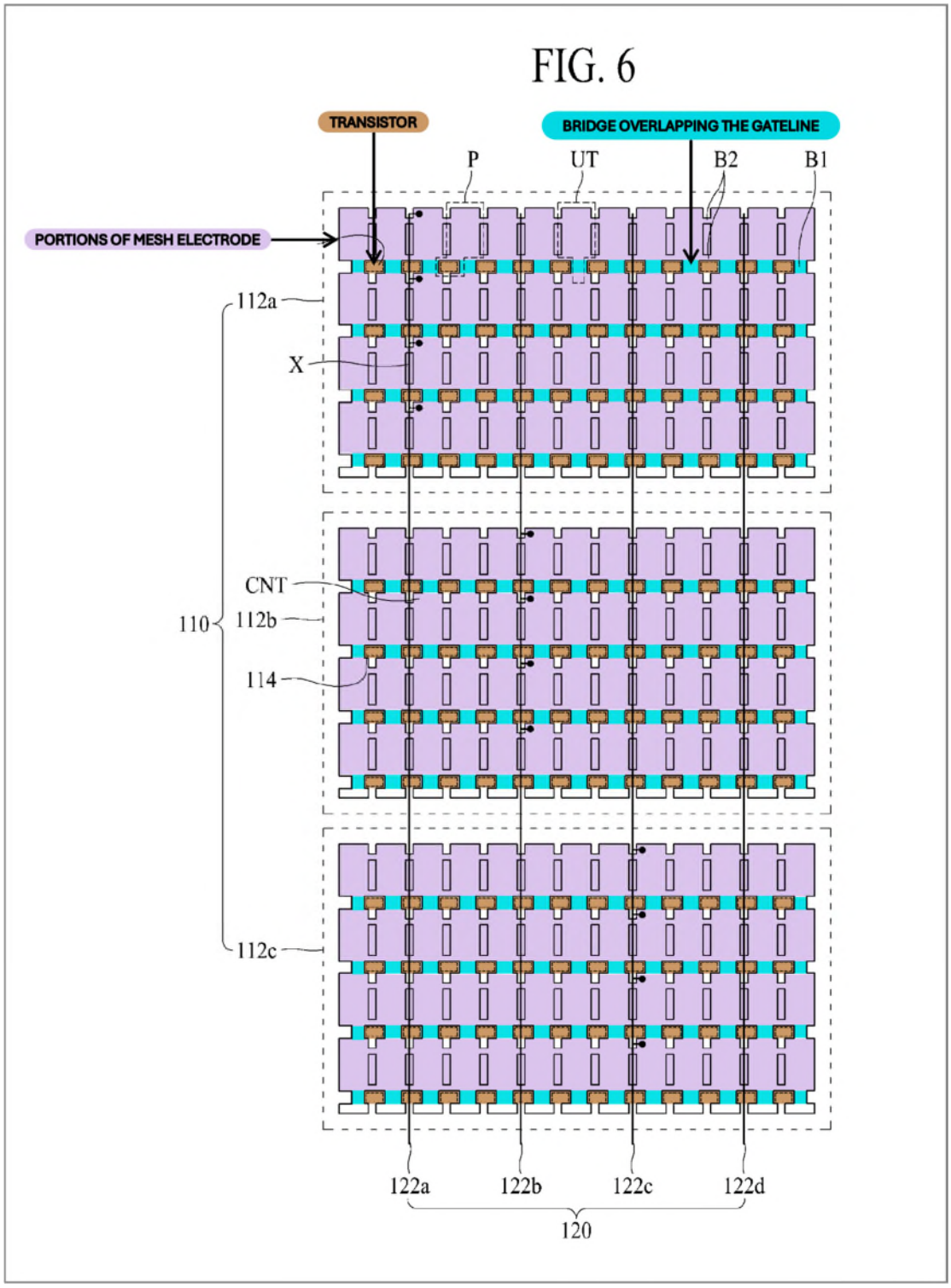


Kim, Fig. 8. Thus, based on Kim's second embodiment alone, a POSITA would understand, or at least find it obvious, that the horizontal gate lines would take the most direct, straight path through the division area to connect to the transistors, such that the division area would be on the gate line as the claim requires. Ex. 1003 ¶130.

Second, the disclosures relating to Kim's substantially similar first embodiment also make clear that the "*division area*" in Kim's second embodiment would be, or would be obvious to place, on the gate line. Specifically, Kim's first embodiment teaches a mesh-like touch electrode without segment rows or "*division areas*." *See generally* Kim, Fig. 6. While the first and second embodiment differ regarding their touch electrode structure and the use of bridge lines, Kim never teaches any differences regarding the placement of transistors, gate lines, or data lines. *See, e.g.*, Kim at [0099], [0117] (describing the first and second embodiments based on the structures of their touch electrodes). Accordingly, a POSITA would understand that the structure of the underlying display components is, or would obviously be, identical in both embodiments. Ex. 1003 ¶¶131-133.

A POSITA would thus understand, or find it obvious, that the placement of gate lines in connection with Kim's first embodiment likewise teaches the position of gate lines in Kim's second embodiment, meaning the division areas of Kim's

second embodiment would be "*on the gate line*" as the claim requires. Kim's first embodiment is depicted in Figure 6, and teaches vertical "bridges B1" and horizontal "bridges B2" to connect the portions of a particular touch electrode. Kim at [0114]. These "bridges B1" bridge the area that aligns with the horizonal row of transistors, which is the same portion of the panel that corresponds to the "division area" of Kim's second embodiment. *See* Kim, Fig. 6. Kim explains that this portion is where the gate line is located—"bridges B1 may electrically connect two unit touch electrodes UT which are adjacent to each ***other along a corresponding gate line***." Kim at [0114] (emphasis added). Kim explains that "bridges B1 may be disposed to ***overlap the gate lines***." Kim at [0115] (emphasis added). This is depicted in Figure 6:



Kim, Fig. 6. Accordingly, given that Kim's first and second embodiments differ only with regard to the structure of their common electrodes, a POSITA would

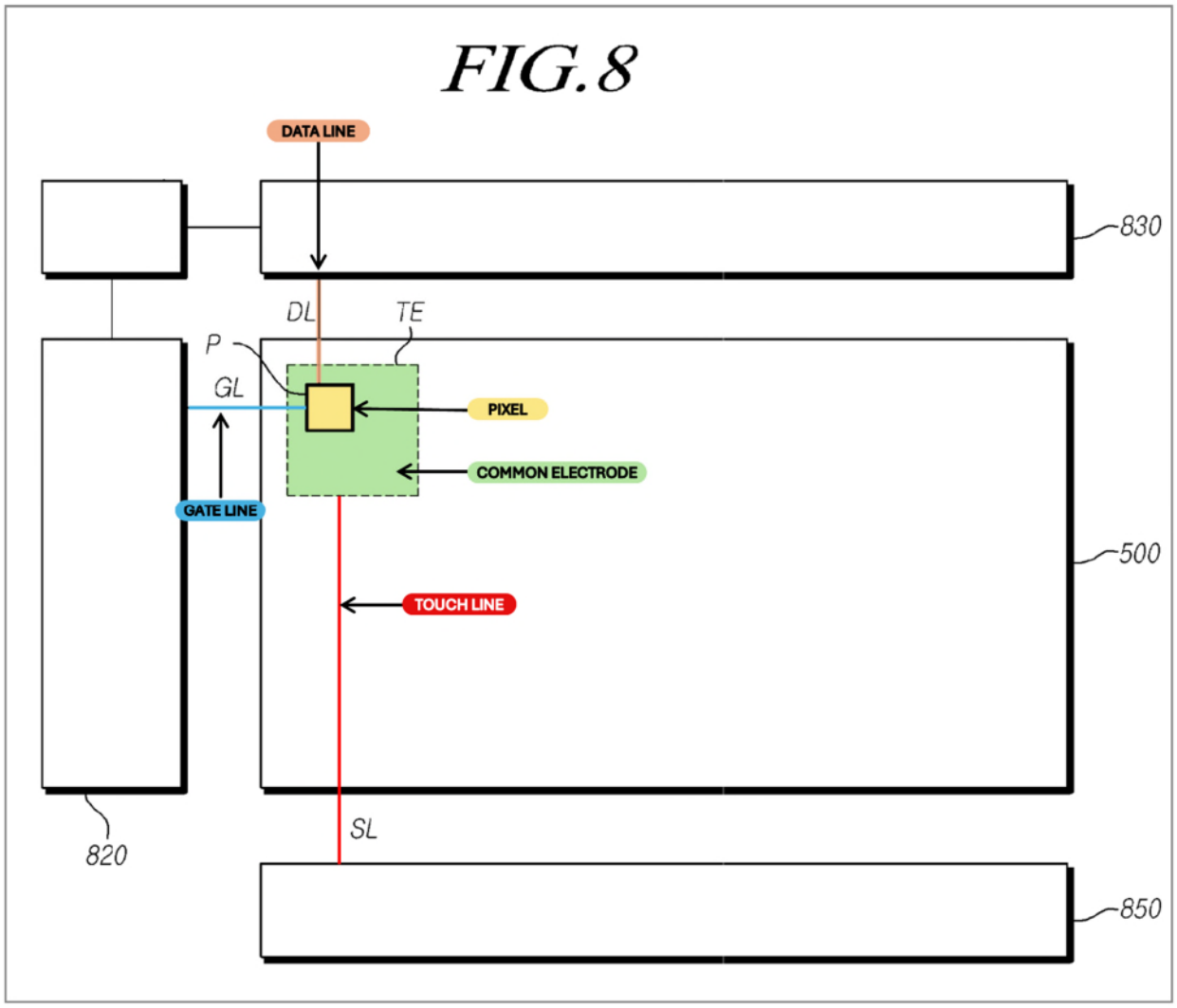
understand that Kim's teachings regarding its first embodiment confirm that the "*division area*" between ITO line segment electrodes taught by Kim's second embodiment is, or would be obvious to place, "*on the gate line*." Ex. 1003 ¶¶131-133.

Further, a POSITA would have additionally understood that Kim's "*division area[s]*" are, or would be obvious to place, "*on the gate line*" based on Kim's teachings regarding the benefits of slits 114. Regarding its first embodiment, Kim explains that the touch electrodes contain vertical "slits 114" bridged by the bridges B2, as well as "slits 114" that are over the transistors. Kim at [0028], [0100]-[0101], [0111]-[0112] (explaining that these slits 114 are in the "non-display area" to avoid interference with the pixel electrode's electric field during display driving" and can be located "where a thin film transistor" is present). Kim explains that these slits correspond to the location of the touch line, and as a result "a load in each of the touch electrodes is reduced, and an overlap capacitance between a corresponding touch signal line and a corresponding touch electrode is reduced." Kim at [0116]. Thus, just as bridges B2 bridge the vertically-extending "slit" non-display area with the touch line and data line, a POSITA would recognize that bridges B1 bridge the horizontally-extending "slit" non-display area corresponding to the "*division area*" of Kim's second embodiment where the gate line is (or would obviously be) positioned to obtain the same benefits of reducing

overlap capacitance and furthering Kim's goal of avoiding an "effect" on display driving. Kim at [0116], [0100], Ex. 1003 ¶134.

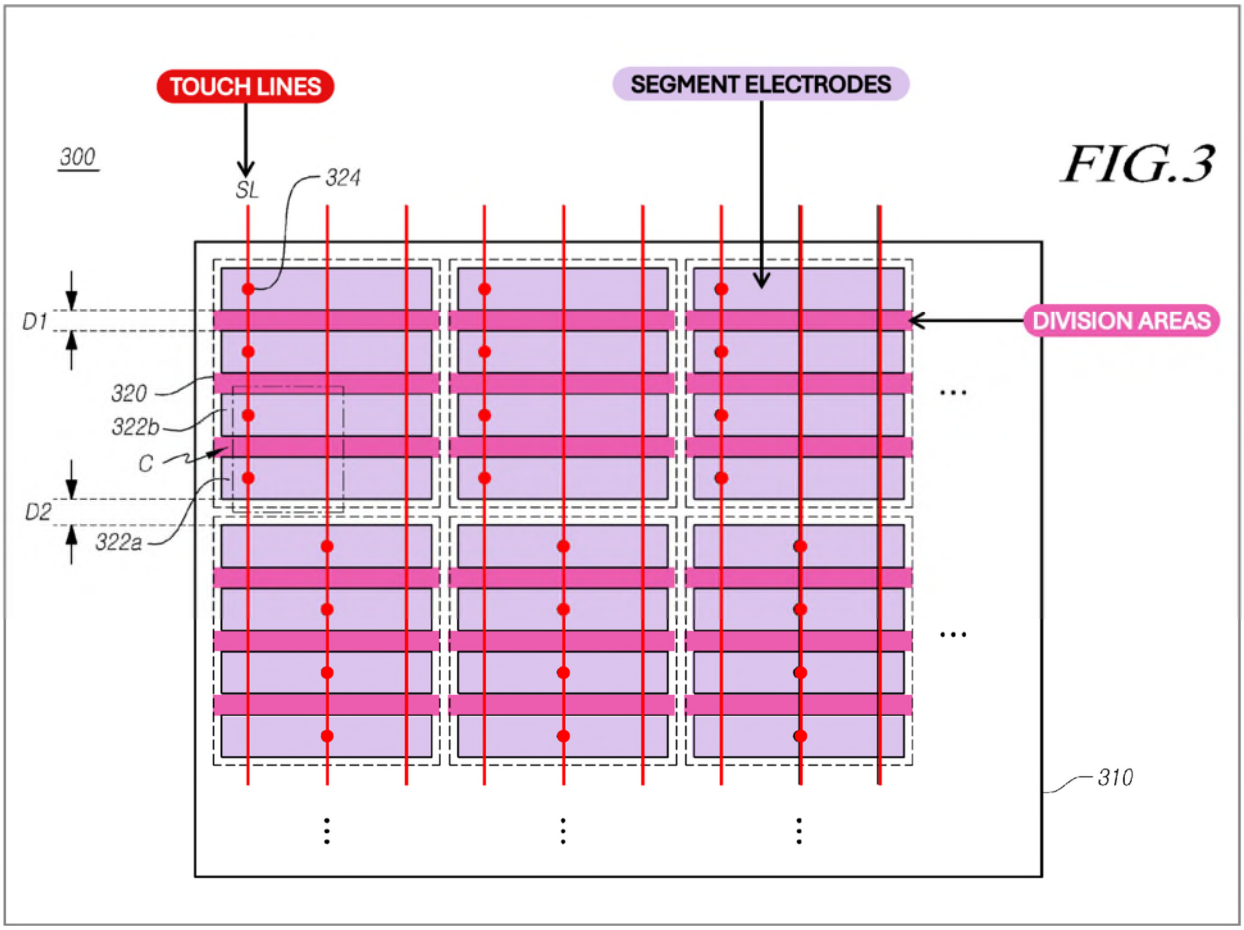
Finally, a POSITA reading Kim would have also found it obvious to position the "*division area on the gate line*" in light of Kim II because it provides extensive disclosure of this concept. Ex. 1003 ¶¶135-145.

Kim II has the same applicant and disclosed a similar touch panel as Kim. Both have horizontal (blue) gate lines GL, vertical (orange) data lines DL, and vertical (red) touch lines (called "sensing lines SL"). *See* Kim II at [0008] (gate lines and data lines intersect at the transistor of a pixel); [0022] (sensing lines overlap with the data lines). Kim II teaches that its panel includes (green) touch electrodes, *i.e.*, common electrodes, that are "disposed over a plurality of pixel areas." Kim II at [0013]. These elements can be seen below in Kim II's Figure 8.

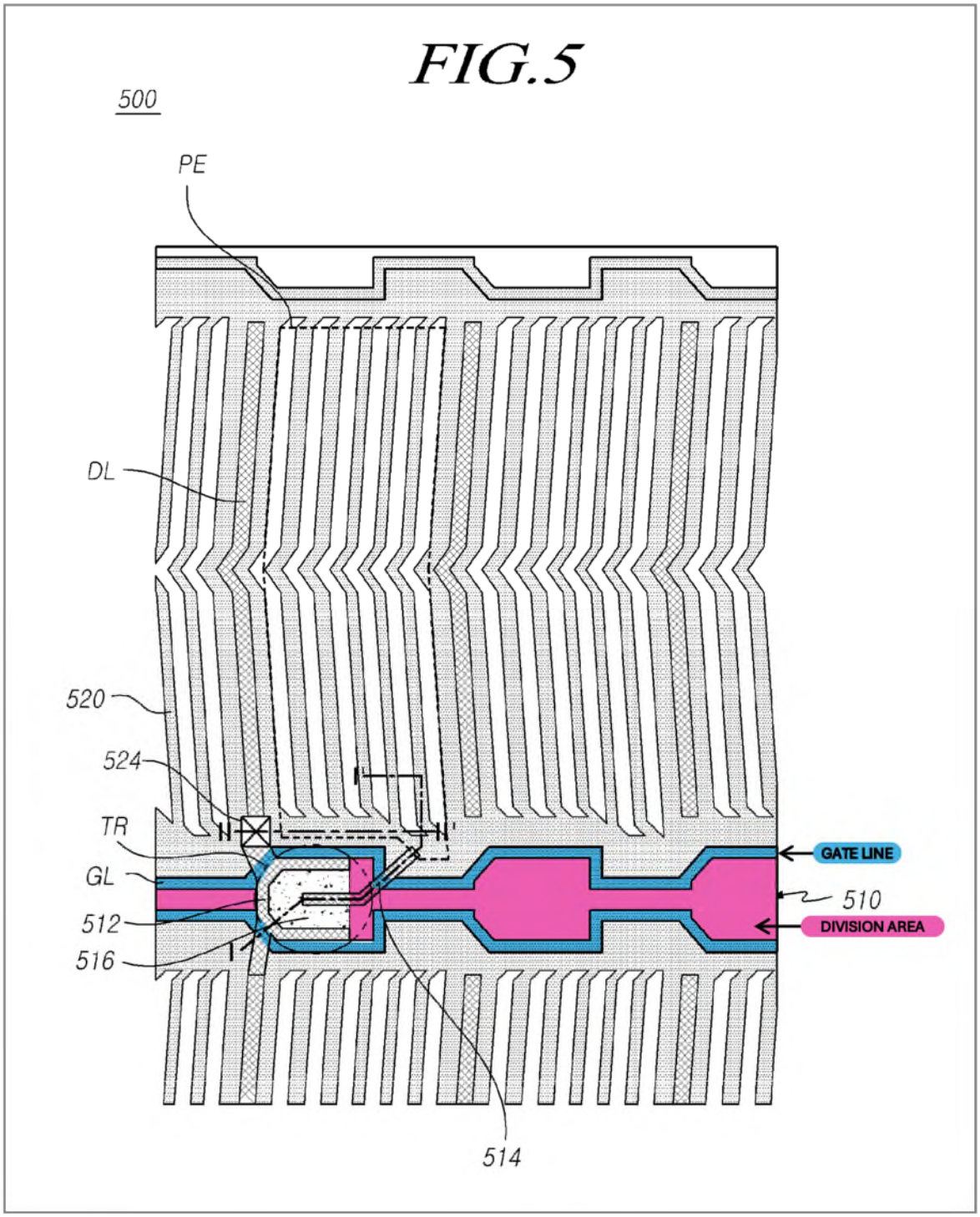


Kim II, Fig. 8; Ex. 1003 ¶¶135-136.

Kim II likewise teaches that its touch electrodes are divided into "common voltage electrode rows," *i.e.*, segment electrodes. Kim II at [0052]. And Kim II teaches that the sensing lines connect to all the rows within a common electrode through contact holes. Kim II at [0058].



Kim II, Fig. 3; Ex. 1003 ¶137. As the claims require, Kim II teaches that there is a (pink) space between the (purple) rows, which Kim II describes as a "separation distance D1." Kim II at [0060]. Kim II also refers to this area as "separation space 430b," which "separate[es] common voltage electrode rows within a touch electrode 320." Kim II at [0065]; *see also* Figs. 4-6. Kim II further describes this (pink) "separation space 510" in connection with Figure 5, shown below:



Kim II, Fig. 5, [0089]-[0090]; Ex. 1003 ¶138.

Further, Kim II teaches that this (pink) separation space is "on the" (blue) gate line as the claim requires. Kim II at [0090] ("The separation space 510, *i.e.*, separation area, formed between different rows of the common voltage electrodes 520 may correspond to a line area of the gate lines GL. Specifically, in the exemplary embodiment as illustrated in FIG. 5, the gate line GL or a portion of the gate line GL may be formed in the separation space 510 between two common voltage electrodes 520."); Ex. 1003 ¶139.

In other words, this separation space is identical to the claimed "*division area*" between "*segment electrodes*." Given these similarities, a POSITA would have recognized that Kim and Kim II describe highly analogous teachings to nearly identical touch display panels, such that a POSITA would have had significant confidence that they were compatible and could be combined with a reasonable expectation of success. *Id.* ¶¶139-140.

A POSITA would have been motivated to adopt Kim II's teachings regarding the placement of the division area on the gate line based on its teachings that such placement prevents potential display defects. *Id.* ¶¶141-145. Kim II teaches, in conventional touch panels, large common electrodes overlaying a plurality of pixels would cause overlapped transistors to experience different capacitances relative to their proximity to the edge of the large common electrode. Kim II at [0013]-[0016]. This would distort the gate-source voltage of the gate

electrodes, which could delay the activation of the transistor or prevent the data voltage from being supplied to the pixel entirely. Kim II at [0016], [0047]-[0048]. Because "the gate line GL and an electrode adjacent thereto greatly affect a capacitance of the gate electrode 518," (Kim II at [0090]), Kim II teaches positioning the division area between common voltage electrode rows, *i.e.*, segment electrodes, on the gate line, explaining that "[t]he separation space 510, i.e., separation area, formed between different rows of the common voltage electrodes 520 may correspond to a line area of the gate lines GL." Kim II at [0089]-[0090]; Kim II explains that this placement allows "a capacitance of the gate electrode 518 [to] become[] substantially uniform regardless of being inside the touch electrode and at an outer periphery of the touch electrode" and that "[b]y positioning the separation space 510 on the gate line GL, a capacitance of the gate electrode 518 may be decreased and the transistor TR may be driven at an increased speed." Kim II at [0089]-[0090]; Ex. 1003 ¶¶141-142. A POSITA would therefore have been highly motivated to adopt Kim II's gate line placement in Kim's existing separation areas to avoid these gate electrode capacitance problems and achieve Kim II's speed benefits. *See* Kim II at [0036]-[0048], [0089], [0090]; Ex. 1003 ¶¶141-145.

Further, a POSITA reading Kim would have been additionally motivated to adopt Kim II's teachings regarding the position of the gate line based on Kim's

express teachings about the desirability of similarly reducing overlap capacitance in Kim's touch lines. Specifically, in connection with Kim's first embodiment, Kim teaches that, by positioning the touch lines over slits in the touch electrode, "an overlap capacitance between a corresponding touch signal line and a corresponding touch electrode is reduced" and "image quality is prevented from being degraded due to the overlap capacitance." Kim at [0116]. Accordingly, Kim already recognizes the wisdom of positioning lines in gaps to avoid overlap capacitance, so a POSITA reading Kim II's teachings concerning reducing capacitance in connection with the position as of the gate line would recognize Kim II to teach a complimentary and sensible solution in line with Kim's design goals. Ex. 1003 ¶143.

A POSITA would have recognized that the teachings of Kim and Kim II could be readily combined with a more than reasonable expectation of success. Both Kim and Kim II related to in-cell touch panels, and come from the same applicant company. Both relate to in-cell touch panels with conventional structures, including an array of pixels, gate lines, data lines, common electrodes overlapping those pixels, and only immaterial differences. *See* Kim at [0007], [0073], [0075]; *see also* Kim II at [0003], [0037], [0068]; Ex. 1003 ¶139. And both describe segmenting those common electrodes into segment electrodes. *See* Kim at [0118], [0142]; *see also* Kim II at [0052], [0058]; *see also* Kim II, Fig. 3.

Given these similarities, a POSITA would have predictably and successfully combined them without undue experimentation. Ex. 1003 ¶¶139-140.

A POSITA would recognize that Kim II's solution would be particularly desirable to combine with Kim. Kim II teaches that these capacitances issues are especially problematic for in-cell panels that use the "in-plane" structure (*i.e.*, where the pixel electrodes and common electrodes are both disposed on the same side of the liquid crystals), noting that, for such a structure, these capacitance issues "may become a big problem." Kim II at [0092]. Kim teaches a panel with such an "in-plane" structure. *See* Kim, Fig. 9 (showing common electrodes and pixel electrodes as part of the array substrate below the liquid crystal layer). Accordingly, a POSITA following Kim's teachings would recognize that Kim II's solution was specifically desirable for, and compatible with, Kim's teachings. Ex. 1003 ¶145.

h) [1-H]

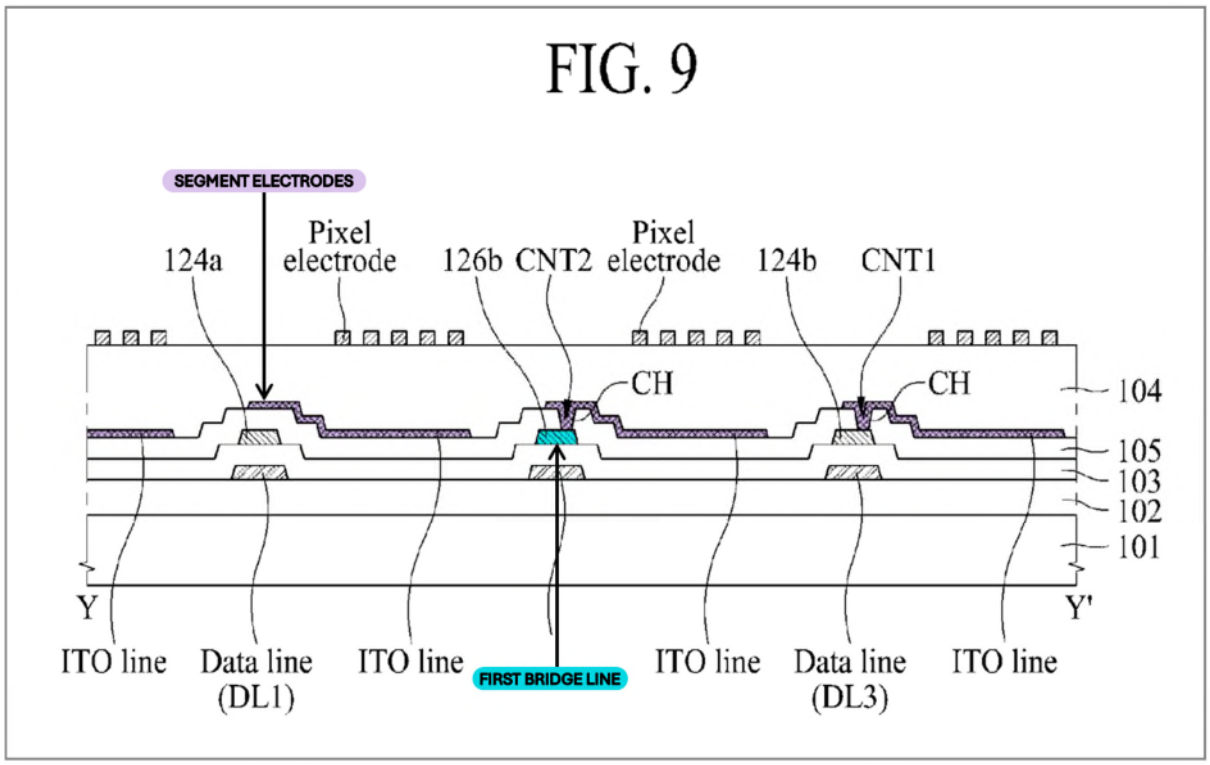
Kim teaches, or at least renders obvious, that the "*segment electrodes included in one of the common electrodes are connected by at least one of the touch lines*." Kim teaches that the "touch signal lines" can connect to each ITO line, *i.e.*, "*segment electrode*," within a particular touch electrode, i.e., "*common electrode*," but are insulated from the other touch electrodes. *See* Kim at [0121] (explaining that "the first touch signal line 124a may be connected to the first

touch electrode 116a, but may be insulated from the other touch electrodes 116."), [0122] (similar). *See also* Kim, Fig. 7 (showing touch line 124a and 124b connecting to only one of the two depicted touch electrodes 116a and 116b of the plurality of touch electrodes 110); Fig. 8 (same); Ex. 1003 ¶¶146-147.

i) [1-I]

Kim teaches, or at least renders obvious, that "*the first bridge line and each of the two of the segment electrodes are connected via a contact hole*." Kim's second embodiment uses connecting lines, *i.e.*, "*bridge line[s]*," that connect to two of the ITO lines, *i.e.*, "*segment electrodes*." *See, e.g.*, Kim at [0126] (explaining "the first touch electrode 116a may be connected to the first connecting lines 126a through a plurality of second contacts CNT2" and "each contact CNT2 connects a single ITO line to a single first touch signal line 124a."); [0128] (disclosing the same regarding a second connecting line connecting to the ITO lines of a second touch electrode); Figs. 7 and 8; Ex. 1003 ¶¶148-149.

Kim further explains that these connections "contact CNT2" are formed via "contact holes CH in the insulation layer 105," as the claim requires. Kim at [0147]. Figure 9 shows this contact hole CH (indicated with a CH) through which the (purple) ITO line is connected to the (cyan) connecting line 126b:



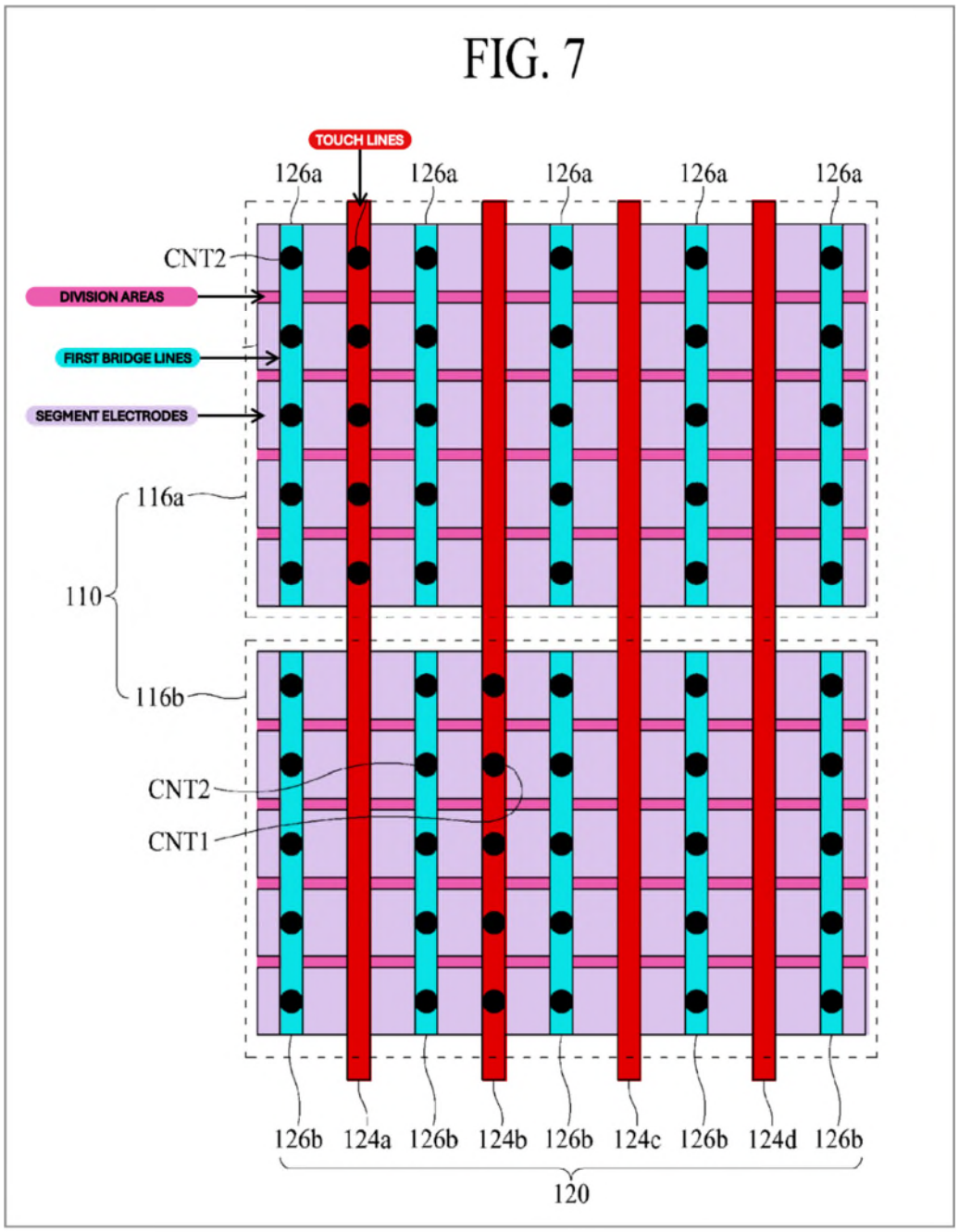
Kim, Fig. 9; Ex. 1003 ¶150.

j) [1-J]

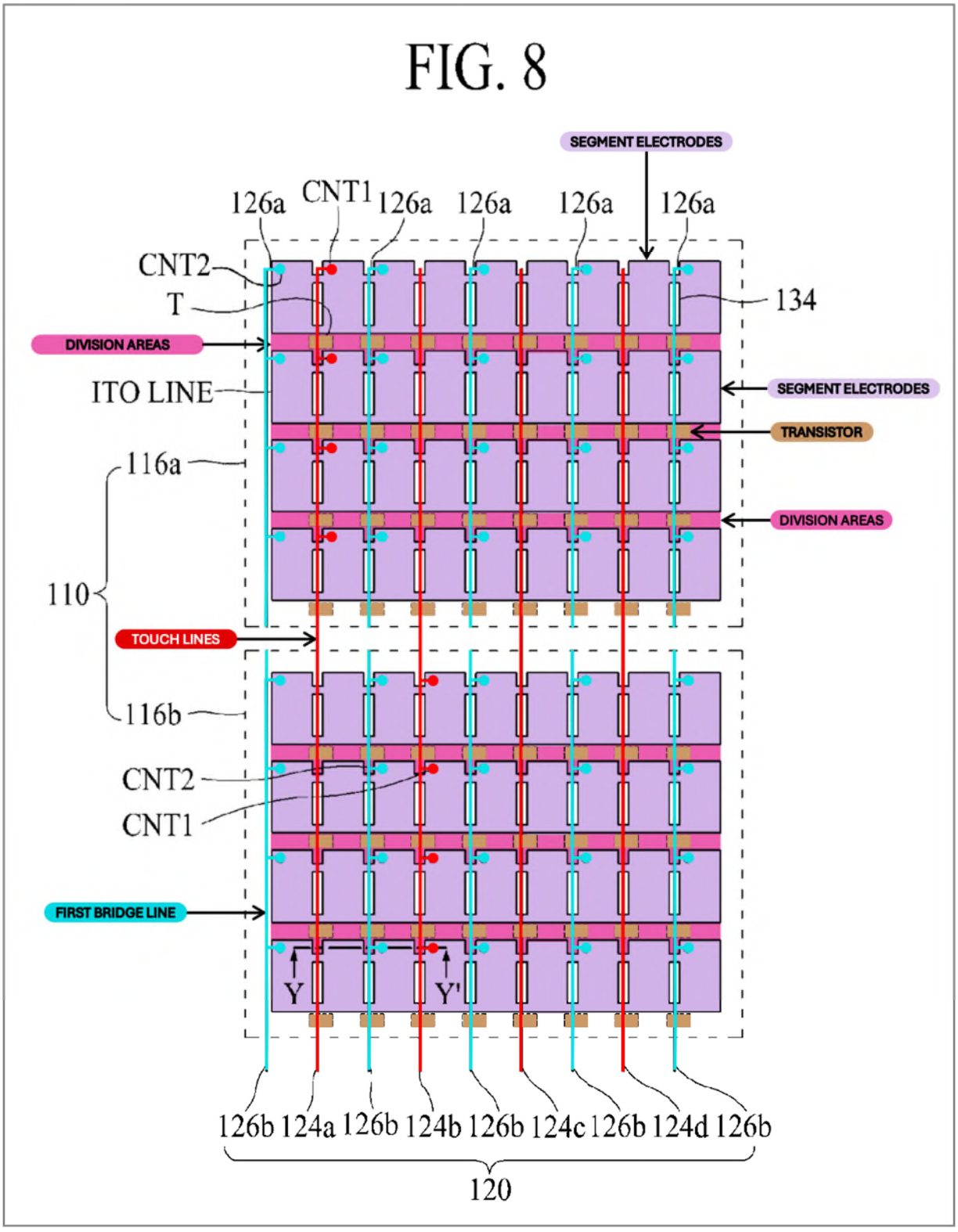
Kim teaches and obvious "*the first bridge line extends in the second direction so as to overlap with the segment electrodes included in the one of the common electrodes, and be connected to the segment electrodes included in the one of the common electrodes.*" The "connecting line 126 is a line of conductive material that connects different ITO lines" *i.e.*, segment electrodes, "of a touch electrode 110," *i.e.*, a common electrode, "to each other." Kim at [0120]. These connecting lines overlap one of the touch electrodes (and thus the ITO lines, *i.e.*, segment electrodes, that make up that touch electrode). *See* Kim at [0130] ("On

the other hand, the plurality of first connecting lines 126a may overlap the first touch electrode 116a, but may not overlap other touch electrodes."). As explained above, these connecting lines are also connected to the ITO lines within a particular touch electrode via a contact hole. Section VII.A.1.i *supra*; s*ee* also Kim at [0120] ("By connecting together different ITO lines, the connecting lines 126 reduces an internal load deviation of each of the touch electrodes 110, and a load deviation between the plurality of touch electrodes 110 is reduced."); Ex. 1003 ¶¶151-152.

Kim further teaches that "connecting lines 126 extend in a vertical direction," *i.e.*, the "*second direction*." Kim at [0118]. Kim's figures show these (cyan) connecting lines extending vertically so as to overlap and connect the (purple) ITO lines of a touch electrode:


FIG. 7
TOUCH LINES
126a
126a
126a
126a
126a
CNT2
DIVISION AREAS
FIRST BRIDGE LINES
SEGMENT ELECTRODES
116a
110
116b
CNT2
CNT1
126b
124a
126b
124b
126b
124c
126b
124d
126b
120

Kim, Fig. 7.



Kim, Fig. 8; Ex. 1003 ¶¶153-154.

2. Claim 2

Claim 2 depends from Claim 1 and further recites "*wherein the first bridge line is formed in a different layer from the common electrode*." Kim expressly teaches this limitation. Specifically, Kim states "[t]he ITO lines are located on a different metal layer than the connecting lines 126 and touch signaling lines 124." Kim at [0147]; *see also* Fig. 9; Ex. 1003 ¶¶155-157.

3. Claim 3

Claim 3 depends from Claim 1 and further recites "*wherein the first bridge line is formed in a same layer as the touch line*." Kim expressly teaches this limitation, explaining that "[t]ouch signaling lines 124 and connecting lines 126 are located in an intermediate metal layer formed on the passivation layer 103." Kim at [0146]; Ex. 1003 ¶¶158-160.

4. Claim 6

Claim 6 depends from Claim 1 and further recites "*wherein the first bridge line overlaps with the data line in a planar view*." Kim teaches this limitation. Kim explains "[t]he connecting line 126b is located over and overlaps with another data line DL2." Kim at [0146]. *See also* Kim Fig. 9 (shows that connecting line 126b is directly above data line DL2 when viewed from the planar view angle of Figure 9); Ex. 1003 ¶¶161-163.

5. Claim 9

Claim 9 depends from Claim 1 and further recites "*wherein a plurality of the first bridge lines are provided in the one of the common electrodes*." Kim teaches that "each of the plurality of touch electrodes 110 may be connected to a plurality of connecting lines." Kim at [0120]; *see also* [0126]. Further, in Figures 7 and 8, Kim teaches that there is a plurality of connecting lines 126 connecting the ITO lines of a single touch electrode. *See* Kim, Figs. 7 and 8; Ex. 1003 ¶¶164-166.

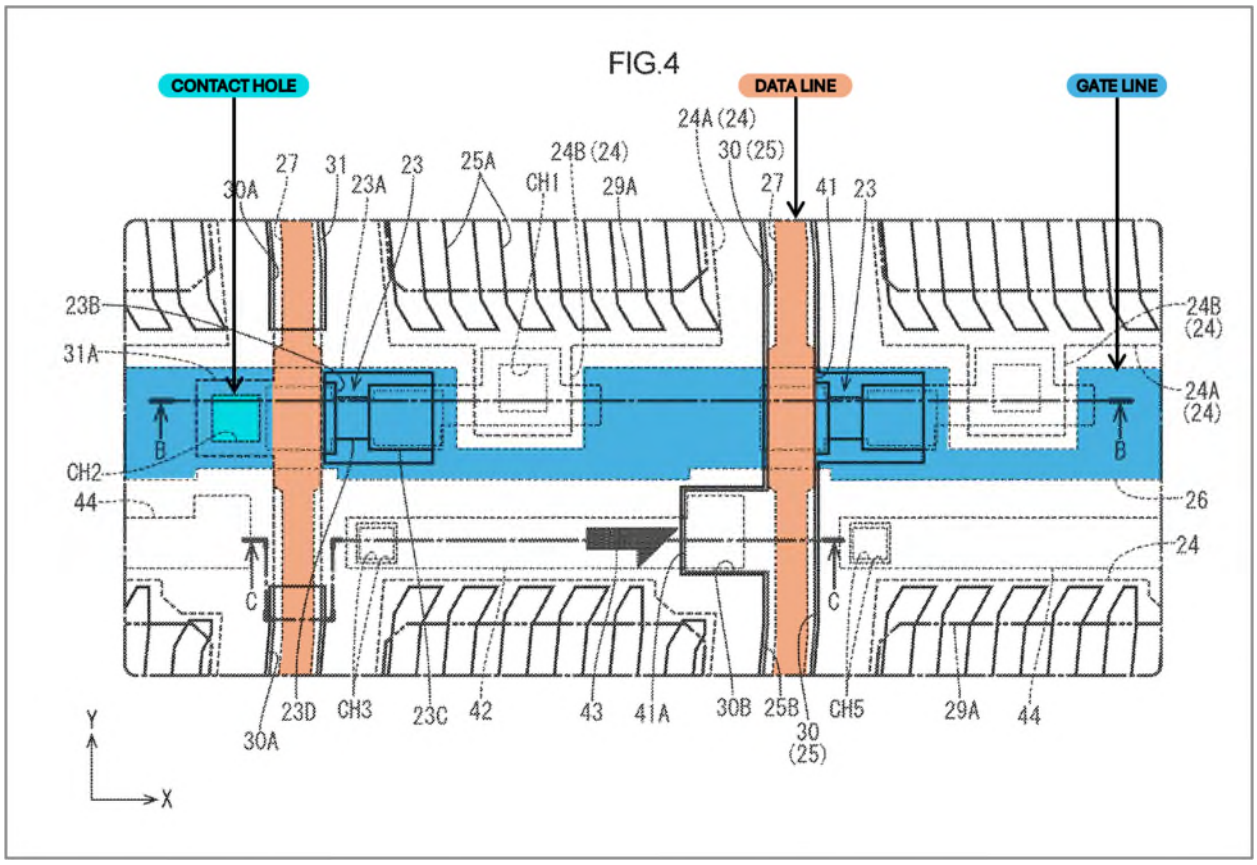
B. GROUND 2: Claims 4, 5, and 8 are Obvious under 35 U.S.C. § 103 Over Kim in Combination With Kim II and Yoshida.

Ground 2 is provided to address specific dependent claims. A POSITA would have been motivated to combine Kim and Kim II with Yoshida, a reference that teaches a similar in-cell touch panel, because it provides for spare touch lines that can be beneficially used for repair. Ex. 1003 ¶167. A detailed discussion of the POSITA's motivation to combine these references is provided below.

1. Claims 4 and 5

Claim 4 depends from claim 1 and adds the limitation "*wherein the contact hole overlaps with the gate line in a planar view*." Claim 5 depends from claim 1 and adds "*wherein the contact hole does not overlap with the data line in a planar view*."

Kim does not indicate whether the contact holes of connecting lines 126 overlap the gate line. Yoshida, however, teaches a (cyan) contact hole CH2 used to connect the touch line to the touch electrode 30, which is both on the gate line and offset from the data line, as required by these claims:



Yoshida at [0034], Fig. 4; Translation at [0022], Fig. 4; Ex. 1003 ¶¶168-171.

It would have been obvious to provide similarly positioned contact holes for Kim's connecting lines, which are positioned similarly to, and connected to the same electrodes, as the touch lines. Kim at [0118]; Ex. 1003 ¶172. Consistent with the '025 patent's description of this placement, which provides no particular

reason or advantage of it, a POSITA would recognize that using offset contact holes would have been a routine design choice providing an advantageous layout in some circumstances, and would have known how to easily adopt such a design with no particular obstacles to its success. '025 patent, 11:52-55; Ex. 1003 ¶172. Further, a POSITA would have been motivated to use this placement to minimize the potential risk of shorting at the contact hole between the first bridge line and the underlying data line. Ex. 1003 ¶173; *see also* Section VII.B.2.c (describing further motivation to combine)

2. Claim 8

Claim 8 is obvious in light of Kim combined with Kim II and Yoshida. Ex. 1003 ¶174.

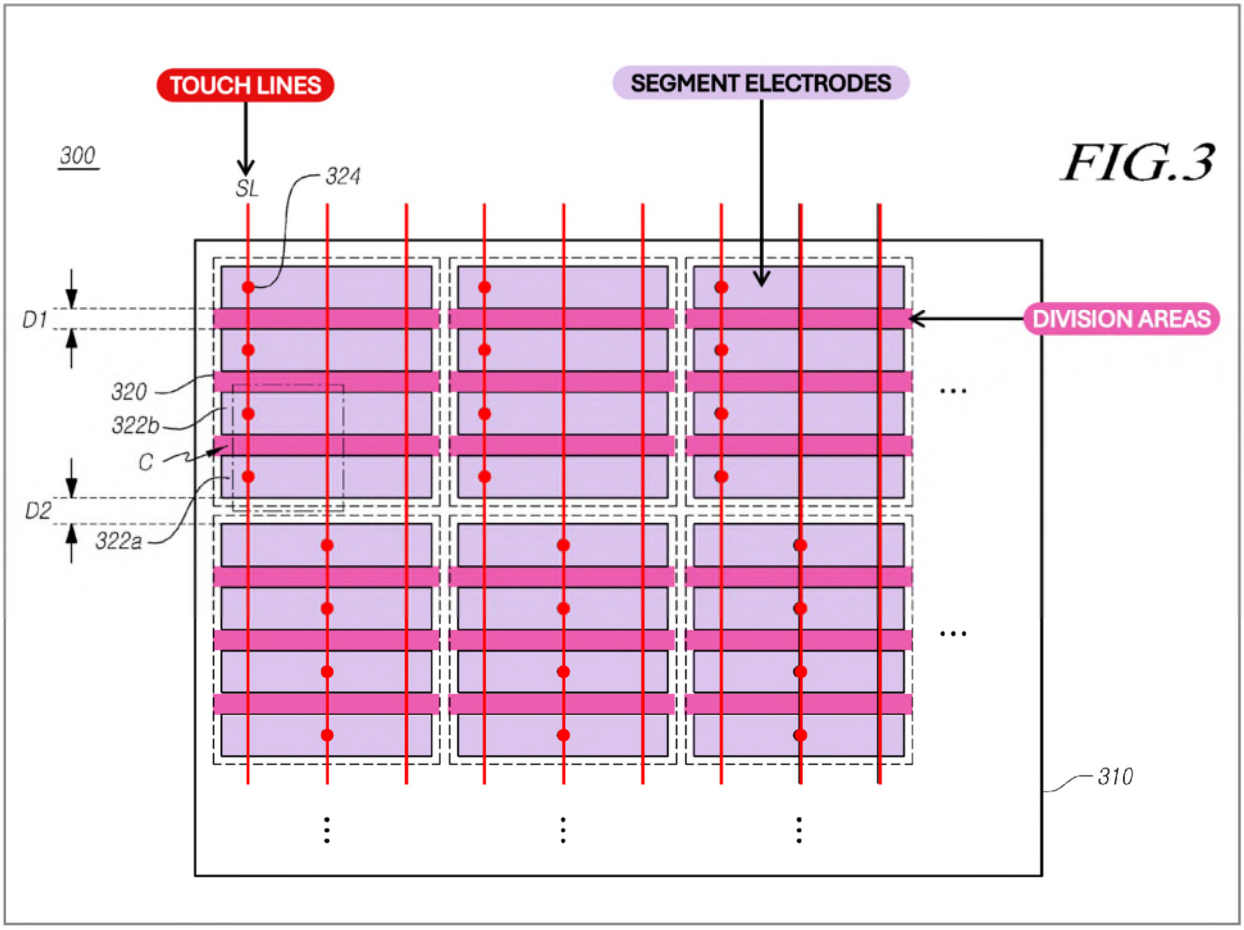
a) [8-PRE]

As explained above, Kim alone and in combination with Kim II renders obvious the limitation of claim 1. *See* supra Section VII.A.1; Ex. 1003 ¶175.

b) [8-A]

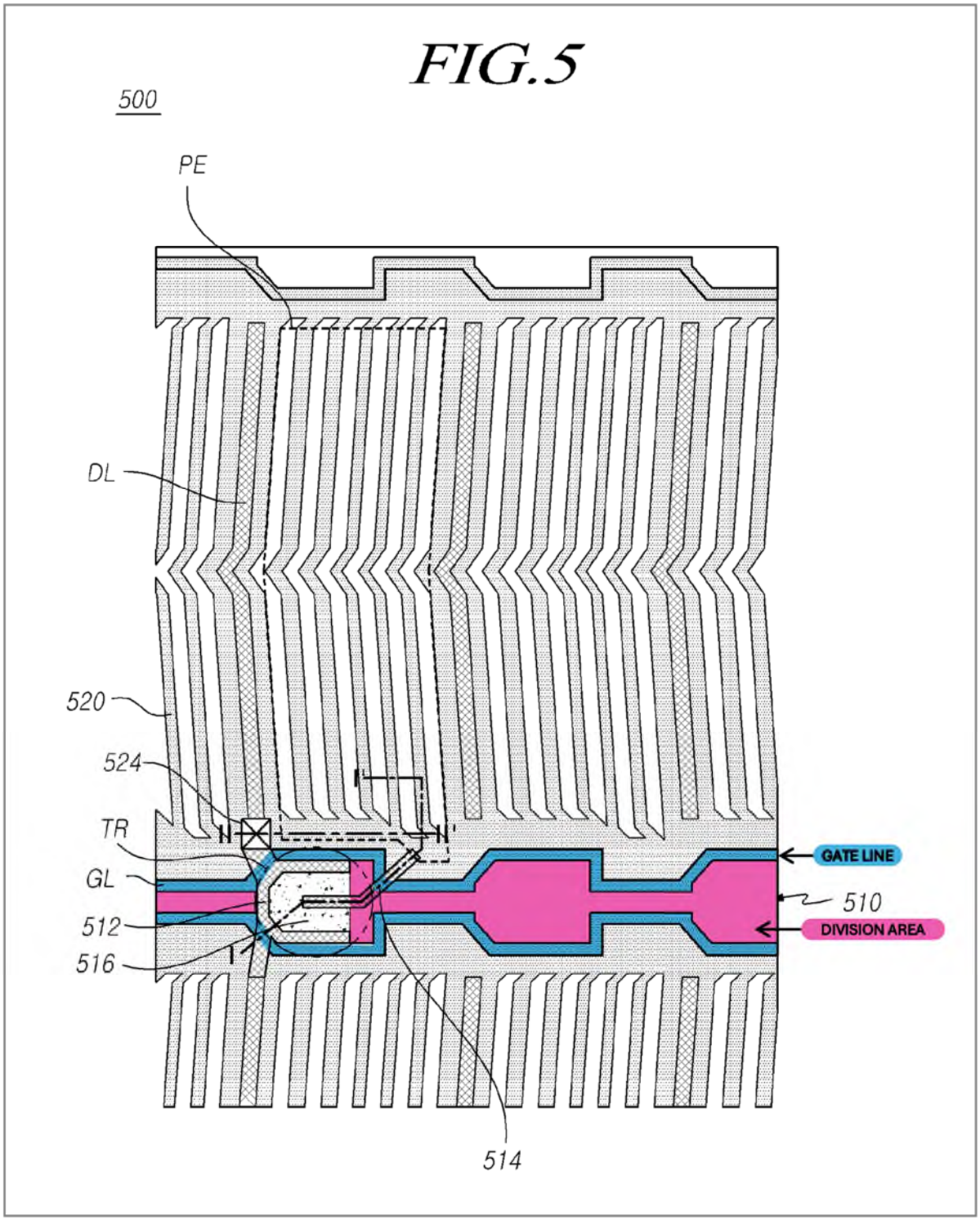
Kim II renders obvious the limitation "*wherein two of the common electrodes adjacent in the second direction are separated from each other with the separation area on the gate line.*" For Figure 3, there is a separation distance "D2" between touch electrodes— and in Figure 4, this space is referred to as "separation space 430a," (as distinct from 430b, which is within a touch electrode). Kim II at

[0060], [0065].



Kim II, Fig. 3; *see also* Fig. 4.

Regarding Figure 5, which is a plan view of a display panel, Kim II refers to these both the gaps between electrodes and the gaps within electrodes as "separation space 510. Kim II at [0089] (explaining that 510 refers to separation spaces "regardless of being inside the touch electrode and at an outer periphery of the touch electrode").



Kim II at Fig. 5. Kim II teaches that the gate line is positioned in this separation space 510 between common electrodes. *See* Section VII.A.1.d; Ex. 1003 ¶¶176-

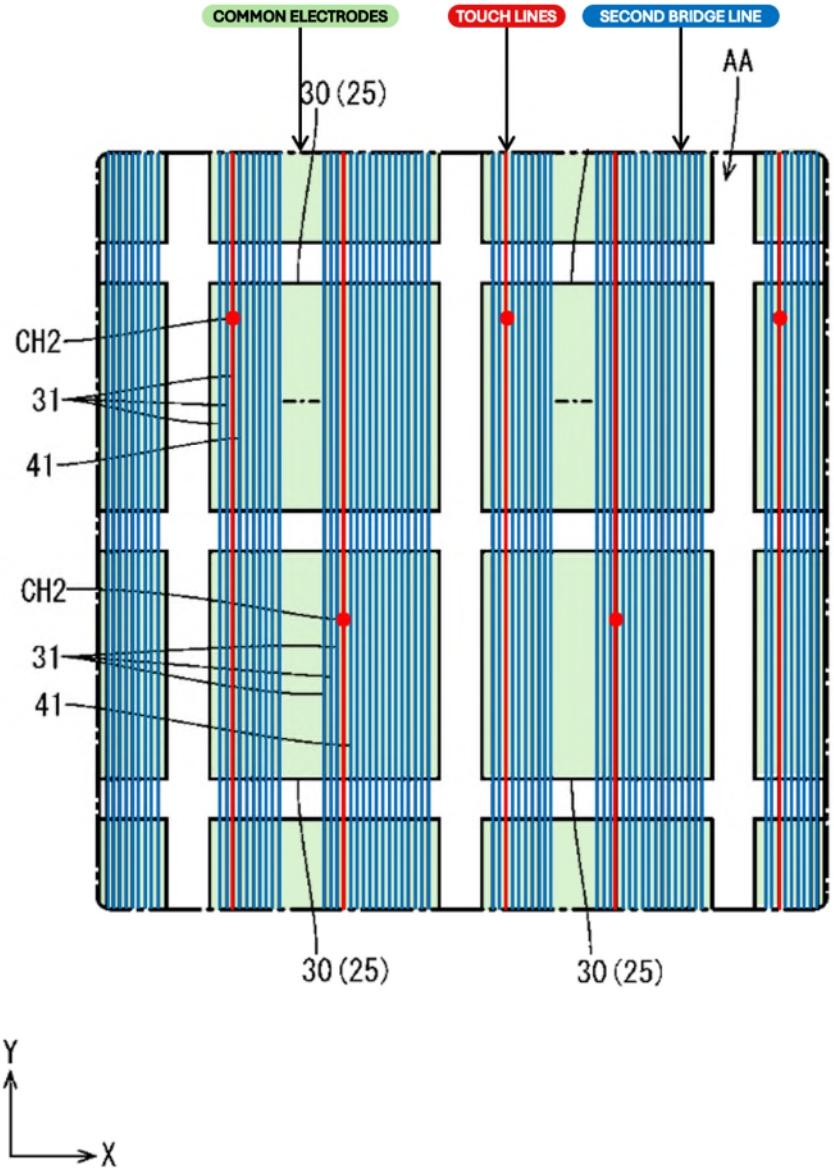
179.

c) [8-B]

Yoshida renders obvious "*the in-cell touch panel includes a second bridge line laterally bridging the two of the common electrodes adjacent in the second direction across the separation area.*" As the '025 patent explains, this "second bridge line" is a dummy line. '025 patent, 12:16-17.

While Kim and Kim II do not teach dummy "*second bridge line[s]*," Yoshida teaches dummy "spare touch line[s] 41" that overlap the touch electrodes (as distinct from the spare touch lines that a between touch electrodes, as discussed in the Grounds 3 and 4 below). These spare touch lines extend in "*the second direction*", "generally … in the Y-axis direction in parallel with the source lines 27" and can also "overlap[] the touch electrodes 30", bridging the "separation area" between such electrodes. *See* Yoshida at [0035]; Translation at [0023]. Figure 6 shows these (blue) spare touch lines 41 "bridging" the "separation area" between "*two of the common electrodes adjacent in the second direction across the separation area.*":

FIG.6


COMMON ELECTRODES
TOUCH LINES
SECOND BRIDGE LINE
AA
30 (25)
CH2
31
41
CH2
31
41
30 (25)
30 (25)
Y
X

Yoshida, Fig. 6; Translation, Fig. 6.

Yoshida teaches that these spare touch lines allow for repair if one of the touch lines is damaged or rendered inoperable. Yoshida at [0035]; Translation at [0023]. Yoshida explains that touch lines 31 are positioned over the data lines, but because each touch electrode can overlap more data lines than there are touch electrodes in a column, the number of necessary touch lines (to connect to the touch electrodes in a column) will be less than the number of overlapped data lines. *Id*. Yoshida nonetheless teaches that these data lines should still be covered with a spare touch line 41 that does not connect to any touch electrode. *Id*. Accordingly, a POSITA would also recognize that these spare touch lines are provided to maintain uniformity in the design. Ex. 1003 ¶¶180-182. A POSITA would therefore have been motivated to employ Yoshida's spare lines in a touch panel based on the combination of Kim and Kim II to provide for uniformity and to allow for the repair Kim's touch lines (or even Kim's connecting lines). *Id.* ¶183.

Further, a POSITA would have recognized that Yoshida, Kim, and Kim II all relate to similar in-cell touch panels involving vertical touch lines connecting to common electrodes, and therefore could be compatibly combined to achieve Yoshida's advantages. Yoshida at [0028]; Translation at [0016]; *see* Kim at [0118], [0145]; *see also* Kim II at [0022]. Accordingly, a POSITA would have had a significant expectation of success in combining Yoshida with Kim and Kim II.

Ex. 1003 ¶184.

d) [8-C]

Yoshida renders obvious the limitation "*the second bridge line is not electrically connected to any of the two of the common electrodes*." As shown in Figure 6, there are at least two common electrodes not connected to excess spare touch line 41. *See* Yoshida at [0035] (explaining that connections are "indicated by dots"); Translation at [0023]. Further the spare touch line 41 is provided in a different layer than the common electrodes 30/25, with an insulating film 39 between. Yoshida, Fig. 5; Translation at Fig. 5; Ex. 1003 ¶¶185-188.

C. GROUND 3: Claims 18 is Obvious Under 35 U.S.C. § 103 Over Yoshida Alone.

Claims 18 is rendered obvious by Yoshida alone. Unlike Claim 1, Claim 18 does not require segment electrodes or bridge lines, and instead merely claims the concept of "dummy touch lines" positioned between horizontally adjacent common electrodes. Yoshida teaches these "dummy touch lines" as "spare touch lines 41." Ex. 1003 ¶189.

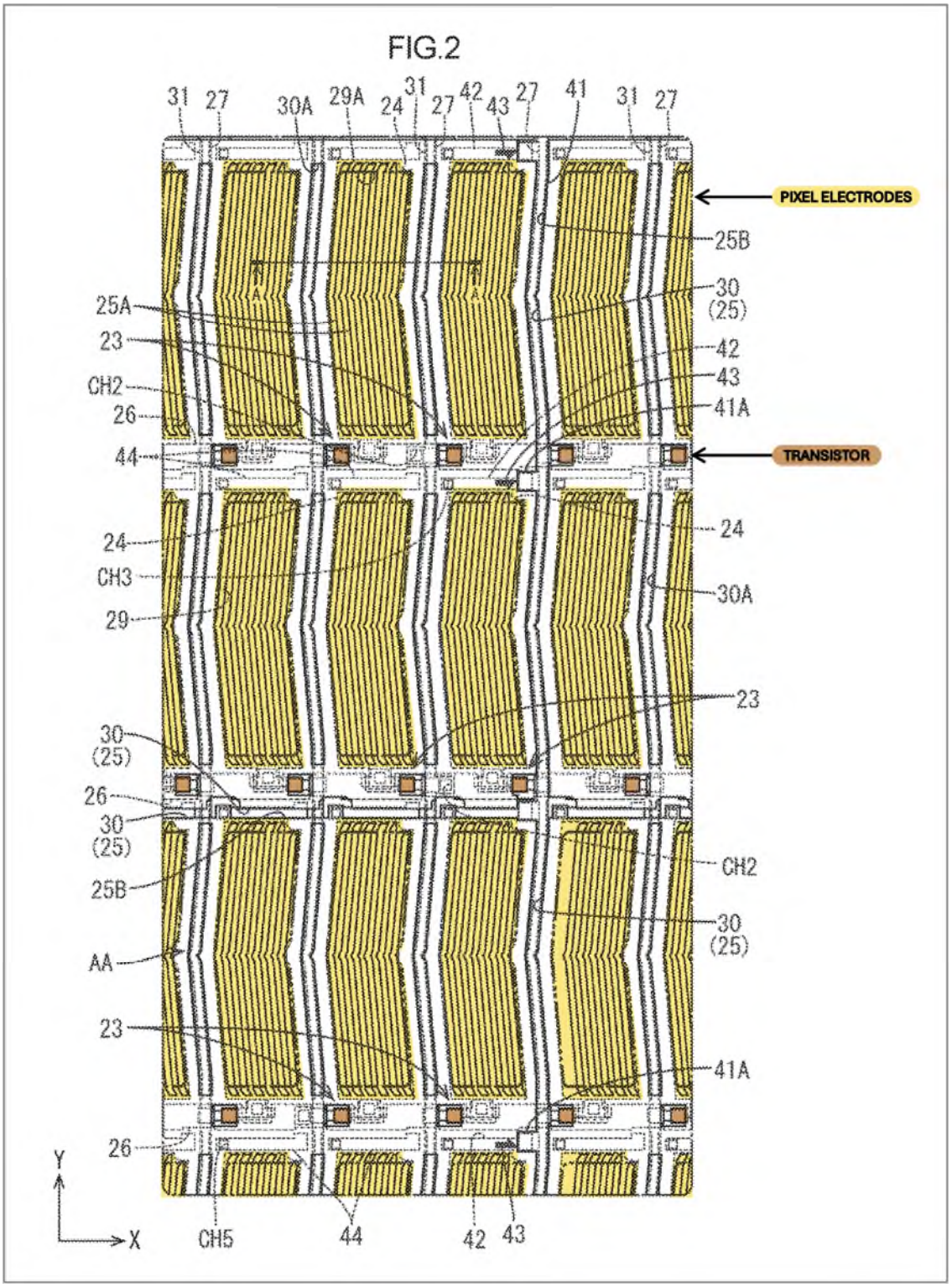
1. Independent Claim 18

Claim 18 is rendered obvious by the teachings of Yoshida alone. Ex. 1003 ¶190.

a) [18-PRE]

Yoshida discloses and renders obvious any requirements of the preamble.

Specifically, Yoshida discloses "*an in-cell touch panel having an image display area made up of pixels arranged in a first direction and a second direction orthogonal to the first direction*." *See, e.g.*, Yoshida at [0026] (describing how a display "touch panel pattern for implementing the touch panel function is integrated (in-cell technology)"), [0024] (explaining that the panel is configured to display an image), [0028] (explaining the pixels and other components are "disposed orthogonal to (intersecting) each other"):



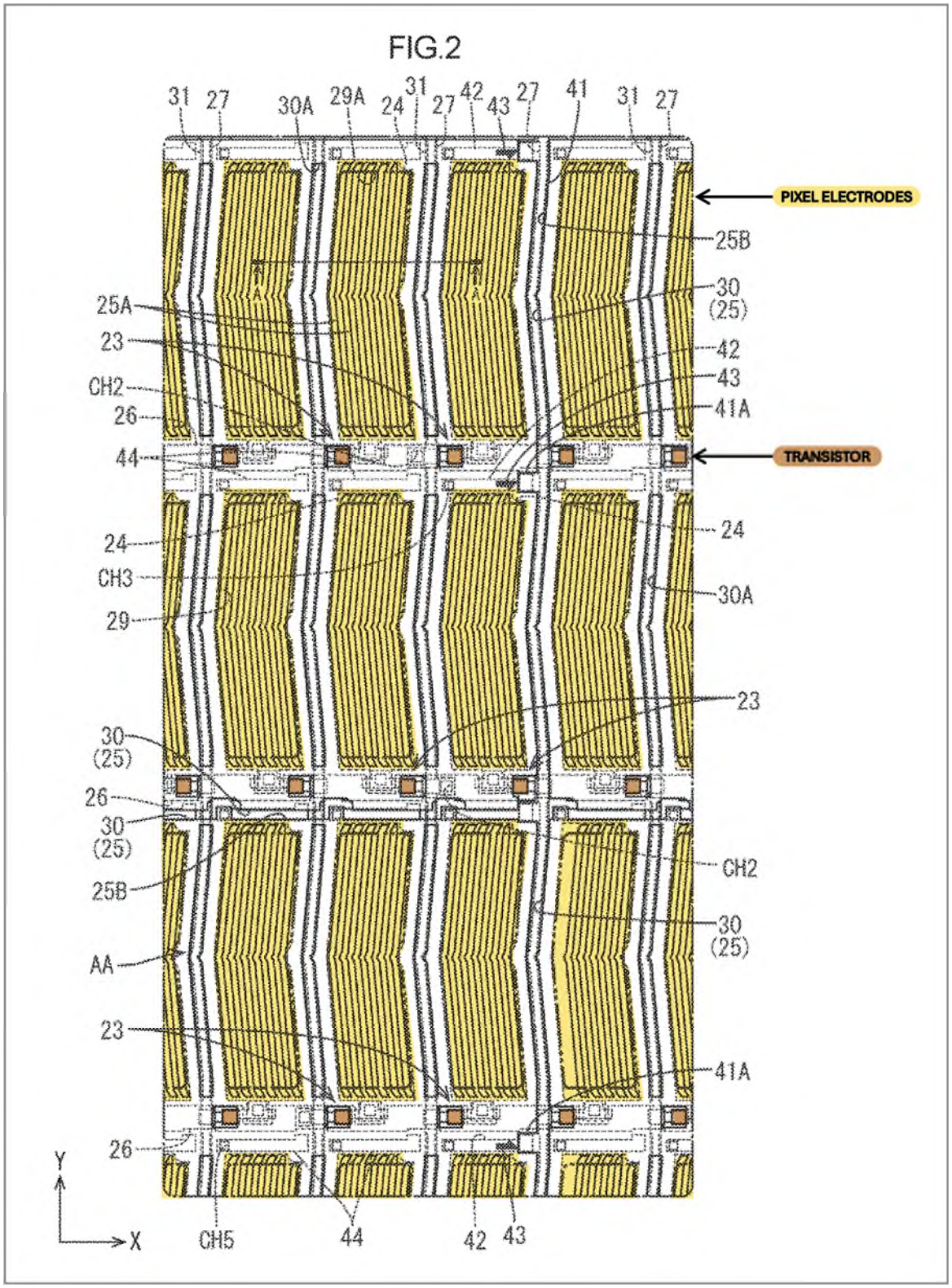
Yoshida, Fig. 2; [0029] (describing pixels portions as having an arrangement in the

X and Y directions); Translation, Fig. 2, [0012], [0016], [0017]; Ex. 1003 ¶¶191-192.

b) [18-A]

Yoshida discloses and renders obvious that the touch panel comprises "*transistors and pixel electrodes respectively provided in the pixels*."

Yoshida explains that each of its pixels includes a transistor and a pixel electrode. For example, Yoshida's "liquid crystal panel 11," includes "thin-film transistors (TFTs; switching elements) 23 and pixel electrodes 24 are provided" in a pixel portion. Yoshida at [0028], [0029]; Translation at [0016], [0017]. Figure 2 shows a (brown) transistor 23 and (yellow) pixel electrode 24 is provided in each pixel:

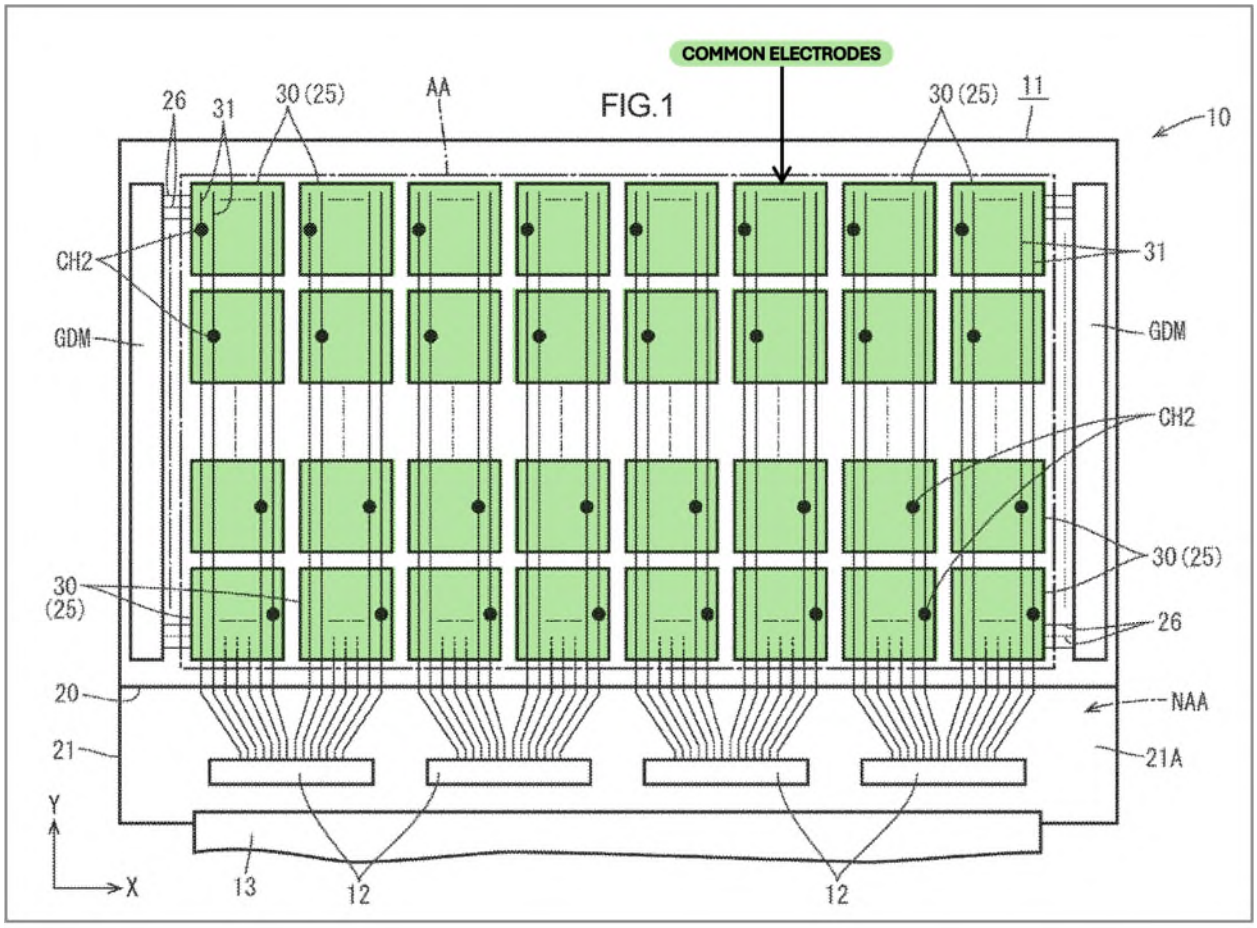


Yoshida, Fig. 2; Translation, Fig. 2; Ex. 1003 ¶¶193-194.

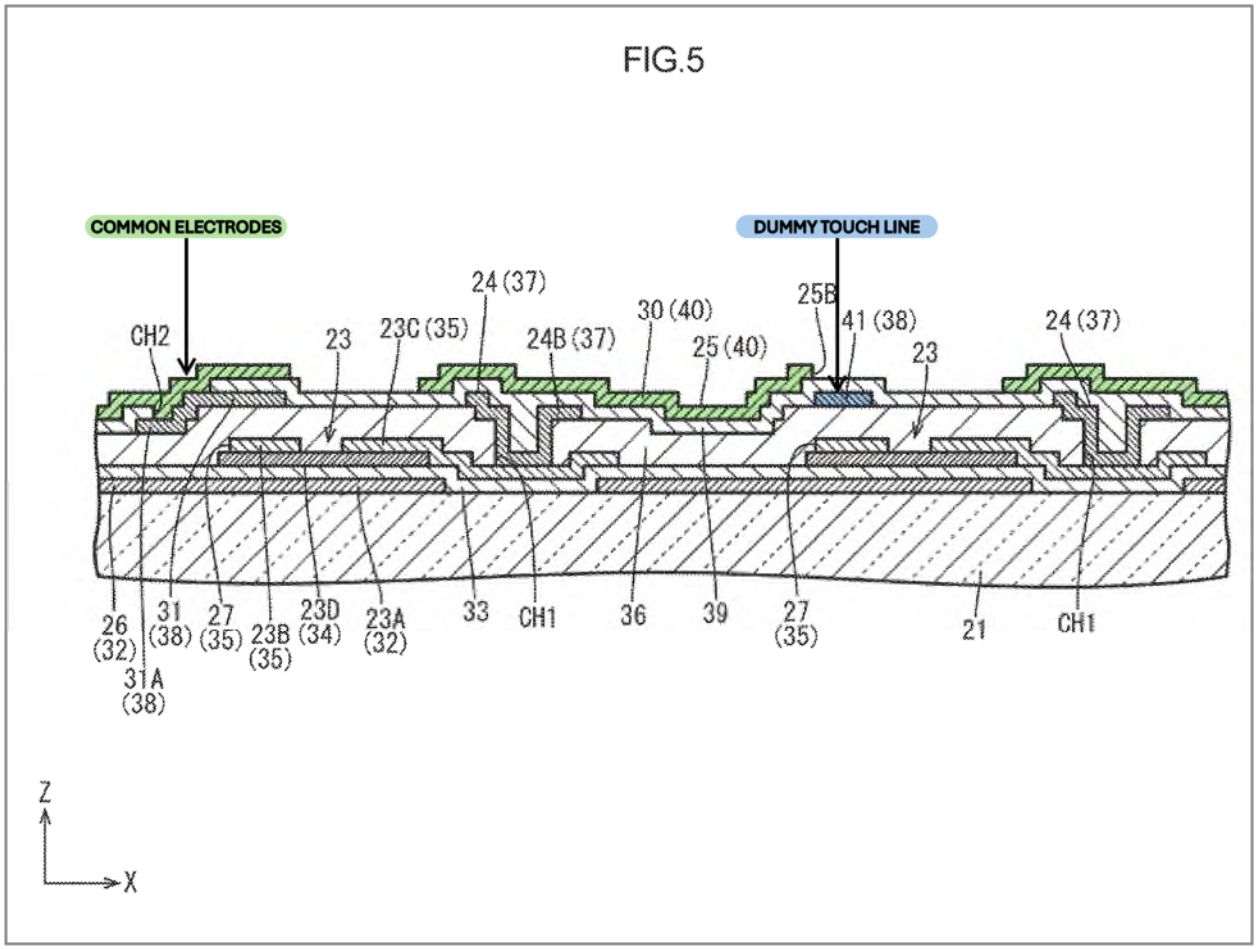
c) [18-B]

Yoshida discloses and renders obvious that the touch panel comprises "*common electrodes arranged in the first direction and the second direction, respectively facing one or more of the pixel electrodes and provided separately from each other*." Ex. 1003 ¶195.

Although Yoshida describes its "common electrode 25" as a single electrode, it is provided in separate pieces divided along gaps called "partition openings 25B" to form a plurality of "touch electrodes 30" (*i.e.*, common electrodes) that are "divided into a grid by the partitioning openings 25B and which are electrically independent from each other." Yoshida at [0030], Figs. 1, 3; Translation at [0018], Figs. 1, 3. As shown in Figure 1, Yoshida's (green) touch electrodes 30 are arranged in the first direction and the second direction (*i.e.*, in rows and columns):



Yoshida, Fig. 1; Translation, Fig. 1; *see also* Yoshida at [0026] (explaining that touch electrodes 30 (*i.e.*, common electrodes) are "disposed side by side in a matrix."); Translation at [0014]; Ex. 1003 ¶196. The partitioning openings 25B between touch electrodes 30 is labeled in Figure 5:



Yoshida at Fig. 5; Translation at Fig. 5.

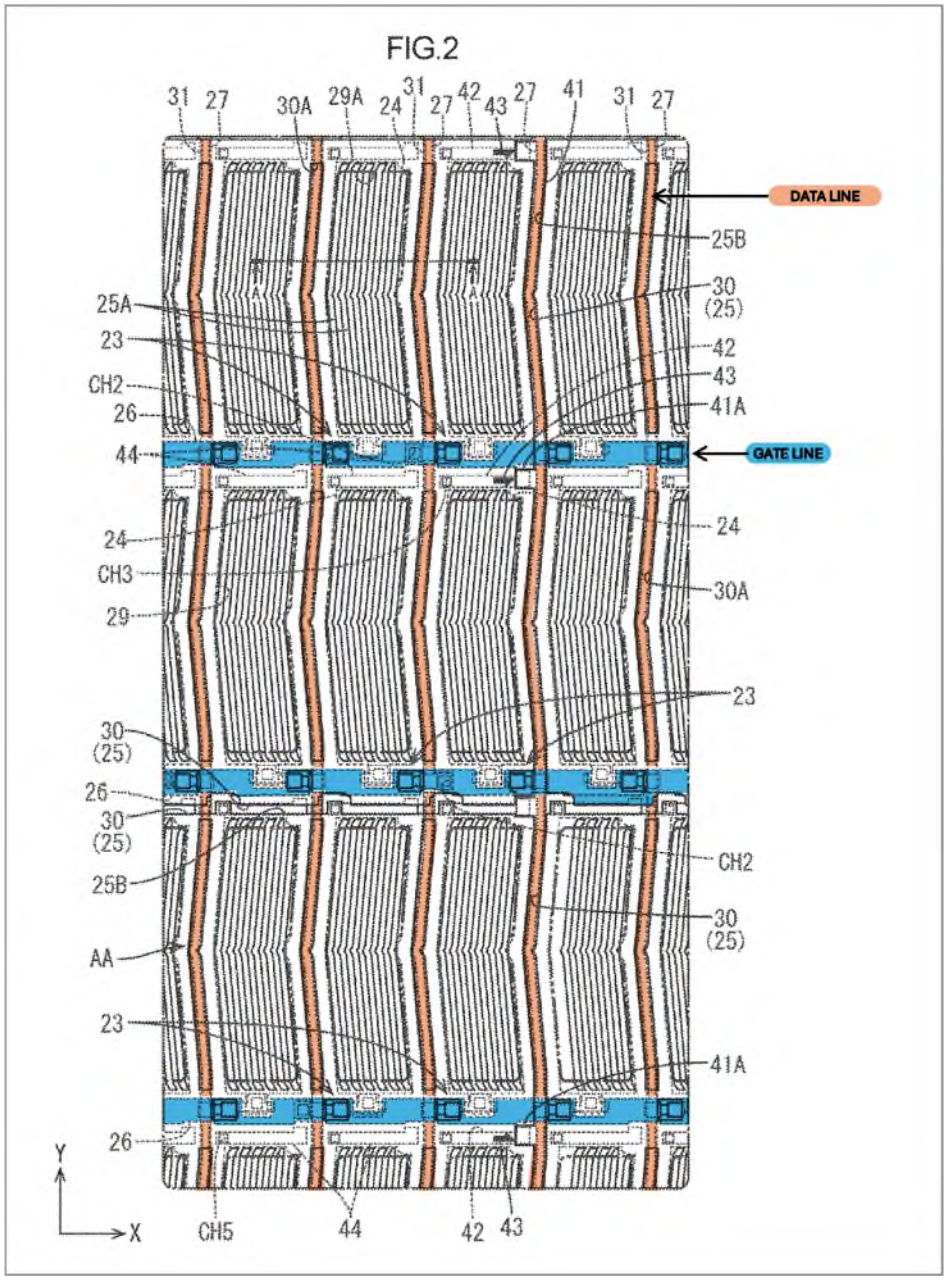
Yoshida teaches that its common/touch electrodes 30 face, *i.e.*, overlap one or more pixel electrodes, as required. Yoshida at [0030] ("The common electrode 25 [made up of touch electrodes 30]…includes portions overlapping the pixel electrodes 24 (specifically, pixel electrode body 24A which will be described later), Figs. 1, 3; and are "arranged in an area spanning over a number (such as several tens) of pixel portions PX"); *see also* Yoshida at [0026], Translation at [0014], [0018]; Ex. 1003 ¶197.

d) [18-C] and [18-D]

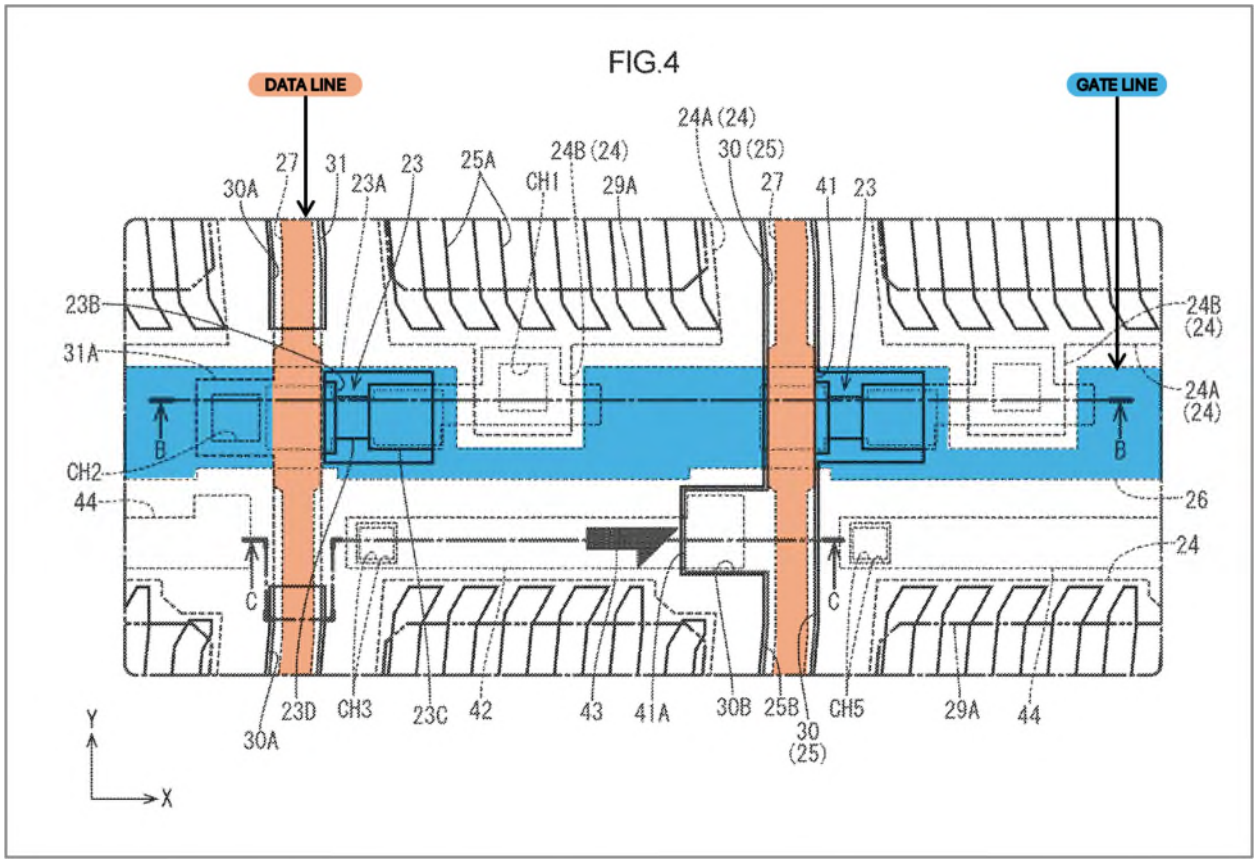
Yoshida discloses and renders obvious that its touch panel comprises "*gate lines that extend along the first direction and supply gate signals to the transistors respectively*" and "*data lines that extend along the second direction and supply data signals to the transistors respectively*." Ex. 1003 ¶198.

Specifically, Yoshida teaches that its panels include "gate lines (scan lines) 26 and source lines (signal lines, data lines) 27" that "are disposed orthogonal to (intersecting) each other" (*i.e.*, that the "*gate lines … extend along the first direction*", the X direction, and that the "*data lines … extend along the second direction,*" the Y direction). Yoshida at [0028] (explaining the arrangement of gate lines 26 and source lines 27); *see also* [0029], [0031]; Translation at [0016], [0017], [0019]; Ex. 1003 ¶199.

This arrangement is shown in Figures 2 and 4:



Yoshida, Fig. 2; Translation, Fig. 2.



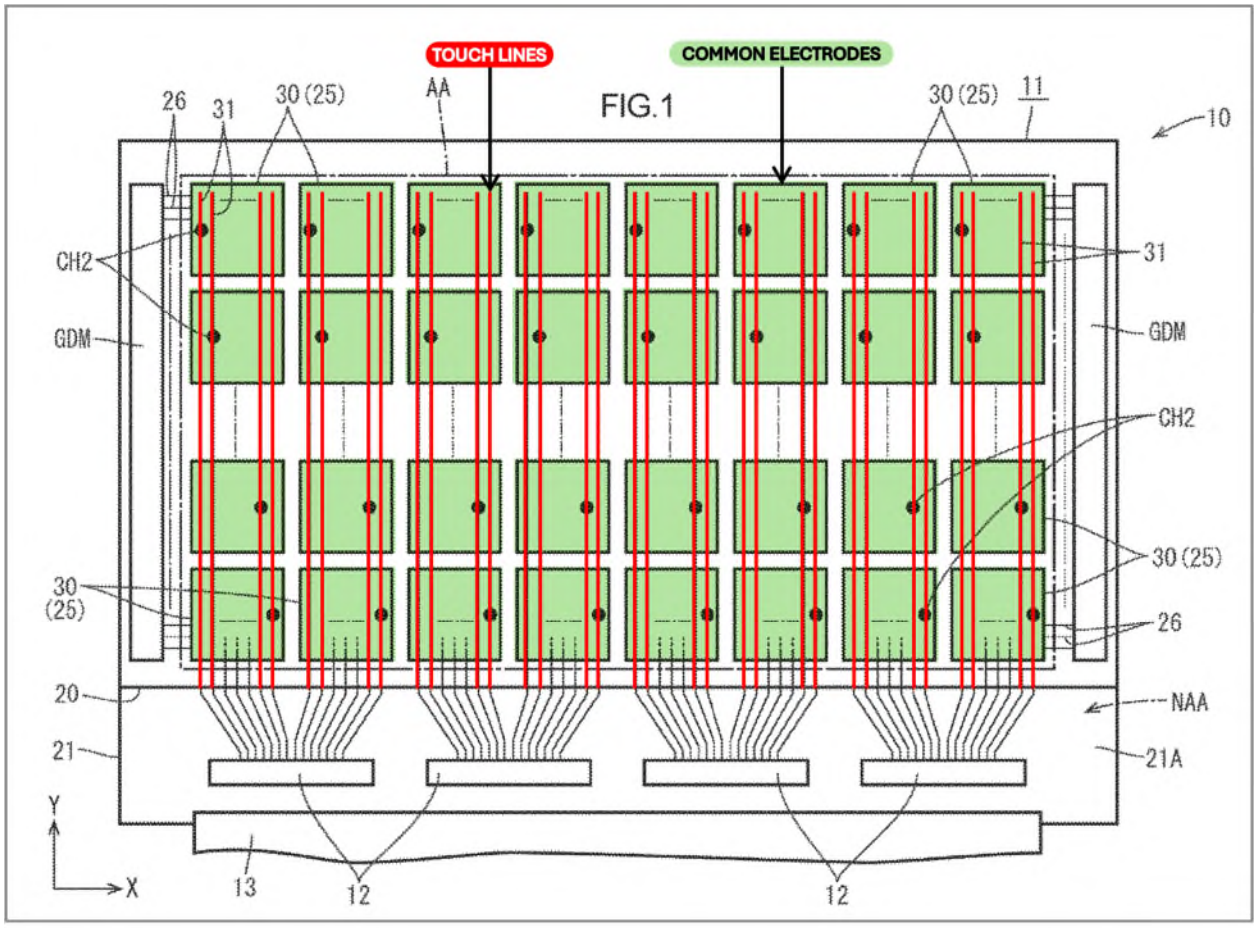
Yoshida, Fig. 4; Translation, Fig. 4.

Yoshida discloses that its gate lines "*supply gate signals to the transistors*" and that its data lines "*supply data signals to the transistors*." *See*, *e.g.*, Yoshida at [0028] ("The gate lines 26 and the source lines 27 are respectively connected to a gate electrode 23A and a source electrode 23B of the TFTs 23" which are "driven based on various signals supplied to the gate lines 26 and the source lines 27, and control the supply of potentials to the pixel electrodes 24"), [0031], [0032] (further describing the signals carried by gate and data lines), Figs. 2, 4; Translation at [0016], [0019], [0020], Figs. 2, 4; Ex. 1003 ¶200.

e) [18-E] and [18-G]

Yoshida discloses and renders obvious that the touch panel comprises "*touch lines that extend along the second direction and are each connected to a corresponding one of the common electrodes*" and that "*each touch line is connected with a corresponding one of the common electrodes arranged in the second direction*." Ex. 1003 ¶201.

Yoshida discloses "touch lines (position detection lines) 31," that "extend in the Y-axis direction, and are selectively connected to specific touch electrodes 30 among the touch electrodes 30 arranged in the Y-axis direction." Yoshida at [0026]; Translation at [0014]. As Figure 1 shows below, the (red) touch lines 31 are arranged in the Y-axis direction, and are each individually selectively connected to each of the (green) touch electrodes 30 forming the column. In Figure 1, dots indicate the portions of the touch electrodes 30 connecting to touch lines 31. Yoshida at [0026], [0027]; Translation at [0014],[0015],



Yoshida, Fig. 1; *see also* Fig. 2 (touch lines 31); Translation, Figs. 1, 2.

Thus, Yoshida's touch lines 31 both "*extend along the second direction*" (*i.e.*, the Y direction), and "*each connect to a corresponding one of the common electrodes*" (*i.e.*, a single touch electrode 30, as indicated by the dots). *Id.*; Ex. 1003 ¶¶202-203.

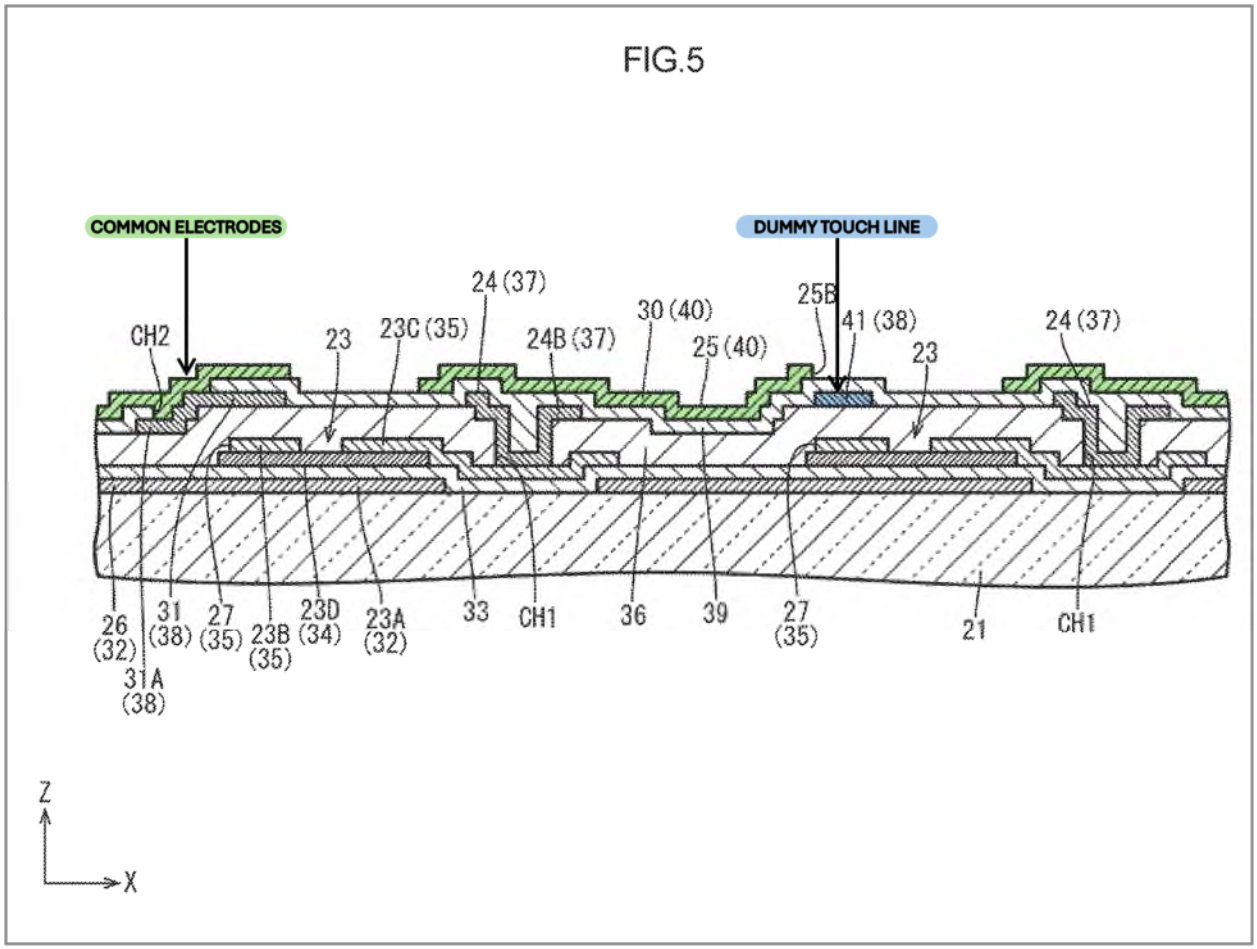
Yoshida also discloses that "*each touch line is connected with a corresponding one of the common electrodes arranged in the second direction*" for the same reasons. *Id.*

f) [18-F]

Yoshida discloses and renders obvious that the touch panel comprises "*a dummy touch line that extends along the second direction, is formed in a same layer as the touch lines, and is electrically isolated from any of the common electrodes*." Ex. 1003 ¶204.

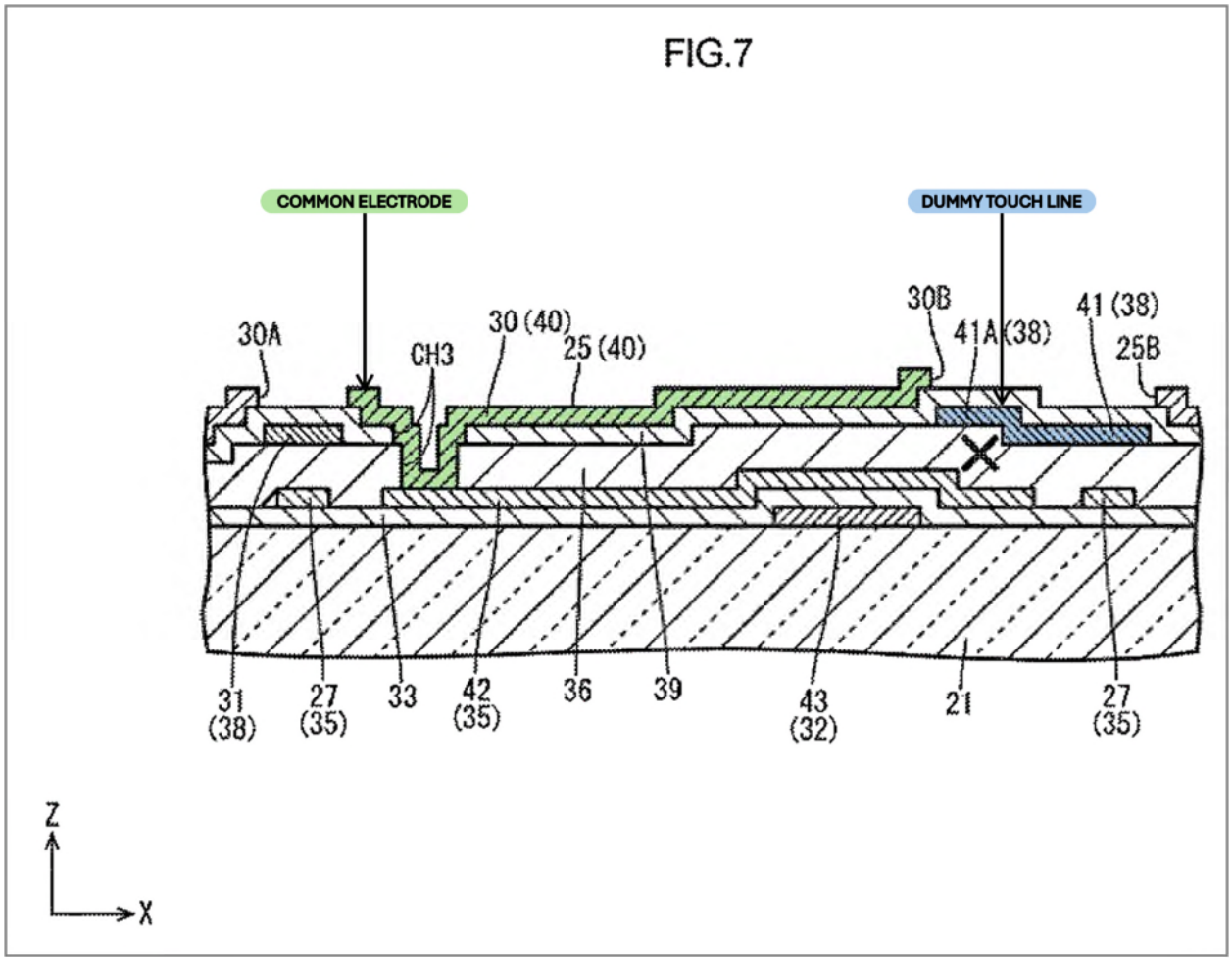
Yoshida teaches the claimed "*dummy touch line*" as "spare touch line 41." As explained above in Section V.C.1, the term "*dummy touch line*" should be construed to refer to a "line that does not carry a touch signal." Yoshida's spare touch lines 41 that are between common electrodes meet this construction. Yoshida explains that these spare touch lines are "excess" touch lines, beyond the requisite number of touch lines 31 needed to connect to the touch electrodes 30, and so they are not themselves connected to the touch electrodes. Ex. 1003 ¶205. Rather, these spare touch lines 41 potentially "enable[] a repair when a disconnection has occurred in the touch lines 31." Yoshida at [0035]; Translation at [0023]; Ex. 1003 ¶¶206-207.

Thus, by default, as shown in Figure 5, the (blue) spare touch lines 41 are not connected with the (green) touch electrodes 30 and so they do not carry any touch signal.



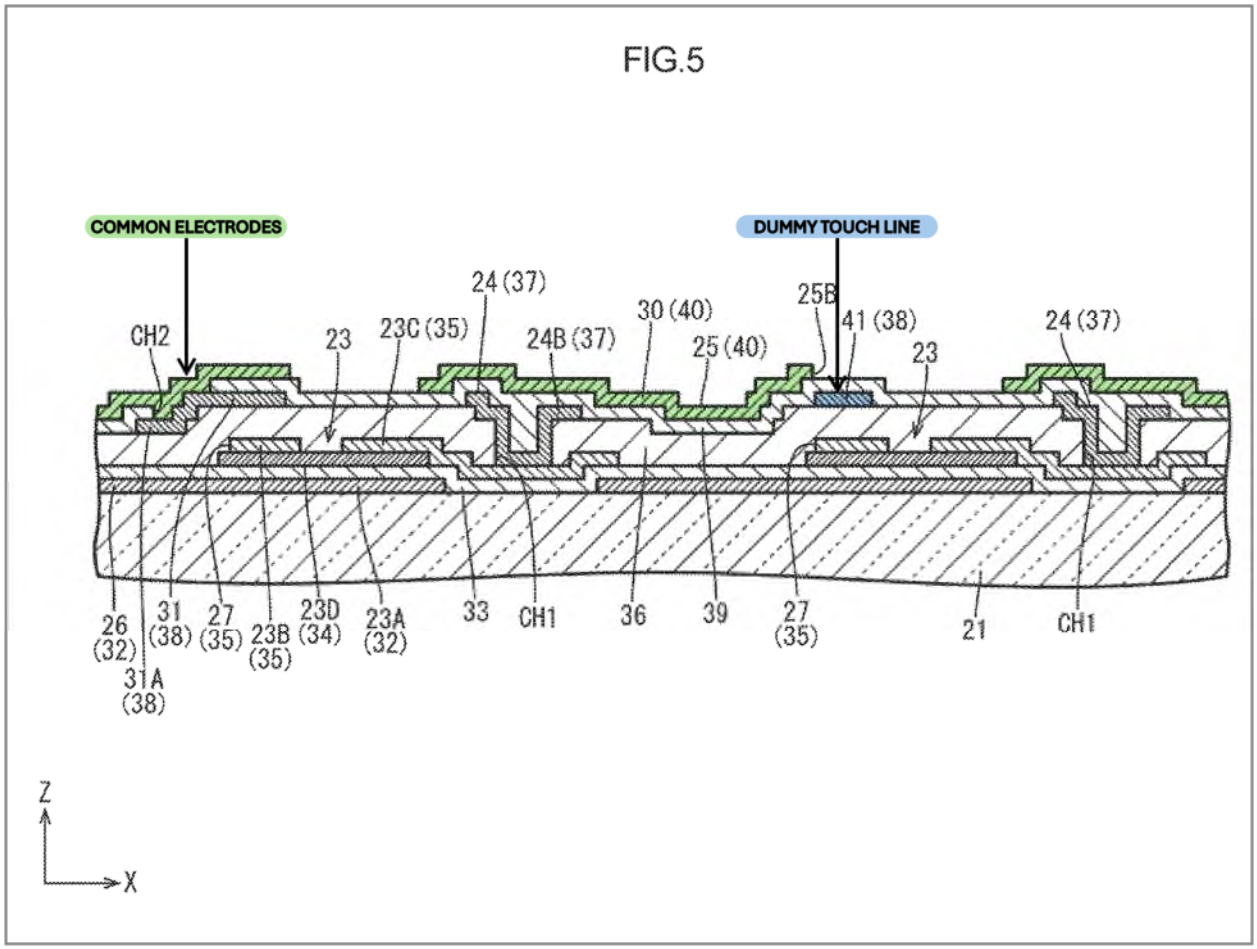
Yoshida at [0035], Fig. 5; *see also* Translation at [0023], Fig. 5; Ex. 1003 ¶207.

Yoshida only teaches that the spare touch lines 41 can selectively be connected with the touch electrodes 30 if "a disconnection has occurred in the touch line 31." Yoshida at [0036]-[0037]; Translation at [0024]-[0025]. This is shown in Figure 7:



Yoshida at [0036], Fig. 7; *see also* Translation at [0024], Fig. 7; Ex. 1003 ¶207.

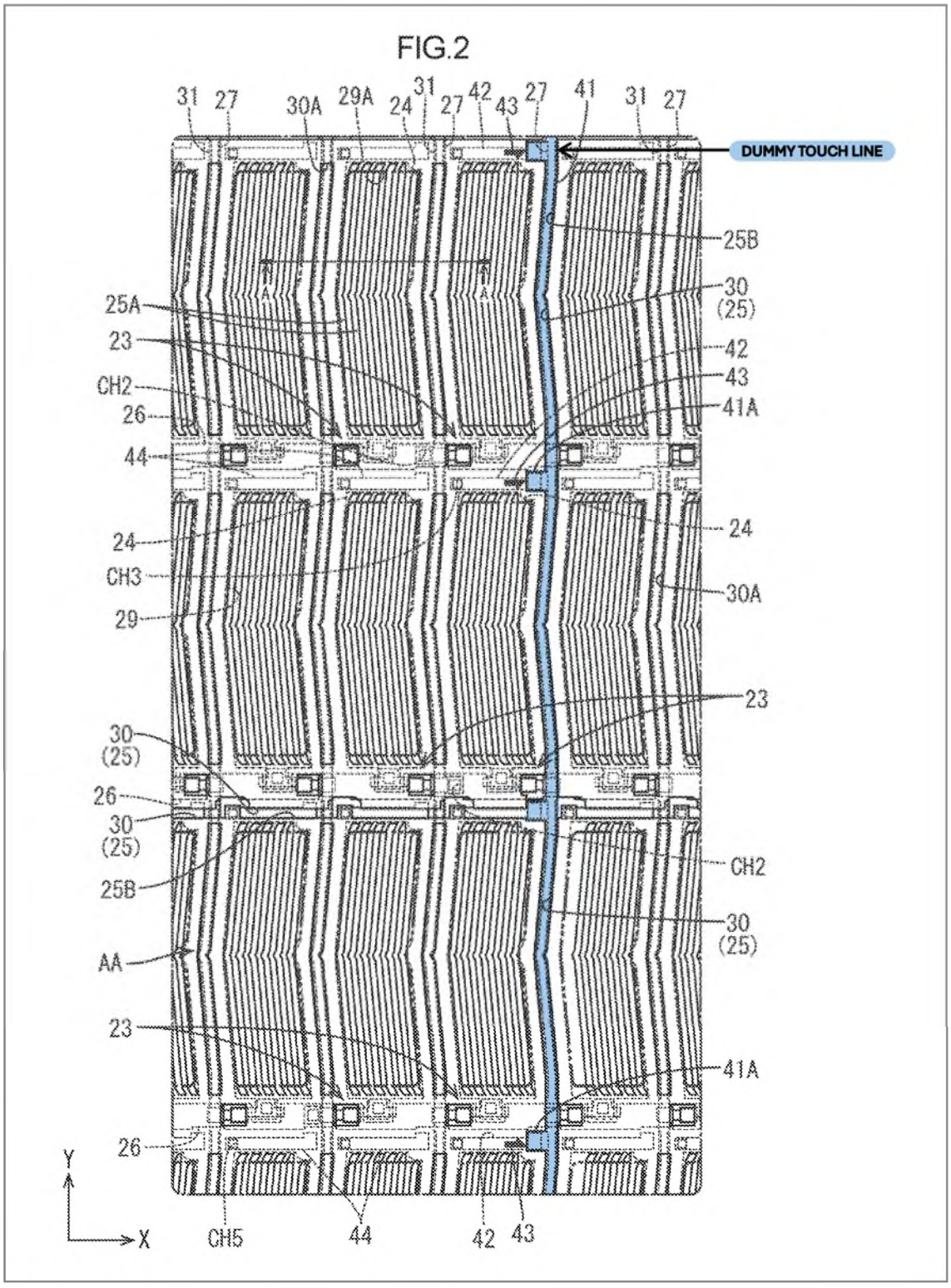
Normally, when the touch line 31 remains connected, there is no need to perform this connecting process, and the insulation between the spare touch lines 41 and touch electrodes 30 is maintained. Figure 5 shows this scenario, with Yoshida's (blue) spare touch lines 41 *"electrically isolated*" from all of the (green) touch electrodes 30:



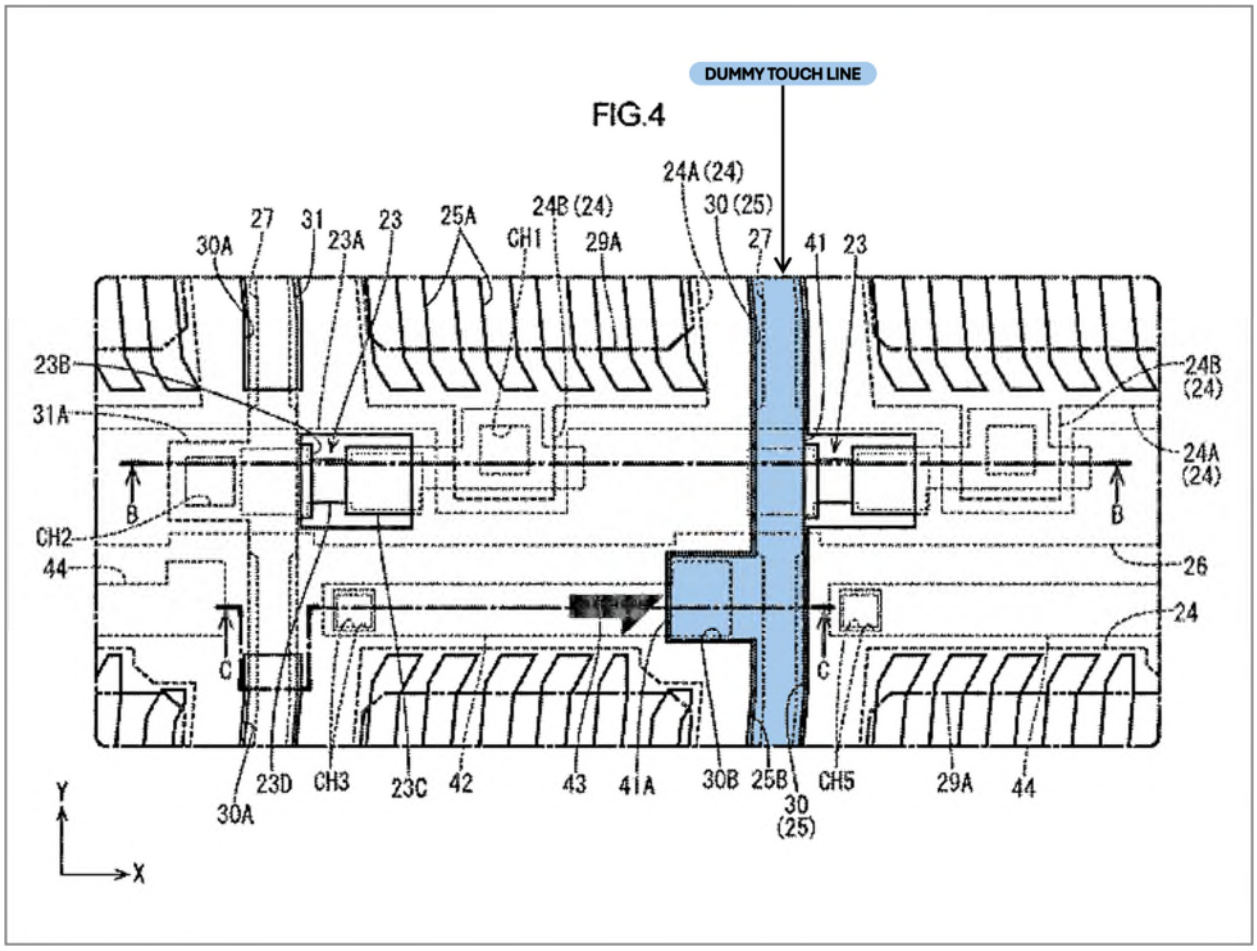
Yoshida, Fig. 5; Translation, Fig. 5. *See also* Yoshida at [0027] (spare touch lines are "not connected to the touch lines 31" and thus, must also not be connected to touch electrodes 30); Translation at [0015]; Ex. 1003 ¶¶205-207. For this reason, Yoshida's spare touch lines 41 teach Claim 18's "*dummy touch line[s]*," regardless of whether or not Petitioner's construction is not adopted. And, for these same reasons, the spare touchlines 41 are also electrically isolated from any of the common electrodes, as the claim requires.

Yoshida also explains that its spare touch lines 41 "extend in parallel with

the Y-axis direction." Yoshida at [0027]; [0035]; Translation at [0015], [0023]:

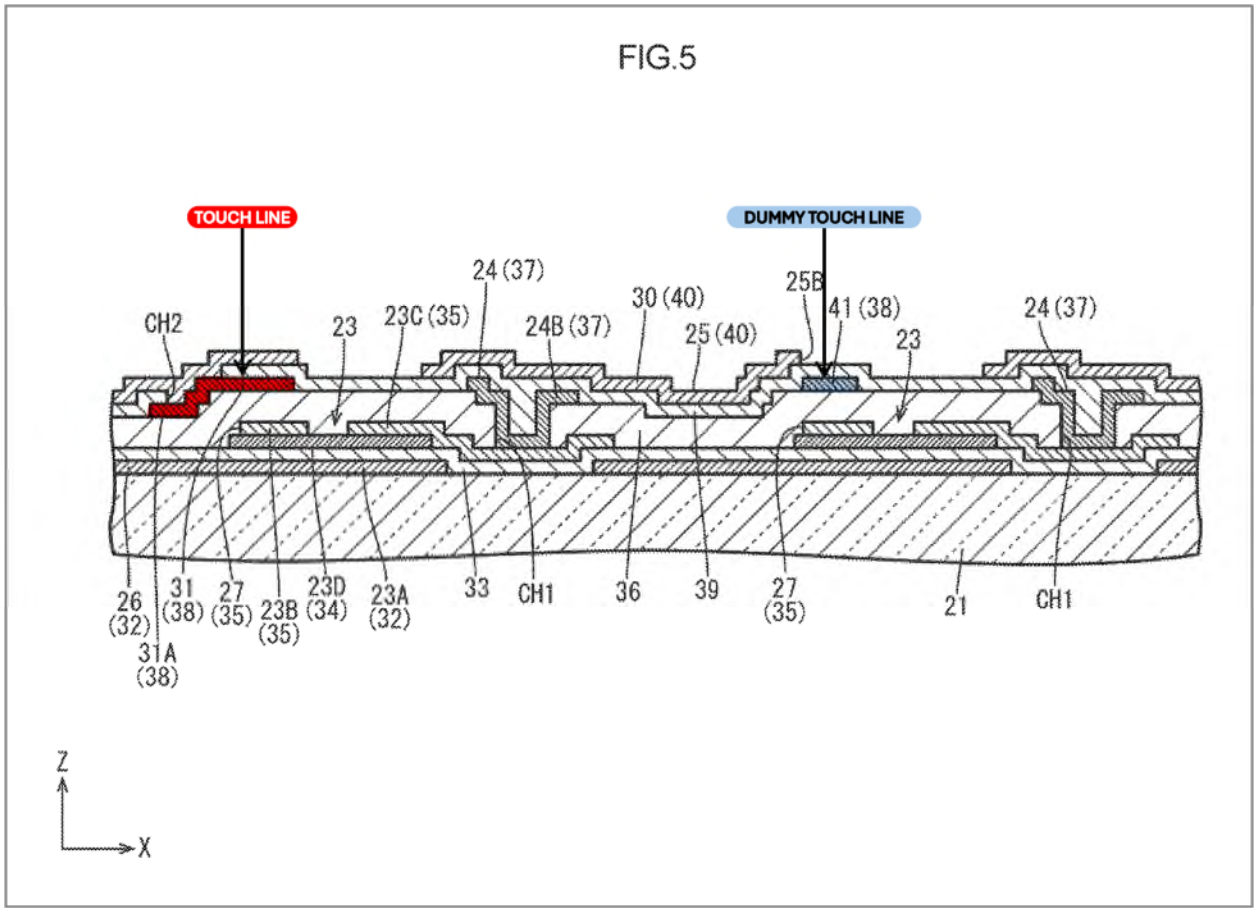


Yoshida, Fig. 2; Translation, Fig. 2.



Yoshida, Fig. 4; Translation, Fig. 4; Ex. 1003 ¶208.

Yoshida further teaches that its touch lines 31 and spare touch lines 41 are "mutually disposed in the same layer." Yoshida at [0033]; [0035] ("The spare touch line 41, as illustrated in FIG. 5, is made of the same third metal film 38 of the touch lines 31"); *see also* Translation at [0021], [0023].



Yoshida, Fig. 5; Translation, Fig. 5; Ex. 1003 ¶209.

Further, if the term "*dummy touch line*" were construed to require that it provide the functionality or benefits described (but not claimed) in the '025 patent, Yoshida would still teach such a dummy touch line. As the '025 patent explains, the gap between two horizontally adjacent common electrodes can lead to "unintended rotation of liquid crystal molecules existing in the vicinity of the gap … due to the electromagnetic field from the data line 50." '025 patent, 21:61-22:3. The dummy touch line is connected, outside the display area to a source that supplies it with the "same voltage level as the common voltage (Vcom) … so that

[the] dummy touch line 60B and common electrode 30 have the same potential when displaying images." '025 patent, 20:12-19. This "fixed voltage" causes the "electromagnetic field from data line 50 existing below second separation area SA2" to be "more effectively shielded by dummy touch line 60B" and "prevent[s] the occurrence of the display unevenness." *Id.* 22:8-14; Ex. 1003 ¶¶210-211.

Yoshida teaches that its spare touchlines are configured in precisely the same way. Yoshida teaches that certain spare touch lines are located in the separation area and overlap the data line, and therefore are between the data line and the liquid crystal layer. Yoshida at [0027], [0035], [0051]; Translation at [0015], [0023], [0039]. Like the dummy touch line in the '025 patent, Yoshida teaches that these spare touch lines carry the common voltage carried by the common electrodes. Specifically, in its third embodiment,[8] Yoshida explains that the spare touch lines are provided "with the same common signal supplied to the common electrode." Yoshida at [0062; [0065]; Translation at [0050], [0053]. This configuration helps to reduce instability in that area caused by the electrical field of the common electrode and pixel electrode. *Id.*; Ex. 1003 ¶¶212-214.

A POSITA would understand that this configuration shields liquid crystals

[8] This embodiment simply builds on the first embodiment, discussed above. *See* Yoshida at [0061]; Translation at [0049].

from the electrical field of the data line. For example, Xie (Ex. 1007)—which likewise describes an in-cell touch panel and predates the '025 patent—demonstrates that it was already well known that a "shield line 106" with the "same electric potential as the common electrode 102" could be used "for shielding an electrical field generated during transmission of signal by the data line 101." Xie at [0029]. Xie positioned its "shield line" in the same place, "at a location corresponding to the gap 1020" that is "provided between two neighboring common electrodes 102." *Id.* And Xie shows that it was known that a shield line placed above the data line and supplied with the common voltage could "shield the electrical field generated by the data line 101, thus avoiding effects on rotations of the liquid crystals 130 by the electrical field through the gap 1020, thereby solving the light leakage problem of the existing touch display devices." Xie at [0031]. Accordingly, a POSITA would have been familiar with both the problem concerning inadvertent liquid crystal rotation and the shield line solution, and recognize that Yoshida's configuration would provide the same shielding. Ex. 1003 ¶¶215-216.

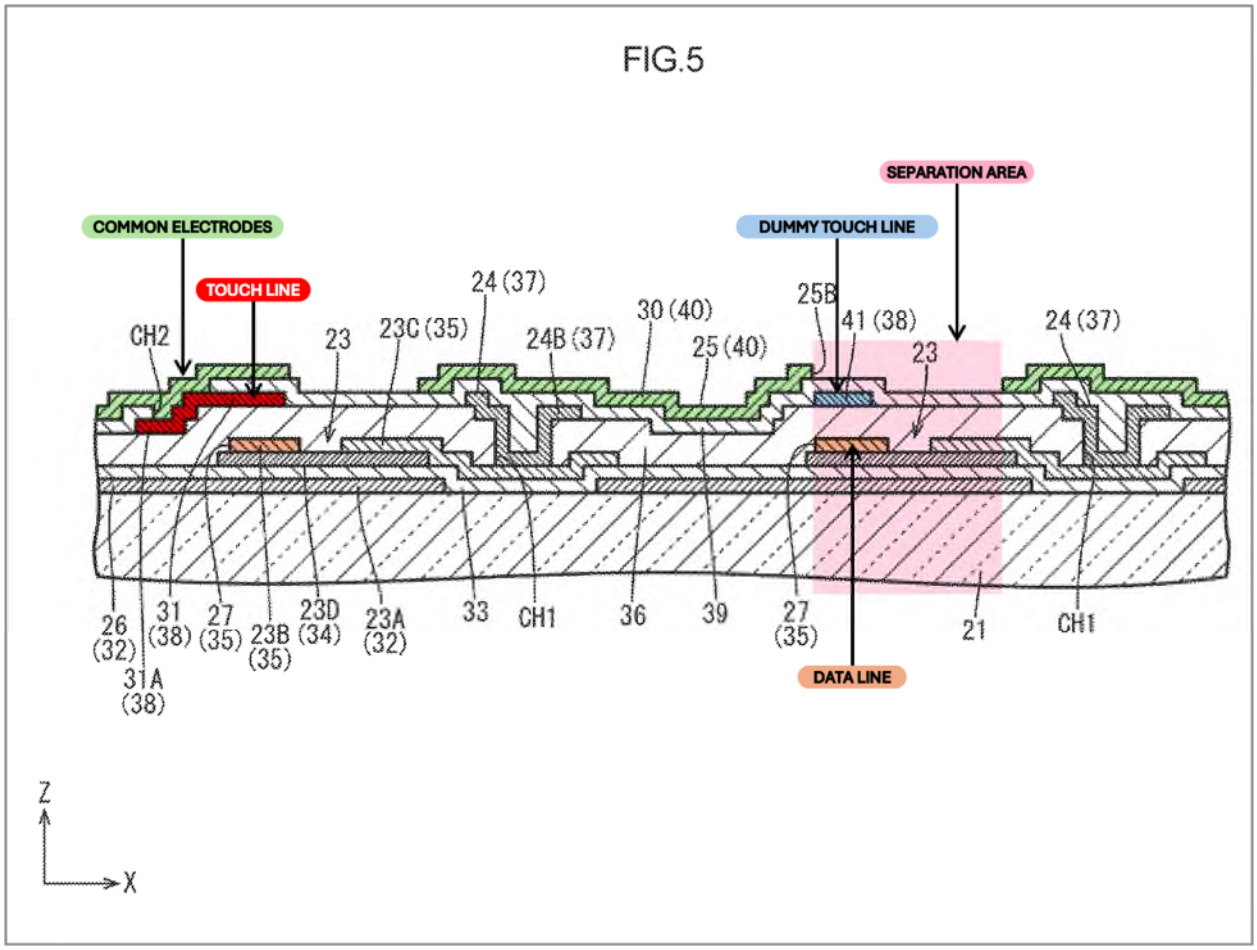
g) [18-H]

Yoshida discloses and renders obvious that "*two of the common electrodes adjacent in the first direction are separated from each other with a separation area*

on the data line." Ex. 1003 ¶217.

Yoshida explains that there are "partitioning openings (partitioning slits) 25B" that exist "between two touch electrodes 30 adjacent to each other in the X-axis direction Yoshida at [0027]; Translation at [0015]. This partitioning opening is a "*separation area*" between "*two of the common electrodes adjacent in the first direction*" as required by the claim. The spare touch lines 41 are "arranged between two touch electrodes 30" so "as to overlap partitioning openings." *Id.* Further, the spare touch lines overlap the source lines 27, *i.e.*, data lines. Yoshida at [0035]; Translation at [0023]. Thus, the "*separation area*" is "*on the data line*" as required by the claim. Ex. 1003 ¶¶218-219.

This arrangement is depicted in Figures 2, 4, and 7 but it is most easily seen in Figure 5:



Yoshida, Fig. 5; *see also* Figs. 2, 4, 7; Translation, Figs. 2, 4, 5, 7.

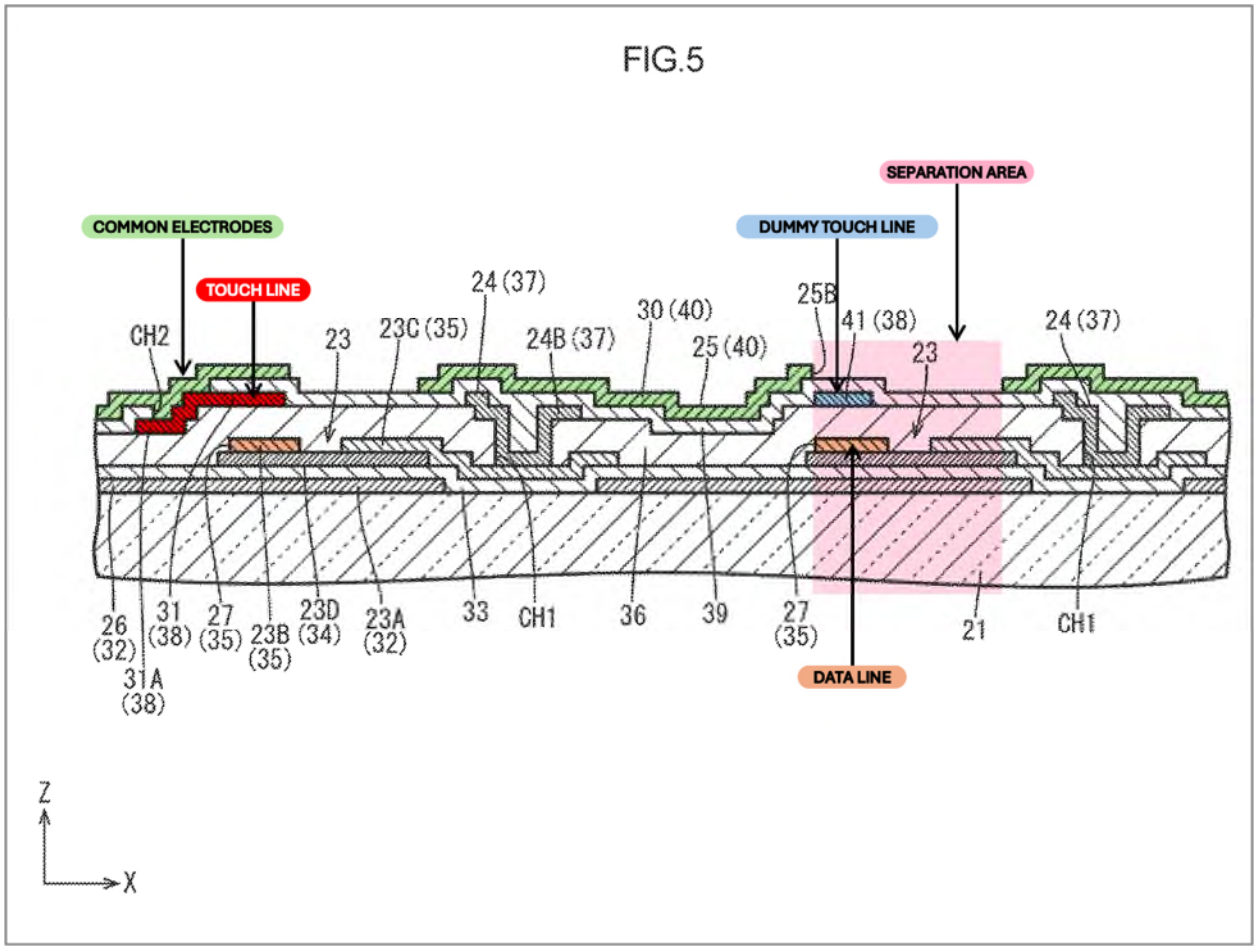
As shown, the partitioning openings 25B forms a (pink) gap which separates two adjacent (green) touch electrodes 30 in the X-axis direction (*i.e.*, separate two of the "*common electrodes adjacent in the first direction*") and that gap is also on the (orange) source lines 27 (*i.e.*, the data lines). Ex. 1003 ¶220.

h) [18-I]

Yoshida discloses and renders obvious that "*the dummy touch line is provided in the separation area*." Ex. 1003 ¶221.

As discussed for limitation [18-H] above, spare touch line 41, *i.e.*, the dummy touch line, is provided in the partition between touch electrodes, *i.e.*, the "*separation area,*" which is wider than the spare touch line. *See* Yoshida at [0027] ("[T]he spare touch line 41 is arranged between two touch electrodes 30 adjacent to each other in the X-axis direction so as to overlap partitioning openings (partitioning slits) 25B" (internal parenthesis omitted); [0062], [0065] (explaining that the spare touch line is within the partition area and does not overlap with the common electrodes); Translation at [0015], [0050], [0053]; Ex. 1003 ¶222.

As shown best in Figure 5, the (blue) spare touch lines 41 are between two (green) touch electrodes 30 adjacent to each other in the X-axis direction (*i.e.*, in the (pink) separation area, as explained for the previous limitation).



Yoshida, Fig. 5; *see also* Fig. 4; Translation, Figs. 5 and 4; Ex. 1003 ¶223.

D. GROUND 4: Claims 10, 11, 14, and 17 are Obvious Under 35 U.S.C. § 103 Over Yoshida in Combination With Kim II.

1. Independent Claim 10

Claim 10 is rendered obvious by the combination of Yoshida and Kim II. As explained above, Claim 10 largely mirrors Claim 18 but includes additional limitations pertaining to segment electrodes, which are taught by Kim II.

a) [10-PRE] through [10-F], and [10-I] through [10-K]

Claim elements [10-PRE] through [10-F] and [10-I] through [10-K] are

largely identical to limitations in Claim 18 already discussed above, with only non-substantive differences. *See* Ex. 1014. Specifically, aside from a typographical error in Element [18-H], Elements [10-A] through [10-E] and [10-J] through [10-K] are identical to Elements [18-A] through [18-E] and [18-H] through [18-I], respectively. They are therefore obvious in light of Yoshida for the same reasons provided above for Ground 3. *See* Sections VII.C.1.b, c, d, e, g, h; Ex. 1003 ¶¶225-228.

The preamble of Claim 18 requires that the pixels be arranged such that the second direction be "*orthogonal* to" the first direction, whereas Claim 10 requires that the second direction be "*intersecting*" the first direction. Yoshida teaches an array intersecting at right angles, i.e., orthogonal, as shown above. *See* Section VII.C.1.a; Ex. 1003 ¶¶229-230.

Claim element [10-F] has a minor wording difference from element [18-F] specifying that the dummy touch line is "*extending*" rather than "*extends*" in the second direction, and further requires that the dummy touch line be "*not electrically connected*" to the common electrodes rather than "*electrically isolated*" from them. These slight wording changes are non-substantive differences and so are taught or rendered obvious by Yoshida, as explained above. *See* Section VII.C.1.f.; Ex. 1003 ¶231.

Claim element [10-I] is very similar to, but slightly different than [18-G]. Element [10-I] recites "*wherein the touch lines are connected one-by-one with the common electrodes arranged in the second direction among the common electrodes,*" whereas Element [18-G] recites "*wherein each touch line is connected with a corresponding one of the common electrodes arranged in the second direction.*" These limitations are substantively identical and are rendered obvious by Yoshida for the same reasons set forth for limitations [18-G] above. *See* Section VII.C.1.e; Ex. 1003 ¶¶232-233.

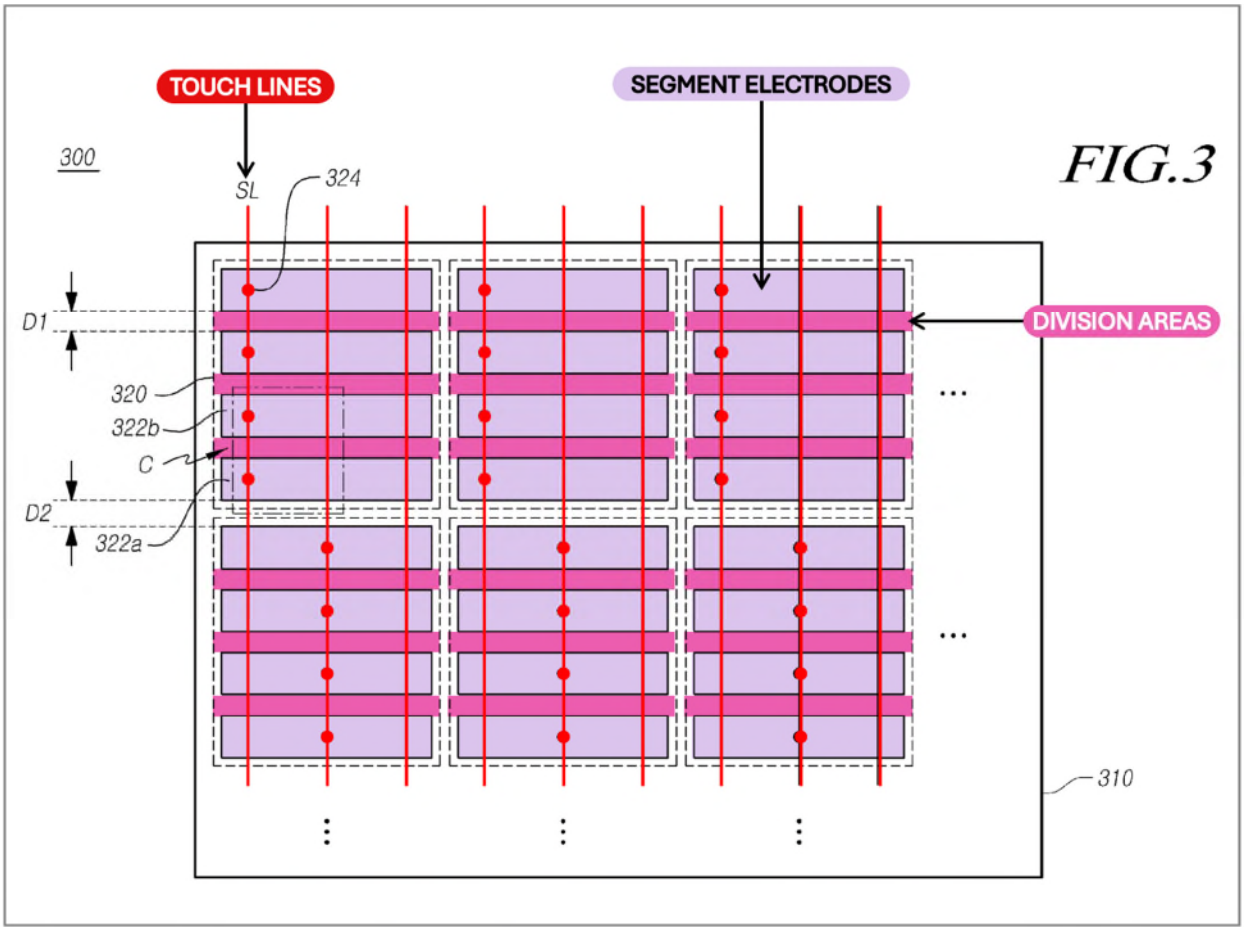
b) [10-G]

Kim II teaches and renders obvious "*wherein each common electrode has segment electrodes divided with a division area on the gate line*."

While Yoshida does not teach that its common/touch electrodes are divided into segment electrodes, Kim II teaches that such common electrodes can be divided into several "common voltage electrode rows," *i.e.*, "*segment electrodes*." Kim II at [0052]; Ex. 1003 ¶¶234-235.

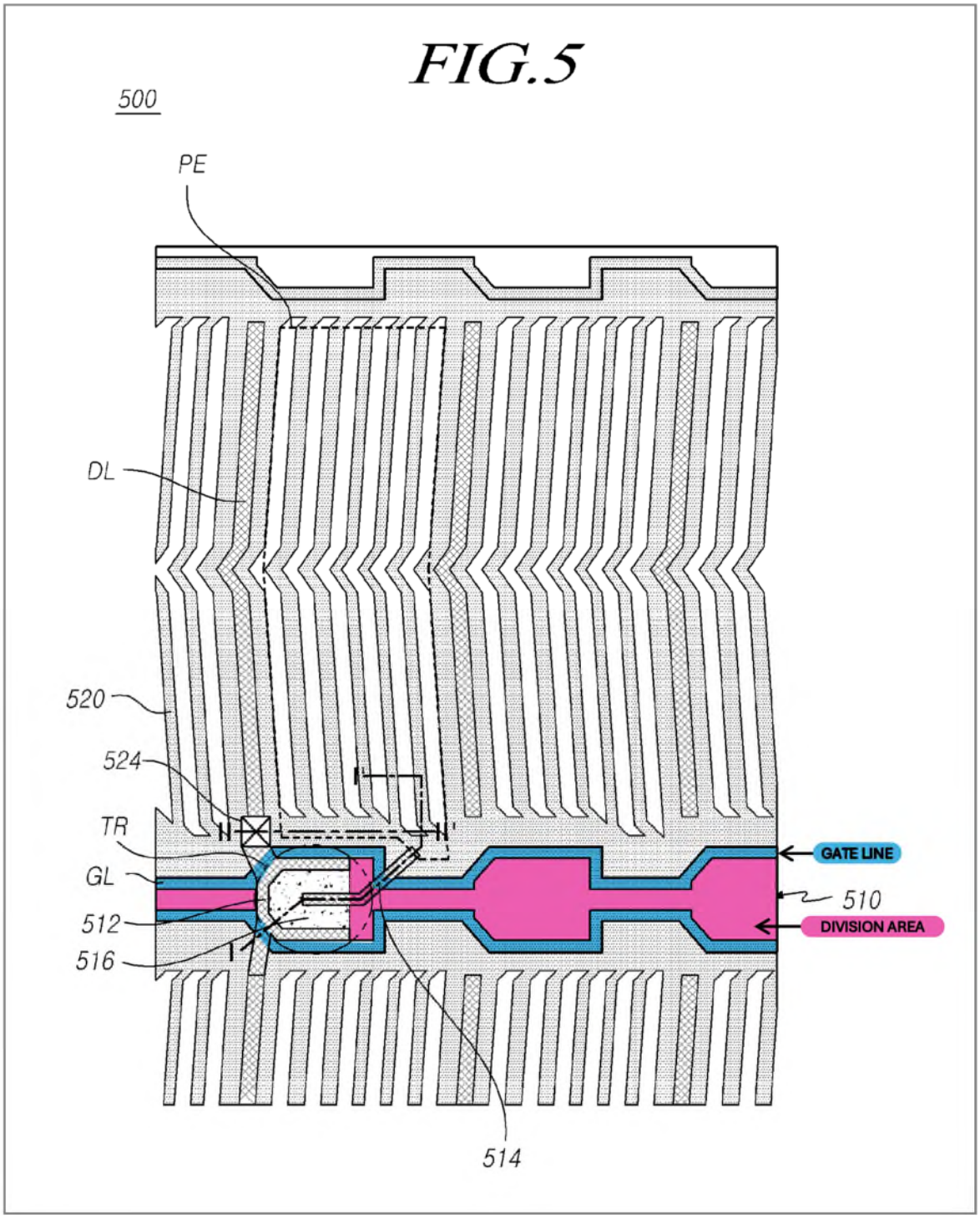
As shown in the figure below, Kim II teaches common electrodes, divided into segment electrodes, as the claim requires. *See* Section VII.A.1.g. Specifically, Kim II teaches in connection with Figure 3 that "[e]ach touch electrode 320 may include a plurality of common voltage electrodes," with "a

separation distance D1 between common voltage electrodes in different rows within the touch electrode 320." Kim II at [0052], [0060].



Kim II, Fig. 3; Kim II at [0058]. Kim II further teaches that there is a (pink) space between the "voltage electrode rows," which Kim II describes as a "separation distance D1." Kim II at [0060]. Kim II also refers to this area as "separation space 430b" which it describes as "separating common voltage electrode rows within a touch electrode 320." Kim II at [0065]; Ex. 1003 ¶¶236-237. And Kim II, in connection with Figure 5, likewise explains that each touch electrode is divided

into "common voltage electrodes 520" that are separated within a touch electrode via a (pink) "separation space 510," shown below:



Kim II, Fig. 5. Kim II at [0087]-[0090]. Further, Kim II teaches that this (pink) separation space 510 is "*on the*" (blue) gate line as the claim requires. Kim II at [0090] ("The separation space 510, *i.e.*, separation area, formed between different rows of the common voltage electrodes 520 may correspond to a line area of the gate lines GL. Specifically, in the exemplary embodiment as illustrated in FIG. 5, the gate line GL or a portion of the gate line GL may be formed in the separation space 510 between two common voltage electrodes 520."); Ex. 1003 ¶¶236-239.

A POSITA would have been motivated to implement Kim II's design for dividing common electrodes into segment electrodes "*on the gate line*." Ex. 1003 ¶¶240-241. As explained above (*See* Section VI.B), Kim II describes several related problems that arise when common electrodes are disposed over large areas of pixels. Such arrangements lead to "a difference in coupling capacitance between a transistor positioned at the outer periphery of the touch electrode and a transistor positioned inside the touch electrode." Kim II at [0015]. This capacitance, in turn "affects a gate-source voltage" of the gate electrode (*i.e.*, the voltage necessary to turn on the transistor) and causes adverse effects, such as the pixel electrode being unable to fully receive the data voltage, or causing the transistor to take longer to turn on. Kim II at [0016], [0047]. Ultimately, this non-uniformity in the gate voltage of the transistors leads to pixel defects and horizontal line defects in the display, particularly at the outer periphery of the

common electrodes. Kim II at [0017], [0024], [0048], [0107]; Ex. 1003 ¶¶240-241.

Kim II observed that "the gate line GL and an electrode adjacent thereto greatly affect a capacitance of the gate electrode 518." Kim II at [0090]. Accordingly, Kim II teaches that the above-discussed problems with non-uniform capacitance and hindered performance of the gate electrode can be resolved by dividing the common electrodes into rows such that the separation areas between rows would fall on the gate line, leaving it uncovered, as explained above. Kim II at [0089]-[0090]. Based on Kim II's express teachings, a POSITA would appreciate that this gate line placement would allow "a capacitance of the gate electrode 518 [to] become[] substantially uniform regardless of being inside the touch electrode and at an outer periphery of the touch electrode." Kim II at [0089]; Ex. 1003 ¶241. Further, because this placement would reduce the capacitance of the gate electrode, "transistor TR may be driven at an increased speed." Kim II at [0090]; Ex. 1003 ¶241. Likewise, the POSITA would appreciate that Kim II's placement of the gate line and these advantages serve to prevent the pixel defects and horizontal line defects caused by the overlap capacitance of a common electrode. Kim II at [0024], [0107]; Ex. 1003 ¶241.

Kim II teaches that these issues are particularly problematic for in-cell panels that use the "in-plane" structure (*i.e.*, where the pixel electrodes and

common electrodes are both disposed on the same side of the liquid crystals), noting that, for such a structure, these capacitance issues "may become a big problem." Kim II at [0092]. A POSITA following Yoshida's teachings without Kim II's guidance would have encountered these problems, and been motivated to find a solution, such as Kim II's. Ex. 1003 ¶¶243-244. And because Yoshida likewise includes "touch electrodes" that are "each arranged in an area spanning over a number (such as several tens) of pixel portions PX," a POSITA following Yoshida's teachings would be motivated to follow Kim II's teachings to avoid the problems discussed above. Yoshida at [0026], [0028]; Translation at [0013], [0014].

A POSITA would have been motivated to follow the teachings of Yoshida in part because it provides a robust and detailed teachings of the conventional structures for an in-cell touch panel. Ex. 1003 ¶¶244-245. A POSITA would recognize that both Yoshida and Kim II incorporate design elements to reduce the negative impacts of capacitance, and would recognize Kim II and Yoshida as pursuing similar design goals. *Id.* ¶243. Further, a POSITA would be particularly motivated to combine Kim II's teachings with Yoshida because Yoshida uses exactly the type of "in-plane" structure that Kim II warns may suffer more acutely from the described capacitance problems, as both its pixel electrodes and common electrodes are below the liquid crystals. *See* Yoshida at [0030] (the array substrate

includes both pixel and touch electrodes), Fig. 3; Translation at [0018], Fig. 3. Accordingly, a POSITA would be particularly motivated to avoid the "big problem" described by Kim II, while likewise being assured that Kim II's proposed solution is appropriate and compatible for Yoshida's structure. Ex. 1003 ¶¶243-245.

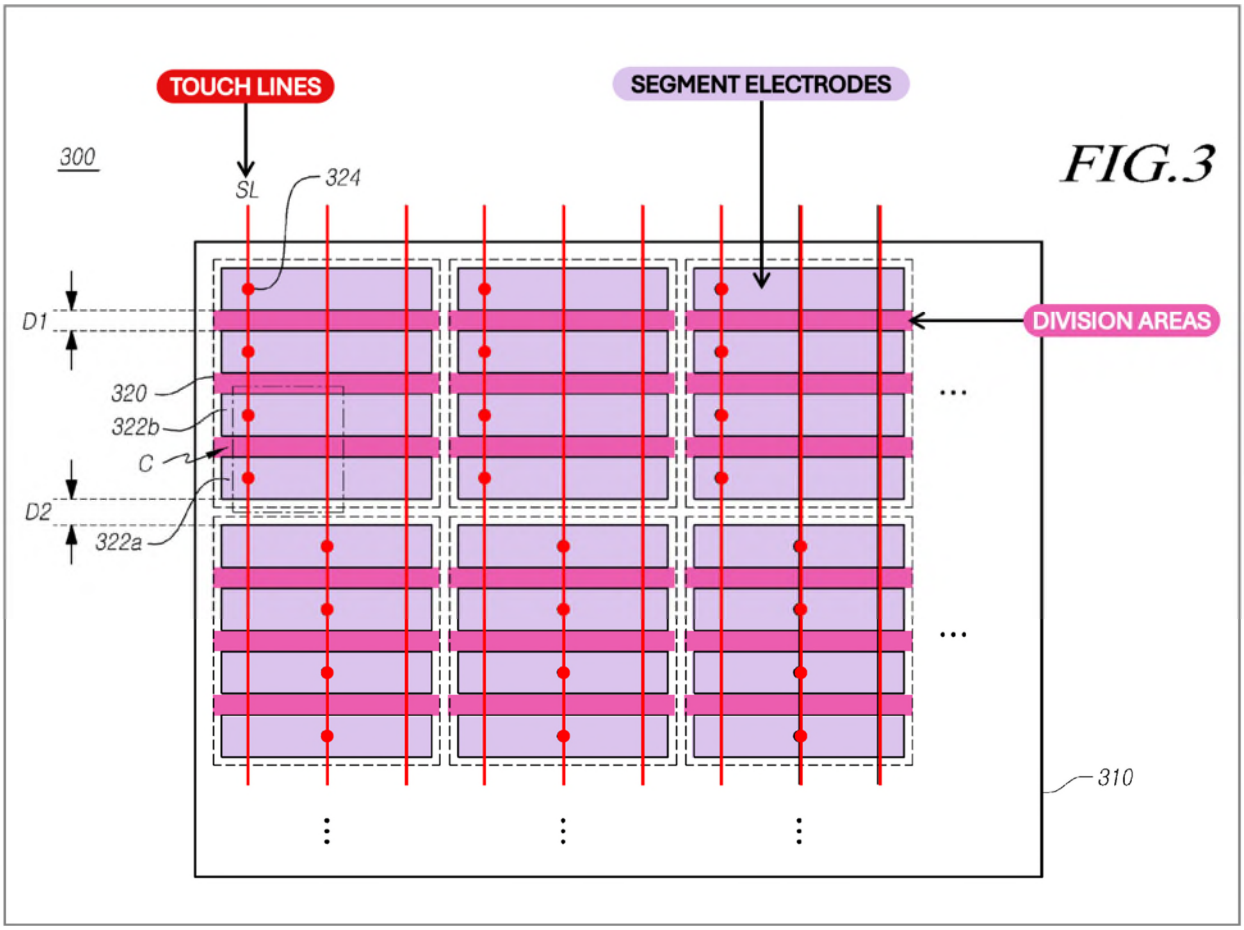
A POSITA would recognize that Yoshida's provides advantages as well. *Id.* ¶¶246-250. Specifically, Yoshida provides a way to repair potential touch line disconnects with minimal risk of "secondary trouble" such as damage to the touch electrodes or the liquid crystal layer, thus increasing manufacturing efficiency and yield. Yoshida at [0037]; Translation at [0025]; Ex. 1003 ¶248. A POSITA would also appreciate Yoshida's spare touchlines help reduce instability caused by the electric fields of the common electrode and pixel electrode. Yoshida at [0062], [0065]; Translation at [0050], [0053]; Ex. 1003 ¶249. Further, a POSITA would appreciate that Yoshida's spare touchlines carrying the common voltage in the gap between touch electrodes and over the data line would beneficially "shield the electrical field generated by the data line 101" to prevent inadvertent rotation of liquid crystals. *See, e.g.*, Xie at [0031]; Ex. 1003 ¶250.

Because Yoshida and Kim II both relate to similar touch panels involving common electrodes facing pixels, a POSITA would have recognized that Yoshida and Kim II describe highly analogous teachings and have significant confidence

that their teachings were compatible and could be combined with a reasonable expectation of success. Ex. 1003 ¶242.

c) [10-H]

Kim II teaches and renders obvious "*segment electrodes included in one of the common electrodes are connected by at least one of the touch lines*." In particular, Kim II also teaches that the segment electrodes included in one of the common electrodes are connected by at least one of the touch lines. Kim II explains, in connection with both Figures 3 and 4, that each of the common electrode rows within a touch electrode, *i.e.*, segment electrodes, is connected to the others via a single "sensing line," *i.e.*, touch line. Kim II at [0058], [0066]; *see also* [0056], [0083]. Figure 3 below depicts these (red) touch lines connect to all the (purple) rows within a common electrode through contact holes, such that one touch line connects to all rows within a common electrode:



Kim II, Fig. 3; *see also* Kim II, Figs. 4 and 5 (showing connection via contact holes 324 and 524, respectively); Ex. 1003 ¶¶251-252, 255.

Further, while Kim II does not discuss the touch lines connecting to every row within a common electrode in connection with Figure 5, that is because Figure 5 focuses only on a single row. Ex. 1003 ¶¶253-254. Kim II's Figure 5 embodiment provides additional details to the Figures 3 and 4 embodiment and does not suggest any change in the connections of the touch lines to the rows. *Id.* At the very least, a POSITA combining Kim II and Yoshida would have found it

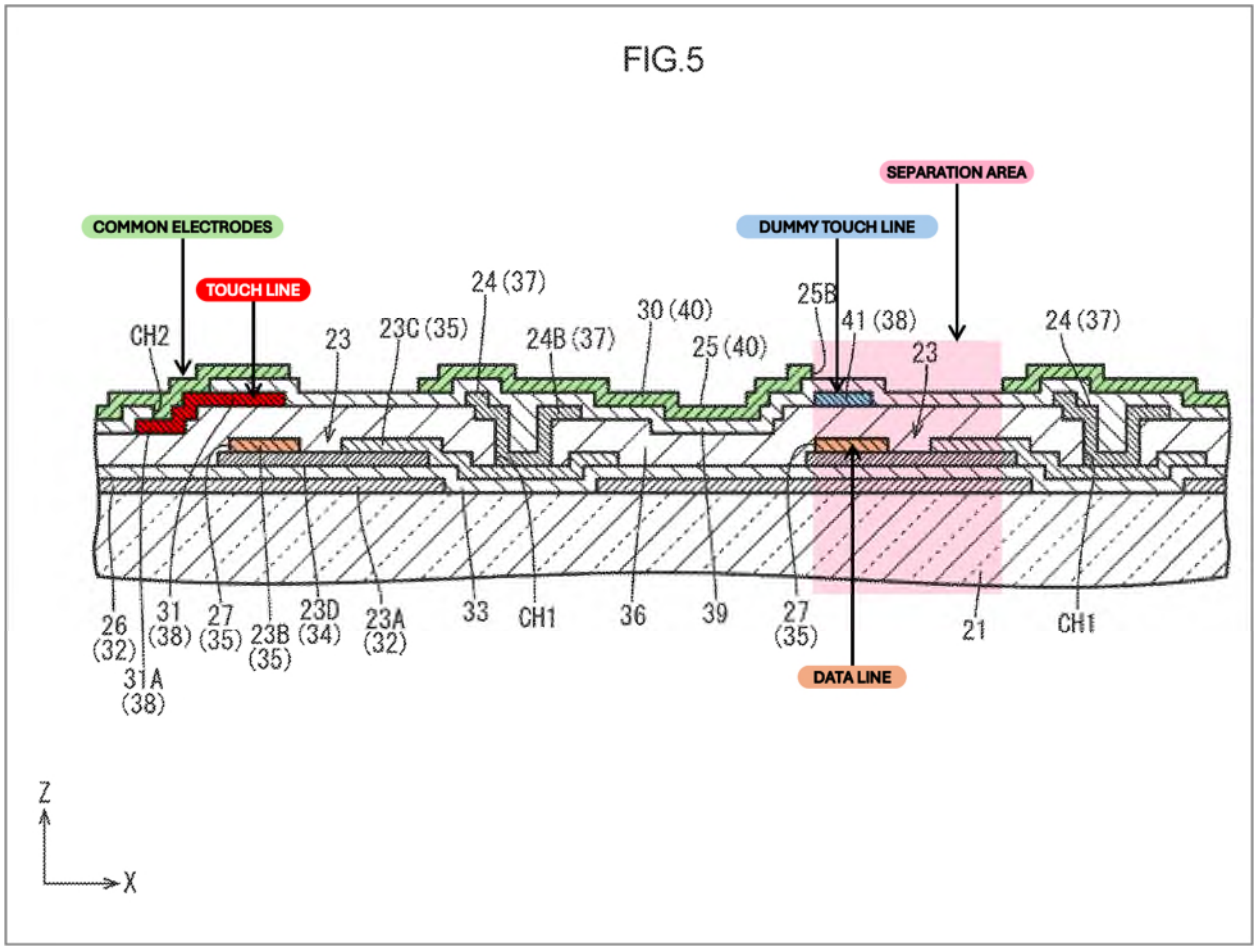
obvious to, and been motivated to, connect segment electrodes within a single touch electrode 30 to a common touch line 31 based on Kim II's teachings that doing so allows the common voltage electrodes to "function as a single common voltage electrode." Kim II at [0055]; Ex. 1003 ¶¶255-256.

2. Claim 11

Yoshida teaches and renders obvious "*wherein a fixed voltage is applied to the dummy touch line, and the fixed voltage is a common voltage to be applied to the common electrode.*" Specifically, Yoshida's spare touchline is provided with "the same common signal supplied to the common electrode." Yoshida at [0062], [0065]; Translation at [0050], [0053]. Yoshida further explains that the "common electrode 25 is supplied with a substantially constant reference potential at all times" which a POSITA would understand to mean that a fixed voltage is applied to the common electrode, as well as the spare touchline. Yoshida at [0030]; Translation at [0018]; Ex. 1003 ¶¶257-260.

3. Claim 14

Yoshida teaches and renders obvious "*wherein a width of the dummy touch line is smaller than a distance between the dummy touch line and the common electrode.*" As is at least rendered obvious by Figure 5, Yoshida shows that the distance between the right side of the spare touch line 41 and edge of adjacent common electrode to the right is larger than the width of the spare touch line 41:

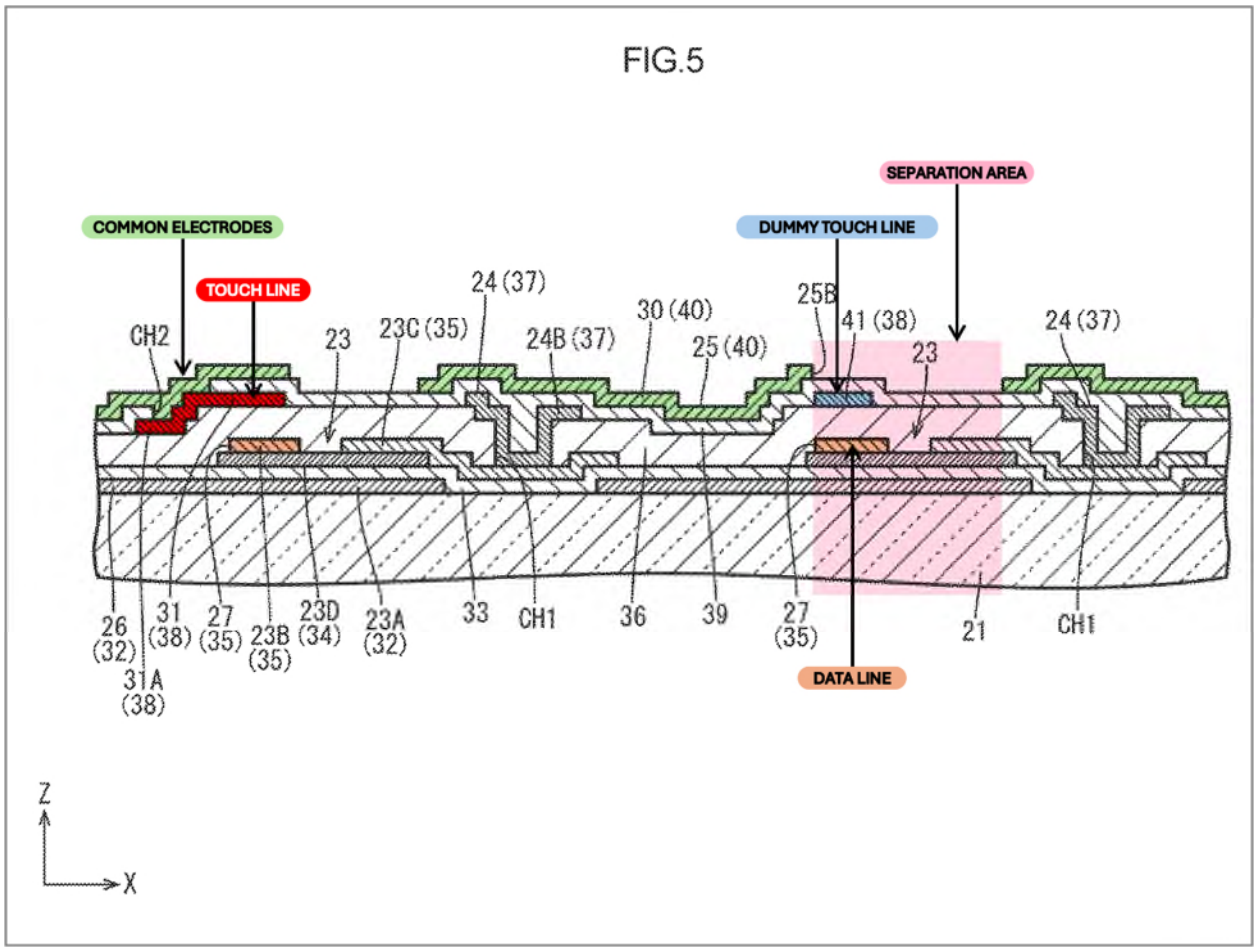


Yoshida, Fig. 5; Translation, Fig. 5; Ex. 1003 ¶¶261-263. Although Yoshida does not specifically discuss the dimensions of its spare touch lines and partition areas, a POSITA would recognize from Figure 5, for example, that it would be obvious to at least attempt a design that employed components with proportions in accordance with the figure. Ex. 1003 ¶264.

4. Claim 17

Yoshida teaches and renders obvious "*wherein the dummy touch line is offset from any of the common electrodes in a planar view*." Specifically,

Yoshida's Figure 5 shows a cross section of Yoshida's spare touch line 41, which shows that, if viewed from a planar view, it would be offset from any of the common electrodes, as it is between and does not overlap any of the common electrodes:



Yoshida, Fig. 5, [0062], [0065] (explaining that certain spare touch lines 41 do not overlap the touch electrodes); Translation, Fig. 5, [0050], [0053]. Ex. 1003 ¶¶265-268.

VIII. SECONDARY CONSIDERATIONS

Petitioner is not aware of any secondary considerations that would overcome these strong showings of obviousness. Ex. 1003 ¶269. Further, any attempt by Patent Owner to rely on alleged secondary considerations cannot overcome the showing of obviousness detailed above. *Tokai Corp. v. Easton Enters., Inc.*, 632 F.3d 1358, 1370 (Fed. Cir. 2011).

IX. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests the Board institute review of the ’025 patent and cancel all Challenged Claims.

Date: August 5, 2025

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,126,025 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42 *et seq.* complies with the type volume limitation in 37 C.F.R. § 42.24(a)(1). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, a table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, or listing of exhibits, and claim listing—contains 13,758 words.

Dated: August 5, 2025

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,126,025 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42 *et seq.* and associated Exhibits 1001-1015 were caused to be served on August 5, 2025 via overnight courier upon the following counsel of record for Patent Owner:

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Re: Paneltouch Technologies LLC; U.S. Patent No. 11,126,025

Courtesy copies were also served via email on Patent Owner's counsel of record in a related district court litigation styled *Paneltouch Technologies LLC v. BOE Technology Group Co., Ltd.*, No. 2:25-cv-00245 (E.D. Tex.):

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