

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE Technology Group Co., Ltd.,
Petitioner,

v.

Paneltouch Technologies LLC,
Patent Owner.

U.S. Patent No. 11,126,025
Original Issue Date: September 21, 2021
Title: IN-CELL TOUCH PANEL

Case No. IPR2025-01267

DECLARATION OF RICHARD A. FLASCK, M.S.

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,126,025 (the “’025 patent”)
1002	Prosecution History of U.S. Patent No. 11,126,025
1003	Declaration of Richard A. Flasck, M.S. (“Flasck Decl.”)
1004	<i>Curriculum Vitae</i> of Richard A. Flasck, M.S. (“Flasck C.V.”)
1005	U.S. Patent Application Publication No. 2016/0224155 A1 (“Kim”)
1006	U.S. Patent Application Publication No. 2017/0192568 A1 (“Kim II”)
1007	U.S. Patent Application Publication No. 2018/0113541 A1 (“Xie”)
1008	U.S. Patent Application Publication No. 2019/0294273 A1 (“Yoshida”)
1009	Japanese Patent Application No. 2018-058356 and Certified Translation (“Translation”)
1010	U.S. Patent No. 3,824,003
1011	Willem den Boer, <i>Active Matrix Liquid Crystal Displays: Fundamentals and Applications</i> (Elsevier 2005)
1012	U.S. Patent No. 4,582,395
1013	Excerpt from <i>Wiley Electrical and Electronics Engineering Dictionary</i> (2004)
1014	Redline comparing Claims 10 and 18 of U.S. Patent No. 11,126,025
1015	U.S. Patent Application Publication No. 2016/0054627 A1

CHALLENGED CLAIM LISTING

Claim	Limitation No.	Limitation
1	[1-PRE]	An in-cell touch panel having an image display area made up of pixels arranged in a first direction and a second direction intersecting the first direction, the in-cell touch panel comprising:
	[1-A]	transistors and pixel electrodes respectively provided in the pixels;
	[1-B]	common electrodes arranged in the first direction and the second direction, respectively facing one or more of the pixel electrodes and provided separately from each other;
	[1-C]	gate lines that extend along the first direction and supply gate signals to the transistors respectively;
	[1-D]	data lines that extend along the second direction and supply data signals to the transistors respectively;
	[1-E]	touch lines that extend along the second direction and are each connected to a corresponding one of the common electrodes; and
	[1-F]	a first bridge line laterally bridging two of the segment electrodes adjacent in the second direction across one of the division areas,
	[1-G]	wherein each common electrode has segment electrodes divided with a division area on the gate line,

Claim	Limitation No.	Limitation
	[1-H]	segment electrodes included in one of the common electrodes are connected by at least one of the touch lines,
	[1-I]	the first bridge line and each of the two of the segment electrodes are connected via a contact hole, and
	[1-J]	the first bridge line extends in the second direction so as to overlap with the segment electrodes included in the one of the common electrodes, and be connected to the segment electrodes included in the one of the common electrodes.
2	2	The in-cell touch panel according to claim 1, wherein the first bridge line is formed in a different layer from the common electrode.
3	3	The in-cell touch panel according to claim 1, wherein the first bridge line is formed in a same layer as the touch line.
4	4	The in-cell touch panel according to claim 1, wherein the contact hole overlaps with the gate line in a planar view.
5	5	The in-cell touch panel according to claim 1, wherein the contact hole does not overlap with the data line in a planar view.
6	6	The in-cell touch panel according to claim 1, wherein the first bridge line overlaps with the data line in a planar view.
8	[8-PRE]	The in-cell touch panel according to claim 1, wherein
	[8-A]	two of the common electrodes adjacent in the second direction are separated from each other with the separation area on the gate line,

Claim	Limitation No.	Limitation
	[8-B]	the in-cell touch panel includes a second bridge line laterally bridging the two of the common electrodes adjacent in the second direction across the separation area, and
	[8-C]	the second bridge line is not electrically connected to any of the two of the common electrodes.
9	9	The in-cell touch panel according to claim 1, wherein a plurality of the first bridge lines are provided in the one of the common electrodes.
10	[10-PRE]	An in-cell touch panel having an image display area made up of pixels arranged in a first direction and a second direction intersecting the first direction, the in-cell touch panel comprising:
	[10-A]	transistors and pixel electrodes respectively provided in the pixels;
	[10-B]	common electrodes arranged in the first direction and the second direction, respectively facing one or more of the pixel electrodes and provided separately from each other;
	[10-C]	gate lines that extend along the first direction and supply gate signals to the transistors respectively;
	[10-D]	data lines that extend along the second direction and supply data signals to the transistors respectively;

Claim	Limitation No.	Limitation
	[10-E]	touch lines that extend along the second direction and are each connected to a corresponding one of the common electrodes; and
	[10-F]	a dummy touch line extending along the second direction, formed in a same layer as the touch lines, and not electrically connected to any of the common electrodes,
	[10-G]	wherein each common electrode has segment electrodes divided with a division area on the gate line,
	[10-H]	segment electrodes included in one of the common electrodes are connected by at least one of the touch lines,
	[10-I]	wherein the touch lines are connected one-by-one with the common electrodes arranged in the second direction among the common electrodes,
	[10-J]	two of the common electrodes adjacent in the first direction are separated from each other with a separation area on the data line, and
	[10-K]	the dummy touch line is provided in the separation area.
11	[11-A]	The in-cell touch panel according to claim 10, wherein a fixed voltage is applied to the dummy touch line, and
	[11-B]	the fixed voltage is a common voltage to be applied to the common electrode.
14	14	The in-cell touch panel according to claim 10, wherein a width of the dummy touch line is smaller than a distance between the dummy touch line and the common electrode.

Claim	Limitation No.	Limitation
17	17	The in-cell touch panel according to claim 10, wherein the dummy touch line is offset from any of the common electrodes in a planar view.
18	[18-PRE]	An in-cell touch panel having an image display area made up of pixels arranged in a first direction and a second direction orthogonal to the first direction, the in-cell touch panel comprising:
	[18-A]	transistors and pixel electrodes respectively provided in the pixels;
	[18-B]	common electrodes arranged in the first direction and the second direction, respectively facing one or more of the pixel electrodes and provided separately from each other;
	[18-C]	gate lines that extend along the first direction and supply gate signals to the transistors respectively;
	[18-D]	data lines that extend along the second direction and supply data signals to the transistors respectively;
	[18-E]	touch lines that extend along the second direction and are each connected to a corresponding one of the common electrodes; and
	[18-F]	a dummy touch line that extends along the second direction, is formed in a same layer as the touch lines, and is electrically isolated from any of the common electrodes,

Claim	Limitation No.	Limitation
	[18-G]	wherein each touch line is connected with a corresponding one of the common electrodes arranged in the second direction,
	[18-H]	two of the common electrodes adjacent in the first direction are separated from each other with a separation area on the data line as, and
	[18-I]	the dummy touch line is provided in the separation area.

I. INTRODUCTION

I, Richard A. Flasck, declare as follows:

1. I have been retained by counsel for BOE Technology Group Co., Ltd., (“BOE”) in the above-captioned *inter partes* review as an independent consultant to offer opinions regarding the validity of the Challenged Claims in U.S. Patent No. 11,126,025 (the “’025 patent”).

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration – supplemented with my own knowledge and experience in the field. Should new materials, analyses, or opinions be introduced subsequent to the filing of this Declaration, I reserve the right to provide supplementary Declarations to the extent necessary to address any such newly introduced items.

3. If requested, I am prepared to explain in a deposition or at a trial before the Patent Trial and Appeal Board (the “Board”) the technology disclosed in the ’025 patent, including the state of the art around 2019, the earliest alleged priority date of the ’025 patent. Similarly, I am prepared to explain the technology disclosed in the prior art references cited herein. This may include, among other things, background information on the fields of display devices and touch panels.

II. QUALIFICATIONS

4. My qualifications to testify as an expert in display devices and touch

panels are set forth in my *curriculum vitae*, attached as Ex. 1004.

5. I have decades of experience as a scientist and consultant in the display devices and touch panel fields.

6. I received a Bachelor of Science in Physics from the University of Michigan, Ann Arbor in 1970. After receiving my bachelor's degree, I was employed as a scientist and manager by Energy Conversion Devices, Inc., where my work focused on the development of electroluminescent displays, thin film photovoltaics, thin film transistors, ablative imaging films, non-volatile memory, multi-chip modules, and superconducting materials.

7. I received a Master of Science in Physics from Oakland University in Rochester, Michigan, in 1976. After completing my master's degree, I continued my employment with Energy Conversion Devices, Inc. until 1982.

8. After leaving Energy Conversion Devices, I founded and served as CEO of Alphasil, Inc., where I developed amorphous silicon thin film transistor (TFT) active matrix liquid crystal displays (AMLCDs). My work at Alphasil included thin film transistor array substrate process and circuit design, data driver and gate driver design, scalars, video circuits, gamma correction circuits, backlighting, and inverter design. At Alphasil I also designed and incorporated touch panel screens into active matrix display devices. The touch panel technologies included resistive and capacitive sensing. I worked at Alphasil from

1982 through 1989.

9. I am the founder and Chief Executive Officer of RAF Electronics Corp. (“RAF”), a company that I established after leaving Alphasil, Inc. (“Alphasil”) in 1989. At RAF, I have developed and patented Liquid Crystal on Silicon (“LCOS”) microdisplay projection technology using active-matrix transistor arrays, as well as proprietary Light Emitting Diode (“LED”) based Solid State Lighting (“SSL”) products. My work at RAF has also included the development of High-Definition Television (“HDTV”) projection technology, including transistor array substrates for LCOS devices and the associated optical systems, as well as advancements in lighting systems using both traditional LED and OLED (Organic Light Emitting Diode) technologies. In 2016, I was granted a patent, U.S. Patent No. 9,328,898, which covers LED and OLED technology and lighting systems, and in 2019, RAF received a CalSEED grant from the California Energy Commission to develop ultra-efficient lighting products and explore options on establishing a Central Valley manufacturing facility.

10. From 2002 to 2007, I also served as a co-founder and Chief Operating Officer of Diablo Optics, Inc., where I developed, produced, and commercialized key optical components for HDTV projectors, such as polarization optics, condenser lenses, projection lenses, and ultra-high performance optical interference filters using thin film stacks in conjunction with LED and thin film

transistor arrays and devices.

11. Between 1997 to 1999, I held the positions of President and Chief Operating Officer at Alien Technology Corporation, where I was responsible for completing a Defense Advanced Research Projects Agency (DARPA) contract and implementing MicroElectroMechanical (“MEM”) fluidic self-assembly (FSA) technology for flat panel displays. I left that position in 1999.

12. I have fifty-five years of professional experience focused heavily on the design and development of flat panel displays, transistor array substrates, touch panels, and OLED and LED devices.

13. I am listed as an inventor on twenty-six patents issued in the United States and foreign countries, including one United States design patent. My inventions concern technologies that include LED devices, semiconductor materials, glass materials, non-volatile memory cells, thin film transistors, flat panel backplanes and displays, and wafer based active matrices, and various transistor array substrates. I have also authored or co-authored more than 25 publications in journals and major international conference proceedings, many of which are specifically related to displays, touch screens, and the associated thin film technologies. My *curriculum vitae* (Exhibit 1004) lists these articles, conference presentations, and patents.

14. I am also a member of several professional organizations, including

Optica (formerly the Optical Society of America (OSA)), the International Society for Optics and Photonics (SPIE), the Audio Engineering Society (AES), the Society for Information Display (SID), and the Institute of Electrical and Electronics Engineers (IEEE).

15. I have served as an expert witness in over sixty patent cases, written scores of expert reports and declarations, and testified in district courts or before the International Trade Commission (ITC) eight times. Since 2019, I have also served as an expert witness in eight Patent Trial and Appeal Board (“PTAB”) proceedings involving touch panel screen technology.

16. My *curriculum vitae* also contains further details regarding my experience, education, publications, and other qualifications that support my ability to render expert opinions in connection with this proceeding.

III. COMPENSATION

17. I am being compensated for my work in this matter at an hourly rate of \$495 for consulting services.

18. My compensation is not contingent upon the opinions I render or the outcome of this proceeding.

IV. MATERIALS CONSIDERED

19. In preparing this declaration, I reviewed and considered the following materials, along with any other documents referenced in the body of my

declaration:

- The '025 patent (Ex. 1001) and its file history (Ex. 1002).
- U.S. Patent Application Publication No. 2016/0224155 A1 (“**Kim**”) (Ex. 1005)
- U.S. Patent Application Publication No. 2017/0192568 A1 (“**Kim II**”) (Ex. 1006)
- U.S. Patent Application Publication No. 2019/0294273 A1 (“**Yoshida**”) (Ex. 1008)
- U.S. Patent Application Publication No. 2018/0113541 A1 (“**Xie**”) (Ex. 1007)

20. I may use these documents and information, or other information obtained during the course of this proceeding, as well as representative charts, graphs, schematics and diagrams, animations, and models based on those documents and information, to support and to explain my testimony.

21. My opinions are based in part on a review and analysis of the above-mentioned documents and materials. I have also drawn on my education, experience, and knowledge of basic engineering and scientific principles in forming my opinions.

V. UNDERSTANDING OF THE LAW

A. Legal Standards

22. I am not an attorney, but I have been informed of several legal principles, which I have employed when forming my opinions in this declaration. I have been informed and understand that each patent claim is considered separately for purposes of validity and that a dependent claim that depends from another claim includes all of the limitations of the claim it depends from.

23. ***Claim Construction.*** I have been informed and understand that the claims of the challenged patents in this proceeding are to be construed using the same claim construction standard that is applied in district court. I have been informed and understand the claim construction analysis begins with the ordinary meaning of a claim term, and there is a presumption that the term carries its plain and ordinary meaning to persons of ordinary skill in the art as of the effective filing date of the patent. I have also been informed and understand that the most important sources for determining the meaning of a claim term are the claims, the specification, and the prosecution history of the patent at issue, which collectively is called “intrinsic evidence.” I have been further informed and understand that the meaning of a claim term may also be guided by “extrinsic evidence,” such as contemporaneous dictionaries and treatises.

24. ***Burden of Proof.*** I have been informed and understand that the

petitioner in an *inter partes* review bears the burden of establishing invalidity by “a preponderance of the evidence.” I have been further informed and understand that, to prove an assertion by “a preponderance of the evidence,” the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

25. **Obviousness.** I have been informed and understand that a patent claim is invalid if it would have been obvious to a person of ordinary skill in the art at the time of the claimed invention. I have been further informed and understand that a claimed invention is not patentable if differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. I have been informed and understand that factors relevant to the determination of obviousness include the scope and content of the prior art, the level of ordinary skill in the art at the time of the invention, differences between the claimed invention and the prior art, and “secondary considerations” or objective indicia of non-obviousness.

26. I have been informed that a single reference alone can render a patent claim obvious, if any differences between the reference and the claim would have been known or obvious to a person of ordinary skill in the art (“POSITA”) at the time of the invention. That is, if the POSITA could have adapted the reference to

meet the claims of the patent by applying known concepts to achieve the expected results, then the patent claims are rendered obvious by that reference.

27. I have been informed and understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have been further informed and understand that when a patent claim simply arranges old elements, with each performing the same function it had been known to perform, and yields no more than one of ordinary skill would expect from such an arrangement, the combination is obvious.

28. I have been informed and understand that a patent claim composed of several limitations is not obvious merely because each limitation was independently known in the prior art. Hindsight reasoning is not an appropriate basis for combining references to form an obviousness combination. I have been further informed and understand that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references.

29. I have been informed that various “secondary considerations” (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations must be considered as part of an obviousness analysis. I have been informed that even strong evidence of secondary considerations may not be sufficient to rebut a strong

showing of obviousness. I have been informed that the patentee bears the burden of showing the existence and effect of secondary considerations of non-obviousness, after which the burden of coming forward with rebuttal evidence shifts to the party arguing obviousness. I have been informed that the following secondary considerations may indicate non-obviousness:

- Copying: evidence that others, including the accused infringer, copied the patented invention.
- Long-standing problem or need: evidence of a persistent problem or need in the art that was resolved by the patented invention.
- Prior failure: evidence that others have tried and failed to solve the problem or failed to provide the need resolved by the claimed invention.
- Commercial acquiescence of competitors: the willingness of industry to license the patent at issue.
- Skepticism: evidence that those of ordinary skill in the art were skeptical as to the merits of the invention.
- Praise: evidence of praise directed to an invention by others in the field.
- Unexpected results: evidence that those of ordinary skill in the art were surprised by the capabilities of the claimed invention.

30. I have also been informed that the near-simultaneous invention by others can be evidence that a claimed invention is obvious. I have further been

informed and understand that the patentee bears the burden of showing a “nexus” between the claimed invention and the evidence proffered on secondary considerations (*e.g.*, proof of commercial success of a product that practices the claimed invention is not enough; there must be evidence that the commercial success resulted, at least in part, from the claimed invention).

B. Priority Date

31. I have been informed and understand that a U.S. patent may claim “priority” to the filing date of one or more earlier filed applications. I have been informed that the priority date, also called the “effective filing date,” is the earliest filing date to which a claim is entitled and that such date is relevant for determining what qualifies as prior art. I understand that a claim must have written description support in the application(s) to which it claims priority to be entitled to an earlier effective filing date. I have been informed that the priority date determination is done on a claim-by-claim basis and that claims in the same patent may have different priority dates.

32. I understand that when a U.S. patent or application is invoked as prior art, its effective filing date may be deemed to be the filing date of a related foreign application when said related foreign applications discloses the same subject matter as said U.S. patent or application, and that a related U.S. application was filed within a year of the foreign application. I understand for post-AIA patents,

like the '025 patent at issue here, whether the claims of the prior art reference are actually entitled to claim priority to the related foreign application is not relevant to this inquiry.

C. Level of Skill in the Art

33. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art may have for combining references.

34. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art is also a person of ordinary creativity.

35. In light of these factors, I have developed an opinion on the appropriate level of ordinary skill in the art that I have applied in my analysis set forth in this declaration. As explained, the challenged patent pertains generally to the fields of displays and touch panels. A POSITA at the time of the alleged invention would have had at least a bachelor's degree in electrical engineering,

physics, or a similar discipline, along with 2-3 years of display and touch panel technology experience. Relevant experience can substitute for education and *vice versa*. I was, at all relevant times, at least a POSITA in the art relevant to the challenged patents.

36. While it is my opinion that the above stated level of ordinary skill in the art is correct, my opinions set forth herein may remain unchanged under a different articulation of the level of ordinary skill in the art. I reserve the right to explain how, if at all, my opinions would differ if the Patent Owner alleges that a different level of ordinary skill in the art should apply.

VI. SUMMARY OF OPINIONS

37. I have been asked to compare various prior art references to Claims 1-6, 8-11, 14, 17, and 18 of the '025 patent (the "Challenged Claims"). In my opinion, the Challenged Claims are all unpatentable as obvious – based on these prior art references, combined with the knowledge of a POSITA.

38. My substantive analysis in Section X provides examples of why these prior art references render the Challenged Claims unpatentable. I reserve the right to cite and rely on additional portions of these references in any future declarations or depositions.

VII. TECHNOLOGY BACKGROUND

39. Before considering the '025 patent in detail, some background on the

technology of the '025 patent should be considered. Specifically, display device having both a touch function and a display function were well established by September 2019, building on the decades-old understanding of such panels and their core components.

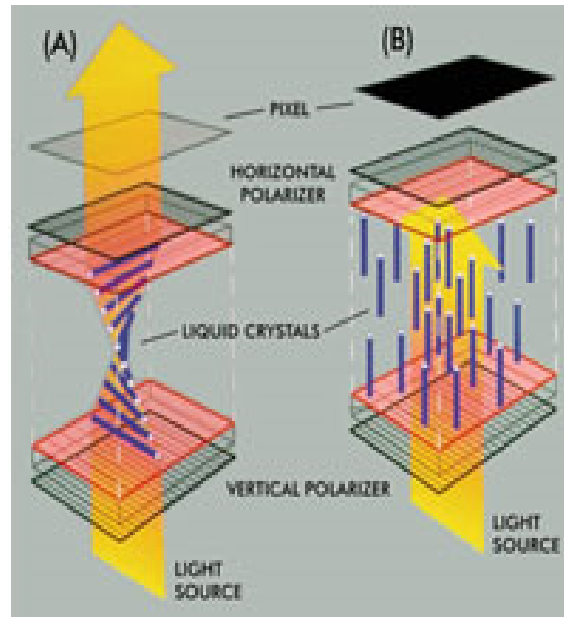
A. Active Matrix Liquid Crystal Displays

40. The fundamental design and components of active matrix liquid crystal displays, including those recited by the '025 patent, have been known for decades. For example, a patent covering the conventional design for a liquid crystal matrix display, with pixels, transistors, horizontal gate lines and vertical data lines that worked substantially as described below issued in 1974. *See* Ex. 1010 at, *e.g.*, claim 4.

41. In the 1990s, flat panel liquid crystal displays (LCDs) began emerging as the display technology to supplant the legacy cathode ray tube displays that had been used in most commercial and consumer applications. Most LCD monitors and televisions today use what is known as an “Active Matrix Liquid Crystal Display” (AMLCD) which uses Thin Film Transistors (TFTs). Typical AMLCDs comprise an array of pixels, a common electrode that overlaps the entire array of pixels, and a back light. Each pixel can further comprise color sub-pixels, usually including red, green, and blue filters. The specific color perceived by the human eye (including white) is determined by the proportions of red, green and blue light

transmitted by each pixel.

42. At each sub-pixel is a sample and hold circuit, addressed by a thin film transistor, wherein the voltage across the liquid crystal material is carried by a pixel electrode and held by a storage capacitor. Each subpixel acts like a variable shutter, allowing a controllable level of light from to backlight to pass through the color sub-pixel based on the voltage of a pixel electrode across the liquid crystal material. For example, in the figure below, on the left there is no voltage and all light is allowed to pass. On the right, full voltage is applied, and no light is allowed to pass. At intermediate voltages, an intermediate level of light is allowed to pass. The common electrode overlapping all of the pixels maintains a common voltage, and thus sets the “default” position for the liquid crystals of each sub-pixel, and the “default” voltage from which the data voltage of the pixel electrodes deviates to act on the liquid crystals.



43. In an AMLCD, the way these pixel voltages are individually controlled throughout an array of potentially several thousands of pixels is through the synchronized operation of a gate driver (sometimes called a row driver) and a data driver (sometimes called a column driver). As a somewhat simplified summary, to provide the correct voltage to a particular sub-pixel (so as to cause it to display the proper amount of light through the color filter needed to display the desired image), the gate driver sends a gate signal as a pulse across a single horizontally oriented gate line (sometimes called a row line, scan line, address line or select line) to “turn on” each of the pixel transistors in that given row, thereby enabling the transistor to allow data voltages to reach those transistors’ pixel electrodes. At the same time, the data driver supplies voltages through the plurality of vertically oriented data lines (sometimes called column lines or signal

lines) to set the particular voltage programmed for each of the particular pixel electrodes in the currently active row, thus setting the particular levels of light allowed to pass through each pixel. This, in turn, determines the color that is displayed to the human eye. Because the gate signal pulse only activates one row of transistors at a time, this data signal has no influence on the other rows and provides voltages only to the active row.

44. This process, which takes microseconds per row, cycles sequentially through all the gate lines, constantly refreshing each row of pixels with new data voltages to govern the amount of light that passes through each pixel. *See generally* Ex. 1011 (Willem den Boer, *Active Matrix Liquid Crystal Displays* (2005)), pp. 45-48. The amount of time it takes to fully cycle through all the rows and provide data voltages to every pixel on every row of gate lines is called a frame. So when a display runs at 60 frames per second (*i.e.*, has a refresh rate of 60Hz), it means that every row of pixels on the display will be provided data voltages in this way 60 times in a second.

45. A circuit diagram reflecting this fundamental aspect of active matrix LCD design is provided below:

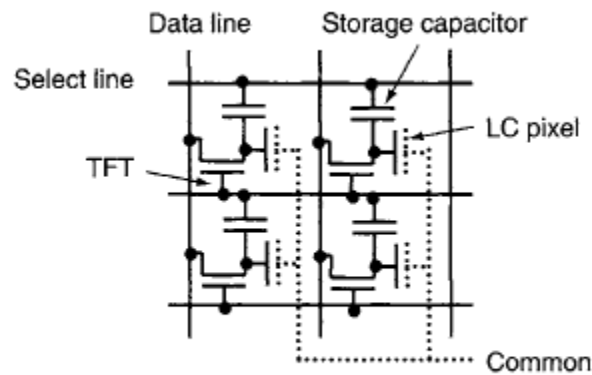


Figure 2.3: Circuit diagram for four pixels in an active matrix LCD.

Ex. 1011, p. 32, Fig. 2.3 (showing a circuit diagram reflecting this arrangement and referring to gate lines as “select lines”).

46. While the general components and fundamental design of AMLCDs have been well known for decades, there are different types of AMLCDs that vary from one another in their arrangement and use of these conventional components. For example, Fringe Field Switching (FFS) is a type of LCD panel technology that allows for wider viewing angles and improved image quality as compared to prior art LCD panels. These panels use an “in plane” structure designed to keep the liquid crystals parallel to the plane of the display surface. In these panels, both the pixel electrodes and the common electrodes (and/or touch electrodes, as discussed below) are on the same substrate, with the liquid crystal layer positioned above, closer to the surface of the display.

B. Capacitive Touch Screen Technology

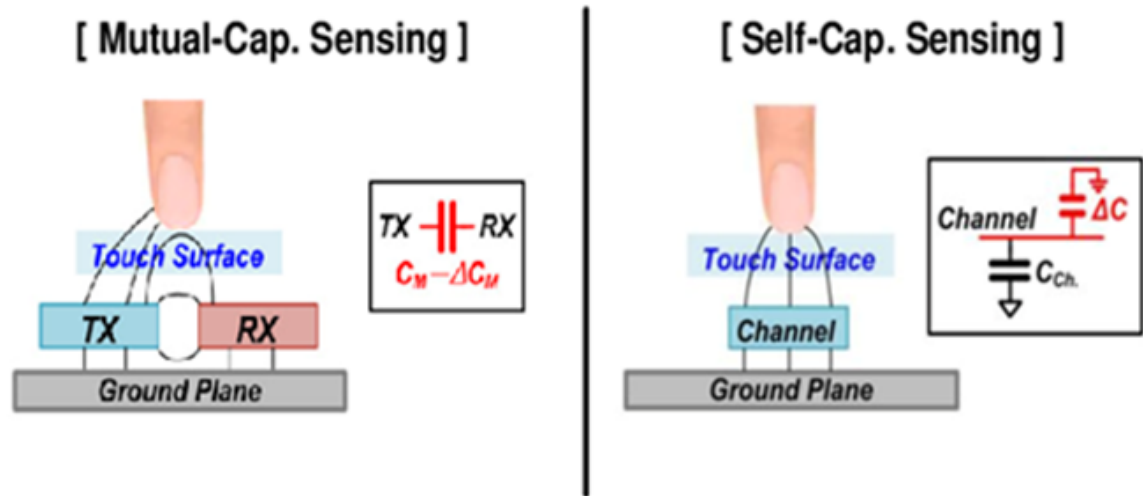
47. By the mid-2000s, LCD panel displays that served as touch screens

were in widespread use. “TFT LCDs with touch screens have become popular in displays for industrial and retail applications, as well as in PDAs, smart phones, and tablet PC products. They allow easy and fast access to computer information with a more interactive approach than a mouse or a touch pad. Touch panels use ‘soft-buttons’ that can be easily reconfigured with software. Therefore, they give an integrated solution with more design flexibility than a display with a separate keypad or keyboard.” Ex. 1011, p. 192.

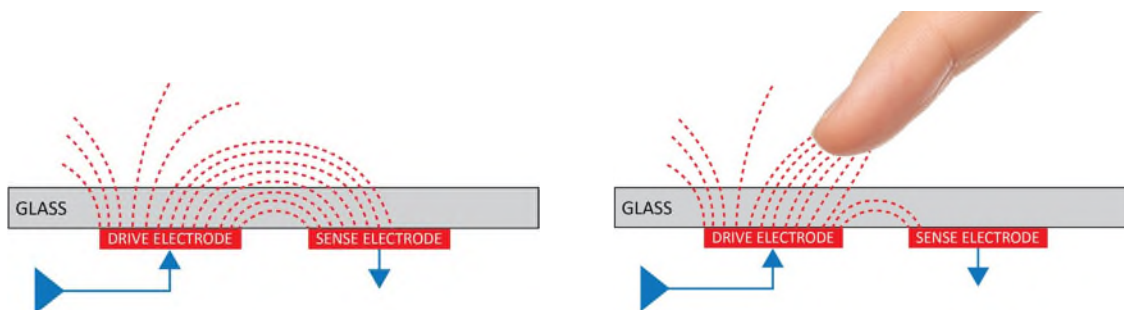
48. While various touch screen technologies exist, the use of capacitive touch screen technology has become dominant today. A capacitive touch system can be designed to detect and report a two-dimensional coordinate (*e.g.*, x, y position) identifying the location of the user’s finger or stylus. When a finger touches a capacitive touch sensor, it changes the capacitive coupling of the sensor near the touch. This effect is commonly referred to as a change in capacitance within the touch screen at the location of the touch. A touch controller, microprocessor, or other related application-specific integrated circuit (“ASIC”) may be used to measure this electrical effect and process the resulting information to determine the position of the touch on the screen.

49. There are two basic forms of capacitance touch screens: self-capacitance panels which detect a capacitance change between a sense electrode and ground, and mutual capacitance panels which sense a capacitance change

between two electrodes. These different approaches are illustrated in the following two figures:



As a finger touch interacts with the electric field of the touch electrodes, the amount of capacitance is changed. Conceptually, when a finger comes near a capacitive node, it effectively “steals” charge from the electrode, which reduces the capacitance of the node in a measurable way, as depicted below:



C. In-Cell Touch Panels

50. There are generally three type of touch panel, (1) In-Cell, (2) On-cell and (3) On-Glass-Solution. They differ primarily with regard to where the touch

sensors are positioned relative to the display substrate. A display typically includes a transistor substate at the bottom, followed by the liquid crystal layer, and then the color filter substrate. In an In-Cell touch panel, the touch sensors are included in and among those three layers. The '025 patent and the references discussed in this Declaration all relate to a particular type of touch panel known as an “in-cell” touch panel.

51. In in-cell panels, the common electrode that traditionally overlapped the array of pixels to set a common “default” voltage has been modified to also serve as the touch sensing electrodes, essentially performing double duty. Specifically, in-cell touch panels are implemented with the unitary common electrode divided into multiple separate common electrodes, with each held at the traditional constant potential to provide a “default” voltage to the pixels until a touch signal is sent to determine if the individual common electrode portion is touched. This interrogation time is usually brief compared to the frame time and may be within a blanking period (*i.e.*, a period when the pixels at issue are not activated by a gate signal).

D. Incremental Improvements to In-Cell Touch Panel Design

52. By the earliest 2019 priority date of the '025 patent, the above-discussed core components and design of in-cell touch panel displays were well known. Indeed, the '025 patent itself admits that such panels with “a plurality of

gate lines extending in the row direction, a plurality of data lines extending in the column direction, a pixel electrode provided in each of the plurality of pixels, a plurality of common electrodes (counter electrodes) provided facing the plurality of pixel electrodes, and signal lines connected to the common electrodes as touch lines” that could “sense the touch position” based on a “change in capacitance” were prior art. ’025 patent, 1:40-53. Similarly, all prior art discussed in the petition and this declaration describes such a touch panel having these same conventional attributes.

53. Further, by the earliest asserted 2019 priority date, several improvements to this conventional in-cell touch panel had already been invented, described, and patented by those in the touch panel industry, including those described in the prior art references discussed in this declaration.

VIII. THE ’025 PATENT

54. U.S. Patent No. 11,126,025 (the “’025 patent”) is entitled “In-cell Touch Panel.” The ’025 patent claims priority to foreign applications, JP2019-035692 and JP2019-035902, both of which were filed on February 28, 2019.

55. The ’025 patent is related to “in-cell” LCD panels, which are touch panels with touch-detecting functionality integrated directly into the liquid crystal display itself. ’025 patent, 1:32-37. As I have just discussed, according to the ’025 patent, the prior art in this area included panels with “a plurality of gate lines

extending in the row direction, a plurality of data lines extending in the column direction, a pixel electrode provided in each of the plurality of pixels, a plurality of common electrodes (counter electrodes) provided facing the plurality of pixel electrodes, and signal lines connected to the common electrodes as touch lines.” ’025 patent, 1:40-47.

A. Problem Addressed by the ’025 Patent and the Alleged Invention

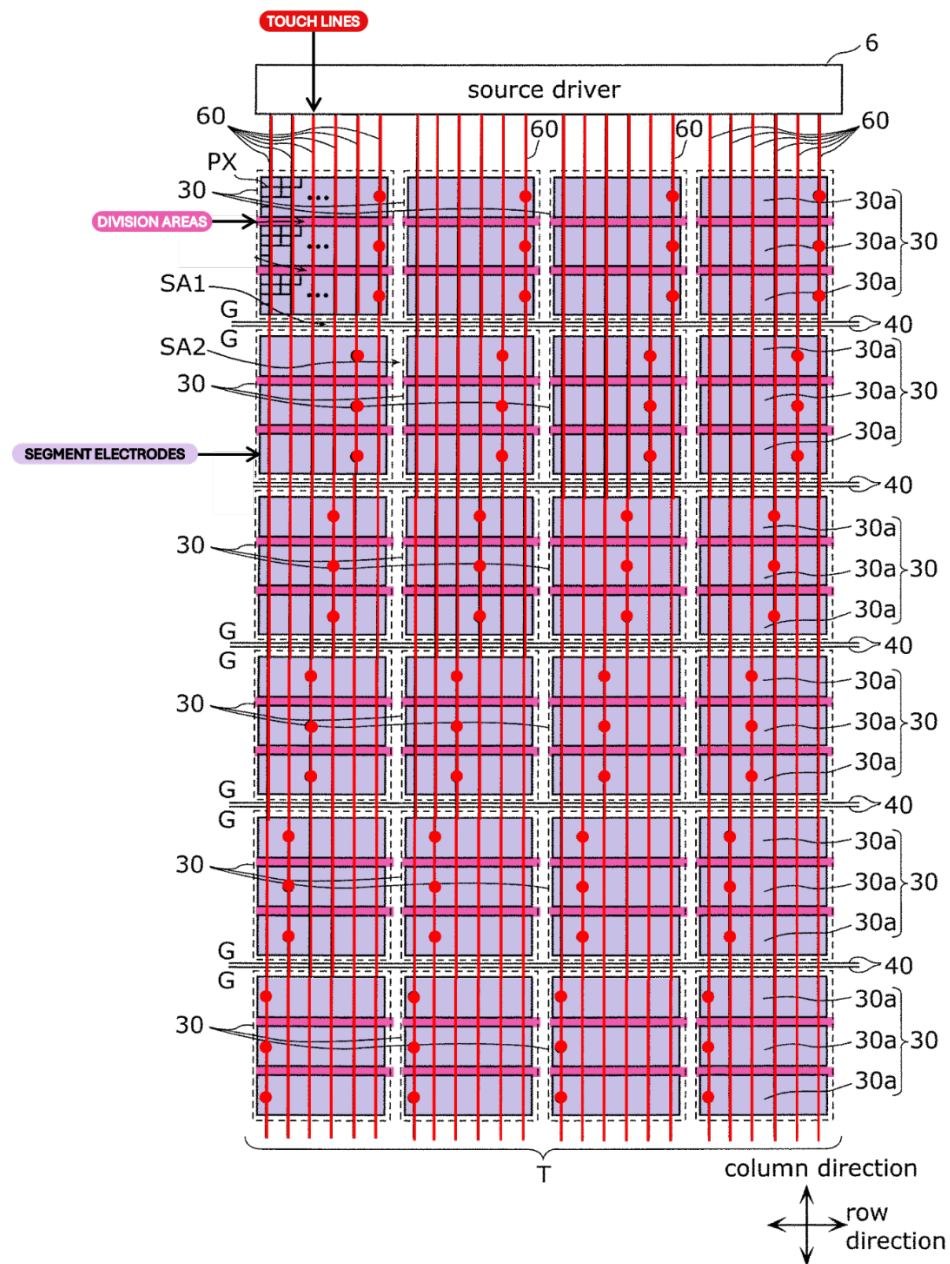
56. The ’025 patent purports to have recognized and addressed two main problems with these conventional in-cell touch panels.

57. The first problem is that when common electrodes (*i.e.*, touch electrodes) span several pixels, they overlap with the gate lines between pixel rows, which the ’025 patent explains, somewhat vaguely, can lead to capacitance imbalances that can negatively affect image quality. ’025 patent, 1:65-2:13. To address this, the ’025 patent proposes dividing each common electrode into several smaller segment electrodes, allowing gate lines to pass between these segments so as to prevent the distortion caused by coupling capacitances between the gate line and the common electrode. ’025 patent, 2:46-53; 16:48-56. Additionally, the segment electrodes forming a single common electrode can be interconnected with bridge lines, allowing them to act as a single common electrode while still minimizing the capacitance differences between the gate lines and the common electrode. ’025 patent, 17:16-47 (explaining that the bridge line is a preferable

alternative to connecting segment electrodes using bridge portions of the segment electrodes themselves).

58. As reproduced and annotated below, Figure 3 of the patent illustrates an embodiment showing common electrodes 30, each divided into three segment electrodes 30a (annotated Figure 3, purple). Each common electrode 30 is linked to a specific touch line 60 (annotated Figure 3, red), connecting all segment electrodes 30a within the common electrode. The Division Areas (“DA”) (annotated Figure 3, pink) separate the segment electrodes within each common electrode, and although not shown in Figure 3, the ’025 patent states that gate lines are present in DAs between segment electrodes. ’025 patent, 11:19-30; 7:20-23.

FIG.3



'025 patent, Fig. 3.¹

¹ All figures appearing throughout this declaration are annotated with labels and colors to help illustrate my opinions.

59. The '025 patent also describes “first bridge lines 80” which “extend[] in the column direction so as to overlap with each of the plurality of segment electrodes 30a included in one common electrode 30, and is connected to each of the plurality of segment electrodes 30a included in the concerned one common electrode 30.” '025 patent, 18:57-63.²

60. As explained above, by the time the '025 patent was filed in 2019, these capacitance distortion problems had already been observed, and the solution of not covering the gate line with common electrodes had already been described in Kim II—in much more detail than it is described in the '025 patent—as a solution. Kim II at [0013]-[0016], [0047]-[0048], [0088], [0092] (discussing problems caused by capacitance-related voltage distortion in the gate electrodes of the transistor and gate line). Like the '025 patent, Kim II leverages common electrodes that are subdivided into segments—separate rows of common voltage electrodes—with the gate lines routed through the gaps between these common

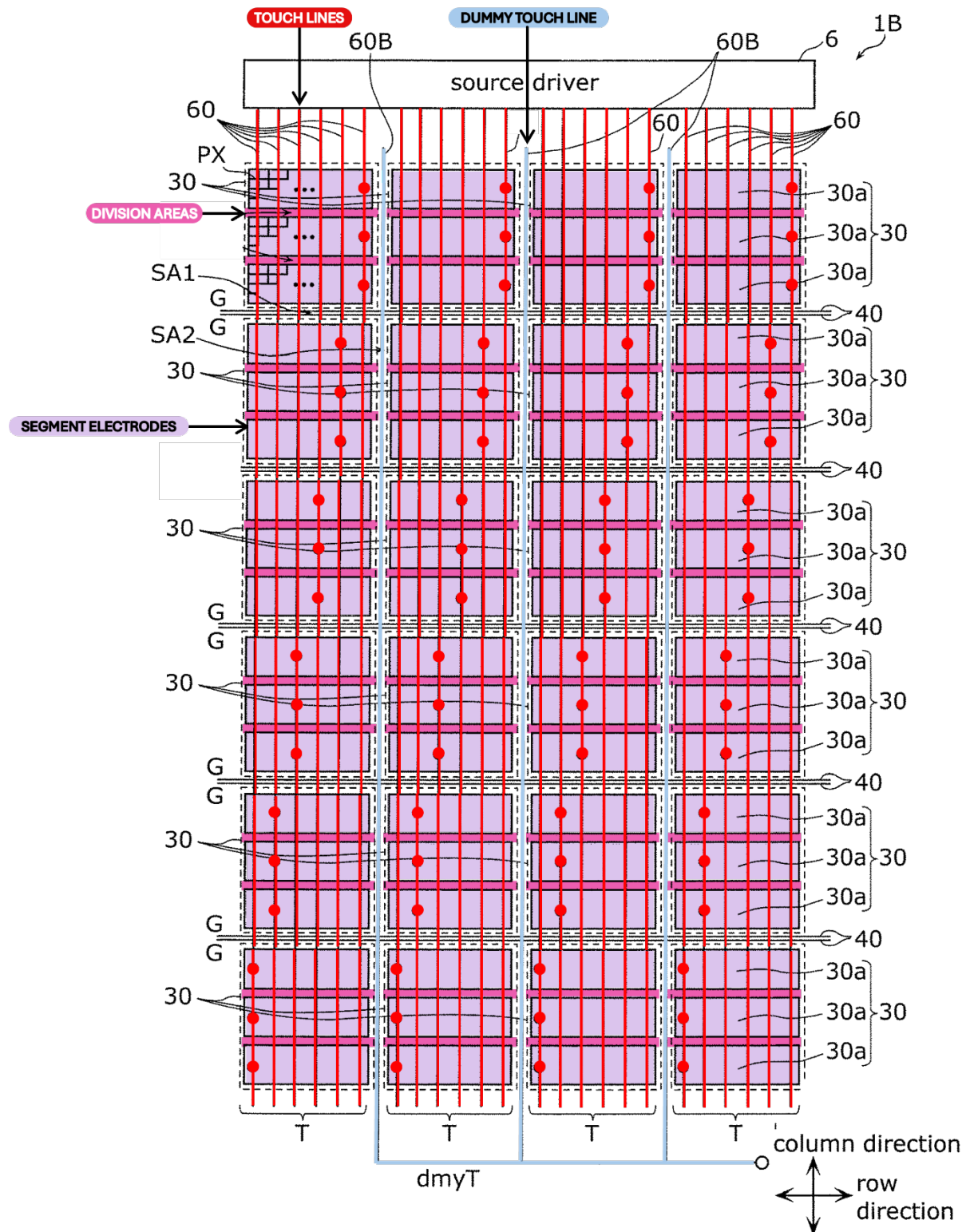
² Figure 12 purports to depict the first bridge lines 80, but appears to include a draftsman's error such that it does not match the description of those first bridge lines in the '025 patent. Specifically, Figure 12 depicts first bridge lines 80 as spanning a single segment electrode while connecting in multiple places on a particular segment electrode, which is not how the bridge lines are ever described in the '025 patent. The bridge lines are instead described as spanning the division areas between segment electrodes within a common electrode, not connecting different points within the same single segment electrode.

voltage electrode rows. Kim II at [0018]-[0020], claims 5, 14. This configuration positioned the gate line within the separation spaces, and “[b]y positioning the separation space 510 on the gate line GL, a capacitance of the gate electrode 518 may be decreased and the transistor TR may be driven at an increased speed,” thereby preventing the potential display defects caused by the differing gate electrode capacitances. Kim II at [0090].

61. Further, like the ’025 patent, Kim also taught that these divided segments could be connected together with connecting lines to reduce the internal load deviation between common electrodes. Kim at [0120].

62. The second problem identified by the ’025 patent involves the data line being situated in the gap between two common electrodes. Such positioning of the data line can create an electric field that unintentionally rotates the liquid crystal in the display, leading to image quality degradation (’025 patent, 2:18-31). The patent’s solution is to add a dummy touch line above the data line in this separation area, which acts as a shield to prevent the data line’s electric field from affecting the liquid crystals. ’025 patent, 2:54-3:9; 22:10-14. These dummy touch lines 60B are illustrated in Figure 14 (blue) of the patent, as reproduced and annotated below.

FIG.14



'025 patent, Fig. 14.

B. Prosecution History of the '025 Patent

63. The '025 patent was prosecuted in the United States as Application No. 16/784,806 ("'806 Application") and claims priority to foreign applications JP2019-035692 and JP2019-035902.

64. The '806 Application was filed on February 7, 2020. The application, as filed, included 20 claims. Ex. 1002 at 107-111 (U.S. Patent Application Publication No. 2020/0278571 A1, Claims 1-20). Claim 1, as originally filed, omitted the claimed "bridge lines" as an element. *Id.* Dependent Claims 2 and 10, as originally filed, recited limitations related to the bridge lines. *Id.*

65. On March 3, 2021, the Examiner issued a non-final rejection. Pending claim 20 (later issued as claim 18) was allowed, and the Examiner noted that claims 9 through 19 would also be allowable if they were rewritten as independent claims. Ex. 1002 at 227 (*Office Action*, dated March 3, 2021). Claim 1 was rejected as obvious based on a combination of U.S. Patent Application Publication No. 2019/0196638 to Tominaga, U.S. Patent Application Publication No. 2008/0068516 to Mori, and claims 2–8 were rejected on similar grounds, with an additional reference to U.S. Patent Application Publication No. 2018/0120997 to Moon. *Id.* at 229, 231.

66. In response, the applicant cancelled pending claims 2 and 10 and

incorporated their limitations into claim 1. Ex. 1002 at 255 (*Office Action Response*, dated June 1, 2021). The applicant also amended pending claim 12 (later issued as claim 10) to make it an independent claim. *Id.* This new claim included the content of the original claim 1 (without bridge line limitations) and added the dummy touch line limitations. *Id.* at 252. The applicant did not make any substantive arguments against the rejections. *See id.* at 255.

67. The Examiner allowed the claims on June 11, 2021, and the '025 patent was issued on September 21, 2021. Ex. 1002 at 260-61 (*Notice of Allowance*, dated June 11, 2021); '025 patent, 1:45.

C. Claim Construction

68. In my opinion, the claims of the '025 patent can be interpreted according to their plain and ordinary meaning as understood by a POSITA, taking into account the context provided by the claims, specification, and prosecution history of record, for the purpose of this IPR.

69. In order to construe the claims, I have reviewed the '025 patent and its prosecution history. Consistent with these standards, I propose the following interpretation.

1. “dummy touch line”

70. With respect to the term “dummy touch line,” which appears in Challenged Claims 10-11, 14, 17, 18, the claims specify certain requirements about

the placement and orientation of the dummy touch line, as well as what it must not be connected to. However, the claims do not require the dummy touch line to perform any particular function, nor do they explain how to determine whether a given line qualifies as a “dummy touch line.” In my opinion, this lack of context necessitates construing the term. Based on my review of the ’025 patent and its prosecution history, I believe that “dummy touch line” should be interpreted as “a line that does not carry a touch signal.”

71. Furthermore, from the perspective of a POSITA, the term “dummy” in “dummy touch line” indicates that the line is similar in form to a touch line but does not actually perform the function of carrying a touch signal; in other words, it is a non-functional or imitation touch line. This interpretation aligns with the ordinary meaning of “dummy” in technical contexts, where it denotes something that is a replica or stand-in but not operational. Ex. 1013 (*Wiley Electrical and Electronics Engineering Dictionary* (2004)) at 3 (defining “dummy” as “[a] non-operational component, device, or piece of equipment which can be connected or installed as if it were a working component, device, or piece of equipment”). The ’025 patent’s specification supports this understanding, explicitly stating that the “dummy touch line 60B” “does not contribute to detection of a touch position.” ’025 patent, 19:39-43; 20:5-6.

72. Based on the discussion above, it is my opinion that the term “dummy

touch line” should be construed to mean “a line that does not carry a touch signal.”

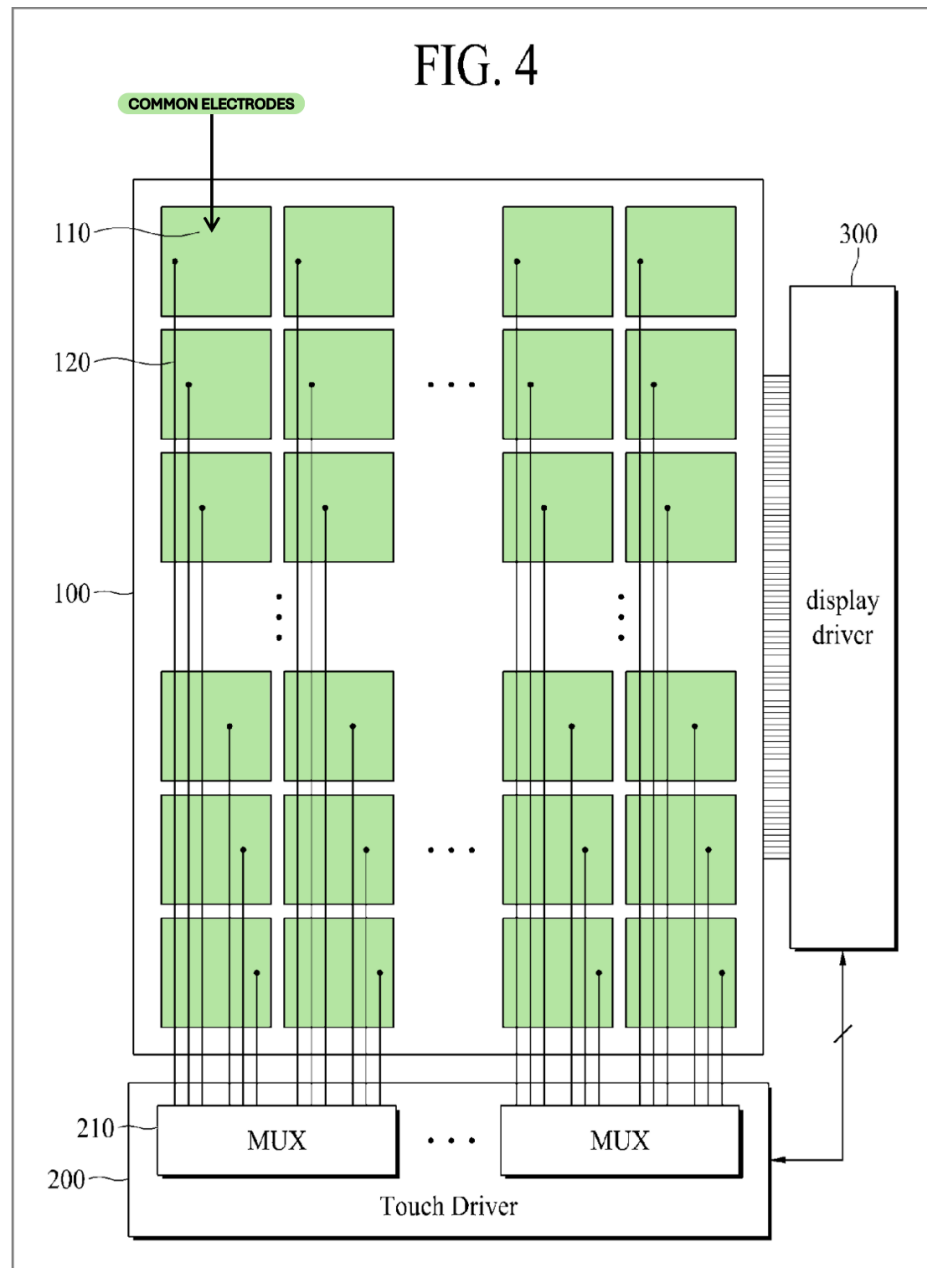
IX. THE PRIOR ART REFERENCES

A. Kim

73. Kim, titled “Touch Display Apparatus,” was published on August 4, 2016, filed on December 30, 2015, and claims priority to two Korean patent applications filed in 2015. Kim at (43), (22), (30).

74. Kim relates to an in-cell type “touch sensitive display apparatus.” Kim at Abstract. Kim describes an in-cell type touch-sensitive apparatus and identifies the issue of image quality degradation caused by load deviation in touch electrodes. Kim at [0017]-[0019]. Kim proposes addressing this problem through a revised design for touch panels that “reduces a load deviation of a touch electrode, thereby enhancing image quality.” Kim at [0023].

75. Kim discloses two embodiments, both of which modify the conventional touch panel structure that includes pixels, data lines, gate lines, common electrodes, and touch lines, as shown in Figure 4 below. See Kim at [0074] (pixels), [0075] (gate lines and data lines), [0076] (common electrodes) and [0078] (touch lines). Notably, in Kim’s second embodiment, each of the common touch electrodes (116a, 116b) is divided into multiple segment touch electrodes (ITO line). Kim at [0118].

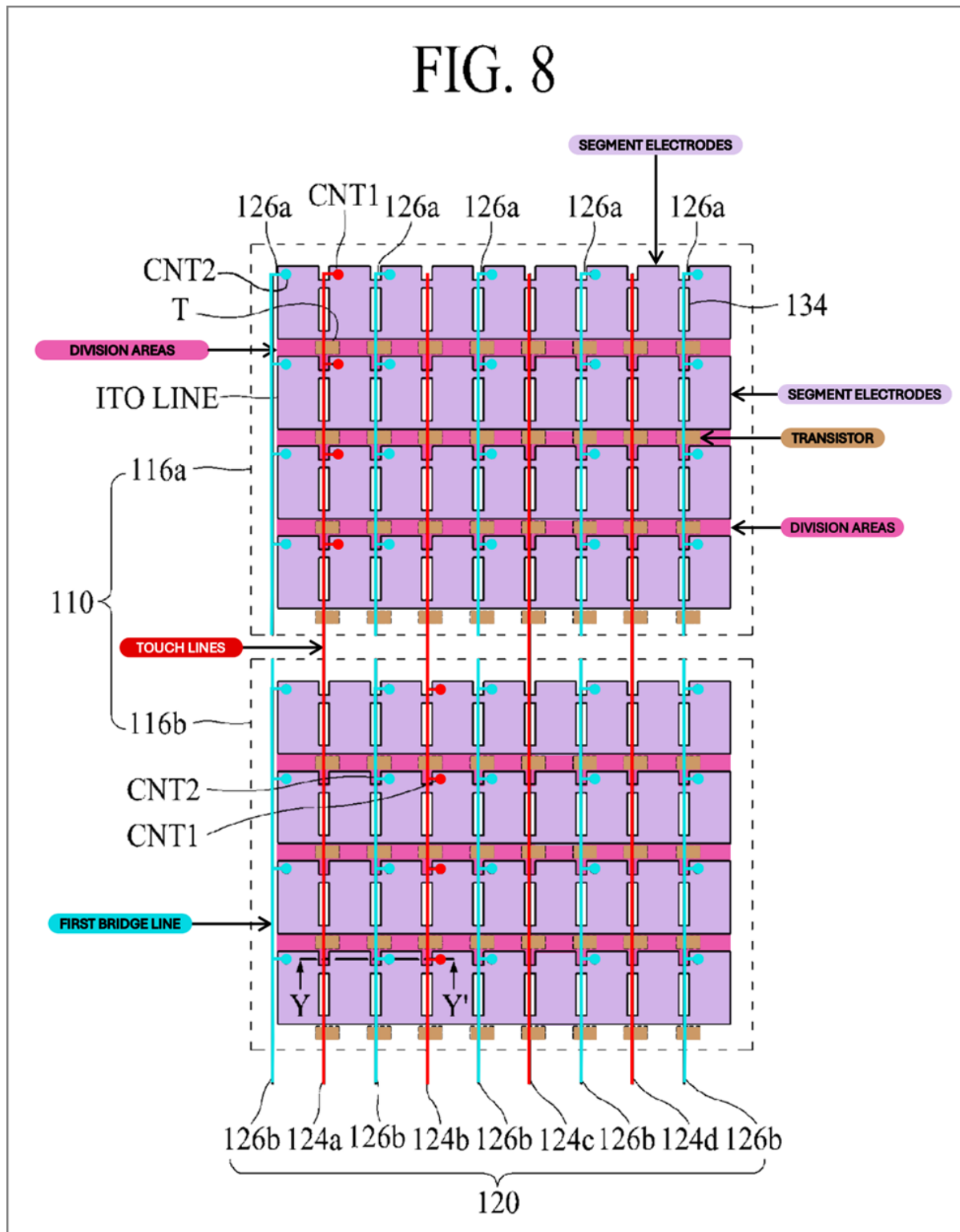


Kim, Fig. 4; *see also* Kim at [0074] (pixels), [0075] (gate lines and data lines), [0076] (common electrodes) and [0078] (touch lines).

76. Notably, in Kim's second embodiment, each of the common touch electrodes (116a, 116b) is divided into multiple segment touch electrodes (ITO

line). Kim at [0118]. Within a common touch electrode (116a, 116b), each of the segment touch electrodes (ITO Lines) are connected by connecting lines (126a), *i.e.*, bridge lines. *Id.*; Fig. 7, Fig. 8.

77. Kim's second embodiment is depicted best in Figure 8, reproduced and annotated below. Figure 8 shows two common touch electrodes, which are comprised of four segment touch electrodes (purple; ITO lines) separated by gaps (pink; Division Areas D1) that overlap the thin film transistors (brown). Each common touch electrode is connected to a touch signal line, and the individual segment electrodes (ITO lines) within each common touch electrode are interconnected by connecting lines (cyan).



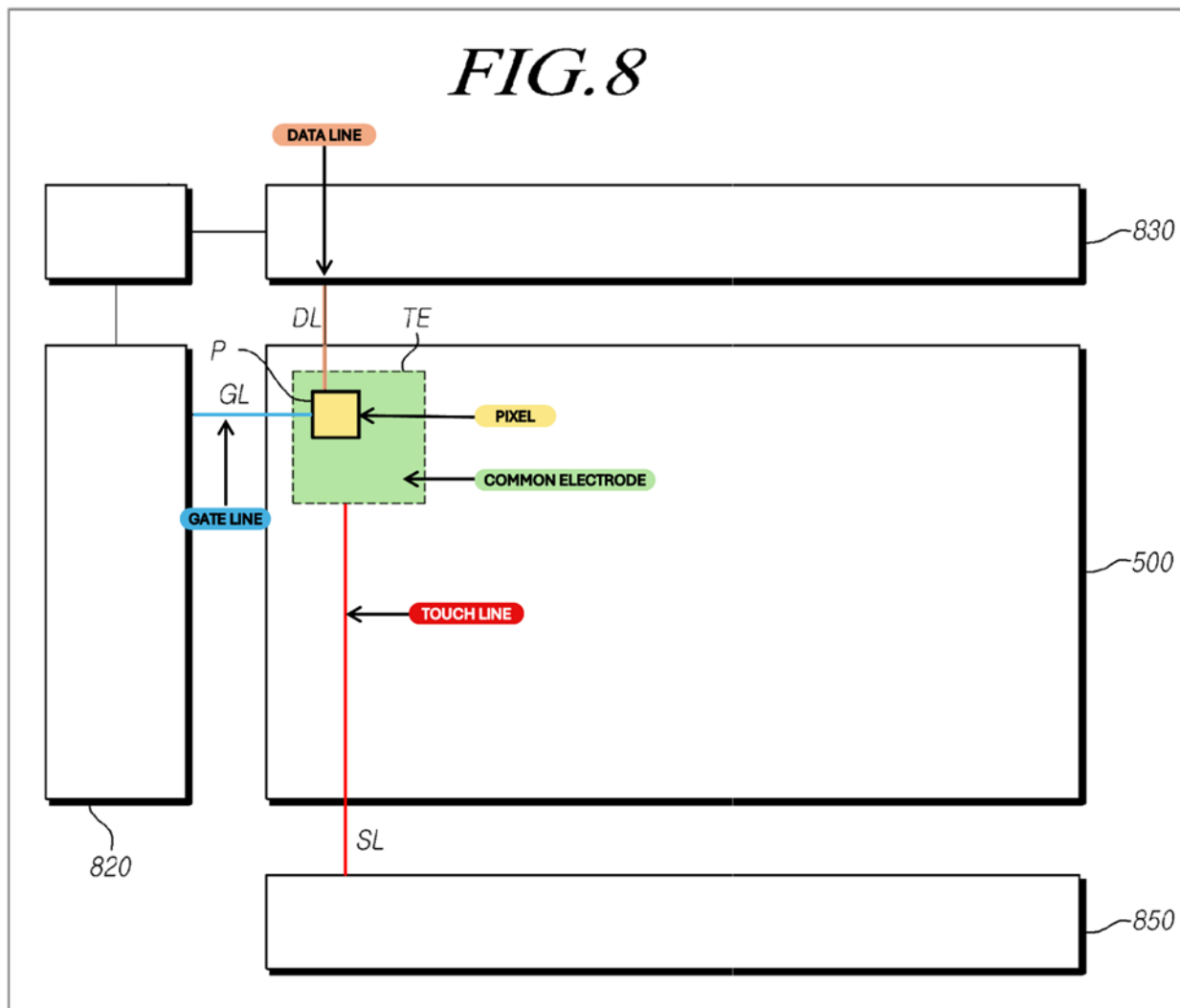
Kim, Fig. 8.

78. Thus, in my opinion, Kim identifies the same image quality problem as the '025 patent, and Kim solves it in the same way—by dividing common electrodes into segment electrodes and using connecting lines to link segment electrodes to reduce the load of the touch electrodes. Kim at [0118]. And like the '025 patent, Kim expressly states that this solution reduces internal load deviation and enhances image quality. *Id.* at [0131].

B. Kim II

79. Kim II, titled “Touch-Integrated Display Device,” was published on July 6, 2017, filed on December 13, 2016, and claims priority to a Korean patent application filed in 2015. Kim II at (43), (22), (30).

80. Kim II directly relates to in-cell touch panel technology, as it discusses “a touch-integrated display device in which a touch electrode is positioned inside a display panel.” Kim II at [0003]. Kim II details the conventional components of such a touch display panel, including pixels, gate lines, data lines, sensing lines (or touch lines), and touch electrodes (or common electrodes). Kim II at [0095]-[0102]. Figure 8 of Kim II is reproduced and annotated below for discussion.



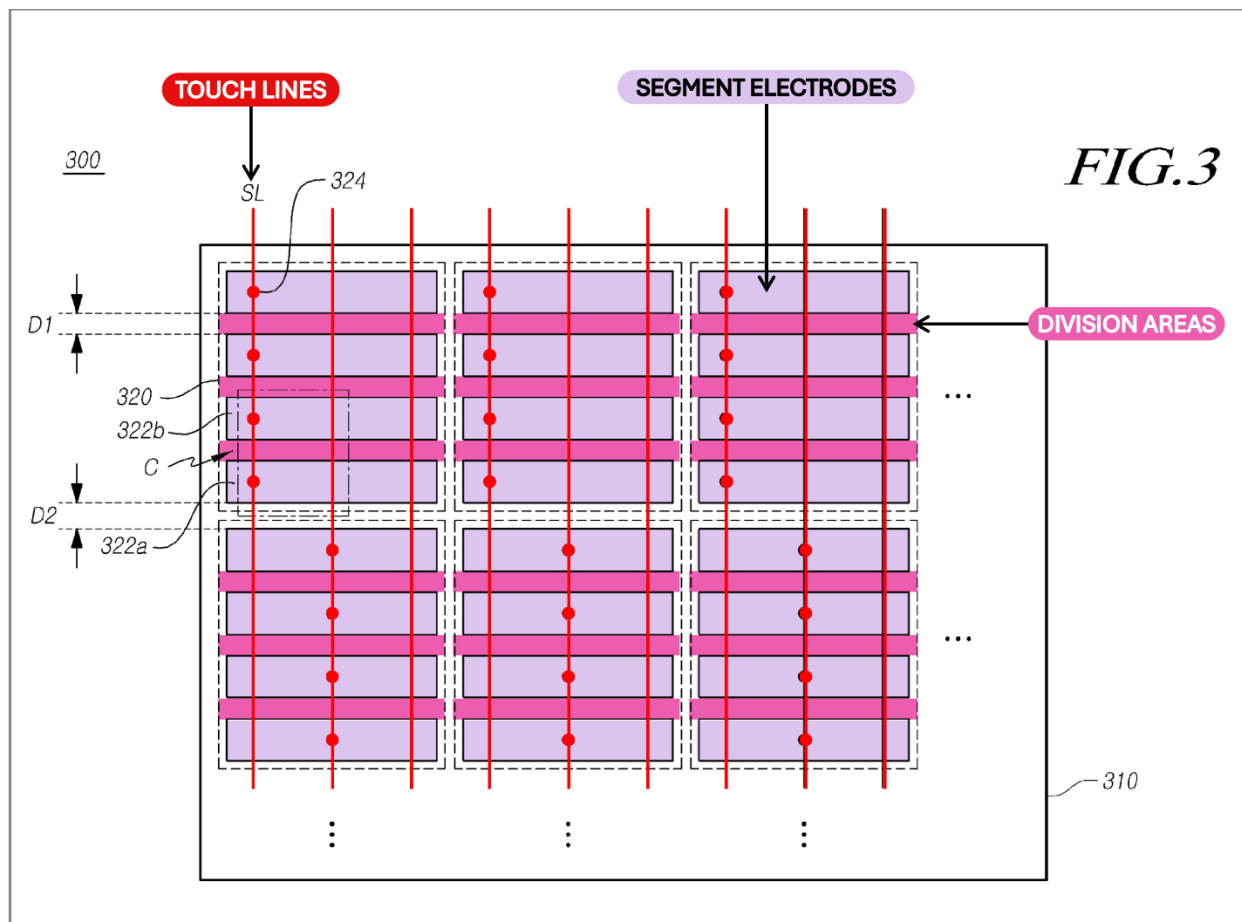
Kim II, Fig. 8.

81. Kim II acknowledges that in “conventional display panel[s],” a significant difference in capacitance between the gate lines and a large common electrode overlapping those gate lines can cause the capacitance of the gate electrodes to drop to a level that results in device failure and display defects. Kim II at [0016]-[0017]. Specifically, Kim II taught that, when a large common electrode covers multiple pixels, as is typical, transistors will experience a different

coupling capacitance based on where they are relative to the edge of the common electrode. Kim II at [0013]-[0016]. As a result of this, the gate-source voltage of the gate electrode, *i.e.*, the level of voltage needed to activate the transistor, is distorted, which can prevent the pixel electrodes from effectively receiving data voltages from the data line and lead the transistor to have a delayed response, resulting in display defects. *Id.* at [0016], [0047]-[0048].

82. Kim II describes a solution to these problems premised on its observation that “[t]he gate line GL and an electrode adjacent thereto greatly affect a capacitance of the gate electrode 518.” Kim II at [0090]. Accordingly, to resolve these problems, Kim II explains that common electrodes can be divided into sub-unit rows such that the separation space between those rows would fall on the gate line, leaving it uncovered. *Id.* Because the gate line is connected to the transistor gate electrode, positioning the gate lines in the separation area eliminates the varying capacitance of the gate electrodes based on their proximity to the edge of the common electrode, and allows them to have a more uniform capacitance, while simultaneously preventing the potential display problems caused by the gate-voltage distortion. *Id.* at [0089]-[0090]. As a result, the placement of the gate line in the separation area prevents the pixel transistor from being unable to transfer the correct data line voltage to the pixel electrode, and prevents the potential display problems. *Id.* at [0090].

83. In my view, Figure 3 of Kim II, reproduced and annotated below, effectively illustrates this concept. Figure 3 illustrates touch electrodes segmented into rows 322a, 322b (purple) with division areas between them, and further explains, particularly with regard to Figure 5, that the gate lines run through these gaps. Kim II at [0090]. Additionally, Figure 3 demonstrates that each touch electrode is connected to a specific sensing line (red).



Kim II, Fig. 3.

C. Yoshida

84. Yoshida, titled “Position Input Device,” was published on September 26, 2019, filed on March 13, 2019, and claims priority to Japanese Application JP2018-058356, which was filed on March 26, 2018. Yoshida at (43), (22), (30).

85. Because Yoshida claims priority to a foreign application, I have also reviewed a certified translation of Yoshida’s original Japanese application (“Translation”). In my opinion, that Japanese application discloses the same material that I rely on here for my opinions. In general, based on my review of the translation, the primary difference seems to be that, whereas Yoshida numbers each of the 13 sentences as their own paragraph in the “Description of the Drawings” section, the Translation groups them all into one paragraph. As a result, there is a paragraph numbering offset of 12 between the Translation and Yoshida, such that *e.g.*, paragraph [0030] of Yoshida corresponds to paragraph [0018] of the Translation. This also occurs at the very end of the disclosure, where Yoshida provides 25 enumerated paragraphs, each of which are treated as a separate paragraph in Yoshida (*see* [0068]-[0093], but which are all deemed to be paragraph [0056] of the Translation.

86. Based on my review, corresponding paragraphs in Yoshida and the Translation are identical in substance, with only minor word choice and syntax differences that I assume are due to the fact that Yoshida and the Translation are

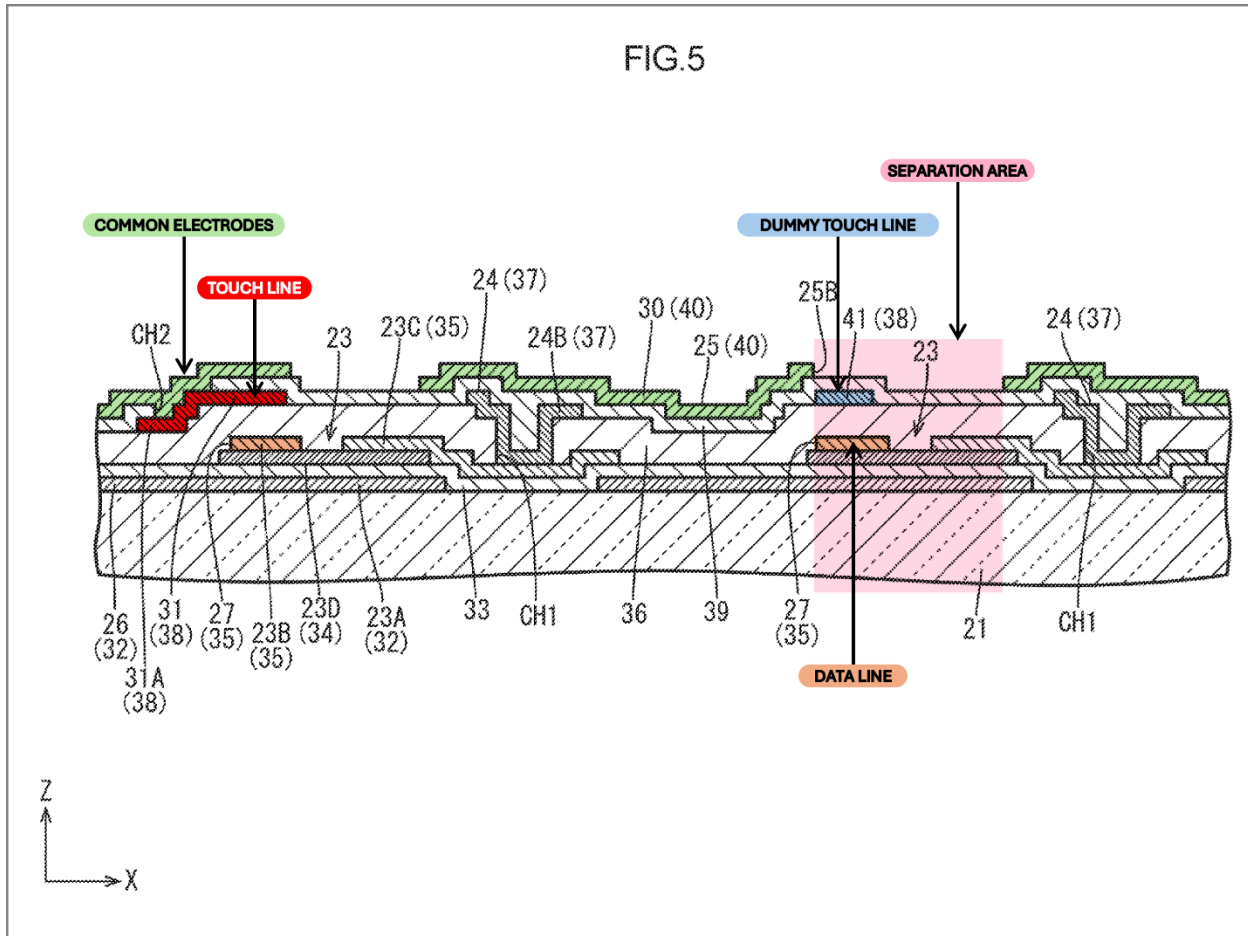
two different translations of the same underlying, original Japanese text. For example, the Translation may refer to components using different, but obviously synonymous, terms than those used, *e.g.*, “touch wiring” rather than “touch lines.” Further, the figures in both versions are the same.

87. In sum, the differences between Yoshida and the translation are immaterial word choice and syntax differences (likely caused by independent translation) and differing alignment of paragraph numbering. In light of this, it is my understanding that Yoshida is therefore entitled to claim priority to the filing date of the Japanese application.

88. Yoshida relates to an in-cell touch panel device using horizontal gate lines, vertical data lines, touch electrodes, and touch lines. Yoshida at [0028]; Translation at [0016]. Yoshida also describes “spare touch lines” that run parallel to the touchlines, but are disconnected from the touch electrodes in their default state. Yoshida at [0035]; Translation at [0023]. If a regular touch line becomes damaged or disconnected, the spare touch lines can be connected to a touch electrode to substitute for a damaged touch line. *Id.*

89. Similar to the dummy touchlines claimed in the '025 patent, Yoshida's spare touch lines can also be positioned in the gap (pink) between the common electrodes 30 (green), such that the spare touch lines overlap the source [data] line 27 (orange). Yoshida at [0035], [0038]; Translation at [0023], [0026].

Figure 5 of Yoshida, reproduced and annotated below, reflects this arrangement from a cross-sectional view.

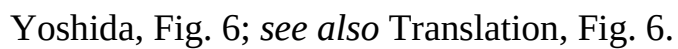


Yoshida, Fig. 5; *see also* Translation, Fig. 5.

90. In its third embodiment, Yoshida explains that these spare touch lines positioned between common electrodes can be supplied by a “terminal portion 55” with “the same common signal supplied to the common electrode.” *See* Yoshida at [0062], [0065]; Translation at [0050], [0053]. According to Yoshida, this configuration helps stabilize the area that would otherwise be exposed to potentially destabilizing electric fields between the common electrodes and pixel

electrodes. *Id.*

91. Additionally, Yoshida explains that some of its (blue) spare touch lines (*i.e.*, labeled as second bridge lines, below) can overlap the touch electrodes, as shown in Figure 6:



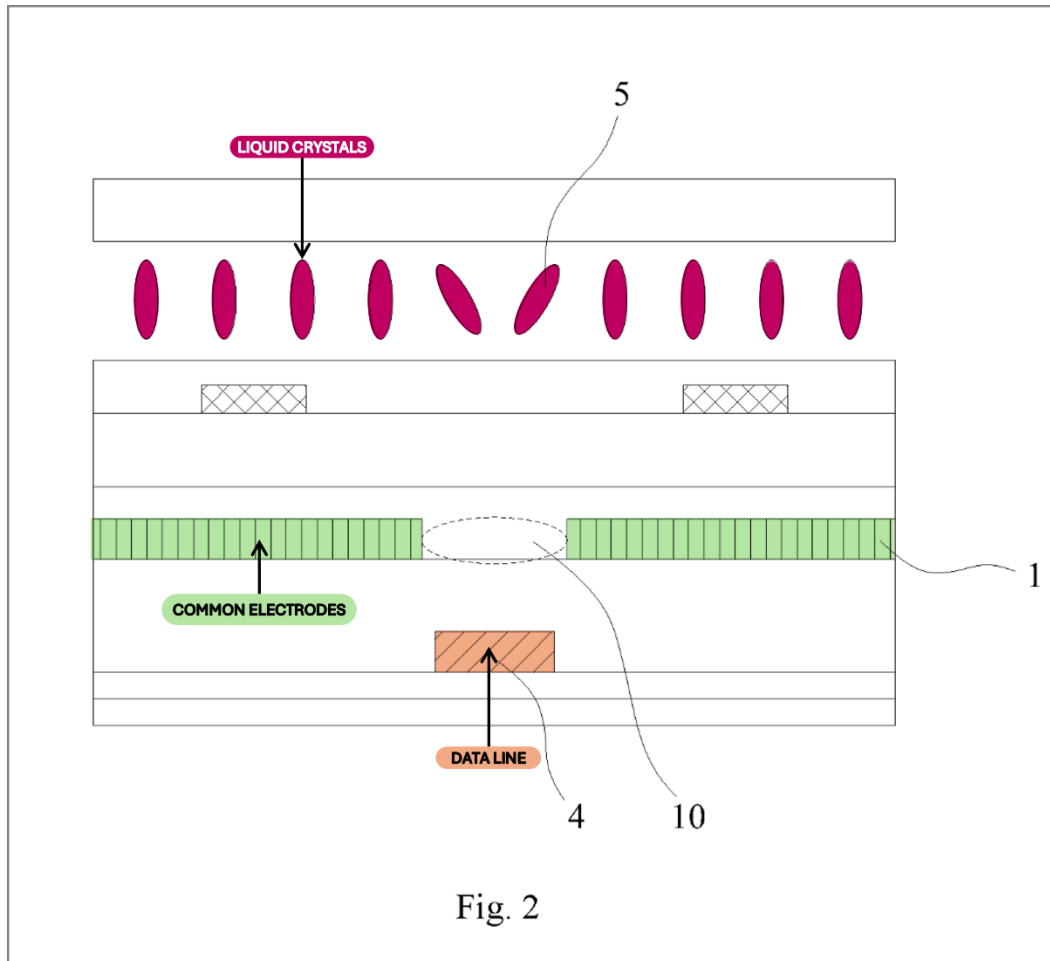
D. Xie

92. Xie is titled “Array substrate and touch display device,” was published on April 26, 2018, filed on September 12, 2017, and claims priority through a PCT application to a Chinese patent application filed in 2015. Xie at (43), (22), (86), (30). Although not relied on for any of the combinations presented in the Petition, Xie is relevant background prior art because it illustrates that the problem of undesired liquid crystal rotation due to the electrical field of the data line extending through a gap between common electrodes was known before the ’025 patent, and that the solution of shielding the liquid crystal from said electric field by positioning another line carrying the common voltage above the data line was a known solution. This shielding function is not recited or required by any of the claims, but the existing knowledge in the art of its utility is relevant to explaining the POSITA’s motivation to use certain configurations, as discussed in more detail in the grounds below.

93. Xie relates to in-cell touch panel devices, and recognizes that such devices typically include the same fundamental components as those claimed in the ’025 patent. Xie at [0025]-[0028].

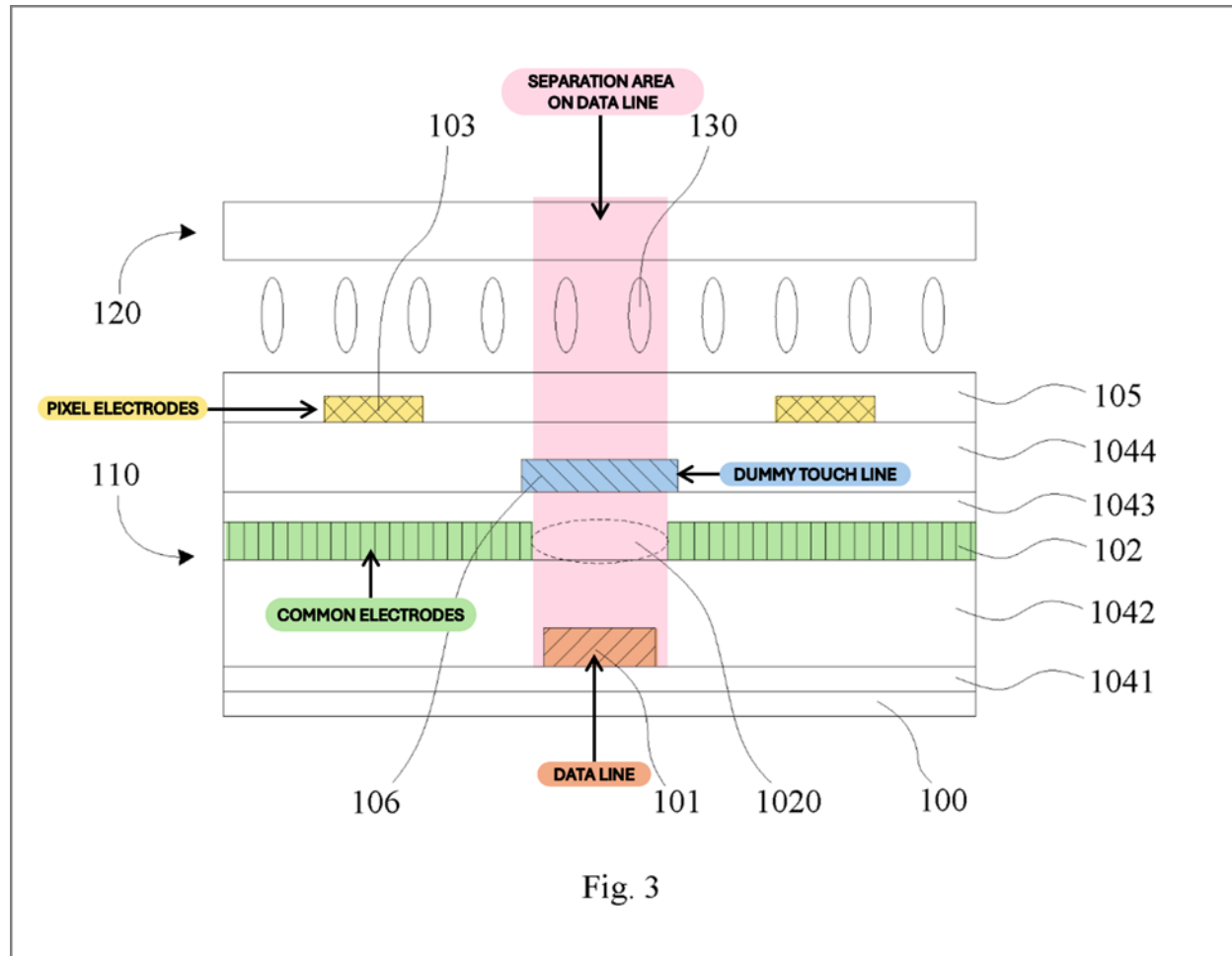
94. Xie notes that “in current in-cell technologies, a common electrode has to be cut and divided into a plurality of common electrodes,” which results in a “gap between two common electrodes [that] usually corresponds to position of the

data line.” Xie at [0005], [0029]. Xie further explains, “when a data line 4 transmits signal, an electrical field generated by the data line will go through a gap between the common electrodes 1 and consequently interfere with rotating directions of liquid crystals 5 near the gap, thereby leading to light leakage near the gap.” Xie at [0005]. Xie illustrates this issue in Figure 2, reproduced and annotated below, which shows the electric field from the data line (orange) passing through the gap between the common electrodes (green) and causing the liquid crystals (magenta) to rotate undesirably – precisely the same problem identified in the ’025 patent. *See* ’025 patent at 2:18-31.



Xie, Fig. 2.

95. Xie also teaches the same solution described in the '025 patent. '025 patent at 2:54-3:9; 22:10-14. Specifically, Xie proposes the use of a “shield line,” formed in the same layer and running parallel to Xie’s touch “address” lines, which can be positioned above the data line to block the electric field from adversely affecting the liquid crystals. Xie at [0031]-[0032]. This approach is depicted in Xie’s Figure 3 (reproduced and annotated below), and in my opinion, represents the same technical solution that the '025 patent later claims.



Xie, Fig. 3.

X. INVALIDITY ANALYSIS

96. As explained in detail in my analysis below, it is my conclusion and opinion that the Challenged Claims of the '025 patent are invalid.

A. Ground 1 – Claims 1-3, 6, and 9 Are Obvious in View of Kim and Kim II.

97. In my opinion, Kim alone and in combination with Kim II discloses and makes obvious every limitation of Claim 1 of the '025 patent under this ground. In particular, Kim, as explained in more detail below, teaches all of the

conventional elements of an in-cell touch panel recited by the challenged claims (*i.e.*, pixels, transistors, gate lines, data line, common electrodes, touch lines), and also teaches that the common electrodes are divided into segment electrodes and that the segment electrodes forming a common electrode are connected via a connecting bridge line, as recited by the claim. Although my analysis relies on Kim’s second embodiment, which does not explicitly describe a “division area” between segment electrodes being specifically located “on the gate line,” in my opinion, a POSITA would find it obvious that the division area is, or could be, positioned on the gate line, given Kim’s description of its first embodiment—which does place the gate line in the division area—and the structural similarities between Kim’s first and second embodiments.

98. Further, in my opinion, even if Kim alone did not render the limitations of Claim 1 obvious, then claim 1 would certainly be obvious based on Kim combined with Kim II, which describes a similar in-cell touch panel with segmented common electrodes and has the same corporate applicant³ as Kim. Further, Kim II teaches several advantages to placing the division area on the gate line.

³ See Kim and Kim II at (71) (each listing “LG Display Co., Ltd.” as the applicant).

1. Independent Claim 1

99. In my opinion, Kim alone and in combination with Kim II discloses and renders obvious Claim 1 of the '025 patent.

a) [1-PRE]

100. In the event that the Claim 1 preamble is found to be limiting, in my opinion, Kim discloses and renders obvious “[a]n in-cell touch panel having an image display area made up of pixels arranged in a first direction and a second direction intersecting the first direction.”

101. Specifically, Kim discloses an “in-cell touch panel,” which is referred to as a “touch sensitive display apparatus.” Kim at Abstract. Kim describes an improved “touch sensitive panel” in which a touch sensor is integrated “into a liquid crystal panel in the in-cell touch type.” Kim at [0007].

102. Kim also explains that its touch panel includes “an image display area made up of pixels arranged in a first direction and a second direction intersecting the first direction.” See Kim at [0072]-[0074]. Specifically, Kim describes the “touch sensitive panel” as having a “liquid crystal layer” with a “plurality of pixels” arranged on the transistor array in a “matrix type” configuration. Kim at [0072]-[0074]. A POSITA would understand that pixels being arranged in an array or “matrix type” configuration are arranged in rows and columns, or “in a first direction and a second direction intersecting the first direction,” as claimed. In my

view, a POSITA would recognize that Kim's panel is a typical Active Matrix (AM), composed of rows and columns of pixels. *See* Ex. 1011, p. 32, Fig. 2.3, p. 49, Fig. 2.20.

103. For the purposes of this claim mapping, I interpret the "first direction" to correspond to the horizontal rows and the "second direction" to the vertical columns, based on the orientation depicted in Kim's figures.

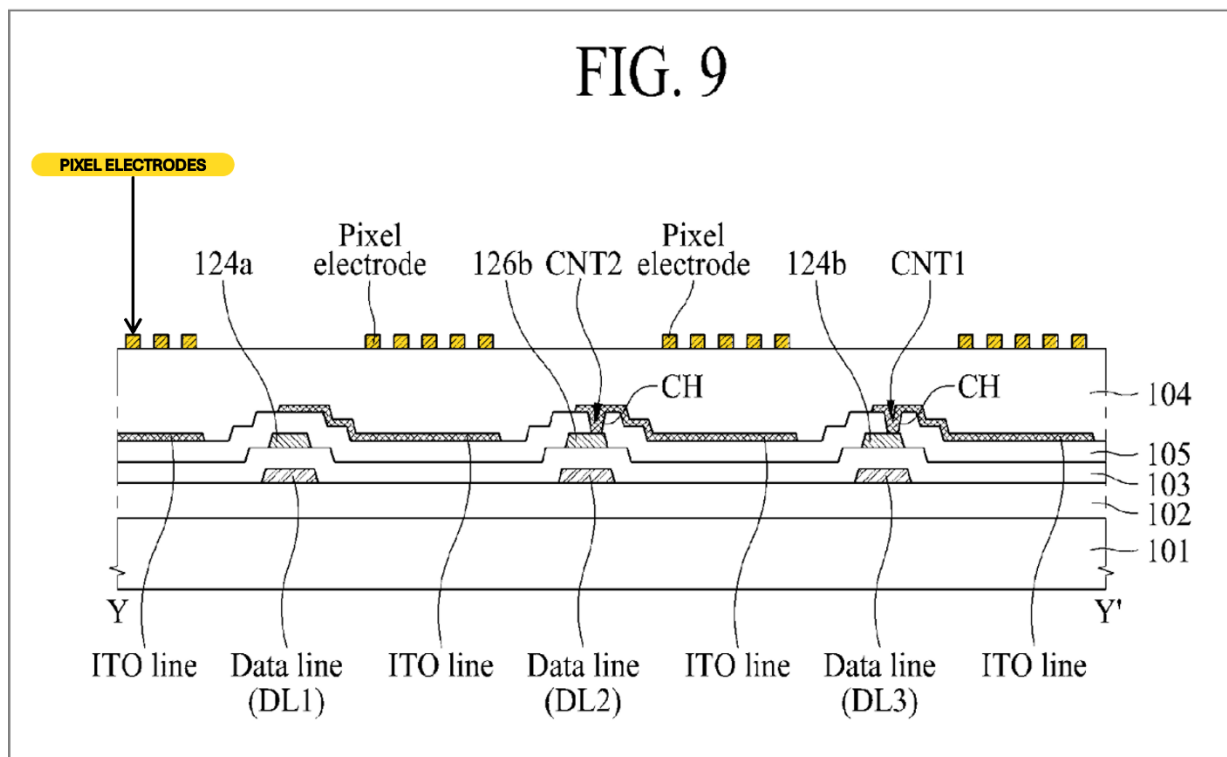
b) Element [1-A]

104. In my opinion, Kim discloses and renders obvious "transistors and pixel electrodes respectively provided in the pixels." Because Kim describes a panel comprising an LCD display, it is my view that a POSITA would understand that this entails pixels that are equipped with both transistors and pixel electrodes, as those are well-known components of an LCD pixel that have been used for decades. *See id.* at pp. 31-32, Fig. 2.3; *see also* pp. 48-49, Fig. 2.20.

105. Further, Kim explicitly discloses that each pixel includes a thin film transistor ("TFT"), stating: "The display panel may also comprise a pixel having a thin film transistor." Kim at [0036]. These TFTs are arranged in an array and configured in a matrix that corresponds to the pixel layout. Kim at [0074]. Kim further confirms these transistors correspond to the pixels, noting that its panel includes "a thin film transistor (TFT) T" that is "driving a corresponding pixel P." Kim at [0112].

106. Additionally, Kim teaches that pixel electrodes are provided within the pixels. Specifically, Kim states: “The plurality of pixels may be defined by a plurality of data lines and a plurality of gate lines which intersect each other. A TFT [*i.e.*, a transistor], a pixel electrode, and a storage capacitor (Cst) may be disposed in each of a plurality of areas defined by intersections of the data lines and the gate lines.” Kim at [0075]. In other words, consistent with the understanding of the way pixels have long worked in LCD panels, Kim explains that pixel corresponds to an intersection of the gate lines and data lines at the transistor, and a pixel electrode driven by the transistor.

107. Kim’s Figure shows these pixel electrodes, below:



Kim. Fig. 9.

c) Element [1-B]

108. In my opinion, Kim discloses and renders obvious “common electrodes arranged in the first direction and the second direction, respectively facing one or more of the pixel electrodes and provided separately from each other.” Kim at [0076].

109. Kim teaches that its touch panel includes a plurality of “common electrode[s], which “may be used as the touch electrode[s].” Kim at [0076]. Kim makes clear that these touch electrodes function as common electrodes because they are supplied a common voltage (Vcom) through the touch signal lines. Kim at [0080].⁴

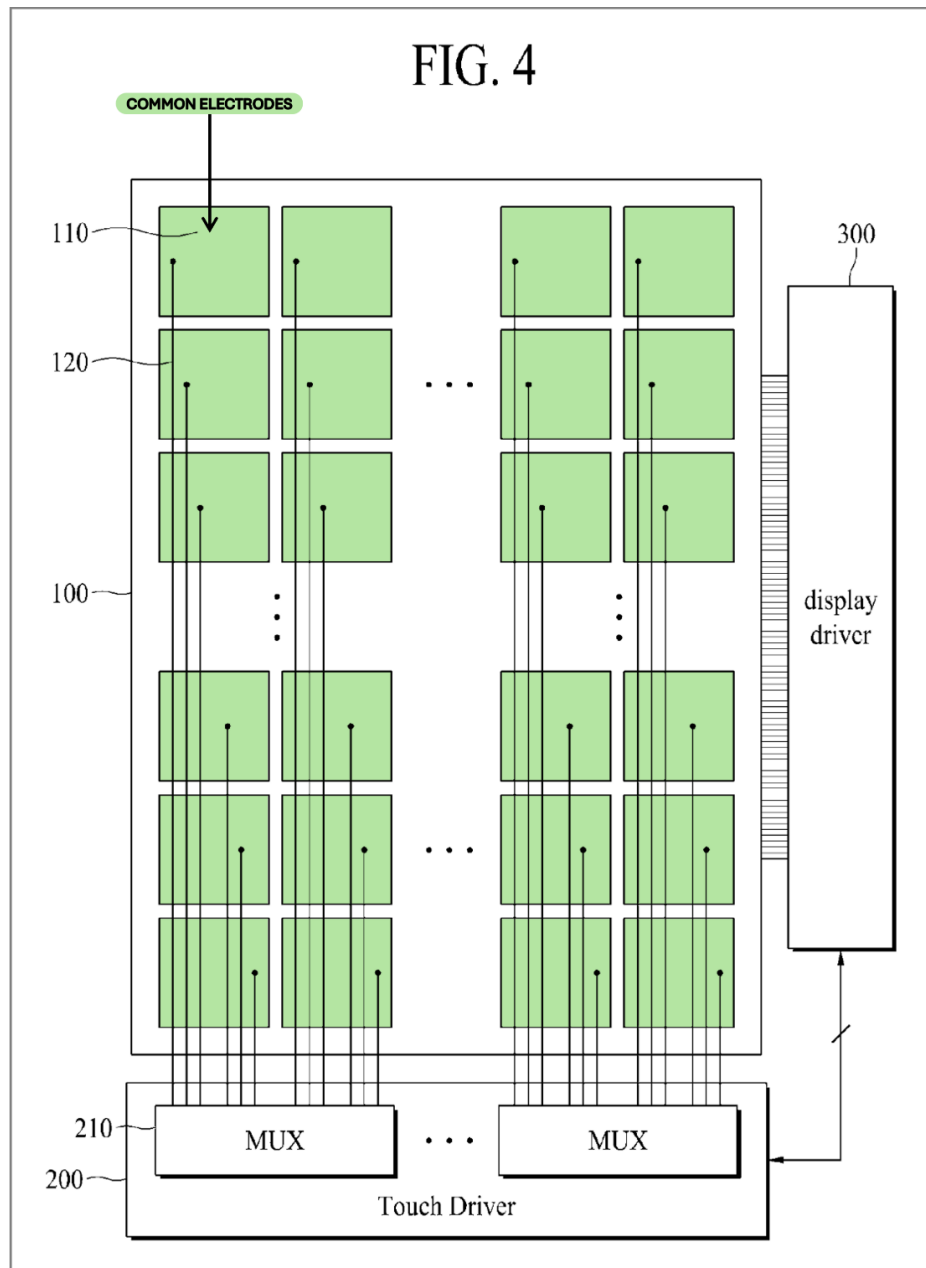
110. Kim further explains that these touch electrodes (*i.e.*, common electrodes) are arranged in both the first and second directions, stating that, “[f]or example, twenty touch electrodes 110 are disposed in a horizontal direction, and thirty-two touch electrodes 110 are disposed in a vertical direction,” resulting in a

⁴ Ex. 1011, pp. 31-32, Fig. 2.3. (noting that “[i]n a TFT based AMLCD (Fig. 2.3), both select and data lines are on the active matrix substrate, along with the pixel electrode and storage capacitor. The counter-electrode of each LC pixel capacitor, indicated by the dotted line, is a single common transparent electrode on the opposite substrate (which usually also has color filters.) This common electrode is shared by all pixels in the array.”).

total of 640 touch electrodes in the touch sensitive panel 100. Kim at [0077]. In other words, the touch electrodes (*i.e.*, common electrodes) are arranged in the first and second directions, as the claim requires. This is also evident from Kim's Figure 4, shown below.

111. Additionally, it is my understanding that Kim's touch electrodes (*i.e.*, common electrodes) are positioned to face the pixel electrodes, as the claim required. Kim explains that the touch electrodes 110 (*i.e.*, common electrodes) can be created "by patterning the common electrodes in units of pixels," with each pixel containing a pixel electrode. Kim at [0076]. This means, each touch electrode respectively faces one or more of the pixel electrodes. See Kim at [0076], [0078]. Kim further states that "Each touch electrode 110 is shared by a respective block of pixels (not shown) and serves as the display electrode for the respective block of pixels." Kim at [0078].

112. Finally, Kim teaches that these common electrodes are "provided separately from each other," as the claim requires. In addition to the above discussion regarding the plurality of separate common electrodes, Kim's Figure 4 below also depicts the plurality of common electrodes (green) as distinct and separate electrodes. The same separation of common electrodes is also depicted in Kim's Figures 7 and 8, illustrating Kim's second embodiment that I discuss further below in Section X.A.1.g.



Kim, Fig. 4.

d) Element [1-C]

113. In my opinion, Kim discloses and renders obvious “gate lines that extend along the first direction and supply gate signals to the transistors respectively.”

114. Kim explains that its gate lines supply gate signals to the transistors. Specifically, Kim describes a touch panel that includes a “display driver 300,” which may incorporate “a gate driver, a data driver, and a timing controller.” Kim at [0081]. Kim further explains that “[t]he gate driver may sequentially supply the gate driving signal to the plurality of gate lines included in the liquid crystal panel during the display period in one frame period” and that these gate signals are delivered to the TFTs “included in each of the plurality of pixels.” Kim at [0089].

115. Kim does not specifically say that the gate lines extend horizontally in the “first direction” but, as explained above, Kim appears to utilize an active matrix LCD design, and therefore a POSITA would know that it utilizes gate lines that extend horizontally, as has been conventional in LCD displays for decades. *See* Section VII.A; Ex. 1011, p. 32, Fig. 2.3, p. 84, Fig. 3.25.

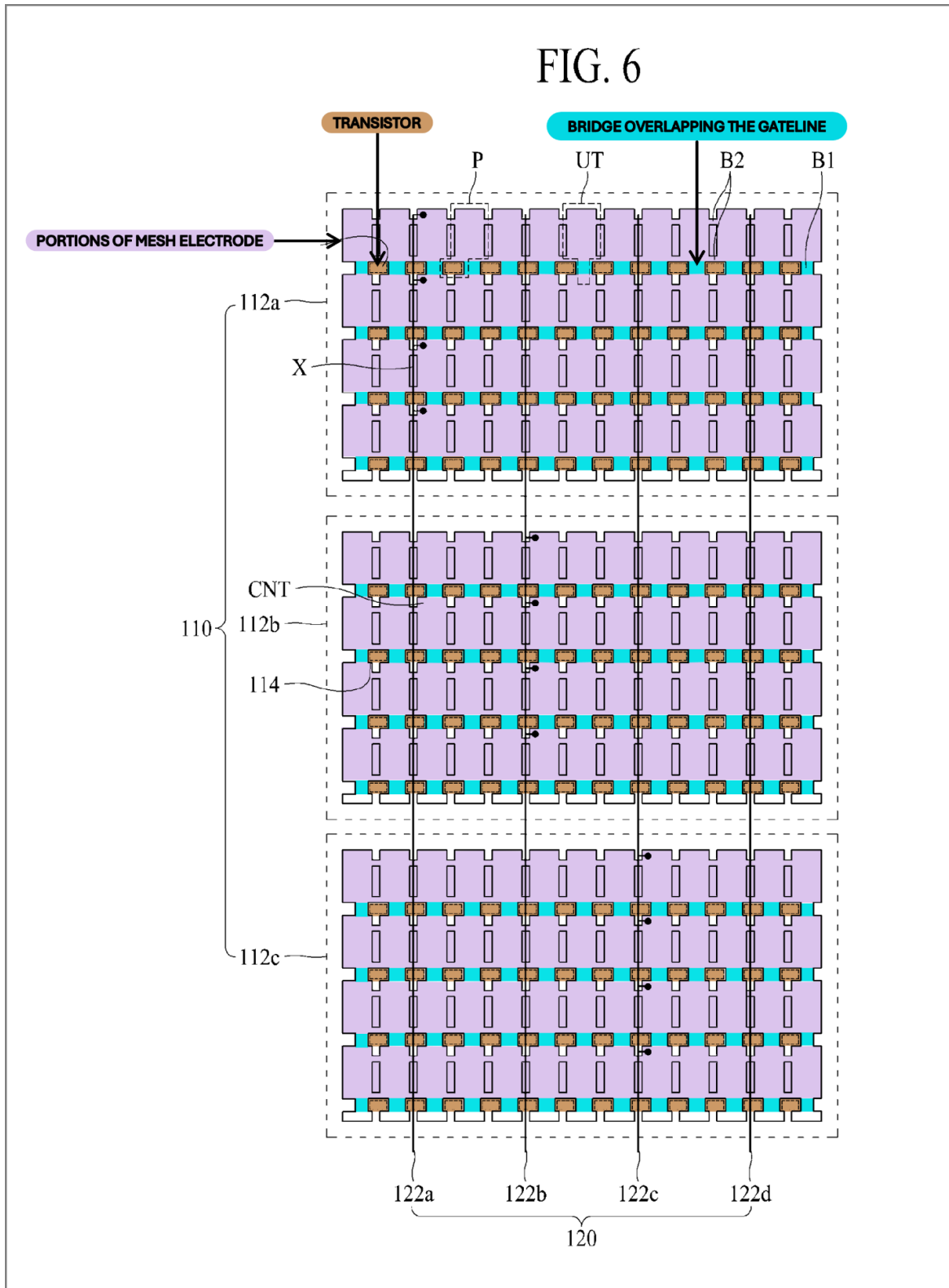
116. Further, Kim’s disclosures nonetheless make clear that the gate lines extend horizontally. Kim teaches that the gate lines intersect with the data lines, which, in an array-based panel such as Kim’s, would be understood to mean that the gate lines are perpendicular to the data lines. Kim at [0075]. Because Kim makes clear that its data lines run in the vertical direction (as I explain below for the next element), it follows that the gate lines must run horizontally. This, again, would be necessary for Kim’s active matrix display to work, as the gate lines would need to connect to every transistor in a row to activate them so they could

receive data signals from the data lines. *See* Section VII.A.

117. Additionally, the use of horizontal gate lines is a fundamental and longstanding convention in LCD design, and has been widely recognized and routinely practiced for decades. Accordingly, a POSITA would readily understand that Kim's gate lines are oriented in the first (horizontal) direction.

118. Second, in connection with Kim's first embodiment,⁵ Kim explains that Figure 6, below, depicts two unit touch electrodes connected by (cyan) bridges B1, and explains that these connected unit touch electrodes are "adjacent to each other along a corresponding gate line." Kim at [0114]. In my opinion, based on this disclosure, a POSITA would readily recognize that B1 extends vertically, connecting two touch electrodes located in vertically adjacent rows with a bridge B1 spanning over the gate line that is between them. As shown in Figure 6, these bridges B1 connect units UT that are vertically adjacent to one another (in adjacent rows). Accordingly, a POSITA would understand that the gate lines run horizontally beneath these vertical bridges, as claimed:

⁵ As explained in more detail below, while my opinions are based on Kim's second embodiment, in my opinion, a POSITA would understand that Kim's first embodiment and Kim's second embodiment differ with regard to the structure of their common electrodes, and do not differ with regard to the other conventional elements of a touch panel, including with regard to the positions and orientations of their gate lines.



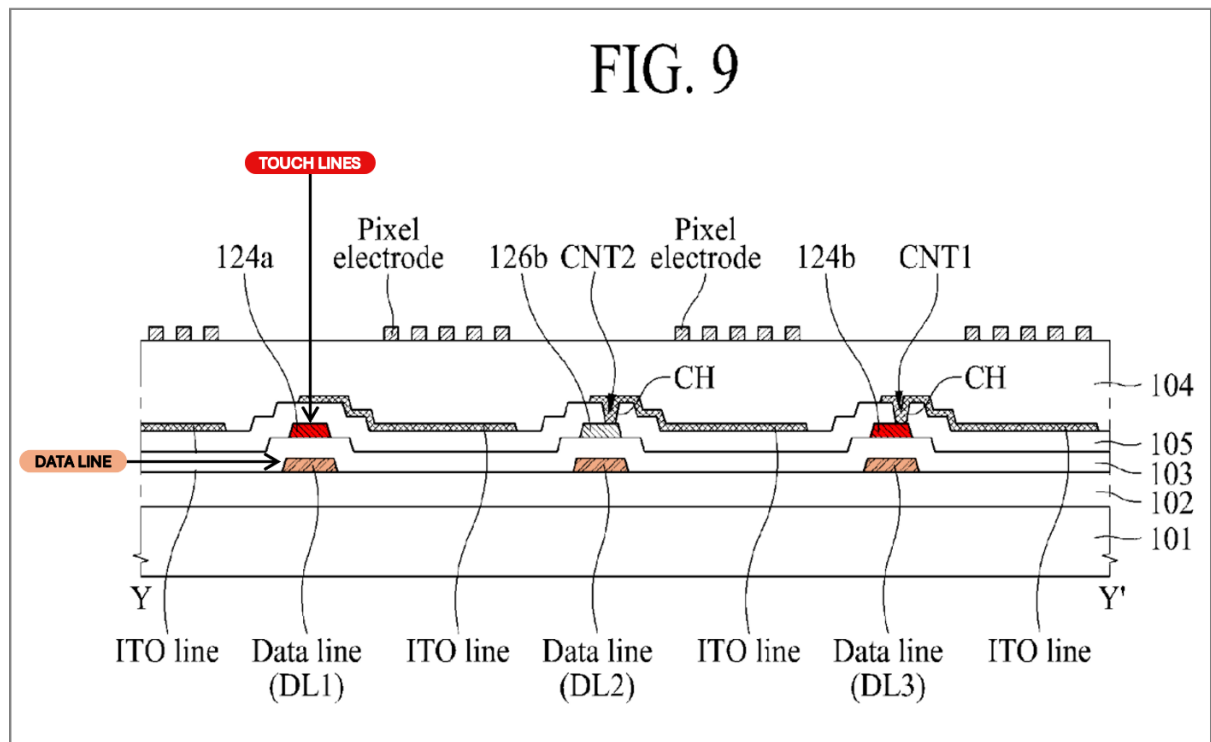
Kim, Fig. 6.

e) Element [1-D]

119. In my opinion, Kim discloses and renders obvious “data lines that extend along the second direction and supply data signals to the transistors respectively.”

120. Kim explains that it includes data lines that are responsible for supplying data signals to the transistors. For example, Kim explains that “the data driver may respectively supply the data voltages to the plurality of data lines at a time when the TFT of each pixel is turned according to the gate driving signal.” Kim at [0090]. Kim further explains that “when a first gate driving signal is supplied to a first gate line, data voltages which are to be respectively supplied to a plurality of pixels connected to the first gate line may be supplied to the plurality of data lines.” Kim at [0091].

121. Kim also teaches that the data lines extend along the second direction, *i.e.*, vertically. Specifically, Kim explains that its touch signal lines “extend in a vertical direction.” Kim at [0118], *see also* Figs. 4, 7 and 8 (showing the same). And in Kim’s Figure 9, which provides a cross-sectional view of the second embodiment, data lines (orange) are shown extending in a direction toward and away from the viewer, parallel to the vertical touch signal lines (red), meaning they are also extending in the same vertical “second direction.”



Kim, Fig. 9; *see also* [0145] (stating that “data lines oriented in the same direction as the touch signal lines 120”); [0114]-[0115] (explaining that bridges B2 can bridge over the data lines).

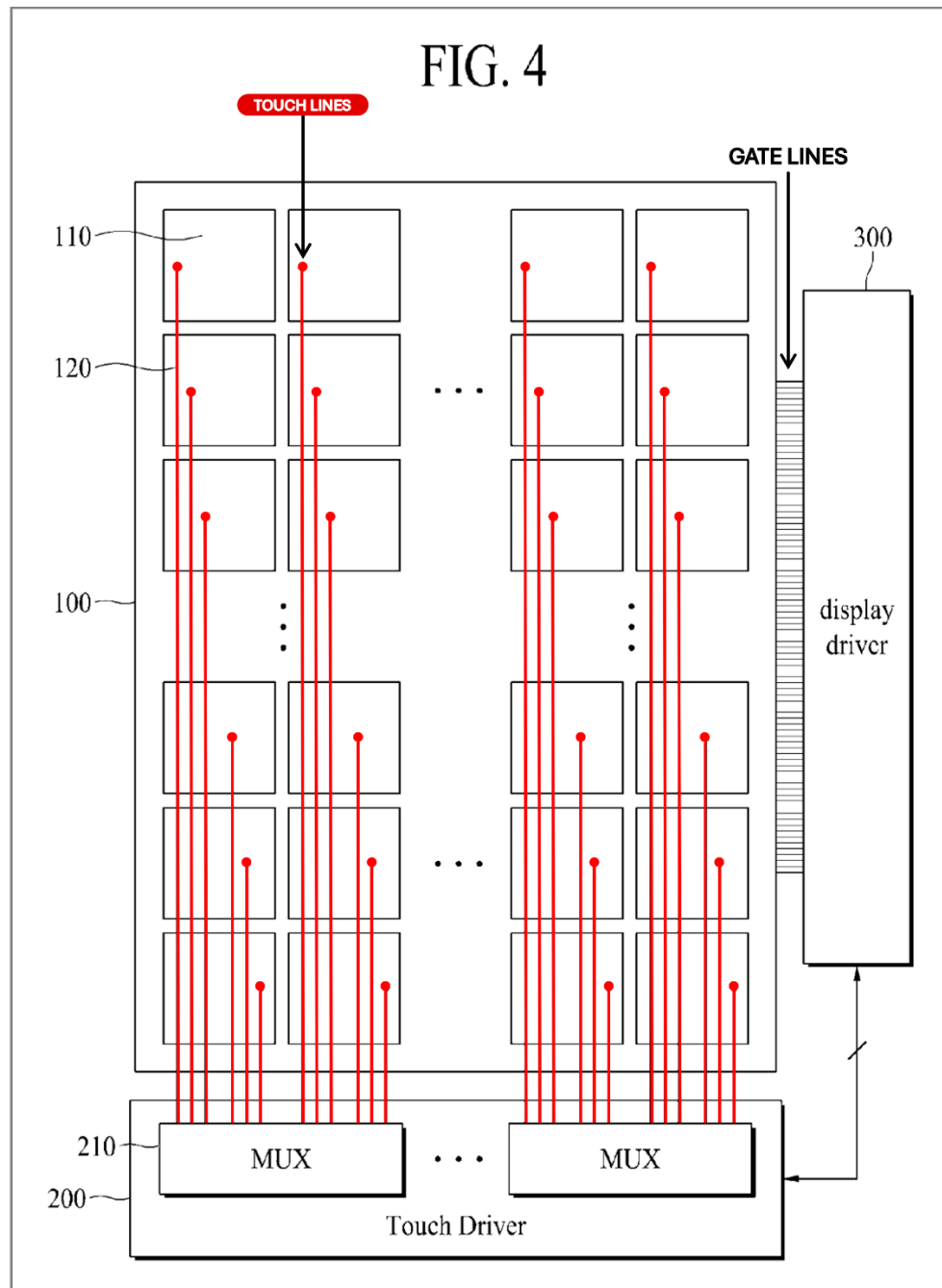
122. Additionally, Kim explains that the touch panel includes data lines that intersect with the gate lines, which indicates that the data lines run in the “second direction.” Kim at [0075]. Kim notes that the pixels are defined by intersecting data lines and gate lines, and that each intersection includes a TFT, a pixel electrode, and a storage capacitor. *Id.* In my assessment, Kim makes clear that this intersection occurs at the transistor, confirming that the data lines are oriented perpendicularly to the gate lines. *See id.*

f) Element [1-E]

123. In my opinion, Kim discloses and renders obvious “touch lines that extend along the second direction and are each connected to a corresponding one of the common electrodes.”

124. Kim specifically discloses that each of the touch electrodes 110, which serve as common electrodes, “may be connected to a corresponding channel of the touch driver 200 through a corresponding touch signal line 120 among a plurality of touch signal lines 120.” Kim at [0078], Fig. 4. Kim teaches that each touch line may be connected to a corresponding touch electrode (*i.e.*, common electrode). Kim explains that “each of the plurality of touch electrodes 110 may be connected to one or more touch signal lines 120 through a plurality of first contacts CNT1 at different locations.” Kim at [0119]. This arrangement is also visually represented in Figure 4, which shows each touch line connecting to a corresponding touch electrode: ⁶

⁶ For Kim’s second embodiment, certain of these touch signal lines are referred to as “touch signal lines 124.” Kim at [0118]; Fig. 7 (showing touch line 124a and 124b connecting to only one of the two depicted touch electrodes); Fig. 8 (same).



Kim, Fig. 4.

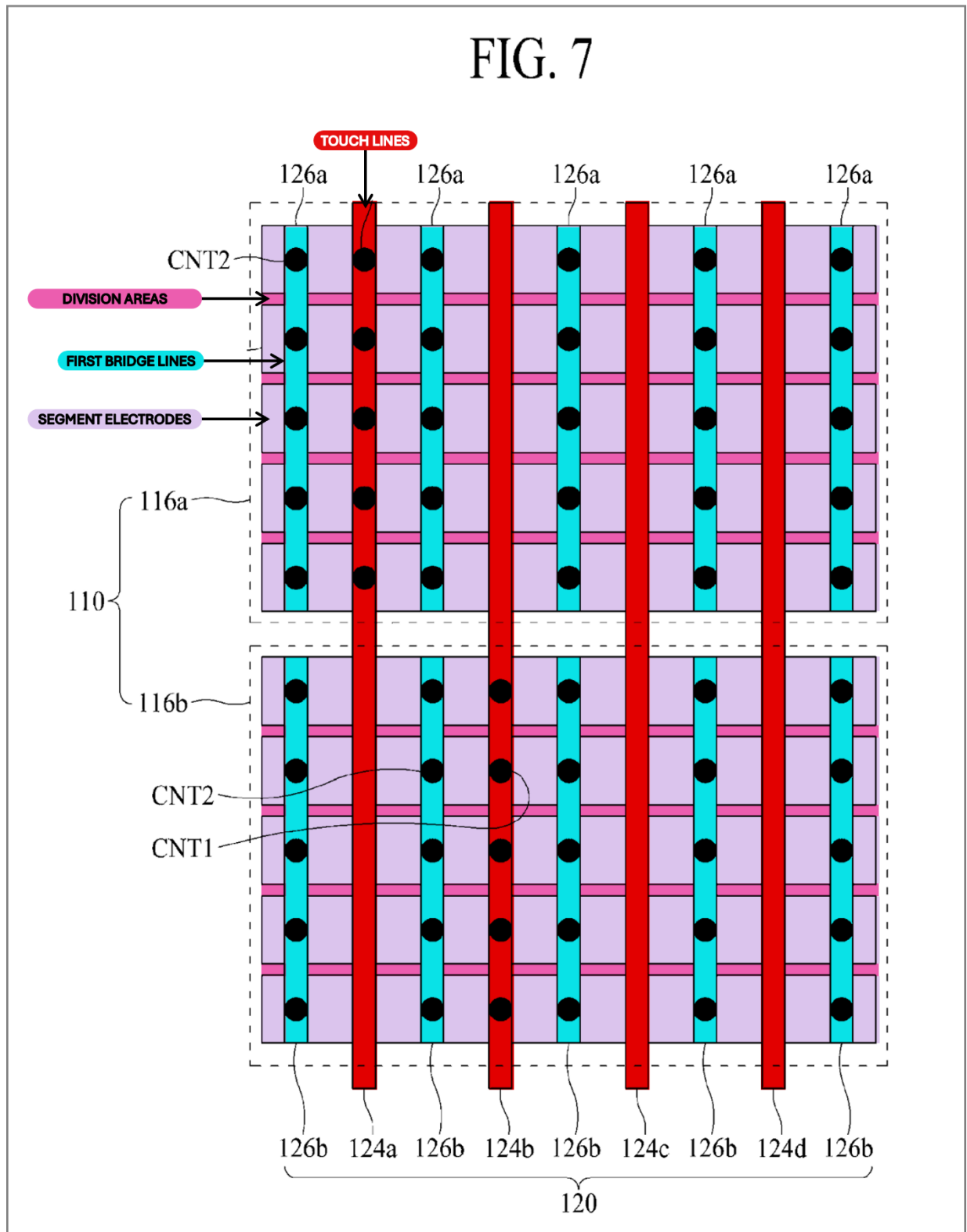
125. Additionally, Kim expressly states that these touch signal lines “extend in a vertical,” *i.e.*, the claimed “second direction.” Kim at [0118]. This is also evident from Kim’s Figures 4, 7 and 8, all of which show these vertically

oriented touch lines. *See also* Kim at [0145] (stating that “data lines oriented in the same direction as the touch signal lines 120”).

g) Element [1-F] and [1-G]

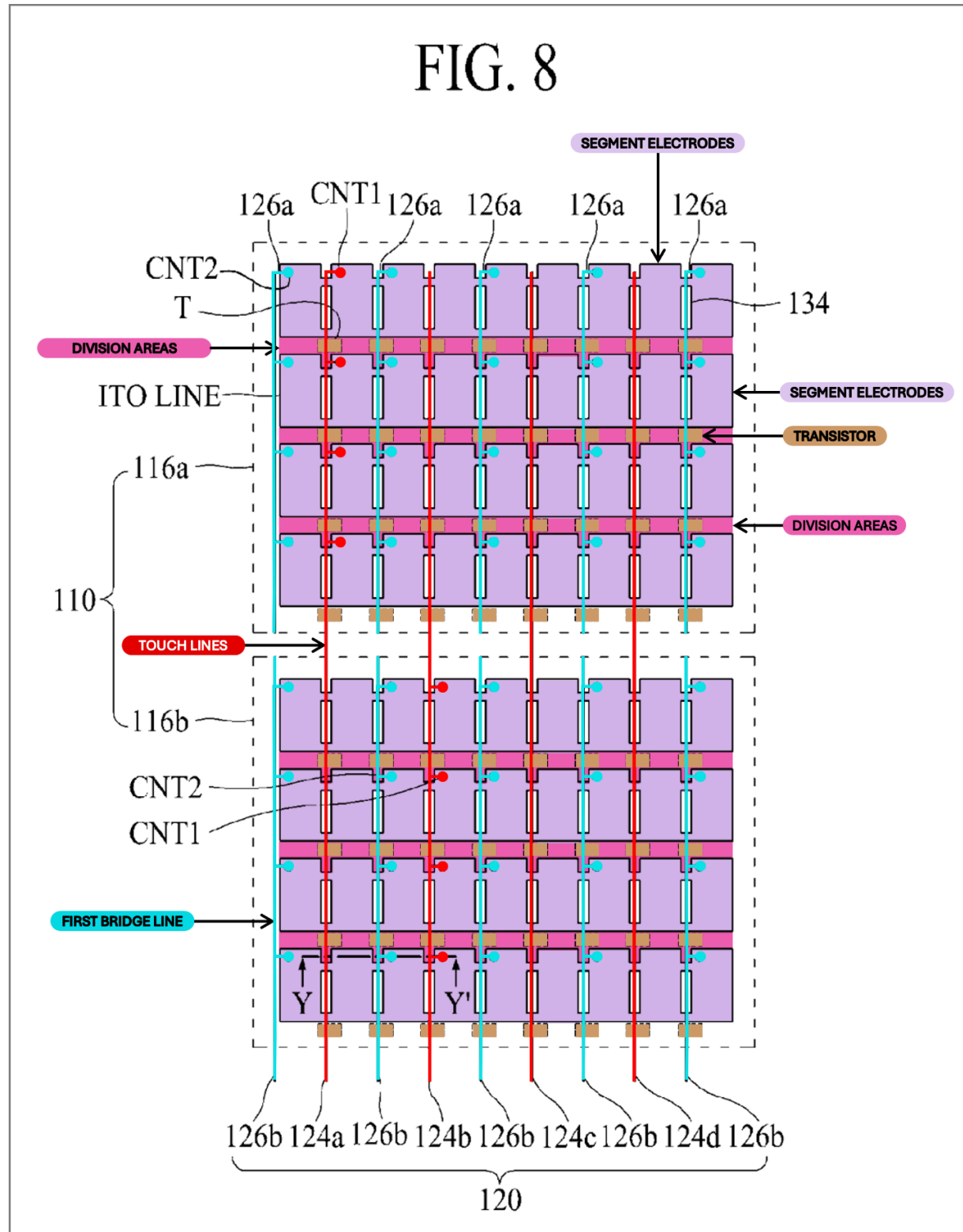
126. In my opinion, Kim both alone and in combination with Kim II, discloses and renders obvious “a first bridge line laterally bridging two of the segment electrodes adjacent in the second direction across one of the division areas, wherein each common electrode has segment electrodes divided with a division area on the gate line.”

127. With regard to the “wherein” limitation, Kim alone teaches common electrodes that are divided into segment electrodes with a division area between them. For example, in Kim’s second embodiment, the touch electrodes 110 (*i.e.*, common electrodes) are divided into “multiple touch electrode lines made from ITO (ITO Line),” each corresponding to what the ’025 patent refers to as a segment electrode. Kim at [0118], [0142]. Kim explains that these “ITO lines extend in the horizontal direction and are parallel to each other.” *Id.*; Figure 7 of Kim, reproduced and annotated below, confirms this orientation and shows these ITO lines (purple) as spaced apart from each other by a small distance, *i.e.*, a division area (pink). *See also* Kim, Fig. 8.



Kim, Fig. 7. Figure 8 provides a more detailed illustration of these elements.

FIG. 8



Kim Fig. 8.

128. With regard to the “a first bridge line” limitation, Kim teaches “a first bridge line laterally bridging two of the segment electrodes adjacent in the second direction across one of the division areas.” In particular, Kim discloses “connecting lines 126,” that correspond to the “bridge lines” of the ’025 patent. Kim explains that these connecting lines serve as a bridge between segment electrodes, as they “connect[] different ITO lines of a touch electrode 110 to each other.” Kim at [0120]. Kim further explains that these “connecting lines 126 extend in a vertical direction and are perpendicular to and intersect the ITO lines,” and thus laterally bridge adjacent ITO lines (segment electrodes) in the second direction (vertical), crossing over the division areas. *See* Kim at [0118], [0120]. This is illustrated in Figures 7 and 8, provided above, which show these (cyan) bridge lines laterally bridging the (pink) division areas between the (purple) segment electrodes.

129. The final part of this element requires that the “division area” between “segment electrodes” be “on the gate line.” In my opinion, Kim alone teaches, or at least renders obvious this limitation. But even if this limitation were deemed to not be taught or obvious based on Kim, it would certainly be obvious based on Kim II.

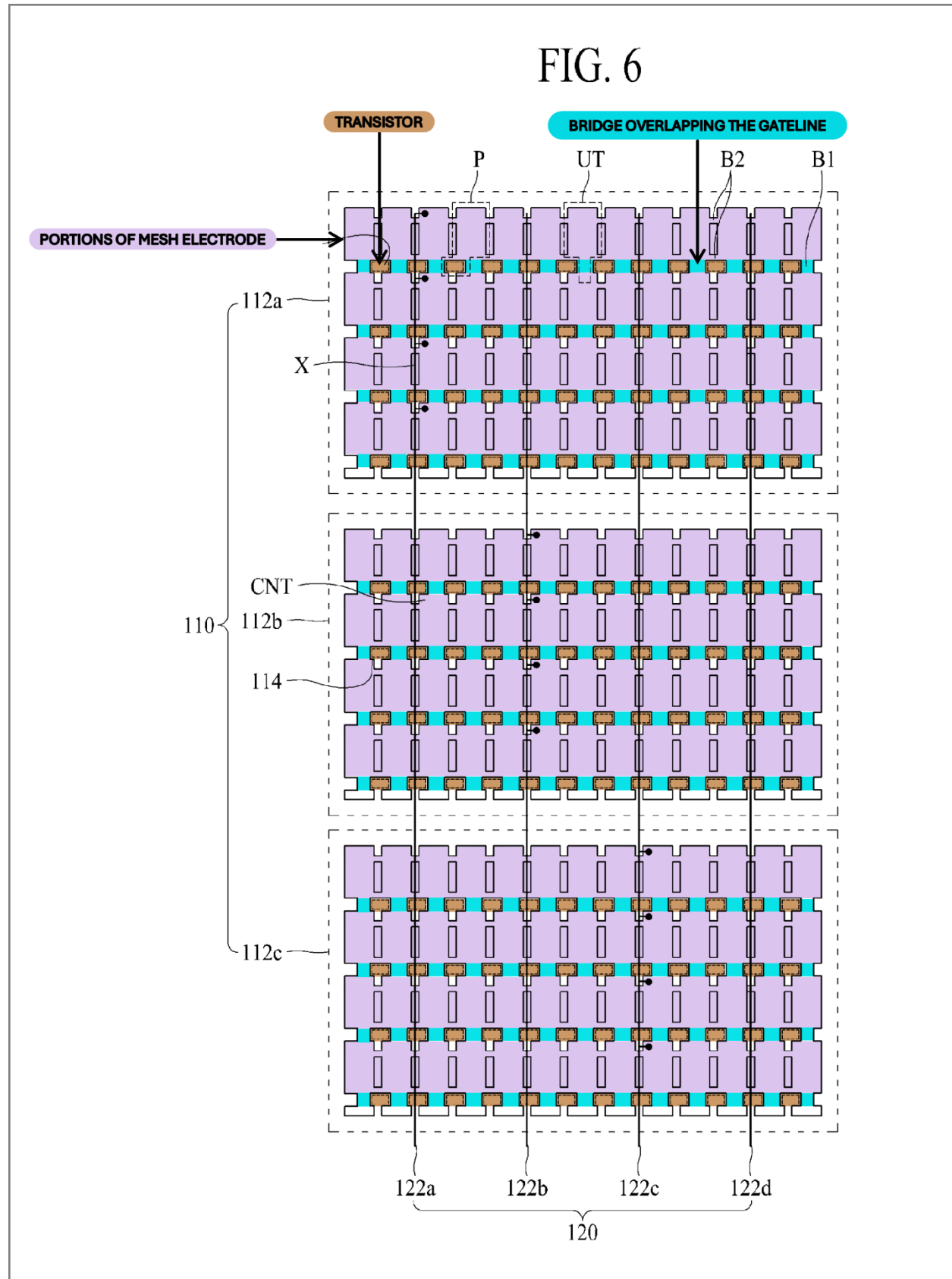
130. First, it is my view that a POSITA would understand, or at least find it obvious, that in Kim’s second embodiment, the division areas between segment

electrodes are positioned on the gate line. Unfortunately, with regard to Kim's second embodiment, Kim does not include a detailed description of how the gate lines are positioned. But, as I explained above, Kim makes clear that its gate lines run horizontally and connect to Kim's transistors, and that the transistors are disposed within the division areas. *See* Section X.A.1.d above; *see also* Kim, Fig. 8 (reproduced and annotated above). Because the gate lines connect to and supply signals to these transistors, it would be apparent to a POSITA that the most straightforward design would have the gate lines run directly through the division areas to connect to the transistors, thus placing the division area on the gate line as required by the claim. Kim at [0089]. Indeed, it would be unusual and overly complex to provide the gate line elsewhere, and there is no real reason why a POSITA would wish to put the gate line anywhere other than this natural and obvious place. Moreover, a POSITA would also understand that such an indirect gate line placement could be potentially detrimental, as a longer or serpentine gate line could cause increased resistance and capacitance along the line, leading to potential distortions or delays of the gate signal. *See* Ex. 1011, pp. 177-178, Fig. 6.38.

131. Second, despite the lack of detail concerning the positions of the gate lines for Kim's second embodiment, Kim does include more details relating to its first embodiment, which is substantially similar to Kim's second embodiment.

Instead of using touch electrodes that are divided into ITO lines like in Kim's second embodiment, Kim's first embodiment teaches a mesh-like touch electrode that nonetheless has a similar size and shape to the divided touch electrode of the second embodiment. *See, e.g.*, Kim, Figs. 6 and 8. The mesh electrodes of this first embodiment, however, are not divided and thus do not create the same "division area" that appear in the second embodiment. That portion of the panel, however, is obviously still present in Kim's first embodiment. It is the horizontal area in line with the row of transistors, over which the (cyan) bridges B1 extend, as shown in Figure 6 below:

FIG. 6



Kim, Fig. 6.

132. In connection with this first embodiment, Kim makes clear that the gate lines are positioned in that same area that corresponds to the “division area” of the second embodiment. In particular, Kim explains that these bridges are located along the gate line, stating that “bridges B1 may electrically connect two unit touch electrodes UT which are adjacent to each other ***along a corresponding gate line,***” and that “bridges B1 may be disposed to ***overlap the gate lines.***” Kim at [0114], [0115] (emphasis added).

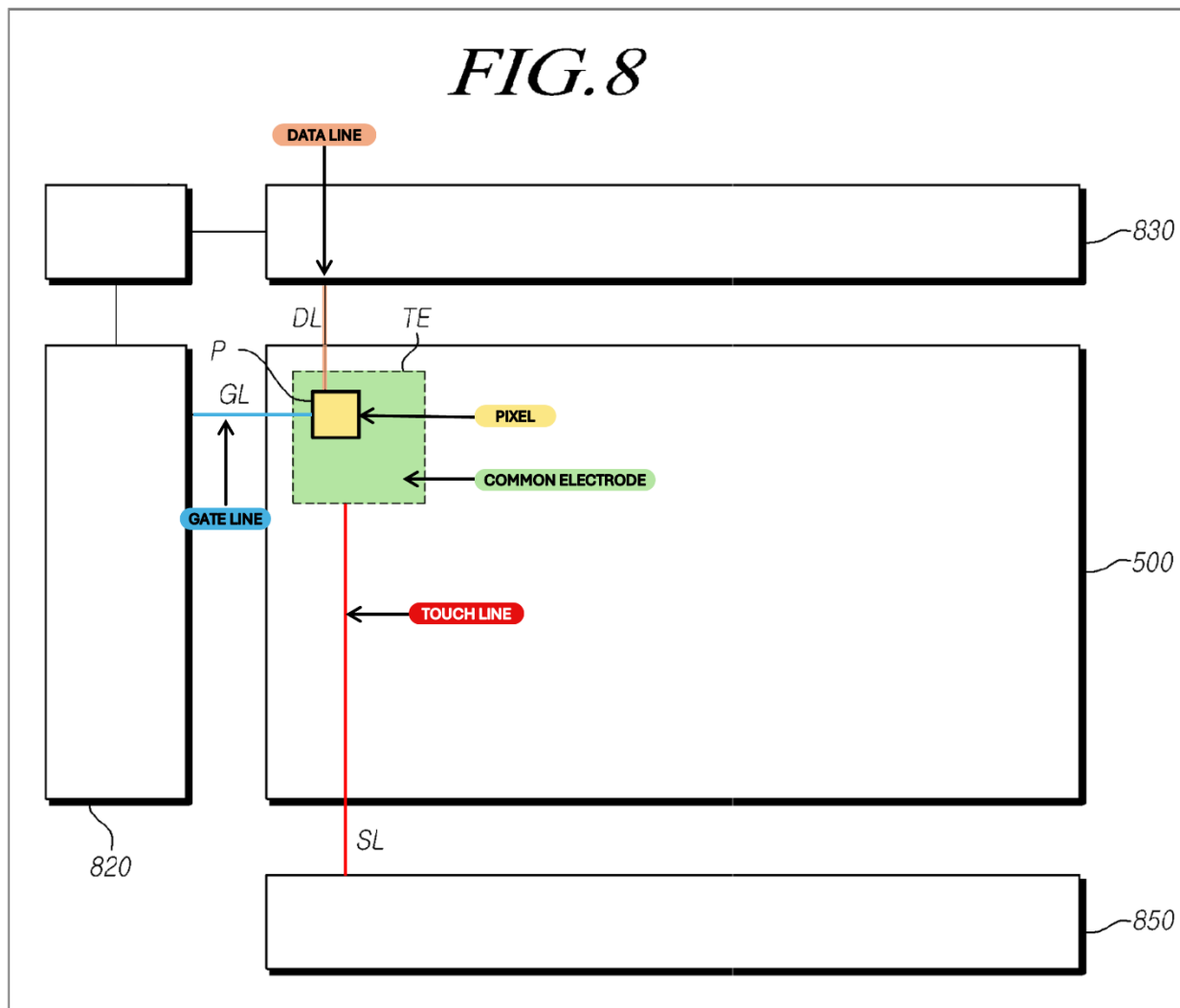
133. While this disclosure concerns the first embodiment, in my opinion, a POSITA would understand that its discussion concerning the position of the gate line would similarly apply to Kim’s second embodiment. A POSITA would understand that the difference between Kim’s first and second embodiment is the structure of its common electrode, not the underlying structure of its pixels, data lines and gate lines. *see, e.g.,* Kim at [0099], [0117] (describing the first and second embodiments based on the structures of their touch electrodes). Nowhere does Kim suggest there are any difference in the placement of transistors, gate lines, or data lines between the two embodiments. Accordingly, a POSITA would understand and find obvious that the underlying structure, including the placement of gate lines, is the same in both embodiments. At the very least, a POSITA would find it obvious that they could be the same.

134. In my opinion, a POSITA would have further understood that the “division areas” in Kim are, or could obviously be, positioned “on the gate line” in light of Kim’s teachings regarding the benefits of slits 114. In its first embodiment, Kim describes touch electrodes containing vertical slits 114, which are bridged by bridges B2, as well as slits 114 located over the transistors. *See* Kim at [0028], [0100]–[0101], [0111]–[0112] (noting that these slits 114 are placed in the “non-display area so as not to affect an operation of generating an electric field with the pixel electrode in display driving” and can be “disposed in an area where a thin film transistor” is located). Kim further explains that these slits correspond to the location of the touch line, providing the benefit of reducing the load in each touch electrode and decreasing the overlap capacitance between the touch signal line and the touch electrode. *See* Kim at [0116]. Accordingly, just as bridges B2 bridge the vertical “slit” non-display area with the touch line and data line, it is my opinion that a POSITA would recognize that bridges B1 bridge the horizontal “slit” non-display area corresponding to the “division area” of Kim’s second embodiment—where the gate line is, or could obviously be, positioned—to achieve the same benefits of reducing overlap capacitance and supporting Kim’s goal of avoiding any effect on display driving. Kim at [0116], [0100].

135. In my opinion, a POSITA would also have found it obvious to position the “division area on the gate line” in view of Kim II, which provides an

even more detailed disclosure of this feature. Kim II describes a remarkably similar touch panel to Kim. Kim II was applied for by the same company as Kim and describes a touch-integrated panel that is nearly identical to Kim's.

136. Kim II describes including horizontal (blue) gate lines (GL), vertical data lines (DL), and vertical (red) touch lines (referred to as "sensing lines SL" in Kim II). *See* Kim II at [0008] (explaining how gate lines and data lines intersect at the transistor of a pixel); [0022] (describing the sensing lines overlapping with the data lines); Fig. 8. Kim II further teaches that its panel includes (green) touch electrodes (*i.e.*, common electrodes) that are disposed over multiple pixel areas. Kim II at [0013]; Fig. 8 (reproduced and annotated below).

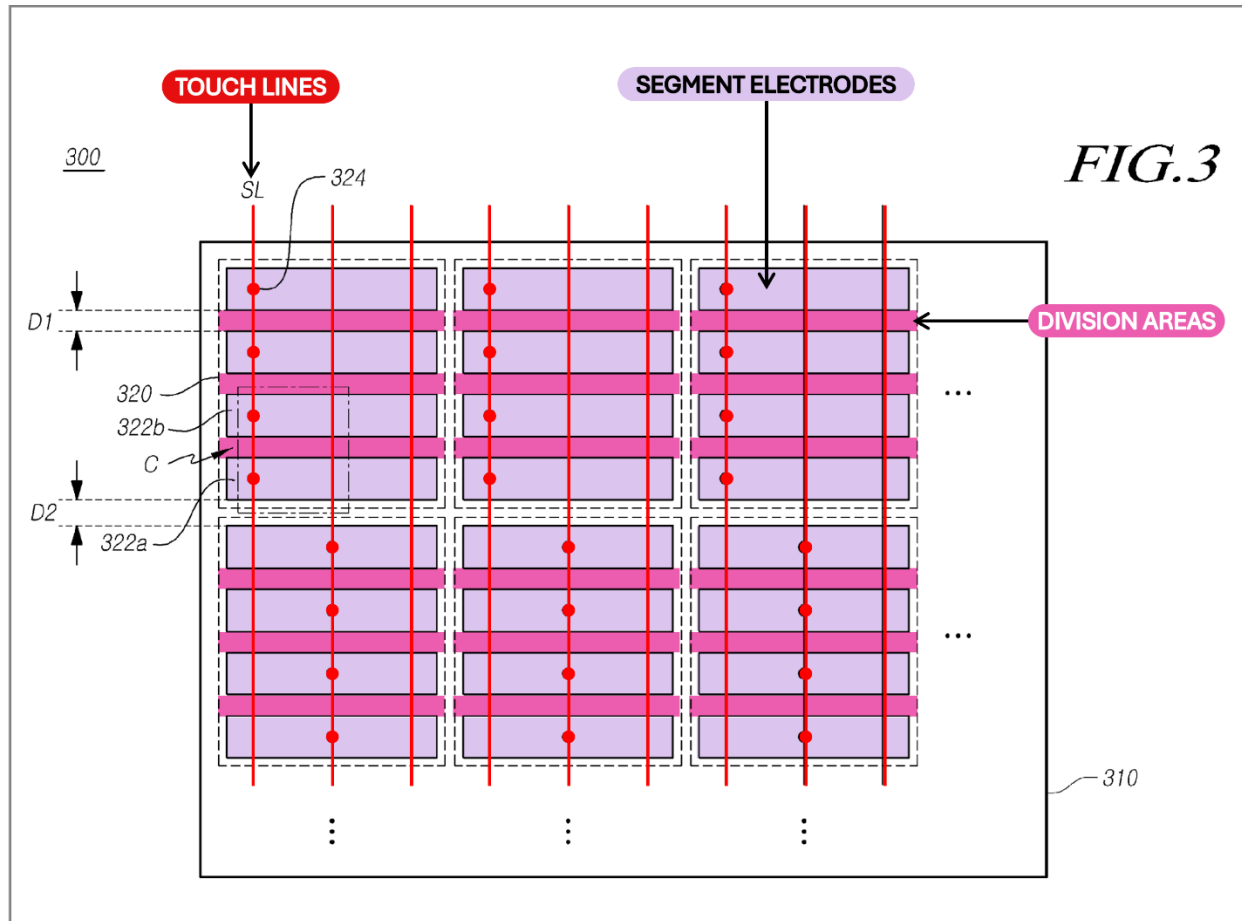


Kim II, Fig. 8.

137. Like Kim, Kim II also teaches that its touch electrodes are divided into several “common voltage electrode rows,” which correspond to the segment electrodes in the ’025 patent, and that Kim II’s sensing lines (*i.e.*, touch lines) connect to all the common voltage rows within a common electrode through contact holes. Kim II at [0052], [0058]; *see also* Fig. 3 (reproduced below).

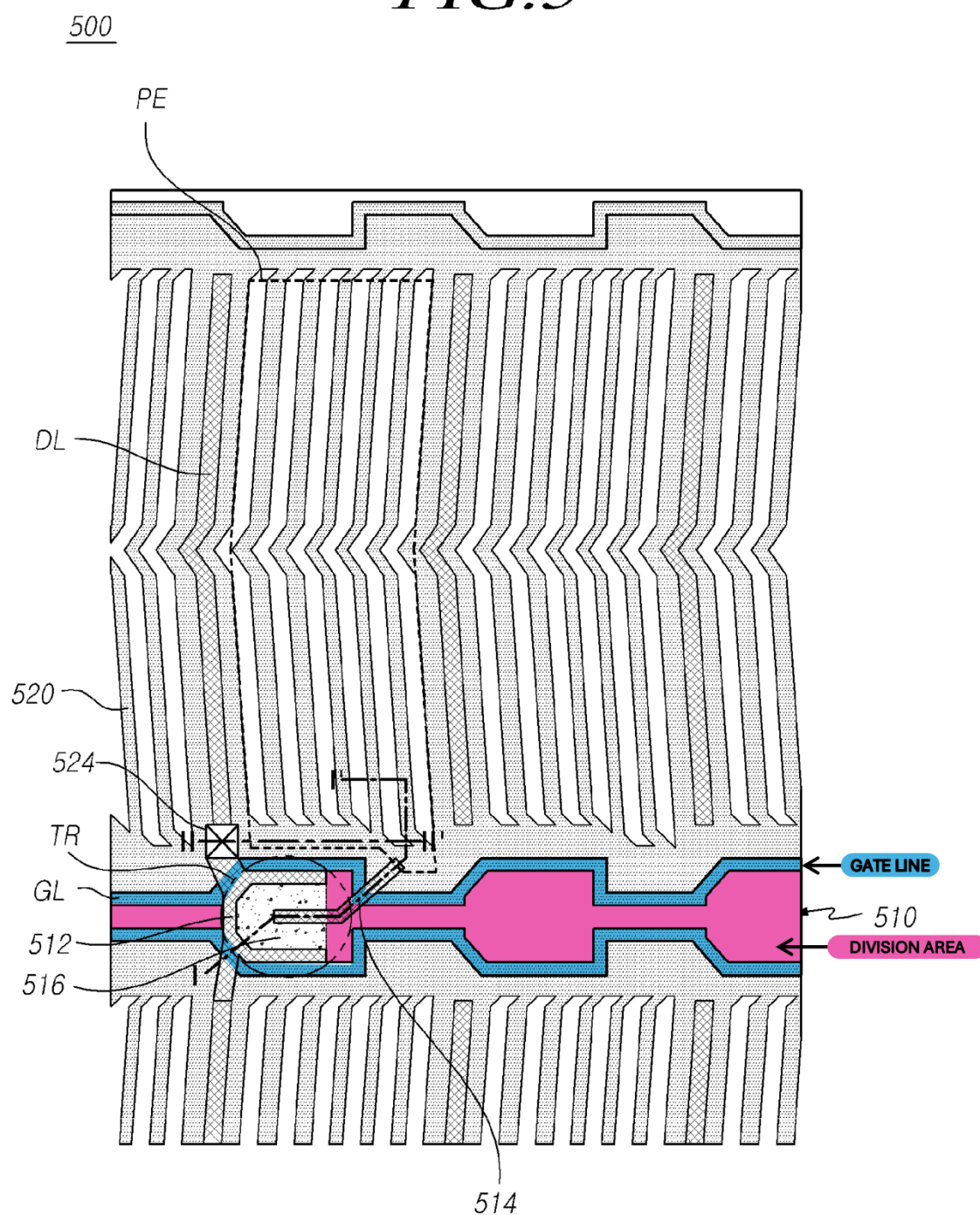
138. Further, Kim II describes a (pink) separation space between these

(purple) rows—referred to as “separation distance D1” or “separation space 430b”—which separates common voltage electrode rows within a touch electrode 320. Kim II at [0060], [0065]; [0089]-[0090], *see also* Figs. 4-6. In connection with Figure 5, Kim II further refers to this separation as “separation space 510,” *i.e.*, separation area, (pink) and explicitly teaches that this separation space is “on the” (blue) gate line, as required by the Challenged Claim. Kim II at [0090]; Fig. 5. Specifically, Kim II states that the separation space between different rows of the common voltage electrodes may correspond to a line area of the gate lines, and that the (blue) gate line may be formed in the (pink) separation space 510 between two common voltage electrodes 520. Kim II at [0065], [0090] (“The separation space 510, *i.e.*, separation area, formed between different rows of the common voltage electrodes 520 may correspond to a line area of the gate lines GL. Specifically, in the exemplary embodiment as illustrated in FIG. 5, the gate line GL or a portion of the gate line GL may be formed in the separation space 510 between two common voltage electrodes 520.”).



Kim II, Fig. 3.

FIG. 5



Kim II, Fig. 5, [0089]-[0090]. Kim II therefore teaches that the claimed “division area” is “on the gate line” as claimed.

139. In my opinion, a POSITA would have certainly been motivated to combine Kim and Kim II, and would have had significant assurance that their teachings were compatible and could be easily combined with a reasonable expectation of success. Indeed, given that Kim and Kim II have the same corporate applicant, it seems that in actuality, the teachings were in fact provided by engineers working at the same company, almost certainly on the same or substantially similar touch panels. Further, as explained above, Kim and Kim II have very similar structures, including with regard to their pixels, transistors, gate lines, data lines, common electrodes that are divided into segment electrodes and touch lines. Further, a POSITA would recognize that the only differences between Kim and Kim II are largely immaterial, and pertain to the precise mechanism that the components use to manipulate the liquid crystals rather than the type or function of the claimed components. For example, Kim discusses embodiments of panels where the pixel electrodes are above the common electrodes (see Kim, Fig. 9), whereas Kim II has the common electrodes above the pixel electrodes (see Kim II, Figs. 6 or 7).

140. In my opinion, a POSITA would have been strongly motivated to combine the teachings of Kim and Kim II, as Kim and Kim II are both FFS (Fringe

Field Switching) mode displays. Further, while Kim and Kim II use different arrangements as to whether the common electrode is above or below the pixel electrode is immaterial, both arrangements have been widely used in the art for decades and a POSITA would understand these design considerations and how to modify and adapt the teachings of a panel despite such a minor design difference. See Kim at [0068]. Further, a POSITA would also recognize that the particulars of the vertical arrangement of Kim and Kim II's common electrodes as compared to pixel electrodes is immaterial to Kim II's teaching regarding reducing capacitance between the gate line and the common electrode, as the POSITA would recognize that Kim II's approach teachings relate to the spatial relationship between these elements, not their vertical order in the substrate stack. In fact, in Kim's structure—where the common electrode is beneath the pixel electrode and thus even closer to the gate electrode—the POSITA would recognize that the capacitance issues Kim II seeks to prevent would be even more pronounced, further motivating a POSITA to adopt Kim II's approach.

141. Further, a POSITA would have been specifically motivated to implement Kim II's teachings regarding the placement of the gate line in the division area in a design based primarily upon Kim. Specifically, Kim II teaches that this placement provides several advantages and helps avoid common display problems. In particular, Kim II explains that, in conventional touch panels,

common electrodes were large and overlap multiple pixels and there transistors, which would cause uneven and excessive capacitance at the gate electrodes of the transistors, especially between those transistors at the center of a large touch electrodes as compared to those at the edge. Kim II at [0013]-[0016], [0036]-[0048], [0088]. This uneven and, in some places, excessive capacitance would distort and delay the gate-source voltage of the gate electrode (*i.e.*, the voltage needed to turn on the transistor), particularly for transistors located far from the gate driver and the edge of a touch electrode. As a result, the data line may be prevented from fully and accurately supplying the data voltage to the transistor's pixel electrode, leading to potential display defects. Kim II at [0016]. Further, this distortion may also increase the time required to turn on the transistor, causing image problems for certain pixels in a horizontal row. Kim II at [0047].

142. Kim II teaches that each of these problems can be solved by placing the division area between common voltage electrode rows (*i.e.*, segment electrodes) on the gate line. *See* Kim II at [0089]-[0090]. Specifically, Kim II recognizes that “[t]he gate line GL and an electrode adjacent thereto greatly affect a capacitance of the gate electrode 518.” Kim II at [0090]. Accordingly, Kim II explains that positioning the separation space on the gate line makes the capacitance of the gate electrode more uniform “regardless of being inside the touch electrode and at an outer periphery of the touch electrode,” and “[b]y

positioning the separation space 510 on the gate line GL, a capacitance of the gate electrode 518 may be decreased,” thereby avoiding the display defects, and further allowing “transistor TR” to be “driven at an increased speed.” Kim II at [0089], [0090]. As such, a POSITA would be highly motivated to adopt Kim II’s specific gate line placement in Kim’s existing separation areas to avoid capacitance-related display problems, and to achieve the performance benefits described in Kim II. *See* Kim II at [0036]-[0048], [0089]-[0090].

143. Furthermore, Kim’s own teachings reinforce the desirability of reducing overlap capacitance. For example, Kim’s first embodiment teaches that positioning touch lines over slits in the touch electrode reduces overlap capacitance “between a corresponding touch signal line and a corresponding touch electrode” and prevents image quality degradation “due to the overlap capacitance.” Kim at [0116]. Thus, Kim already recognizes the value of positioning lines to minimize capacitance, and a POSITA would view Kim II’s teachings regarding gate line placement as a logical and complementary solution aligned with Kim’s design goals.

144. As I have explained above, Kim already teaches—or at least renders obvious—that its gate lines run parallel to the division areas between its segment electrodes, which also include the transistors to which the gate lines must connect. To the extent a POSITA would not have immediately understood that the gate lines

should overlap the division areas, it would have been obvious to design the panel so that Kim's gate lines and division areas do overlap. I believe that a POSITA would find clear motivation to adopt this design in order to lower the capacitance between the gate line and the common electrode and to increase transistor speed, as Kim II teaches.

145. In my opinion, a POSITA would also recognize that the solution disclosed in Kim II would be particularly advantageous to combine with the teachings of Kim. Kim II specifically identifies that capacitance issues are especially significant in in-cell panels employing an "in-plane" structure—where both the pixel electrodes and common electrodes are positioned on the same side of the liquid crystal layer—and expressly notes that such capacitance issues can "become a big problem." Kim II at [0092]. Kim, in turn, discloses a panel utilizing this very "in-plane" structure. See Kim at [0069], Fig. 9. Thus, a POSITA considering Kim's disclosure would appreciate that Kim II's solution is not only compatible with, but especially well-suited for, addressing the challenges presented in Kim's structure.

h) Element [1-H]

146. In my opinion, Kim discloses and renders obvious "segment electrodes included in one of the common electrodes are connected by at least one of the touch lines."

147. Kim specifically discloses that the touch signal lines can be connected to each ITO line (corresponding to '025 patent's segment electrode) within a particular touch electrode (corresponding to '025 patent's common electrode), while remaining insulated from other touch electrodes. For example, Kim explains that "the first touch signal line 124a may be connected to the first touch electrode 116a, but may be insulated from the other touch electrodes 116." See Kim at [0121], [0122]; *see also* Kim, Fig. 7 (showing touch line 124a and 124b connecting to only one of the two depicted touch electrodes 116a and 116b of the plurality of touch electrodes 110); Fig. 8 (same).

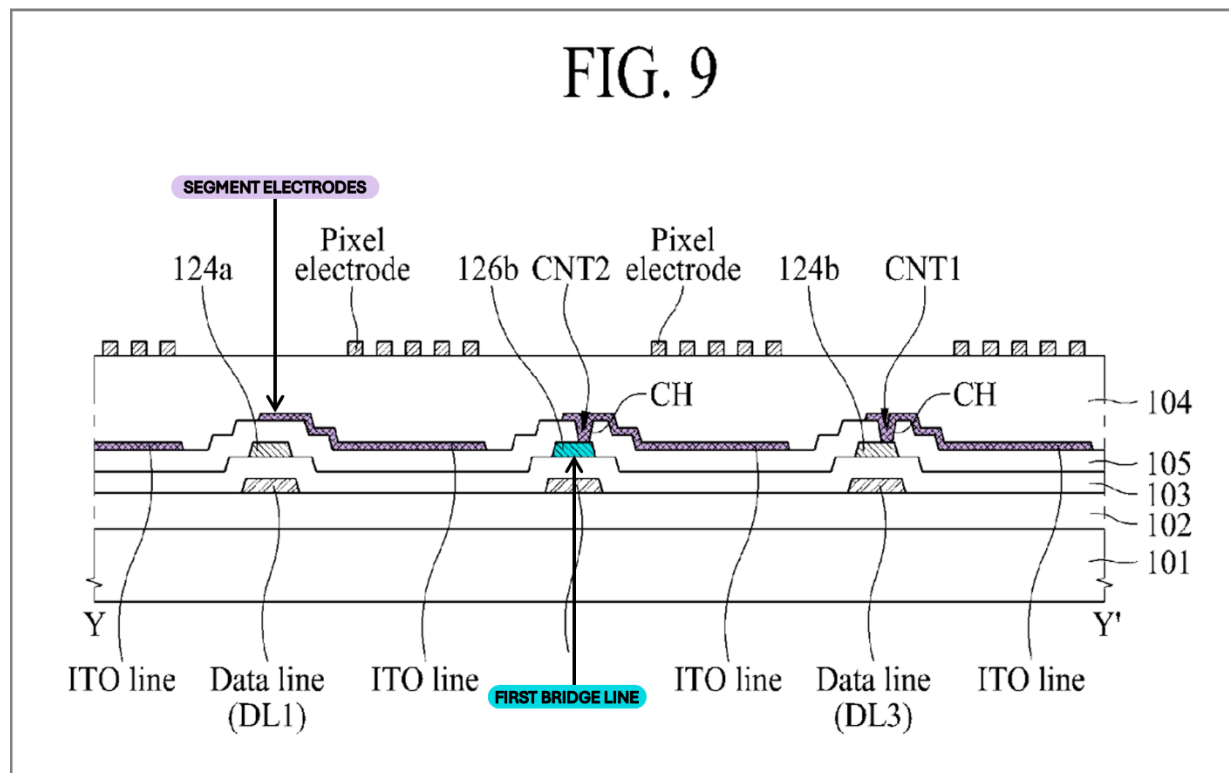
i) Element [1-I]

148. In my opinion, Kim discloses and renders obvious "the first bridge line and each of the two of the segment electrodes are connected via a contact hole."

149. In particular, with respect to Kim's second embodiment, Kim describes that its connecting lines—functioning as the '025 patent's bridge lines—are connected to each of the ITO lines (corresponding to '025 patent's segment electrodes) through contacts referred to as CNT2. For example, Kim explains that the first touch electrode 116a is connected to the first connecting lines 126a through multiple second contacts CNT2, with each contact CNT2 linking a single ITO line to a single first touch signal line 124a. Kim at [0126]; [0128] (disclosing

the same regarding a second connecting line connecting to the ITO lines of a second touch electrode); *see also* Kim, Fig. 7 and Fig. 8 (connecting lines connected to at least two ITO lines).

150. Furthermore, Kim clarifies that these contacts (CNT2) are formed through contact holes, stating that “[c]ontacts CNT1 and CNT2 are located in respective contact holes CH in the insulation layer 105.” Kim at [0147]. This configuration is visually represented in Figure 9 of Kim, which shows the contact hole (labeled as CH) through which the (purple) ITO line is linked to the (cyan) connecting line 126b.



Kim, Fig. 9.

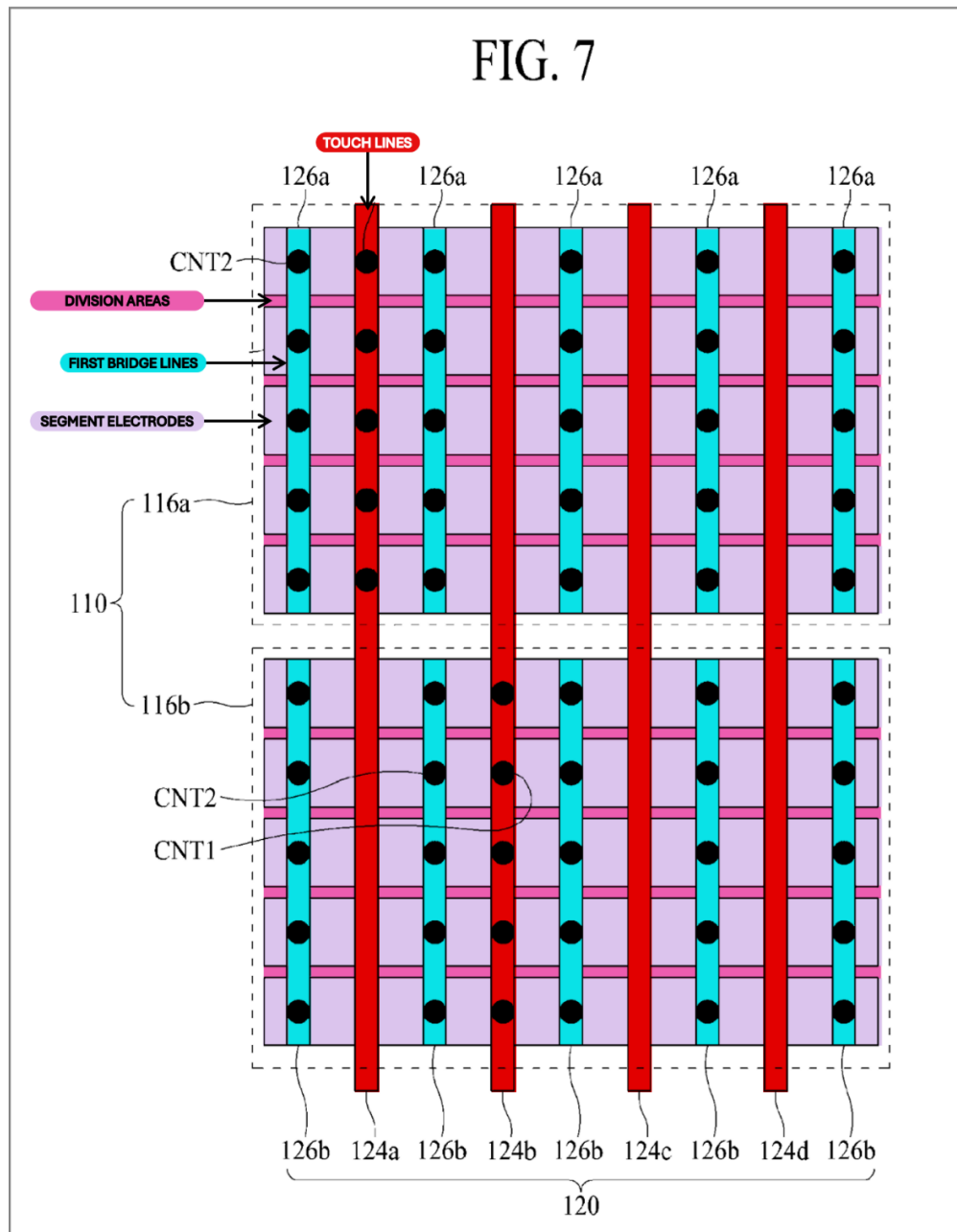
j) Element [1-J]

151. In my opinion, Kim discloses and renders obvious “the first bridge line extends in the second direction so as to overlap with the segment electrodes included in the one of the common electrodes, and be connected to the segment electrodes included in the one of the common electrodes.”

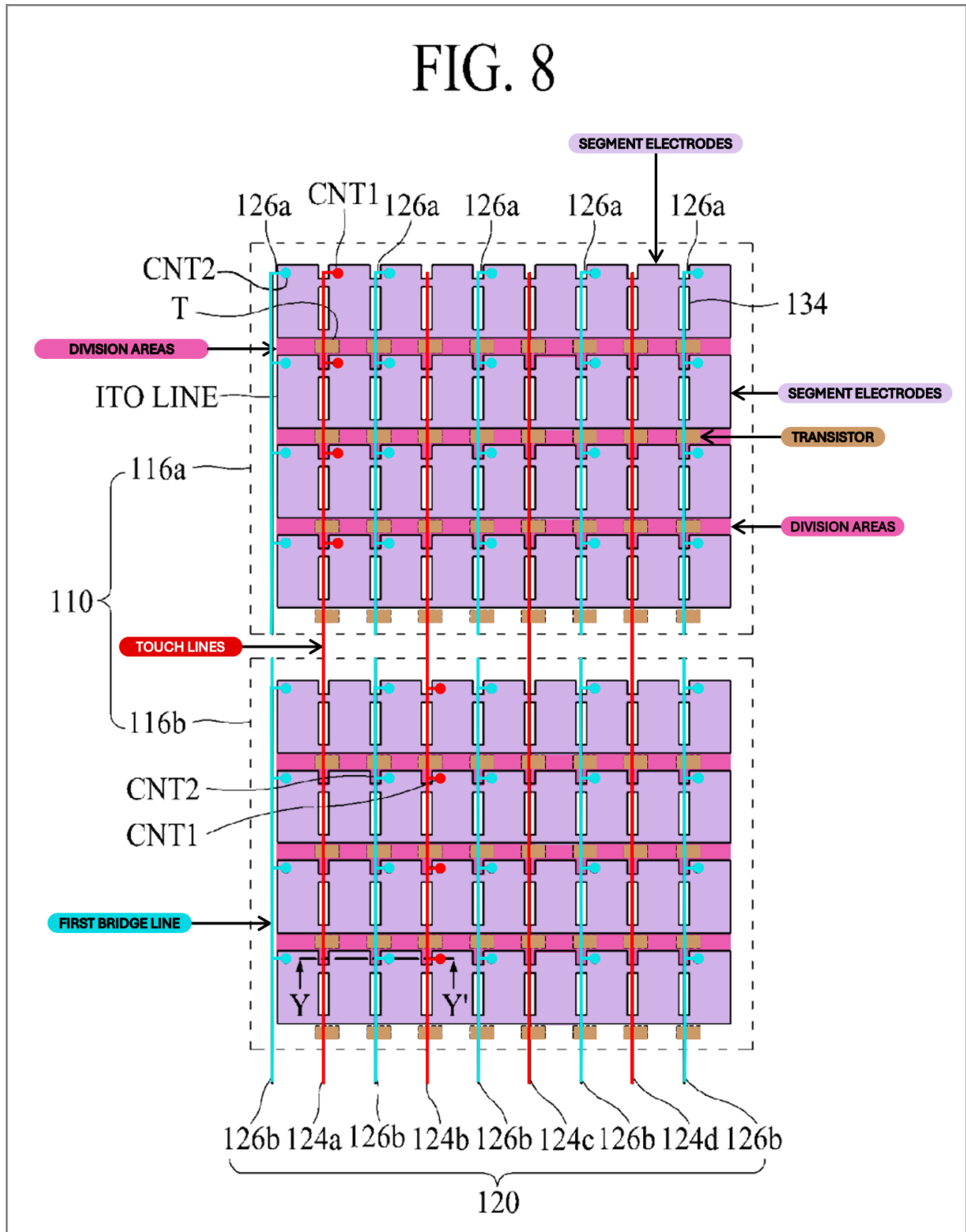
152. Kim describes the connecting line 126 (corresponding to '025 patent's bridge lines) as a conductive line that links different ITO lines (corresponding to '025 patent's segment electrodes) within a single “touch electrode 110” (corresponding to '025 patent's common electrode). Kim at [0120]. Kim further clarifies that each connecting line overlaps a particular touch electrode and, therefore, only the ITO lines (segment electrodes) that constitute that touch electrode (common electrode). See Kim at [0130] (“On the other hand, the plurality of first connecting lines 126a may overlap the first touch electrode 116a, but may not overlap other touch electrodes.”).

153. As discussed previously, these connecting lines are connected to the ITO lines within a particular touch electrode through contact holes. Kim at [0120] (“By connecting together different ITO lines, the connecting lines 126 reduces an internal load deviation of each of the touch electrodes 110, and a load deviation between the plurality of touch electrodes 110 is reduced.”). Kim also explains that these connecting lines extend in the vertical direction, which corresponds to the

second direction as defined in the Challenged Claims. Kim at [0118]. This arrangement is clearly depicted in Kim's Figures 7 and 8, reproduced and annotated below, where the (cyan) connecting lines extend vertically, overlapping and connecting to the (purple) ITO lines of a common electrode.



Kim, Fig. 7.



Kim, Fig. 8.

154. In my view, these disclosures collectively demonstrate that Kim teaches, or at least renders obvious, every aspect of this claim limitation.

2. Dependent Claim 2

155. Claim 2 of the '025 patent depends from Claim 1 and recites “[t]he in-cell touch panel according to claim 1, wherein the first bridge line is formed in a different layer from the common electrode.”

156. Claim 1 is disclosed and rendered obvious by Kim and Kim II, for at least the reasons discussed above.

157. In my opinion, Kim also teaches and renders obvious “wherein the first bridge line is formed in a different layer from the common electrode.” Kim expressly teaches this limitation. Specifically, Kim states “[t]he ITO lines are located on a different metal layer than the connecting lines 126 and touch signaling lines 124.” Kim at [0147]; *see also* Fig. 9.

3. Dependent Claim 3

158. Claim 3 of the '025 patent depends from Claim 1 and recites “[t]he in-cell touch panel according to claim 1, wherein the first bridge line is formed in a same layer as the touch line.”

159. Claim 1 is disclosed and rendered obvious by Kim and Kim II, for at least the reasons discussed above.

160. In my opinion, Kim teaches and renders obvious “wherein the first

bridge line is formed in a same layer as the touch line.” Kim expressly teaches this limitation. Specifically, Kim discloses “[t]ouch signaling lines 124 and connecting lines 126 are located in an intermediate metal layer formed on the passivation layer 103.” Kim at [0146].

4. Dependent Claim 6

161. Claim 6 of the '025 patent depends from Claim 1 and recites “[t]he in-cell touch panel according to claim 1, wherein the first bridge line overlaps with the data line in a planar view.”

162. Claim 1 is disclosed and rendered obvious by Kim and Kim II, for at least the reasons discussed above.

163. In my opinion, Kim teaches and renders obvious “wherein the first bridge line overlaps with the data line in a planar view.” Kim expressly teaches this limitation. Specifically, Kim teaches “[t]he connecting line 126b is located over and overlaps with another data line DL2.” Kim at [0146]. *See also* Kim, Fig. 9 (shows that connecting line 126b is directly above data line DL2 when viewed from the planar view angle of Figure 9).

5. Dependent Claim 9

164. Claim 9 of the '025 patent depends from Claim 1 and recites “[t]he in-cell touch panel according to claim 1, wherein a plurality of the first bridge lines are provided in the one of the common electrodes.”

165. Claim 1 is disclosed and rendered obvious by Kim and Kim II, for at least the reasons discussed above.

166. In my opinion, Kim teaches and renders obvious “wherein a plurality of the first bridge lines are provided in the one of the common electrodes.” Kim expressly teaches this limitation. Specifically, Kim discloses that “each of the plurality of touch electrodes 110 may be connected to a plurality of connecting lines.” Kim at [0120]; *see also* [0126] (“A plurality of connecting lines 126 may be disposed to overlap each of the plurality of touch electrodes 110.”). Further, as shown in Kim’s Figures 7 and 8, Kim discloses that there is a plurality of connecting lines 126 connecting the ITO lines of a single common electrode.

B. Ground 2 – Claims 4, 5, and 8 are Obvious in View of Kim in Combination With Kim II and Yoshida

167. In my opinion, Kim alone and in combination with Kim II and Yoshida renders Dependent Claims 4, 5, and 8 of the ’025 patent obvious. Claim 8 introduces “second bridge lines” that laterally bridge common electrodes, in contrast with the “first bridge line” discussed above. which connects segment electrodes. *See* Section X.A.1.j. In my opinion, a POSITA would have been motivated to combine the teachings of Kim and Kim II with Yoshida, which discloses a similar in-cell touch panel incorporating spare touch lines that can be advantageously used for repair purposes. Additional details regarding the

motivation for a POSITA to combine these references are discussed in the analysis below.

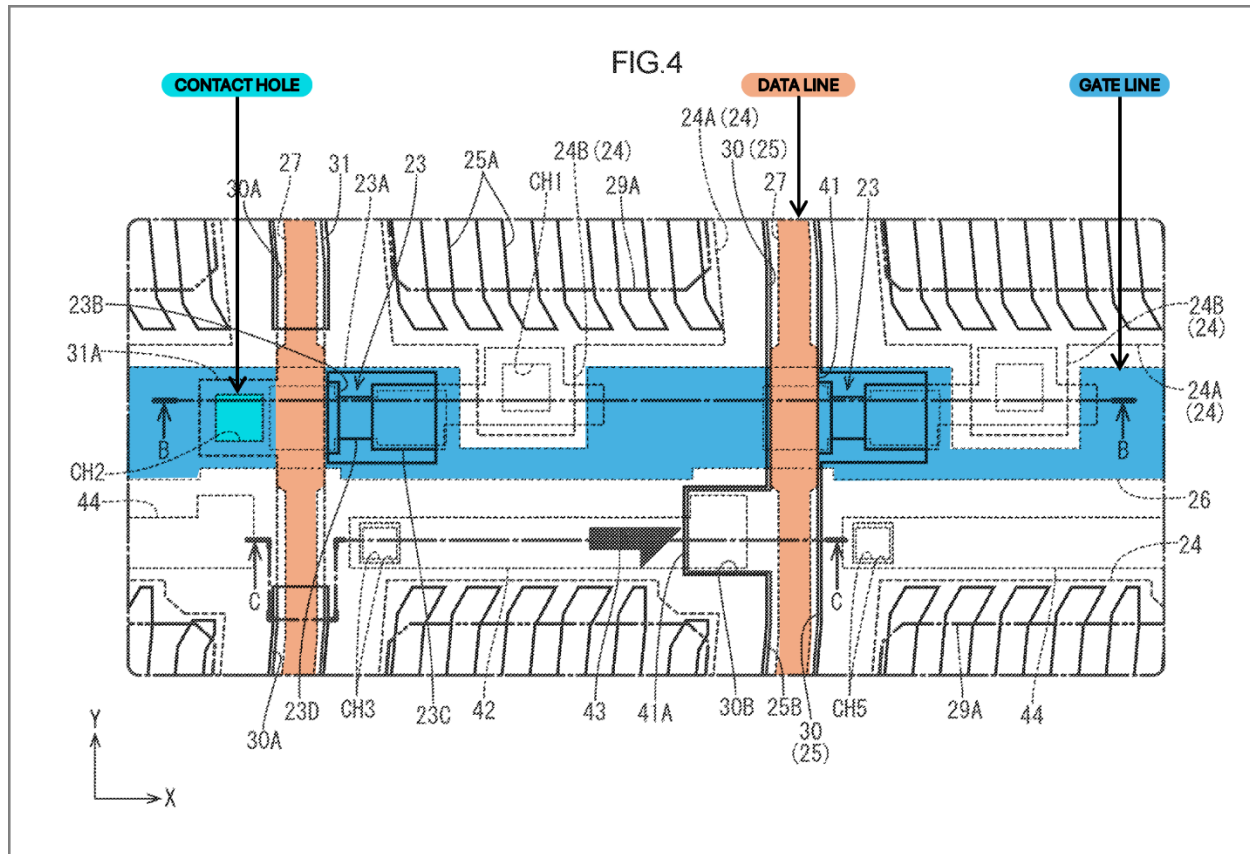
1. Dependent Claim 4 and 5

168. Claim 4 depends from Claim 1 and further requires “wherein the contact hole overlaps with the gate line in a planar view,” while Claim 5 depends from Claim 1 and adds the limitation “wherein the contact hole does not overlap with the data line in a planar view.”

169. Claims 4 and 5 are disclosed and rendered obvious by Kim and Kim II, for at least the reasons discussed above.

170. In my opinion, Kim combined with Yoshida also teach and render obvious “wherein the contact hole overlaps with the gate line in a planar view,” and “wherein the contact hole does not overlap with the data line in a planar view.”

171. Although Kim does not specify whether the contact holes for connecting lines 126 overlap the gate line, Yoshida discloses a contact hole (CH2) that connects the touch line to the touch electrode 30. *See* Yoshida at [0034], Translation at [0022]. As shown in Figure 4, this (cyan) contact hole CH2 is both positioned over the gate line and offset from the data line, as required by Claims 4 and 5:



Yoshida at [0034], Fig. 4; Translation at [0022], Fig. 4.

172. In my opinion, it would have been obvious to a POSITA to implement similarly positioned contact holes for Kim's connecting lines, as these lines are arranged and connected to the same electrodes as the touch lines. See Kim at [0118]. Consistent with the '025 patent's description—which does not attribute any particular technical advantage to this placement—a POSITA would have recognized that adopting such an offset contact hole arrangement, as taught by Yoshida, would have been a routine design choice readily implemented without difficulty. See '025 patent, 11:52–55.

173. Furthermore, a POSITA would have been recognized that this placement provides an advantage that would reduce the possibility of manufacturing defects. Specifically, a POSITA would recognize that, unlike the gate line, Kim's data line is higher in the layer stack used to make the display substrate, and thus closer to the touch lines and the connecting line, i.e., first bridge lines that exist in the same layer as the touch lines. *See, e.g.*, Kim at Fig. 9. A POSITA would therefore recognize positioning the contact hole in a location that is not directly over the data line would minimize the possibility that a faulty etch or photolithography process could lead to a short circuit between the connecting line and the nearby data line. Accordingly, a POSITA would have been motivated to use this placement to reduce the risk of shorting at the contact hole between the first bridge line and the underlying data line. *See also* Section X.B.2.c (discussing additional motivation to combine).

2. Dependent Claim 8

174. In my opinion, Claim 8 is obvious in view of Kim combined with Kim II and Yoshida.

a) Element[8-PRE]

175. The preamble of Claim 8 recites "[t]he in-cell touch panel according to claim 1." As I explained above, in my opinion, Kim, alone and in combination with Kim II, renders Claim 1 obvious. *See* Section X.A.1.

b) Element [8-A]

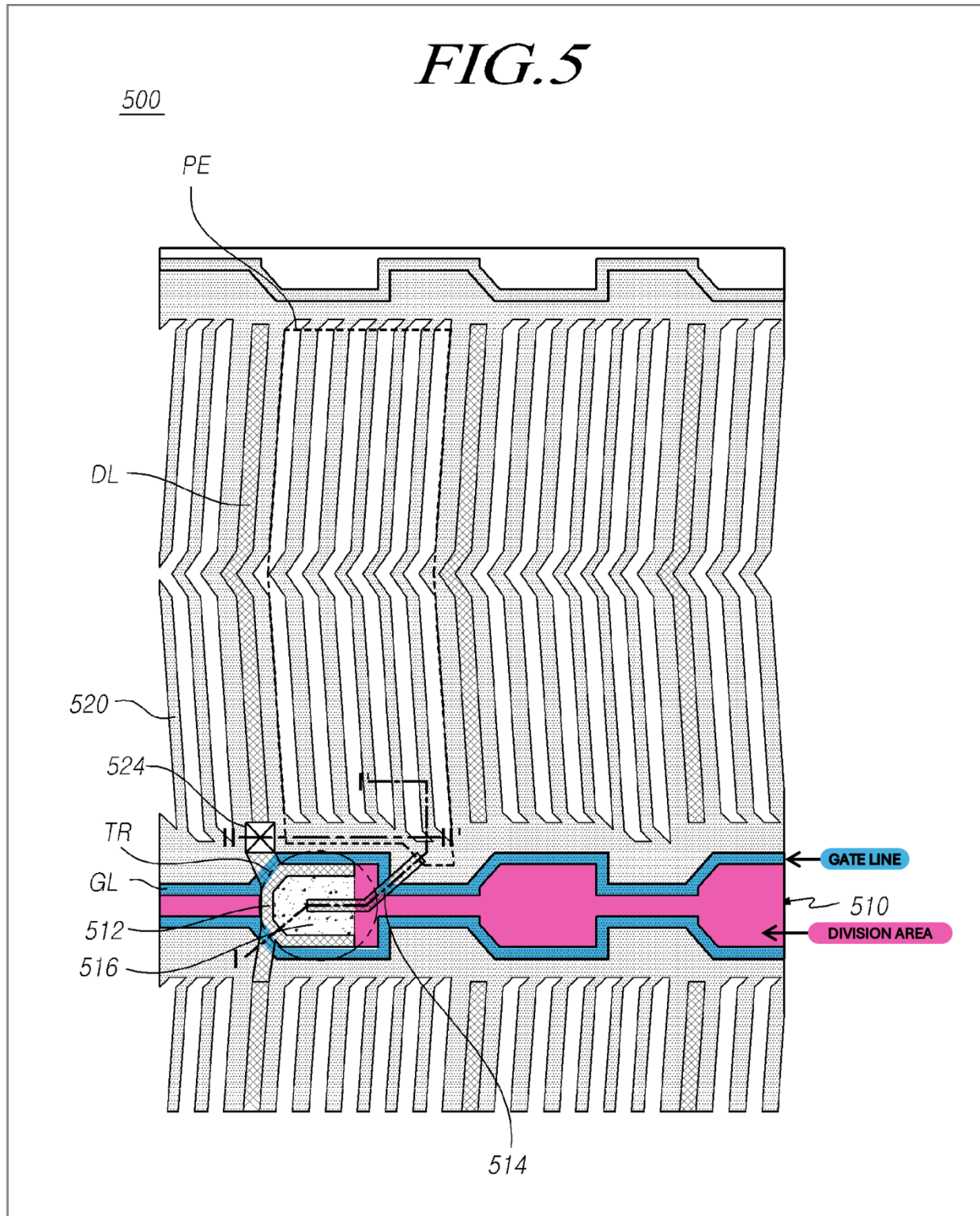
176. In my opinion, Kim II discloses and renders obvious this element of Claim 8: “wherein two of the common electrodes adjacent in the second direction are separated from each other with the separation area on the gate line.”

177. Specifically, Kim II describes a separation distance “D2,” between touch electrodes and identifies this “separation area” as “separation space 430a,” with reference to Kim II’s Figures 3 and 4. Separation space 430a is distinct from separation space 430b, which is the separation area within a touch electrode itself, rather than the area in between touch electrodes. Kim II at [0060], [0065].

178. Kim II drops this distinction when discussing the more specific embodiment of Figure 5. In particular, for that embodiment, Kim II refers to both types of separation spaces as “separation space[s] 510,” which are “formed in the direction parallel to the gate lines GL ***regardless of being inside the touch electrode and at an outer periphery of the touch electrode.***” Kim II at [0089] (emphasis added). Thus, in connection with Figure 5, Kim II teaches that these separation spaces 510 are the same regardless of whether they are a gap between rows within a common electrode, or a gap between different common electrodes.

179. Kim II also teaches that the preferred placement of the gate line is within the “separation space 510”. Kim II at [0090]; *see also* Section X.A.1.d. Therefore, Kim II teaches that the gate line is located within separation space 510,

whether that space is between rows within a common electrode or between adjacent common electrodes. This is shown in Figure 5, produced below:



Kim II, Fig. 5.

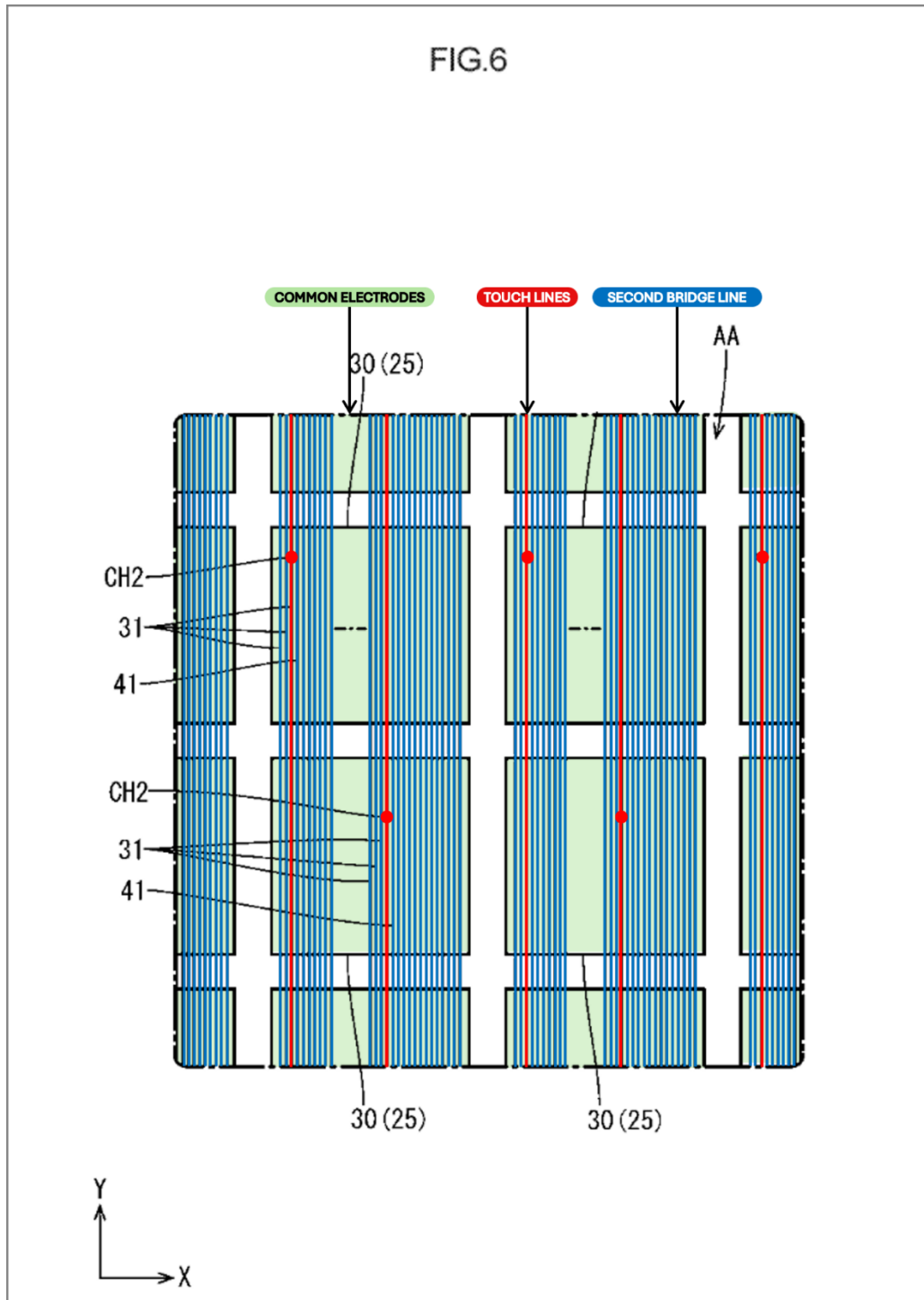
c) Element [8-B]

180. In my opinion, Yoshida discloses and renders obvious this element of Claim 8: “the in-cell touch panel includes a second bridge line laterally bridging the two of the common electrodes adjacent in the second direction across the separation area.”

181. The “second bridge line” described in the ’025 patent is a dummy line. ’025 patent, 12:16-17.

182. In my opinion, Yoshida discloses such a “second bridge line” that literally bridges two common electrodes adjacent in the second direction, *i.e.*, vertically, across the separation area described above. Specifically, Yoshida teaches these dummy “second bridge lines” as the particular “spare touch line[s] 41,” that are overlapping the touch electrodes, in contrast to the spare touch lines that are positioned between touch electrodes, as discussed in the grounds below. Specifically, Yoshida explains that when there are more data lines under a touch electrode than there are touch electrodes in a column, the amount of overlapped data lines will outnumber the amount of touch lines needed to connect to the touch electrodes in a particular column. Yoshida at [0035]; Translation at [0022]. Accordingly, Yoshida’s design requires that each data line is nonetheless covered by a touch line, causing there to be excess touch lines 31 that become spare touch lines 41. Yoshida at [0035]; Translation at [0022]. Yoshida explains that these

spare touch lines extend “generally ... in the Y-axis direction in parallel with the source lines 27,” *i.e.*, in the claimed second direction. Yoshida at [0035]. Yoshida further explains that these excess spare touch lines 41 also overlap with Yoshida’s common electrodes 30, thereby bridging the “separation area” between such common electrodes. *See* Yoshida at [0035] (“There are also the spare touch lines 41 overlapping the touch electrodes 30.”). Further, Yoshida’s Figure 6 shows these (blue) excess spare touch lines 41 bridging the gap between vertically adjacent touch electrodes:



Yoshida, Fig. 6; *see also* Translation, Fig. 6.

183. A POSITA would have been motivated to implement Yoshida's spare

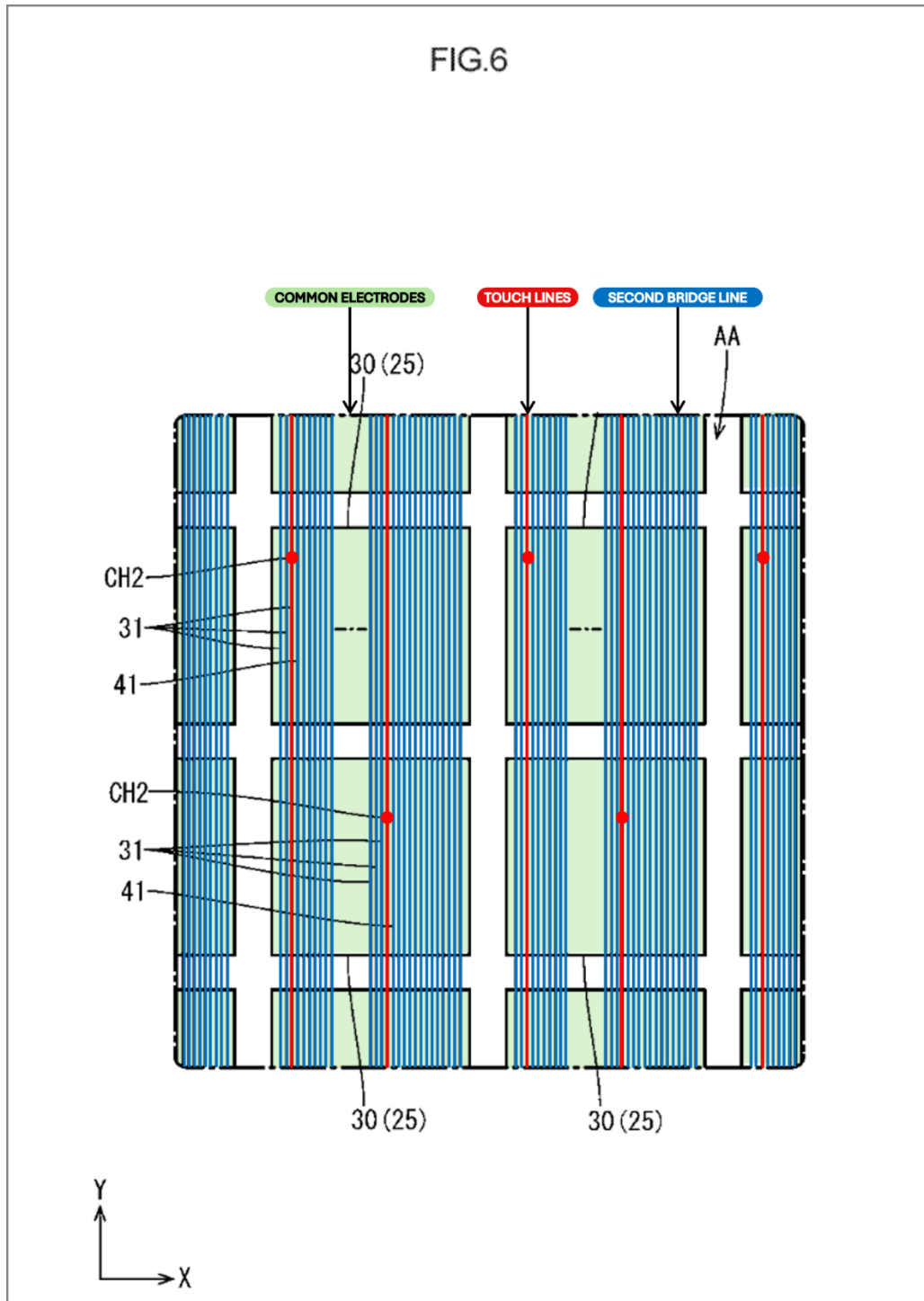
touch lines in a design for an in-cell touch panel. Specifically, as Yoshida explains, these spare touch lines provide the benefit of permitting repairs when the main touch line 31 becomes disconnected. Yoshida at [0035]; Translation at [0023]. Yoshida explains at length how this can be accomplished, particularly in connection with Figure 7. *See, e.g.*, Yoshida at [0036]-[0037]. Additionally, a POSITA would recognize that over the data lines that do not have an operating touch line, Yoshida's excess spare touch lines help to maintain uniformity across the display. *See* Yoshida at [0035]; A POSITA would also recognize that the ability to repair potentially faulty touch lines would improve manufacturing yield and likely profits, and therefore be motivated to include such spare touch lines in a design based on the teachings of Kim and Kim II.

184. Further, a POSITA would recognize that Yoshida discloses the same type of device as Kim and Kim II, including a substantially similar structure. For example, like Kim and Kim II, Yoshida's touch panel includes thin film transistors, pixel electrodes, horizontal gate lines, vertical data lines, touch electrodes, and touch lines. Yoshida at [0027]- [0028]. Accordingly, a POSITA would recognize that Yoshida's teachings are compatible with Kim and Kim II and would have had every expectation that the spare touch lines (*i.e.*, excess touch lines) could be implemented in a design based on those teachings, described above.

d) Element [8-C]

185. In my opinion, Yoshida discloses and renders obvious this element of Claim 8: “the second bridge line is not electrically connected to any of the two of the common electrodes.”

186. First, as shown in Figure 6, Yoshida’s spare touch lines, pictured in blue, are not connected to any of the several depicted common electrodes (which number more than two), as evidenced by the fact that there are no “dots” representing connections on any of the spare touch lines:



Yoshida, Fig. 6.

187. Second, Yoshida teaches that the spare touch lines 41 are provided in a different layer than the common electrode/touch electrodes 30/25 and that there

is an insulating film 39 between them. *See* Yoshida at [0033], Fig. 5; Translation at [0021], Fig. 5. Yoshida explains that the number of data lines under a touch electrode may exceed the number of touch lines needed to connect to the number of touch electrodes in a particular column of touch electrodes, which will result in excess spare touch lines that are not connected to touch electrodes, and instead function as the dummy “second bridge line[s].” *See* Yoshida at [0035]; Translation at [0023]. Further, Yoshida teaches that these excess spare touch lines 41 are “not connected to the touch lines 31” which are themselves connected to the common/touch electrodes. Yoshida at [0027]; Translation at [0015]. Accordingly, a POSITA would recognize that Yoshida’s spare touch lines are therefore not connected to the touch electrodes, and the insulating film prevents the spare touch lines from electrically connecting to the common electrodes, as that is the purpose of an insulating film.

188. Although Yoshida teaches a way to establish an electrical connection between the excess spare touch line to the common electrode, a POSITA would recognize the obvious fact that, absent the need for a repair, such a connection would not be made, and the spare touch line would remain disconnected from the common electrode and maintaining uniformity across the display, as explained above.

C. Ground 3 – Claim 18 is Obvious in View of Yoshida Alone.

189. In my opinion, Claim 18 is obvious in view of Yoshida alone. In contrast with Claim 1, Claim 18 does not limit its scope to include segment electrodes or bridge lines, but instead introduces “dummy touch lines” positioned between horizontally adjacent common electrodes. As explained below, Yoshida discloses such “dummy touch lines” in the form of its spare touch lines 41.

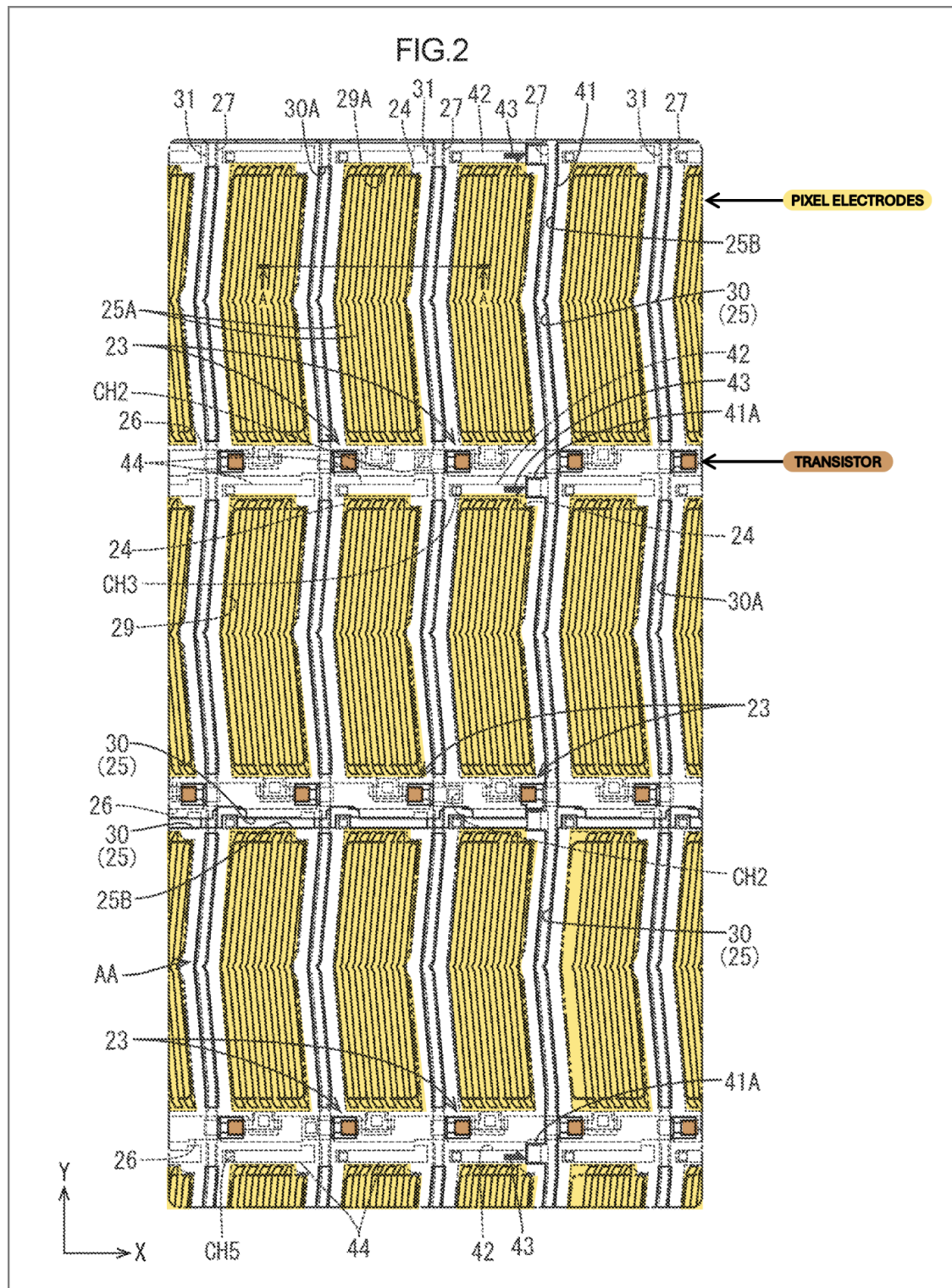
1. Independent Claim 18

190. In my opinion, Yoshida alone renders obvious Claim 18 of the '025 patent.

a) Element [18-PRE]

191. In the event that the Claim 18 preamble is found to be limiting, in my opinion, Yoshida discloses and renders obvious all requirements of the preamble.

192. For example, Yoshida discloses “an in-cell touch panel having an image display area made up of pixels arranged in a first direction and a second direction orthogonal to the first direction.” *See, e.g.*, Yoshida at [0026] (describing how a display “touch panel pattern for implementing the touch panel function is integrated (in-cell technology)”), [0024] (explaining that the panel is configured to display an image), [0028] (stating that the pixels and other components are “disposed orthogonal to (intersecting) each other”):

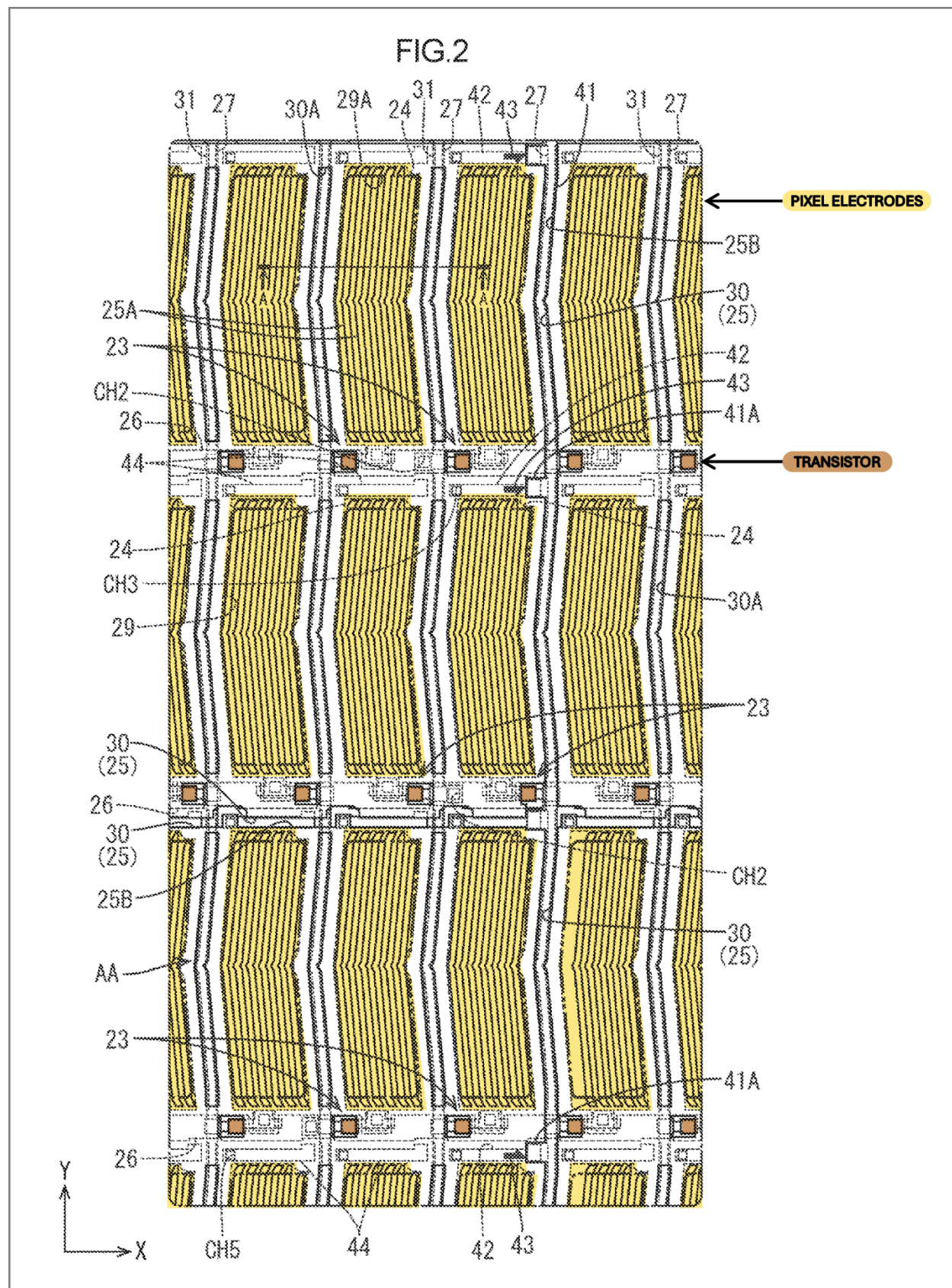


Yoshida, Fig. 2; [0029] (describing pixels portions as having an arrangement in the X and Y directions); Translation, Fig. 2, [0012], [0016], [0017].

b) Element [18-A]

193. In my opinion, Yoshida discloses and renders obvious the requirement that the touch panel includes “transistors and pixel electrodes respectively provided in the pixels.”

194. Yoshida specifically states that each pixel contains both a transistor and a pixel electrode. For instance, Yoshida explains that, “[o]n the inner surface side in the display region AA of the array substrate 21 of the liquid crystal panel 11, as illustrated in FIG. 2, thin-film transistors (TFTs; switching elements) 23 and pixel electrodes 24 are provided” in a pixel portion. Yoshida at [0028], [0029]; Translation at [0016], [0017]. As illustrated in Figure 2, each pixel includes a (brown) transistor 23 and a (yellow) pixel electrode 24.

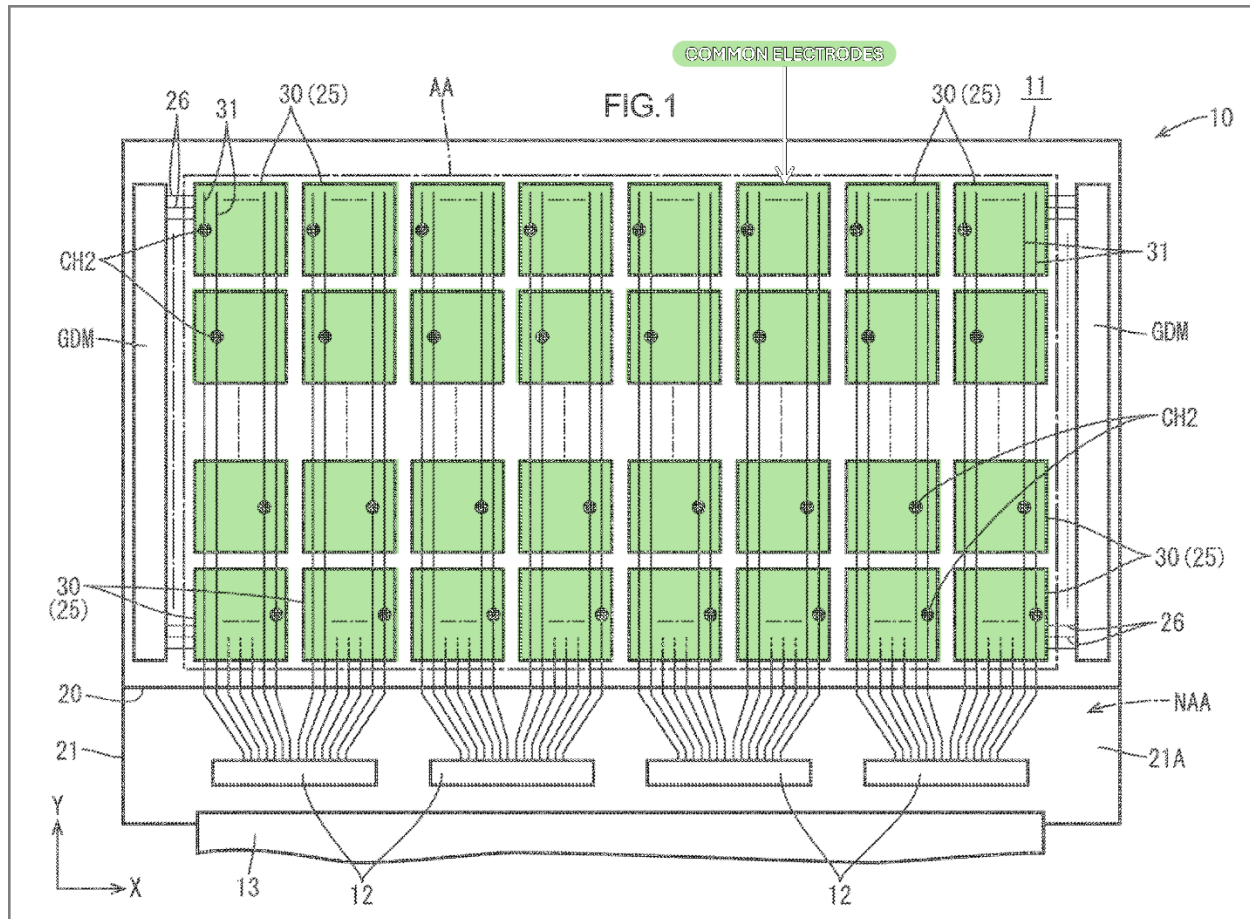


Yoshida, Fig. 2; Translation, Fig. 2.

c) Element [18-B]

195. In my opinion, Yoshida discloses and renders obvious the requirement that the touch panel comprises “common electrodes arranged in the first direction and the second direction, respectively facing one or more of the pixel electrodes and provided separately from each other.”

196. Although Yoshida refers to its “common electrode 25” in the singular, the specification makes clear that it is actually divided into multiple, electrically independent pieces—referred to as “touch electrodes 30” (*i.e.*, common electrodes)—by gaps called “partition openings 25B.” See Yoshida at [0030], Figs. 1, 3; Translation at [0018], Figs. 1, 3. As shown in Figure 1, Yoshida’s (green) touch electrodes 30 are arranged in both the first and second directions (*i.e.*, in rows and columns):



Yoshida, Fig. 1; Translation, Fig. 1; *See also* Yoshida at [0026] (explaining that touch electrodes 30 (*i.e.*, common electrodes) are “disposed side by side in a matrix”); Translation at [0014].

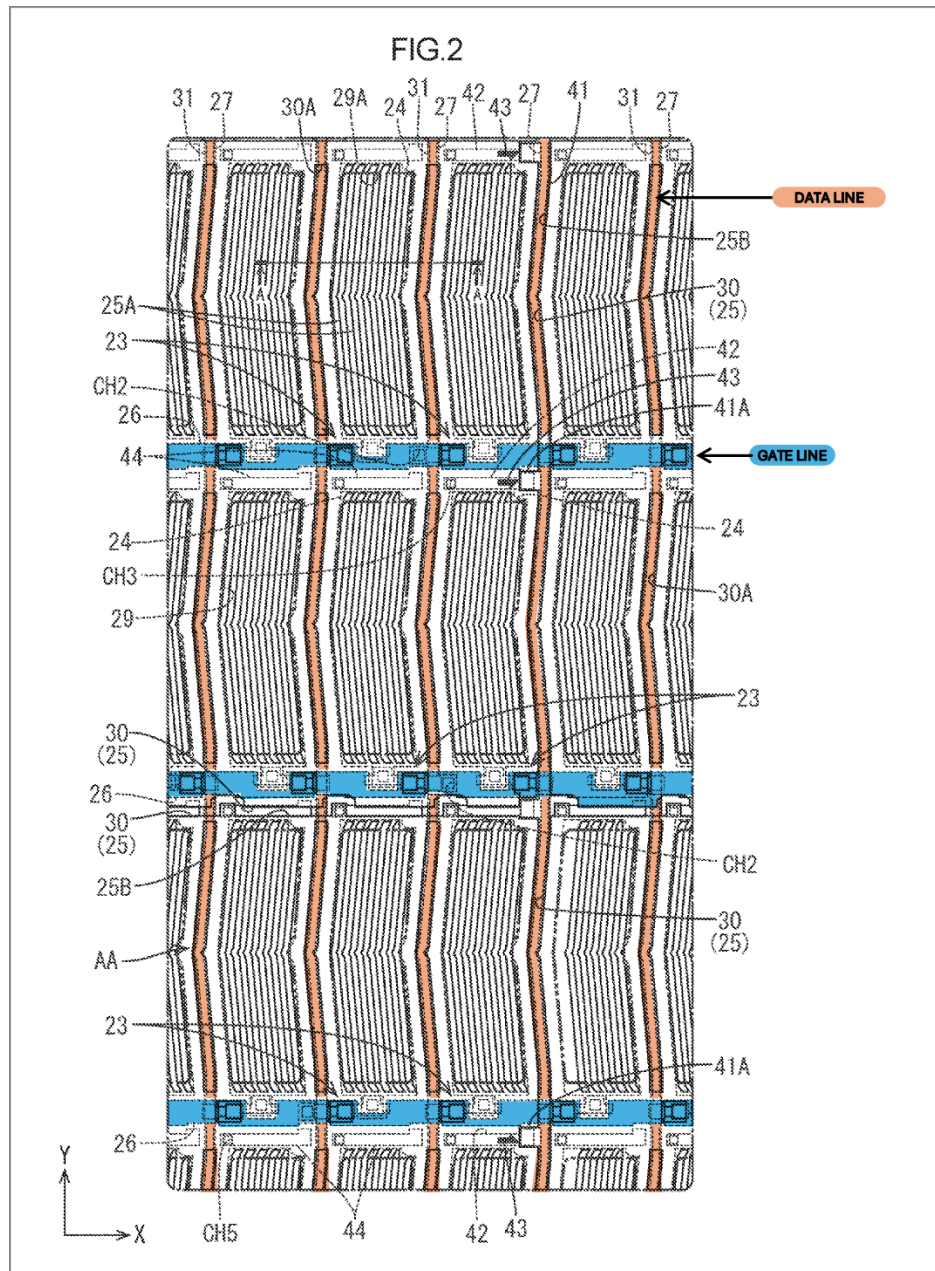
197. Yoshida also discloses that its common or touch electrodes 30 are positioned to face, or overlap, one or more pixel electrodes, as required by the claims. Yoshida explicitly states that “the common electrode 25 [composed of touch electrodes 30]...includes portions overlapping the pixel electrodes 24,” (specifically, pixel electrode body 24A which will be described later), and that these electrodes are “arranged in an area spanning over a number (such as several

tens) of pixel portions PX. *See* Yoshida at [0026], [0030]; Translation at [0014], [0018]; Figs. 1, 3.

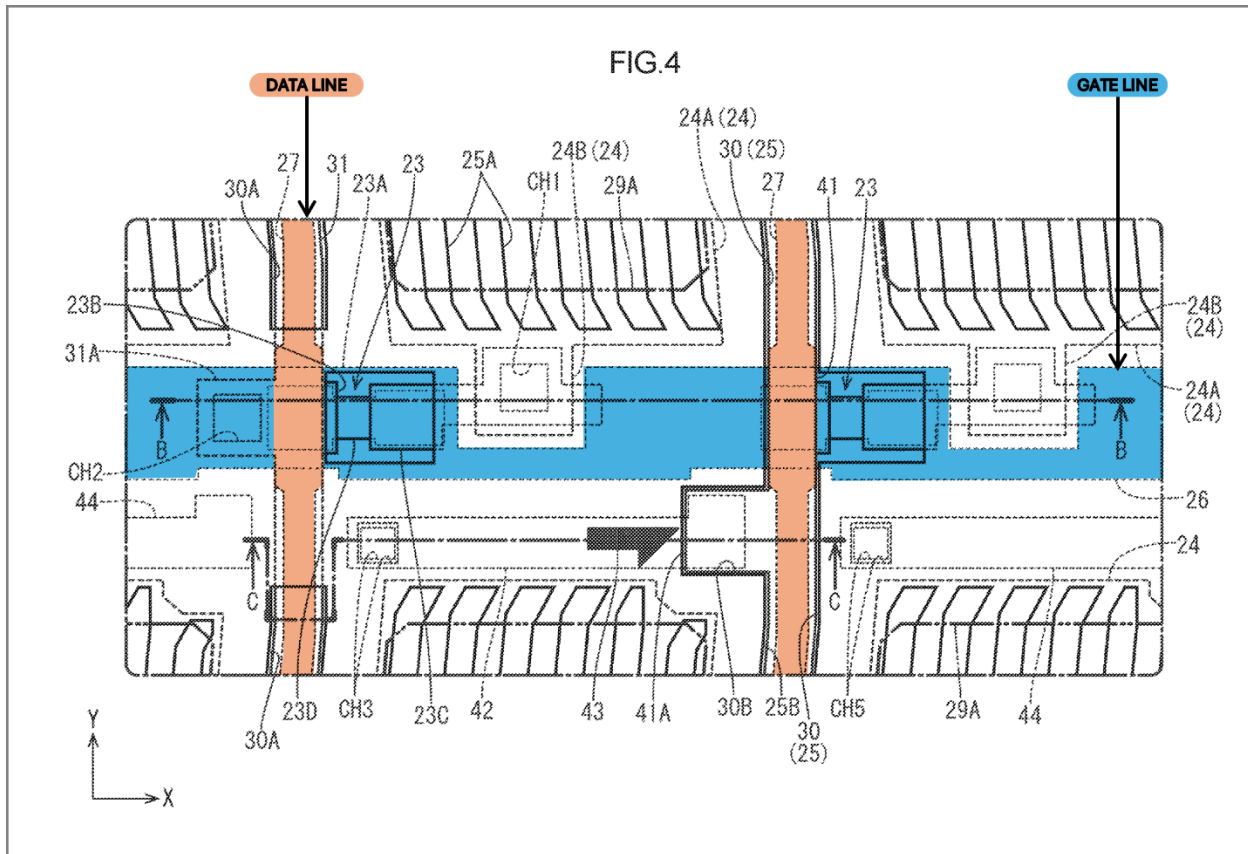
d) Element [18-C] and [18-D]

198. In my opinion, Yoshida discloses and renders obvious the requirement that the touch panel includes “gate lines that extend along the first direction and supply gate signals to the transistors respectively” and “data lines that extend along the second direction and supply data signals to the transistors respectively.”

199. Yoshida teaches that its panels incorporate “gate lines (scan lines) 26 and source lines (signal lines, data lines) 27,” which are arranged orthogonally to one another—meaning the gate lines extend along the first direction (X direction), while the data lines extend along the second direction (Y direction). *See* Yoshida at [0028]; *see also id.* (describing the orientation of the pixel electrodes relative to the gate and source lines), [0029], [0031]; Translation at [0016], [0017], [0019]. This arrangement is shown in Figures 2 and 4:



Yoshida, Fig. 2; Translation, Fig. 2.



Yoshida, Fig. 4; Translation, Fig. 4.

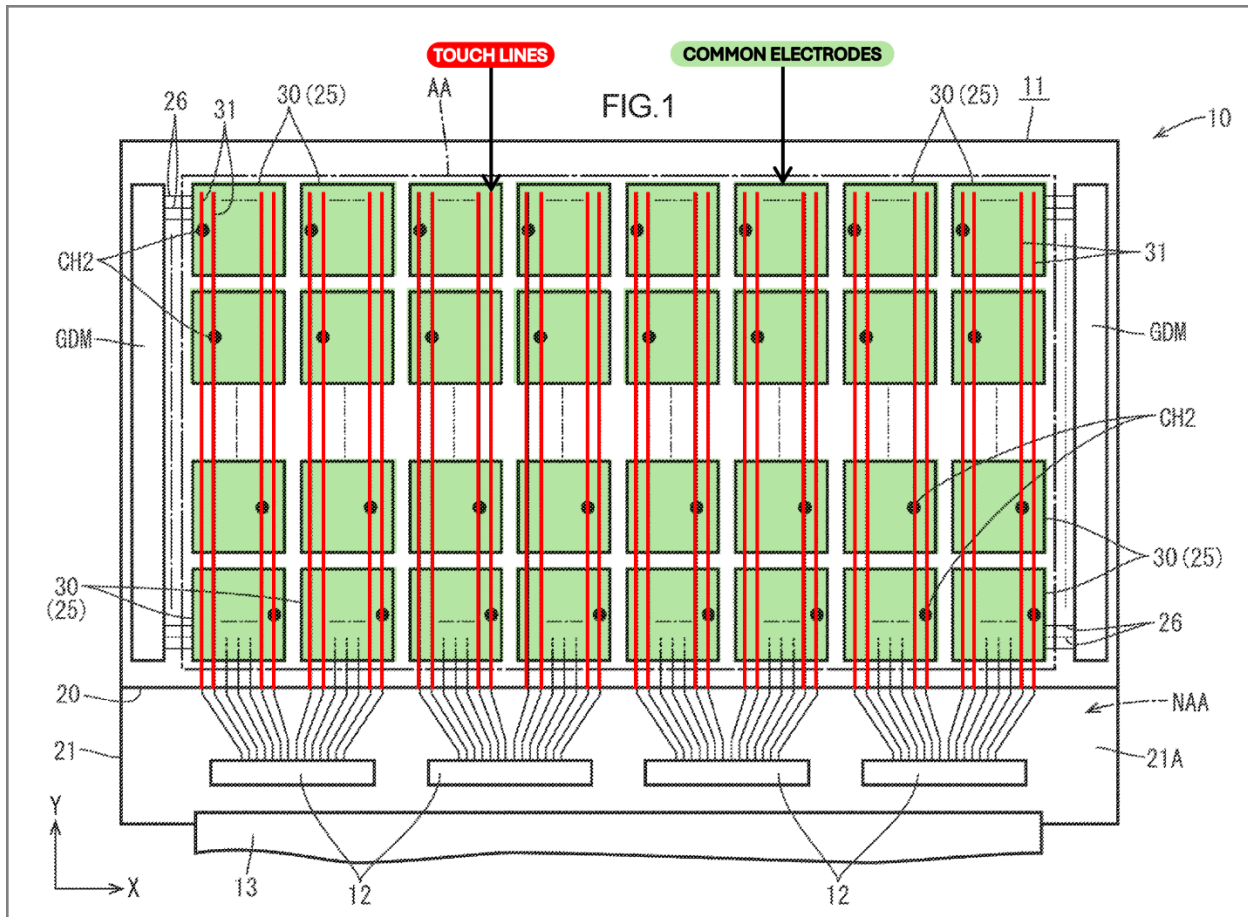
200. Yoshida further discloses that the gate lines supply gate signals to the transistors and that the data lines supply data signals to the transistors, as is obvious given their designation alone. *See* Yoshida at [0028]; Translation at [0016]. But, more specifically, Yoshida explains that “[t]he gate lines 26 and the source lines 27 are respectively connected to a gate electrode 23A and a source electrode 23B of the TFTs 23” which are “driven based on various signals supplied to the gate lines 26 and the source lines 27, and control the supply of potentials to the pixel electrodes 24.” *See* Yoshida at [0031], [0032]; Figs. 2, 4; Translation at

[0019], [0020], Figs. 2, 4.

e) Element [18-E] and [18-G]

201. In my opinion, Yoshida discloses and renders obvious the requirement that the touch panel includes “touch lines that extend along the second direction and are each connected to a corresponding one of the common electrodes,” as well as the requirement that “each touch line is connected with a corresponding one of the common electrodes arranged in the second direction.”

202. Specifically, Yoshida describes “touch lines (position detection lines) 31,” which “extend in the Y-axis direction, and are selectively connected to specific touch electrodes 30 among the touch electrodes 30 arranged in the Y-axis direction.” Yoshida at [0026]; Translation at [0014]. As illustrated in Figure 1, the (red) touch lines 31 run in the Y-axis direction and are each individually and selectively connected to one of the (green) touch electrodes 30 forming each column, with the connection points indicated by dots. See Yoshida at [0026], [0027]; Translation at [0014], [0015].



Yoshida, Fig. 1; Translation, Fig. 1. *see also* Fig. 2 (depicting touch lines 31);

Translation, Figs. 1, 2.

203. Thus, Yoshida's touch lines 31 both extend along the second direction (the Y direction) and are each connected to a corresponding common electrode (a single touch electrode 30, as shown by the dots). *Id.* For the same reasons, Yoshida also discloses that each touch line is connected with a corresponding one of the common electrodes arranged in the second direction.

f) Element [18-F]

204. In my opinion, Yoshida discloses and renders obvious that the touch

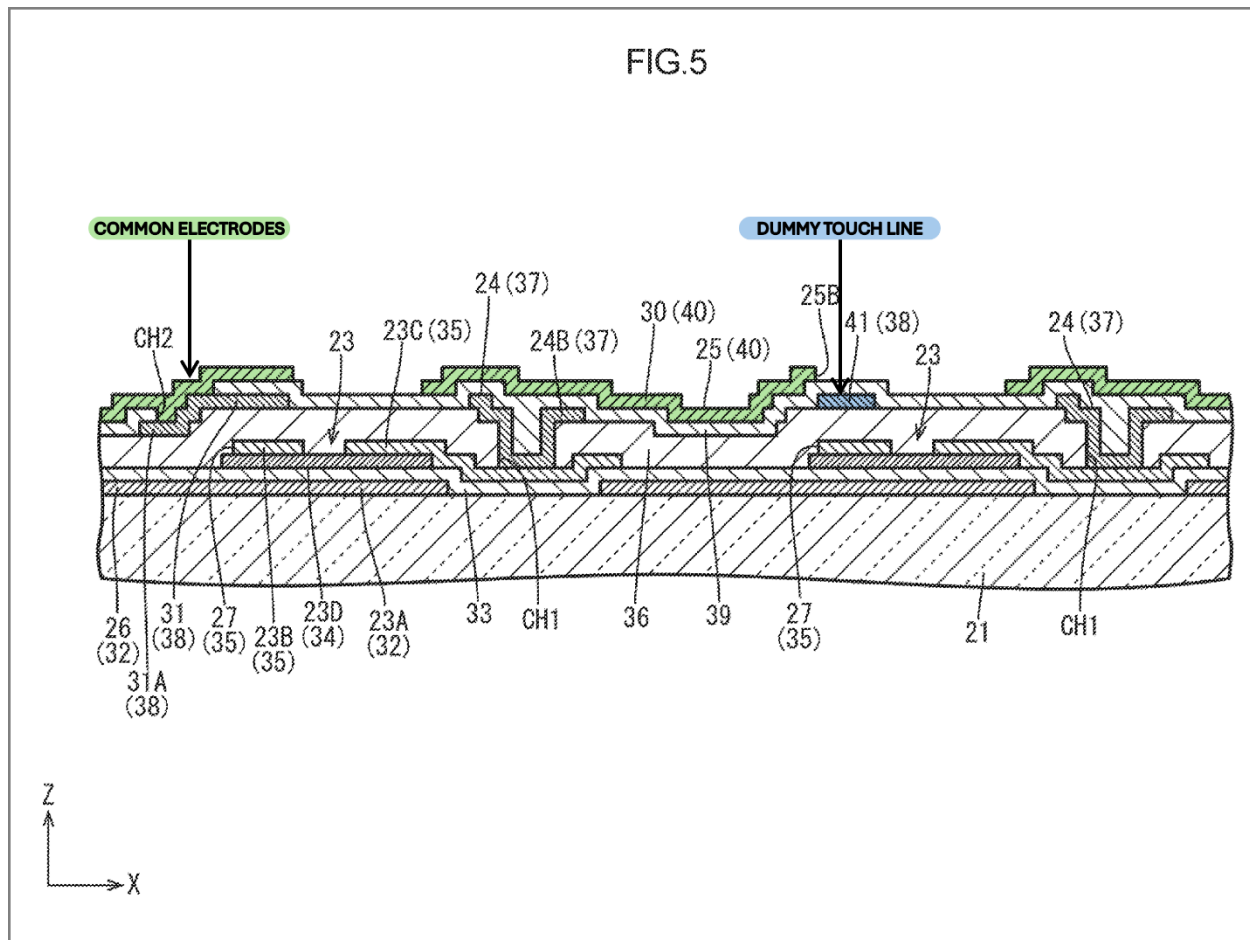
panel comprises “a dummy touch line that extends along the second direction, is formed in a same layer as the touch lines, and is electrically isolated from any of the common electrodes.”

205. Yoshida teaches these claimed “dummy touch lines” as “spare touch line 41” that are between common electrodes. These spare touch lines meet my proposed construction for “dummy touch line” explained in Section VIII.C.1 above. Specifically, the term “dummy touch line” should be construed to refer to a “line that does not carry a touch signal,” and Yoshida’s spare touch lines 41 do not carry such a touch signal. Yoshida explains that its spare touch lines are “excess touch lines” that are not needed to connect to a touch electrode, and so a POSITA would understand that they are in fact not connected to any such touch electrode. Yoshida at [0035]; Translation at [0023]. Indeed, Yoshida explains that the spare touch lines are “not connected to the touch lines 31” and thus, must also not be connected to touch electrodes 30, and so do not carry a touch signal; Yoshida at [0027]; Translation at [0015], [0023]. Nor does Yoshida ever provide any teaching that suggests the spare touch lines carry a touch signal in their disconnected state.

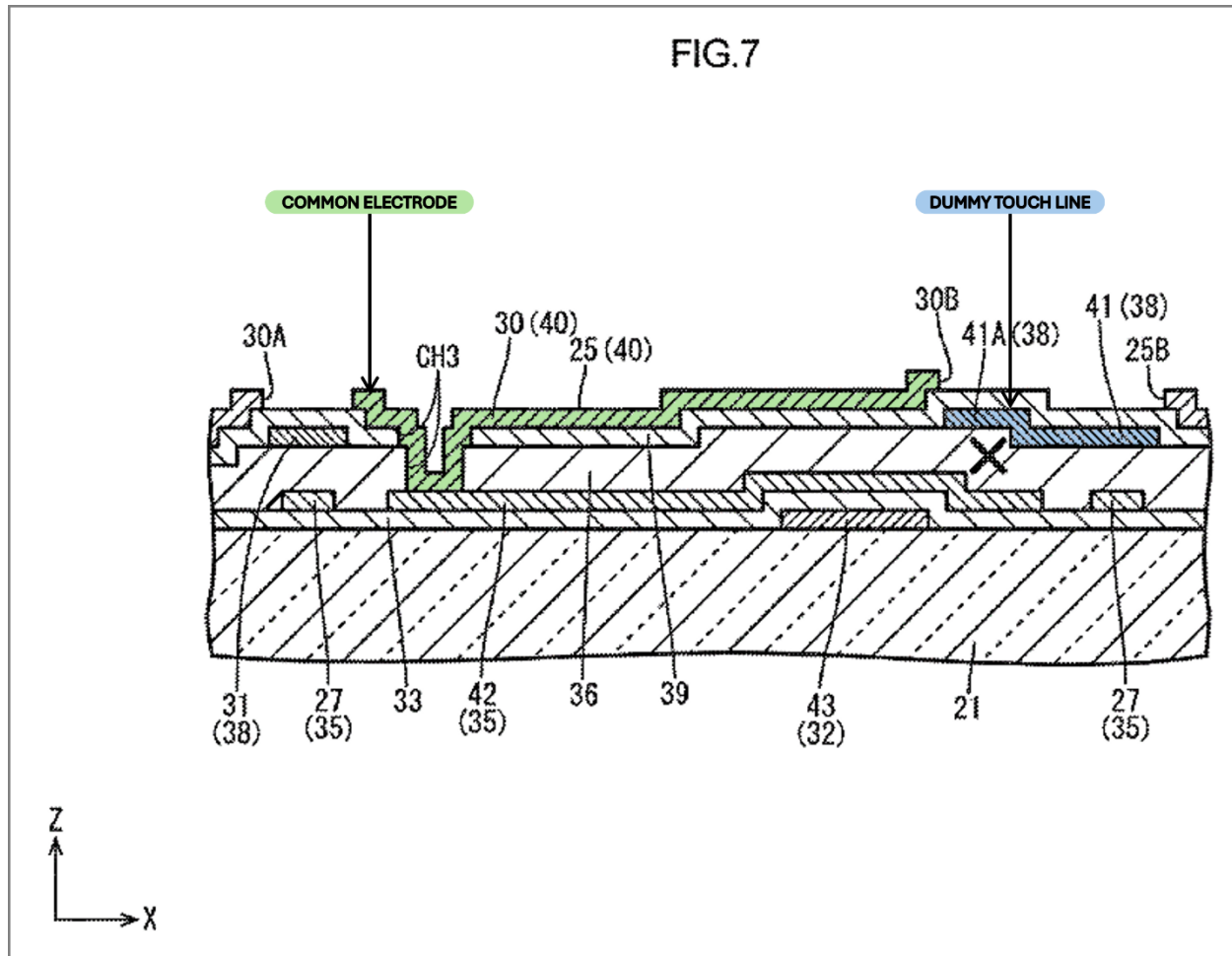
206. Rather, Yoshida explains that the purpose of these spare touch lines is to “enable[] a repair when a disconnection has occurred in the touch lines 31.” Yoshida at [0035]; Translation at [0023]. Yoshida teaches that making such a repair is necessary only when “a disconnection has occurred in the touch line 31.”

Yoshida at [0037]; Translation at [0025]. Yoshida teaches that making the repair involves connecting the spare touch line 41 to a touch electrode 30 by destroying the “first inter-layer insulating film 36 interposed in the overlapping parts between the first connection-enabling portion 42 and the spare touch line 41,” so that “the overlapping parts are short-circuited.” *Id.* But, again, if there is no disconnection, there is no need for this repair. And a POSITA would recognize that, because Yoshida teaches that there can be many spare touch lines per touch electrode (*see, e.g.,* Yoshida at [0035], Fig. 6; Translation at [0023]; Fig. 6), and there would almost certainly always be spare touch lines that were not connected to any touch electrode, even in panels where a repair proved necessary.

207. Yoshida’s figures depict these spare touch lines. Before any such repair is needed, as shown in Figure 5, the (blue) spare touch lines 41 are not connected with the (green) touch electrodes 30, and therefore cannot carry a touch signal:

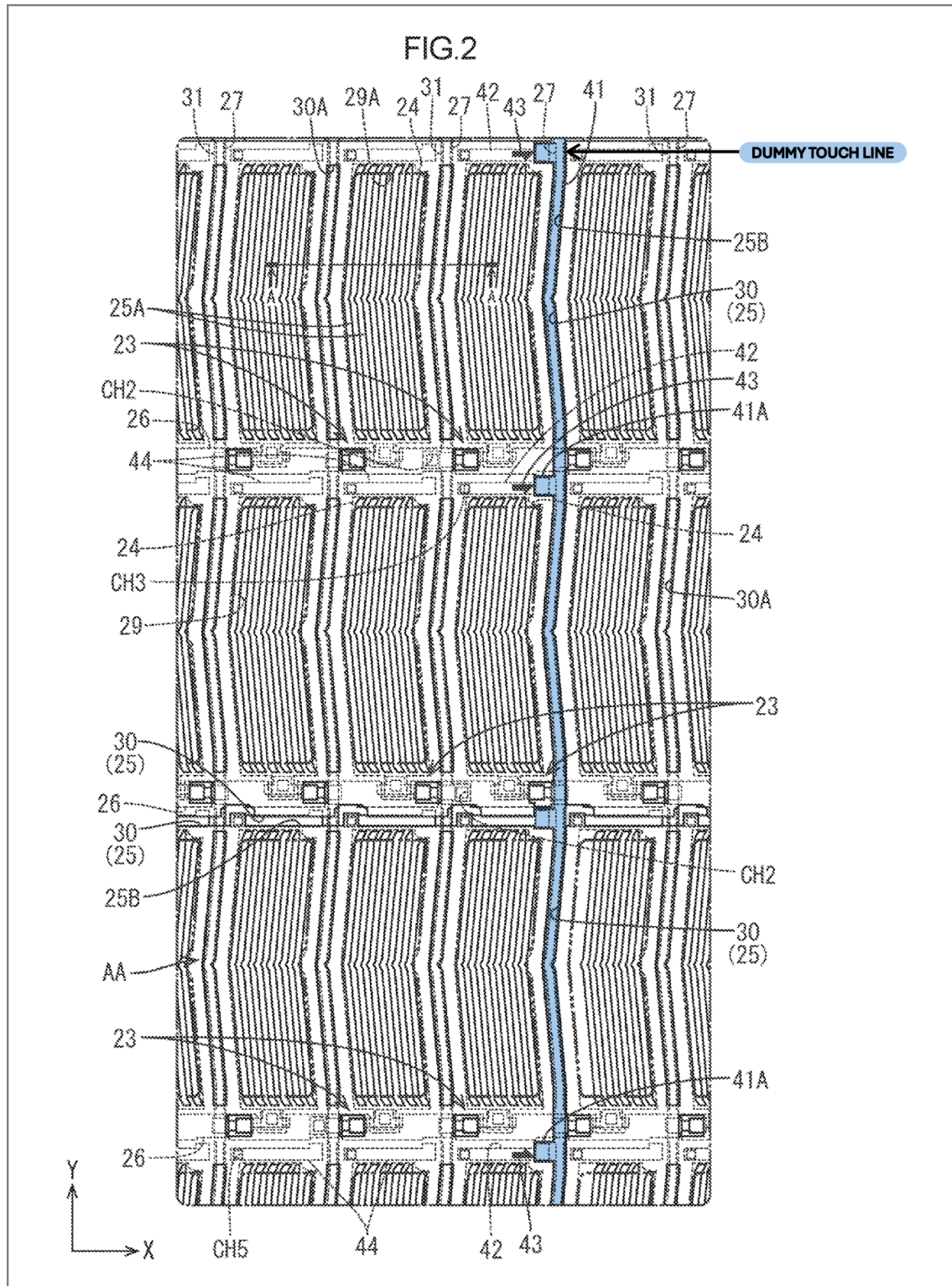


Yoshida at [0035], Fig. 5; Translation at [0023], Fig. 5. And Figure 7 shows a location where a repair can be performed by connecting a dummy touch line extended portion to a connecting portion that electrically connects to a common/touch electrode:

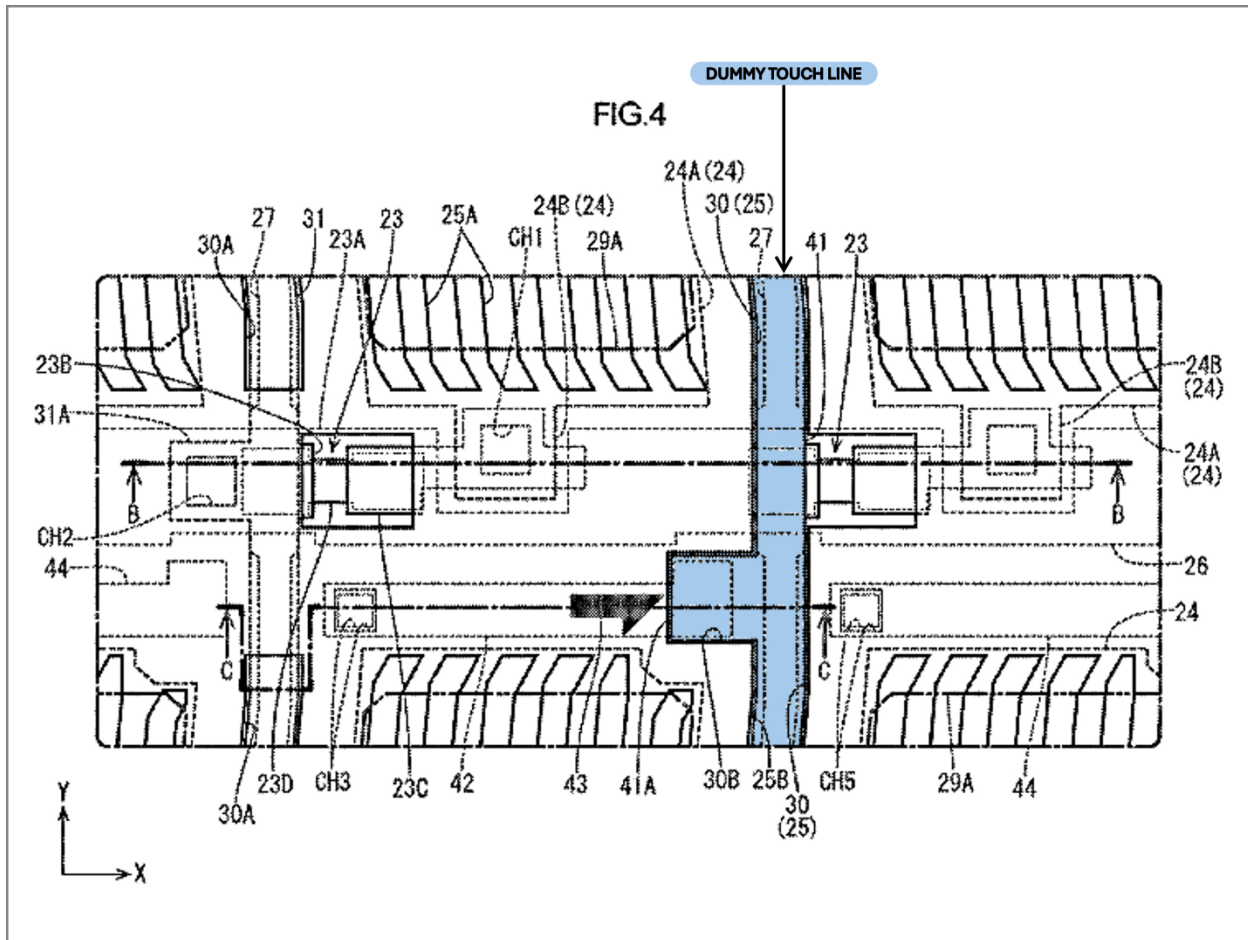


Yoshida at [0036], Fig. 7; *see also* Translation at [0024], Fig. 7. Accordingly, Yoshida's spare touch lines are "dummy touch lines" and are also "electrically isolated from any of the common electrodes" as the claim requires.

208. In my opinion, Yoshida also teaches that its spare touch lines 41 "extend in parallel with the Y-axis direction." Yoshida at [0027]; [0035]; Translation at [0015], [0023]. This is likewise evident from Yoshida's figures, which depict the (blue) spare touch lines:



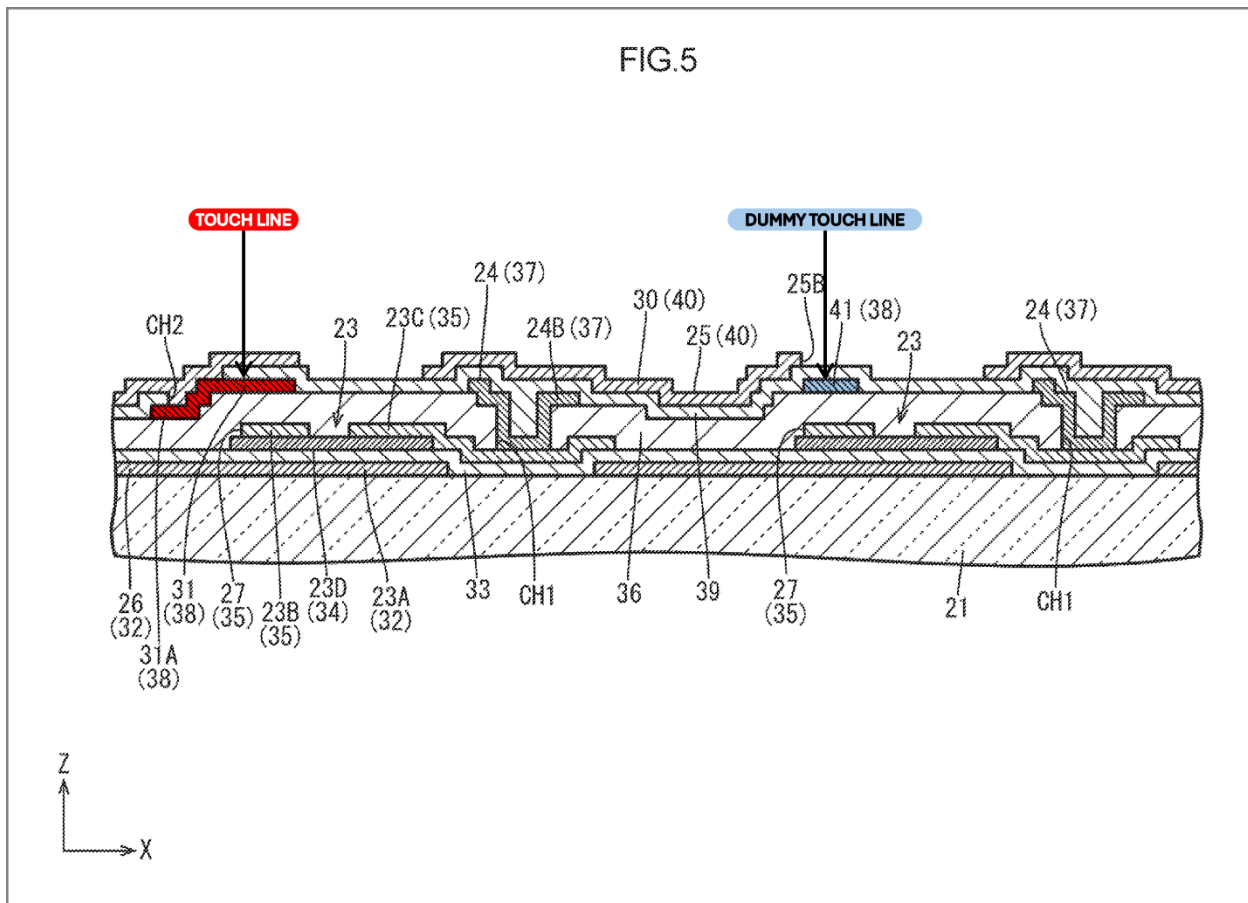
Yoshida, Fig. 2; Translation, Fig. 2.



Yoshida, Fig. 4; Translation, Fig. 4.

209. In my opinion, Yoshida also teaches that its spare touch line 41 “is formed in a same layer as the touch lines” as the claim requires. Specifically, Yoshida says that touch lines 31 and spare touch lines 41 are “mutually disposed in the same layer.” Yoshida at [0033]; Translation at [0021]. Yoshida further explains that “the spare touch line 41, as illustrated in FIG. 5, is made of the same third metal film 38 of the touch lines 31” indicating they are formed as part of the same process. Yoshida at [0035]; Translation at [0023]. Further, as can be seen in

Figure 5 below, both spare touch line 41 and touch line 31 are shown in the same layer, between first inter layer insulating film 36 and second inter layer insulating film 39:



Yoshida, Fig. 5; Translation, Fig. 5.

210. As explained above in Section VIII.C.1, in my opinion, the claimed “dummy touch line” does not need to serve any purpose or provide any specific function—it just needs to be a line that does not function as a touch line. But if the Patent Owner were to argue that a particular function is necessary for the claimed

“dummy touch line” then, in my opinion, Yoshida would still teach the functions for the dummy touch line disclosed in the ’025 patent or, at the very least, it would be obvious to a POSITA that the spare touch lines 41 do already, or could readily, provide that shielding functionality.

211. Specifically, as ’025 patent explains, the purpose of the dummy touch line is to shield the gap between two horizontally adjacent common electrodes. This gap can lead to “unintended rotation of liquid crystal molecules existing in the vicinity of the gap ... due to the electromagnetic field from the data line 50.” ’025 patent, 21:61-22:3. To shield against this data line electric field, the dummy touch line is described as being connected to a source that supplies it with the “same voltage level as the common voltage (Vcom) ... so that [the] dummy touch line 60B and common electrode 30 have the same potential when displaying images.” ’025 patent, 20:12-19. As a result, the “electromagnetic field from data line 50 existing below second separation area SA2” is “more effectively shielded by dummy touch line 60B” and this “prevent[s] the occurrence of the display unevenness.” *Id.*, 22:8-14.

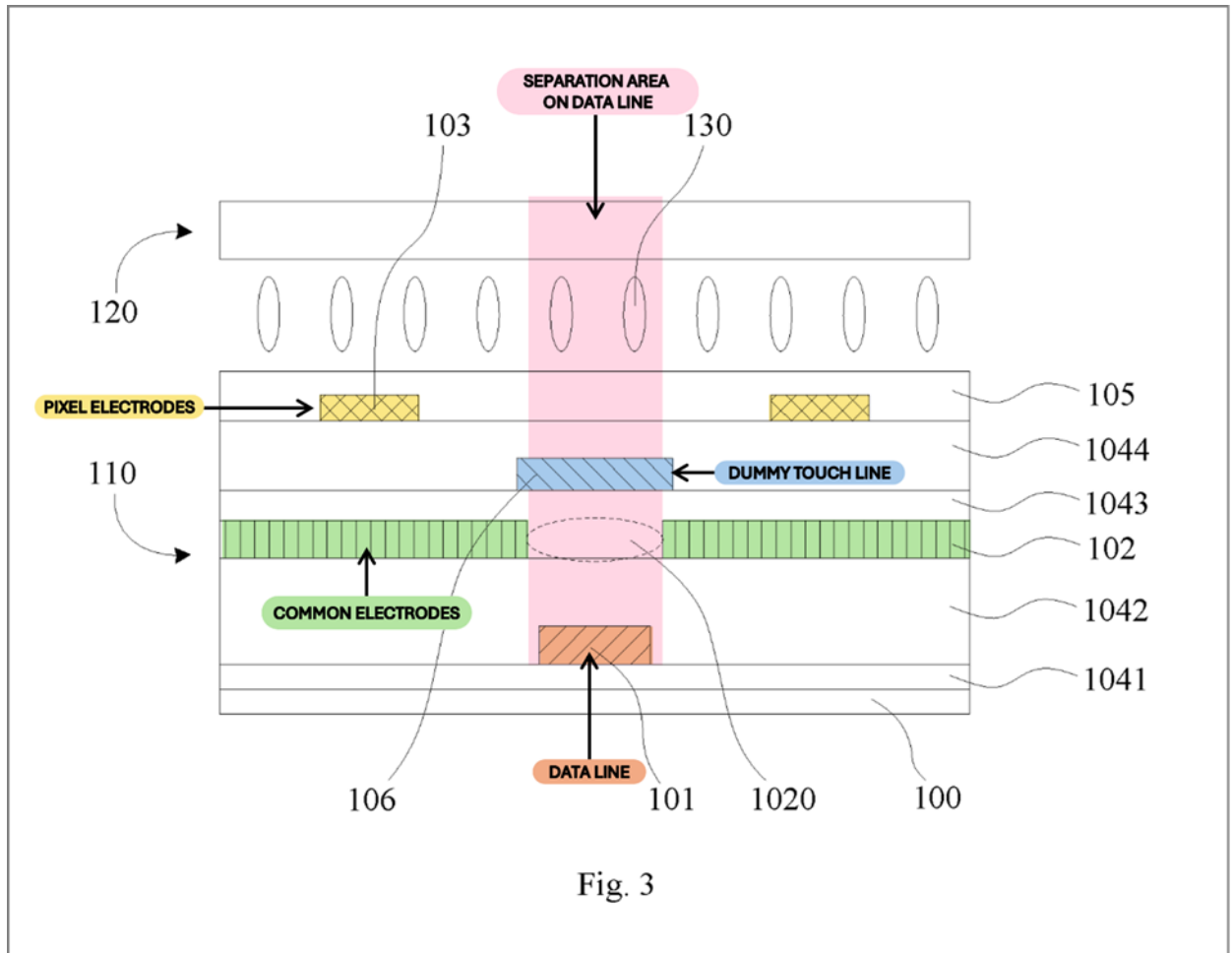
212. Yoshida’s spare touch lines that are located in the partition between touch electrodes are also above the data line and supplied with the common voltage, and so a POSITA would understand that the spare touch line 41 would provide shielding for the liquid crystals above the substrate in exactly the same

way.

213. Specifically, Yoshida discloses that certain spare touch lines are located in the separation area and overlap the data line, and therefore are between the data line and the liquid crystal layer. Yoshida at [0027], [0035], [0051]; Translation at [0015], [0023], [0039]. This is exactly where the dummy touch line in the '025 patent is positioned. '025 patent at 21:53-22:3. Additionally, Yoshida teaches that its spare touch lines can carry the “same common signal supplied to the common electrode,” with its third embodiment. Yoshida at [0062], [0065]; Translation at [0050], [0053]. This is also exactly how the dummy touch line is described in the '025 patent. '025 patent at 18:37-43. This arrangement serves to reduce instability in the region caused by the electric fields generated by the common electrode and pixel electrode. *Id.*

214. Yoshida does not discuss shielding the liquid crystals from the electrical field of the data line. Instead, Yoshida explains that its particular configuration of the spare touch line helps reduce instability caused by the electrical field of the common electrode and pixel electrode. Yoshida at [0062], [0065]; Translation at [0050], [0053]. But, despite Yoshida's omission, a POSITA would also understand that Yoshida's spare touch line supplied with the common voltage would also shield the electric field of the data line, precisely as described in the '025 patent.

215. At the time of the '025 patent, the concept of using lines to protect liquid crystals from inadvertent rotation by the electric field of the data line was well known. This is evident from the Xie reference. Like the '025 patent and Yoshida, Xie describes an in-cell touch panel, and it predates the '025 patent. *See* Xie at (86); [0004]-[0005] (explaining that Xie relates to in-cell touch panel technology). Xie's disclosure shows that it was already known by the priority date of the '025 patent that a "shield line 106" with the "same electric potential as the common electrode 102" could be used "for shielding an electrical field generated during transmission of signal by the data line 101." Xie at [0029]. In Xie's configuration, just like the Yoshida and the '025 patent, the "shield line" is positioned "at a location corresponding to the gap 1020" that is "provided between two neighboring common electrodes 102." *Id.* *See* Xie, Fig. 3:



Xie, Fig. 3.

216. Xie explains that, as a result of this place—above the data line—a shield line supplied with the common voltage could “shield the electrical field generated by the data line 101, thus avoiding effects on rotations of the liquid crystals 130 by the electrical field through the gap 1020, thereby solving the light leakage problem of the existing touch display devices.” Xie at [0031]. In other words, this shielding effect was a known phenomenon in the art of touch panels, and a POSITA would have known that Yoshida’s configuration for its spare touch

lines would provide this known shielding effect as well.

g) Element [18-H]

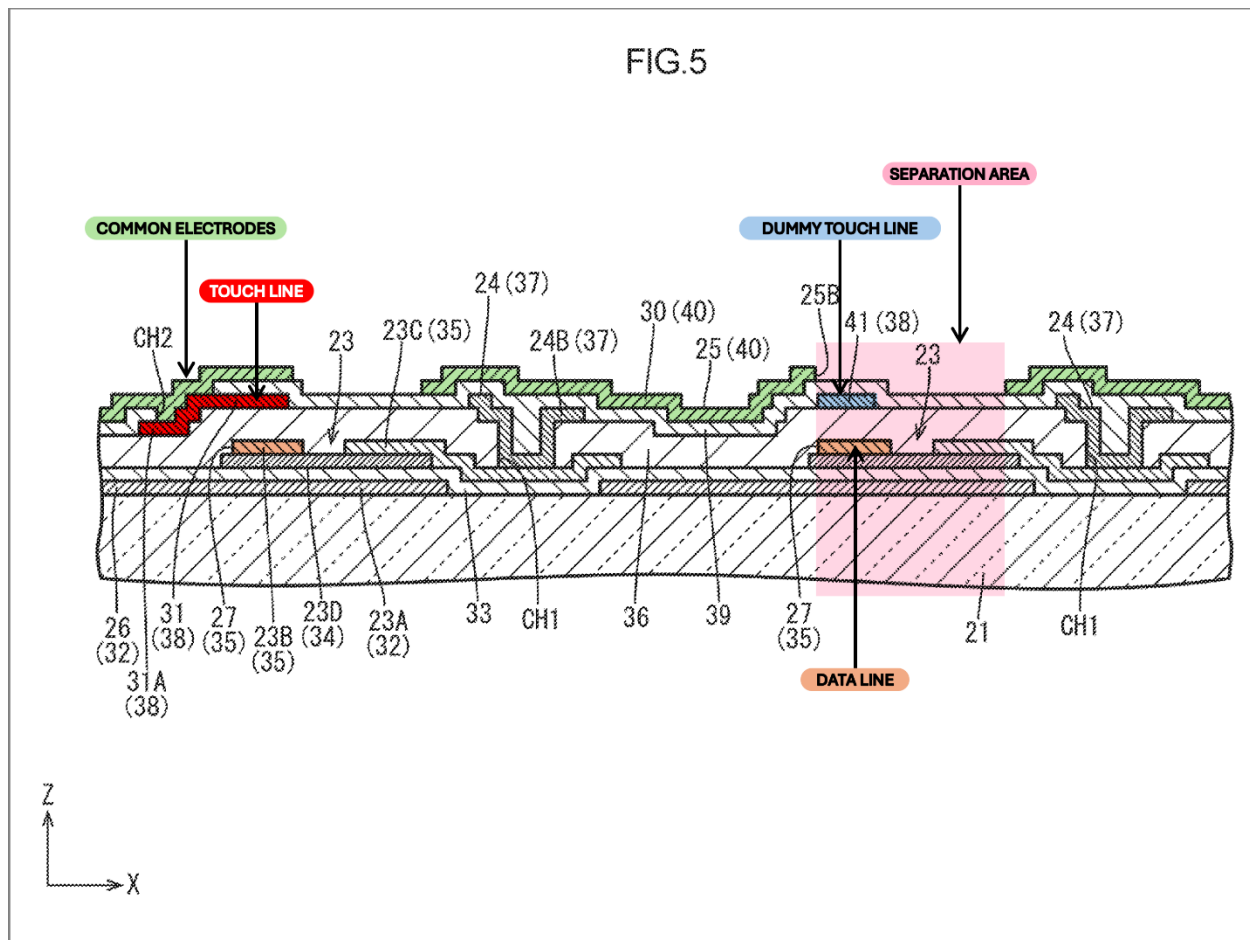
217. In my opinion, Yoshida discloses and renders obvious that “two of the common electrodes adjacent in the first direction are separated from each other with a separation area on the data line.”

218. Yoshida refers to the separation between its common/touch electrodes as “partitioning openings (partitioning slits) 25B,” and describes them as being “between two touch electrodes 30 adjacent to each other in the X-axis direction.” Yoshida at [0027]; Translation at [0015]. This partition opening is the same as the claimed “separation area” between “two of the common electrodes adjacent in the first direction” required by the claim.

219. Yoshida further teaches that certain spare touch lines 41 are positioned “between two touch electrodes 30” such that they “overlap partitioning openings.” *Id.* Yoshida also explains that these spare touch lines overlap the source lines 27, *i.e.*, data lines. Yoshida at [0035]; Translation at [0023]. Because the spare touch line is in the “partition area” and also overlapping the data line, the partition area/separation area is “on the data line” as required by the claim.

220. This position is also evident from Yoshida’s figures, including Figures 2, 4, 5 and 7. For example, Figure 5 provides a cross-sectional view below depicting the (blue) spare touch line 41/dummy touch line in the (pink) partition

area /separation area in between two adjacent (green) touch electrodes 30 in the X-axis direction (*i.e.*, separate two of the common electrodes adjacent in the first direction), and that partition area /separation area is also on the (orange) source line 27/data line:



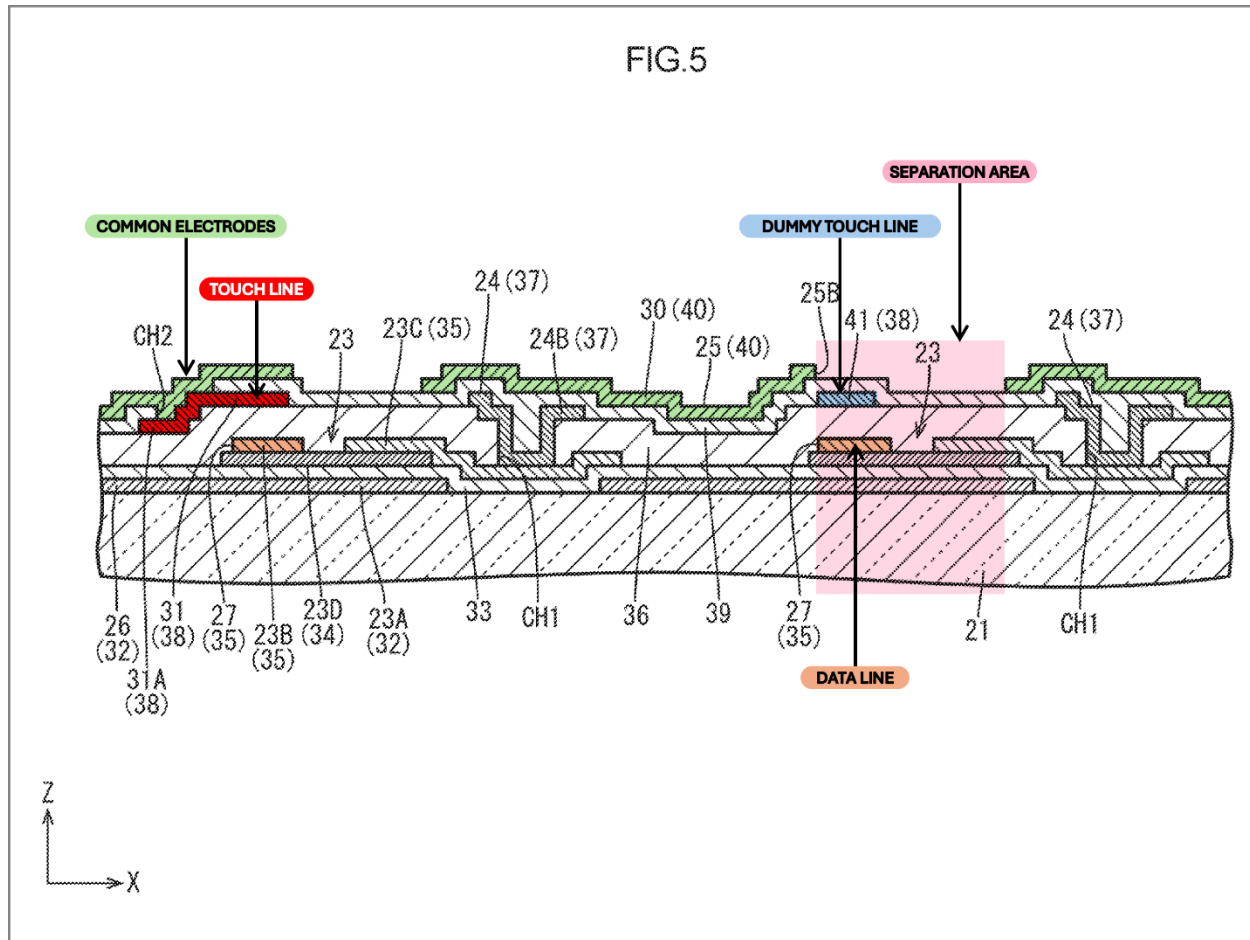
Yoshida, Fig. 5; *see also* Figs. 2, 4, 7; Translation, Figs. 2, 4, 5, 7.

h) Element [18-I]

221. In my opinion, Yoshida discloses and renders obvious that “the dummy touch line is provided in the separation area.”

222. As discussed for the prior limitation [18-H], spare touch line 41, *i.e.*, the dummy touch line, is located in the partition between touch electrodes, *i.e.*, the separation area, which is wider than the spare touch line. Specifically, Yoshida explains that “[t]he spare touch line 41 is arranged between two touch electrodes 30 adjacent to each other in the X-axis direction so as to overlap partitioning openings (partitioning slits) 25B.” Yoshida at [0027] (internal parenthesis omitted); [0062], [0065] (explaining that the spare touch line is within the partition area and non-overlapping with the common electrodes); Translation at [0015], [0050], [0053].

223. Once again, Figure 5 shows this limitation clearly. The (blue) spare touch lines 41 are between two (green) horizontally adjacent touch electrodes 30 adjacent to each other, in the (pink) separation area:



Yoshida, Fig. 5; *see also* Fig. 4; Translation, Figs. 5 and 4.

D. Ground 4 – 10, 11, 14, and 17 are Obvious Under 35 U.S.C. § 103 Over Yoshida in Combination With Kim II.

224. In my opinion, Yoshida combined with Kim II renders Claim 10, 11, 14 and 17 of the '025 patent obvious.

1. Independent Claim 10

225. As discussed above, Claim 10 is similar to Claim 18, but further recites limitations relating to segment electrodes, which are disclosed by Kim II. In my opinion, Yoshida combined with Kim II discloses and renders obvious Claim

10 of the '025 patent. Most of the limitations of Claim 10 are largely identical to Claim 18 and so do not need to be addressed again in significant detail. *See* Ex. 1014. Below, I address the slight differences in claim wording to explain how they do not change my opinion that Yoshida combined with Kim II discloses those elements.

226. Claim 10, however, does include some additional limitations not recited in Claim 18, and those additional limitations concern the concept of common electrodes that are divided into “segment electrodes” that with division areas that are “on the gate line.” This purported innovation, however, was taught years earlier in Kim II, and it would have been obvious to any POSITA designing a conventional in-cell touch panel (like Yoshida’s) that Kim II’s teachings could be—and desirably would be—implemented to provide similar but distinct improvements to the design.

a) Elements [10-PRE] through [10-F], and [10-I] through [10-K]

227. In my opinion, each of limitations [10-PRE] through [10-F], and [10-I] through [10-K] are substantively identical to corresponding limitations in Claim 18, and so are taught and/or rendered obvious by Yoshida for the same reasons I have discussed above in connection with Claim 18. I address each corresponding pair below.

228. Elements [10-A] through [10-E] are identical to Elements [18-A] through [18-E]. See Sections X.C.1.a through X.C.1.e above. Element [10-J] is identical to Element [18-H], except Element [18-H] appears to include an inconsequential typographical error in the form of a vestigial “as” at the end of the limitation, which does not appear to change the meaning or scope of the element. Element [10-K] is identical to Element [18-I]. Accordingly, in my opinion, Elements [10-A] through [10-E], [10-J], and [10-K] are rendered obvious for the same reasons I provided above in connection with the corresponding element of Claim 18. See Sections X.C.1.b, c, d, e, g, and h above.

229. In the event the Claim 10 preamble is found to be limiting, Yoshida discloses it and renders it obvious for the same reasons I explained above regarding the preamble of Claim 18. See Section X.C.1.a above.

230. Specifically, Claim 10’s preamble recites: “[a]n in-cell touch panel having an image display area made up of pixels arranged in a first direction and a second direction **intersecting** the first direction, the in-cell touch panel comprising” whereas Claim 18’s preamble recites “[a]n in-cell touch panel having an image display area made up of pixels arranged in a first direction and a second direction **orthogonal** to the first direction, the in-cell touch panel comprising.” (emphasis added). The substitution of the word “intersecting” for “orthogonal” is irrelevant to my opinions, as Yoshida taught a display panel with an array of pixels formed in

columns and rows, meaning their respective directions were both intersecting and orthogonal. *See* Section X.C.1.a above.

231. Element [10-F] recites “a dummy touch line ***extending*** along the second direction, formed in a same layer as the touch lines, and ***not electrically connected to*** any of the common electrodes.” This is almost identical to Element [18-F], which recites “a dummy touch line ***that extends*** along the second direction, is formed in a same layer as the touch lines, and ***is electrically isolated from*** any of the common electrodes.” (emphasis added). The change from “that extends” to “extending” is immaterial, and the change from being “not electrically connected to” to the synonymous phrase “electrically isolated from” is likewise immaterial to my analysis. To the extent these changes result in any difference in claim scope, the analysis I set forth above regarding Element [18-F] is equally applicable to demonstrating that Yoshida teaches and/or renders obvious the slightly reworded limitations of Element [10-F]. *See* Section X.C.1.f above.

232. Elements [10-G] and [10-H] do not have a corresponding limitation from Claim 18, so they are addressed separately below.

233. Element [10-I] reads “wherein ***the*** touch lines are connected ***one-by-one*** with the common electrodes arranged in the second direction ***among the common electrodes***.” (emphasis added). This is worded differently, but appears to be substantively identical to Element [18-G], which recites “wherein ***each*** touch

line is connected ***with a corresponding one*** of the common electrodes arranged in the second direction.” (emphasis added). Although reworded, both elements seem to be addressing the same concept—a given touch line should connect to one of the common electrodes within a column of common electrode. Even with the changed wording, in my opinion, all of the reasons I set forth above in connection with Element [18-G] similarly demonstrate that Element [10-I] would be rendered obvious as well. See Section X.C.1.e above.

b) Element [10-G]

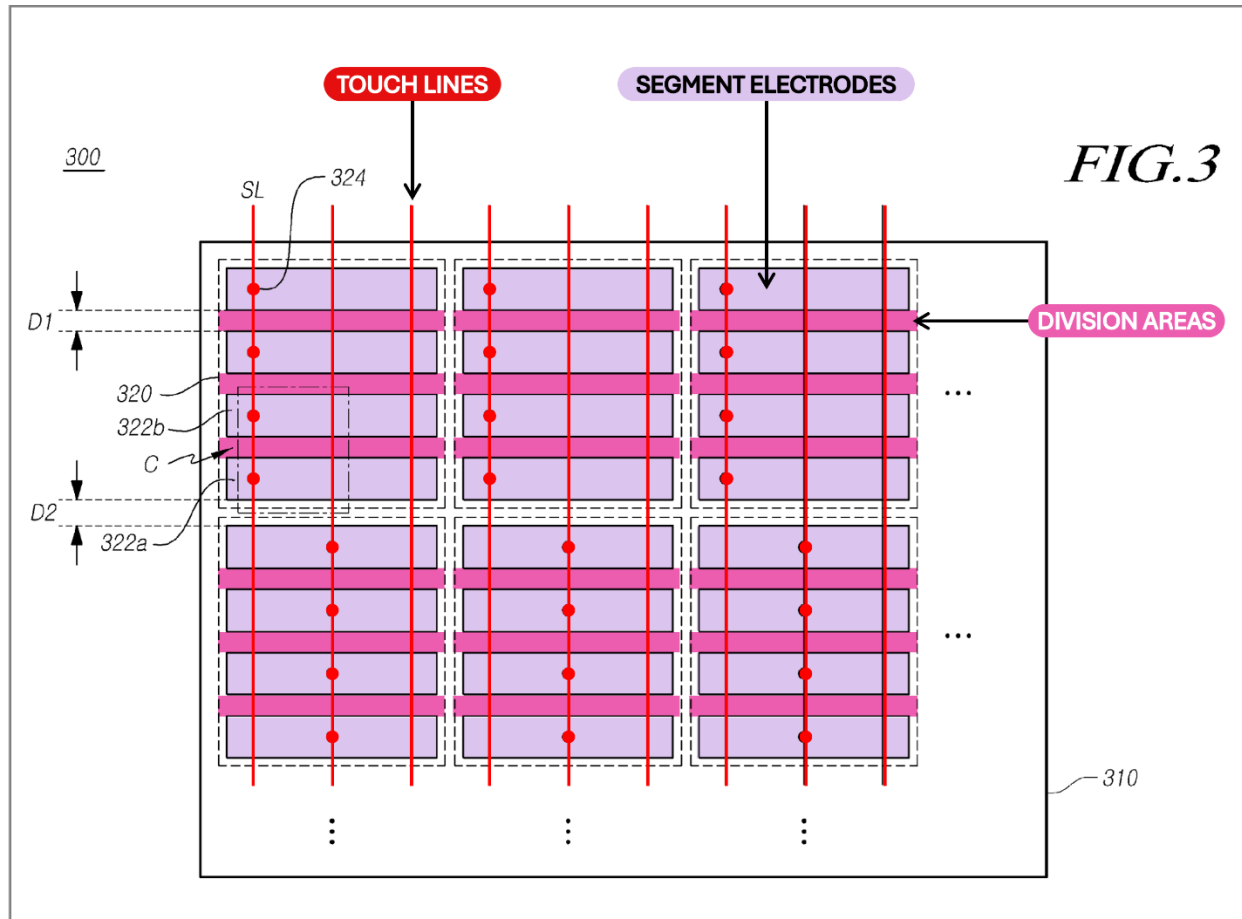
234. In my opinion, Kim II discloses and renders obvious these elements of Claim 10: “wherein each common electrode has segment electrodes divided with a division area on the gate line.”

235. Yoshida does not provide any disclosures regarding its common electrodes being divided into segment electrodes. Instead, Yoshida, as a reference, is primarily focused on describing its spare touch line solution, and is fairly light on details regarding the structure of its common/touch electrodes. A POSITA would therefore have been motivated to look outside of Yoshida for details and best practices for designs of those components such as Kim II, for guidance concerning the optimal structure for common electrodes. In particular, a POSITA would have been motivated to adopt Kim II’s teachings as to improvements regarding the design of common electrodes so as to avoid common problems that

arise when a large common electrode, such as those conventionally used in touch panels (including Yoshida's), overlaps several pixels and their corresponding gate lines. Kim II at [0036]-[0048]. For example, Yoshida includes "touch electrodes" that are "each arranged in an area spanning over a number (such as several tens) of pixel portions PX." Yoshida at [0026], [0028]; Translation at [0013], [0014]. Indeed, as Kim II and the '025 patent teach, a POSITA following Yoshida's teachings could have noticed the display defects caused by such large common electrode capacitance irregularities, which would have motivated the POSITA to seek solutions such as Kim II's.

236. Regarding Element [10-G], in my opinion, Kim II teaches that "each common electrode has segment electrodes divided with a division area on the gate line." *See also* Section X.A.1.g. Specifically, Kim II explains with regard to several of its figures that its common electrodes are divided into "common electrode voltage rows," separated by a "separation space" on the gate line, as claimed. For example, in connection with Figure 3, Kim II explains that "[e]ach touch electrode 320 may include a plurality of common voltage electrodes." Kim II at [0052]. Kim II further explains that "[w]ithin the touch electrode 320, the common voltage electrodes are physically separated from each other in a longitudinal direction of the sensing line SL," *i.e.*, vertically relative to Kim II's figures. Kim II at [0056]. Kim II further explains that there is "a separation

distance D1 between common voltage electrodes in different rows within the touch electrode 320.” Kim II at [0060]. Figure 3 shows these (purple) common voltage electrode rows, *i.e.*, segment electrodes, and (pink) separation distances below:



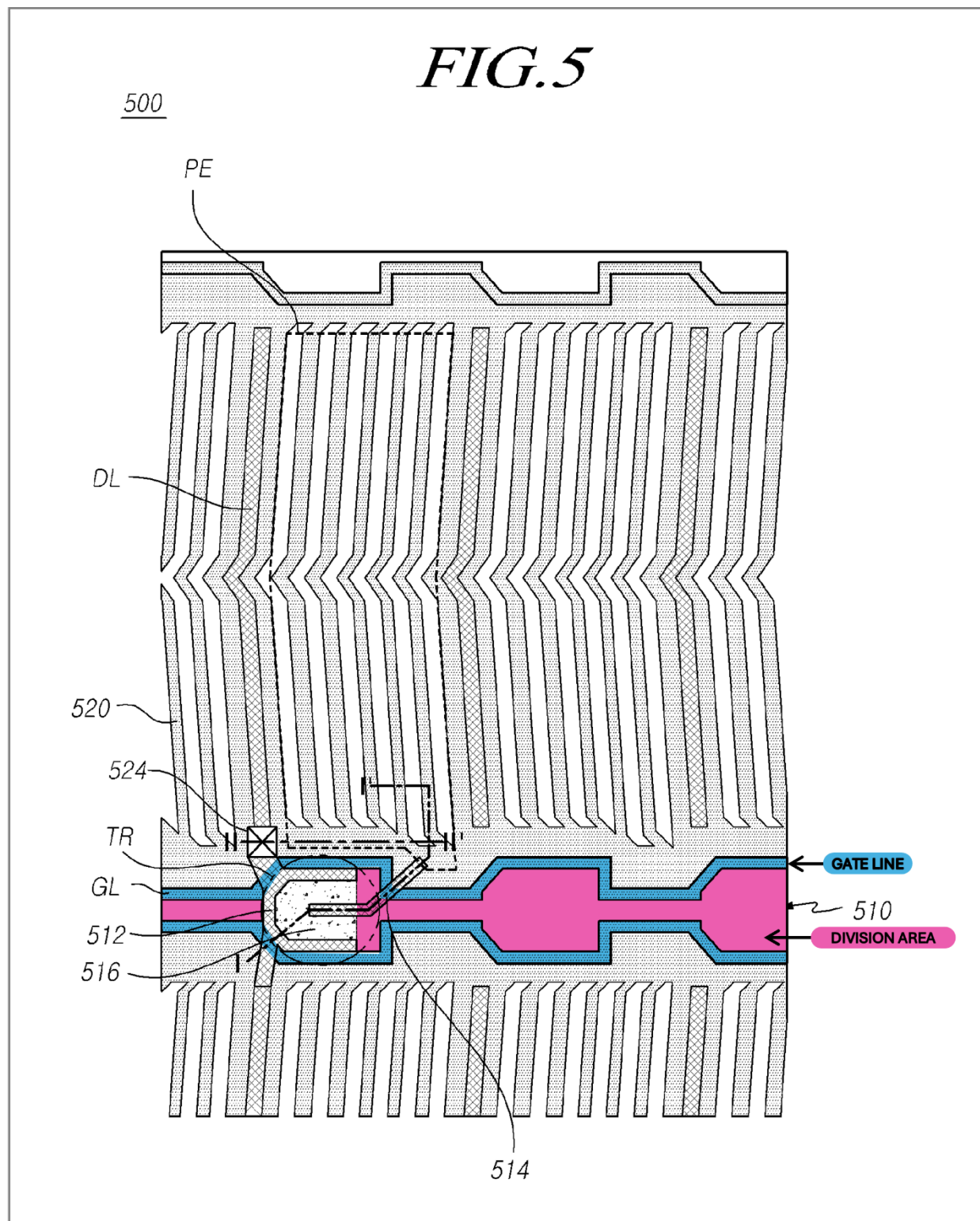
Kim II, Fig. 3.

237. Kim II’s Figure 4 provides a close up of the region “C” from Figure 3. In Figure 4, Kim refers to the “separation space” between rows within a common electrode as “separations space 430b,” which Kim II explains is “separating common voltage electrode rows within a touch electrode 320.” Kim II at [0065].

238. Regarding Figure 5, Kim II then refers to this same concept as

“separation space 510,” (*i.e.*, separation area). In connection with Figure 5, Kim II explains that there are several “common voltage electrodes 520” *i.e.*, segment electrodes “within the touch electrode” indicating that the touch electrode is divided into segments, as claimed. Kim II explains that “a separation space 510 [*i.e.*, separation area] is formed between the common voltage electrodes 520 in the direction parallel to the longitudinal direction of the gate lines GLs,” *i.e.*, horizontally, and Kim II adds this that “separation space 510 is formed in the direction parallel to the gate lines GL regardless of being inside the touch electrode and at an outer periphery of the touch electrode.” Kim II at [0088]-[0089]. In other words, Kim II explains that separation space 510 is formed between segments electrodes within a common electrode, and not just between distinct common electrodes. Kim II further specifically teaches that this “separation space 510” is on the gate line: “The separation space 510, *i.e.*, separation area, formed between different rows of the common voltage electrodes 520 may correspond to a line area of the gate lines GL. Specifically, in the exemplary embodiment as illustrated in FIG. 5, the gate line GL or a portion of the gate line GL may be formed in the separation space 510 between two common voltage electrodes 520.” Kim II at [0090].

239. These elements are visible in Kim II’s Figure 5 below, showing the (blue) gate line in the (pink) division area:



Kim II, Fig. 5.

240. Kim II also provides several teachings as to why it is advantageous to divide common electrodes into rows with the gate line in the division area between those rows. Specifically, Kim II explains that covering several pixels and their transistors with large common electrodes causes the transistors to experience varying coupling capacitances based on where they are relative to the edge of the common electrode. Kim II at [0013]-[0016]. As a result of this, the gate-source voltage of the gate electrode (*i.e.*, the voltage needed to activate the transistor) is distorted, which can prevent the pixel electrode from effectively receiving data voltages from the data line and lead the transistor to have a delayed response, resulting in pixel defects and horizontal line defects in the display, particularly at the outer periphery of the common electrodes. *Id.* at [0016]-[0017], [0024], [0047]-[0048], [0107].

241. Kim II explains that this existing problem can be solved by dividing otherwise large common electrodes into sub-unit rows such that the separation space between those rows would fall on the gate line, leaving it uncovered. *Id.*; *see also* Section IX.B. Specifically, Kim II noted that “[t]he gate line GL and an electrode adjacent thereto greatly affect a capacitance of the gate electrode 518.” Kim II at [0090]. Thus, because the gate line is connected to the transistor gate electrode, positioning the gate lines in the separation area eliminates the varying capacitance of the gate electrodes based on their proximity to the edge of the

common electrode, and allows them to have a more uniform capacitance, preventing the potential display problems caused by the gate-voltage distortion. *Id.* at [0089]-[0090]. Specifically, Kim II teaches that, by placing the division area on the gate line, “a capacitance of the gate electrode 518 becomes substantially uniform regardless of being inside the touch electrode and at an outer periphery of the touch electrode.” Kim II at [0089]. Kim further teaches that, as a result of the placement of the gate line in the separation area, the capacitance issues that would otherwise interfere with the pixel transistor ability to readily receive data voltages are prevented. *Id.* at [0090]. Specifically, Kim II explains that “[b]y positioning the separation space 510 on the gate line GL, a capacitance of the gate electrode 518 may be decreased and the transistor TR may be driven at an increased speed.” *Id.*

242. A POSITA would have recognized that Yoshida and Kim II are analogous references with highly compatible teachings. Both references relate to in-cell touch panels, with common electrodes, pixels, gate lines and the other typical components of such panels. Further, both references provide similar designs, with pixel electrodes positioned below common electrodes, indicating that each panel likely employs the same, similar, or at the very least, entirely compatible modes of aligning the liquid crystals in the liquid crystal layer. Further, with regard the Kim II’s solution concerning the structure and division of

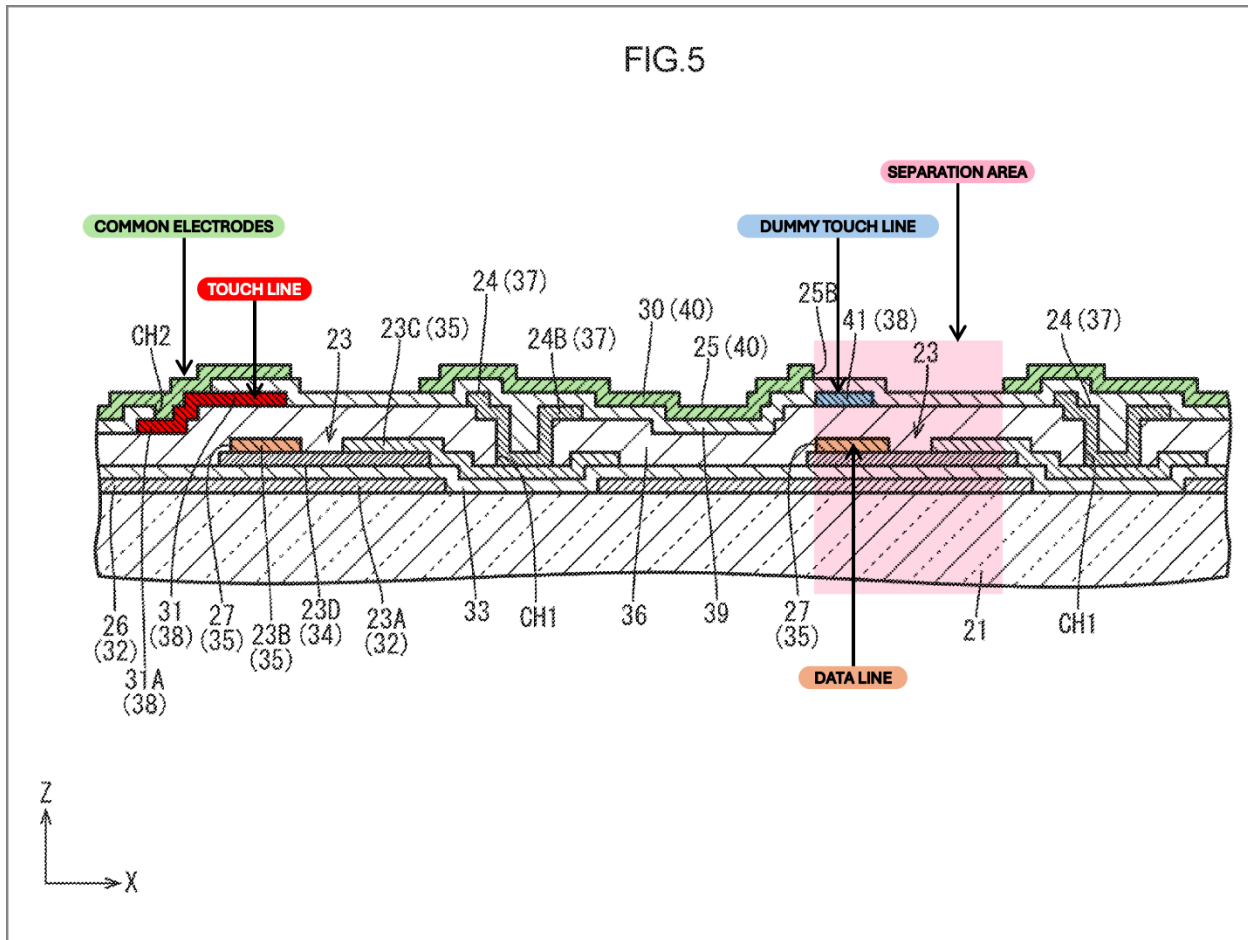
common/touch electrodes, both references also teach that those electrodes are the same shape and made up the same material. *See, e.g.*, Yoshida at [0033] (explaining that the touch electrodes are made of a second transparent electrode film 40); [0033] (explaining that film is made of ITO). Accordingly, given this and the generally mature state of the art, a POSITA would have readily understood how one could implement Kim II's segment electrode solution in a panel based on Yoshida's teachings, and would have recognized the simple rearrangement of components that would permit this minor adjustment to achieve Kim II's advantages. Thus, a POSITA would understand that, given these similarities, the teachings of either reference could be readily and easily incorporated into a design based on the teachings of the other without any particular obstacles and with a more than reasonable expectation of success.

243. Further, a POSITA would understand that these solutions are consistent with Yoshida's own design goals. For example, a POSITA reading Yoshida would already be aware of the desirability of reducing gate line capacitance, as Yoshida teaches that its gate lines can have cutout area to "reduce the capacitance between the gate lines 26 and the pixel electrodes 24" and also teaches that the "the drain electrode 23C overlaps the gate lines 26 ... to prevent variation of the capacitance between the gate lines 26 and the drain electrode 23C (i.e., the pixel electrodes 24) when the position of the drain electrode 23C is

displaced with respect to the gate lines 26 during the manufacture of the array substrate 21.” Yoshida at [0032]; Translation at [0020]. Thus, a POSITA would be motivated to look to Kim II for a more complete solution to avoid these capacitance problems that are a concern, but not a primary focus, of Yoshida.

244. Further, a POSITA would recognize that Kim II expressly describes its solution being particularly well suited for panels using Yoshida’s particular structure. Specifically, Kim II explains that when a particular “in-plane” structure is used for a touch panel, *i.e.*, “a structure in which the pixel electrode PE” and “the common voltage electrode 520 are positioned on one side of the liquid crystal layer,” then the capacitance issues “may become a big problem.” Kim II at [0092]. And Kim II explains that “if the separation space 510 is formed between common voltage electrode rows (*i.e.*, segment electrodes) in the in-plane structure as suggested in an exemplary embodiment, a capacitance between the common voltage electrode 520 and the gate electrode 518 may become more uniform.” *Id.*

245. A POSITA would recognize the Yoshida uses exactly such a “in plane” structure, as both its pixel electrodes and common electrodes are below the liquid crystals. *See* Yoshida, Fig. 5, *see also* Figs. 3, 7, 9 and 13; Translation, Figs. 5, 3, 7, 9 and 13.



Yoshida, Fig. 5; Translation, Fig. 5. Thus, a POSITA following Yoshida's teachings would have been recognized, based on Kim II's teachings, that Yoshida's structure rendered it particularly prone to the pixel defects and horizontal line defects described in Kim II if the described issues concerning gate line capacitance were not properly addressed. A POSITA would have been highly motivated to adopt these teachings to avoid such problems and achieve Kim II's taught benefits of achieving a more uniform capacitance between the common voltage electrode and gate electrode of the transistor. Likewise, a POSITA would also understand that the two references are particularly compatible and that there

would be no obstacle to implementing their similar but distinct solutions to differing capacitance-related display panel problems.

246. Further, a POSITA would also recognize that Yoshida's provides several advantageous teachings. First, as explained, a POSITA would recognize that Yoshida provides a robust and detailed disclosure of a touch panel device, and would recognize Yoshida as a strong starting place for a potential touch panel design.

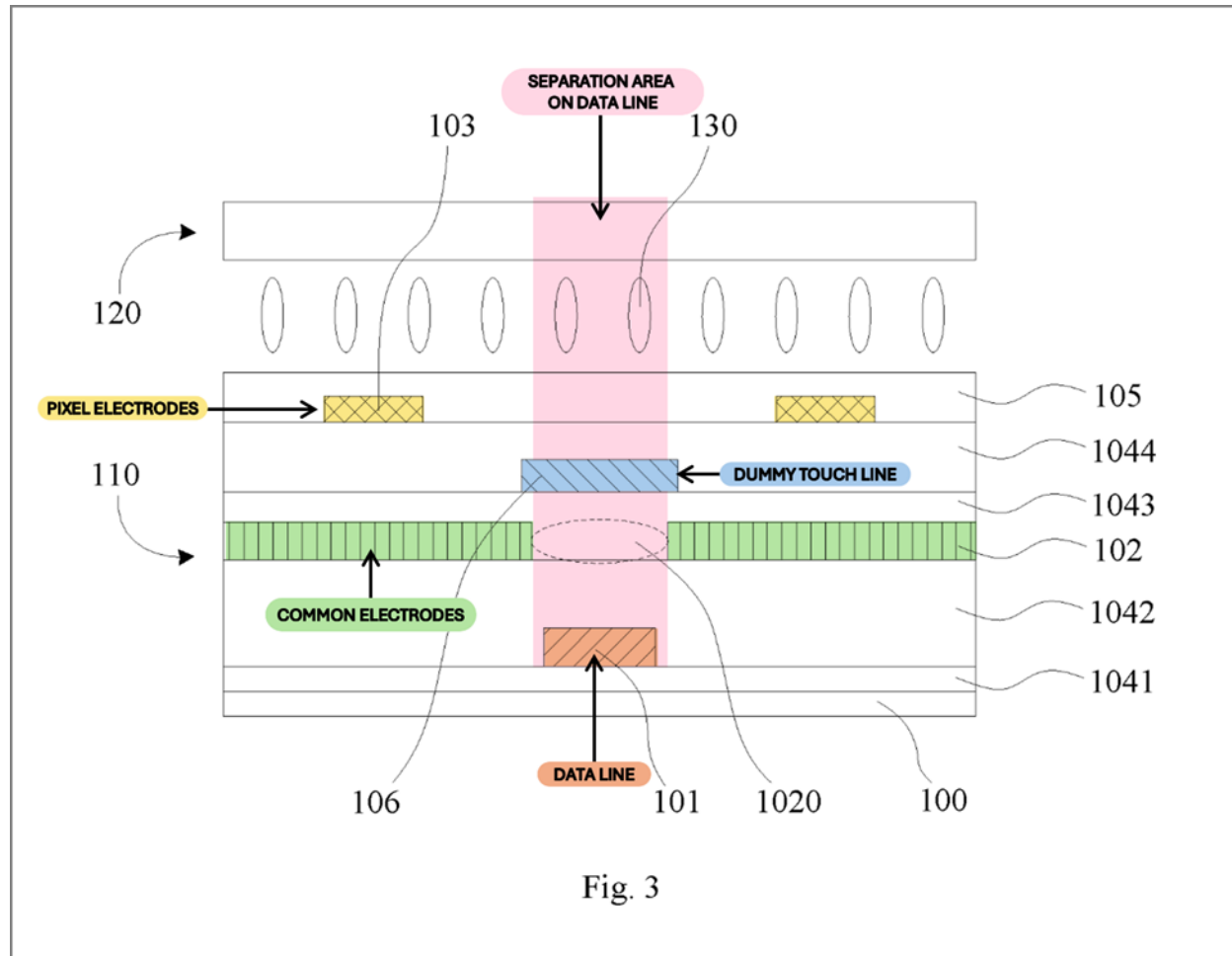
247. Second, a POSITA would recognize that Yoshida's spare touch lines would be beneficial to provide uniformity across the display design by ensuring that every data line is similarly overlapped by a line, even when there is no need for an active touch line to connect to a touch electrode in the column of the data line. *See* Yoshida at [0035]; Translation at [0022].

248. Third, a POSITA would also recognize that Yoshida teaches a beneficial and simplified method for repairing touch line disconnects without risking "secondary trouble" such as damage to the touch electrodes or the liquid crystal layer. Yoshida at [0037]; Translation at [0025]. A POSITA would recognize that this is a valuable addition that would increase manufacturing efficiency and yield, and therefore lower costs and increase the profitability of any business manufacturing touch panel display devices.

249. Fourth, as explained above, POSITA would also appreciate that, as

Yoshida teaches in connection with its third embodiment, that spare touch lines help reduce instability caused by the electric fields of the common electrode and pixel electrode. Yoshida at [0062], [0065]; Translation at [0050], [0053]. In particular, a POSITA would recognize that by reducing the instability in this area, the potential for manufacturing defects and misalignments would decrease and provide similar yield and cost reduction benefits.

250. Fifth, as explained above regarding Xie and the known phenomenon of shielding in the art. *See* Section X.C.1.f. A POSITA would also appreciate that Yoshida's spare touch lines carrying the common voltage in the gap between touch electrodes and over the data line would beneficially shield "shield the electrical field generated by the data line 101" to prevent inadvertent rotation of liquid crystals. *See, e.g.,* Xie at [0031]. This is shown in Xie's figure below:



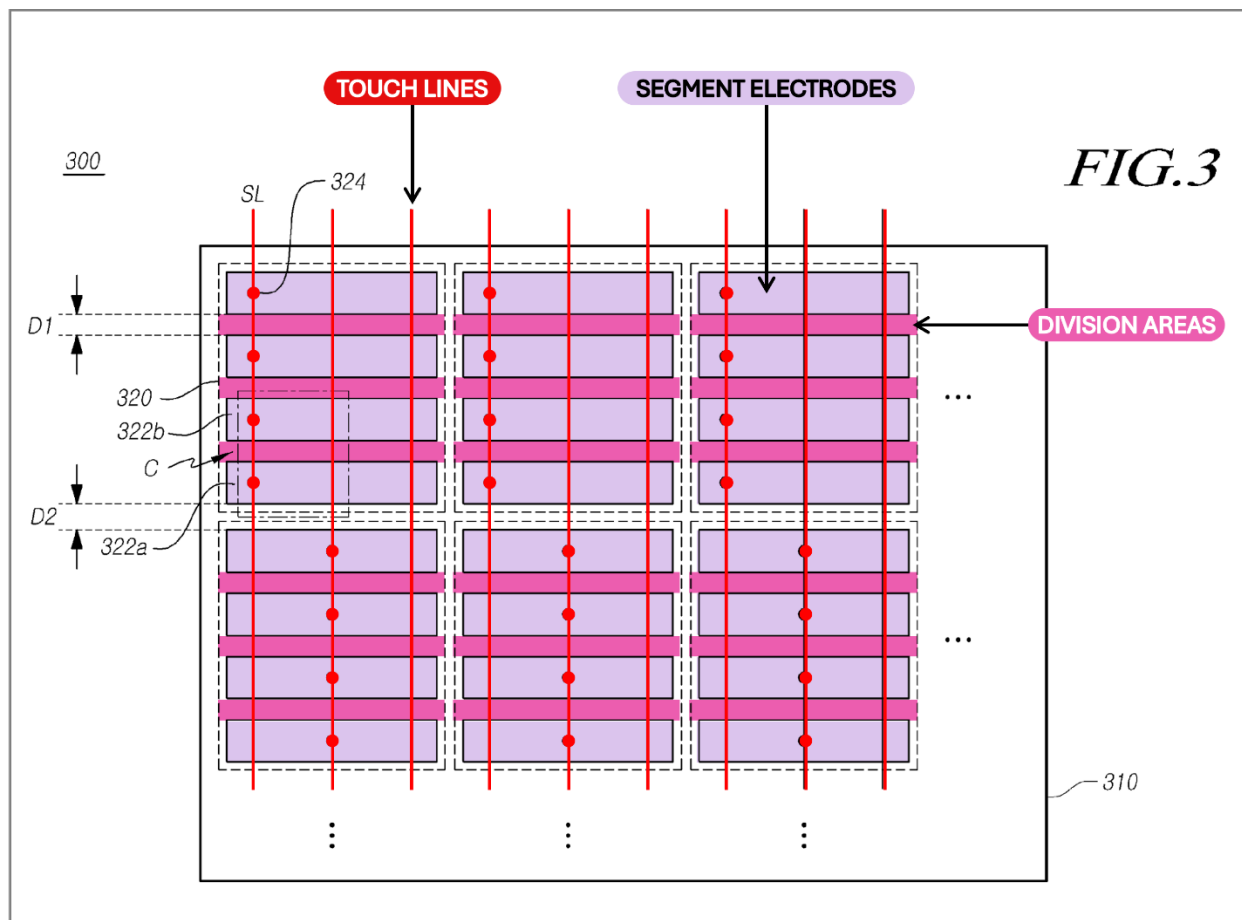
Xie, Fig. 3. Because a POSITA would recognize that Yoshida employs this exact configuration, a POSITA would therefore recognize that Yoshida provides additional benefits towards reducing light leakage and display defect problems like those described in Xie, and be further motivated to use it as part of a combination to provide for an improve touch display panel.

c) Element [10-H]

251. In my opinion, Kim II discloses and renders obvious these elements of Claim 10: “segment electrodes included in one of the common electrodes are

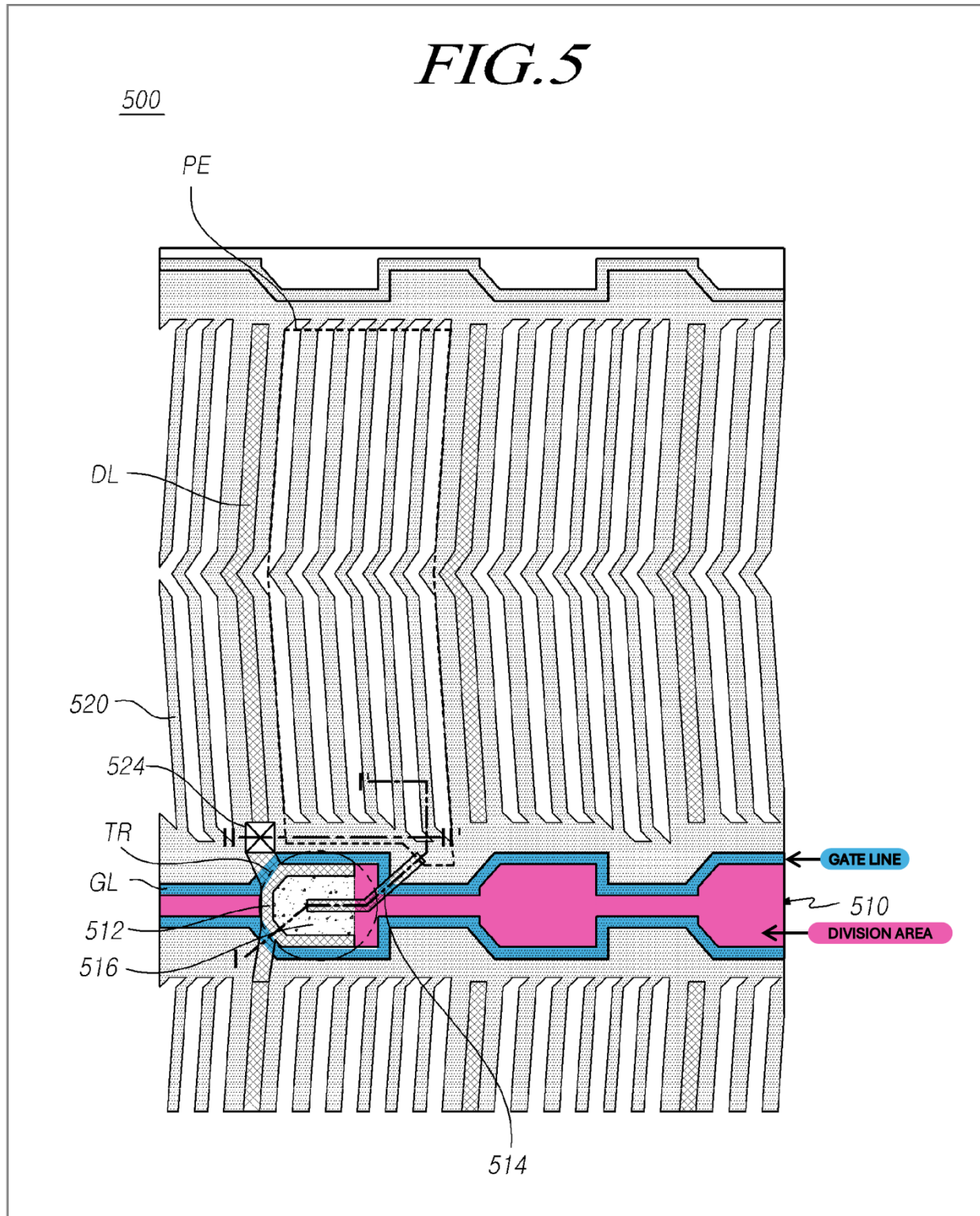
connected by at least one of the touch lines.”

252. Kim II teaches that the common voltage electrode rows, *i.e.*, segment electrodes, included in one of the common electrodes are connected by at least one of the touch lines. Specifically, Kim II explains, in connection with the embodiment depicted in both Figures 3 and 4, that each of common electrode rows within a touch electrode is connected to the others via a single “sensing line,” *i.e.*, touch line. Kim II at [0058], [0066]; *see also* [0056], [0083]. Figure 3 shows each of these (red) touch lines connecting to all the (purple) rows within a particular common electrode:



Kim II, Fig. 3.

253. When describing Figure 5, which Kim II describes as “an embodiment,” Kim II does not expressly state that the touch lines connect to each common electrode voltage row. It is fairly obvious why—Figure 5 only shows one row.



Kim II, Fig. 5.

254. A POSITA would therefore recognize that Kim II's Figure 5 does not depict a rigidly distinct and mutually exclusive embodiment as compared to Figures 3 and 4, but rather is a more specific embodiment that builds off those teachings and provides further detail concerning the gate line placement. In other words, a POSITA would assume the Kim II's Figure 5 provides an essentially "zoomed in" explanation of Figure 4, and thus understand that its rows of "common voltage electrode 520" that are "within the touch electrode" are similarly connected to a single touch line, as was described in the prior embodiments. Kim II at [0087]. Indeed, Kim II describes this feature as an "aspect" of the invention rather than a unique feature of a particular embodiment, and explains that "sensing line SL is connected to M number of common voltage electrode rows, and, thus, the M number of common voltage electrode rows connected to each other form one touch electrode 320." Kim II at [0061].

255. That said, even if there was some reason to believe that Figure 5 does not include touch lines connecting to all of the common electrode rows within a common electrode, a POSITA combining Kim II and Yoshida still would have found it obvious to connect segment electrodes within a single touch electrode 30 to a common touch line 31. Specifically, Kim II teaches that the touch electrodes 30 are composed of transparent oxide conductor (TCO) material such as ITO. Kim II at [0085]. ITO has a sheet resistance of about 100 ohms per square. Thin film

metals such as aluminum or copper have a sheet resistance of about 1 ohm per square, a factor of 100 times less. A POSITA would have known that, to avoid signal delay, distortion and non-uniformity (for both the application of a constant voltage and the touch line signals) the resistance between the touch line 31 and every part of each segment electrode must be minimized. Similarly, given the above, a POSITA would have known that charge transfer through a low resistance metal line, like the touch line 31, instead of through the ITO common electrode segments themselves is thus desirable. Further, Kim II teaches that this connection is formed via a contact hole 524, which is positioned in an area that does not overlap with the gate line. Kim II at [0090], Fig. 5. Accordingly, a POSITA would readily understand how to modify Yoshida's touch electrodes to divide them into segment electrodes and to connect touch line 31 to each segment electrode based on Kim II's guidance. Further, a POSITA would have recognized that doing so would desirably allow a set of segment electrodes to function more efficiently as a single touch electrode 30, avoiding signal delay, distortion, and non-uniformity. Indeed, Kim II recognized the necessity and desirability of such a connection, noting that doing so allowed the common voltage electrodes to "function as a single common voltage electrode" Kim II at [0055].

256. As explained above, a POSITA would have understood that the above teachings concerning segment electrodes could be, would be, and should be readily

and easily combinable with Yoshida's teachings, without any obstacle to—and with a more than reasonable expectation of—success. *See* Section X.D.1.b, above.

2. Dependent Claim 11

257. Claim 11 recites “[t]he in-cell touch panel according to claim 10, wherein a fixed voltage is applied to the dummy touch line, and the fixed voltage is a common voltage to be applied to the common electrode.”

258. Claim 10 is disclosed and rendered obvious by Yoshida and Kim II, for at least the reasons discussed above.

259. In my opinion Yoshida also teaches and renders obvious the dependent limitations “wherein a fixed voltage is applied to the dummy touch line, and the fixed voltage is a common voltage to be applied to the common electrode.” Specifically, as discussed above, Yoshida teaches in connection with its third embodiment that the spare touch line 41 located in between touch electrodes is supplied with “the same common signal supplied to the common electrode.” Yoshida at [0062], [0065]; Translation at [0050], [0053]. In other words, the spare touch line is supplied with the “common voltage to be applied to the common electrode.”

260. Yoshida also teaches, or at least renders obvious, that this is a “fixed voltage” as required by the claim. Specifically, Yoshida explains that “common electrode 25 is supplied with a substantially constant reference potential

at all times,” indicating it that Yoshida recognizes that the common voltage is a fixed voltage. Yoshida at [0030]; Translation at [0018]. Further, a POSITA would have understood this common reference potential to be a fixed voltage, as it is the conventional purpose in LCD technologies to utilize common electrodes that are supplied with a fixed, common voltage to provide the reference potential for pixel pixels, as I explain above in Section VII.A.

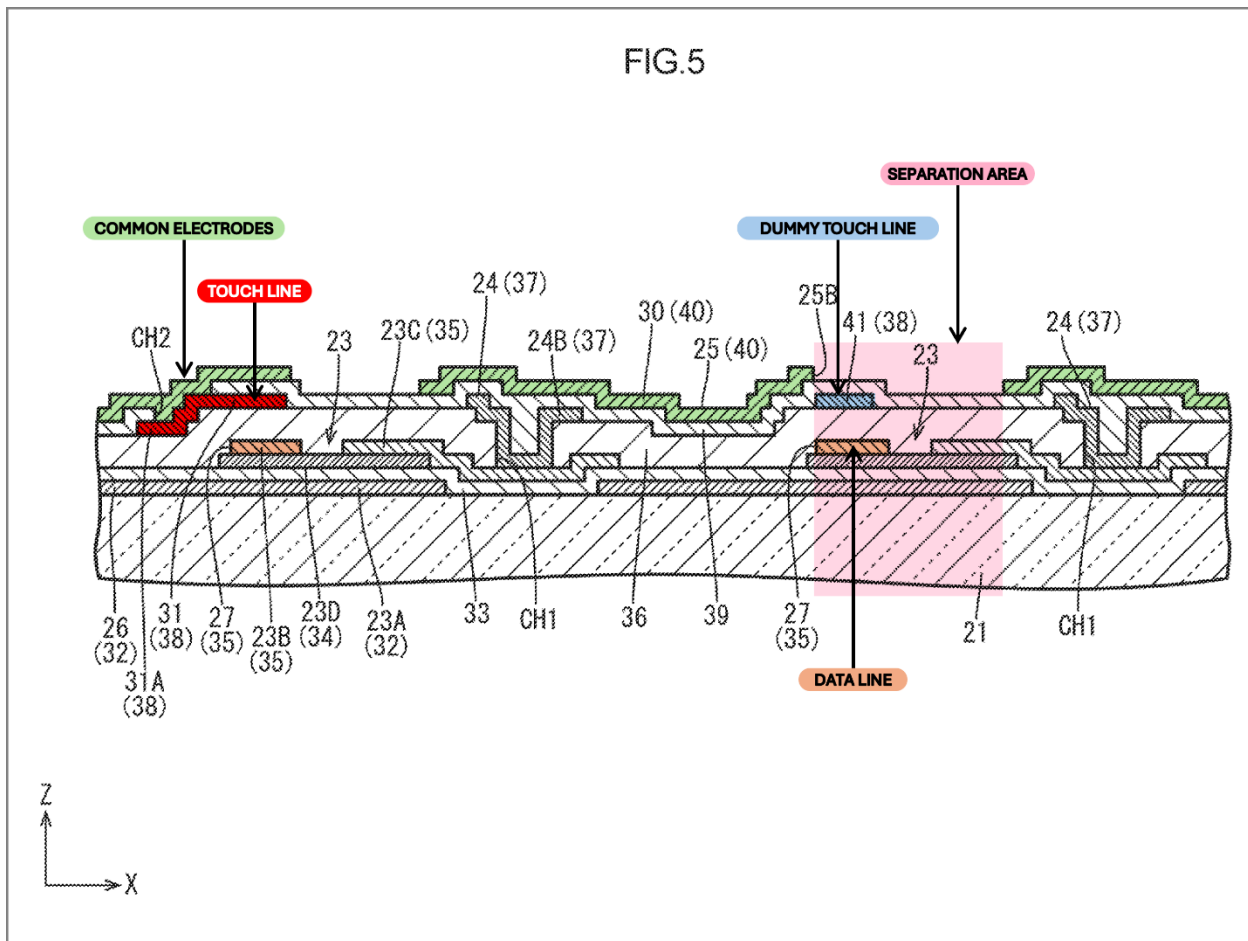
3. Dependent Claim 14

261. Claim 14 recites “[t]he in-cell touch panel according to claim 10, wherein a width of the dummy touch line is smaller than a distance between the dummy touch line and the common electrode.”

262. Claim 10 is disclosed and rendered obvious by Yoshida and Kim II, for at least the reasons discussed above.

263. In my opinion, Yoshida teaches and renders obvious “wherein a width of the dummy touch line is smaller than a distance between the dummy touch line and the common electrode.” Although Yoshida does not provide exact dimensions of its spare touch line as compared to the partition area, it does disclose that the spare touch line may be between and not overlap with the common electrodes. *See, e.g.*, Yoshida at [0062], [0065]; Translation at [0050], [0053]. Further, a POSITA would have found it obvious based on Yoshida’s figures that that the spare touch line 41 could be less wide than the distance between the spare touch

line and one of the common electrodes. For example, in Figure 5, the distance between the right side of the spare touch line 41 and left edge of the neighboring common electrode to the right is greater than the width of the spare touch line 41:



Yoshida, Fig. 5; Translation, Fig. 5.

264. A POSITA would have understood that the precise dimensions of these components are flexible rather than fixed, as evidenced by the fact that neither Yoshida nor any of the other references discussed in this Declaration refers to any strict requirements concerning relative dimension. Accordingly, a POSITA

would have found it obvious that the particular relative sizes of these components are a design choice within the capabilities of the POSITA, and would have, given the dimensions depicted in Yoshida's Figure 5, for example, found it at least obvious to try formulating a touch panel with components of corresponding proportions that would practice the claim limitations.

4. Dependent Claim 17

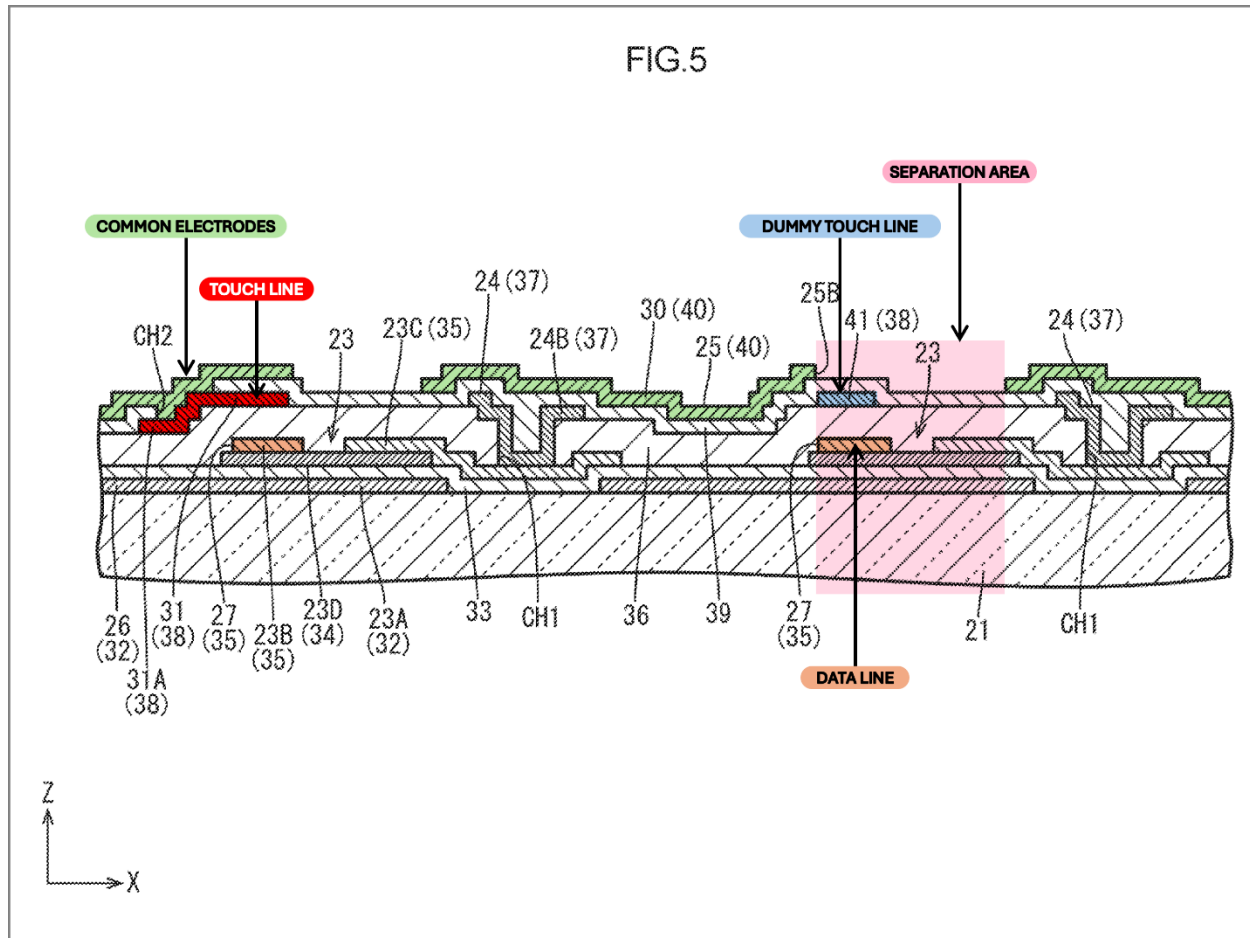
265. Claim 17 recites “[t]he in-cell touch panel according to claim 10, wherein the dummy touch line is offset from any of the common electrodes in a planar view.”

266. Claim 10 is disclosed and rendered obvious by Yoshida and Kim II, for at least the reasons discussed above.

267. The '025 patent does not use the term “offset” in the specification or provide any particular guidance as to what the term means in the context of this claim limitation.

268. Nonetheless, in my opinion, Yoshida also teaches and renders obvious the limitation “wherein the dummy touch line is offset from any of the common electrodes in a planar view.” Specifically, Figure 5 shows a cross section of Yoshida's spare touch line 41. Based on this cross section, it is evident that if the spare touch line was perceived from the planar view, it would be offset from any of the common electrodes because it is between and does not overlap any of the

common electrodes, just as is the case with the dummy touch line of the '025 patent:



Yoshida, Fig. 5; Translation, Fig. 5, [0062], [0065] (explaining that certain spare touch lines 41 do not overlap the touch electrodes); Translation, Fig. 5, [0050], [0053].

XI. SECONDARY CONSIDERATIONS

269. I am not aware of secondary considerations of non-obviousness that bear on the Challenged Claims. If I am made aware in the future of arguments of

any secondary consideration, I expressly reserve the right to assess those arguments when they arise in order to form opinions regarding their correctness or incorrectness.

XII. CONCLUSION

270. It is my conclusion and opinion that the Challenged Claims of the '025 patent are invalid.

Declaration of Richard A. Flasck, M.S.

U.S. Patent No. 11,126,025

I declare under penalty of perjury that the foregoing is true and correct.

Executed this 4th day of August, 2025 in SAN RAMON, CA.

A handwritten signature in blue ink, reading "Richard A. Flasck", written over a horizontal line.

Richard A. Flasck, M.S.

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