VDNROM: A Novel Four-Bits-Per-Cell Vertical Channel Dual-Nitride-Trapping-Layer ROM for High Density Flash Memory Applications

Falong Zhou, Yimao Cai, Ru Huang , Yan Li, Xiaonan Shan, Jia Liu,
Ao Guo, Xing Zhang, and Yangyuan Wang

Institute of Microelectronics, Peking University, Beijing 100871, China
Tel: 86-10-62757761, Fax: 86-10-62751789
Email: huangr@ime.pku.edu.cn

Abstract - A novel vertical channel nonvolatile memory cell with oxide–nitride–oxide–nitride–oxide (ONONO, dual nitride trapping layers) dielectrics stack is proposed and experimentally demonstrated for the first time. Compared with the conventional planar NROM cell, since the cell area of the proposed vertical structure is independent of the gate length, the VDNROM structure can relax the limitation of the gate length scaling, and can have high capability of cell area shrinking. The fabrication process of this VDNROM device is basically compatible with planar CMOS technology. The VDNROM cell can be programmed and erased by the hot carrier injection to the localized trapping dual-nitride-layers, so it can achieve a four physical bits storage capability each cell. The reliability behaviors including the cycling endurance and the bake retention at 150°C have also been investigated and show the acceptable characteristics. The experiment results verify the VDNROM cell as a good candidate for high-density applications.

I. INTRODUCTION

Recently, SONOS flash memory has been paid more attention and considered as a promising technology bridging the gap between the floating-gate flash and the next generation memories because of its intrinsic better endurance, good scalability, simpler fabrication process and its perfect compatibility with conventional CMOS technology for embedded applications [1-3]. However, conventional SONOS cell is only one-bit-per-cell storage, and the data retention is still a big problem due to the direct tunneling of stored charge through the ultra thin tunneling oxide.

The NROM concept [4-5] was proposed to solve the drawbacks of SONOS by using channel hot electrons injection (CHEI) for programming and band-to-band tunneling induced hot holes injection (BBTIHH) for erasing. This device can allow thicker tunneling oxide, while still maintaining high efficient Program /Erase (P/E) operations. Moreover, the P/E mechanisms lead to localized charge storage in the trapping nitride layer, so the NROM can store two distinct bits per cell. However, the further scaling of the cell area of the conventional planar NROM device for higher density is limited by the gate length scaling for two reasons. Firstly, the drain voltage can not be scaled below 3.2V for CHEI, and therefore the punch-through effect would become worse as the gate length scaling [6]. Secondly, since two bits are stored in physically distinct areas in the nitride layer, the lateral distributions of the charges have to be well separated to avoid any interference between the two bits [7].

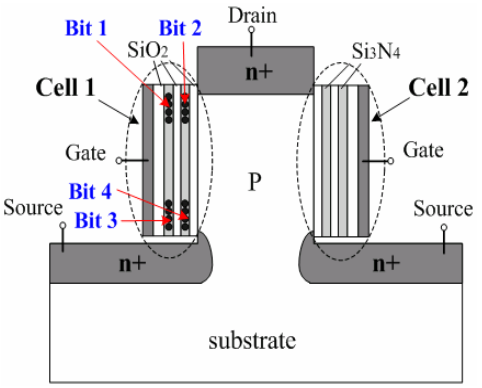

Fig. 1 Schematic cross sectional view of the proposed 4 bits/cell VDNROM flash memory.

In this work, as shown in Fig. 1, we proposed and demonstrated experimentally a novel vertical channel dual-nitride-trapping-layers ROM (VDNROM) structure nonvolatile memory device achieving four-bits-per-cell function for the first time. Compared with the conventional planar NROM cell, since the cell area of this vertical channel structure is independent of the gate length, the VDNROM structure can relax the limitation of the gate length scaling, and can have high capability to shrink the cell area. Moreover, the fabrication of this VDNROM device is basically compatible with planar

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CMOS technology. The experimental results demonstrate continued better scalability of the VDNROM cell for high-density applications.

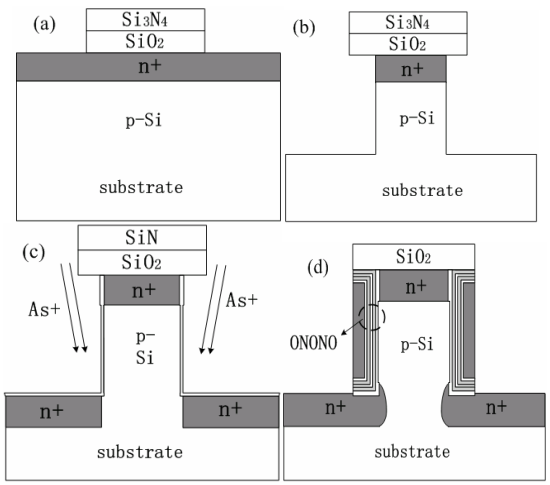

Fig. 2. The process flow of the proposed 4bits/cell VDNROM flash memory.

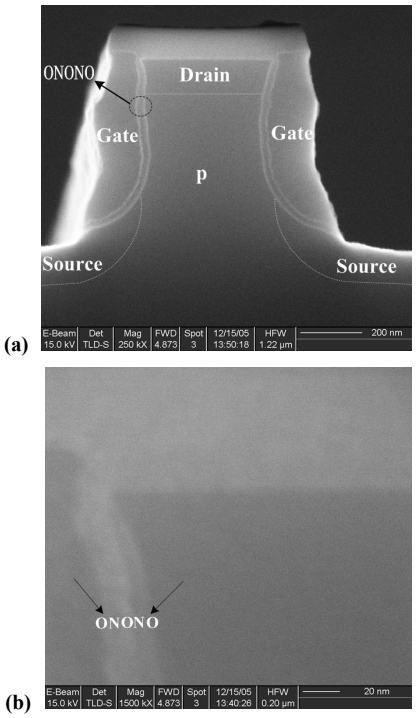

Fig. 3. The SEM images of the proposed 4bits/cell VDNROM flash memory cell (a) and the ONONO gate dielectric stack (b).

II. Device Structure and Fabrication

The schematic cross-sectional view of the proposed VDNROM flash memory cell with the oxide-nitride-oxide-nitride-oxide (ONONO) gate dielectric stack is illustrated in Fig. 1. The charges can be stored in the dual nitride trapping layers above the channel next to the n+/p junctions, so this VDNROM cell can achieve a four physical bits storage capability as shown in Fig.1. The tunneling oxide and the block oxide are thicker than 5 nm to avoid any direct tunneling of the charges, and the gate dielectric stack of the ONONO five layers (the tunneling oxide, the first trapping nitride layer, the inter-nitride oxide, the second trapping nitride layer, the block oxide) are 7/4/5/5/13 nm respectively.

Referring to Fig. 1, the process flow to realize such a 4bits/cell VDNROM device was shown in Fig. 2(a)-(b). After isolation, the channel boron doping and the drain arsenic doping were implemented. Two layers of oxide and nitride was deposited, patterned and etched to form the dual-layers hard masks as shown in Fig. 2(a). The silicon substrate was then etched by ICP (Inductive Coupled Plasma) to form the steep device mesa. Next, the device mesa was etched isotropically by RIE (Reactive Ion Etch) to form the recessed self-aligned poly gate structure shown in Fig. 2(b). To remove the surface damage on the sidewalls of the device mesa, thin sacrificial oxide was grown, which was followed by source arsenic implantation ($4\times10^{15}cm^{-2}$, 100KeV), as shown in Fig. 2(c). After sacrificial oxide removed, 7.0-nm gate oxide was grown at 850ºC by dry thermal oxidation. Next, a dielectric stack of trapping-nitride /inter-oxide/trapping-nitride/block-oxide (NONO) with 4/5/5/13 nm respectively was deposited. Then, a polysilicon film was deposited, implanted and etched to form the self-aligned gate spacer. After the nitride hard mask removed, rapid thermal annealing was implemented to activate the dopants in the S/D region and poly gate, as shown in Fig. 2(d). Finally, the device was covered by low temperature deposited oxide (LTO), and followed by the rest of the process such as contact opening, metal defining and annealing. Fig. 3 (a) shows the SEM (scanning electron microscope) micrograph of the cross section of the fabricated VDNROM cell, and the SEM image of the ONONO gate dielectric stack is shown in Fig. 3 (b).

III. Operation Mechanism and Experiment Results

The VDNROM cell is programmed and erased by channel hot carriers injection. The four states ("00", "01", "10", "11") corresponding to bit-1 and bit-2 are shown in Fig. 4 (a)-(d), and the programming and erasing operations of the four states are shown in Table I. For example, applying 7.0 V on the drain electrode, 12.0 V on WL (the gate electrode) and grounding the source electrode for programming the state "00" in Fig. 4(a). The accelerated channel electrons are injected into the both two nitride layers of the ONONO gate dielectric stack near the drain junction, a self-aligned storage with the junction edge. As shown in Fig. 4(b) and Table I, the state of "01" is programmed by the hot electrons injection to the first trapping nitride layer with lower drain voltage 5.0 V (compared with the programming of the state of "00"), 6.0 V on WL (the

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gate electrode) and grounding the source electrode. The state of "10" shown in Fig. 4(c) is realized by two steps. As shown in Table I, the first step is the hot electrons injection to the dual trapping nitride layers with Vg=12.0 V, Vd=7.0V and Vs=0V, and the second is the hot holes injection to the first nitride layer applying Vd=-8.0 V, Vg=5.0 V and Vs=0V. Holes are generated by band-to-band tunneling in the deep depletion layer under the gate dielectric stack above the n+/p junction [4, 8]. Holes increase their energy due to the lateral field in depletion region of the channel and they are injected through the bottom oxide into the nitride trapping layer, where they recombine with the stored electrons or are trapped. As shown in Fig. 4(d), the state of "11" is the initial state and it can also been realized by erasing from other states shown in Table I.

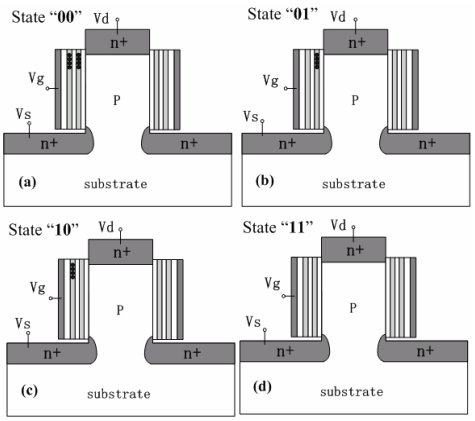

Fig. 4. The four states corresponding to bit-1 and bit-2 of the proposed VDNROM flash memory.

TABLE I.
VDNROM Flash Memory Program/Erase Operating Conditions
(Four states corresponding to bit-1 and bit-2)

State	P/E	Gate (Pulse)	Drain (Pulse)	Source	Time	Vth
'00'	Program from "11"	12V, 0V, 1μs	7V, 0V, 1μs	0 V	10 ms	5.5V
'01'	Program from "11"	6V, 0V, 1μs	5V, 0V, 1μs	0 V	10 ms	4.3V
'10'	Program from "11"	12V, 0V, −8V, 1μs, 9μs	7V, 0V, 5V, 1μs, 9μs	0 V	100 ms	3.3V
'11'	Erase	0V, −12V, 1μs	6V, 0V, 1μs	0 V	100 ms	2.3V

Fig. 5 shows transfer characteristics of the VDNROM flash memory cell with 0.3μm channel length in the four states. The threshold voltage of State "11" is 2.3V (the same Vth as the initial). State "00" has a threshold shift of ΔVth=3.2V from State "11". The ΔVth of 2.0V in State "01" is observed. The threshold voltage of State "10" is 3.3V, and the ΔVth is 1.0V. The transfer characteristics of each state exhibits excellent subthreshold performance as shown in Fig. 5. The programming and erasing characteristics of the VDNROM flash memory are shown in Fig. 6.

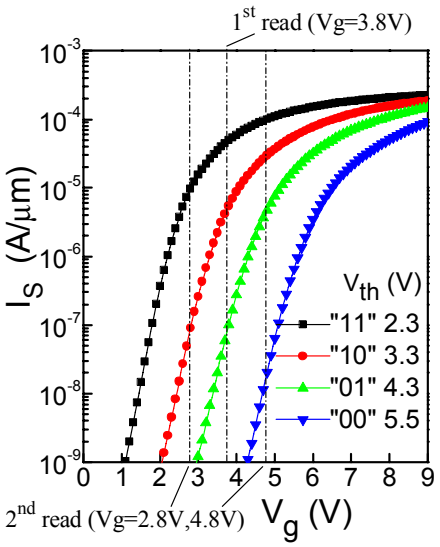

Fig. 5. The transfer characteristics of the programmed/erased bit-1 and bit-2 of the VDNROM flash memory.

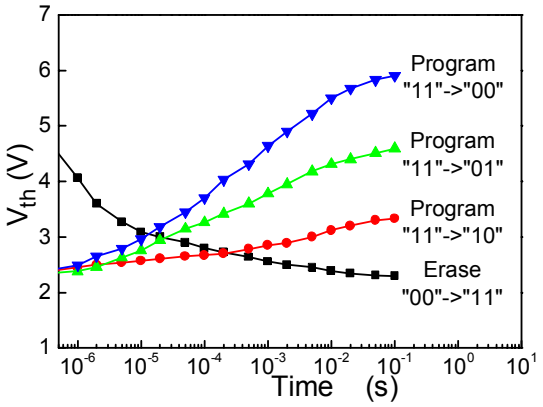

Fig. 6. The Programming/Erasing characteristics of the VDNROM flash memory.

The device is read in the "reverse" direction compared to programming, by applying the read biases to source electrode (1.5V) and grounding the drain electrode. This reverse read mode can enhance the threshold voltage sensitivity to the localized trapping charges [4]. As shown in Fig. 5, during the first read operation, the "00"and "01" states can be distinguished from the "10" and "11" states at 3.8V (gate voltage). After that, State "11" from State "10" and State "01" from State "00" at 2.8V and 4.8V (gate voltage), respectively, is performed for the second read operation.

Similarly, the bit-3 and bit-4 can be programmed, erased and read by interchanging the role of the drain/source electrodes.

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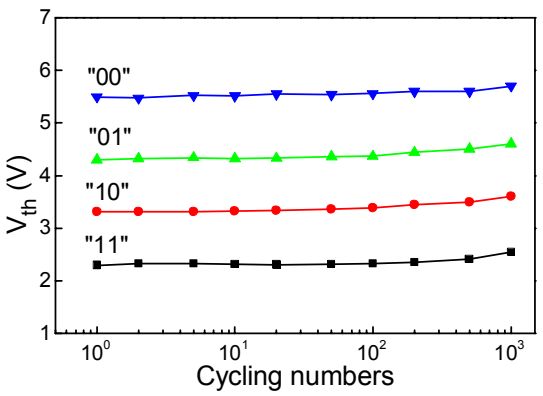

Fig. 7. The Endurance characteristics of the VDNROM flash memory.

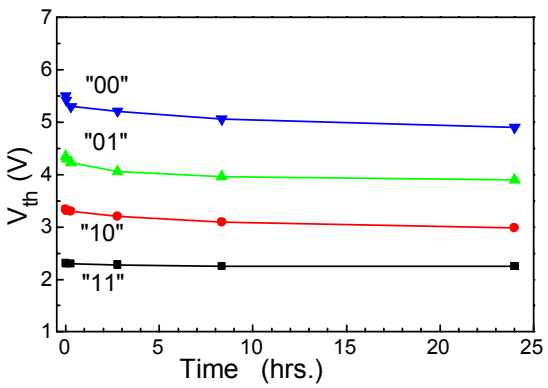

Fig. 8. The bake retention performance of the VDNROM flash memory at 150°C

Fig. 7 shows the endurance characteristics of the four states (corresponding to bit-1 and bit-2). The 2-bit cycling loop consists of the sequence of bit-2 program (State "11" to State "01") →bit-1 program ("01" to "00") →bit-2 erase ("00" to "10") →bit-1 erase ("10" to "11") that can be considered as the worst case, because the tunneling oxide has been tunneled by twice hot electrons and twice hot holes in one cycle (the inter-nitride oxide by once electrons and once holes). After 10^3 P/E cycles, the worst Vth window of 0.8V is maintained in spite of the Vth increase at the erased cell. These electrical results indicate that the cycling endurance performance of the VDNROM cell is acceptable.

Fig. 8 shows the bake retention performance of the VDNROM measured at 150°C. 0.4V small degradation and saturation of Vth are observed after 24 hours baking measurement. With the better quality tunneling oxide, the smaller degradation of Vth window can be observed.

IV. Conclusion

For the first time, a novel VDNROM flash memory cell with an oxide-nitride-oxide-nitride-oxide (ONONO) gate dielectric stack has been proposed, demonstrated experimentally, and successfully operated in four-bits-per-cell mode in the 0.3μm channel length vertical device. In the conventional planar NROM cell, the cell area further scaling is limited by the gate length scaling. In contrast, since the cell area of the VDNROM structure is independent of the gate length, the structure can have high capability of the cell area shrinking with the relaxed requirement of the gate length scaling. Moreover, the fabrication of the VDNROM is basically compatible with planar CMOS technology. The reliability performances including the cycling endurance and the bake retention at 150°C have also been investigated and are acceptable. This new technology can be used for data storage due to the high density, and for embedded applications due to the simplicity of the process.

Acknowledgment

The authors would like to thank the Microfabrication Laboratory staffs of Peking University for their supports in device fabrication. This work is supported by National Natural Science Foundation of China (No. 90207004) and State Key Fundamental Research Project of China.

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