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A Comparison of N+ Type and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories

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ABSTRACT

The polarity of gates and the threshold voltages are primary parameters that determine the electric fields in the gate stack region of non-volatile memories. This field is central to programming, retention and the other characteristics of the devices. We have investigated the effect of the gate polysilicon polarity, experimentally, for silicon-oxide-nitride-oxide-silicon (SONOS) memory devices on silicon-on-insulator (SOI) wafers. An ultra-thin oxide-nitride-oxide (ONO) film with high trap density and strong localization of the trapping provides the scalability and retention in our structures. The effect of ONO film, grown and deposited and of doping was simulated and characterized. Retention is affected by the electric field between the control gate and the storage node. Our experiments and simulations verify the consequences of different polarity of control gates through the change in electric field that they cause in retention and erase times for n^+ and p^+ polysilicon gate SONOS memories is verified through the characteristic energies of the processes.

INTRODUCTION

There is broad consensus that achieving both the reliability and low voltages of operation is a very difficult challenge for the floating gate type EEPROM as the gate lengths shrink [1]. The floating-gate-type EEPROM requires a thicker tunneling oxide of more than 7-9 nm to guarantee retention characteristics by suppressing tunneling. This gives rise to a high-voltage operation necessitated by a 6 MV/cm of programming/erase electric fields [2]. Use of distributed storage, thus reducing consequences of leakage paths, is one of the ways of addressing these problems. Advanced thin film technology has resulted in a low voltage operation and long retention characteristics in devices based on Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) [3][4]. Silicon nitride and its interface with silicon dioxide provides an alternative for this charge storage where the highly localized storage of charge at increased number of sites may allow a further scaling of the insulator thickness and a trade-off in other attributes. But, SONOS memory has problems in discharging of the electrons from the traps of silicon nitride. When SONOS memory is discharged, the electrons from a gate electrode are injected into silicon nitride through the top oxide stack. To resolve this problem, we have used p^+ polysilicon gate, which has a higher work function than n^+ polysilicon gate. This decreases the amount of back-tunneling electrons from the gate. In our experiments, the effect of doping levels has been simulated and characterized.

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EXPERIMENT

Figure 1 shows schematic views of n^+ type and p^+ type polysilicon gate SONOS structures. 0.5 um gate width/length devices with n^+ polysilicon/ p^+ polysilicon are fabricated on SOI substrates using conventional CMOS processing technology. Active area is defined by optical lithography method and isolation is achieved by separating islands. The oxide-nitride-oxide layers are stacked with the thickness of 3 nm/5.5 nm/7 nm and Figure 2 shows a transmission-electron micrograph of the cross section of this grown and deposited memory stack where the dark region is silicon nitride. The n^+ type and p^+ type polysilicon layers in each device are deposited using LPCVD. N^+/p^+ implants were employed to achieve doping levels around 10^{20} cm^{-3}. Side walls, source/drain implantations and metallization are utilized in fabrication of the completed SONOS devices.

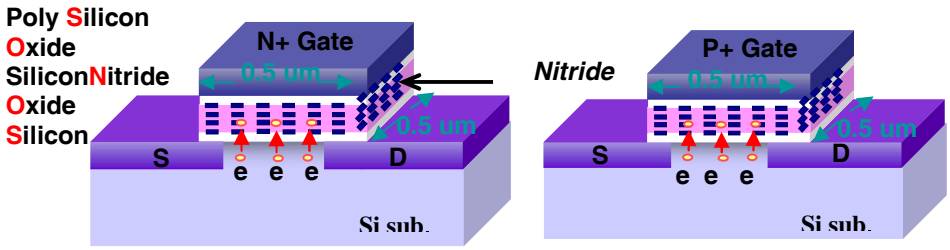


Figure 1. Schematics of n^+ type and p^+ type polysilicon gate SONOS.

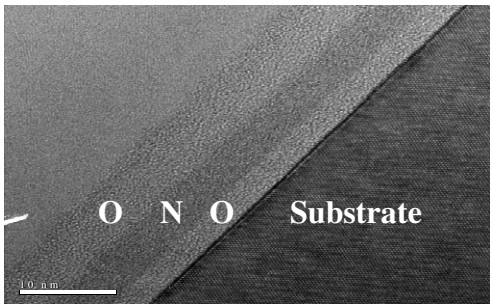


Figure 2. Transmission-electron-micrograph (TEM) of the ONO stack (3 nm / 5.5 nm / 7 nm).

DISCUSSION

Figure 3 shows the energy band diagram of SONOS memory when discharging electrons from the silicon nitride. It has a different energy barrier than for electrons in the polysilicon gate that are tunneling into the silicon nitride through the silicon oxide. The energy barrier between n^+ polysilicon gate and the top oxide is 3.1eV and that of p^+ polysilicon gate with the top oxide is 4.1eV. A higher work function of p^+ polysilicon gate might be expected to improve erase efficiency by reducing electrons back tunneling from the gate. To simulate threshold voltage difference on boron doping concentrations of polysilicon gates in erasure mode, a one-dimensional (1-D) and one band model of charge transport is used, which takes into account Hall-Shockley-Reed statistics for trap population. And the thin oxide between Si and Si_3N_4

facilitates the electron injection because the electric field is amplified in the oxide due to the lower dielectric constant of oxide in comparison to that of nitride [5].

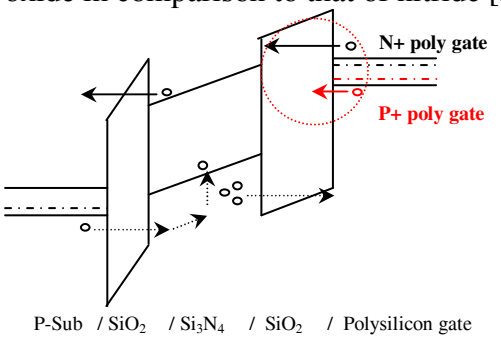


Figure 3. Energy band diagram of n^+ polysilicon and p^+ polysilicon gate SONOS when negative voltage is applied to the gate in erasure process.

Figure 4 shows threshold voltage dependence on boron doping concentrations of polysilicon in erasure mode. As the boron doping level is increased, the erasure speed is faster and the erased threshold voltage of p^+ polysilicon gate with over 10^{20} cm^{-3} doping level is below -2.5 V at the erasure pulse of 1 *m*s.

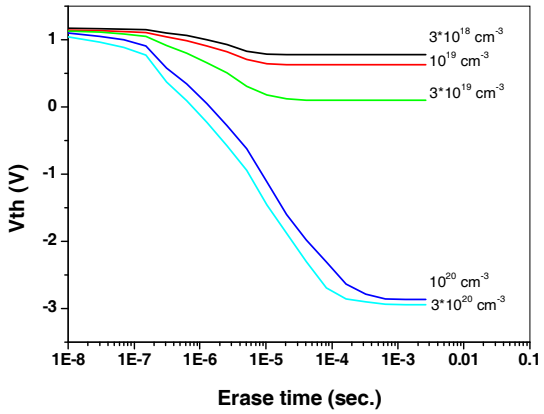


Figure 4. Threshold voltage dependence on boron doping concentrations of polysilicon gates in erasure mode.

Figure 5 shows transfer characteristics with n^+ and p^+ polysilicon gates at 0.5 V drain voltage. The difference of the threshold voltages between devices of n^+ and p^+ polysilicon gates is about 1.1 eV because of the Fermi level difference of n^+ and p^+ polysilicon and the process variance in ONO films in each device. To get high-speed SONOS memory devices, optimization of ONO thickness is very important [6]. The characteristics of ONO layers in these devices are not as good as previous devices. However, it shows clear differences in erasure characteristics. Reducing thicknesses of layers can improve memory speeds but it occurs at the expense of reduced retention time in the limits due to the reduction of tunneling barrier thickness.

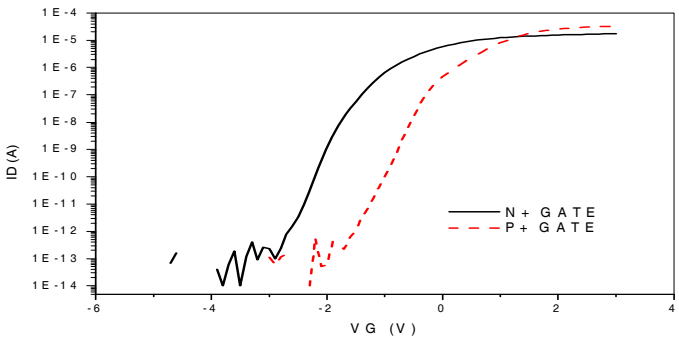


Figure 5. Transfer characteristics of n^+ and p^+ polysilicon gates at 0.5V drain voltage.

Figure 6 shows programming speed characteristics employing field assisted tunneling mechanism. Larger write voltages result in higher tunneling probabilities due to the reduction of the effective barrier. This is observed in these plots as a decrease in writing times with increased applied tunneling voltages. To obtain 4 V of threshold voltage shift, the program time is about 20 us at 16 V program voltage, and this programming time is sufficiently short for usage in semiconductor memories for massive data storage. In Figure 6 we can also see the alteration and differences in program speed behavior for the n^+ and p^+ polysilicon gates near 14 V program voltage.

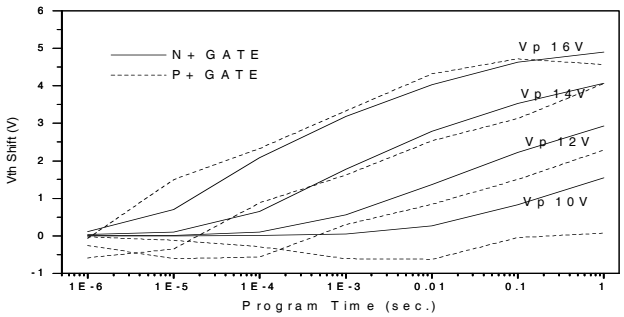


Figure 6. Programming speed characteristics of n^+ and p^+ gate.

The effective field of 14V programming voltage is 10.89 MV/cm and Φ_{os}/X_{ot} is 10.3 MV/cm. Here Φ_{os}, X_{ot} are the energy barrier between silicon and silicon oxide and the thickness of tunneling oxide, respectively. The mechanism of the programming state for $E_{ot} > \Phi_{os}/X_{ot}$ is Fowler-Nordheim (FN) tunneling. In FN tunneling, the programming speed of n^+ and p^+ polysilicon gate memory is almost the same, but in direct tunneling and modified FN tunneling (<14V), the programming speed of n^+ polysilicon gate is faster than that of p^+ polysilicon gate. The erasure time of SONOS memory is somewhat slow because it occurs via the injection of electrons through the top oxide from the gate and because of the heavy effective mass of the hole for hole transport for erasure. To solve this problem, several methods have been introduced recently. The use of high-k material instead of top SiO_2 film would help decrease the number of back-tunneling electrons from the top oxide arising from capacitive coupling. The high-k material has numerous trap charges and the usage of high-k material is significant change from current practice of CMOS processes. We expect that a higher work function of p^+ polysilicon gate will improve the erase speed.

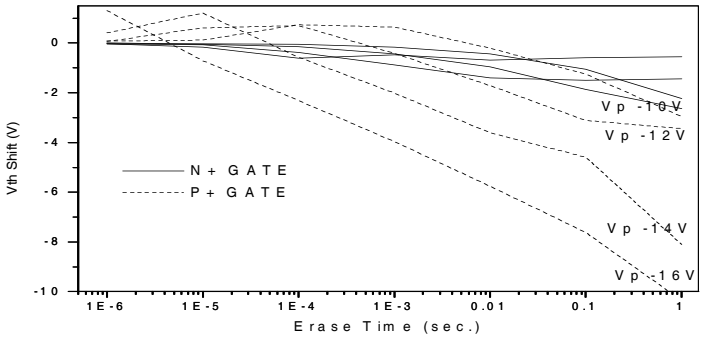


Figure 7. Erasing speed characteristics of n^+ and p^+ gate.

Figure 7 shows erasure speed characteristics by field-assisted tunneling method. The erase speed of p^+ polysilicon gate memory is much faster than that of n^+ polysilicon gate memory. To achieve -4 V threshold voltage shift from a programmed state in p^+ polysilicon gate memory, the erase time is about 1 ms at -16 V erase voltage.

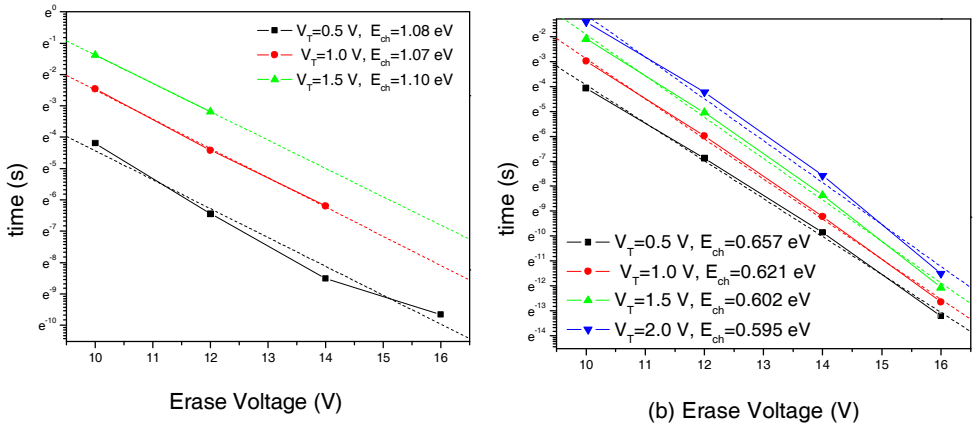


Figure 8. Emission characteristic energy of
(a) n^+ polysilicon gate and (b) p^+ polysilicon gate SONOS.

Figure 8 shows the erasing characteristic energy for various voltages for n^+ type and p^+ type polysilicon gate SONOS memories. The characteristic energy for tunneling for the charging and discharging arises from the tunneling transmission probability, and hence preserves the exponential aspect. Emission process has a higher characteristic energy than a capture process due to the use of a cold mechanism and the erase efficiency of p^+ type polysilicon gate SONOS is improved compared to that of n^+ type polysilicon gate SONOS. The emission characteristic energy of n^+ polysilicon gate SONOS is somewhat larger than that of p^+ polysilicon gate (0.59 ~0.65 eV). Figure 9 shows the endurance characteristics of n^+ and p^+ polysilicon gate memories after various erase and programming cycles. The threshold voltage is changed by 0.3 V in the erasure state of n^+ polysilicon gate memory and by 0.8 V in the program state of n^+ polysilicon gate memory after 10^4 cycles by FN program and erasure. The main reason is that electrons are overcharged into silicon nitride when SONOS memory is programmed. In the case of p^+ polysilicon gate memory, the threshold voltage variance of the program state is 0.35 V and that

of the erase state is over 0.8 V after 10^4 cycles. The different erasure method, i.e. using hot holes, in flash memories causes higher tunnel oxide damage. But it is expected that D_2 annealing treatment may decrease the rate of the degradation of the tunnel oxide.

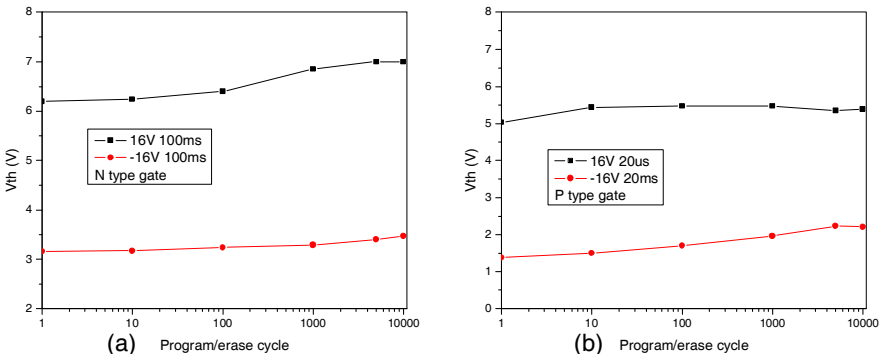


Figure 9. Endurance characteristics of (a) n^+ and (b) p^+ polysilicon gate memories.

CONCLUSIONS

According to our simulation, the erased threshold voltage of p^+ polysilicon gate memory with over 1E20/cm^3 doping level was below -2.5 V at the erase pulse of 1 ms. In our experimental results, considering the program/erase threshold voltage window as 4 V in p^+ polysilicon gate memory, the program time is approximately 20 us at 16 V program voltage and the erase time is about 1 ms at −16V erase voltage using FN tunneling method. In conclusion, this study has helped understand trapping/detrapping process in the presence of different fields that are obtained through different polarity control gates. A higher work function of p^+ polysilicon gate can improve erase speed while satisfying other memory characteristic needs such as of endurance.

ACKNOWLEDGMENTS

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