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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
60/940,160	05/25/2007		200	PM2007027CSP		

CONFIRMATION NO. 6240

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
BLDG. 2.2
SAN JOSE, CA95134

FILING RECEIPT

Date Mailed: 06/19/2007

Receipt is acknowledged of this provisional Patent Application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Igor Polishchuk, Fremont, CA;
Sagy Levy, Sunnyvale, CA;
Krishnaswamy Ramkumar, San Jose, CA;

Power of Attorney: The patent practitioners associated with Customer Number 60909

If Required, Foreign Filing License Granted: 06/18/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US60/940,160**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

SONOS Gate Stack With Multiple Oxynitride Layers and High Workfunction Gate Electrode

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PTO/SB/14 (02-07)
Approved for use through 02/28/2007. OMB 0651-0032
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM2007027CSP
	Application Number	
Title of Invention	SONOS Gate Stack With Multiple Oxynitride Layers and High Workfunction Gate Electrode	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Igor		Polishchuk	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Fremont	State/Province	CA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i: US

Mailing Address of Applicant:

Address 1	637 Amberfield Terrace		
Address 2			
City	Fremont	State/Province	CA
Postal Code	94536	Country i	US

Applicant 2 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Sagy		Levy	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Sunnyvale	State/Province	CA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i: US

Mailing Address of Applicant:

Address 1	1139 Parkington Avenue		
Address 2			
City	Sunnyvale	State/Province	CA
Postal Code	94085	Country i	US

Applicant 3 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Krishnaswamy		Ramkumar	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Jose	State/Province	CA	Country of Residence i	US

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM2007027CSP
	Application Number	
Title of Invention	SONOS Gate Stack With Multiple Oxynitride Layers and High Workfunction Gate Electrode	

Citizenship under 37 CFR 1.41(b) [i]	IN		
Mailing Address of Applicant:			
Address 1	1193 Lynbrook Way		
Address 2			
City	San Jose	**State/Province**	CA
Postal Code	95129	**Country**[i]	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	60909		
Email Address	pbj@cypress.com, cmm@cypress.com	Add Email	Remove Email

Application Information:

Title of the Invention	SONOS Gate Stack With Multiple Oxynitride Layers and High Workfunction Gate Electrode		
Attorney Docket Number	PM2007027CSP	**Small Entity Status Claimed**	☐
Application Type	Provisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)		**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☒ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not been and will not be the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ US Representative (37 CFR 11.9)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM2007027CSP
	Application Number	
Title of Invention	SONOS Gate Stack With Multiple Oxynitride Layers and High Workfunction Gate Electrode	

Customer Number	60909

Domestic Priority Information:

This section allows for the applicant to claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c). Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Priority Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			◉ Yes ○ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☒

Organization Name	Cypress Semiconductor Corporation		
Mailing Address Information:			
Address 1	198 Champion Court		
Address 2			
City	San Jose	**State/Province**	CA
Country [i] US		Postal Code	95134
Phone Number	408-545-6962	Fax Number	408-545-6911
Email Address	pbj@cypress.com, cmm@cypress.com		

Additional Assignee Data may be generated within this form by selecting the **Add** button. Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

PTO/SB/14 (02-07)
Approved for use through 02/28/2007. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM2007027CSP
	Application Number	
Title of Invention	SONOS Gate Stack With Multiple Oxynitride Layers and High Workfunction Gate Electrode	

Signature	/Michael Moore/			Date (YYYY-MM-DD)	2007-05-25
First Name	Michael	Last Name	Moore	Registration Number	53346

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Sandisk Technologies, Inc. - Ex. 1037, Page 000008

PM2007027

Title: SONOS gate stack with multiple oxynitride layers and high workfunction gate electrode

Inventors: Igor Polishchuk, Sagy Levy, Ramkumar Krishnaswamy.

Current technology:

Significant improvements in SONOS memory performance have been achieved through band-gap engineering of the gate dielectric (ONO) stack.
Further enhancements are possible if the work function of the gate electrode is increased. Current publications refer to a TANOS technology, where the blocking silicon dioxide layer is replaced with an aluminum oxide layer and the N+ gate electrode is replaced with a metal – tantalum. This new materials (Al2O3 and Ta) present a significant challenge for integration into a present day CMOS fabrication flow.
In contrast, the present invention relies exclusively on the materials with long and proven integration history: A gate stack consisting of a unique combination of silicon oxide, silicon nitride and silicon oxynitride layers (and no exotic high-K dielectrics) and a P+ doped polysilicon gate electrode are used to create an NMOS-type SONOS non-volatile memory device. This proposed device can be easily and inexpensively integrated into a standard dual poly CMOS logic flow (that already has P+ poly implant).

New invention.

The unique features of the proposed process flow are outline below, in reference to the diagrams in Figure1.
The ONO stack is created on silicon substrate by sequentially forming the following layers:

1. tunnel oxide layer
2. 2 or more of distinct nitride layers
3. blocking oxide layer.

In the subsequent steps the ONO stack is selectively removed from the logic areas of the substrate, and a thermal oxide is grown in the logic areas.
Later a polysilicon layer is deposited over the entire substrate to form the gate electrodes. The polysilicon layer is also implanted with appropriate species either prior to, or following, the gate patterning process. Boron or BF2 implants can be used to implant the gate electrodes of both non-volatile NMOS SONOS memory transistors and the PMOS logic transistors.

The advantages of the proposed device are further illustrated by the available experimental data in the following figures. Figure 2 shows that the P+ SONOS gate electrode results in a deeper erase. Figure 3 shows that the P+ SONOS gate electrode additionally improves data retention.

Figure 1.

Key features of fabrication process.

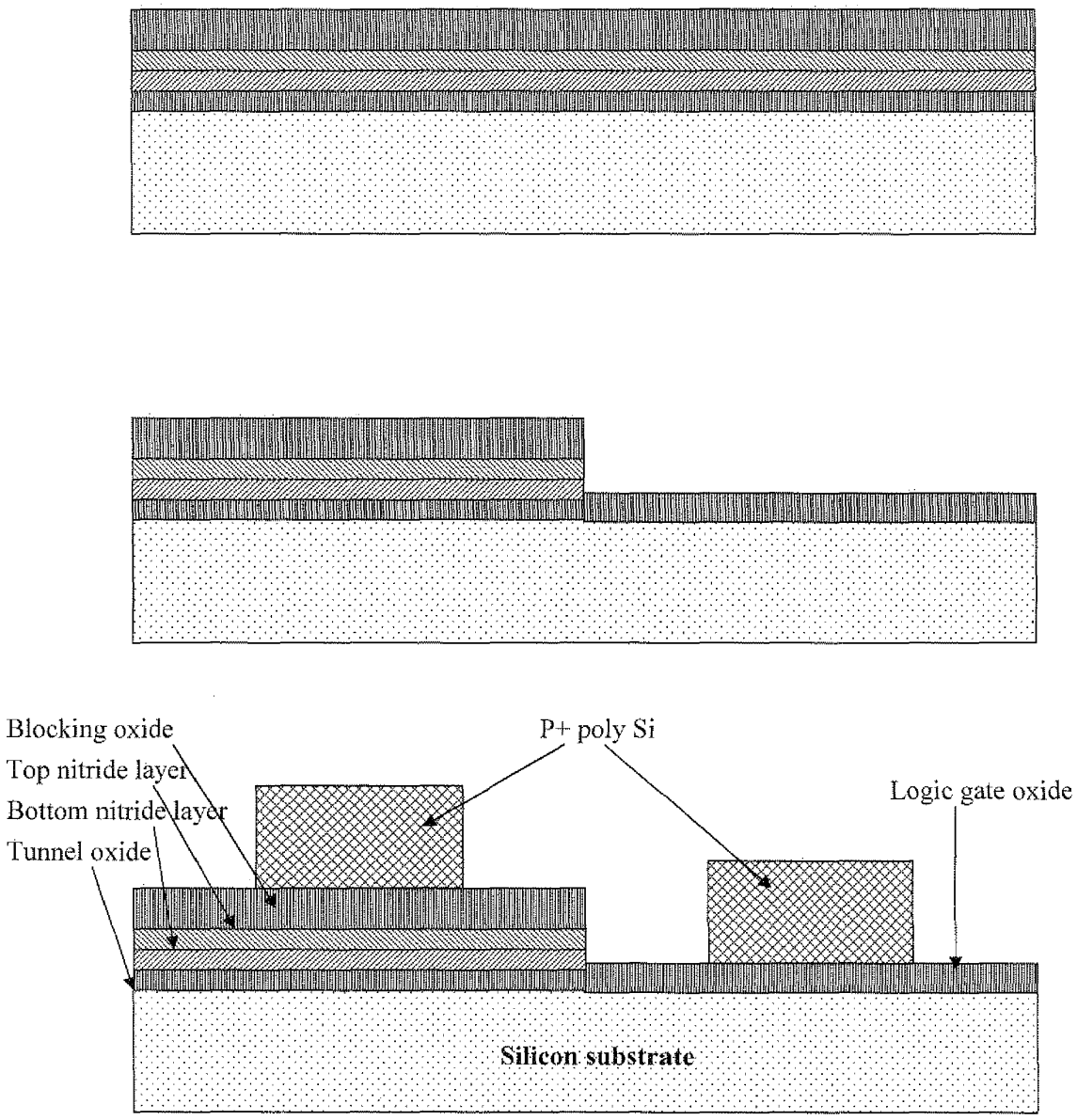


Figure 2. Comparison of the erase/program characteristics for SONOS FETs with N+ and P+ poly gates.

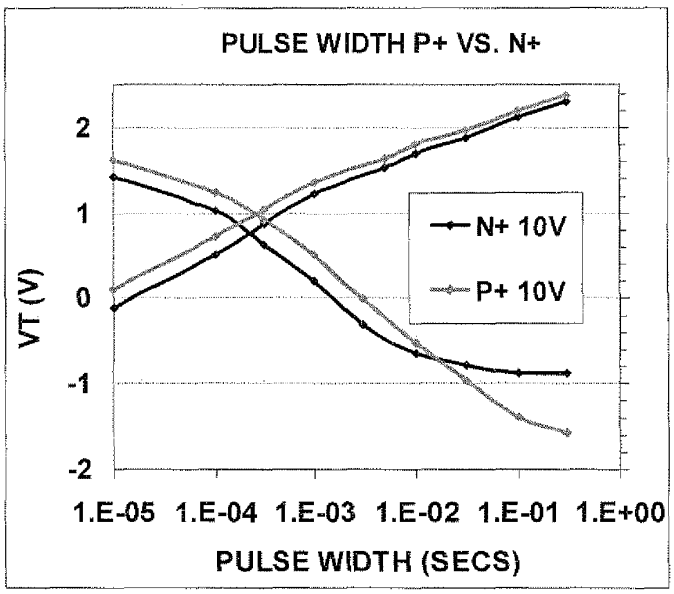
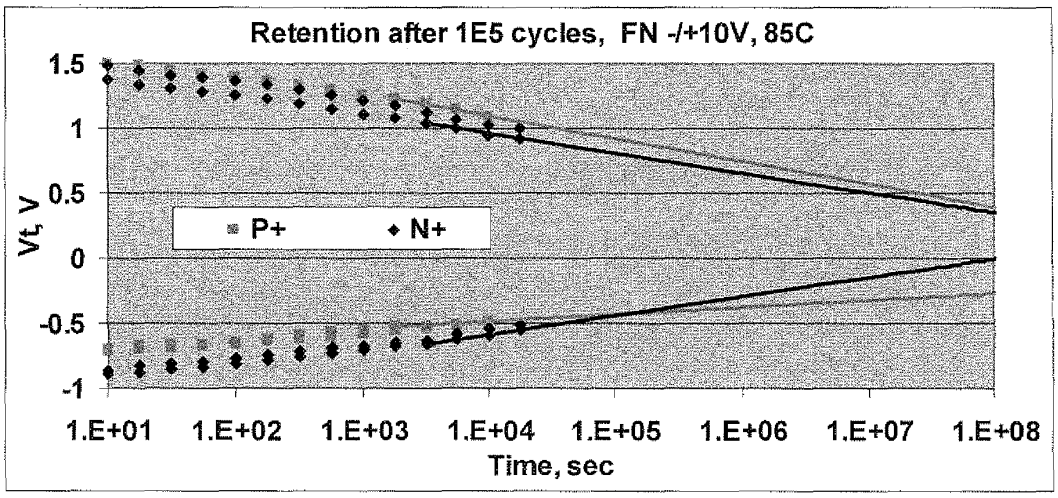


Figure 3. Comparison of the data retention characteristics for SONOS FETs with N+ and P+ poly gates.



IN THE CLAIMS

What is claimed is:

1. A non-volatile NMOS transistor memory structure:
   where the gate stack of the transistor is comprised of an oxide tunneling layer, an oxynitride charge trapping layer that in turn is comprised of 2 or more distinct sub-layers, an oxide blocking layer and a P+ doped semiconductor gate electrode.
2. A structure of claim 1 that is produced in a standard dual-poly gate CMOS logic flow.
3. A structure of claim 2, where the P+ doped semiconductor gate electrodes for the memory NMOS transistors and for the logic PMOS transistor are made by separate processing steps including
   deposition
   masking
   implantation
   anneal
4. A structure of claim 2, where the P+ doped semiconductor gate electrodes for the memory NMOS transistors and for the logic PMOS transistor are made simultaneously by the same processing steps including
   deposition
   masking
   implantation
   anneal
5. A non-volatile transistor memory structure:
   where the gate stack of the transistor is comprised of an oxide tunneling layer, an oxynitride trapping layer that in turn is comprised of 2 or more distinct sub-layers, an oxide blocking layer and a gate electrode formed from a high workfunction material **other than** P+ doped silicon.
6. A method of programming a non-volatile transistor memory structure by Fowler-Norheim tunneling.
7. A method of programming a non-volatile transistor memory structure by hot carrier injection.
8. A non-volatile PMOS transistor memory structure:
   where the gate stack of the transistor is comprised of an oxide tunneling layer, an oxynitride trapping layer that in turn is comprised of 2 or more distinct sub-layers, an oxide blocking layer and a N+ doped semiconductor gate electrode.
9. A structure of claim 8 that is produced in a standard dual-poly gate CMOS logic flow or in a standard single-poly gate NMOS flow.
10. A structure of claim 9, where the N+ doped semiconductor gate electrodes for the memory PMOS transistors and for the logic NMOS transistor are made by separate processing steps including
    deposition
    masking
    implantation
    anneal

11. A structure of claim 9, where the P+ doped semiconductor gate electrodes for the memory NMOS transistors and for the logic PMOS transistor are made simultaneously by the same processing steps including
deposition
masking
implantation
anneal

12. A non-volatile transistor memory structure:
where the gate stack of the transistor is comprised of an oxide tunneling layer, an oxynitride trapping layer that in turn is comprised of 2 or more distinct sub-layers, an oxide blocking layer and a gate electrode formed from a low workfunction material other than N+ doped silicon.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SONOS Gate Stack With Multiple Oxynitride Layers and High Workfunction Gate Electrode
First Named Inventor/Applicant Name:	Igor Polishchuk
Filer:	Penny Jackson
Attorney Docket Number:	PM2007027CSP
Filed as Large Entity	

Provisional Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Provisional application filing	1005	1	200	200
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**200**

Electronic Acknowledgement Receipt

EFS ID:	1812324
Application Number:	60940160
International Application Number:	
Confirmation Number:	6240
Title of Invention:	SONOS Gate Stack With Multiple Oxynitride Layers and High Workfunction Gate Electrode
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Penny Jackson
Filer Authorized By:	
Attorney Docket Number:	PM2007027CSP
Receipt Date:	25-MAY-2007
Filing Date:	
Time Stamp:	14:14:34
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$200
RAM confirmation Number	5748
Deposit Account	503781
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	PM2007027CSPappdatasheet.pdf	1146749	no	5
Warnings:					
Information:					
2	Specification	PM2007027CSPapp.pdf	308701	no	5
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8146	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1463596		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.