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(54) SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

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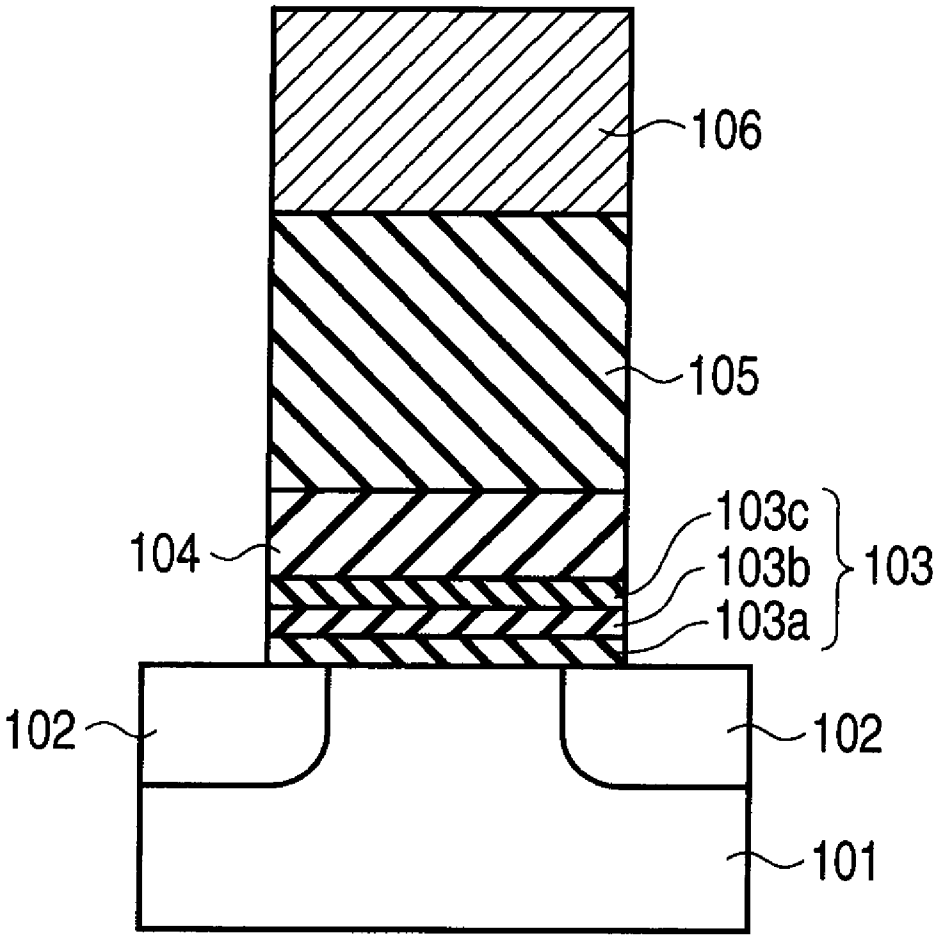
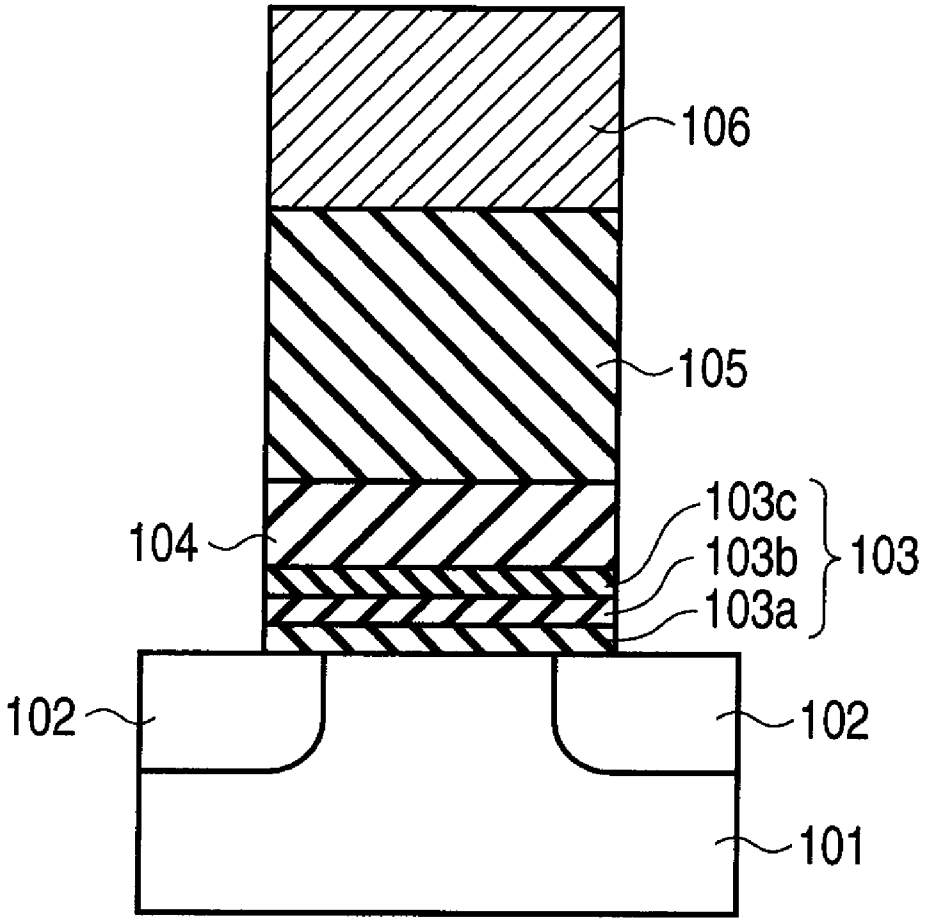
H01L 21/28 (2006.01)

(52) **U.S. Cl.** .. **257/326**; 438/763; 438/591; 257/E21.423; 257/E21.192; 257/E29.309

(57) **ABSTRACT**

A semiconductor device includes a semiconductor region, a tunnel insulating film formed on a surface of the semiconductor region, a charge-storage insulating film formed on a surface of the tunnel insulating film and containing silicon and nitrogen, a block insulating film formed on a surface of the charge-storage insulating film, and a control gate electrode formed on a surface of the block insulating film, wherein the tunnel insulating film has a first insulating film formed on the surface of the semiconductor region and containing silicon and oxygen, a second insulating film formed on a surface of the first insulating film, and a third insulating film formed on a surface of the second insulating film and containing silicon and oxygen, and a charge trap state in the second insulating film has a lower density than that in the charge-storage insulating film.





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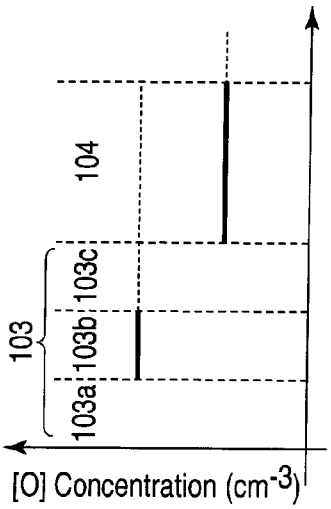
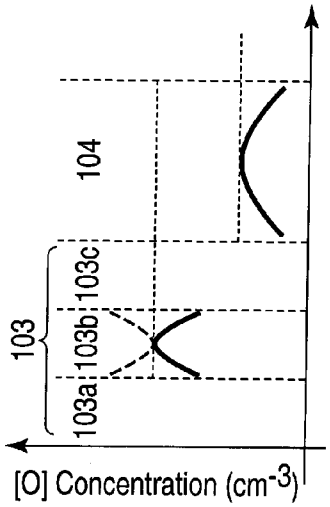


FIG. 2A



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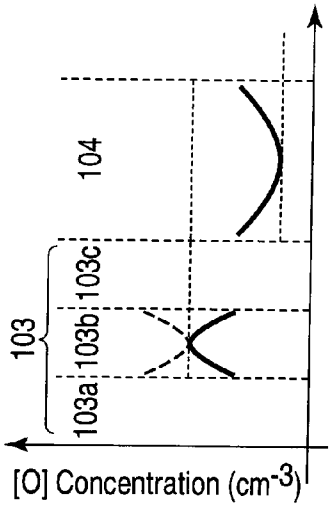


FIG. 2C

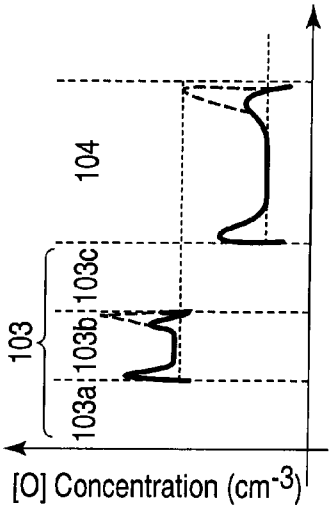
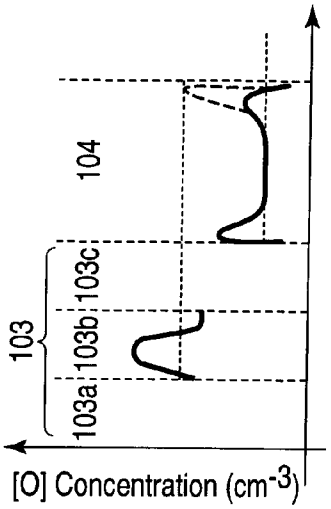


FIG. 2D



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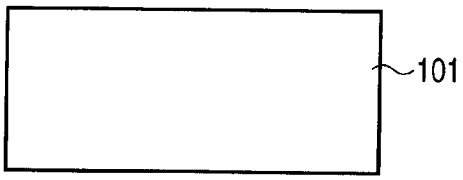
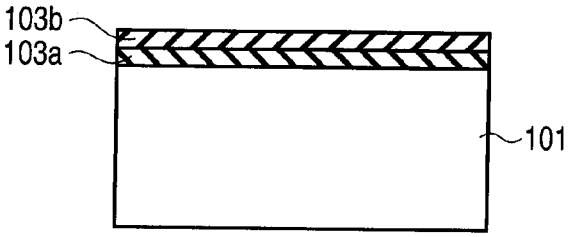


FIG. 3



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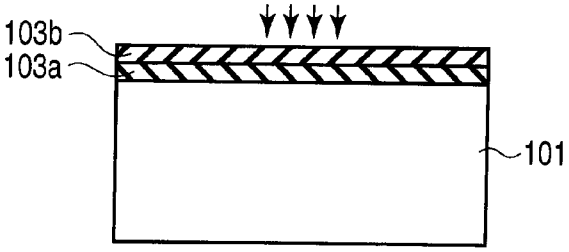
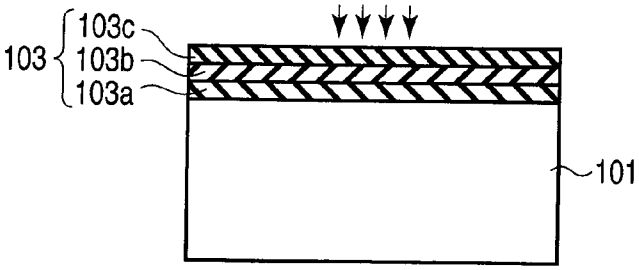


FIG. 5



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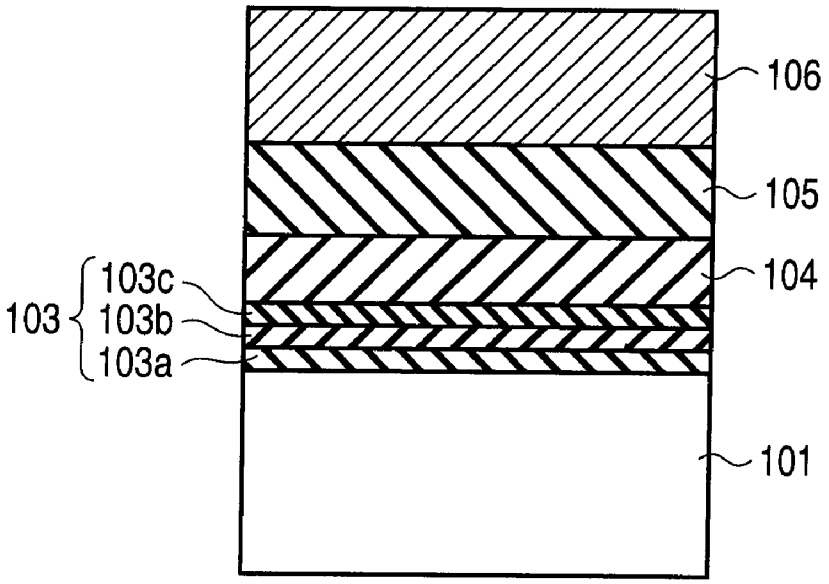
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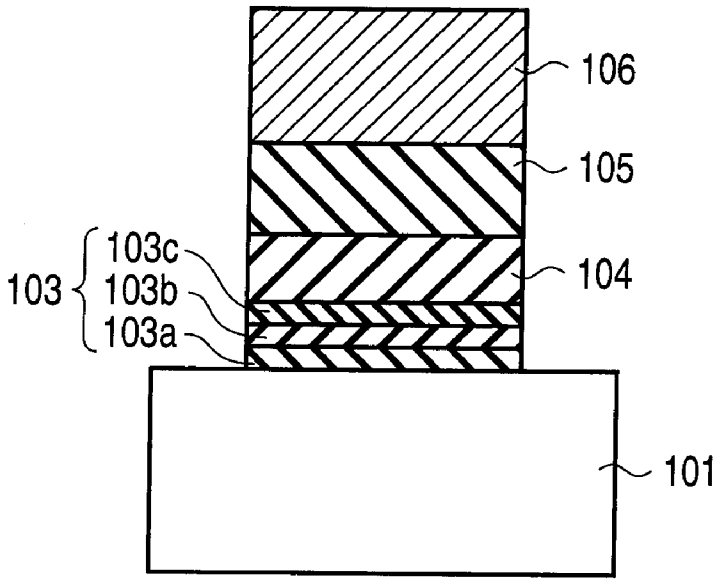
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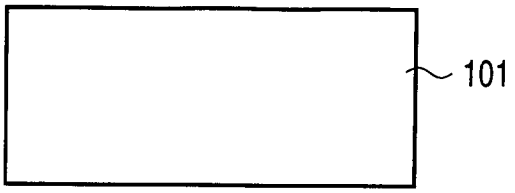

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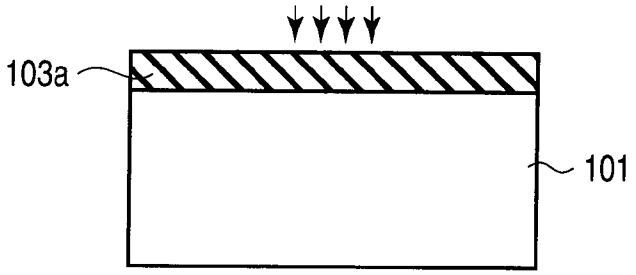
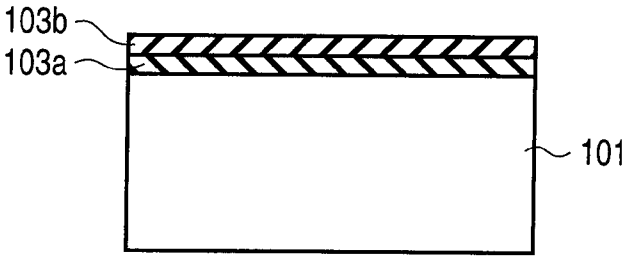


FIG. 10



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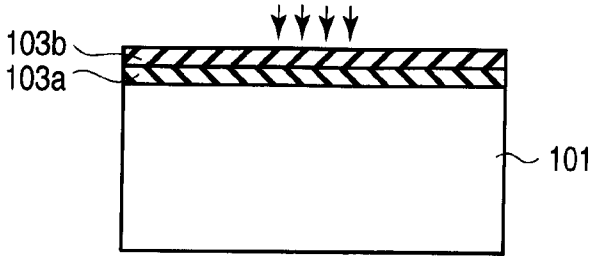

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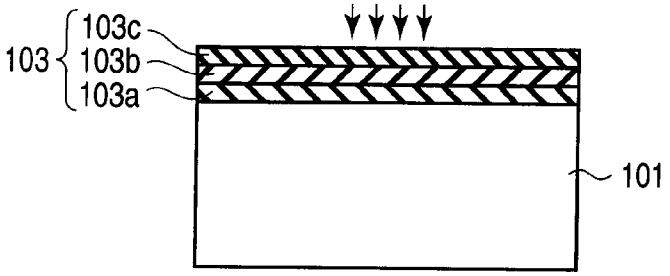

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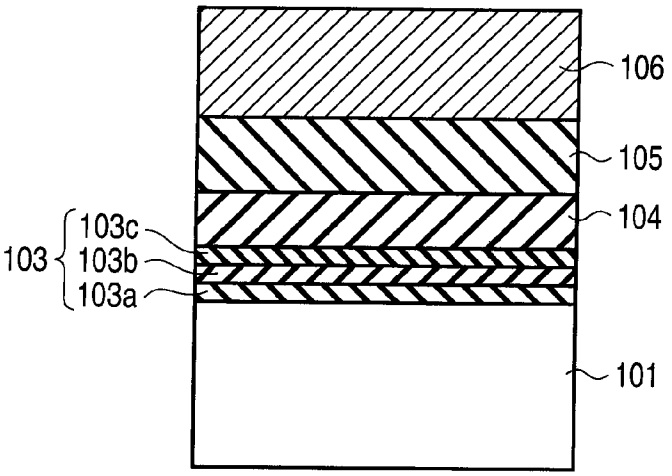

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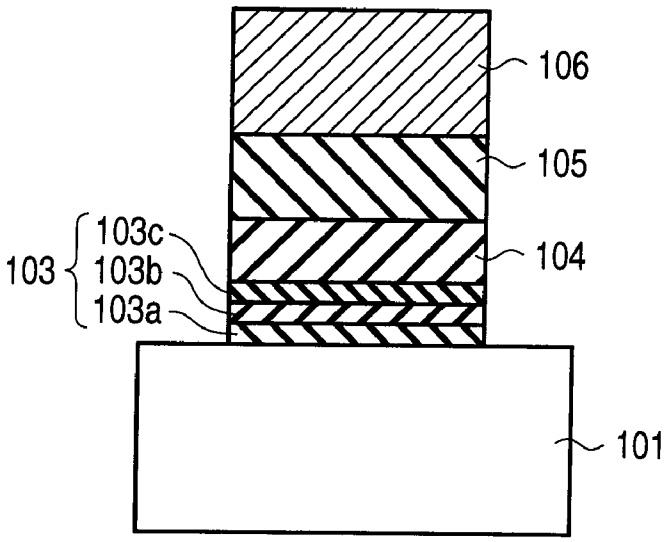
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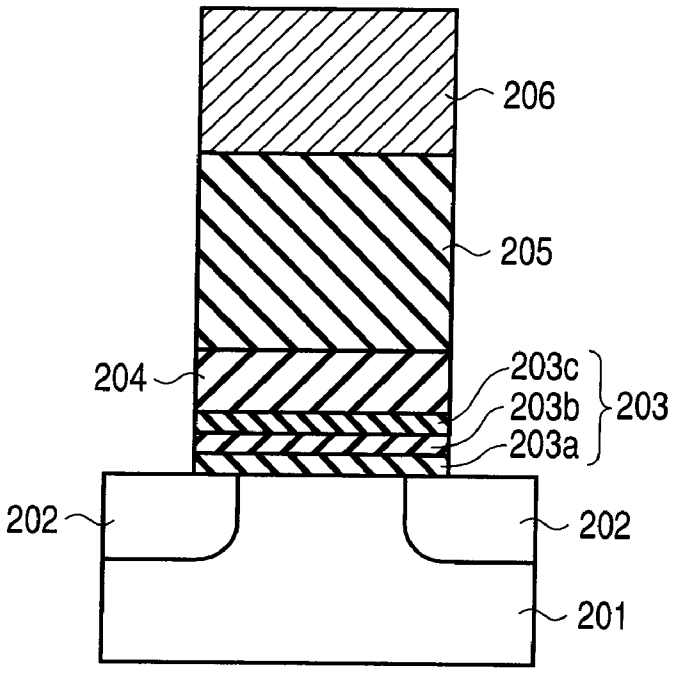
FIG. 15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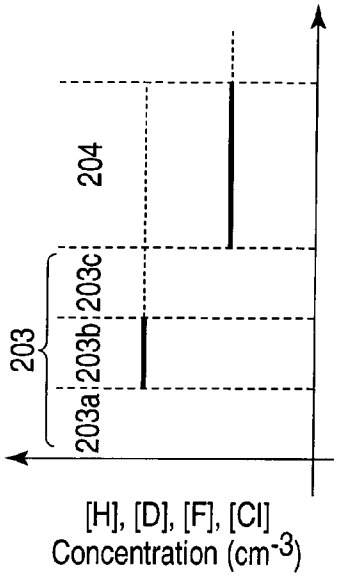

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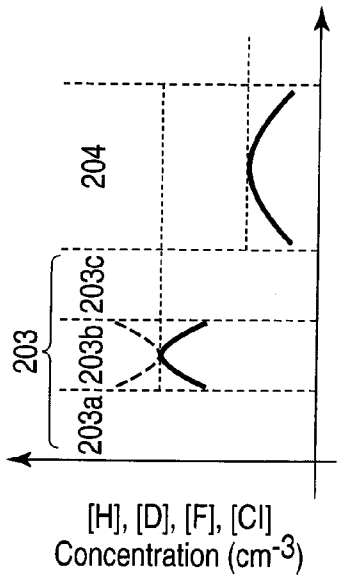

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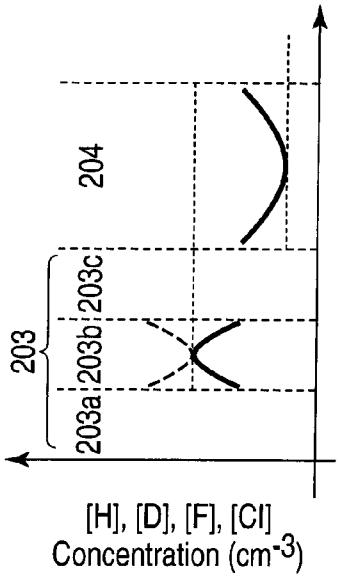

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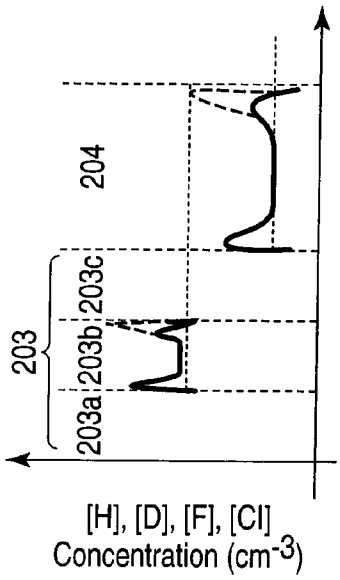

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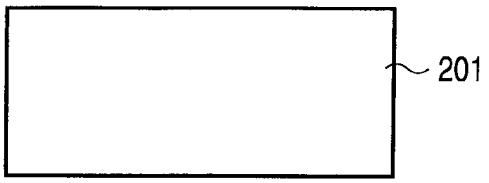

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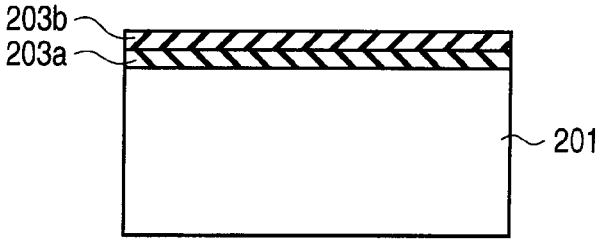


FIG. 19

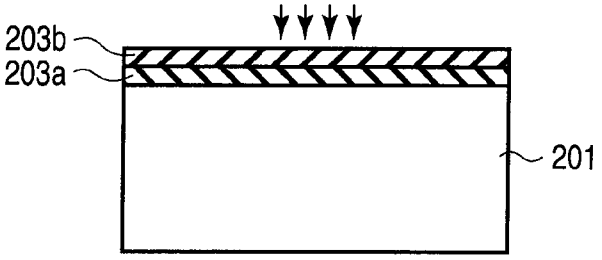
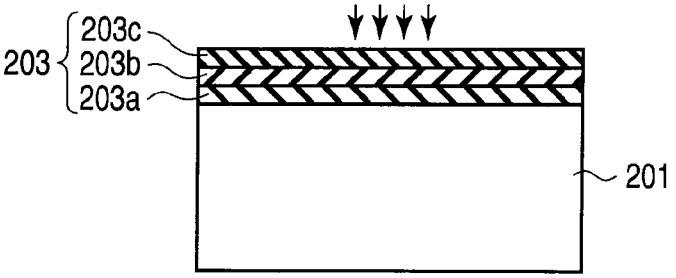


FIG. 20



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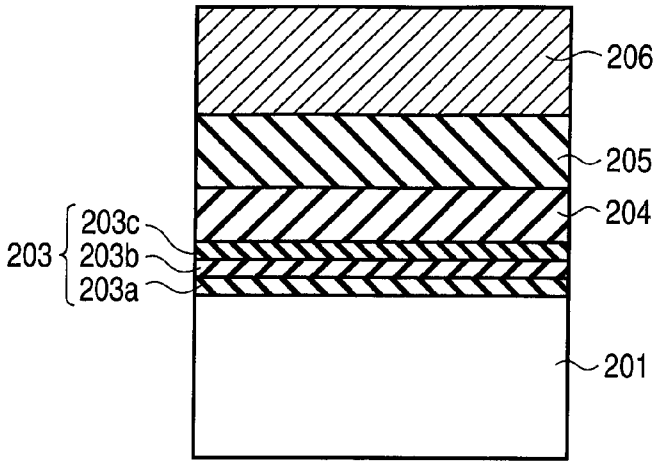

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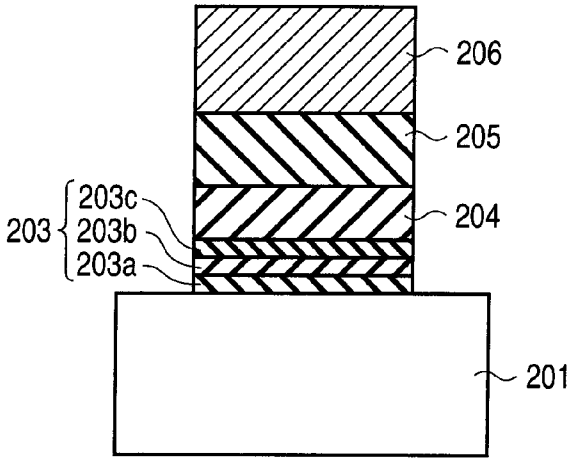

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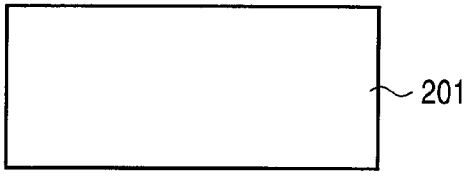

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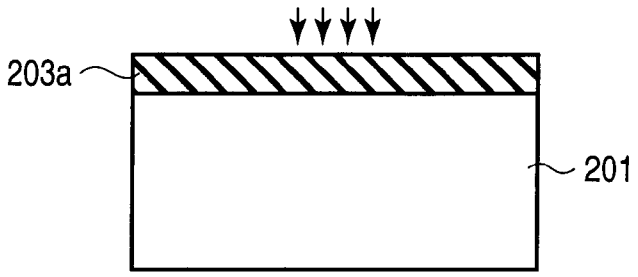

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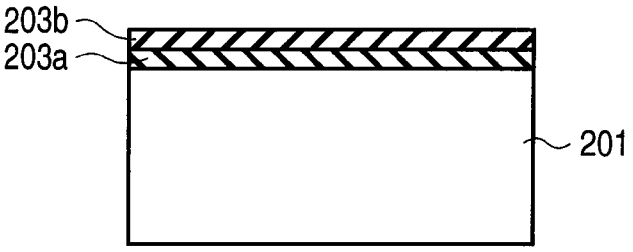


FIG. 26

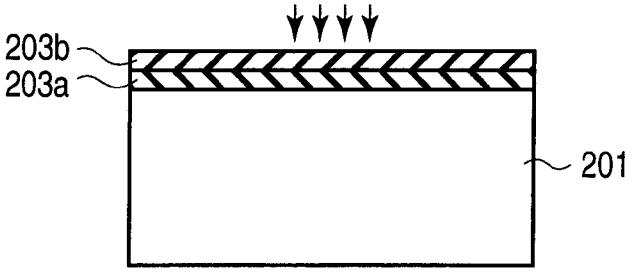
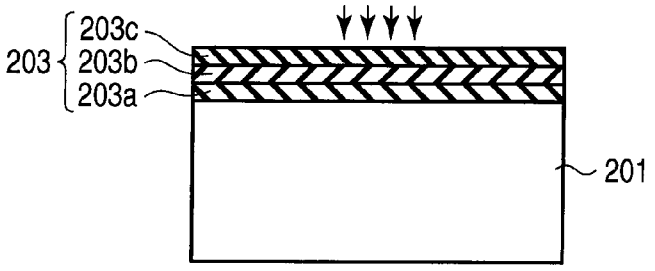


FIG. 27



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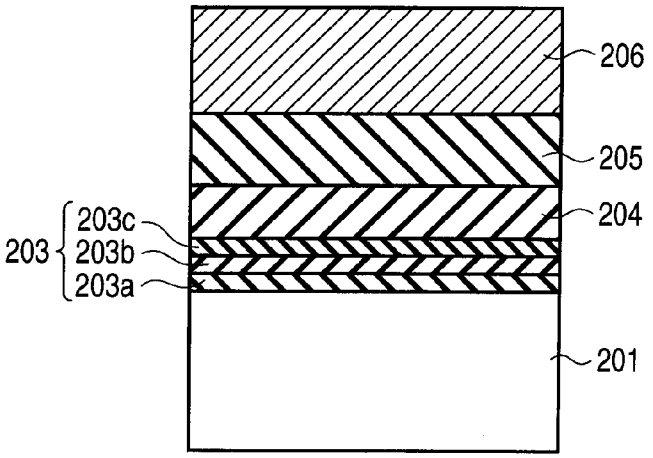

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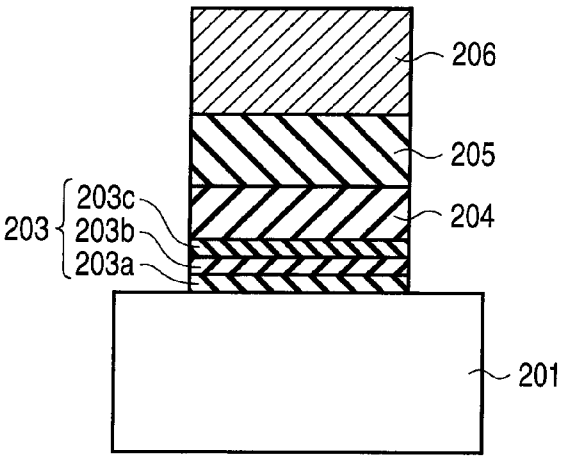

FIG. 30

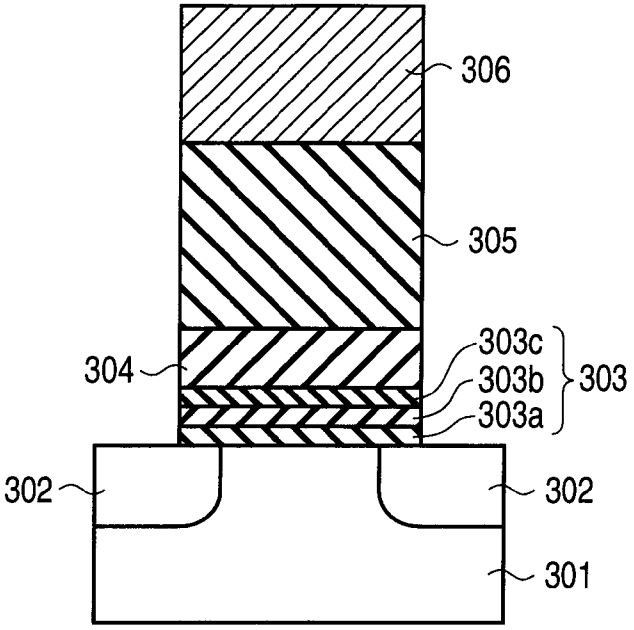

FIG. 31

FIG. 32

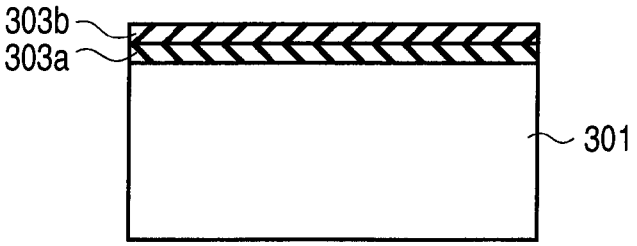

FIG. 33

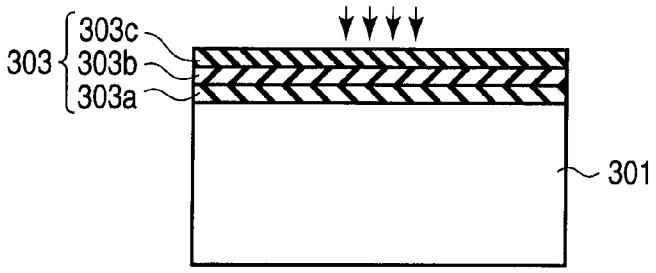

FIG. 34

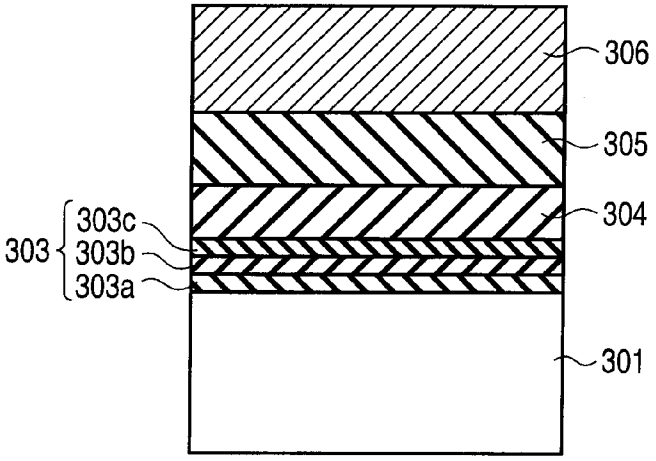

FIG. 35

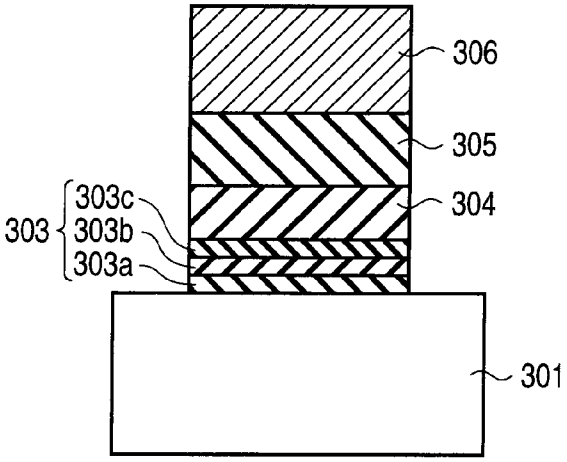

FIG. 36

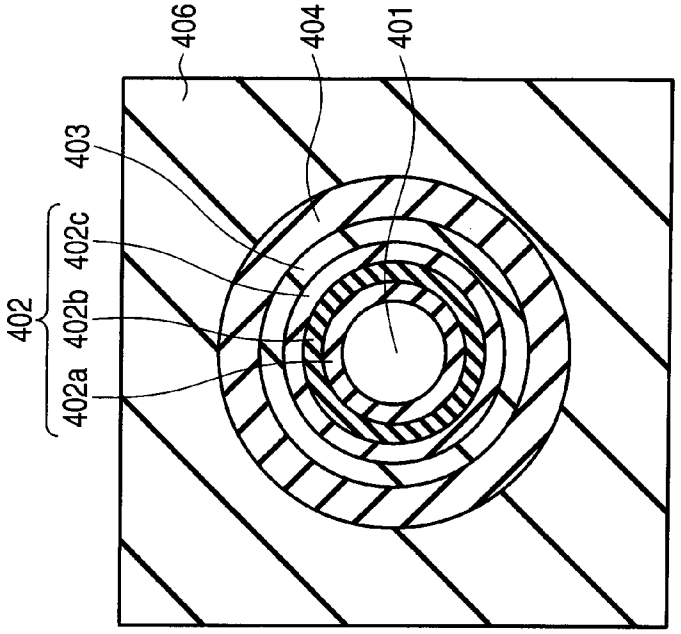

FIG. 37B

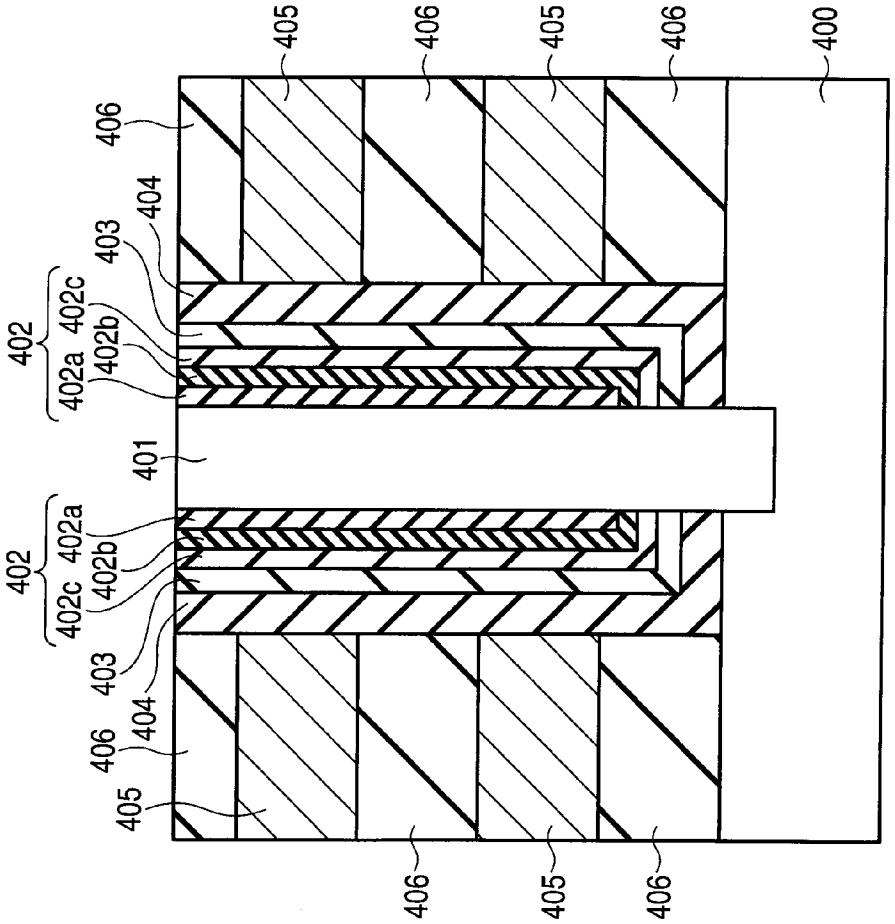

FIG. 37A

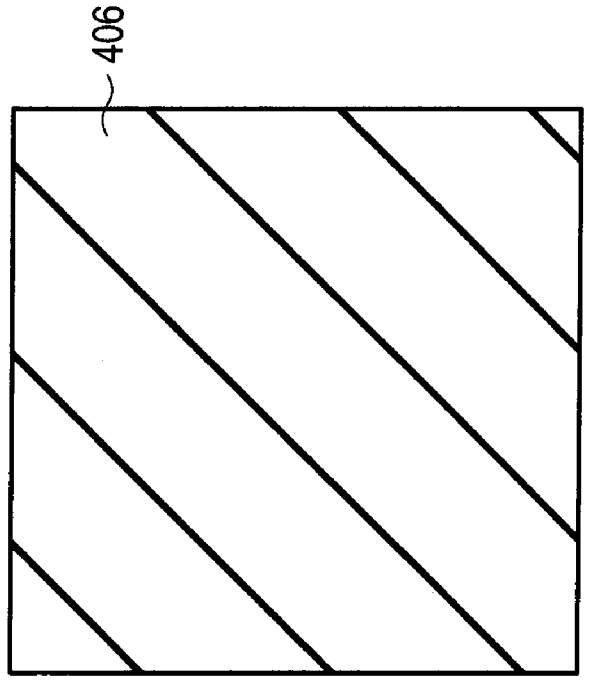

FIG. 38B

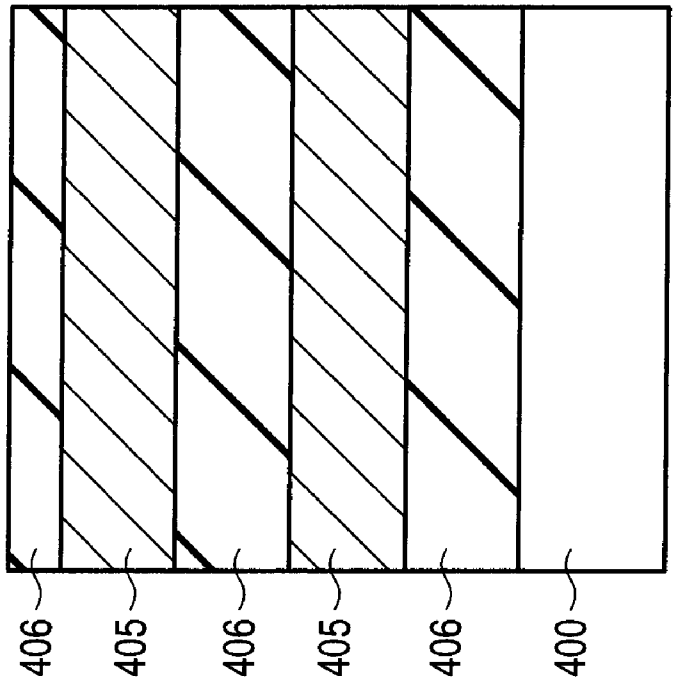

FIG. 38A

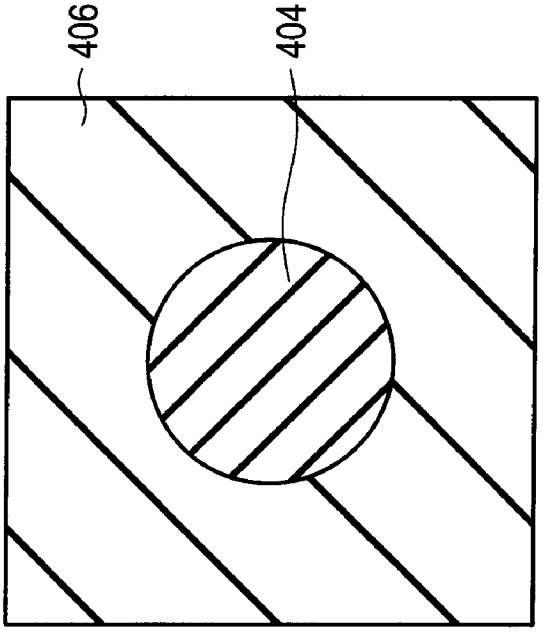

FIG. 39B

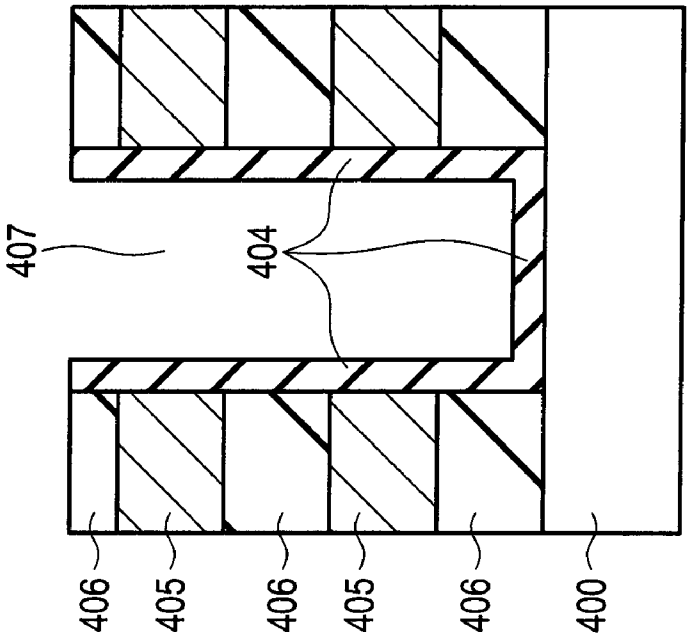

FIG. 39A

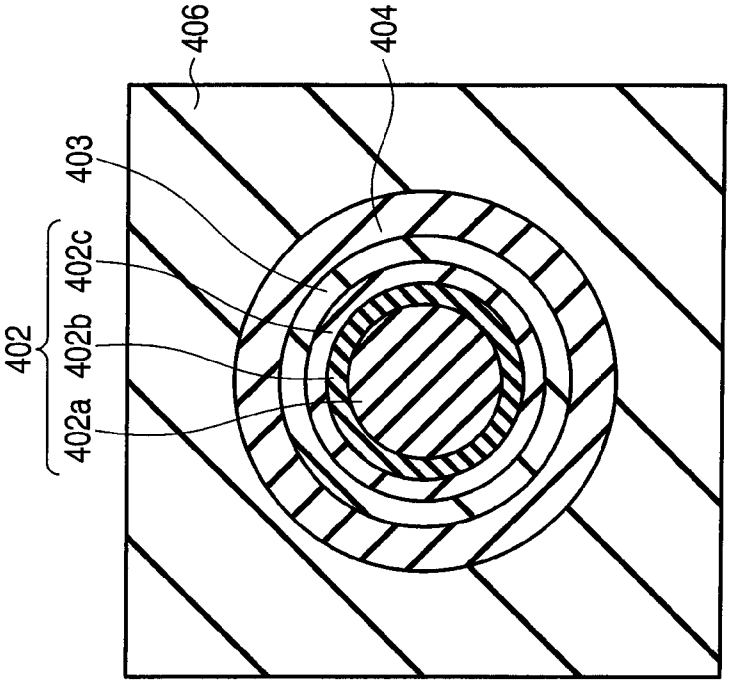

FIG. 40B

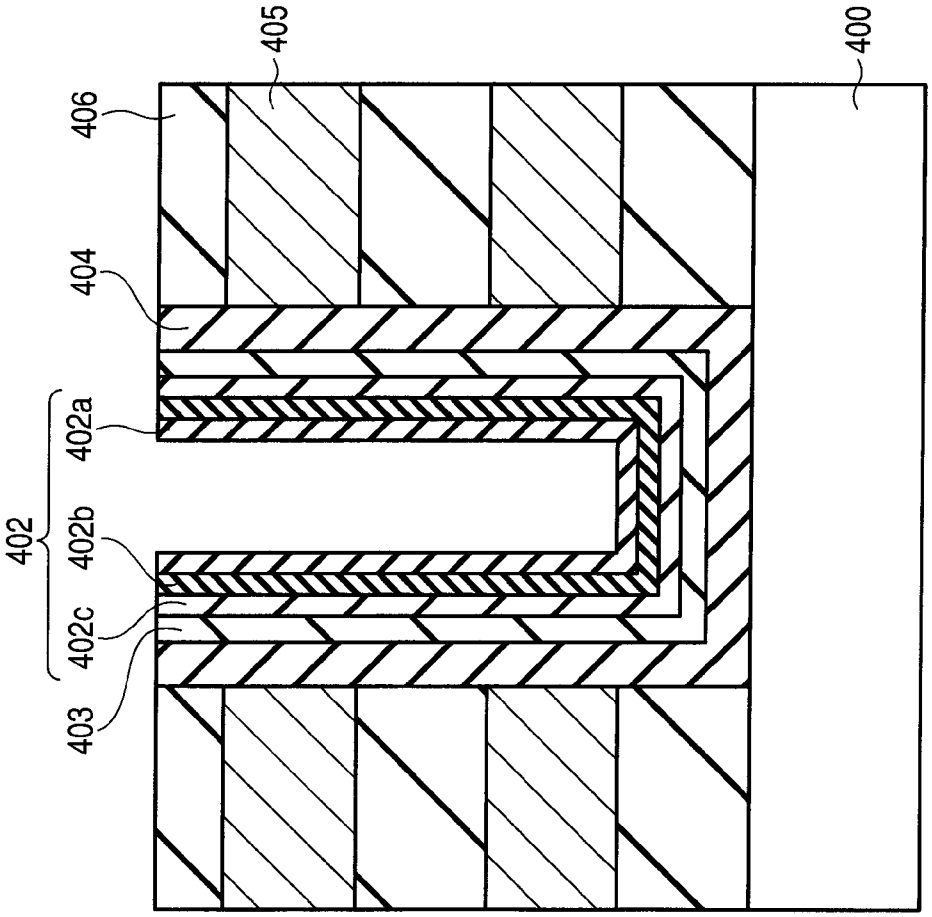

FIG. 40A

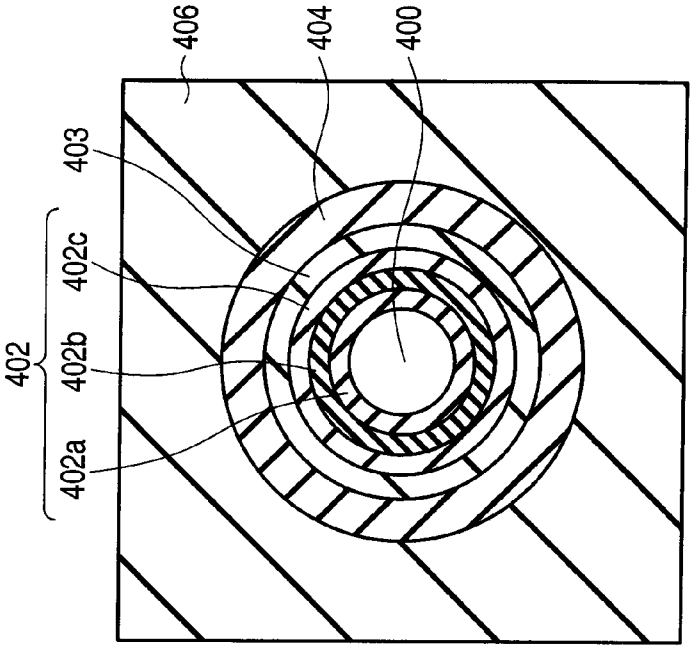

FIG. 41B

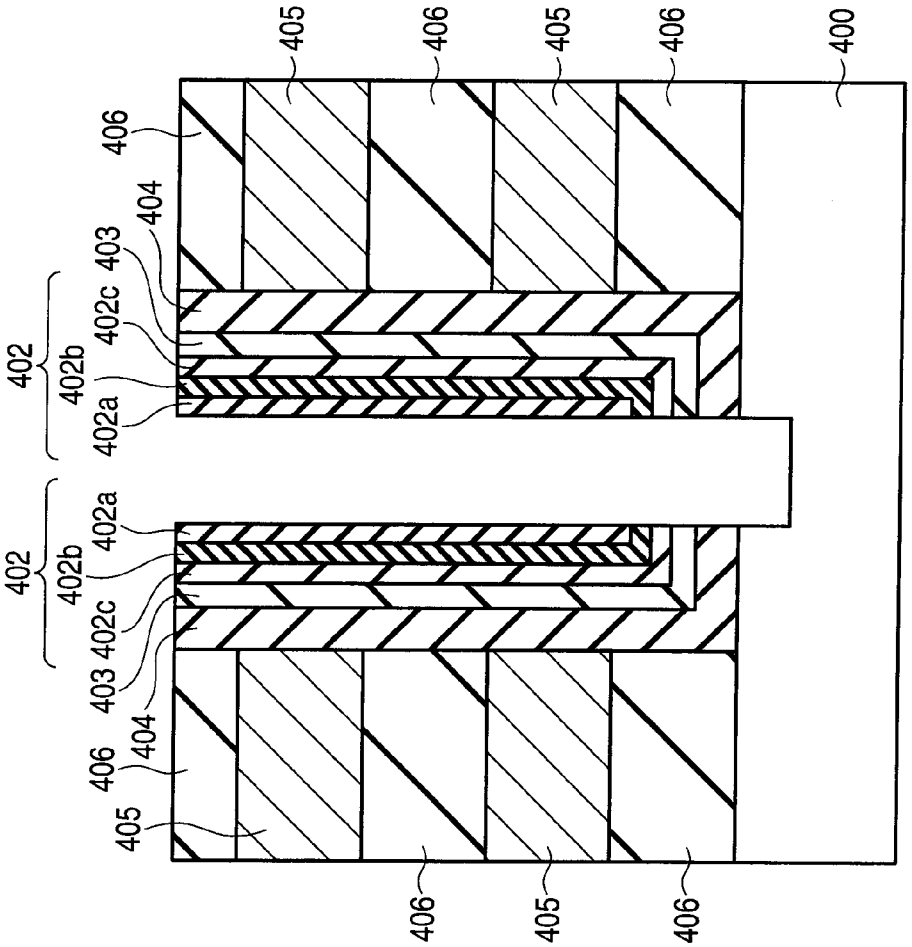

FIG. 41A

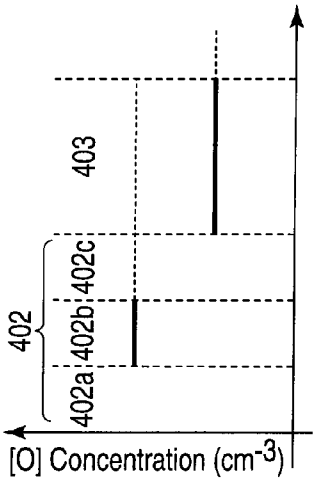

FIG. 42A

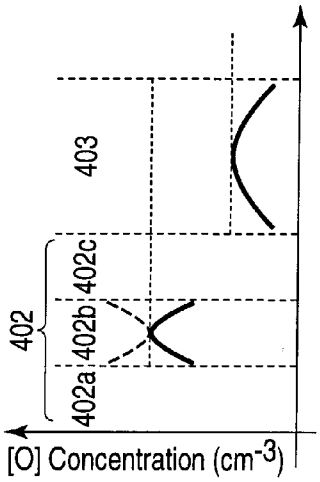

FIG. 42B

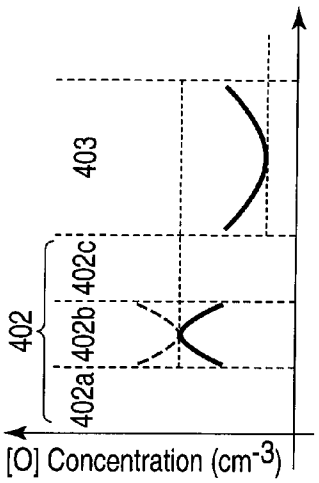

FIG. 42C

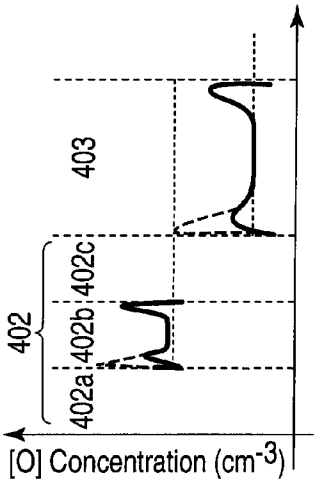

FIG. 42D

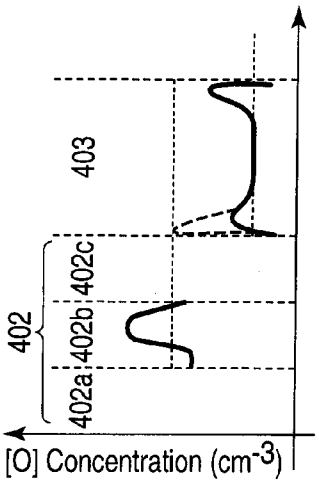

FIG. 42E

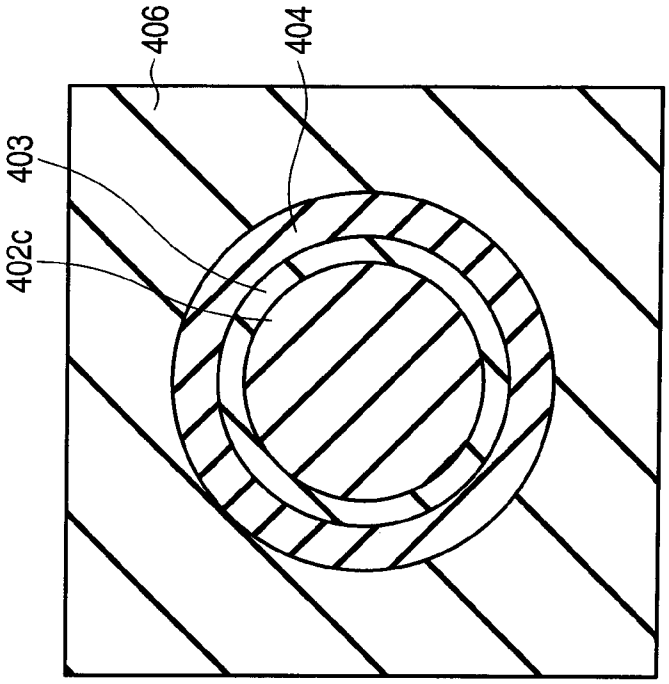

FIG. 43B

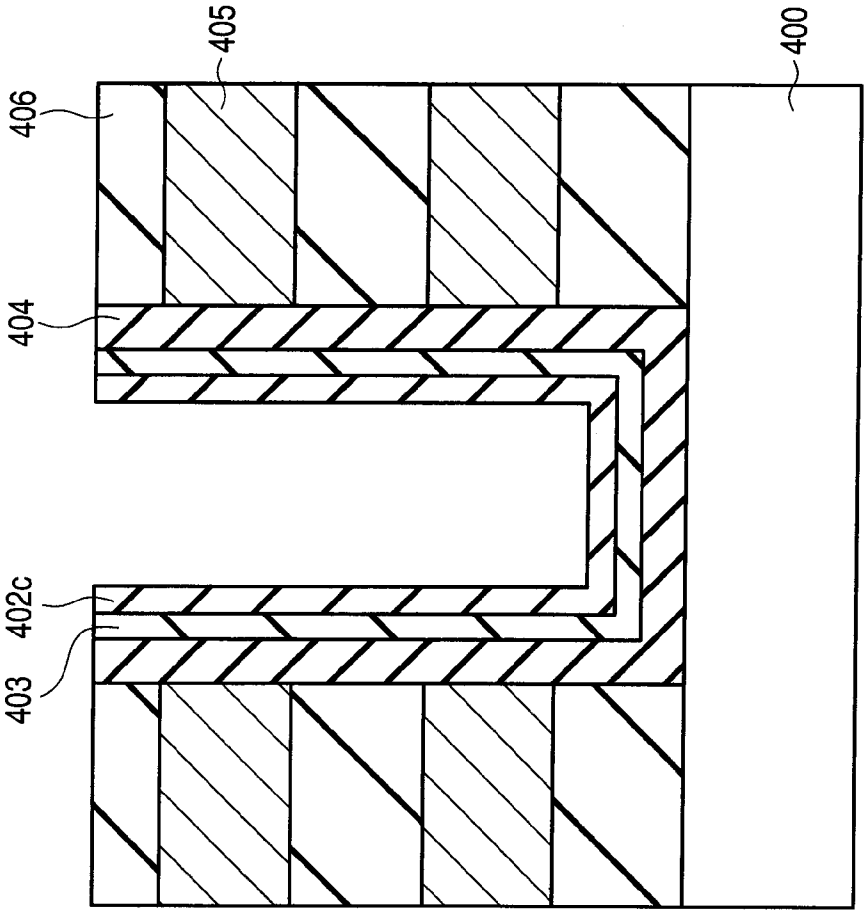

FIG. 43A

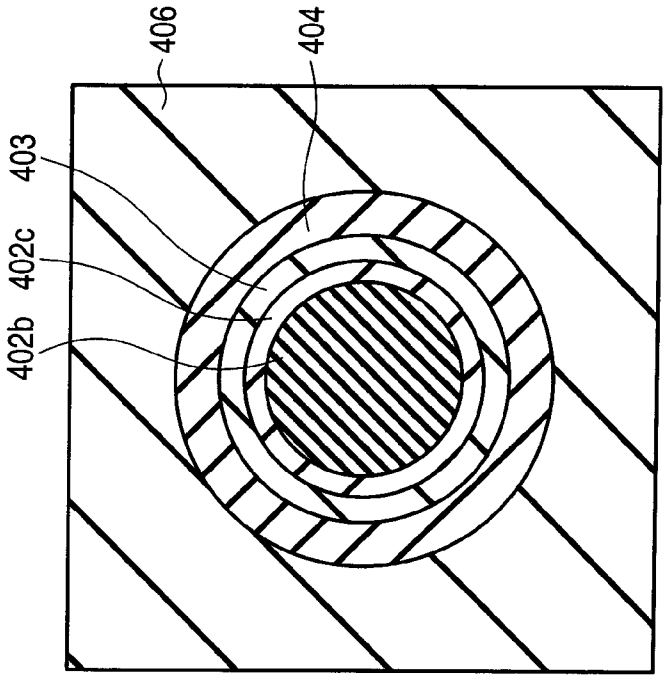

FIG. 44B

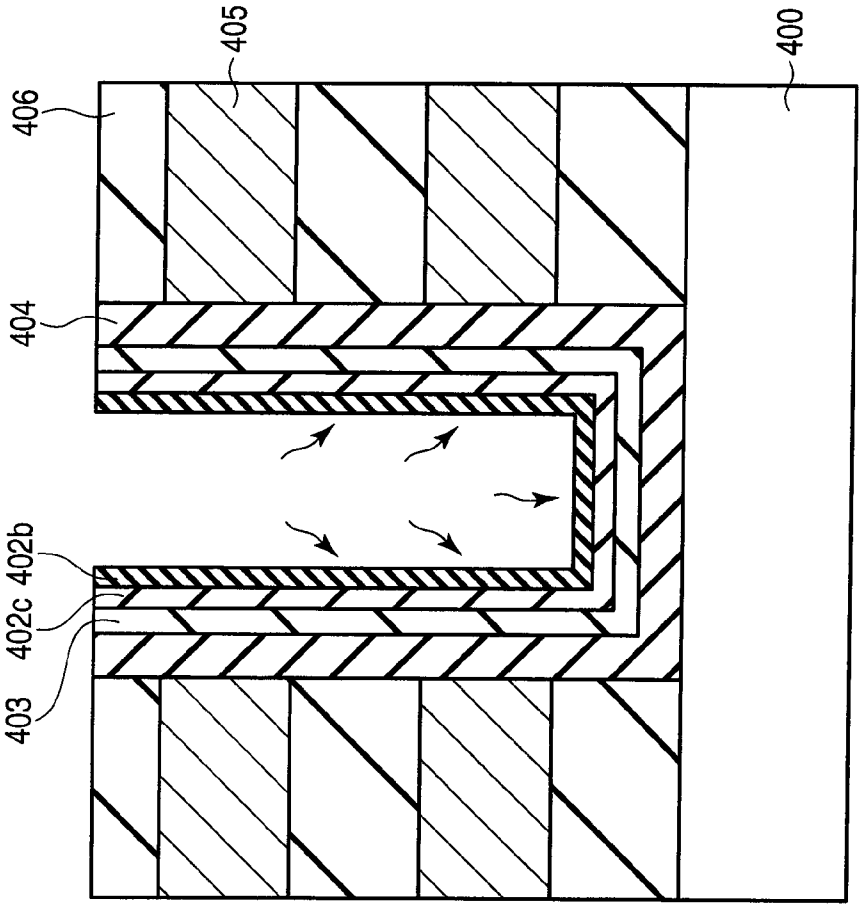

FIG. 44A

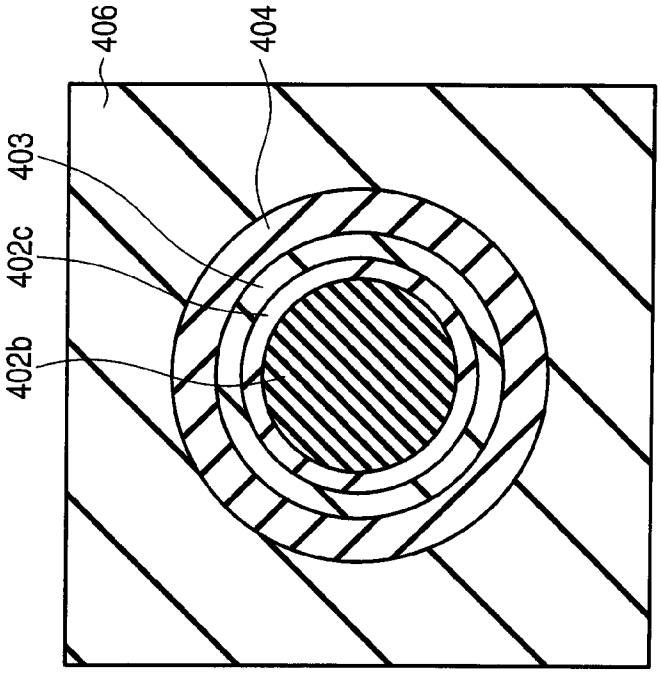

FIG. 45B

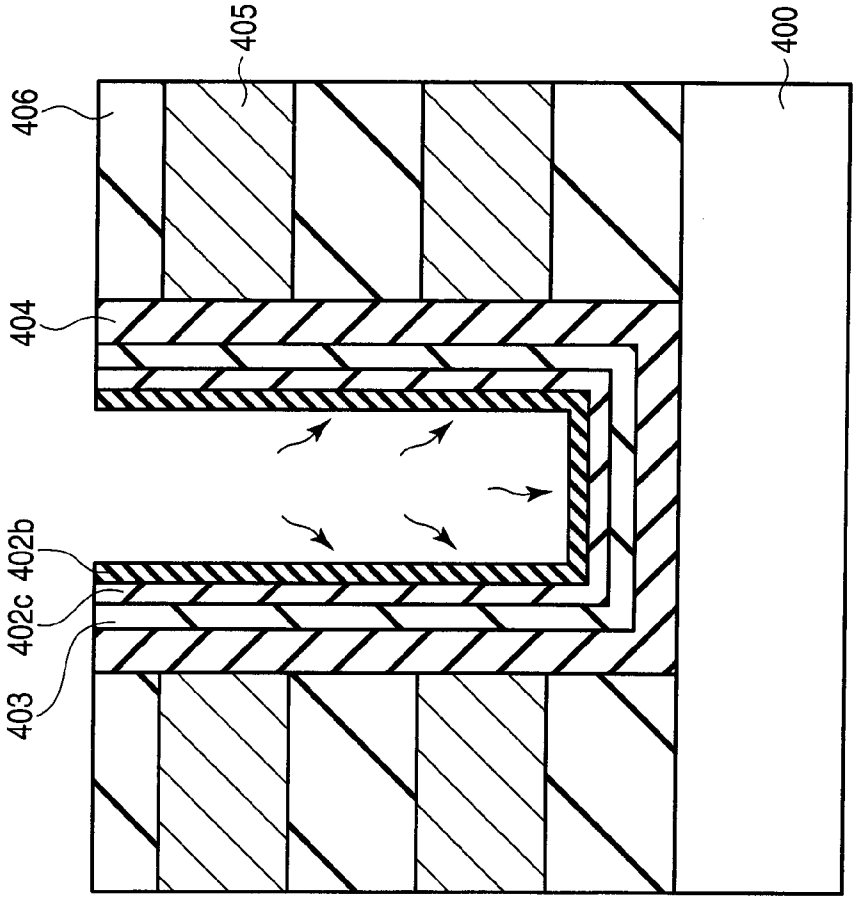

FIG. 45A

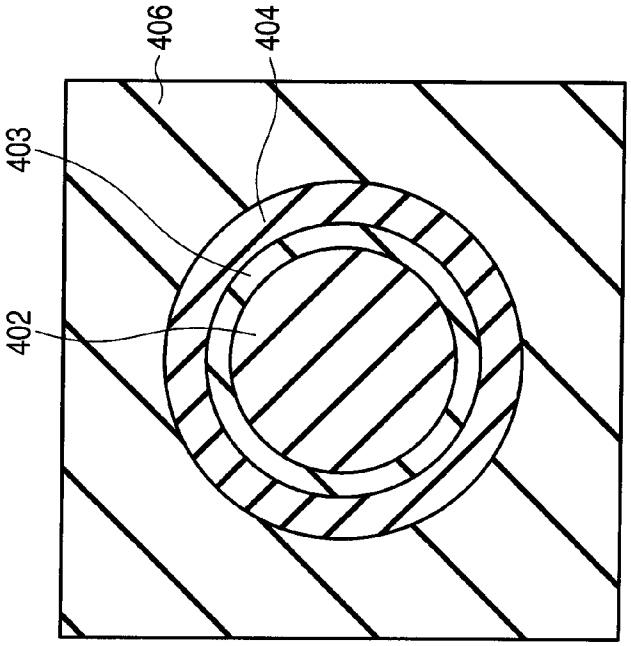

FIG. 46B

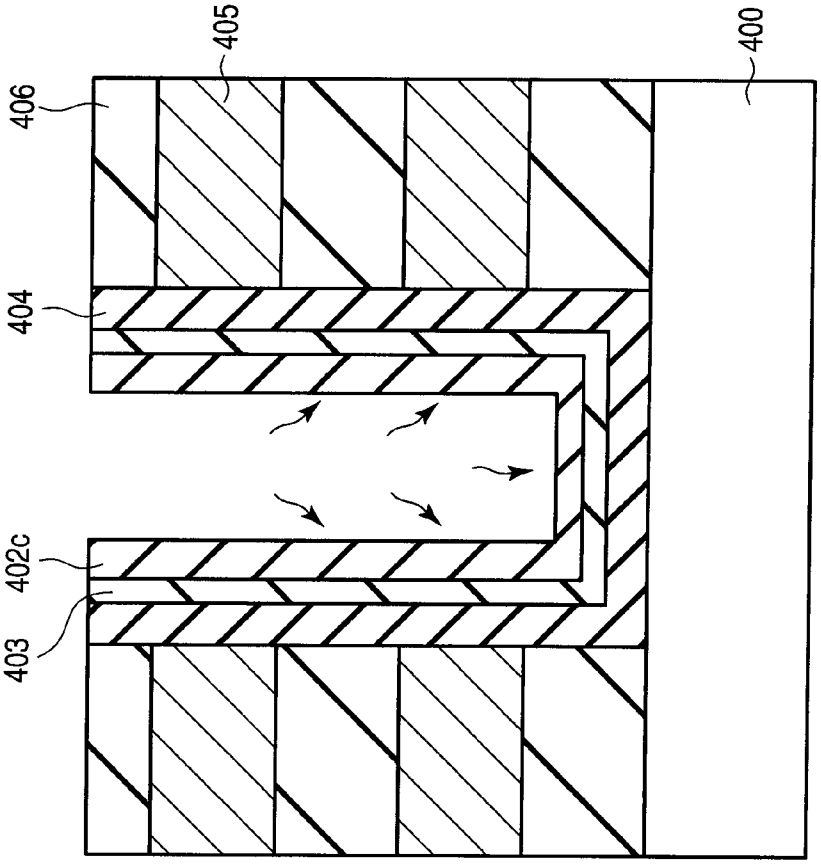

FIG. 46A

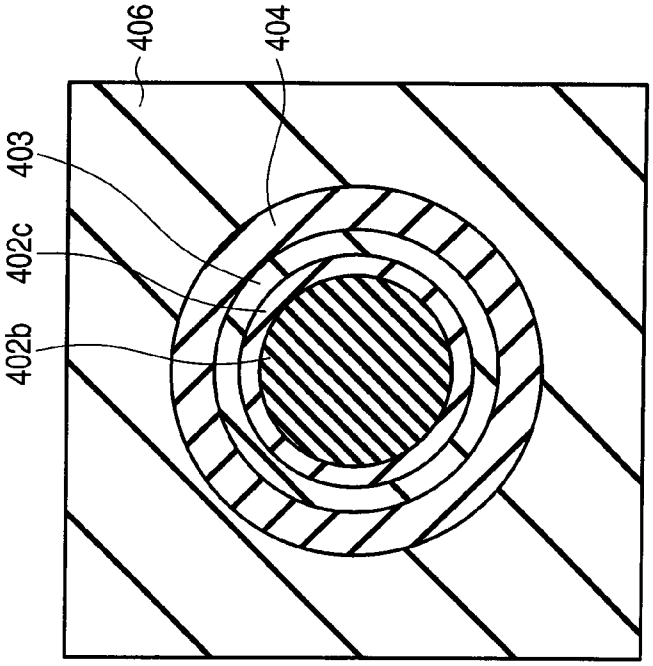

FIG. 47B

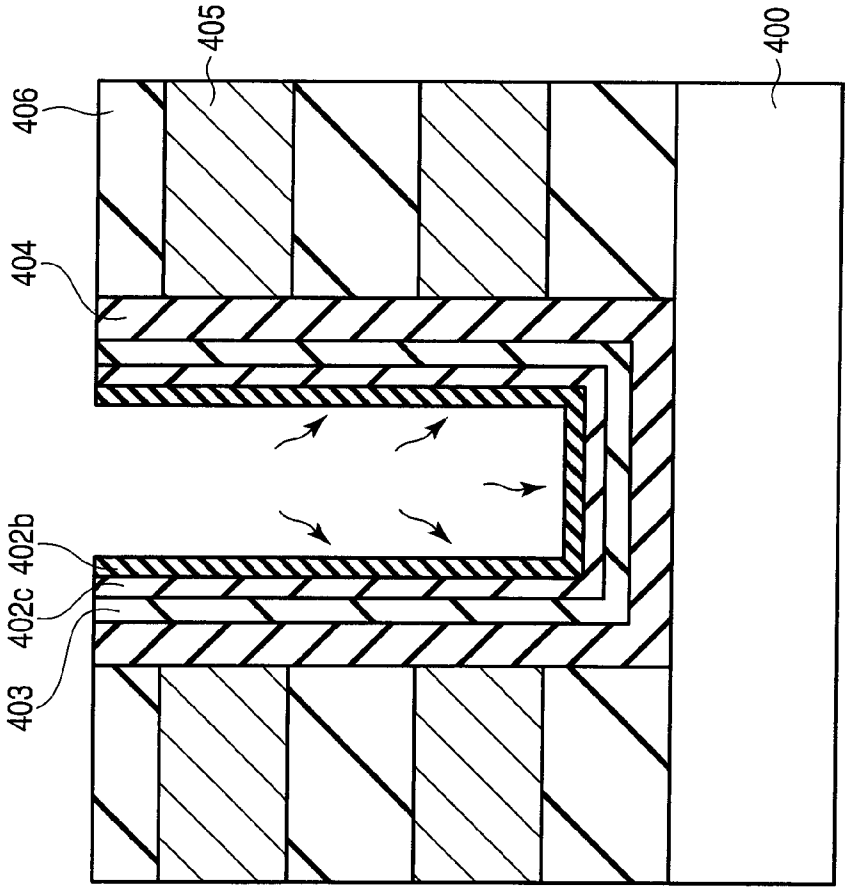

FIG. 47A

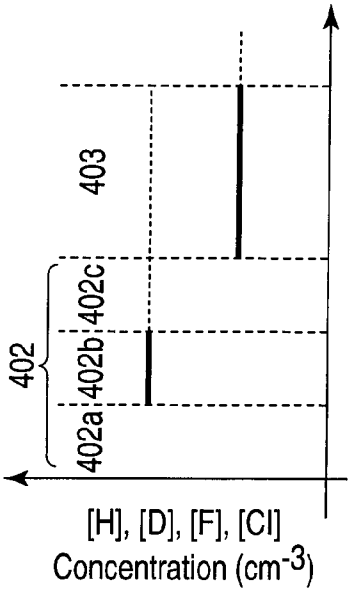

FIG. 48A

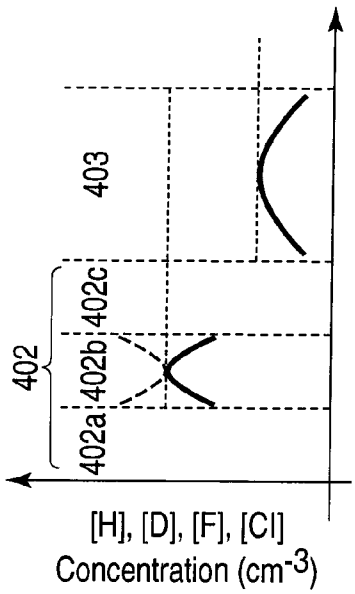

FIG. 48B

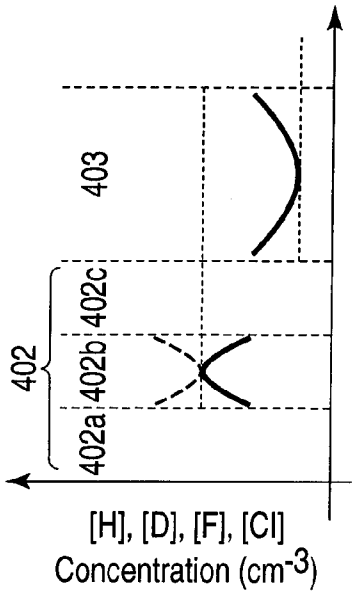

FIG. 48C

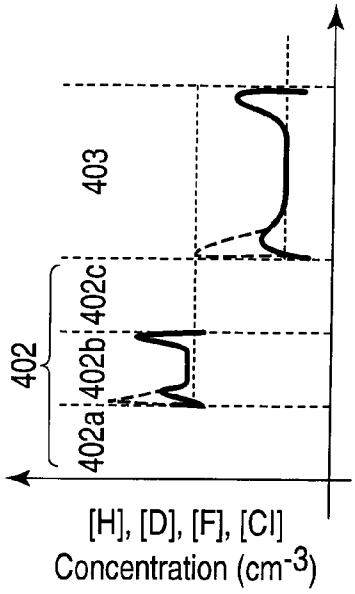

FIG. 48D

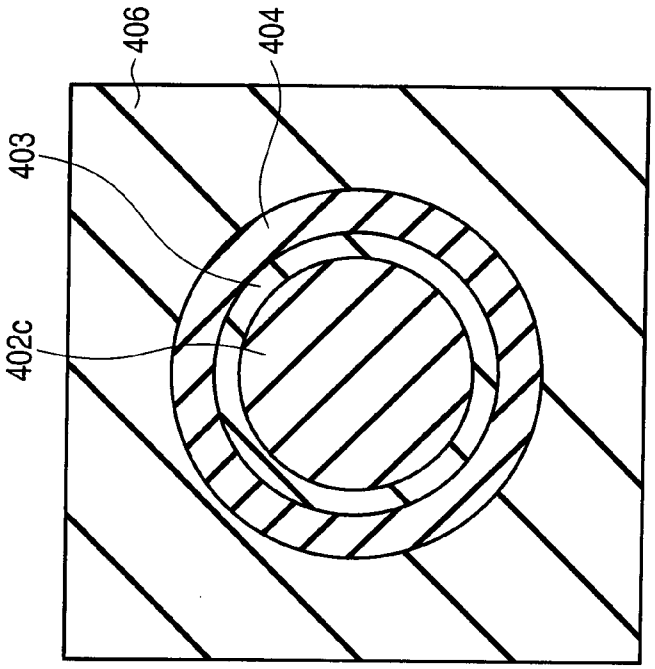

FIG. 49B

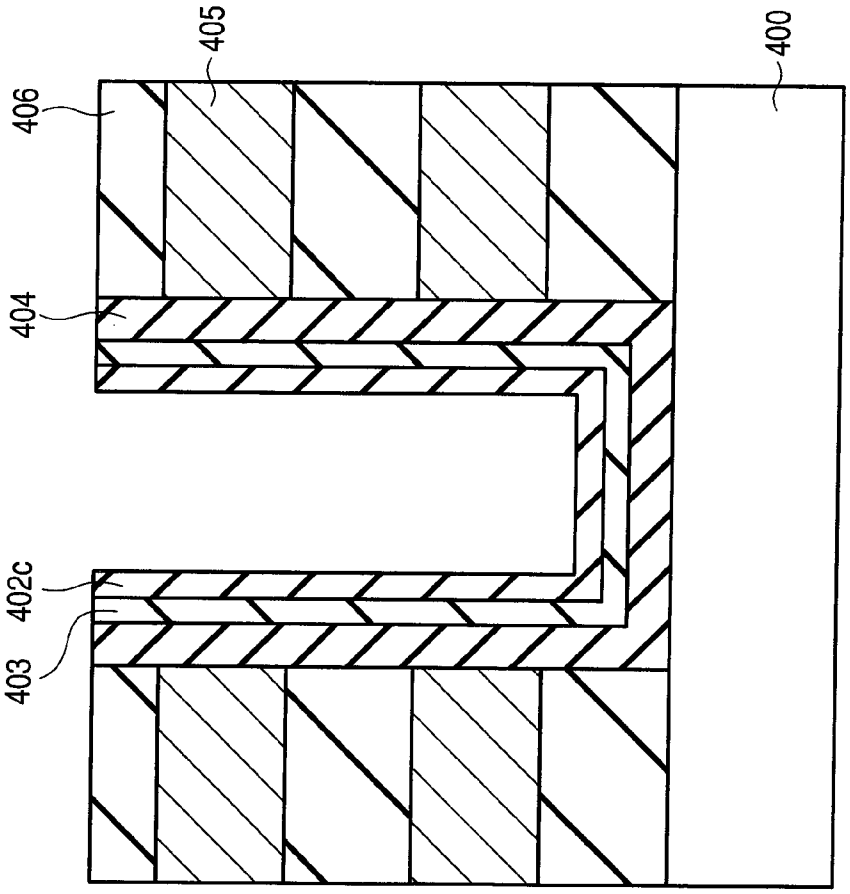

FIG. 49A

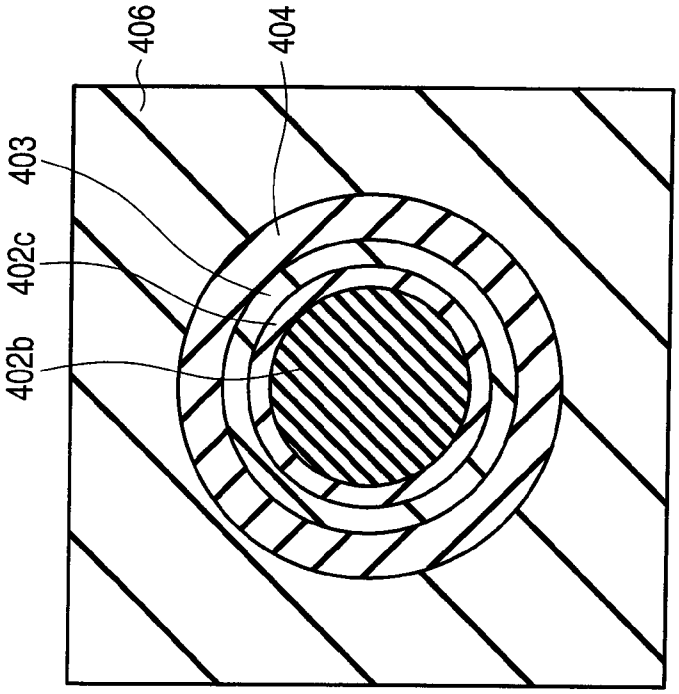

FIG. 50B

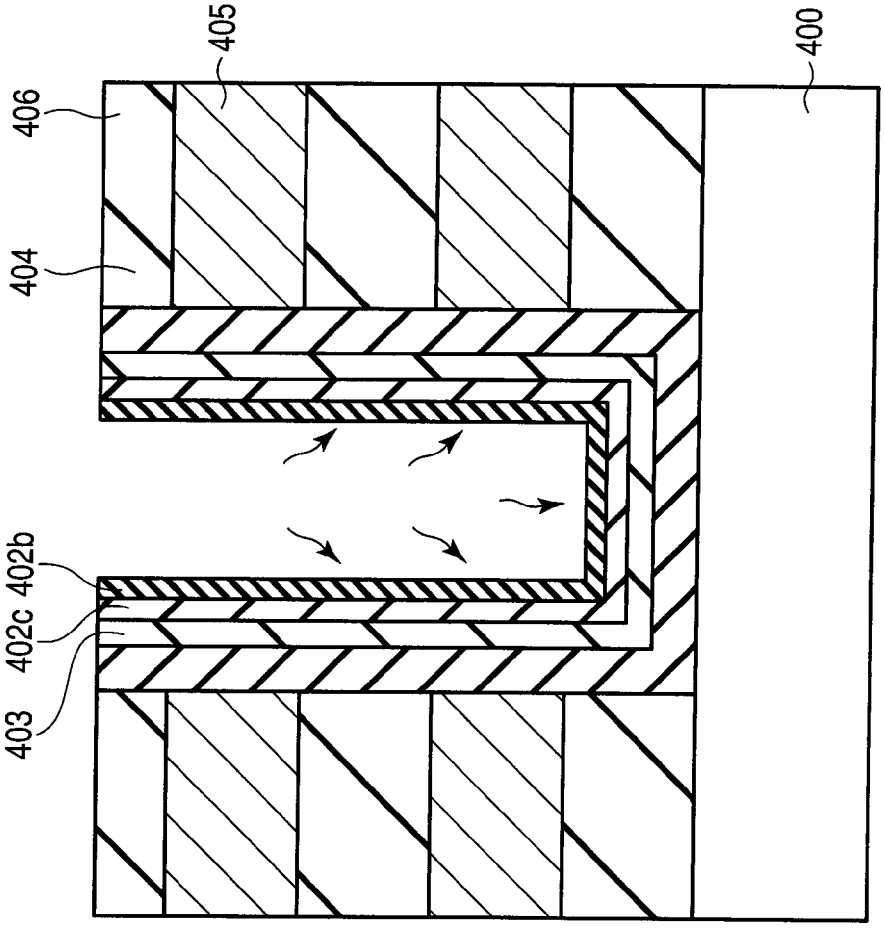

FIG. 50A

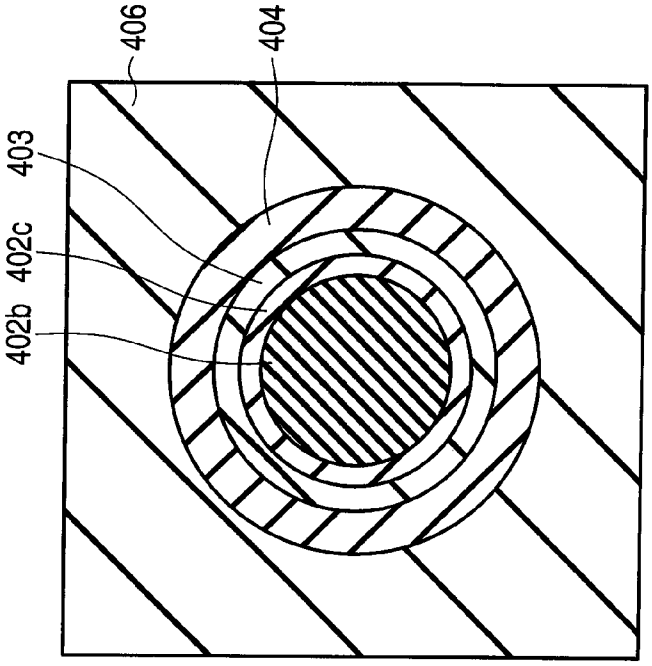

FIG. 51B

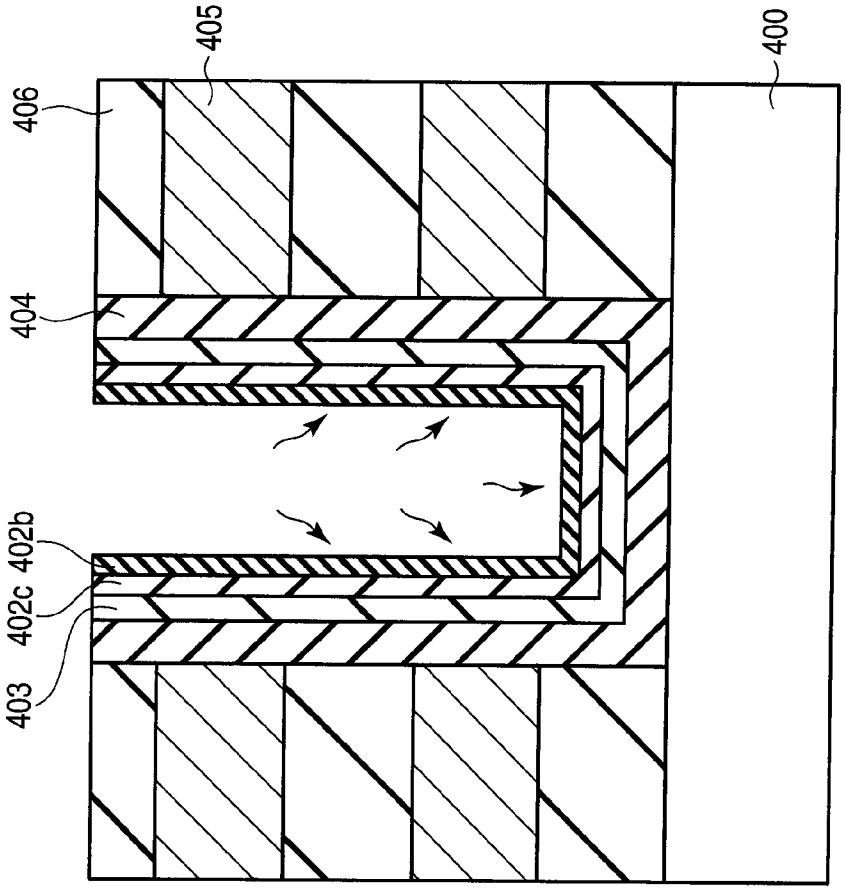

FIG. 51A

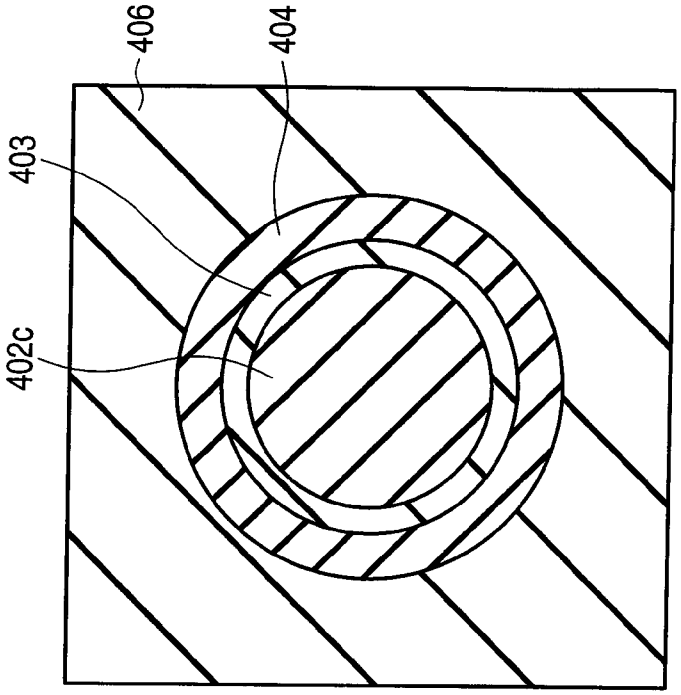

FIG. 52B

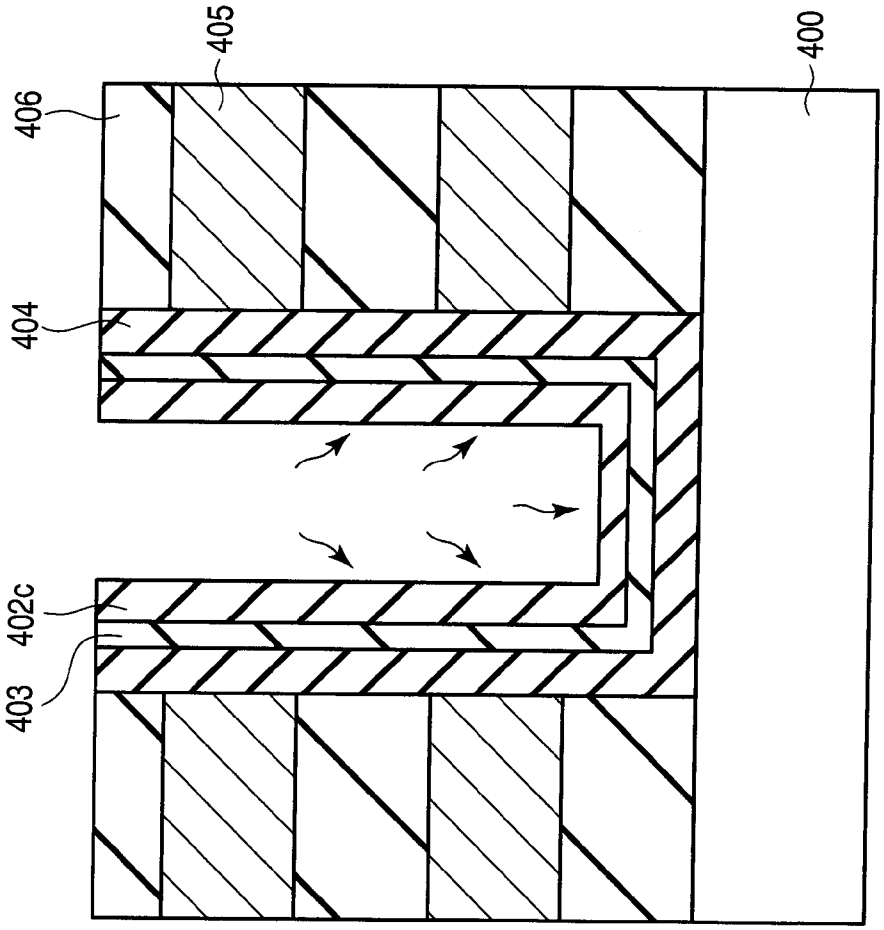

FIG. 52A

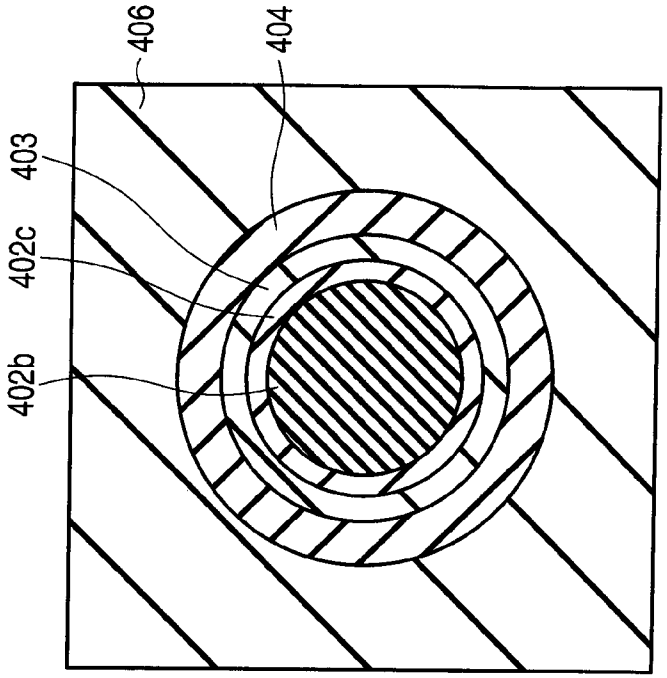

FIG. 53B

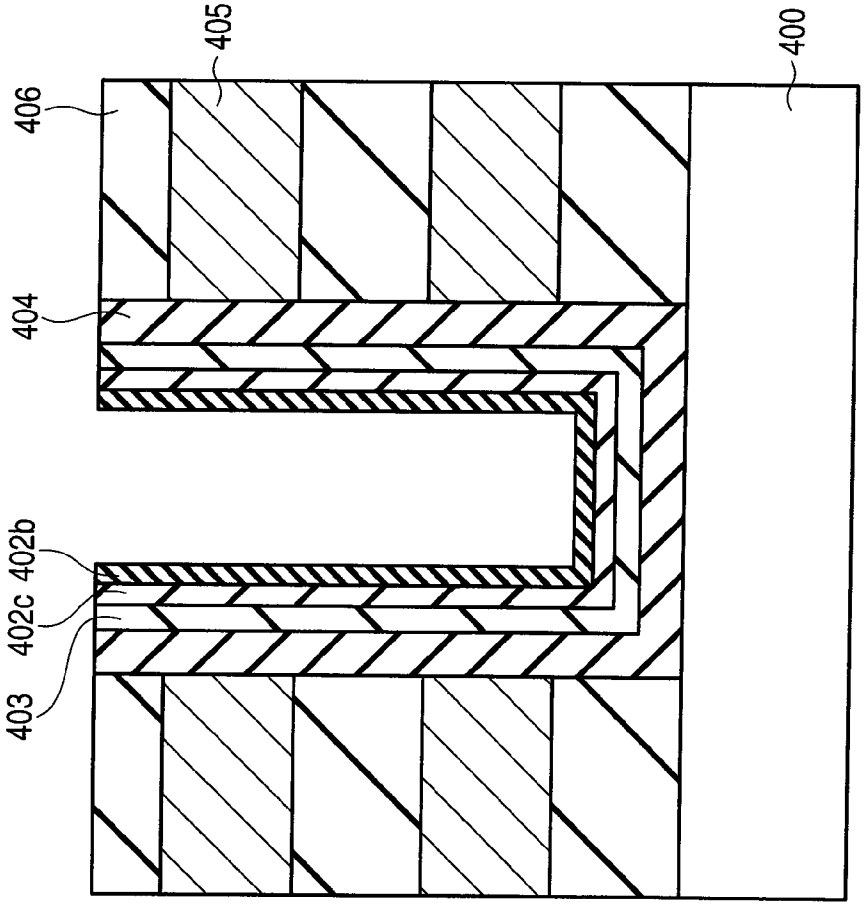

FIG. 53A

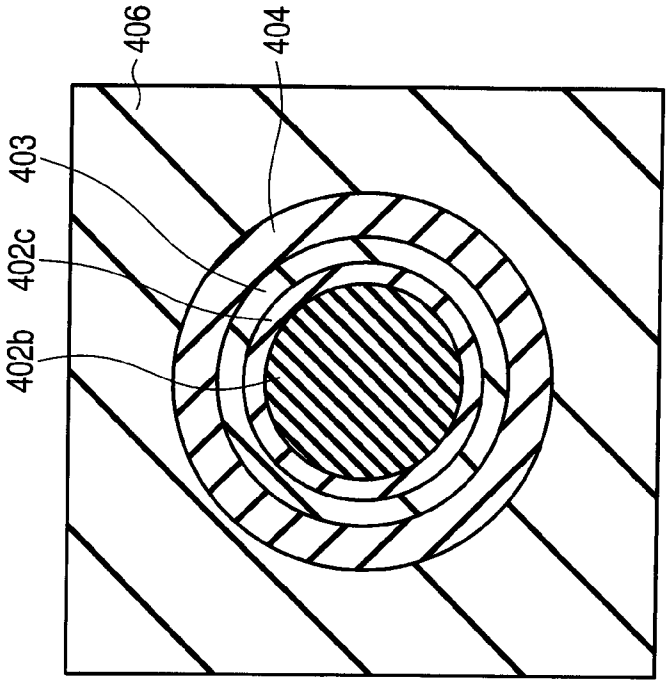

FIG. 54B

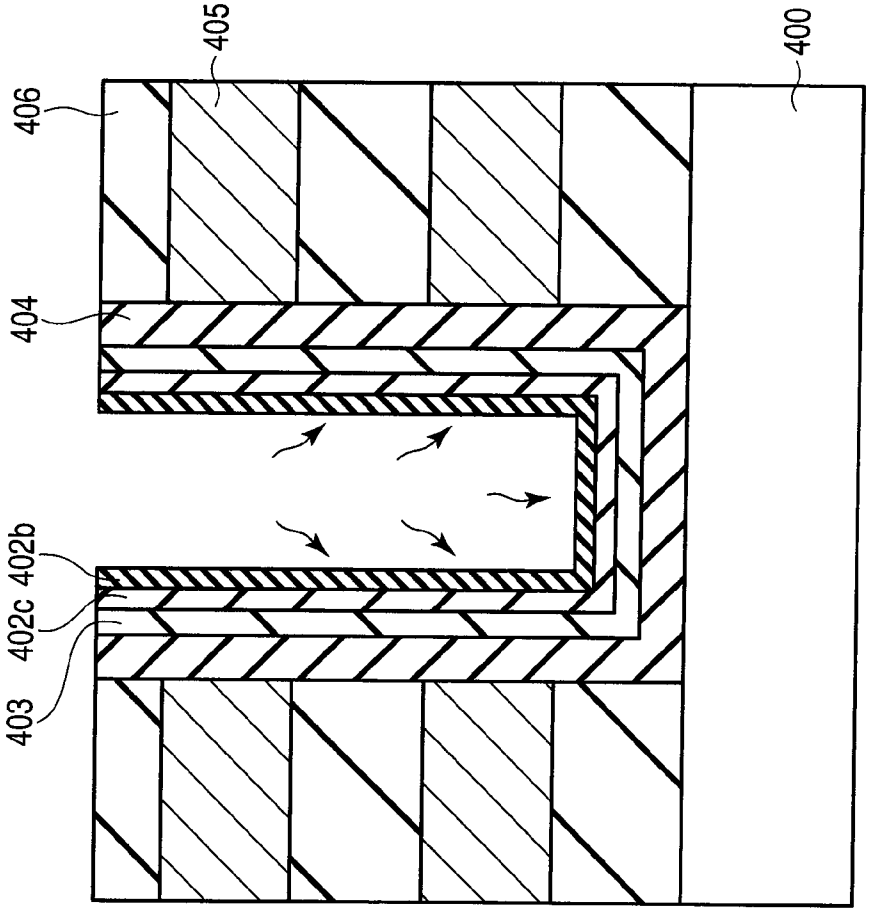

FIG. 54A

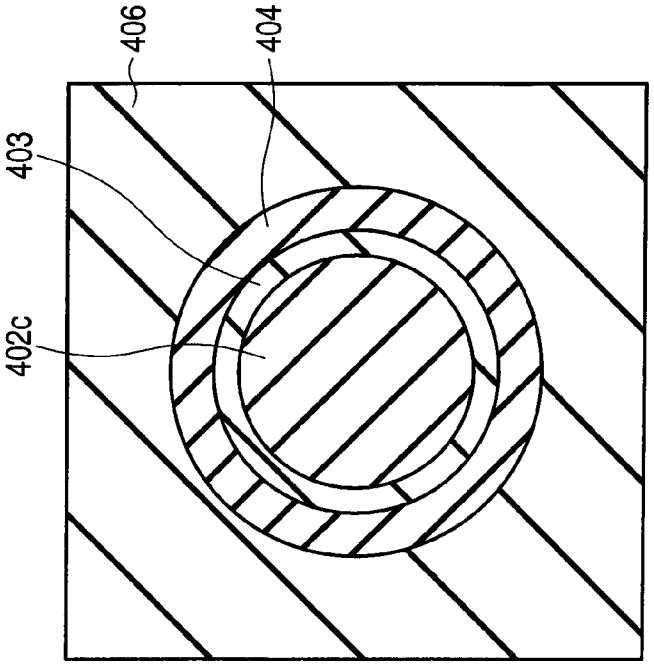

FIG. 55B

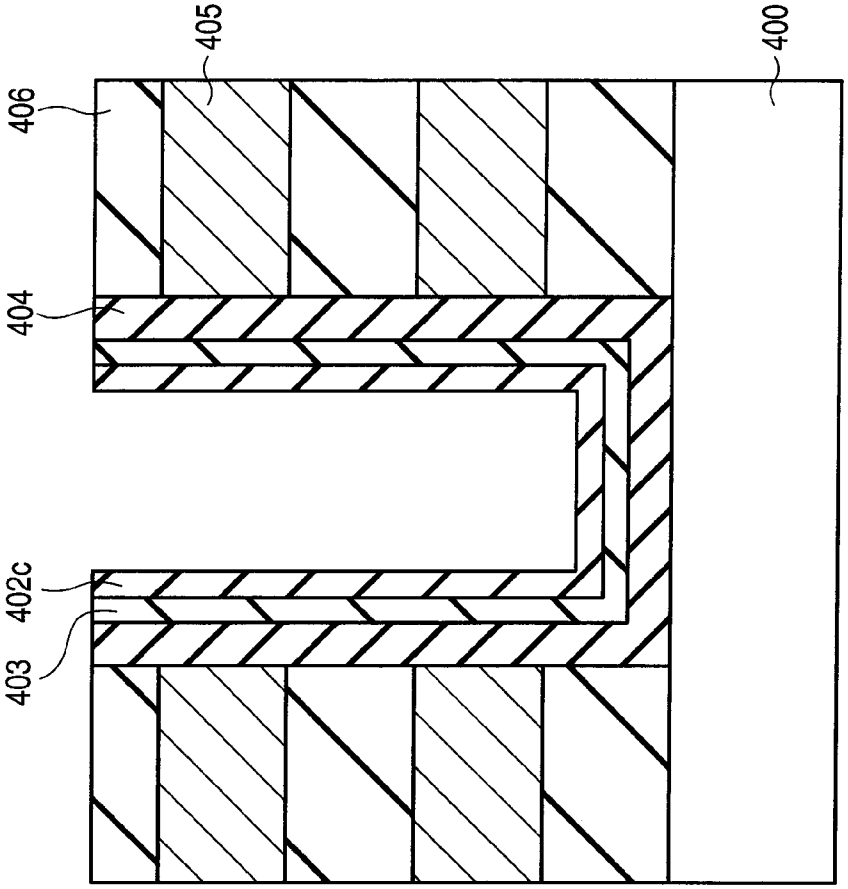

FIG. 55A

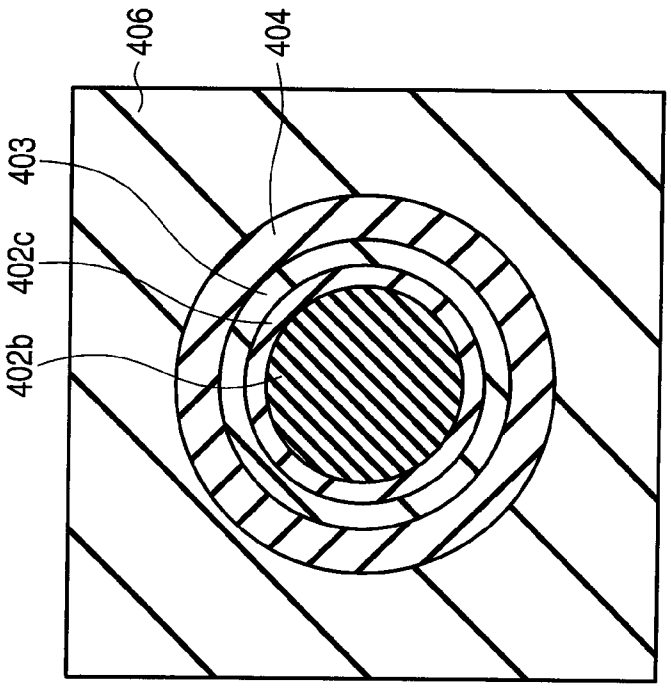

FIG. 56B

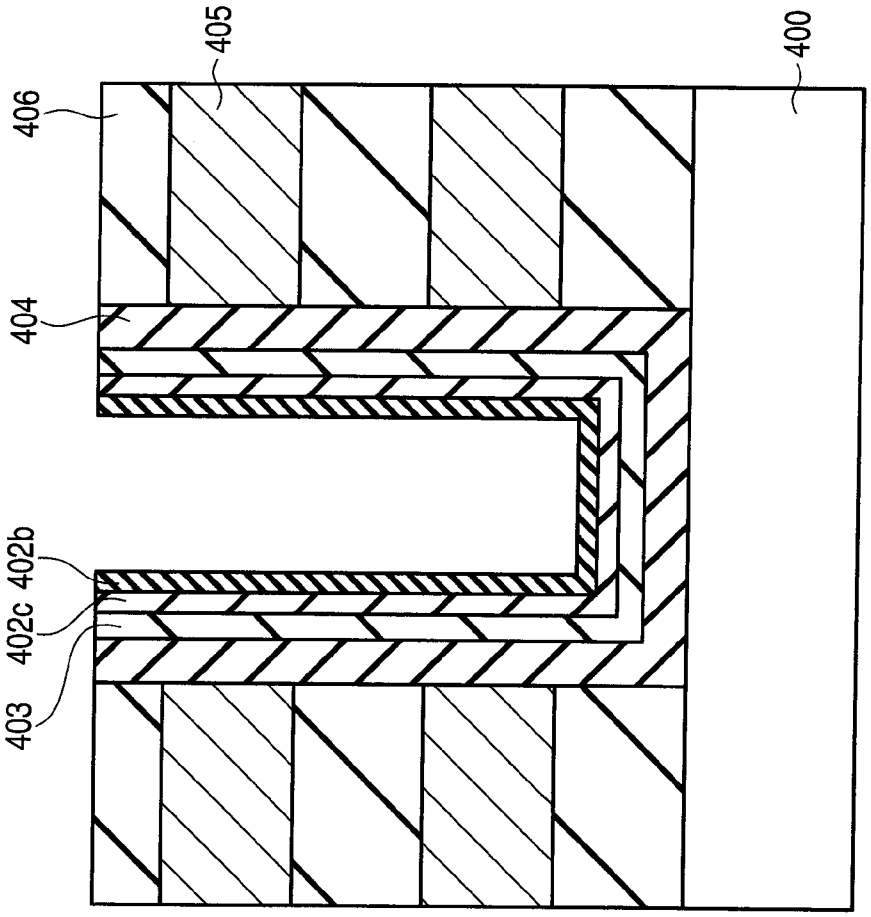

FIG. 56A

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from prior Japanese Patent Application No. 2008-193922, filed Jul. 28, 2008, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor device and a method for manufacturing the semiconductor device.

[0004] 2. Description of the Related Art

[0005] Nonvolatile semiconductor memory devices using, as a charge-storage layer, a charge-storage insulating film in which charges can be trapped have been proposed (see, for example, Jpn. Pat. Appln. KOKAI Publication No. 2004-158810). The charge-trap nonvolatile semiconductor memory device traps charges injected into the charge-storage insulating film through a tunnel insulating film, in a trap state in the charge-storage insulating film. The charges are thus stored in the charge-storage insulating film. Known typical charge-trap nonvolatile semiconductor memory devices are of a MONOS or SONOS type.

[0006] To neutralize charges in the charge-trap nonvolatile semiconductor memory device, the erase characteristics need to be improved by effectively injecting holes into the charge-storage insulating film. Thus, a structure has been proposed which uses a stacked film of a silicon oxide film, a silicon nitride film, and a silicon oxide film as a tunnel insulating film (see, for example, Jpn. Pat. Appln. KOKAI Publication No. 2006-216215). However, the resulting tunnel insulating film may not be optimum.

BRIEF SUMMARY OF THE INVENTION

[0007] According to a first aspect of the present invention, there is provided a semiconductor device comprising: a semiconductor region; a tunnel insulating film formed on a surface of the semiconductor region; a charge-storage insulating film formed on a surface of the tunnel insulating film and containing silicon and nitrogen; a block insulating film formed on a surface of the charge-storage insulating film; and a control gate electrode formed on a surface of the block insulating film, wherein the tunnel insulating film has a first insulating film formed on the surface of the semiconductor region and containing silicon and oxygen, a second insulating film formed on a surface of the first insulating film, and a third insulating film formed on a surface of the second insulating film and containing silicon and oxygen, and a charge trap state in the second insulating film has a lower density than that in the charge-storage insulating film.

[0008] According to a second aspect of the present invention, there is provided a method for manufacturing a semiconductor device a tunnel insulating film formed on a surface of a semiconductor region, a charge-storage insulating film formed on a surface of the tunnel insulating film and containing silicon and nitrogen, a block insulating film formed on a surface of the charge-storage insulating film, and a control gate electrode formed on a surface of the block insulating film, wherein a process of manufacturing the tunnel insulating film comprises: forming a first insulating film containing silicon and oxygen on the surface of the semiconductor region; introducing nitrogen into an upper portion of the first insulating film to form a second insulating film containing silicon, nitrogen, and oxygen; and forming a third insulating film containing silicon and oxygen on a surface of the second insulating film.

[0009] According to a third aspect of the present invention, there is provided a method for manufacturing a semiconductor device comprising a tunnel insulating film formed on a surface of a semiconductor region, a charge-storage insulating film formed on a surface of the tunnel insulating film and containing silicon and nitrogen, a block insulating film formed on a surface of the charge-storage insulating film, and a control gate electrode formed on a surface of the block insulating film, the tunnel insulating film including a first insulating film formed on a surface of the semiconductor region and containing silicon and oxygen, a second insulating film formed on a surface of the first insulating film and containing silicon and nitrogen, and a third insulating film formed on a surface of the second insulating film and containing silicon and oxygen, wherein forming the second insulating film, the second insulating film is formed at a lower temperature than the charge-storage insulating film.

[0010] According to a fourth aspect of the present invention, there is provided a method for manufacturing a semiconductor device comprising a tunnel insulating film formed on a surface of a semiconductor region, a charge-storage insulating film formed on a surface of the tunnel insulating film and containing silicon and nitrogen, a block insulating film formed on a surface of the charge-storage insulating film, and a control gate electrode formed on a surface of the block insulating film, wherein a process of forming the tunnel insulating film comprises forming a third insulating film containing silicon and oxygen on an exposed surface of the charge-storage insulating film, introducing nitrogen into an exposed surface side region of the third insulating film to form a second insulating film containing silicon, nitrogen, and oxygen, and forming a first insulating film containing silicon and oxygen on an exposed surface of the second insulating film.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

[0011] FIG. **1** is a sectional view schematically showing the configuration of a semiconductor device according to a first embodiment of the present invention;

[0012] FIGS. **2**A to **2**E are diagrams showing the distribution of the concentration of oxygen in a tunnel insulating film and a charge-storage insulating film in a semiconductor device according to a first embodiment of the present invention;

[0013] FIG. **3** is a sectional view schematically showing a part of a process of manufacturing a semiconductor device according to the first embodiment of the present invention;

[0014] FIG. **4** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the first embodiment of the present invention;

[0015] FIG. **5** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the first embodiment of the present invention;

[0016] FIG. **6** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the first embodiment of the present invention;

[0017] FIG. **7** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the first embodiment of the present invention;

[0018] FIG. **8** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the first embodiment of the present invention;

[0019] FIG. **9** is a sectional view schematically showing a part of a process of manufacturing a semiconductor device according to a modification of the first embodiment of the present invention;

[0020] FIG. **10** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the first embodiment of the present invention;

[0021] FIG. **11** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the first embodiment of the present invention;

[0022] FIG. **12** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the first embodiment of the present invention;

[0023] FIG. **13** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the first embodiment of the present invention;

[0024] FIG. **14** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the first embodiment of the present invention;

[0025] FIG. **15** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the first embodiment of the present invention;

[0026] FIG. **16** is a sectional view schematically showing the configuration of a semiconductor device according to a second embodiment of the present invention;

[0027] FIGS. **17**A to **17**D are diagrams showing the distribution of the concentration of a predetermined element in a tunnel insulating film and a charge-storage insulating film in the semiconductor device according to the first embodiment of the present invention;

[0028] FIG. **18** is a sectional view schematically showing a part of a process of manufacturing a semiconductor device according to the second embodiment of the present invention;

[0029] FIG. **19** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the second embodiment of the present invention;

[0030] FIG. **20** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the second embodiment of the present invention;

[0031] FIG. **21** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the second embodiment of the present invention;

[0032] FIG. **22** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the second embodiment of the present invention;

[0033] FIG. **23** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the second embodiment of the present invention;

[0034] FIG. **24** is a sectional view schematically showing a part of a process of manufacturing a semiconductor device according to a modification of the second embodiment of the present invention;

[0035] FIG. **25** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the second embodiment of the present invention;

[0036] FIG. **26** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the second embodiment of the present invention;

[0037] FIG. **27** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the second embodiment of the present invention;

[0038] FIG. **28** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the second embodiment of the present invention;

[0039] FIG. **29** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the second embodiment of the present invention;

[0040] FIG. **30** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the modification of the second embodiment of the present invention;

[0041] FIG. **31** is a sectional view schematically showing the configuration of a semiconductor device according to a third embodiment of the present invention;

[0042] FIG. **32** is a sectional view schematically showing a part of a process of manufacturing a semiconductor device according to the third embodiment of the present invention;

[0043] FIG. **33** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the third embodiment of the present invention;

[0044] FIG. **34** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the third embodiment of the present invention;

[0045] FIG. **35** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the third embodiment of the present invention;

[0046] FIG. **36** is a sectional view schematically showing a part of the process of manufacturing the semiconductor device according to the third embodiment of the present invention;

[0047] FIGS. **37**A and **37**B are diagrams schematically showing the configuration of a semiconductor device according to a fourth embodiment of the present invention;

[0048] FIGS. **38**A and **38**B are diagrams schematically showing a part of a process of manufacturing a semiconductor device according to the fourth embodiment of the present invention;

[0049] FIGS. **39**A and **39**B are diagrams schematically showing a part of the process of manufacturing the semiconductor device according to the fourth embodiment of the present invention;

[0050] FIGS. **40**A and **40**B are diagrams schematically showing a part of the process of manufacturing the semiconductor device according to the fourth embodiment of the present invention;

[0051] FIGS. **41**A and **41**B are diagrams schematically showing a part of the process of manufacturing the semiconductor device according to the fourth embodiment of the present invention;

[0052] FIGS. **42**A to **42**E are diagrams showing the distribution of oxygen concentration in a tunnel insulating film **402** and a charge-storage insulating film **403**;

[0053] FIGS. **43**A and **43**B are diagrams schematically showing a part of a process of manufacturing a tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention;

[0054] FIGS. **44**A and **44**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention;

[0055] FIGS. **45**A and **45**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention;

[0056] FIGS. **46**A and **46**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention;

[0057] FIGS. **47**A and **47**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention;

[0058] FIGS. **48**A to **48**D are diagrams showing the distribution of the concentration of a predetermined element (deuterium, hydrogen, fluorine, or chlorine) in a tunnel insulating film **402** and a charge-storage insulating film **403**;

[0059] FIGS. **49**A and **49**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention;

[0060] FIGS. **50**A and **50**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention;

[0061] FIGS. **51**A and **51**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention;

[0062] FIGS. **52**A and **52**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention;

[0063] FIGS. **53**A and **53**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention;

[0064] FIGS. **54**A and **54**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention;

[0065] FIGS. **55**A and **55**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention; and

[0066] FIGS. **56**A and **56**B are diagrams schematically showing a part of the process of manufacturing the tunnel insulating film in the semiconductor device according to the fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0067] Embodiments of the present invention will be described below with reference to the drawings.

First Embodiment

[0068] FIG. **1** is a sectional view schematically showing the basic structure of a semiconductor device according to the present invention; the sectional view is taken along a bit line direction (channel length direction).

[0069] First, the configuration of the present embodiment will be described with reference to FIG. **1**.

[0070] As shown in FIG. **1**, an element region with a source/drain region **102** is formed in a semiconductor substrate (silicon substrate) **101**. A tunnel insulating film **103** is formed on the element region. A charge-storage insulating film **104** is formed on the tunnel insulating film **103**. A block insulating film **105** is formed on the charge-storage insulating film **104**. A control gate electrode **106** is formed on the block insulating film **105**.

[0071] The tunnel insulating film **103** has a lower insulating film **103***a* containing silicon and oxygen, an intermediate insulating film **103***b* formed on the lower insulating film **103***a* and containing silicon, nitrogen, and oxygen, and an upper insulating film **103***c* formed on the intermediate insulating film **103***b* and containing silicon and oxygen. Specifically, the tunnel insulating film **103** has the lower insulating film **103***a* formed of a silicon oxide film and having a thickness of about 1 to 2 nm, the intermediate insulating film **103***b* formed of a silicon nitride film (for example, silicon oxynitride film) containing oxygen and having a thickness of about 1 to 3 nm, and the upper insulating film **103***c* formed of a silicon oxide film and having a thickness of about 1 to 4 nm.

[0072] The charge-storage insulating film **104** is formed of a silicon nitride film of thickness about 2 to 5 nm. The block insulating film **105** is formed of a silicon oxide film or a high-dielectric-constant insulating film of thickness about 10 to 25 nm. The high-dielectric-constant insulating film is, for example, alumina (Al_2O_3), which exhibits a large band gap. The control gate electrode **106** is formed of polysilicon or a metal material. The metal material is desirably metal with a high work function.

[0073] In the present embodiment, the intermediate insulating film **103***b*, a part of the tunnel insulating film **103**, has a higher oxygen concentration than the charge-storage insulating film **104**.

[0074] FIGS. **2**A to **2**E are diagrams of the concentration of oxygen in the tunnel insulating film **103** and the charge-storage insulating film **104**. As shown in FIGS. **2**A to **2**E, regardless of the form of the graph of the oxygen concentration, the effects of the present embodiment are exerted pro-

vided that the oxygen in the intermediate insulating film **103***b* has a higher average concentration than that in the charge-storage insulating film **104**.

[0075] According to the above-described embodiment, the intermediate insulating film **103***b*, a part of the tunnel insulating film **103**, contains a larger amount of oxygen than the charge-storage insulating film **104**. A large amount of oxygen thus contained in the silicon nitride film in the tunnel insulating film **103** reduces the charge trap state in the silicon nitride film. The charge-storage insulating film **104** contains almost no oxygen and thus provides a sufficient charge trap state. The charge-storage insulating film **104** can thus reliably store charges. Thus, the present embodiment can provide a non-volatile semiconductor memory device with an excellent write/erase property, an excellent charge retention property, and high reliability.

[0076] FIGS. **3** to **8** are sectional views schematically showing the basic structure of the semiconductor device according to the present invention; the sectional views are taken along the bit line direction.

[0077] First, as shown in FIG. **3**, the semiconductor substrate **101** is cleaned.

[0078] Then, as shown in FIG. **4**, the surface of the semiconductor substrate **101** is oxidized by a thermal oxidation method at 800 to 1,000° C. to form a silicon oxide film having a thickness of about 1.0 to 2.5 nm and serving as a lower insulating film **103***a*. Forming the lower insulating film **103***a* at the high temperature enables the reaction between the semiconductor substrate **101** and nitrogen to be inhibited when a silicon nitride film is formed during a subsequent step. Furthermore, after the formation of the lower insulating film **103***a*, heat treatment is carried out in an NO atmosphere at 800 to 900° C. to introduce nitrogen into the interface between the semiconductor substrate **101** and the lower insulating film **103***a*. This allows the stress resistance of the tunnel insulating film **103** to be improved. The above-described heat treatment enables the reaction between the semiconductor substrate **101** and both nitriding agent and oxidizer to be inhibited. This is advantageous for a reduction in the thickness of the tunnel insulating film **103**.

[0079] To form the lower insulating film **103***a* on the semiconductor substrate **101** by deposition, a silicon oxide film is deposited at 700 to 800° C. by the low-pressure chemical vapor deposition (LPCVD) method. In this case, a dense silicon oxide film is formed, thus inhibiting the semiconductor substrate **101** and the nitriding agent. As a precursor, for example, SiH_2Cl_2 (dichlorosilane [DCS]) and N_2O or Si_2H_6 (disilane [DS]) and N_2O are used. Using N_2O as a precursor allows nitrogen to be introduced into the interface between the semiconductor substrate **101** and the lower insulating film **103***a*. This enables the stress resistance to be improved and allows the reaction between the semiconductor substrate **101** and both nitriding agent and oxidizer to be inhibited. If the lower insulating film **103***a* is formed at low temperature, the reaction of the semiconductor substrate **101** can be inhibited by densifying the silicon oxide film by heat treatment at 900 to 1,000° C.

[0080] Thereafter, a silicon nitride film having a thickness of 1.0 to 3.0 nm and serving as the intermediate insulating film **103***b* is formed on the lower insulating film **103***a* at a temperature of at most 450° C. Forming the silicon nitride film at the low temperature of at most 450° C. allows an appropriately flat silicon nitride film to be deposited on the lower insulating film **103***a*.

[0081] The atomic layer deposition (ALD) method is preferably used as a method of forming a silicon nitride film at the low temperature of at most 450° C. For example, DCS and ammonia may be used as a precursor. Nitrogen radicals may also be used as a nitriding agent.

[0082] Moreover, forming the silicon nitride film at a temperature of at most 450° C. allows formation of a silicon nitride film into which oxygen can be easily introduced. Thus, a high concentration of oxygen can be introduced into the silicon nitride film.

[0083] Then, as shown in FIG. **5**, the silicon nitride film formed at the low temperature is exposed to an oxidizing atmosphere at 400 to 900° C. to introduce oxygen into the silicon nitride film. The introduction of oxygen into the silicon nitride film enables the charge trap state in the silicon nitride film to be significantly reduced. In particular, heat treatment in an atmosphere at 400 to 700° C. containing steam enables the charge trap state to be more significantly reduced. In this manner, the intermediate insulating film **103***b* is formed.

[0084] Then, as shown in FIG. **6**, after the formation of the intermediate insulating film **103***b*, a silicon oxide film having a thickness of about 1.0 to 3.0 nm and serving as the upper insulating film **103***c* is deposited at 450 to 600° C. using the ALD method. The ALD method at the low temperature allows a flat, thin silicon oxide film to be formed on the intermediate insulating film **103***b* with elements prevented from being relocated. Furthermore, a silicon oxide film of high quality with a possible leakage current reduced is obtained. For example, DCS and O_3 are preferably used as a precursor. By introducing oxygen after the formation of the upper insulating film **103***c*, the charge trap state in the intermediate insulating film **103***b* can be reduced, and the charge trap state at the interface between the intermediate insulating film **103***b* and the upper insulating film **103***c* can also be reduced. If oxygen is introduced after the formation of the upper insulating film **103***c*, the oxygen introduction is preferably carried out in a temporarily diluted oxidizing atmosphere at 600 to 900° C. at which the elements are prevented from being relocated.

[0085] Then, as shown in FIG. **7**, a silicon nitride film serving as the charge-storage insulating film **104** is deposited on the upper insulating film **103***c* using the LPCVD method at 600° C. or higher. Forming the charge-storage insulating film **104** at high temperature allows oxidation resistance to be improved.

[0086] Excellent oxidation resistance is offered by the charge-storage insulating film **104** is formed using the ALD method at a temperature of at least 550° C. If the charge-storage insulating film **104** is formed at a temperature of at most 550° C., heat treatment in an inert gas atmosphere at 700 to 1,000° C. densities the silicon nitride film to improve the oxidation resistance. This exerts effects similar to those exerted by the formation of a silicon nitride film by the LPCVD method.

[0087] An alumina film having a thickness of about 10 to 20 nm and serving as the block insulating film **105** is formed on the charge-storage insulating film **104** by the ALD or metal organic chemical vapor deposition (MOCVD) method. When the ALD or MOCVD method is used, for example, trimethyl aluminum (TMA) and H_2O or O_3 are used as a precursor. Moreover, polysilicon having a thickness of about 150 to 200 nm and serving as a control gate electrode film **106** is deposited by the LPCVD method. For the control gate electrode

film **106**, a metal material with a work function may be formed by the sputtering or ALD method.

[0088] Forming the charge-storage insulating film **104** at high temperature inhibits reducing of the charge trap state in the charge-storage insulating film **104** caused by the oxidizer during the formation of the block insulating layer **105**, the oxidizer during the formation of an interlayer insulating film, or the like.

[0089] Then, as shown in FIG. **8**, the above-described films are processed to form the control gate electrode **106**.

[0090] Thereafter, impurity elements such as arsenic are ion-injected into a surface region on the semiconductor substrate **101**, which is then heat treated. Thus, a source/drain region **102** is formed as shown in FIG. **1**.

[0091] Thereafter, well-known steps, that is, a step of forming an interlayer insulating film (not shown in the drawings) and a step of forming wiring (not shown in the drawings) and the like, are carried out to obtain a nonvolatile semiconductor memory device.

[0092] According to the above-described embodiment, the intermediate insulating film **103***b* is formed by introducing oxygen into the silicon nitride film provided on the lower insulating film **103***a*. Thus, the introduction of oxygen into the silicon nitride film enables the charge trap state in the silicon nitride film to be significantly reduced. Consequently, a tunnel insulating film of high quality is obtained.

[0093] In the above-described embodiment, the silicon nitride film is formed on the lower insulating film **103***a* at the low temperature. Thus, a high concentration of oxygen can be easily introduced into the silicon nitride film. Moreover, an appropriately flat silicon nitride film can be formed on the lower insulating film **103***a*. As a result, a possible low-field leakage current through a local leakage path can be inhibited, thus improving the charge retention property. This also inhibits generation of the charge trap state caused by penetration of the nitriding agent to the interface between the semiconductor substrate **101** and the lower insulating film **103***a*. Thus, a possible trap assist tunnel current can be inhibited, enabling a reduction in the field leakage current from the tunnel insulating film **103**. As a result, the read disturb property of the memory cell transistor can be drastically improved.

[0094] Furthermore, according to the above-described embodiment, the charge-storage insulating film **104** is formed by depositing a silicon nitride film on the upper insulating film **103***c* at the high temperature. The formation at the high temperature allows a silicon nitride film with high oxidation resistance to be formed. Thus, a sufficient trap state can be ensured.

[0095] In the above-described embodiment, the intermediate insulating film **103***b* is formed by depositing a silicon nitride film on the lower insulating film **103***a* and then oxidizing the silicon oxide film. However, the intermediate insulating film **103***b* may be a silicon oxynitride film directly formed by the ALD method at low temperature. In this case, no oxidizer needs to be subsequently supplied, enabling a reduction in the number of steps required. To form the silicon oxynitride film by the ALD method, for example, DCS, a radicalized nitriding agent, and a radicalized oxidizer may be sequentially supplied. The ratio of nitrogen and oxygen in the silicon oxynitride film can be controlled by controlling the ratio of the amount of oxidizer supplied to the amount of nitriding agent supplied.

(Modification)

[0096] FIGS. **9** to **15** are sectional views schematically showing a basic method for manufacturing a semiconductor device according to a modification of the first embodiment; the sectional views are taken along the bit line direction. The basic structure and the basic manufacturing method are similar to those in the above-described embodiment. Thus, the matters described above in the embodiment and matters easily conceivable from the embodiment will not be described below.

[0097] First, as shown in FIG. **9**, the semiconductor substrate **101** is cleaned.

[0098] Then, as shown in FIG. **10**, the surface of the semiconductor substrate **101** is oxidized by the thermal oxidation method at 800 to 1,000° C. to form a silicon oxide film having a thickness of about 2.0 to 4.0 nm and serving as a lower insulating film **103***a*. Forming the lower insulating film **103***a* at the high temperature enables the reaction between the semiconductor substrate **101** and nitrogen to be inhibited when a silicon nitride film is formed during a subsequent step. Furthermore, after the formation of the lower insulating film **103***a*, heat treatment is carried out in an NO atmosphere at 800 to 900° C. to introduce nitrogen into the interface between the semiconductor substrate **101** and the lower insulating film **103***a*. This allows the stress resistance of the tunnel insulating film **103** to be improved.

[0099] Then, as shown in FIG. **11**, nitrogen is introduced into an upper portion of the silicon oxide film **103***a* by a plasma or radical nitriding method to form a silicon oxynitride film having a thickness of about 1.0 to 3.0 nm and serving as an intermediate insulating film **103***b*. As a result, the upper portion of the silicon oxide film **103***a* is reformed into a silicon oxynitride film containing a large amount of oxygen and in which a reduced number of charges are trapped. In this case, the thickness of the silicon oxide film **103***a* is reduced to about 1.0 to 2.0 nm. In the plasma or radical nitriding method, the surface of the silicon oxide film **103***a* may be exposed, at the room temperature to 500° C., to an atmosphere containing ions or radicals serving as a nitriding agent. Furthermore, to reduce damage that may occur while the surface of the silicon oxide film **103***a* is being reformed, inductively coupled plasma (ICP) or microwave excitation plasma is preferably used. After the reformation, heat treatment is carried out at 900 to 1,050° C. This preferably enables recovery from damage that may occur during the introduction of nitrogen, increasing the lifetime of the tunnel insulating film **103**. The atmosphere for the heat treatment preferably contains a small amount of oxygen to the degree that the thickness of the films is prevented from being increased by the oxidation of the semiconductor substrate **101**. This is because the small amount of oxygen serves to enhance the reforming effect.

[0100] As shown in FIG. **12**, the intermediate insulating film **103***b* may be heat treated in an atmosphere at 400 to 700° C. containing steam to introduce oxygen into the intermediate insulating film **103***b*.

[0101] Then, as shown in FIG. **13**, after the intermediate insulating film **103***b* is reformed and heat treated, a silicon oxide film having a thickness of about 1.0 to 3.0 nm and serving as an upper insulating film **103***c* is deposited using the ALD method at 450 to 600° C. After the formation of the upper insulating film **103***c*, oxygen may be introduced into the intermediate insulating film **103***b* via the upper insulating film **103***c* in a diluted oxidizing atmosphere at 600 to 900° C. at which the elements are prevented from being relocated.

[0102] Then, as shown in FIG. **14**, as is the case with the first embodiment, a silicon nitride film serving as a charge-

storage insulating film **104** is deposited on the upper insulating film **103***c* using the LPCVD method at 600° C. or higher. In the present embodiment, such an oxygen concentration distribution as shown in FIG. **2**E is obtained.

[0103] Then, as is the case with the first embodiment, an alumina film having a thickness of about 10 to 20 nm and serving as a block insulating film **105** is formed on the charge-storage insulating film **104** using the ALD or MOCVD method. Moreover, polysilicon having a thickness of about 150 to 200 nm and serving as a control gate electrode film **106** is deposited by the LPCVD method.

[0104] Then, as shown in FIG. **15**, the control gate electrode **106** is formed by a lithography process as is the case with the first embodiment.

[0105] Thereafter, impurity elements such as arsenic are ion-injected into a surface region on the semiconductor substrate **101**, which is then heat treated. Thus, a source/drain region **102** is formed as shown in FIG. **1**.

[0106] Thereafter, well-known steps, that is, a step of forming an interlayer insulating film (not shown in the drawings) and a step of forming wiring (not shown in the drawings) and the like, are carried out to obtain a nonvolatile semiconductor memory device.

[0107] The above-described modification exerts effects similar to those of the first embodiment. Furthermore, according to the above-described modification, the intermediate insulating film **103***b* is formed by nitriding the upper portion of the lower insulating film **103***a* by plasma or radical nitriding. Thus, the concentration of nitrogen in the intermediate insulating film **103***b* can be varied in stages from the surface to the interior of the film. This prevents a definite interface from being formed between the lower insulating film **103***a* and the intermediate insulating film **103***b*. Consequently, the charge trap state is reduced which is formed at the interface between the lower insulating film **103***a* and the intermediate insulating film **103***b*. Therefore, the charge retention property can be improved.

Second Embodiment

[0108] FIG. **16** is a sectional view schematically showing the basic structure of a semiconductor device according to the present invention; the sectional view is taken along the bit line direction.

[0109] First, the configuration of the present embodiment will be described with reference to FIG. **16**. The basic structure and the basic manufacturing method are similar to those in the first embodiment. Thus, the matters described in the first embodiment and matters easily conceivable from the first embodiment will not be described below.

[0110] As shown in FIG. **16**, an element region with a source/drain region **202** is formed in a semiconductor substrate **201**. A tunnel insulating film **203** is formed on the element region. A charge-storage insulating film **204** is formed on the tunnel insulating film **203**. A block insulating film **205** is formed on the charge-storage insulating film **204**. A control gate electrode **206** is formed on the block insulating film **205**.

[0111] The tunnel insulating film **203** has a lower insulating film **203***a* containing silicon and oxygen, an intermediate insulating film **203***b* formed on the lower insulating film **203***a* and containing silicon, nitrogen, and a predetermined element selected from hydrogen, deuterium, and halogen, and an upper insulating film **203***c* formed on the intermediate insulating film **203***b* and containing silicon and oxygen. Specifically, the tunnel insulating film **203** has the lower insulating film **203***a* formed of a silicon oxide film and having a thickness of about 1 to 2 nm, the intermediate insulating film **203***b* having a thickness of about 1 to 3 nm and formed of a silicon nitride film containing at least element selected from deuterium, hydrogen, fluorine, and chlorine, and the upper insulating film **203***c* formed of a silicon oxide film and having a thickness of about 1 to 4 nm.

[0112] The charge-storage insulating film **204** is formed of a silicon nitride film of thickness about 2 to 5 nm. The block insulating film **205** is formed of a silicon oxide film or a high-dielectric-constant insulating film of thickness about 10 to 25 nm. The high-dielectric -constant insulating film is, for example, alumina, which exhibits a large band gap. The control gate electrode **206** is formed of polysilicon or a metal material. The metal material is desirably metal with a high work function.

[0113] In the present embodiment, the predetermined element (deuterium, hydrogen, fluorine, or chlorine) in the intermediate insulating film **203***b*, a part of the tunnel insulating film **203**, has a higher concentration than that in the charge-storage insulating film **204**.

[0114] FIGS. **17**A to **17**D are diagrams showing the distribution of the concentration of the predetermined element (deuterium, hydrogen, fluorine, or chlorine) in the tunnel insulating film **203** and the charge-storage insulating film **204**. As shown in FIGS. **17**A to **17**D, regardless of the form of the distribution of the concentration of the predetermined element, the effects of the present embodiment are exerted provided that the predetermined element in the intermediate insulating film **203***b* has a higher average concentration than that in the charge-storage insulating film **204**.

[0115] According to the above-described embodiment, the intermediate insulating film **203***b*, a part of the tunnel insulating film **203**, contains a larger amount of the predetermined element (deuterium, hydrogen, fluorine, or chlorine) than the charge-storage insulating film **204**. Thus, when a large amount of the predetermined element is contained in the silicon nitride film in the tunnel insulating film **203**, dangling bonds present in the silicon nitride film can be terminated. Thus, the charge trap state is reduced. Moreover, dangling bonds can be terminated which are present at the interface between the lower insulating film **203***a* and the intermediate insulating film **203***b* and at the interface between the intermediate insulating film **203***b* and the upper insulating film **203***c*. The charge-storage insulating layer **204** contains almost none of the predetermined element and is thus in a sufficient charge trap state. Thus, charges can be reliably stored in the charge-storage insulating film **204**. As a result, the present embodiment can provide a nonvolatile semiconductor memory device with an excellent write/erase property, an excellent charge retention property, and high reliability.

[0116] If the intermediate insulating film **203***b* contains deuterium or hydrogen, the elements diffuse to the interface between the semiconductor substrate **201** and the lower insulating film **203***a* to terminate the dangling bonds. This prevents the films from being degraded under write or erase stress. This improvement effect is enhanced particularly when the intermediate insulating film **203***b* contains deuterium.

[0117] FIGS. **18** to **23** are sectional views schematically showing a basic method for manufacturing the semiconductor device according to the present embodiment; the sectional views are taken along the bit line direction.

[0118] First, as shown in FIG. **18**, the semiconductor substrate **201** is cleaned.

[0119] Then, as shown in FIG. **19**, as is the case with the first embodiment, the surface of the semiconductor substrate **201** is oxidized by the thermal oxidation method at 800 to 1,000° C. to form a silicon oxide film having a thickness of about 1.0 to 2.5 nm and serving as a lower insulating film **203***a*. Furthermore, after the formation of the lower insulating film **203***a*, heat treatment is carried out in an NO atmosphere at 800 to 900° C. to introduce nitrogen into the interface between the semiconductor substrate **201** and the lower insulating film **203***a*. This improves the stress resistance of the tunnel insulating film **203**.

[0120] To form the lower insulating film **203***a* on the semiconductor substrate **201** by deposition, a silicon oxide film is deposited at 700 to 800° C. by the LPCVD method.

[0121] Thereafter, a silicon nitride film having a thickness of about 1.0 to 3.0 nm and serving as the intermediate insulating film **203***b* is formed on the lower insulating film **203***a* at a temperature of at most 450° C. Forming the silicon nitride film at the low temperature of at most 450° C. allows an appropriately flat silicon nitride film to be deposited on the lower insulating film **203***a*. Furthermore, the formation of the intermediate insulating film **203***b* at the low temperature makes hydrogen or chlorine (residues of an Si precursor) likely to remain in the silicon nitride film.

[0122] The ALD method is preferably used as a method of forming a silicon nitride film at the low temperature of at most 450° C. For example, DCS and ammonia may be used as a precursor.

[0123] Then, after the formation of the intermediate insulating film **203***b*, the above-described predetermined element is introduced. Specifically, the introduction is carried out as follows.

[0124] To allow fluorine to be introduced, heat treatment at 400 to 700° C. is carried out in an atmosphere containing fluorine. Then, fluorine can be introduced into the intermediate insulating film **203***b* and into the interface between the lower insulating film **203***a* and the intermediate insulating film **203***b*.

[0125] To allow deuterium or hydrogen to be introduced, heat treatment at 400 to 600° C. is carried out in an atmosphere containing deuterium or hydrogen. Then, deuterium or hydrogen can be introduced into the intermediate insulating film **203***b*, into the interface between the semiconductor substrate **201** and the lower insulating film **203***a*, and into the interface between the lower insulating film **203***a* and the intermediate insulating film **203***b*.

[0126] Then, as shown in FIG. **21**, after the intermediate insulating film **203***b* is reformed and heat treated, a silicon oxide film having a thickness of about 1.0 to 3.0 nm and serving as an upper insulating film **203***c* is deposited using the ALD method at 450 to 600° C. The upper insulating film **203***c* is formed by depositing a silicon oxide film on the intermediate insulating film **203***b* at a low temperature. After the formation of the upper insulating film **203***c*, oxygen may be introduced to reduce the charge trap state at the interface between the intermediate insulating film **203***b* and the upper insulating film **203***c*.

[0127] Then, as shown in FIG. **22**, as is the case with the first embodiment, a silicon nitride film serving as a charge-storage insulating film **204** is deposited on the upper insulating film **203***c* using the LPCVD method at 600° C. or higher. The formation of the charge-storage insulating layer **204** at the high temperature enables a reduction in the concentration of hydrogen and chlorine in the charge-storage insulating layer **204**.

[0128] Impurities (hydrogen and chlorine) in the charge-storage insulating film **204** can also be reduced by forming the charge-storage insulating film **204** using the ALD method at a temperature of at least 550° C. When the charge-storage insulating layer **204** is formed at a temperature of at most 550° C., heat treatment is carried out in an inert gas atmosphere at 700 to 1,000° C. to anneal out the impurities. The impurities can thus be reduced. This produces effects similar to those exerted when a silicon nitride film is formed by the LPCVD method.

[0129] Then, as is the case with the first embodiment, an alumina film having a thickness of about 10 to 20 nm and serving as a block insulating film **205** is formed on the charge-storage insulating film **204** using the ALD or MOCVD method. Moreover, polysilicon having a thickness of about 150 to 200 nm and serving as a control gate electrode film **206** is deposited by the LPCVD method.

[0130] Then, as shown in FIG. **23**, the control gate electrode **206** is formed by the lithography process as is the case with the first embodiment.

[0131] Thereafter, impurity elements such as arsenic are ion-injected into a surface region on the semiconductor substrate **201**, which is then heat treated. Thus, a source/drain region **202** is formed as shown in FIG. **16**.

[0132] Thereafter, well-known steps, that is, a step of forming an interlayer insulating film (not shown in the drawings) and a step of forming wiring (not shown in the drawings) and the like, are carried out to obtain a nonvolatile semiconductor memory device.

[0133] According to the present embodiment, the intermediate insulating film **203***b* is formed by introducing the predetermined element (deuterium, hydrogen, fluorine, or chlorine) into the silicon nitride film provided on the lower insulating film **203***a*. Introducing the predetermined element into the silicon nitride film in this manner allows the dangling bonds in the silicon nitride film to be terminated. The charge trap state can thus be significantly reduced.

[0134] According to the above-described embodiment, the silicon nitride film is formed on the lower insulating film **203***a* at the low temperature as is the case with the first embodiment. Thus, a high concentration of the predetermined element can be easily introduced into the silicon nitride film. Furthermore, the silicon nitride film can be appropriately flatly formed on the lower insulating film **203***a*. Consequently, a possible low-field leakage current through a local leakage path can be inhibited, thus improving the charge retention property. This also inhibits generation of the charge trap state caused by penetration of the nitriding agent to the interface between the semiconductor substrate **201** and the lower insulating film **203***a*. Thus, a possible trap assist tunnel current can be inhibited, enabling a reduction in the field leakage current from the tunnel insulating film **203**. As a result, the read disturb property can be drastically improved.

[0135] Furthermore, according to the above-described embodiment, the charge-storage insulating film **204** is formed by depositing a silicon nitride film on the upper insulating film **203***c* at the high temperature as is the case with the first embodiment. The formation at the high temperature allows

formation of a silicon nitride film into which the predetermined element is unlikely to be introduced. Thus, a sufficient trap state can be ensured.

(Modification)

[0136] FIGS. **24** to **30** are sectional views schematically showing a basic method for manufacturing a semiconductor device according to a modification of the second embodiment; the sectional views are taken along the bit line direction. The basic structure and the basic manufacturing method are similar to those in the above-described first and second embodiments. Thus, the matters described above in the above-described first and second embodiments and matters easily conceivable from the above-described first and second embodiments will not be described below.

[0137] First, as shown in FIG. **24**, the semiconductor substrate **201** is cleaned.

[0138] Then, as shown in FIG. **25**, the surface of the semiconductor substrate **201** is oxidized by the thermal oxidation method at 800 to 1,000° C. to form a silicon oxide film having a thickness of about 2.0 to 4.0 nm and serving as a lower insulating film **203***a*. Forming the lower insulating film **203***a* at the high temperature enables the reaction between the semiconductor substrate **201** and nitrogen to be inhibited when a silicon nitride film is formed during a subsequent step. Furthermore, after the formation of the lower insulating film **203***a*, heat treatment is carried out in an NO atmosphere at 800 to 900° C. to introduce nitrogen into the interface between the semiconductor substrate **201** and the lower insulating film **203***a*. This allows the stress resistance of the tunnel insulating film **203** to be improved.

[0139] Then, as shown in FIG. **26**, nitrogen is introduced into an upper portion of the silicon oxide film **203***a* by the plasma or radical nitriding method to form a silicon oxynitride film having a thickness of about 1.0 to 3.0 nm and serving as an intermediate insulating film **203***b*. As a result, the upper portion of the silicon oxide film **203***a* is reformed into a silicon oxynitride film containing a large amount of oxygen and in which a reduced number of charges are trapped. In this case, the thickness of the silicon oxide film **203***a* is reduced to about 1.0 to 2.0 nm. In the plasma or radical nitriding method, the surface of the silicon oxide film **203***a* may be exposed, at the room temperature to 500° C., to an atmosphere containing ions or radicals serving as a nitriding agent. Furthermore, to reduce damage that may occur during reformation, ICP or microwave excitation plasma is preferably used. After the reformation, heat treatment is carried out at 900 to 1,050° C. This preferably enables recovery from damage that may occur during the introduction of nitrogen.

[0140] Then, as shown in FIG. **27**, heat treatment may be additionally carried out, at 400 to 700° C., in an atmosphere containing steam, to introduce oxygen into the intermediate insulating film **203***b*.

[0141] Then, an intermediate insulating film **203***b* is formed, and the above-described predetermined element is introduced into the intermediate insulating film. Specifically, the introduction is performed as follows.

[0142] To allow fluorine to be introduced, heat treatment at 400 to 700° C. is carried out in an atmosphere containing fluorine. Then, fluorine can be introduced into the intermediate insulating film **203***b* and into the interface between the lower insulating film **203***a* and the intermediate insulating film **203***b*.

[0143] To allow deuterium or hydrogen to be introduced, heat treatment at 400 to 600° C. is carried out in an atmosphere containing deuterium or hydrogen. Then, deuterium or hydrogen can be introduced into the intermediate insulating film **203***b*, into the interface between the semiconductor substrate **201** and the lower insulating film **203***a*, and into the interface between the lower insulating film **203***a* and the intermediate insulating film **203***b*.

[0144] Then, as shown in FIG. **28**, after the intermediate insulating film **203***b* is reformed and heat treated, a silicon oxide film having a thickness of about 1.0 to 3.0 nm and serving as an upper insulating film **203***c* is deposited using the ALD method at 450 to 600° C. After the formation of the upper insulating film **203***c*, oxygen may be introduced into the intermediate insulating film **203***b* via the upper insulating film **203***c* in a diluted oxidizing atmosphere at 600 to 900° C. at which the elements are prevented from being relocated.

[0145] Then, as shown in FIG. **29**, as is the case with the first and second embodiments, a silicon nitride film serving as a charge-storage insulating film **204** is deposited on the upper insulating film **203***c* using the LPCVD method at 600° C. or higher. The formation of the charge-storage insulating layer **204** at the high temperature enables a reduction in the concentration of hydrogen and chlorine in the charge-storage insulating film **204**.

[0146] Then, as is the case with the first and second embodiments, an alumina film having a thickness of about 10 to 20 nm and serving as a block insulating film **205** is formed on the charge-storage insulating film **204** using the ALD or MOCVD method. Moreover, polysilicon having a thickness of about 150 to 200 nm and serving as a control gate electrode film **206** is deposited by the LPCVD method.

[0147] Then, as shown in FIG. **30**, the control gate electrode **206** is formed by the lithography process as is the case with the first and second embodiments.

[0148] Thereafter, impurity elements such as arsenic are ion-injected into a surface region on the semiconductor substrate **201**, which is then heat treated. Thus, a source/drain region **202** is formed as shown in FIG. **16**.

[0149] Thereafter, well-known steps, that is, a step of forming an interlayer insulating film (not shown in the drawings) and a step of forming wiring (not shown in the drawings) and the like, are carried out to obtain a nonvolatile semiconductor memory device.

[0150] The above-described modification exerts effects similar to those of the second embodiment. Furthermore, according to the above-described modification, the intermediate insulating film **203***b* is formed by nitriding the upper portion of the lower insulating film **203***a* by plasma or radical nitriding. Thus, the concentration of nitrogen in the intermediate insulating film **203***b* can be varied in stages from the surface to the interior of the film. This prevents a definite interface from being formed between the lower insulating film **203***a* and the intermediate insulating film **203***b*. Consequently, the charge trap state is reduced which is formed at the interface between the lower insulating film **203***a* and the intermediate insulating film **203***b*. Therefore, the charge retention property can be improved.

[0151] As is the case with the first embodiment, the charge trap state can be further reduced by introducing a large amount of oxygen into the intermediate insulating film **203***b*

and thereafter introducing the predetermined element (deuterium, hydrogen, fluorine, or chlorine) into the intermediate insulating film **203***b*.

Third Embodiment

[0152] FIG. **31** is a sectional view schematically showing the basic structure of a semiconductor device according to the present invention; the sectional view is taken along the bit line direction.

[0153] First, the configuration of the present embodiment will be described with reference to FIG. **31**. The basic structure and the basic manufacturing method are similar to those in the first embodiment. Thus, the matters described in the first embodiment and matters easily conceivable from the first embodiment will not be described below.

[0154] As shown in FIG. **31**, an element region with a source/drain region **302** is formed in a semiconductor substrate **301**. A tunnel insulating film **303** is formed on the element region. A charge-storage insulating film **304** is formed on the tunnel insulating film **303**. A block insulating film **305** is formed on the charge-storage insulating film **304**. A control gate electrode **306** is formed on the block insulating film **305**.

[0155] The tunnel insulating film **303** has a lower insulating film **303***a* containing silicon and oxygen, an intermediate insulating film **303***b* formed on the lower insulating film **303***a* and containing silicon and nitrogen, and an upper insulating film **303***c* formed on the intermediate insulating film **303***b* and containing silicon and oxygen. Specifically, the tunnel insulating film **303** has the lower insulating film **303***a* formed of a silicon oxide film and having a thickness of about 1 to 2 nm, the intermediate insulating film **303***b* formed of a silicon nitride with a low trap state density and having a thickness of about 1 to 3 nm, and the upper insulating film **303***c* formed of a silicon oxide film and having a thickness of about 1 to 4 nm.

[0156] The charge-storage insulating film **304** is formed of a silicon nitride film of thickness about 2 to 5 nm. The block insulating film **305** is formed of a silicon oxide film or a high-dielectric-constant insulating film of thickness about 10 to 25 nm. The high-dielectric-constant insulating film is, for example, alumina, which exhibits a large band gap. The control gate electrode **306** is formed of polysilicon or a metal material. The metal material is desirably metal with a high work function.

[0157] In the present embodiment, Si in the intermediate insulating film **303***b*, a part of the tunnel insulating film **303**, has a lower concentration than that in the charge-storage insulating film **304**. That is, the intermediate insulating film **303***b* has a lower Si composition ratio and a higher N composition ratio than the charge-storage insulating film **304**. As a result, the intermediate insulating film **303***b* has a lower trap state density than the charge-storage insulating film **304**.

[0158] In the above-described embodiment, the tunnel insulating film **303** has the stacked structure of the silicon oxide film, the silicon nitride film, and the silicon oxide film. This allows holes to be easily introduced into the charge-storage insulating film **304**, enabling the erase property to be improved.

[0159] According to the above-described embodiment, the intermediate insulating film **303***b* has a lower Si concentration than the charge-storage insulating film **304**. That is, the intermediate insulating film **303***b* is formed of a silicon nitride film with a low Si composition ratio. This enables a sufficient reduction in the charge trap state density of the intermediate insulating film **303***b*. The charge-storage insulating film **304** is formed of a silicon nitride film with a high Si composition ratio. Thus, the charge-storage insulating film **304** has a high charge trap state density and can thus reliably store charges.

[0160] As described above, in the present embodiment, the silicon nitride film provided in the tunnel insulating film **303** has a low charge trap state density. The silicon nitride film serving as the charge-storage insulating film **304** has a high charge trap state density. As a result, the present embodiment can provide a nonvolatile semiconductor memory device with an excellent write/erase property, an excellent charge retention property, and high reliability.

[0161] FIGS. **32** to **36** are sectional views schematically showing a basic method for manufacturing a semiconductor device according to the present embodiment; the views are taken alone the bit line direction.

[0162] First, as shown in FIG. **32**, the semiconductor substrate **301** is cleaned.

[0163] Then, as shown in FIG. **33**, as is the case with the first embodiment, the surface of the semiconductor substrate **301** is oxidized by the thermal oxidation method at 800 to 1,000° C. to form a silicon oxide film having a thickness of about 1.0 to 2.5 nm and serving as a lower insulating film **303***a*. Furthermore, after the formation of the lower insulating film **303***a*, heat treatment is carried out in an NO atmosphere at 800 to 900° C. to introduce nitrogen into the interface between the semiconductor substrate **301** and the lower insulating film **303***a*. This improves the stress resistance of the tunnel insulating film **303**.

[0164] To form the lower insulating film **303***a* on the semiconductor substrate **301** by deposition, a silicon oxide film is deposited at 700 to 800° C. by the LPCVD method.

[0165] Thereafter, a silicon nitride film with a very low charge trap state density is deposited by using the ALD method at a temperature of 300 to 400° C. and alternately supplying DCS and N_2* (N_2 radicals). In place of N_2*, N* (N radicals) or NH* (NH radicals) may be used. In the above-described manner, the silicon nitride film **303***b* with the very low trap density is formed on the lower insulating film **303***a*. The silicon nitride film **303***b* thus formed has a higher nitrogen ratio and a lower silicon ratio than common silicon nitride films.

[0166] Then, as shown in FIG. **34**, after the formation of the intermediate insulating film **303***b*, a silicon oxide film having a thickness of about 1.0 to 3.0 nm and serving as an upper insulating film **303***c* is deposited using the ALD method at 450 to 600° C.

[0167] Then, as shown in FIG. **35**, a silicon nitride film serving as a charge-storage insulating film **304** is deposited on the upper insulating film **303***c* using the LPCVD method at 600° C. or higher. At this time, supplying a large amount of Si precursor enables formation of a silicon nitride film containing a larger amount of silicon than a common stoichiometric composition

[0168] Even if the charge-storage insulating film **304** is formed by the ALD method at a temperature of at least 550° C., effects similar to those described above are exerted by supplying a large amount of Si precursor.

[0169] Then, as is the case with the first embodiment, an alumina film having a thickness of about 10 to 20 nm and serving as a block insulating film **305** is formed on the charge-storage insulating film **304** using the ALD or MOCVD method. Moreover, polysilicon having a thickness of about

150 to 200 nm and serving as a control gate electrode film **306** is deposited by the LPCVD method.

[0170] Then, as shown in FIG. **36**, the control gate electrode **306** is formed by the lithography process as is the case with the first embodiment.

[0171] Thereafter, impurity elements such as arsenic are ion-injected into a surface region on the semiconductor substrate **301**, which is then heat treated. Thus, a source/drain region **302** is formed as shown in FIG. **31**.

[0172] Thereafter, well-known steps, that is, a step of forming an interlayer insulating film (not shown in the drawings) and a step of forming wiring (not shown in the drawings) and the like, are carried out to obtain a nonvolatile semiconductor memory device.

[0173] According to the above-described embodiment, the intermediate insulating film **303***b* is formed by forming the silicon nitride film with the low Si composition ratio on the lower insulating film **303***a*. Thus, the charge trap state in the intermediate insulating film **303***b* can be reduced.

[0174] According to the above-described embodiment, the silicon nitride film is formed on the lower insulating film **303***a* at the low temperature as is the case with the first embodiment. Thus, the silicon nitride film can be appropriately flatly formed on the lower insulating film **303***a*. As a result, a possible low-field leakage current through a local leakage path can be inhibited, thus improving the charge retention property. This also inhibits generation of the charge trap state caused by penetration of the nitriding agent to the interface between the semiconductor substrate **301** and the lower insulating film **303***a*. Thus, a possible trap assist tunnel current can be inhibited, enabling a reduction in the field leakage current from the tunnel insulating film **303**. As a result, the read disturb property can be drastically improved.

[0175] According to the above-described embodiment, the charge-storage insulating film **304** in the sufficient charge trap state can be obtained by forming the silicon nitride film with the high Si composition ratio on the tunnel insulating film **303**. Furthermore, the charge-storage insulating film **304** is formed at the high temperature. Consequently, the silicon nitride film formed is excellent in oxidation resistance and the like, thus ensuring a sufficient charge trap state.

Fourth Embodiment

[0176] Now, a fourth embodiment will be described with reference to FIGS. **37**A to **61**B. In the present embodiment, the configuration of and the manufacturing method for the tunnel insulating film described above in the first to third embodiments are applied to a nonvolatile semiconductor memory device with a three-dimensional structure called bit-cost scalable (BiCS).

[0177] FIG. **37**A is a sectional view schematically showing the basic configuration of a semiconductor device according to the present embodiment. FIG. **37**B is a plan view schematically showing the basic configuration of a semiconductor device according to the present embodiment.

[0178] As shown in FIGS. **37**A and **37**B, a columnar semiconductor region (silicon region) **401** serving as an active region is formed on a substrate **400**. A tunnel insulating film **402**, a charge-storage insulating film **403**, and a block insulating film **404** are formed around the periphery of the semiconductor region **401**. That is, the tunnel insulating film **402** is formed on the surface of the semiconductor region **401**. The charge-storage insulating film **403** is formed on the surface of the tunnel insulating film **402**. The block insulating film **404** is formed on the surface of the charge-storage insulating film **403**.

[0179] The tunnel insulating film **402** has a first insulating film **402***a*, a second insulating film **402***b*, and a third insulating film **402***c*. The first insulating film **402***a* corresponds to the lower insulating films **103***a*, **203***a*, and **303***a* shown in the first to third embodiments. The second insulating film **402***b* corresponds to the intermediate insulating films **103***b*, **203***b*, and **303***b* shown in the first to third embodiments. The third insulating film **402***c* corresponds to the upper insulating films **103***c*, **203***c*, and **303***c* shown in the first to third embodiments. The various configurations and formation methods described in the first to third embodiments are applicable to the tunnel insulating film **402**.

[0180] A stacked structure of a plurality of control gate electrodes **405** and a plurality of interlayer insulating films **406** is formed around the periphery of the block insulating film **404**, that is, on the surface of the block insulating film **404**. The numbers of control gate electrodes **405** and interlayer insulating films **406** stacked are appropriately determined.

[0181] As is apparent from the above description, the above-described semiconductor device is configured such that a plurality of memory cells are stacked in the vertical direction. This enables an increase in the number of memory cells per unit area.

[0182] Now, with reference to FIGS. **37**A to **41**B, a basic manufacturing method for the semiconductor device according to the present embodiment will be described.

[0183] FIGS. **38**A to **41**A are sectional views schematically showing a part of the basic manufacturing method for the semiconductor device according to the present embodiment. FIGS. **38**B to **41**B are plan views schematically showing a part of the basic manufacturing method for the semiconductor device according to the present embodiment.

[0184] First, as shown in FIGS. **38**A and **38**B, silicon oxide film and impurities doped silicon film are alternately stacked a desired number of times using the CVD method; the silicon oxide film has a thickness of about 50 nm and serves as an interlayer insulating film **406**, and the silicon film has a thickness of about 50 nm and serves as a control gate electrode **405**.

[0185] Then, as shown in FIGS. **39**A and **39**B, the interlayer insulating film **406** and the control gate electrode **405** are selectively etched away by an RIE method using a resist mask (not shown in the drawings). Consequently, the semiconductor substrate **400** is exposed. Thus, a cylindrical hole **407** of diameter about 60 nm is formed in the stacked structure of the interlayer insulating films **406** and the control gate electrodes **405**. Thereafter, for example, an alumina film is deposited on the inner wall of the hole **407** using the ALD method; the alumina film has a thickness of about 10 nm, contains aluminum and oxygen as main components, and serves as a block insulating film **404**. Alternatively, the block insulating film **404** may be, for example, a silicon oxide film containing silicon and oxygen as main components.

[0186] Then, as shown in FIGS. **40**A and **40**B, a silicon nitride film having a thickness of about 5 nm and serving as a charge-storage insulating film **403** is deposited using the ALD method. Subsequently, a tunnel insulating film **402** of a stacked structure made up of a first insulating film **402***a*, a second insulating film **402***b*, and a third insulating film **402***c* is formed by a method described below.

[0187] Then, as shown in FIGS. **41**A and **41**B, the RIE method with a resist mask (not shown in the drawings) is carried out to selectively etch away the surface of the block insulating film **404**, charge-storage insulating film **403**, tunnel insulating film **402**, and semiconductor substrate **400** formed on the bottom surface of the hole **407**.

[0188] Then, as shown in FIGS. **37**A and **37**B, a silicon film into which impurities are doped so as to serve as a channel region is deposited by the CVD method. The silicon film is then heat treated in a nitrogen atmosphere at about 600° C. to form a semiconductor region **401**. Thereafter, a well-known technique is used to form wiring and the like (not shown in the drawings) to complete a nonvolatile semiconductor memory device.

[0189] The correspondence relationship between the present embodiment and the first to third embodiments will be described below.

[0190] First, with reference to FIGS. **37**A, **37**B, **40**A, **40**B, and **42**A to **45**B, the application of such a tunnel insulating film as described in the first embodiment to a tunnel insulating film according to the present embodiment will be described.

[0191] FIGS. **43**A to **45**A are sectional views schematically showing a basic method for manufacturing a tunnel insulating film in a semiconductor device according to the present embodiment. FIGS. **43**B to **45**B are plan views schematically showing the basic method for manufacturing the tunnel insulating film in the semiconductor device according to the present embodiment.

[0192] As shown in FIGS. **37**A and **37**B, as is the case with FIG. **1** for the first embodiment, a tunnel insulating film **402** according to the present embodiment has a first insulating film **402***a* containing silicon and oxygen, a second insulating film **402***b* formed on the surface of the first insulating film **402***a* and containing silicon, nitrogen, and oxygen, and a third insulating film **402***c* formed on the surface of the second insulating film **402***b* and containing silicon and oxygen. Specifically, the tunnel insulating film **402** has the first insulating film **402***a* formed of a silicon oxide film and having a thickness of about 1 to 2 nm, the second insulating film **402***b* formed of a silicon nitride film containing oxygen (for example, a silicon oxynitride film) and having a thickness of about 1 to 3 nm, and the third insulating film **402***c* formed of a silicon oxide film and having a thickness of about 1 to 4 nm.

[0193] The second insulating film **402***b*, a part of the tunnel insulating film **402**, has a higher oxygen concentration than a charge-storage insulating film **403**.

[0194] FIGS. **42**A to **42**E are diagrams of the distribution of the concentration of oxygen in the tunnel insulating film **402** and the charge-storage insulating film **403**. As shown in FIGS. **42**A to **42**E, regardless of the form of the distribution of the oxygen concentration, the effects of the present embodiment are exerted provided that the oxygen in the second insulating film **402***b* has a higher concentration than that in the charge-storage insulating film **403**.

[0195] The tunnel insulating film **402** configured as described above enables effects similar to those described in the first embodiment to be exerted.

[0196] A component material similar to that described in the first embodiment can be used for the tunnel insulating film **402**.

[0197] Now, a method for manufacturing the tunnel insulating film **402** corresponding to the first embodiment will be described.

[0198] First, as shown in FIGS. **43**A and **43**B, a silicon oxide film having a thickness of about 1.0 to 3.0 nm and serving as the third insulating film **402***c* is deposited on the exposed surface of the charge-storage insulating film **403** using the ALD method at 450 to 600° C.

[0199] Then, as shown in FIGS. **44**A and **44**B, a silicon nitride film having a thickness of about 1.0 to 3.0 nm and serving as the second insulating film **402***b* is formed on the exposed surface of the third insulating film **402***c* using the ALD method at 450° C. or lower.

[0200] Then, as shown in FIGS. **45**A and **45**B, the silicon nitride film formed at the low temperature is exposed to an oxidizing atmosphere at 400 to 900° C. to introduce oxygen into the exposed surface side region of the silicon nitride film. The second insulating film **402***b* is thus formed.

[0201] Then, as shown in FIGS. **40**A and **40**B, a silicon nitride film having a thickness of about 1.0 to 2.5 nm and serving as the first insulating film **402***a* is formed using the ALD method.

[0202] Thus, the tunnel insulating film **402** is formed which is similar to the tunnel insulating film **103** according to the first embodiment.

[0203] Forming the tunnel insulating film **402** as described above enables effects similar to those described in the first embodiment to be exerted.

[0204] Now, with reference to FIGS. **40**A, **40**B, **46**A, **46**B, **47**A, and **47**B, the application of such a variation of the tunnel insulating film as described for the modification of the first embodiment to the tunnel insulating film according to the present embodiment will be described.

[0205] FIGS. **46**A and **47**A are sectional views schematically showing a basic method for manufacturing a tunnel insulating film in a semiconductor device according to the present embodiment. FIGS. **46**B and **47**B are plan views schematically showing the basic method for manufacturing the tunnel insulating film in the semiconductor device according to the present embodiment.

[0206] First, as shown in FIGS. **46**A and **46**B, a silicon oxide film having a thickness of about 2.0 to 6.0 nm and serving as the third insulating film **402***c* is deposited on the exposed surface of the charge-storage insulating film **403** using the ALD method at 450 to 600° C. Nitrogen is subsequently introduced into the exposed surface portion of the silicon oxide film **402***c* by the plasma or radical nitriding method.

[0207] Then, as shown in FIGS. **47**A and **47**B, a silicon nitride film having a thickness of about 1.0 to 3.0 nm and serving as the second insulating film **402***b* is formed. As a result, the exposed surface portion of the silicon oxide film **402***c* is reformed into a silicon oxynitride film containing a large amount of oxygen and in which a reduced number of charges are trapped.

[0208] Then, as shown in FIGS. **40**A and **40**B, a silicon nitride film having a thickness of about 1.0 to 2.5 nm and serving as the first insulating film **402***a* is formed using the ALD method.

[0209] Thus, the tunnel insulating film **402** is formed which is similar to the tunnel insulating film **103** according to the first embodiment.

[0210] Forming the tunnel insulating film **402** as described above enables effects similar to those described for the modification of the first embodiment to be exerted.

[0211] Now, with reference to FIGS. **37**A, **37**B, **40**A, **40**B, and **48**A to **51**B, the application of such a tunnel insulating

film as described in the second embodiment to the tunnel insulating film according to the present embodiment will be described.

[0212] FIGS. **49**A to **51**A are sectional views schematically showing a basic method for manufacturing a tunnel insulating film in a semiconductor device according to the present embodiment. FIGS. **49**B to **51**B are plan views schematically showing the basic method for manufacturing the tunnel insulating film in the semiconductor device according to the present embodiment.

[0213] As shown in FIGS. **37**A and **37**B, as is the case with FIG. **16** for the second embodiment, a tunnel insulating film **402** according to the present embodiment has a first insulating film **402***a* containing silicon and oxygen, a second insulating film **402***b* formed on the surface of the first insulating film **402***a* and containing silicon, nitrogen, and a predetermined element selected from hydrogen, deuterium, and halogen, and a third insulating film **402***c* formed on the surface of the second insulating film **402***b* and containing silicon and oxygen. Specifically, the tunnel insulating film **402** has the first insulating film **402***a* formed of a silicon oxide film and having a thickness of about 1 to 2 nm, the second insulating film **402***b* formed of a silicon nitride film containing at least one element selected from deuterium, hydrogen, fluorine, and chlorine and having a thickness of about 1 to 3 nm, and the third insulating film **402***c* formed of a silicon oxide film and having a thickness of about 1 to 4 nm.

[0214] The predetermined element (deuterium, hydrogen, fluorine, or chlorine) in the second insulating film **402***b*, a part of the tunnel insulating film **402**, has a higher concentration than that in a charge-storage insulating film **403**.

[0215] FIGS. **48**A to **48**D are diagrams of the distribution of the concentration of the predetermined element (deuterium, hydrogen, fluorine, or chlorine) in the tunnel insulating film **402** and the charge-storage insulating film **403**. As shown in FIGS. **48**A to **48**D, regardless of the form of the distribution of the oxygen concentration, the effects of the present embodiment are exerted provided that the oxygen in the second insulating film **402***b* is higher than that in the charge-storage insulating film **403**.

[0216] The tunnel insulating film **402** configured as described above enables effects similar to those described in the second embodiment to be exerted.

[0217] A component material similar to that described in the second embodiment can be used for the tunnel insulating film **402**.

[0218] Now, a method for manufacturing the tunnel insulating film **402** corresponding to the second embodiment will be described.

[0219] First, as shown in FIGS. **49**A and **49**B, a silicon oxide film having a thickness of about 1.0 to 3.0 nm and serving as the third insulating film **402***c* is deposited on the exposed surface of the charge-storage insulating film **403** using the ALD method at 450 to 600° C.

[0220] Then, as shown in FIGS. **50**A and **50**B, a silicon nitride film having a thickness of about 1.0 to 3.0 nm and serving as the second insulating film **402***b* is formed on the exposed surface of the third insulating film **402***c* using the ALD method at 450° C. or lower.

[0221] Then, as shown in FIGS. **51**A and **51**B, after the second insulating film **402***b* is formed, the above-described predetermined element is introduced. Specifically, the introduction is performed as follows.

[0222] To allow fluorine to be introduced, heat treatment is performed in an atmosphere containing fluorine at 400 to 700° C. Then, the fluorine can be introduced into the second insulating film **402***b* and into the interface between the third insulating film **402***c* and the second insulating film **402***b*.

[0223] To allow deuterium or hydrogen to be introduced, heat treatment is performed in an atmosphere containing fluorine at 400 to 600° C. Then, the deuterium or hydrogen can be introduced into the second insulating film **402***b* and into the interface between the third insulating film **402***c* and the second insulating film **402***b*.

[0224] Then, as shown in FIGS. **40**A and **40**B, a silicon nitride film having a thickness of about 1.0 to 2.5 nm and serving as the first insulating film **402***a* is formed using the ALD method.

[0225] Thus, the tunnel insulating film **402** is formed which is similar to the tunnel insulating film **203** according to the second embodiment.

[0226] Forming the tunnel insulating film **402** as described above enables effects similar to those described in the second embodiment to be exerted.

[0227] Now, with reference to FIGS. **40**A, **40**B, and **52**A to **54**B, the application of such a variation of the tunnel insulating film as described for the modification of the second embodiment to the tunnel insulating film according to the present embodiment will be described.

[0228] FIGS. **52**A to **54**A are sectional views schematically showing a basic method for manufacturing a tunnel insulating film in a semiconductor device according to the present embodiment. FIGS. **52**B to **54**B are plan views schematically showing the basic method for manufacturing the tunnel insulating film in the semiconductor device according to the present embodiment.

[0229] First, as shown in FIGS. **52**A and **52**B, a silicon oxide film having a thickness of about 2.0 to 6.0 nm and serving as the third insulating film **402***c* is deposited using the ALD method at 450 to 600° C. Nitrogen is subsequently introduced into the exposed surface portion of the silicon oxide film **402***c* by the plasma or radical nitriding method.

[0230] Thus, as shown in FIGS. **53**A and **53**B, a silicon oxynitride film having a thickness of about 1.0 to 3.0 nm and serving as the second insulating film **402***b* is formed. As a result, the exposed surface portion of the silicon oxide film **402***c* is reformed into a silicon oxynitride film containing a large amount of oxygen and in which a reduced number of charges are trapped. The second insulating film **402***b* may additionally be subjected to heat treatment in an atmosphere containing steam at 400 to 700° C. to introduce oxygen into the second insulating film **402***b*.

[0231] Then, as shown in FIGS. **54**A and **54**B, after the second insulating film **402***b* is formed, the above-described predetermined element is introduced. Specifically, the introduction is performed as follows.

[0232] To allow fluorine to be introduced, heat treatment is performed in an atmosphere containing fluorine at 400 to 700° C. Then, the fluorine can be introduced into the second insulating film **402***b* and into the interface between the third insulating film **402***c* and the second insulating film **402***b*.

[0233] To allow deuterium or hydrogen to be introduced, heat treatment is performed in an atmosphere containing fluorine at 400 to 600° C. Then, the deuterium or hydrogen can be introduced into the second insulating film **402***b* and into the interface between the third insulating film **402***c* and the second insulating film **402***b*.

[0234] Then, as shown in FIGS. **40**A and **40**B, a silicon nitride film having a thickness of about 1.0 to 2.5 nm and serving as the first insulating film **402***a* is formed using the ALD method.

[0235] Thus, the tunnel insulating film **402** is formed which is similar to the tunnel insulating film **203** according to the second embodiment.

[0236] Forming the tunnel insulating film **402** as described above enables effects similar to those described in the modification of the second embodiment to be exerted.

[0237] Now, with reference to FIGS. **37**A, **37**B, **40**A, **40**B, and **55**A to **56**B, the application of such a tunnel insulating film as described in the third embodiment to the tunnel insulating film according to the present embodiment will be described.

[0238] FIGS. **55**A and **56**A are sectional views schematically showing a basic method for manufacturing a tunnel insulating film in a semiconductor device according to the present embodiment. FIGS. **55**B and **56**B are plan views schematically showing the basic method for manufacturing the tunnel insulating film in the semiconductor device according to the present embodiment.

[0239] As shown in FIGS. **37**A and **37**B, as is the case with FIG. **31** for the third embodiment, a tunnel insulating film **402** according to the present embodiment has a first insulating film **402***a* containing silicon and oxygen, a second insulating film **402***b* formed on the surface of the first insulating film **402***a* and containing silicon and nitrogen, and a third insulating film **402***c* formed on the surface of the second insulating film **402***b* and containing silicon and oxygen. Specifically, the tunnel insulating film **402** has the first insulating film **402***a* formed of a silicon oxide film and having a thickness of about 1 to 2 nm, the second insulating film **402***b* formed of a silicon nitride film and having a thickness of about 1 to 3 nm, and the third insulating film **402***c* formed of a silicon oxide film and having a thickness of about 1 to 4 nm.

[0240] In the tunnel insulating film **402**, the second insulating film **402***b* has a lower Si concentration than the charge-storage insulating film **403**. That is, the second insulating film **402***b* is formed of a silicon nitride film with a low Si composition ratio. This enables a sufficient reduction in the charge trap state density of the second insulating film **402***b*. The charge-storage insulating film **403** is formed of a silicon nitride film with a high Si composition ratio. Thus, the charge-storage insulating film **403** has a high charge trap state density and can thus reliably store charges.

[0241] The tunnel insulating film **402** configured as described above enables effects similar to those described in the third embodiment to be exerted.

[0242] A component material similar to that described in the third embodiment can be used for the tunnel insulating film **402**.

[0243] Now, a method for manufacturing the tunnel insulating film **402** corresponding to the third embodiment will be described.

[0244] First, as shown in FIGS. **55**A and **55**B, a silicon oxide film having a thickness of about 1.0 to 3.0 nm and serving as the third insulating film **402***c* is deposited using the ALD method at 450 to 600° C.

[0245] Then, as shown in FIGS. **56**A and **56**B, a silicon nitride film with a very low charge trap state density is deposited by using the ALD method at a temperature of 300 to 400° C. and alternately supplying DCS and N_2* (N_2 radicals). In place of N_2*, N* (N radicals) or NH* (NH radicals) may be used. In the above-described manner, the silicon nitride film (second insulating film) **402***b* with the very low trap density is formed on the third insulating film **402***c*. The silicon nitride film **402***b* thus formed has a higher nitrogen ratio and a lower silicon ratio than common silicon nitride films.

[0246] Then, as shown in FIGS. **40**A and **40**B, a silicon nitride film having a thickness of about 1.0 to 2.5 nm and serving as the first insulating film **402***a* is formed using the ALD method.

[0247] Thus, the tunnel insulating film **402** is formed which is similar to the tunnel insulating film **303** according to the third embodiment.

[0248] Forming the tunnel insulating film **402** as described above enables effects similar to those described in the third embodiment to be exerted.

[0249] In the above-described embodiments, the memory cell has the source/drain diffusion layer. However, the above-described embodiments exert similar effects on a memory cell without a source/drain diffusion layer, that is, what is called a depression memory cell.

[0250] Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

1. A semiconductor device comprising:

a semiconductor region;

a tunnel insulating film formed on a surface of the semiconductor region;

a charge-storage insulating film formed on a surface of the tunnel insulating film and containing silicon and nitrogen;

a block insulating film formed on a surface of the charge-storage insulating film; and

a control gate electrode formed on a surface of the block insulating film,

wherein the tunnel insulating film has a first insulating film formed on the surface of the semiconductor region and containing silicon and oxygen, a second insulating film formed on a surface of the first insulating film, and a third insulating film formed on a surface of the second insulating film and containing silicon and oxygen, and

a charge trap state in the second insulating film has a lower density than that in the charge-storage insulating film.

2. The device according to claim **1**, wherein the second insulating film contains silicon, nitrogen, and oxygen, and has a higher oxygen concentration than the charge-storage insulating film.

3. The device according to claim **2**, wherein the oxygen in the second insulating film has a higher average concentration than that in the charge-storage insulating film.

4. The device according to claim **2**, wherein the oxygen in a central portion of the second insulating film has a higher concentration than the oxygen in a vicinity of an interface between the first insulating film and the second insulating film and the oxygen in a vicinity of an interface between the second insulating film and the third insulating film.

5. The device according to claim **2**, wherein the oxygen in a central portion of the second insulating film has a lower concentration than the oxygen in a vicinity of an interface

between the first insulating film and the second insulating film and the oxygen in a vicinity of an interface between the second insulating film and the third insulating film.

6. The device according to claim **1**, wherein the second insulating film contains silicon, nitrogen, and a predetermined element selected from hydrogen, deuterium, and halogen, and the predetermined element in the second insulating film has a higher concentration than that in the charge-storage insulating film.

7. The device according to claim **6**, wherein the predetermined element in the second insulating film has a higher average concentration than that in the charge-storage insulating film.

8. The device according to claim **6**, wherein the predetermined element in a central portion of the second insulating film has a higher concentration than the predetermined element in a vicinity of an interface between the first insulating film and the second insulating film and the predetermined element in a vicinity of an interface between the second insulating film and the third insulating film.

9. The device according to claim **6**, wherein the predetermined element in a central portion of the second insulating film has a lower concentration than the predetermined element in a vicinity of an interface between the first insulating film and the second insulating film and the predetermined element in a vicinity of an interface between the second insulating film and the third insulating film.

10. The device according to claim **1**, wherein the second insulating film contains silicon and nitrogen, and has a lower silicon composition ratio than the charge-storage insulating film.

11. The device according to claim **10**, wherein the second insulating film has a higher nitrogen composition ratio than the charge-storage insulating film.

12. A method for manufacturing a semiconductor device a tunnel insulating film formed on a surface of a semiconductor region, a charge-storage insulating film formed on a surface of the tunnel insulating film and containing silicon and nitrogen, a block insulating film formed on a surface of the charge-storage insulating film, and a control gate electrode formed on a surface of the block insulating film,

wherein a process of manufacturing the tunnel insulating film comprises:

forming a first insulating film containing silicon and oxygen on the surface of the semiconductor region;

introducing nitrogen into an upper portion of the first insulating film to form a second insulating film containing silicon, nitrogen, and oxygen; and

forming a third insulating film containing silicon and oxygen on a surface of the second insulating film.

13. The method according to claim **12**, wherein nitrogen is introduced into the upper portion of the first insulating film using plasma or radicals.

14. The method according to claim **12**, wherein the second insulating film has a higher oxygen concentration than the charge-storage insulating film.

15. A method for manufacturing a semiconductor device comprising a tunnel insulating film formed on a surface of a semiconductor region, a charge-storage insulating film formed on a surface of the tunnel insulating film and containing silicon and nitrogen, a block insulating film formed on a surface of the charge-storage insulating film, and a control gate electrode formed on a surface of the block insulating film,

the tunnel insulating film including a first insulating film formed on a surface of the semiconductor region and containing silicon and oxygen, a second insulating film formed on a surface of the first insulating film and containing silicon and nitrogen, and a third insulating film formed on a surface of the second insulating film and containing silicon and oxygen,

wherein forming the second insulating film, the second insulating film is formed at a lower temperature than the charge-storage insulating film.

16. The method according to claim **15**, wherein the second insulating film has a lower silicon composition ratio than the charge-storage insulating film.

17. A method for manufacturing a semiconductor device comprising a tunnel insulating film formed on a surface of a semiconductor region, a charge-storage insulating film formed on a surface of the tunnel insulating film and containing silicon and nitrogen, a block insulating film formed on a surface of the charge-storage insulating film, and a control gate electrode formed on a surface of the block insulating film,

wherein a process of forming the tunnel insulating film comprises forming a third insulating film containing silicon and oxygen on an exposed surface of the charge-storage insulating film, introducing nitrogen into an exposed surface side region of the third insulating film to form a second insulating film containing silicon, nitrogen, and oxygen, and forming a first insulating film containing silicon and oxygen on an exposed surface of the second insulating film.

18. The method according to claim **17**, wherein nitrogen is introduced into the upper portion of the first insulating film using plasma or radicals.

19. The method according to claim **17**, wherein the second insulating film has a higher oxygen concentration than the charge-storage insulating film.

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