IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Sandisk Technologies, Inc.,
Petitioner,

v.

Longitude Flash Memory Solutions Ltd.,
Patent Owner.

_____

Case No. IPR2025-01281

U.S. Patent No. 11,456,365

_____

DECLARATION OF JUNE ANN MUNFORD

I, June Ann Munford, declare as follows:

I. Introduction

1. My name is June Ann Munford. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.

2. I have been retained on behalf of the Petitioner to provide assistance in the above-identified matter in establishing the authenticity and public availability of the documents discussed in this declaration. I am being compensated for my services in this matter at the rate of $200.00 per hour plus reasonable expenses. My statements are objective, and my compensation does not depend on the outcome of this matter.

II. Background

3. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.

4. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged,

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purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog search performance and creating lending agreements between libraries during my time as a Library Director.

5. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written in Machine Readable Catalog (herein referred to as "MARC") code and contain information such as a physical description of the material, metadata from the material's publisher, and date of library acquisition. In particular, the 008 field of the MARC record is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item's MARC record indicates the date of an item's public availability.

6. Typically, in creating a MARC record, a librarian would gather various bits of metadata such as book title, publisher and subject headings among others and assign each value to a relevant numerical field. For example, a book's

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physical description is tracked in field 300 while title/attribution is tracked in field 245. The 008 field of the MARC record is reserved for denoting the creation of the library record itself. As this is the only date reflecting the inclusion of said materials within the library's collection, it is my experience that an item's 008 field accurately indicates the date of an item's public availability.

7. I am familiar with the Internet Archive, a digital library accessible to the general public. Among other services that the Internet Archive makes available to the general public is the Wayback Machine, an online archive of the web. The Internet Archive's Wayback Machine service archives webpages as of a certain capture date to track changes in the web over time. The Internet Archive has been in operation as a nonprofit library since 1996 and has hosted the Wayback Machine service since its inception in 2001. During my time as a librarian, I frequently used the Internet Archive's Wayback Machine for research and instruction purposes. This includes teaching instructional classes on using the Wayback Machine to library patrons and using the Wayback Machine to research reference inquiries that require hard-to-find online resources. I consider the Internet Archive's recordskeeping to be as rigorous and detailed as other formal library recordskeeping practices such as MARC records, OCLC records and Dublin Core.

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III. Exhibit 1007 - History Of Semiconductors

8. I have reviewed Exhibit 1007, "History of Semiconductors" by Lidia Łukasiak, et al. as published in Journal of Telecommunications and Information Technology March 2010.

9. Attached hereto as Appendix LUKASIAK01 is a true and correct copy of the MARC record for Journal of Telecommunications and Information Technology as held by the National Library of Poland. I secured this record myself from the library's public catalog. The MARC record contained within Appendix LUKASIAK01 accurately describes the title, publisher and ISSN number of Journal of Telecommunications and Information Technology. The Egzemplarze W Tej Loaklizacji field present on page 4 of this record indicates the library's collection includes the March 2010 issue of Journal of Telecommunications and Information Technology containing "History of Semiconductors". In comparing Exhibit 1007 to Appendix LUKASIAK01, it is my determination that Exhibit 1007 is a true and correct copy of "History of Semiconductors" by Lidia Łukasiak, et al. as published in Journal of Telecommunications and Information Technology

10. The 008 field of the MARC record in Appendix LUKASIAK01 indicates the date of record creation. The 008 field of Appendix LUKASIAK01 indicates the National Library of Poland first acquired Journal of Telecommunications and Information Technology as of May 29, 2000 and held the

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journal in perpetuity until the publication of "History of Semiconductors". Considering this information, it is my determination that Journal of Telecommunications and Information Technology March 2010 and therefore "History of Semiconductors" was made available to the public shortly after its initial publication in March 2010.

IV. Exhibit 1018 - A Multi-Layer Stackable Thin-Film Transistor (TFT) Nand-Type Flash Memory

11. I have reviewed Exhibit 1018, "A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory" by Erh-Kun Lai, et al as published in Proceedings of the 2006 International Electron Devices Meeting.

12. Attached hereto as Appendix LAI01 is a true and correct copy of the MARC record for Proceedings of the 2006 International Electron Devices Meeting as held by the Penn State University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix LAI01 accurately describes the title, publisher and ISBN number of Proceedings of the 2006 International Electron Devices Meeting.

13. Attached hereto as Appendix LAI02 is a true and correct copy of "A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory" as published in Proceedings of the 2006 International Electron Devices Meeting as held by the Penn State University Library. This PDF was secured from the library's collection. In comparing Exhibit 1018 to Appendix LAI02, it is my

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determination that Exhibit 1018 is a true and correct copy of "A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory" by Erh-Kun Lai, et al as published in Proceedings of the 2006 International Electron Devices Meeting.

14. The 008 field of the MARC record in Appendix LAI01 indicates the date of record creation. The 008 field of Appendix LAI01 indicates the Penn State University Library first acquired Proceedings of the 2006 International Electron Devices Meeting as of May 5, 2006. Considering this information, it is my determination that Proceedings of the 2006 International Electron Devices Meeting and therefore "A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory" was made available to the public shortly after May 5, 2006.

V. Exhibit 1020 - Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells

15. I have reviewed Exhibit 1020, "Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells" by Antonio Arreghini, et al as published in IEEE Transactions on Electron Devices May 2008.

16. Attached hereto as Appendix ARREGHINI01 is a true and correct copy of the MARC record for IEEE Transactions on Electron Devices as held by the Penn State University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix ARREGHINI01

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accurately describes the title, publisher and ISSN number of IEEE Transactions on Electron Devices. The Showing Results field present on page 3 of this record indicates the library's collection includes the May 2008 issue of IEEE Transactions on Electron Devices containing "Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells".

17. Attached hereto as Appendix ARREGHINI02 is a true and correct copy of "Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells" as published in IEEE Transactions on Electron Devices as held by the Penn State University Library. These scans were secured from the library's collection. In comparing Exhibit 1020 to Appendix ARREGHINI02, it is my determination that Exhibit 1020 is a true and correct copy of "Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells" by Antonio Arreghini, et al as published in IEEE Transactions on Electron Devices.

18. The 008 field of the MARC record in Appendix ARREGHINI01 indicates the date of record creation. The 008 field of Appendix ARREGHINI01 indicates the Penn State University Library first acquired IEEE Transactions on Electron Devices as of June 29, 2000 and held the journal in perpetuity until the publication of "Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells". Considering this

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information, it is my determination that IEEE Transactions on Electron Devices May 2008 and therefore "Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells" was made available to the public shortly after its initial publication in May 2008.

VI. Exhibit 1025 - VDNROM: A Novel Four-Bits-Per-Cell Vertical Channel Dual-Nitride-Trapping-Layer ROM for High Density Flash Memory Applications

19. I have reviewed Exhibit 1025, "VDNROM: A Novel Four-Bits-Per-Cell Vertical Channel Dual-Nitride-Trapping-Layer ROM for High Density Flash Memory Applications" by Falong Zhou, et al as published in Proceedings of the 2006 European Solid-State Device Research Conference.

20. Attached hereto as Appendix ZHOU01 is a true and correct copy of the MARC record for Proceedings of the 2006 European Solid-State Device Research Conference as held by the Penn State University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix ZHOU01 accurately describes the title, publisher and ISBN number of Proceedings of the 2006 European Solid-State Device Research Conference.

21. Attached hereto as Appendix ZHOU02 is a true and correct copy of "VDNROM: A Novel Four-Bits-Per-Cell Vertical Channel Dual-Nitride-Trapping-Layer ROM for High Density Flash Memory Applications" as published in

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Proceedings of the 2006 European Solid-State Device Research Conference as held by the Penn State University Library. These scans were secured from the library's collection. In comparing Exhibit 1025 to Appendix ZHOU02, it is my determination that Exhibit 1025 is a true and correct copy of "VDNROM: A Novel Four-Bits-Per-Cell Vertical Channel Dual-Nitride-Trapping-Layer ROM for High Density Flash Memory Applications" by Falong Zhou, et al as published in Proceedings of the 2006 European Solid-State Device Research Conference.

22. The 008 field of the MARC record in Appendix ZHOU01 indicates the date of record creation. The 008 field of Appendix ZHOU01 indicates the Penn State University Library first acquired Proceedings of the 2006 European Solid-State Device Research Conference as of April 4, 2006. Considering this information, it is my determination that Proceedings of the 2006 European Solid-State Device Research Conference and therefore "VDNROM: A Novel Four-Bits-Per-Cell Vertical Channel Dual-Nitride-Trapping-Layer ROM for High Density Flash Memory Applications" was made available to the public shortly after April 4, 2006.

VII. Exhibit 1026 - Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory

23. I have reviewed Exhibit 1026, "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory" by H. Tanaka, et al as published in Proceedings of the 2007 Symposium on VLSI Technology.

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24. Attached hereto as Appendix TANAKA01 is a true and correct copy of the MARC record for Proceedings of the 2007 Symposium on VLSI Technology as held by the Rochester Institute of Technology Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix TANAKA01 accurately describes the title, publisher and ISBN number of Proceedings of the 2007 Symposium on VLSI Technology. In comparing Exhibit 1026 to Appendix TANAKA01, it is my determination that Exhibit 1026 is a true and correct copy of "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory" by H. Tanaka, et al as published in Proceedings of the 2007 Symposium on VLSI Technology.

25. The 008 field of the MARC record in Appendix TANAKA01 indicates the date of record creation. The 008 field of Appendix TANAKA01 indicates the Rochester Institute of Technology Library first acquired Proceedings of the 2007 Symposium on VLSI Technology as of August 17, 2009. Considering this information, it is my determination that Proceedings of the 2007 Symposium on VLSI Technology and therefore "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory" was made available to the public shortly after August 17, 2009.

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VIII. Exhibit 1027 - Toshiba Develops New NAND Flash Technology

26. I have reviewed Exhibit 1027, a web page entitled "Toshiba Develops New NAND Flash Technology".

27. Attached hereto as Appendix TOSHIBA01 is a screen capture of the Internet Archive Wayback Machine entry for http://www.toshiba.co.jp/about/press/2007_06/pr1201.htm. I secured these screen captures myself from https://web.archive.org/web/20070614211920/http://www.toshiba.co.jp/about/press/2007_06/pr1201.htm. This record was captured as of June 14, 2007.

28. Appendix TOSHIBA01 is an Internet Archive capture of a web page entitled "Toshiba Develops New NAND Flash Technology" as hosted on the Toshiba website. In comparing Appendix TOSHIBA01 to Exhibit 1027, it is my determination that Exhibit 1027 is a true and correct copy of the "Toshiba Develops New NAND Flash Technology" web page as hosted on the Toshiba website. As the Internet Archive first captured this page as of June 14, 2007, it is my determination that "Toshiba Develops New NAND Flash Technology" was first made available to the public as of June 14, 2007 via the Internet Archive and likely earlier via the original Toshiba website.

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IX. Exhibit 1029 - A Comparison of N+ and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories

29. I have reviewed Exhibit 1029, "A Comparison of N+ and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories" by Moon Kyung Kim, et al as published in MRS Online Proceedings Library January 2007.

30. Attached hereto as Appendix KIM01 is a true and correct copy of the MARC record for MRS Online Proceedings Library as held by the Penn State University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix KIM01 accurately describes the title, publisher and ISSN number of MRS Online Proceedings Library. The Showing Results field present on page 4 of this record indicates the library's collection includes the January 2007 issue of MRS Online Proceedings Library containing "A Comparison of N+ and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories".

31. Attached hereto as Appendix KIM02 is a true and correct copy of "A Comparison of N+ and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories" as published in MRS Online Proceedings Library as held by the Penn State University Library. This PDF was secured from the library's collection. In comparing Exhibit 1029 to Appendix KIM02, it is my determination that Exhibit 1029 is a true and correct copy of "A Comparison of N+ and P+ Type Polysilicon

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Gate in High Speed Non-Volatile Memories" by Moon Kyung Kim, et al as published in MRS Online Proceedings Library.

32. The 008 field of the MARC record in Appendix KIM01 indicates the date of record creation. The 008 field of Appendix KIM01 indicates the Penn State University Library first acquired MRS Online Proceedings Library as of February 2, 2005 and held the journal in perpetuity until the publication of "A Comparison of N+ and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories". Considering this information, it is my determination that MRS Online Proceedings Library January 2007 and therefore "A Comparison of N+ and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories" was made available to the public shortly after its initial publication in January 2007.

X. Exhibit 1042 - Physics of Semiconductor Devices

33. I have reviewed Exhibit 1042, Physics of Semiconductor Devices by S.M. Sze, et al.

34. Attached hereto as Appendix SZE01 is a true and correct copy of the MARC record for Physics of Semiconductor Devices as held by the Carnegie Mellon University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix SZE01 accurately describes the title, author, publisher, and ISBN number of Physics of Semiconductor Devices.

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35. Attached hereto as Appendix SZE01 is a true and correct copy of Physics of Semiconductor Devices as held by the Carnegie Mellon University Library. These scans were secured from the library's collection. In comparing Exhibit 1042 to Appendix SZE01, it is my determination that Exhibit 1042 is a true and correct copy of Physics of Semiconductor Devices by S.M. Sze, et al.

36. The 008 field of the MARC record in Appendix SZE01 indicates the date of record creation. The 008 field of Appendix SZE01 indicates the Carnegie Mellon University Library first acquired Physics of Semiconductor Devices as of October 11, 2007. Considering this information, it is my determination that Physics of Semiconductor Devices was made available to the public shortly after its initial acquisition as of October 11, 2007.

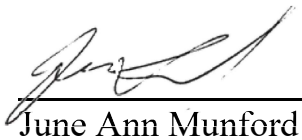
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XI. Conclusion

37. I declare under penalty of perjury that the foregoing is true and correct. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on August 22, 2025

By:



June Ann Munford

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Appendix CV

June A. Munford
Curriculum Vitae

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.

- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.

- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over $400,000 and total assets of approximately $1,300,000.

● Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.

● Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.

● Led the organization and digitization of the library's archival records.

● Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.

● Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013
Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

● Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.

● Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.

● Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013
Library Assistant, Hart Area Public Library
Hart, MI

● Responsible for verifying imported MARC records and original MARC cataloging for the local-level collection as well as the Michigan Electronic Library.

● Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter

- Treasurer, 2012

Library Of Michigan
- Level VII Certification, 2008
- Level II Certification, 2013

Michigan Library Association Annual Conference 2014
- New Directors Conference Panel Member

Southwest Michigan Library Cooperative
- Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008
Petoskey, MI
- Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011
Nashville, TN
- Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012
Fairbanks, AK
- Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 ● Fish & Richardson

Apple v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282 and 39521-00421IP2)

2019 ● Erise IP

Implicit, LLC v. Netscout Systems, Inc (Case No. 2:18-cv-53-JRG)

2019 ● Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Case No. IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 ● O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case No. 5:19-cv-00036-RWS)

2021 ● Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (Case No. IPR2020-1449)

2022 ● Perkins-Coie

Realtek v. Future Link (Case No. IPR2021-01182)

2023 ● Fish & Richardson

Neuroderm Ltd. v. Abbvie, Inc (Case No. PGR2022-00040)

2023 ● Fish & Richardson

Nearmap US Inc. v. Pictometry International Corp. (Case No. IPR2022-00735)

2023 ● Fish & Richardson

Samsung Electronics v. MemoryWeb LLC (Case No. 39843-0136PS1)

2023 ● Pillsbury Winthrop Shaw Whitman LLP

Gravel Rating Systems v. Costco Wholesale Corp. (Case No. 4:21-cv-149-ALM)

2024 ● Willkie-Farr

Netflix, Inc. v. VideoLabs. Inc. (Case No. IPR2023-00628)

2024 ● Quinn Emanuel Urquhart & Sullivan

Purdue University v. Wolfspeed (Case No. 1:21-CV-840)

2024 ● Fish & Richardson

Dish Network v. Entropic Communications (Case No. IPR2024-00393)

2025 ● Perkins Coie

Amazon.com, Inc. v. Nokia Technologies Oy (Case No. IPR2024-00572)

2025 ● Fish & Richardson

Dish Network v. Entropic Communications (Case No. IPR2024-00373)

Limited Case and Clientele History

Alston & Bird

- Ericsson

  v. Collision Communications (Case No. IPR2022-01233)

- Nokia

  v. Neptune Subsea, Xtera (Case No. 1:17-cv-01876)

- Universal Electronics Inc

  v. Roku Inc (Case No. IPR2022-00818)

Alavi & Anaipakos PLLC

- Stingray Group Inc. and Stingray Music USA, Inc.

  v. Edwin A. Hernandez-Mondragon and Egla Corp. (Case No. 1:24-cv-21226-RAR)

Arnold & Porter

- Ivantis

  v. Glaukos (Case No. 8:18-cv-00620)

- Samsung

  v. Jawbone (Case No. 2:21-cv-00186)

Benesch Friedlander Coplan & Aronoff

- Voyis

  v. Cathx (Case No. 5:21-cv-00077-RWS)

Buchanan, Ingersoll & Rooney PC

- Google LLC, AT&T Service Inc., T Mobile USA Inc., Cellco Partnership, Ericsson Inc. & Nokia of America Corp.

  v. KT Corp & Pegasus Wireless Innovation LLC (Case No. IPR2025-00293)

Deschert LLP

- Smaxtec Animal Care

  v. ST Reproductive Technologies, LLC (Case No. IPR2024-00885)

Duane Morris

- Kangxi Communication Technologies

  v. Skyworks Solutions Inc. (Case No. IPR2025-00373)

- Microsoft

  v. Edge Networking Systems LLC (Case No. 1:24-cv-00215)

Erise I.P.

- Apple

  v. Ericsson Inc. (Case No. IPR2022-00715)

  v. Future Link Systems (Case No. IPRs 6317804, 6622108, 6807505, and 7917680)

  v. INVT (Case No. 20-1881)

  v. Navblazer LLC (Case No. IPR2020-01253)

  v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

v. Quest Nettech Corp (Case No. 2:19-cv-00118-JRG)

v. Telefonaktiebolaget LM Ericsson (Case No. IPR2022-00275)

v. Theta IP, LLC (Case No. IPR2024-00818)

v. THL Holding Company LLC (Case No. 1:23-cv-00548)

- Fanduel

v. CGT (Case No. 19-1393)

- Garmin

v. Phillips North America LLC (Case No. 2:19-cv-6301-AB-KS)

- Netscout

v. Longhorn HD LLC (Case No. 2:20-cv-00349)

v. Implicit, LLC (Case No. 2:18-cv-53-JRG)

- Sony Interactive Entertainment LLC

v. Bot M8 LLC (Case No. IPR2020-01288)

v. Infernal Technology LLC (Case No. 2:19-CV-00248-JRG)

- Tesla

v. Charge Fusion Technologies LLC (Case No. IPR2025-00032)

- Unified Patents

v. GE Video Compression (Case No. 2:19-cv-248)

Fish & Richardson

- Apple

v. AliveCor (Case No. 3:21-cv-03958)

v. LBS Innovations (Case No. 2:19-cv-00119-JRG-RSP)

v. Koss Corporation (Case No. IPR2021-00305)

v. Masimo (Case No. IPR 50095-0012IP1, 50095-0012IP2, 50095-0013IP1, 50095-0013IP2, 50095-0006IP1, 50095-0135IP1)

v. Neonode (Case No. 21-cv-08872-EMC)

v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

v. Resonant Sys. (Case No. 7:23-cv-00077-ADA)

- AsusTek Computer Inc.
  v. Videolabs, Inc. (Case No. 22-CV-00720-ADA)

- Dell
  v. Neo Wireless (Case No. IPR2022-00616)

- Dish Network

  v. Entropic Communications, LLC (Case No. 2:2023-CV-01043)

  v. Entropic Communications LLC (Case No. IPR2024-00393)

  v. Realtime Adaptive Streaming (Case No. 1:17-CV-02097-RBJ)

  v. TQ Delta LLC (Case No. 18-1798)

- Evapco Dry Cooling

  v. SPG Dry Cooling (Case No. IPR2021-00688)

- Genetec

  v. Sensormatic Electronics (Case No. 1:20-CV-00760)

- Huawei

  v. Bell Northern Research LLC (Case No. IPR2019-01174)

- Kianxis

  v. Blue Yonder (Case No. 3:20-cv-03636)

- LG Electronics

  v. Bell Northern Research LLC (Case No. 3:18-cv-2864-CAB-BLM)

- MediaTek

  v. MOSAID (Case No. IPR2024-00718)

- Metaswitch

  v. Sonus Networks (Case No. IPR2018-01719)

- Microsoft

  v. Throughputer Inc (Case No. IPR2022-00757)

- Mom Enterprises

  v. Ddrops Company (Case No. 1:22-cv-00332)

- MLC Intellectual Property

  v. MicronTech (Case No. 3:14-cv-03657-SI)

- Nearmap Inc

  v. EagleView Technologies (Case No. IPR2022-01009)

- Neuroderm Ltd.

  v. Abbvie, Inc (Case No. PGR2022-00040)

- Posco Co Ltd.

  v. Pascal Drillet et al. (Case No. IPR2025-00370)

- Realtek Semiconductor

  v. Future Link (Case No. IPR2021-01182)

- Quectel
  - v. Koninklijke Philips (Case No. 1:20-cv-01710)

- Samsung
  - v. Aire Technology (Case No. IPR2022-00877)
  - v. Bell Northern Research (Case No. 2:19-cv-00286-JRG)
  - v. Communication Technologies Inc (Case No. IPR2022-01221)
  - v. Jawbone Innovations (Case No. IPR2022-00865)
  - v. MemoryWeb LLC (Case No. IPR2022-00885)
  - v. Dodots Licensing Solutions (Case No. IPR2023-00701)
  - v. Telefonaktiebolaget LM Ericsson (Case No. IPR2021-00615)

- Texas Instruments
  - v. Vantage Micro LLC (Case No. IPR2020-01261)

- Xilinx
  - v. Sentient Sensors LCC (Case No. 1:22-cv-00173)

Goodwin Proctor

- Intel
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Appendix LAI02

A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory

*Erh-Kun Lai, Hang-Ting Lue, Yi-Hsuan Hsiao, Jung-Yu Hsieh, Chi-Pin Lu, *Szu-Yu Wang, Ling-Wu Yang, Tahone Yang, Kuang-Chao Chen, +Jeng Gong, Kuang-Yeu Hsieh, Rich Liu, and Chih-Yuan Lu

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Abstract

A double-layer TFT NAND-type Flash memory is demonstrated, ushering into the era of three-dimensional (3D) Flash memory. A TFT device using bandgap engineered SONOS (BE-SONOS) [1,2] with fully-depleted (FD) poly silicon (60 nm) channel and tri-gate P^+-poly gate is integrated into a NAND array. Small devices (L/W=0.2/0.09 μm) with excellent performance and reliability properties are achieved. The bottom layer shows no sign of reliability degradation compared to the top layer, indicating the potential for further multi-layer stacking. The present work illustrates the feasibility of 3D Flash memory.

I. Introduction

Recently, the NAND flash becomes very popular for portable electronics, and the demand for memory density multiplies every year. Although NAND Flash is aggressively scaled [3,4], it becomes more and more difficult to follow Moore's law to continue the scaling due to both process and device limitations. Three-dimensional (3D) multi-layer-stack memory is another path to ultra-high density memory.

We demonstrated a low-thermal budget TFT NAND device recently [2]. The TFT memory employs BE-SONOS [1] device, which provides both efficient hole tunneling erase and good data retention [1]. Moreover, BE-SONOS uses only matured frond-end materials (oxide, nitride and poly gate). This greatly enables the multi-layer stack capability without metal contamination issues. In this work, we further fabricate a double-layer TFT NAND Flash. The performance and reliability of bottom and top layers are examined to provide guidelines for further multi-layer stacking. The effects of device dimension, reliability, and NAND array operation are addressed.

II. Fabrication

The typical device parameters and fabrication flow are shown in Table 1 and Table 2. Figures 1-4 show the cross-sectional views of the double layer TFT NAND devices. The TFT device has a 60 nm thick poly silicon channel over the buried oxide. The poly silicon is an amorphous silicon (a-Si) layer deposited by low-pressure chemical vapor deposition (LPCVD) process, followed by a low-temperature thermal annealing (600 ^{0}C) for crystallization. A multi-layer O1/N1/O2 tunneling dielectric is used to achieve easy hole tunneling during erase, while eliminating the direct tunneling leakage during retention [1]. Next, SiN trapping layer (N2) and top blocking oxide (O3) are grown. A heavily doped P^+-poly gate is adopted to suppress the gate injection during –FN erase. The multi-layer ONONO are shown in Fig. 1. The device has a tri-gate structure as shown in Fig. 2.

The top oxide process has the largest thermal budget. Two top oxide (O3) formation processes are compared: an LPCVD oxide (HTO) with rapid thermal annealing, and an in-situ steam generation (ISSG) oxidation to convert a portion of the trapping nitride (N2) into oxide.

After gate patterning, shallow junction is formed by low-energy As^+ implantation. Planarization is then carried out by HDP oxide deposition and CMP. After forming the bottom-layer TFT devices, the processes are duplicated to form the top-layer TFT devices. Contact etching for the two layers are performed independently to avoid over etching. The final double-layer TFT NAND Flash memory is shown in Figs. 3-4.

III. Device Characterization

(a) Short-Channel Effect:

The *I-V* and V_T for the memory cells with various channel lengths are shown in Figs. 5, 6, respectively. Similar to bulk devices, the transconductance (g_m) increases with shorter channel lengths. Figure 6 shows that the –FN erased state (-17 V, 50 msec) follows the same Vt-roll-off characteristics with the initial state, but with 3 V lower Vt. ISSG and HTO top oxide devices show similar Vt roll-off trends.

(b) Narrow-Width Effect:

The *I-V* characteristics for memory cells with various channel widths are shown in Fig. 7. Generally a narrower device shows a better subthreshold slope (S.S.). Figure 8 shows that for a narrow device the transconductance per width (g_m/W) increases, while Vt decreases. Thus a narrower device has a better DC performance due to better gate control capability of the tri-gate structure.

(c) Program/Erase Characteristics:

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The device is programmed by +FN electron injection (Fig. 9), and erased by –FN hole tunneling (Fig. 10). P^+-poly gate is used to suppress the gate electron injection during –FN erase. Accordingly, the device can be erased into depletion mode. Both +FN program and –FN erase saturate for each bias voltage. Samples with ISSG and HTO top oxide show similar P/E speed.

(d) P/E Cycling Endurance:

The P/E cycling endurance is shown in Fig. 11. Erase degradation occurs at < 1K dumb-mode cycles. ISSG top oxide devices show better endurance than those with HTO top oxide. The top oxide process has large impact on the cell endurance because top oxide suffers a large electric field stress during P/E, while the top oxide has lower quality due to the lower thermal process.

The endurance of TFT device is understandably inferior to the bulk BE-SONOS device [1,5], where a high-temperature (950~1000 ^{0}C) process is used to convert nitride into top oxide. The reason may be attributed to that the lower temperature ISSG and HTO top oxides have lower quality that easily trap charges after P/E cycle stressing, resulting in lower endurance.

Adjusted P/E cycling (as commonly practiced) achieves better endurance (Fig. 12). The corresponding P/E shot numbers are recorded in Fig. 13. After 1K cycling the device starts to degrade and more P/E shots are needed to maintain the Vt levels. Figure 14 illustrates that ISSG top oxide has a better subthreshold slope than HTO top oxide. Typical *IV* characteristics during 10K P/E cycling are shown in Fig. 15.

IV. Comparison between the Top and Bottom Layers

Figure 16 compares the V_T-roll-off of erase saturation state for the bottom and top layers. The bottom layer has a slightly faster V_T-roll-off. In addition, the V_T distribution of the bottom-layer is wider. This is because the bottom layer undergoes a higher thermal budget. For better bottom layer performance thermal budget should be further reduced.

The P/E cycle endurance, S.S. degradation, and retention are shown in Figs. 17, 18 and 19, respectively, for the short-channel device (Lg/W=0.2/0.09 um). The bottom layer shows no sign of reliability degradation compared to the top layer. This indicates that further multi-layer stack is feasible.

V. NAND Array Functions

The reading method for the NAND array is shown in Fig. 20. Since TFT NAND array has higher series resistance compared to the bulk device, read current saturates at large gate overdrive. The read current is enhanced by increasing V_{PASS}. For V_{PASS}=7 V, and V_{READ}=1 V, the read current for a 16-string NAND array approaches 1 μA, ample for data Flash design.

The program-inhibit characteristics of TFT NAND array are illustrated in Fig. 21. Cells C and D are under medium-field gate disturb, while cell B can be program-inhibited by raising the channel potential.

VI. Summary

For the first time, a successful double-layer TFT NAND Flash memory is demonstrated. The experimental results are very encouraging for future 3D Flash memories.

VII. Acknowledgements

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Poly channel thickness	60 nm
O1	1.5 nm (ISSG)
N1	2 nm (LPCVD)
O2	2 nm (LPCVD)
N2	7 nm (LPCVD)
O3	9 nm (ISSG or HTO)
Poly gate	P^+-poly
Channel length	0.2 um
Channel width	0.09 um

Table 1 Typical process condition of TFT NAND device.

1. Si substrate	9. N^+ S/D & pocket implantation
2. Buried oxide	10. HDP CVD deposition
3. a-Si channel deposition	11. Oxide CMP planarization
4. Low-temperature annealing	12. Repeat processes from a-Si to N^+ S/D implantation
5. Channel patterning	13. ILD deposition and planarization
6. P-type well doping	14. Contact patterning
7. BE-SONOS: ONONO formation	15. Metal deposition and patterning
8. P^+poly gate patterning	16. Alloy annealing

Table 2 Fabrication flow of multi-layer TFT NAND device

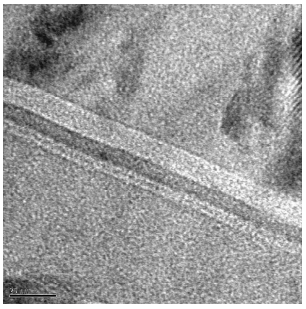


Fig. 1 TEM of the O1/N1/O2/N2/O3 structure for TFT BE-SONOS.

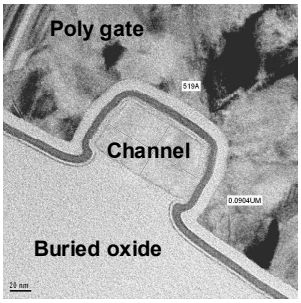


Fig. 2 Tri-gate structure of the TFT device.

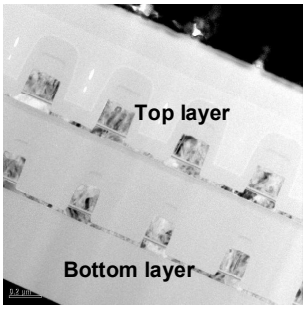


Fig. 3 Channel-length direction of double-layer TFT NAND devices.

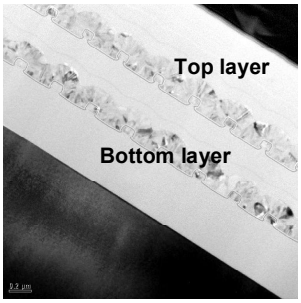


Fig. 4 Channel-width direction of double-layer TFT NAND devices.

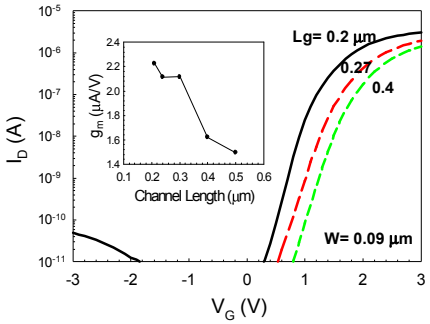


Fig. 5 *IV* characteristics for various channel length devices. Inset shows the corresponding transconductance (g_m). The channel width is 0.09 µm.

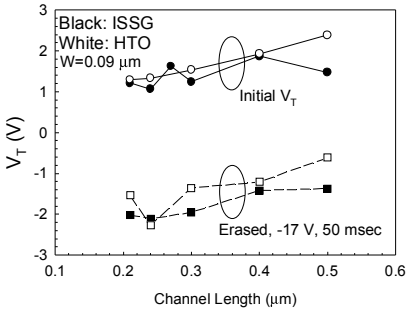


Fig. 6 Short-channel V_T roll-off characteristics for both the initial state and the –FN erased state, with ISSG and HTO top oxide.

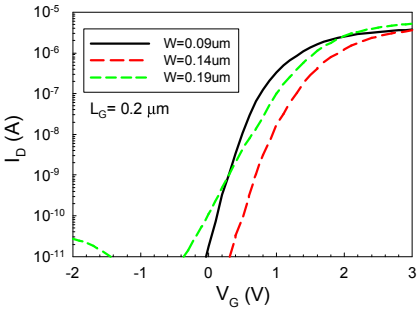


Fig. 7 *IV* characteristics for various channel width devices. Wider devices show worse subthreshold behavior. The channel length is 0.2 µ m.

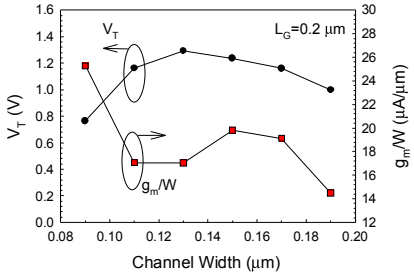


Fig. 8 Narrow-width characteristics. Both normalized transconductance (g_m/W) and V_T are shown. The narrowest device (W=0.09 µm) has the best performance.

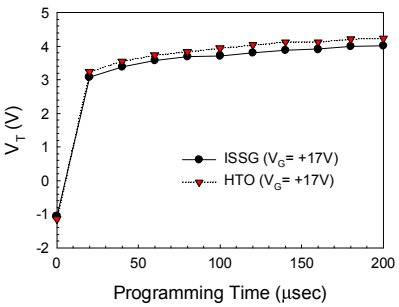


Fig. 9 Comparison of the +FN program characteristics for ISSG and HTO top oxide.

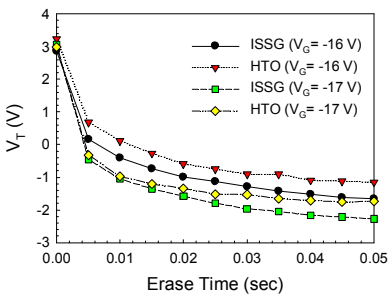


Fig. 10 Comparison of the -FN erase characteristics for ISSG and HTO top oxide.

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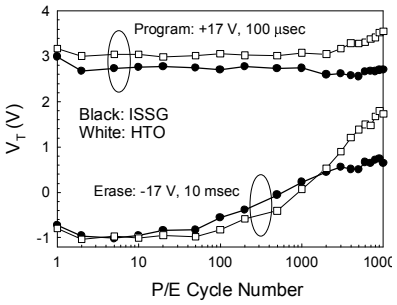


Fig. 11 Dumb-mode P/E cycling endurance (without adjusting the P/E conditions during endurance test). Both ISSG and HTO top oxide are compared.

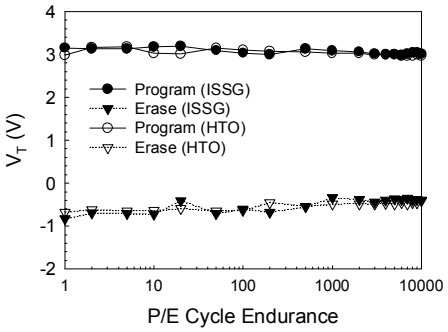


Fig. 12 P/E cycling endurance (with adjusted P/E conditions during endurance test). Both ISSG and HTO top oxide are compared.

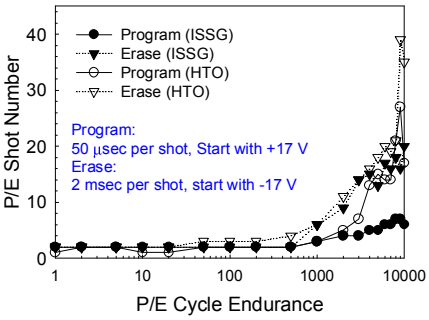


Fig. 13 The required P/E shot number during adjusted P/E tests in Fig. 12. Both ISSG and HTO top oxide are compared.

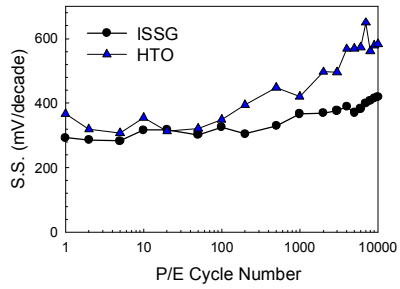


Fig. 14 Subthreshold slope degradation during 10K P/E cycling tests. Both ISSG and HTO top oxide are compared.

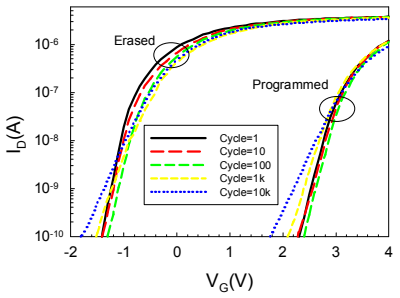


Fig. 15 *IV* characteristics of ISSG top oxide device during 10K P/E cycling endurance testing.

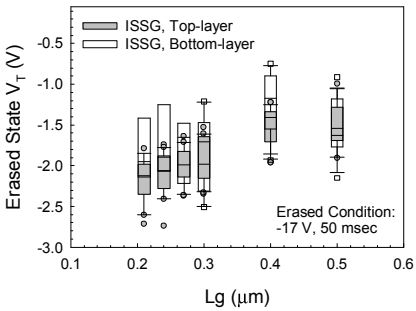


Fig. 16 Short-channel effect comparison of the top and bottom layer TFT NAND devices. A total of 28 identical devices are measured. The devices are in erase saturation state.

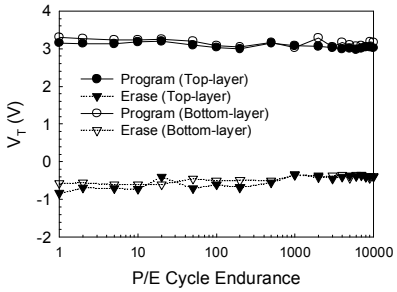


Fig. 17 Adjusted P/E cycling endurance (with adjusted P/E conditions during endurance test). Both bottom and top layers are compared. ISSG top oxide is used.

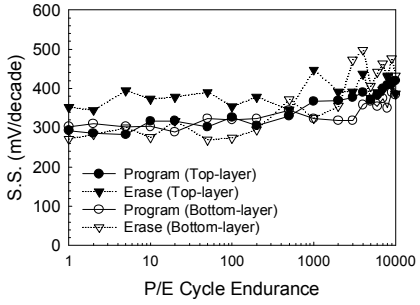


Fig. 18 Subthreshold slope degradation during 10K P/E cycling tests. Both bottom and top layers are compared. ISSG top oxide is used.

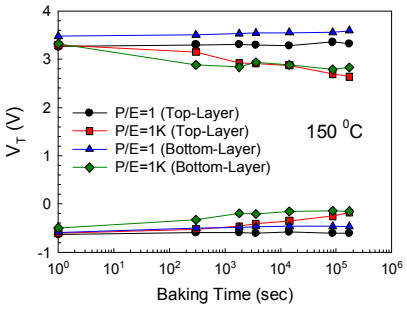
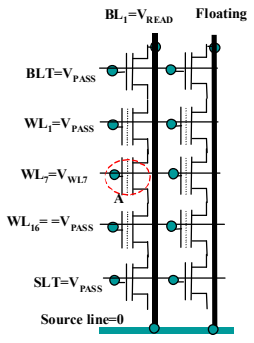


Fig. 19 Retention characteristics. Programmed and erased state with various cycle endurance are compared.



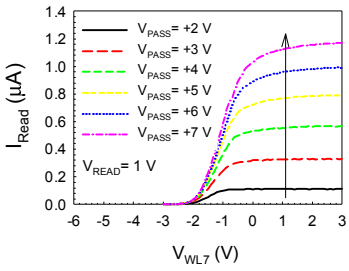
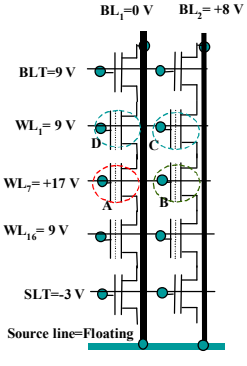


Fig. 20 Read current of a 16 WL's TFT NAND array. The devices are in erased state. For V_{PASS}=+7 V, read current can approach 1 µA, sufficient for NAND Flash design.



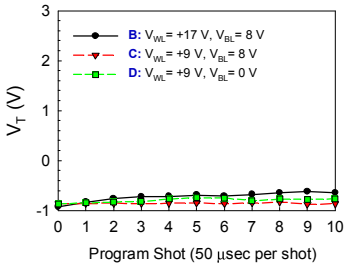


Fig. 21 Program disturb of a TFT NAND array. Cells C and D are under medium field gate disturb, while cell B can be program-inhibited by raising the channel potential.

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Appendix ARREGHINI01

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Appendix ARREGHINI02

Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells

Antonio Arreghini, Francesco Driussi, Elisa Vianello, David Esseni, *Senior Member, IEEE*, Michiel J. van Duuren, Dusan S. Golubović, Nader Akil, and Rob van Schaijk

***Abstract*—We present a broad set of experiments on silicon nitride-based memories aimed at the investigation of the vertical position of the charge trapped in the nitride layer of silicon-oxide–nitride–oxide-semiconductor (SONOS) memories during program and erase in the tunneling regime. The results obtained for SONOS devices with conventional oxide–nitride–oxide and oxide–nitride–oxide–nitride–oxide gate stacks, as well as with high-κ top dielectric, have been validated by comparing different characterization techniques. It has been shown that, for SONOS cells, the charge centroid is located in the center of the silicon nitride layer, and its position is quite insensitive to the program or erase conditions and to the gate-stack composition.**

***Index Terms*—Carrier separation, charge centroid, silicon nitride, silicon-oxide–nitride–oxide-semiconductor (SONOS).**

I. Introduction

FURTHER scaling of modern floating-gate (FG) memory cells is hampered by the charge loss due to the stress-induced leakage current (SILC) in cycled cells [1]. In particular, SILC prevents the tunnel-oxide thinning below 8 nm [2] and, moreover, raises statistical-reliability issues for the nowadays very large cell arrays [3], [4]. Furthermore, a strong lateral scaling of nonvolatile-memory (NVM) arrays leads to reliability issues related to the parasitic capacitive coupling between adjacent FG cells [5].

Nitride-based memories, like the silicon-oxide–nitride–oxide-semiconductor (SONOS) devices, are good candidates to replace FG cells in the Flash memory chips of the future generations for high-density and embedded applications, owing to the SILC immunity achieved with localized-charge trapping, that guarantee very good endurance characteristics [6], [7]. Moreover, the relatively low program/erase (P/E) voltages and the excellent compatibility with the standard CMOS process of SONOS memories make them suitable for embedded applications [8]. Finally, the absence of erratic tail bits reduces the statistical-reliability issues in very large memory arrays, and the limited capacitive coupling between adjacent SONOS cells is beneficial for the reliability issues related to the scaling of the spacing between cells.

However, the data retention of SONOS cells programmed and erased by direct tunneling is still a critical issue because of the thin tunnel oxide ($\approx$2.5 nm) needed for the tunneling of substrate holes under negative gate voltages [9]. Therefore, in order to optimize the retention characteristics of SONOS memories, an accurate analysis of the trapping properties of the silicon nitride layer that is responsible for the charge storage in the cell is required. In this respect, the knowledge of the location of the charge trapped in the nitride and the type of carriers injected during the P/E operations are not yet complete [10]–[13] despite the importance of these pieces of information in order to understand the charge-loss rates from the nitride toward the gate and substrate and, therefore, to model accurately the retention characteristics.

In this framework, this paper presents an extensive analysis of the vertical position of the charge trapped in the gate dielectric for a wide set of SONOS devices with different oxide–nitride–oxide (ONO) stacks, including samples with nonconventional gate stacks and with a high-κ top dielectric. To accomplish this, we have extensively applied the experimental procedure developed in [14] to extract the trapped-charge centroid, thus fully validating it over several gate stacks for memory cells. Compared with other methods used to probe the charge trapped in the gate stack, our technique is based on the simplest MOSFET electrostatics, and no constraints are imposed to the P/E conditions during its application. In particular, whereas the low-frequency charge pumping (LFCP) [15] can extract the trap profile, but only within a few nanometers inside the ONO stack, our procedure can reach the deeper locations inside the gate stack, thus considering the effect of the whole trapped charge. However, the centroid alone does not provide the detailed knowledge of the charge profile inside the nitride, but it determines the effectiveness of a given distribution of charges in generating a corresponding V_T shift. Therefore, our technique can be seen as complementary to other methods used to probe the trapped-charge profile (e.g., the LFCP), overcoming some of their limitations in terms of accuracy and applicability.

A broad range of P/E conditions, i.e., different programming/erasing gate voltages (V_G), have been tested for each device, and the experimental results for the charge-centroid location have been confirmed by the comparison with those derived with the LFCP method, thus demonstrating the advantages and

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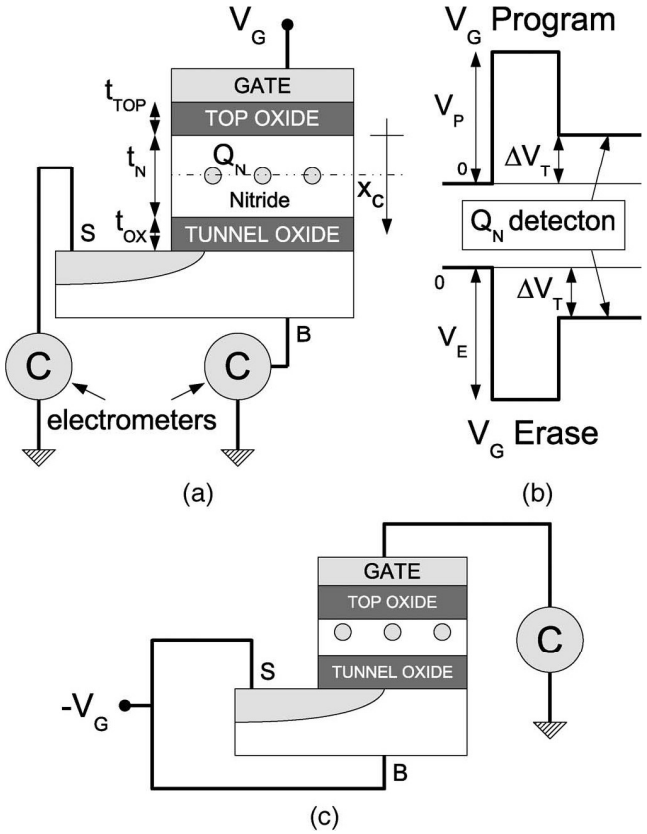


Fig. 1. (a) Measurement setup for carrier separation and charge-centroid extraction. Q_N is the trapped charge, x_C is the centroid position, and $t_{\rm TOP}$, t_N, and $t_{\rm OX}$ are the thicknesses of the top oxide, nitride layer, and tunnel oxide, respectively. (b) Waveforms for the P/E pulses showing the three-level shape used to obtain a null contribution to the overall current integral of the displacement charge in the semiconductor. (c) Measurement setup for the charge-centroid extraction. By measuring Q_N at the gate while pulsing with a reversed waveform with respect to (b) at the source and bulk terminals, no compensation of possible leakage currents is needed.

limitations of each technique. In a limited number of cases, pMOS SONOS devices were fabricated, and carrier-separation experiments were performed to identify the type of carriers involved in the program/erase operation.

II. Experimental Setup and Charge-Centroid-Extraction Procedure

Fig. 1(a) shows the vertical structure of a conventional SONOS device. The charge that is responsible for the threshold-voltage shift (ΔV_T) is supposed to be stored in the silicon nitride layer, which is sandwiched between the tunnel and the top oxides (this assumption will be relaxed later). If we let x_C denote the centroid of the trapped charge measured from the top-oxide/nitride interface [see Fig. 1(a)], then the threshold-voltage shift induced in the cell by the charge Q_N (uniformly injected over the device area A) can be calculated as [14], [16]–[18]

$$\Delta V_T = -\frac{Q_N}{A}\cdot\frac{t_{\rm TOP}}{\epsilon_{\rm OX}} - \frac{1}{\epsilon_N}\int_0^{t_N} x\cdot q(x)dx = -\frac{Q_N}{A}\left(\frac{t_{\rm TOP}}{\epsilon_{\rm OX}}+\frac{x_C}{\epsilon_N}\right) \quad (1)$$

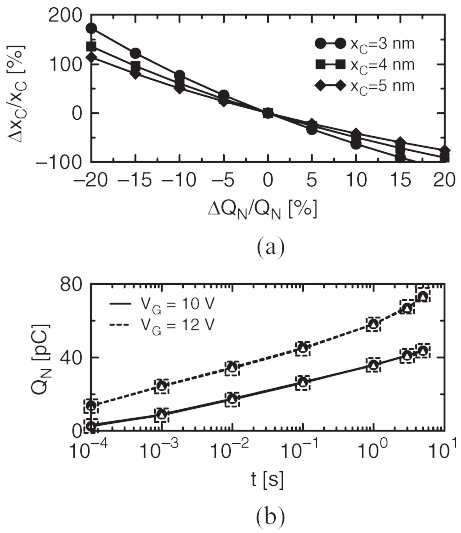


Fig. 2. (a) Sensitivity of the charge centroid on the possible error in the trapped-charge detection. Note that small errors in the measured Q_N lead to large errors in the estimation of x_C. (b) Measured Q_N as a function of the programming pulsewidth for three different devices (circles, squares, and triangles). Note the good repeatability of the measurements obtained with our setup.

where $q(x)$ is the charge density along the nitride depth x, $\epsilon_{\rm OX}$ and ϵ_N are the permittivity of SiO_2 and Si_3N_4, respectively, and $t_{\rm TOP}$ and t_N are the top oxide and nitride thicknesses, respectively. Therefore, if ΔV_T and Q_N are known, the centroid of the charge trapped in the nitride can be univocally determined as

$$x_C = -\epsilon_N\left(\frac{\Delta V_T\cdot A}{Q_N}+\frac{t_{\rm TOP}}{\epsilon_{\rm OX}}\right). \quad (2)$$

Hence, in order to determine x_C by using (2), we have developed a well-controlled experimental setup to directly measure both the programming (erasing) charge Q_N and the corresponding threshold-voltage shift $\Delta V_T = (V_{T\,\rm final} - V_{T\,\rm initial})$ produced by the program (erase) performed in tunneling conditions. For the sake of clarity, it is worth noting that we define program (erase) as the application of gate pulses with positive (negative) V_G, which increase (decrease) the threshold voltage V_T, regardless of the type of the device under test (nMOS or pMOS). In the experimental setup shown in Fig. 1(a), we connected two accurately zeroed electrometers at the source/drain and bulk terminals of the SONOS device. In this way, when an nMOS SONOS cell undergoes a P/E cycle, we can separately measure the contributions to the programming (erasing) charge Q_N of both the electrons detected at source/drain and the holes collected at the bulk, thus performing a carrier-separation experiment.

As for the x_C extraction, an analysis of (2) shows that, while the errors in the detection of ΔV_T are not so critical, x_C is largely sensitive to possible errors on the measured Q_N. With this regard, Fig. 2(a) shows, for a fixed actual centroid position (different symbols), the relative error in the extracted x_C induced by an error in the detection of the charge; we clearly see that even a relatively small error in Q_N can lead to an incorrect estimation of the charge centroid. Therefore, in order to minimize the charge errors, the leakage current through

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the source-to-bulk junction has been compensated for, first, by measuring its spurious contribution to the charge during a pulse train with a reduced V_G value that prevents the injection into the gate stack and, then, by subtracting the obtained value from the Q_N measured during the P/E pulse with large V_G.

Alternatively, because the capacitor is a two-terminal device, the injected charge can be measured also by reversing the roles of the device contacts, hence, through an electrometer connected to the gate, while pulsing on the bulk and source terminals [Fig. 1(c); source and bulk are short-circuited]. In this configuration, a $-V_G$ value is applied during the pulse. In such a way, although carrier separation is not possible, no leakage compensation is needed on the gate terminal (where the charge is measured). Therefore, for the purpose of extracting the charge centroid, the measurement of Q_N by means of the experimental setup in Fig. 1(c) is highly preferable.

Moreover, in order to avoid the spurious contribution to Q_N due to a net, which is the nonnull-time integral of the displacement current, we forced the same $(V_G - V_T)$, hence the same electric field $E_{\rm OX}$ at the Si/SiO_2 interface, which is before and after the program/erase pulse. This was obtained by applying to the gate three-level pulses, as shown in Fig. 1(b), where the final base level of the pulse is displaced by ΔV_T with respect to the initial base level. This approach requires the knowledge in advance of the ΔV_T induced by each program (erase) pulse, and therefore, the P/E characteristics have been preliminarily measured. Afterwards, the measured ΔV_T's have been used to set the pulse shape and measure the Q_N, as shown in Fig. 1(c). Because the programming and the erasing are performed by applying a sequence of several P/E pulses, for each measurement, we monitored both the cumulative charge Q_N involved in the whole P/E sequence and the partial charge q_N injected during each individual P/E pulse.

As shown in Fig. 2(b), by using this measurement scheme on a given SONOS device, we could achieve a very good reproducibility of the measured Q_N and ΔV_T among different runs and dies, provided that all the P/E characteristics start from the same initial V_T value. An *ad hoc* reset procedure of the device consisting of several mild P/E cycles allowed us to enforce always the same starting V_T value within tens of millivolts. The possible degradation produced by the P/E cycling has been monitored by means of charge-pumping measurements, and it was found to be negligible in the range of relatively few P/E cycles used for our characterization experiments.

III. Device Description

The devices used in this paper are nMOS and pMOS SONOS capacitors with a surrounding source diffusion and a gate area of $A = 3100\ \mu\text{m}^2$. For both nMOS and pMOS devices, n+ and p+ polygates are available, and the substrate doping is approximately $10^{17}\ \text{cm}^{-3}$. The vertical dimensions of the ONO gate stack have been extracted by means of transmission electron microscopy (TEM), ellipsometry, and capacitance–voltage (*C–V*) measurements. The nominal thickness of the thermal tunnel oxide is $t_{\rm OX} = 2.2$ nm for all SONOS cells, whereas two thicknesses are available for both the dichlorosilane Si_3N_4 layer ($t_N = 3.3$ and 5.7 nm, respectively) and the high-temperature-oxide (HTO) top oxide [$t_{\rm TOP} = 8.9$ and 5.5 nm, respectively; Fig. 3, device A].

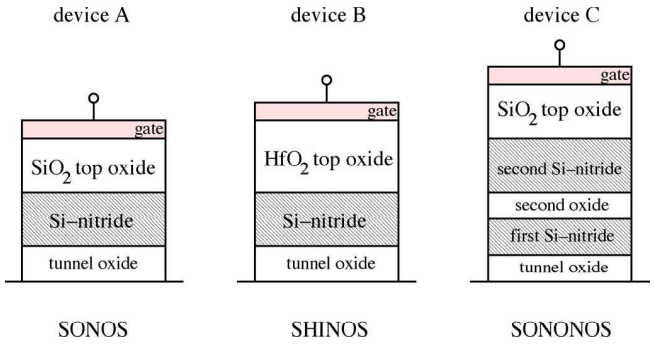


Fig. 3. Gate-stack composition of the devices used in this paper.

A gate stack featuring a 11.8-nm-thick HfO_2 layer as top dielectric, a 5.7-nm-thick Si nitride, and a 2.2-nm-thick tunnel oxide was also available (hereafter denoted as SHINOS; Fig. 3, device B).

Finally, the nonconventional gate-stack structure shown in Fig. 3 (device C, hereafter denoted as SONONOS) has been also used for the experiments related to the charge-centroid determination. This device is composed of two nitride layers sandwiched between the tunnel and top oxides and separated by an additional SiO_2 layer (second oxide) formed by the reoxidation of part of the first silicon nitride layer (the one on top of the tunnel oxide). In this device, the thicknesses extracted by means of TEM and *C–V* measurements are 1.3, 2.8, 1.5, 5.0, and 7.2 nm for the tunnel oxide, the first nitride, the second oxide, the second nitride, and the top oxide, respectively (Fig. 3, device C). All the measured devices are free of the passivation issue discussed in [19].

IV. Carrier-Separation Experiments

Carrier-separation experiments are suitable to investigate quantitatively the contribution of electrons and holes during the program and erase operations. Previous experiments showed that, during program, the charge Q_N is almost entirely due to electrons [11], [13], [14], [17], whereas during erase, the contribution of holes can be significant [9], [14]. In this regard, we first successfully verified with the experimental setup in Fig. 1(a) that Q_N is due to electrons during program [14]. In analogy with the case of quantum-yield experiments, the hole recombination with electrons in the inversion layer is a very unlikely process [20], [21], and, thus, we conclude in agreement with Bachhofer *et al.* [11], Wang and White [13], and Libsch and White [17] that the hole detrapping is negligible during this phase.

In the case of erasing, because our nMOS SONOS test structures are rather large ($20 \times 155\ \mu$m), the electrons that are possibly detrapped from the nitride must diffuse for several micrometers in the substrate before they can reach the source contact; thus, the recombination with substrate holes can take place, and the carrier-separation technique may underestimate the contribution to the erase of the detrapped electrons. The experiments on nMOS devices revealed that the measured Q_N during erase is mainly due to holes [14]; hence, either

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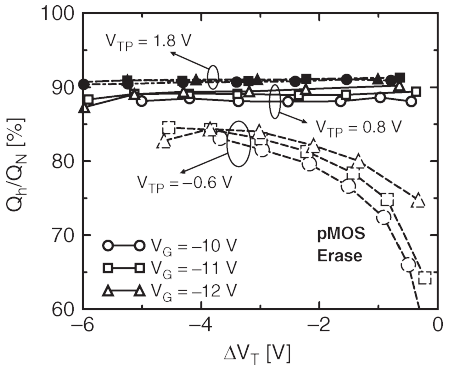


Fig. 4. Fraction of the charge due to holes measured during the pMOS SONOS erase as a function of ΔV_T for different values of V_G and of the initial threshold voltage $V_{\rm TP}$. Note the decreasing contribution of holes for decreasing $V_{\rm TP}$. $Q_h, Q_e > 0$ during erase.

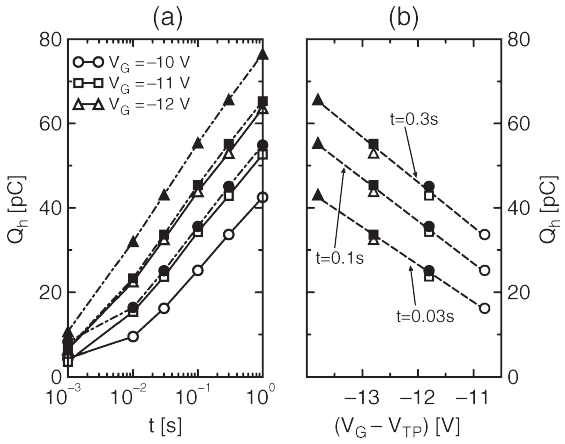


Fig. 5. Hole contribution to pMOS SONOS erase as a function of the (a) erasing time and (b) $(V_G - V_T)$. Open symbols for $V_{\rm TP} = 0.8$ V and filled symbols for $V_{\rm TP} = 1.8$ V.

the electron detrapping is very small or it is masked by the recombination in the p-substrate.

The accuracy of the carrier-separation experiments for determining the contribution of electrons and holes (Q_e and Q_h, respectively) to the erase is significantly improved if we use pMOS SONOS capacitors. In fact, under negative V_G, the holes are supplied by the inversion layer and are measured at the source, whereas the detrapped electrons go through the very thin hole inversion layer and, then, are collected at the bulk terminal of the n-type substrate [20], [21] so that the probability of recombination with holes is drastically reduced with respect to the experiment of the erase in nMOS SONOS.

Fig. 4 shows the carrier-separation measurements performed during the erase transient in pMOS SONOS devices, which, according to our definition, correspond to a reduction of the threshold voltage, i.e., to negative ΔV_T values. We see how the hole contribution Q_h to Q_N depends on the initial programmed state $V_{\rm TP}$. In particular, for $V_{\rm TP} = -0.6$ V, we observe a reduced contribution of holes, hence a large contribution of electrons detrapped from the nitride layer and a strong ΔV_T dependence of the (Q_h/Q_N) ratio. At higher $V_{\rm TP}$, the relative contribution of holes remains constant versus ΔV_T, regardless of the erasing gate voltage V_G. Moreover, if we replot Q_h as in Fig. 5, we see how the hole component directly depends on the

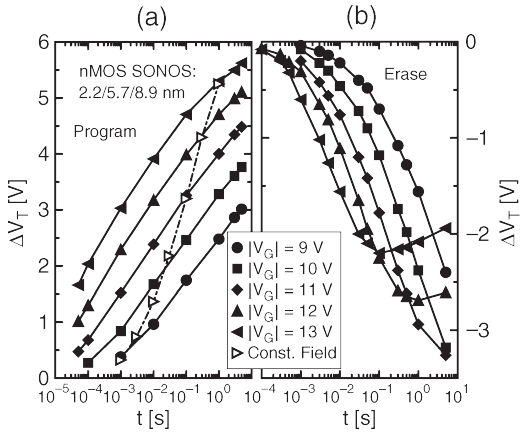


Fig. 6. (a) Program and (b) erase characteristics of an nMOS SONOS capacitor at constant gate voltage. Open triangles correspond to programming at constant tunnel-oxide field, which is obtained by compensating at each program pulse the ΔV_T produced by the previous pulse.

initial gate overdrive voltage $(V_G - V_{\rm TP})$. This latter result can be justified by considering that both the tunneling rate and the hole-inversion-layer density depend on the $(V_G - V_{\rm TP})$ value.

V. Position of the Charge Centroid

After the identification of the different roles played by electrons and holes during P/E, we focused our attention on the extraction of the charge centroid x_C by using (2). In particular, to study the x_C dependence on the P/E conditions and the device structure, the experimental procedure described in Section II has been used to measure Q_N and the induced ΔV_T for several V_G values and for devices featuring different ONO gate stacks.

A. Experimental Results for SONOS and SHINOS Devices

Fig. 6 shows the P/E characteristics as functions of the total program (erase) time t of the nMOS SONOS with $t_{\rm OX} = 2.2$ nm, $t_N = 5.7$ nm, and $t_{\rm TOP} = 8.9$ nm (2.2/5.7/8.9). The ΔV_T's have been evaluated by measuring the shifts of the *C–V* curve after each P/E pulse. Then, the capacitor was reset to the initial state (by mild P/E cycling), and the ΔV_T data have been used to set the shape of the pulses [see Fig. 1(b)] during which we directly measured the injected Q_N with the experimental setup in Fig. 1(c). Finally, in Fig. 7(a), we have calculated the x_C of the cumulative charge Q_N. Each point of the curve is the centroid of the total charge Q_N injected from the beginning of the P/E characteristic to the time corresponding the ΔV_T value reported in the x-axis in Fig. 7(a).

We observe that the centroids for program and erase are very consistent with each other; at the beginning of the program (erase) phase, x_C is located near the middle of the nitride layer, which is in agreement with the results for HTO top oxides reported in [22]. Then, x_C slowly moves toward the top oxide. Moreover, the data in Fig. 7(a) do not show any dependence on the applied gate voltage V_G. In this respect, in order to further investigate a possible bias dependence of x_C, we have also performed measurements by keeping $E_{\rm OX}$

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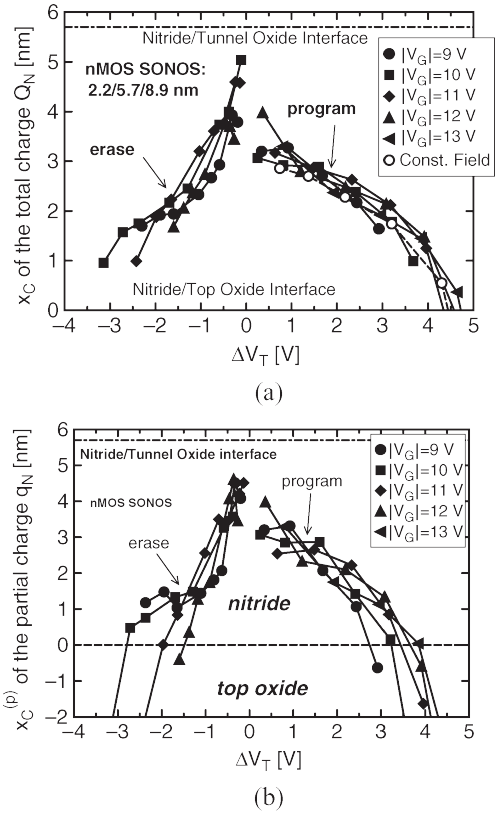


Fig. 7. (a) Centroid of the cumulative charge trapped in the nitride of the nMOS SONOS capacitor (2.2/5.7/8.9-nm ONO stack) extracted for the program and erase pulses at different V_G's. Open circles correspond to the programming at constant electric field across the tunnel oxide (V_G is adjusted after each subsequent pulse). (b) Centroid of the partial charge injected into the nitride during each pulse of the programming/erasing of the nMOS SONOS (2.2/5.7/8.9-nm ONO stack). Note how during the last program/erase pulses (large $|\Delta V_T|$) the centroid of the partial charge is located in the top oxide, indicating that part of the injected charge has been lost through the gate.

at the Si/SiO_2 interface approximately constant during program [Figs. 6(a) and 7(a); open symbols] by increasing V_G after each pulse for an amount equal to the corresponding ΔV_T. This, of course, leads to a faster programming [Fig. 6(a); open symbols], but x_C still agrees well with the data obtained at constant V_G [Fig. 7(a)]. Therefore, we can conclude that there is no dependence of x_C on the injection conditions, at least in the bias range explored in this paper.

For $\Delta V_T > 4$ V, the x_C values move toward the top oxide and eventually become negative. The negative x_C, however, is most likely an artifact due to an electron leakage through the top oxide at the largest programming times, hence largest ΔV_T's. In fact, when the cell is strongly programmed and the nitride is almost completely charged, the electric field across the top oxide is maximum, and the electrons injected in the nitride can tunnel out of the storage layer during the last part of the programming phase. This charge leakage offsets our estimate of Q_N, which hence appears less effective with respect to the measured threshold-voltage shift and results in a smaller value of x_C [see (2)]. In order to more precisely assess the ΔV_T range where the determination of x_C is reliable, in Fig. 7(b), we calculated the centroid $x_C^{(p)}$ of the partial charge packet q_N injected during the last pulse of the P/E sequence used to reach

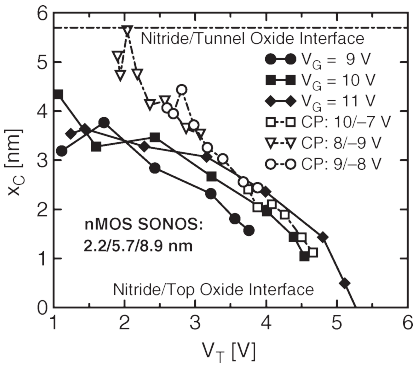


Fig. 8. Centroid x_C for the nMOS SONOS capacitor (2.2/5.7/8.9-nm ONO stack) extracted during programming. The data obtained with the (filled symbols) direct-measurement technique summarized by (2) are in good agreement with those provided by the (open symbols) LFCP experiments.

a given ΔV_T value, hence injected between two adjacent points of the curves in Fig. 7(a). The centroid $x_C^{(p)}$ is calculated by inserting in (2) the charge q_N and the threshold-voltage shift corresponding to the single (individual) P/E pulse. It is worth to note how, for $\Delta V_T > 3$ V, $x_C^{(p)}$ is negative, thus indicating that we are measuring a charge packet q_N that is larger than the one needed to justify the partial threshold-voltage shift obtained during the last P/E pulse. Hence, part of the charge q_N must have been lost through the gate. For $\Delta V_T < 3$ V, on the other hand, the $x_C^{(p)}$ of each partial charge packet is located well inside the nitride, thus indicating that we are not losing charge through the gate and validating the x_C values extracted for the cumulative charge Q_N in this range of ΔV_T values.

Moreover, the analysis of the $x_C^{(p)}$ values shows that the centroid position is independent of the starting V_T, because each point in Fig. 7(b) corresponds to the charge centroid obtained, starting from a different V_T level.

During erase, $x_C^{(p)}$ becomes negative when the electron injection from the gate takes place. In this situation, a steady-state current flows from the substrate to the gate, thus yielding a saturation of the erase characteristics that limit the observable ΔV_T range [Fig. 6(b)]. The charge measured in this condition is largely exceeding the charge responsible for the threshold-voltage shift, and therefore, the extracted x_C becomes unreliable while approaching this region. On the basis of such observations, we estimated that, for the measured device, the x_C values are reliable for $-2 < \Delta V_T < 3$ V and, in this ΔV_T range, the charge centroid stays close to the center of the nitride layer and it only slightly moves toward the top oxide for both program and erase [14], [18], [22].

As stated in Section IV, the carrier-separation experiments showed that, in our nMOS SONOS capacitors, the measured Q_N during program is essentially due to electrons whereas, during erase, it is mainly due to holes. Thus, the net result of a complete P/E cycle is a recombination charge, and we can also use an LFCP technique to detect such a recombined charge Q_N [15]. Fig. 8 shows the x_C values calculated by using Q_N detected by means of LFCP with different base and top pulse levels. We see that the results agree well with the x_C obtained with the direct measure of Q_N on the same device, except at small ΔV_T, where the LFCP method underestimates Q_N, as

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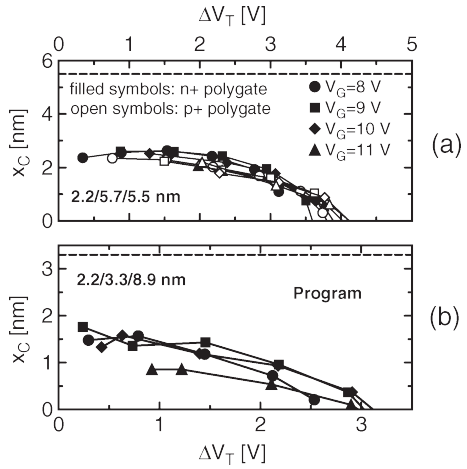


Fig. 9. Centroid x_C extracted during the programming of SONOS devices, featuring two different ONO stacks: (a) 2.2/5.7/5.5 and (b) 2.2/3.3/8.9. Filled and open symbols are the data for SONOS with n+ polygate and p+ polygate, respectively. The dashed line indicates the tunnel-oxide/silicon-nitride interface.

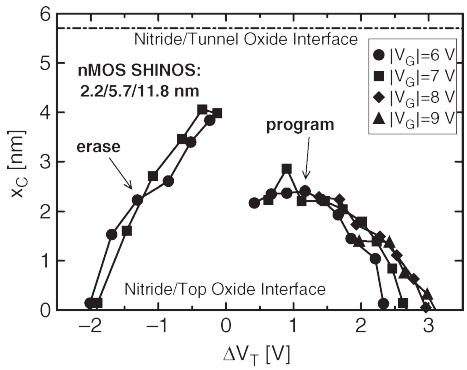


Fig. 10. Charge centroid extracted during the program and the erase at different V_G's for the nMOS SHINOS cells, featuring a HfO_2 top oxide of 11.8 nm.

shown in [14], thus resulting in a deviation of x_C toward the tunnel oxide [see (2)].

Fig. 9 shows the centroid x_C extracted during the programming of SONOS capacitors with different top oxide [$t_{\mathrm{TOP}} = 5.5$ nm; (a)] and silicon nitride thicknesses [$t_N = 3.3$ nm; (b)], whereas all other stack dimensions are the same, as shown in Fig. 7. Also, in this case, we find that x_C is located near the middle of the nitride (slowly shifting toward the top oxide as programming continues) and no gate bias dependence is observed. Moreover, there is no significant dependence of the measured x_C on the polygate type (open and filled symbols). Fig. 10 shows the x_C values extracted from the SHINOS cells featuring the HfO_2 top dielectric (Fig. 3, device B). Also, in this case, x_C is located inside the nitride, no dependence on V_G is observed, and the data for program and erase are consistent with each other. The results obtained for the pMOS SONOS devices are very similar [14].

As a summary, Fig. 11 shows the centroid position normalized to the nitride thickness t_N for all the measured SONOS devices. We see how, for moderate ΔV_T values, x_C is always located near the center of the nitride irrespective of the gate-stack composition and the substrate doping type.

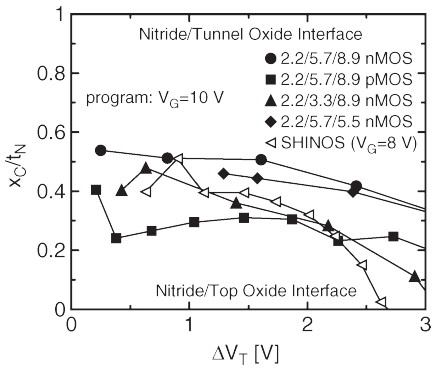


Fig. 11. Normalized position along the nitride layer of the charge centroid extracted from different devices. Note that the relative position of x_C is near the center of nitride for all the samples, as long as ΔV_T is not very large.

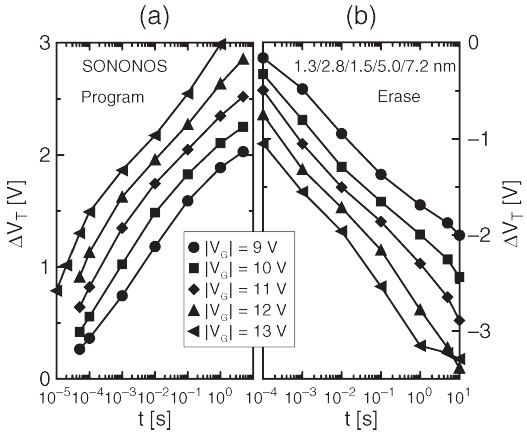


Fig. 12. (a) Program and (b) erase characteristics of the SONONOS cell for different V_G values.

B. Experimental Results for SONONOS Devices

We applied the charge-centroid-extraction procedure also to the SONONOS devices featuring the gate-stack structure shown in Fig. 3 (device C). Fig. 12 shows the P/E characteristics of this SONONOS capacitor, which show a faster programming and erasing compared with SONOS cells (see Fig. 6). In order to perform the x_C extraction accurately, particular care has been taken in the ΔV_T measurement. In fact, the application of even small V_G values produces appreciable threshold-voltage shifts, due to the very thin tunnel oxide (1.3 nm). This results in a considerable hysteresis in the *C–V* characteristics obtained, spanning a relatively large V_G range [Fig. 13(a)]. In our capacitors, the ΔV_T detection is performed by measuring the shift of the *C–V* characteristic, and this can be accomplished by detecting the capacitance at different points, hence V_G values. However, in the SONONOS device, we had to choose an appropriate evaluation point for the ΔV_T [Fig. 13(a), point B] in order to avoid the application of too large $(V_G - V_T)$ values that induce a spurious programming during the ΔV_T extraction, as in the case of the choice of the point A in the *C–V* curve in Fig. 13(a). In the latter case, the gate disturbance leads to a parasitic threshold-voltage shift that depends on the measurement time [Fig. 13(b), in squares]. The experimental results presented in the following have been extracted by detecting the ΔV_T at

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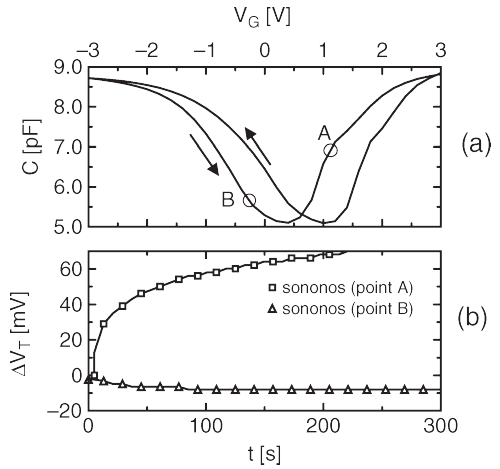


Fig. 13. (a) *C–V* curves of the SONONOS, showing a large hysteresis during the measurement. The arrows indicate the direction of the V_G sweep. (b) The ΔV_T value is measured as a shift of the *C–V* curve. The selection of the right evaluation point in the *C–V* curve avoids a spurious V_T shift induced by a gate disturb during the detection of the ΔV_T.

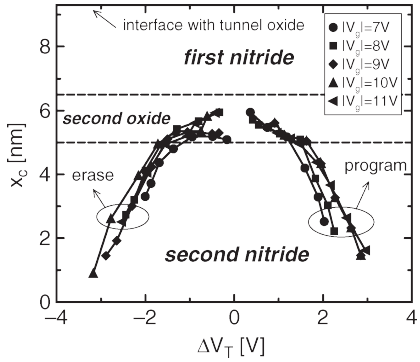


Fig. 14. Charge centroid extracted from the SONONOS devices. Initially, the charge is trapped near the interface between the first nitride and the second SiO_2 layer, and then, it fills the traps in the center of the second nitride. See Fig. 3 (device C) for the gate-stack definition.

(triangles) point B, where the gate disturbance is essentially negligible.

On the other hand, it is worth noting that, in the SONOS samples, the discussed issue is not present due to the fact that the *C–V* curve is not hysteretic because of the thicker tunnel oxide. In this case, the ΔV_T detection can be done at any point of the *C–V* curve, because the application of the V_G bias that is necessary for the capacitance measurement does not also produce spurious threshold-voltage shifts if this V_G value is applied to the device for long times.

The x_C values extracted from the SONONOS cells are shown in Fig. 14. Also, in this case, there is no dependence on the applied P/E conditions, and the data for program and erase are consistent. However, unlike standard SONOS devices, SONONOS structures exhibit a centroid x_C that is initially located very close to the second oxide layer (Fig. 3, device C). This is probably due to the fact that the second oxide has been formed by the reoxidation of part of the first nitride layer. This oxide-fabrication method is known to produce a large number of traps at the interface between the first silicon nitride layer and the second oxide layer [22]–[24]. The density of these interface traps can be larger than the concentration in the bulk of the nitride layer, and the results in Fig. 14 are consistent with the assumption that the carriers are mainly trapped at the Si_3N_4/SiO_2 interface at the beginning of the program/erase operation, namely, for small $|\Delta V_T|$ values. Because in this case, x_C is located in the SiO_2 layer that has a different permittivity $\epsilon_{\rm OX}$ with respect to nitride, for the evaluation of the x_C values, (2) has been modified as follows:

$$x_C = -\epsilon_{\rm OX}\left(\frac{\Delta V_T A}{Q_N} + \frac{t_N}{\epsilon_N}\right) + t_N - t_{\rm TOP}. \qquad (3)$$

By increasing the program (erase) level, electrons (holes) start filling the bulk traps located in the second nitride film, and x_C moves to the middle of the nitride thickness as in the case of SONOS structures. It seems, however, that no significant amount of charge is trapped in the first nitride layer, although a comparable concentration of free traps should be available with respect to the second nitride layer.

These results also indicate that our experimental technique is indeed sensitive; in fact, it can detect changes of the x_C value due to different trapping properties in the gate stack.

VI. Conclusion

We have extensively used carrier-separation experiments with direct measurement of the charge injected during the program and erase operations of SONOS memory cells to study the type of carrier that is mainly involved in each operation as well as the location of the trapped charge Q_N. Preliminary experiments showed that, whereas Q_N is entirely due to electrons during program, during erase, there is a significant contribution of holes, which follows a $(V_G - V_{\rm TP})$ dependence.

Concerning the extraction of the charge centroid, a wide set of experiments in several P/E conditions on SONOS cells with different gate-stack structures has consistently shown that the centroid of the cumulative charge (x_C) is always located close to the center of the trapping layer and it slowly shifts toward the top oxide irrespective of the applied P/E voltages. Moreover, the x_C values do not significantly depend on the top oxide and nitride thicknesses, the composition of the top dielectric, or the substrate and gate doping type.

The centroid results for the SONONOS gate stack instead show that the carriers are initially trapped near the intermediate oxide layer likely because the reoxidation of the first nitride layer has generated a large number of traps at the Si_3N_4/SiO_2 interface [22]–[24]. For larger P/E levels, the carriers start filling the bulk traps of the second Si_3N_4 layer, so that the centroid moves toward the middle of the second nitride layer, which is consistent with the results obtained for SONOS devices. Also, for these devices, the behavior of x_C is essentially independent of the P/E conditions.

This large set of experimental data demonstrates the sensitivity of the characterization procedure proposed in this paper, which is thus useful to study the trapping properties of different gate-stack structures and support the design of the nitride-based NVM cells. The data also represent a valid reference for the calibration of program/erase and retention models of Si nitride-based NVM [25].

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Appendix ZHOU01

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Appendix ZHOU02

VDNROM: A Novel Four-Bits-Per-Cell Vertical Channel Dual-Nitride-Trapping-Layer ROM for High Density Flash Memory Applications

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Abstract - A novel vertical channel nonvolatile memory cell with oxide–nitride–oxide–nitride–oxide (ONONO, dual nitride trapping layers) dielectrics stack is proposed and experimentally demonstrated for the first time. Compared with the conventional planar NROM cell, since the cell area of the proposed vertical structure is independent of the gate length, the VDNROM structure can relax the limitation of the gate length scaling, and can have high capability of cell area shrinking. The fabrication process of this VDNROM device is basically compatible with planar CMOS technology. The VDNROM cell can be programmed and erased by the hot carrier injection to the localized trapping dual-nitride-layers, so it can achieve a four physical bits storage capability each cell. The reliability behaviors including the cycling endurance and the bake retention at 150°C have also been investigated and show the acceptable characteristics. The experiment results verify the VDNROM cell as a good candidate for high-density applications.

I. INTRODUCTION

Recently, SONOS flash memory has been paid more attention and considered as a promising technology bridging the gap between the floating-gate flash and the next generation memories because of its intrinsic better endurance, good scalability, simpler fabrication process and its perfect compatibility with conventional CMOS technology for embedded applications [1-3]. However, conventional SONOS cell is only one-bit-per-cell storage, and the data retention is still a big problem due to the direct tunneling of stored charge through the ultra thin tunneling oxide.

The NROM concept [4-5] was proposed to solve the drawbacks of SONOS by using channel hot electrons injection (CHEI) for programming and band-to-band tunneling induced hot holes injection (BBTIHH) for erasing. This device can allow thicker tunneling oxide, while still maintaining high efficient Program /Erase (P/E) operations. Moreover, the P/E mechanisms lead to localized charge storage in the trapping nitride layer, so the NROM can store two distinct bits per cell. However, the further scaling of the cell area of the conventional planar NROM device for higher density is limited by the gate length scaling for two reasons. Firstly, the drain voltage can not be scaled below 3.2V for CHEI, and therefore the punch-through effect would become worse as the gate length scaling [6]. Secondly, since two bits are stored in physically distinct areas in the nitride layer, the lateral distributions of the charges have to be well separated to avoid any interference between the two bits [7].

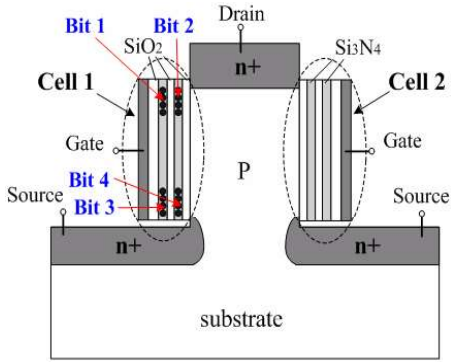


Fig. 1 Schematic cross sectional view of the proposed 4 bits/cell VDNROM flash memory.

In this work, as shown in Fig. 1, we proposed and demonstrated experimentally a novel vertical channel dual-nitride-trapping-layers ROM (VDNROM) structure nonvolatile memory device achieving four-bits-per-cell function for the first time. Compared with the conventional planar NROM cell, since the cell area of this vertical channel structure is independent of the gate length, the VDNROM structure can relax the limitation of the gate length scaling, and can have high capability to shrink the cell area. Moreover, the fabrication of this VDNROM device is basically compatible with planar

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CMOS technology. The experimental results demonstrate continued better scalability of the VDNROM cell for high-density applications.

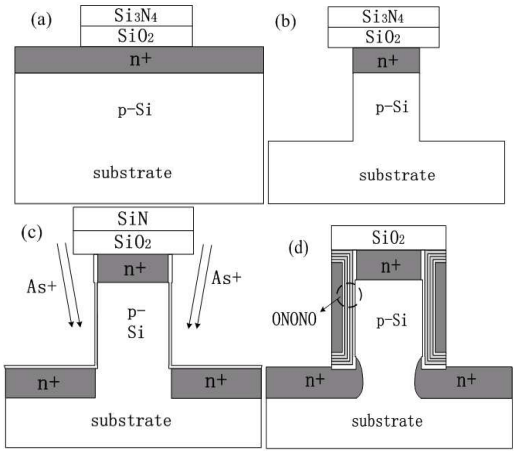


Fig. 2. The process flow of the proposed 4bits/cell VDNROM flash memory.

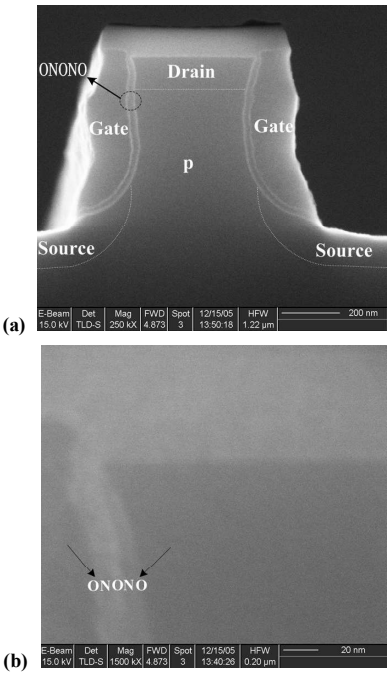


Fig. 3. The SEM images of the proposed 4bits/cell VDNROM flash memory cell (a) and the ONONO gate dielectric stack (b).

II. Device Structure and Fabrication

The schematic cross-sectional view of the proposed VDNROM flash memory cell with the oxide-nitride-oxide-nitride-oxide (ONONO) gate dielectric stack is illustrated in Fig. 1. The charges can be stored in the dual nitride trapping layers above the channel next to the n+/p junctions, so this VDNROM cell can achieve a four physical bits storage capability as shown in Fig.1. The tunneling oxide and the block oxide are thicker than 5 nm to avoid any direct tunneling of the charges, and the gate dielectric stack of the ONONO five layers (the tunneling oxide, the first trapping nitride layer, the inter-nitride oxide, the second trapping nitride layer, the block oxide) are 7/4/5/5/13 nm respectively.

Referring to Fig. 1, the process flow to realize such a 4bits/cell VDNROM device was shown in Fig. 2(a)-(b). After isolation, the channel boron doping and the drain arsenic doping were implemented. Two layers of oxide and nitride was deposited, patterned and etched to form the dual-layers hard masks as shown in Fig. 2(a). The silicon substrate was then etched by ICP (Inductive Coupled Plasma) to form the steep device mesa. Next, the device mesa was etched isotropically by RIE (Reactive Ion Etch) to form the recessed self-aligned poly gate structure shown in Fig. 2(b). To remove the surface damage on the sidewalls of the device mesa, thin sacrificial oxide was grown, which was followed by source arsenic implantation (4×10^{15}cm^{-2}, 100KeV), as shown in Fig. 2(c). After sacrificial oxide removed, 7.0-nm gate oxide was grown at 850ºC by dry thermal oxidation. Next, a dielectric stack of trapping-nitride /inter-oxide/trapping-nitride/block-oxide (NONO) with 4/5/5/13 nm respectively was deposited. Then, a polysilicon film was deposited, implanted and etched to form the self-aligned gate spacer. After the nitride hard mask removed, rapid thermal annealing was implemented to activate the dopants in the S/D region and poly gate, as shown in Fig. 2(d). Finally, the device was covered by low temperature deposited oxide (LTO), and followed by the rest of the process such as contact opening, metal defining and annealing. Fig. 3 (a) shows the SEM (scanning electron microscope) micrograph of the cross section of the fabricated VDNROM cell, and the SEM image of the ONONO gate dielectric stack is shown in Fig. 3 (b).

III. Operation Mechanism and Experiment Results

The VDNROM cell is programmed and erased by channel hot carriers injection. The four states (“00”, “01”, “10”, “11”) corresponding to bit-1 and bit-2 are shown in Fig. 4 (a)-(d), and the programming and erasing operations of the four states are shown in Table I. For example, applying 7.0 V on the drain electrode, 12.0 V on WL (the gate electrode) and grounding the source electrode for programming the state “00” in Fig. 4(a). The accelerated channel electrons are injected into the both two nitride layers of the ONONO gate dielectric stack near the drain junction, a self-aligned storage with the junction edge. As shown in Fig. 4(b) and Table I, the state of “01” is programmed by the hot electrons injection to the first trapping nitride layer with lower drain voltage 5.0 V (compared with the programming of the state of “00”), 6.0 V on WL (the

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gate electrode) and grounding the source electrode. The state of "10" shown in Fig. 4(c) is realized by two steps. As shown in Table I, the first step is the hot electrons injection to the dual trapping nitride layers with Vg=12.0 V, Vd=7.0V and Vs=0V, and the second is the hot holes injection to the first nitride layer applying Vd=-8.0 V, Vg=5.0 V and Vs=0V. Holes are generated by band-to-band tunneling in the deep depletion layer under the gate dielectric stack above the n+/p junction [4, 8]. Holes increase their energy due to the lateral field in depletion region of the channel and they are injected through the bottom oxide into the nitride trapping layer, where they recombine with the stored electrons or are trapped. As shown in Fig. 4(d), the state of "11" is the initial state and it can also been realized by erasing from other states shown in Table I.

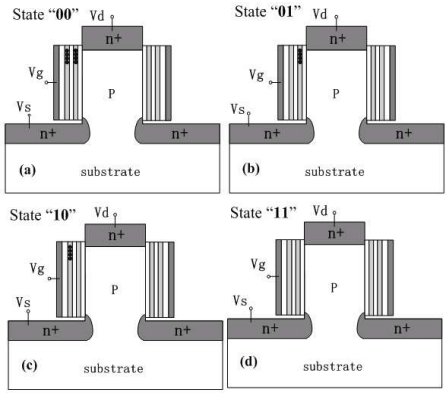


Fig. 4. The four states corresponding to bit-1 and bit-2 of the proposed VDNROM flash memory.

TABLE I.
VDNROM Flash Memory Program/Erase Operating Conditions
(Four states corresponding to bit-1 and bit-2)

State	P/E	Gate (Pulse)	Drain (Pulse)	Source	Time	Vth
'00'	Program from "11"	12V, 0V, 1µs	7V, 0V, 1µs	0 V	10 ms	5.5V
'01'	Program from "11"	6V, 0V, 1µs	5V, 0V, 1µs	0 V	10 ms	4.3V
'10'	Program from "11"	12V, 0V, -8V, 1µs, 9µs	7V, 0V, 1µs, 9µs, 5V	0 V	100 ms	3.3V
'11'	Erase	0V, -12V, 1µs	6V, 0V, 1µs	0 V	100 ms	2.3V

Fig. 5 shows transfer characteristics of the VDNROM flash memory cell with 0.3µm channel length in the four states. The threshold voltage of State "11" is 2.3V (the same Vth as the initial). State "00" has a threshold shift of ΔVth=3.2V from State "11". The ΔVth of 2.0V in State "01" is observed. The threshold voltage of State "10" is 3.3V, and the ΔVth is 1.0V. The transfer characteristics of each state exhibits excellent subthreshold performance as shown in Fig. 5. The programming and erasing characteristics of the VDNROM flash memory are shown in Fig. 6.

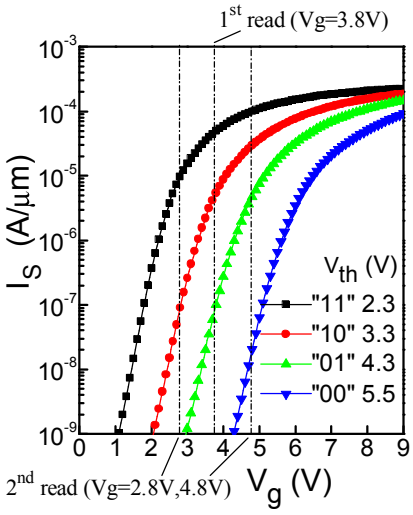


Fig. 5. The transfer characteristics of the programmed/erased bit-1 and bit-2 of the VDNROM flash memory.

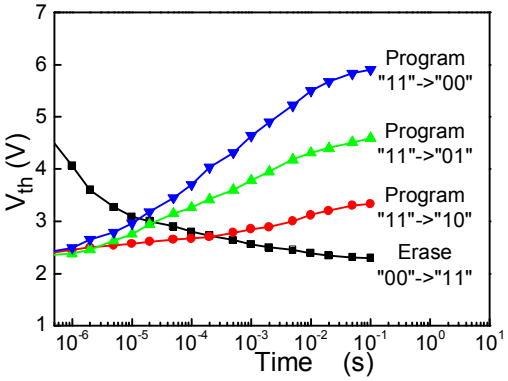


Fig. 6. The Programming/Erasing characteristics of the VDNROM flash memory.

The device is read in the "reverse" direction compared to programming, by applying the read biases to source electrode (1.5V) and grounding the drain electrode. This reverse read mode can enhance the threshold voltage sensitivity to the localized trapping charges [4]. As shown in Fig. 5, during the first read operation, the "00"and "01" states can be distinguished from the "10" and "11" states at 3.8V (gate voltage). After that, State "11" from State "10" and State "01" from State "00" at 2.8V and 4.8V (gate voltage), respectively, is performed for the second read operation.

Similarly, the bit-3 and bit-4 can be programmed, erased and read by interchanging the role of the drain/source electrodes.

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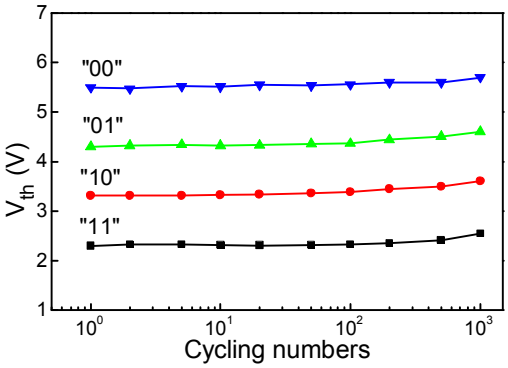


Fig. 7. The Endurance characteristics of the VDNROM flash memory.

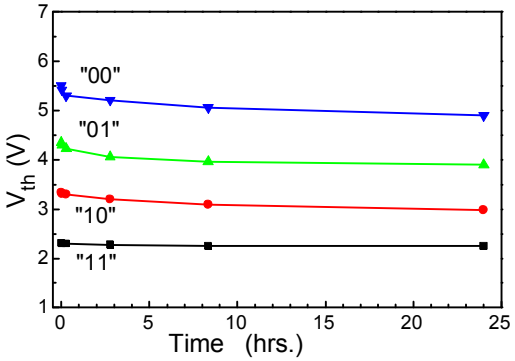


Fig. 8. The bake retention performance of the VDNROM flash memory at 150°C

Fig. 7 shows the endurance characteristics of the four states (corresponding to bit-1 and bit-2). The 2-bit cycling loop consists of the sequence of bit-2 program (State "11" to State "01") →bit-1 program ("01" to "00") →bit-2 erase ("00" to "10") →bit-1 erase ("10" to "11") that can be considered as the worst case, because the tunneling oxide has been tunneled by twice hot electrons and twice hot holes in one cycle (the inter-nitride oxide by once electrons and once holes). After 10^3 P/E cycles, the worst Vth window of 0.8V is maintained in spite of the Vth increase at the erased cell. These electrical results indicate that the cycling endurance performance of the VDNROM cell is acceptable.

Fig. 8 shows the bake retention performance of the VDNROM measured at 150°C. 0.4V small degradation and saturation of Vth are observed after 24 hours baking measurement. With the better quality tunneling oxide, the smaller degradation of Vth window can be observed.

IV. Conclusion

For the first time, a novel VDNROM flash memory cell with an oxide-nitride-oxide-nitride-oxide (ONONO) gate dielectric stack has been proposed, demonstrated experimentally, and successfully operated in four-bits-per-cell mode in the 0.3μm channel length vertical device. In the conventional planar NROM cell, the cell area further scaling is limited by the gate length scaling. In contrast, since the cell area of the VDNROM structure is independent of the gate length, the structure can have high capability of the cell area shrinking with the relaxed requirement of the gate length scaling. Moreover, the fabrication of the VDNROM is basically compatible with planar CMOS technology. The reliability performances including the cycling endurance and the bake retention at 150°C have also been investigated and are acceptable. This new technology can be used for data storage due to the high density, and for embedded applications due to the simplicity of the process.

Acknowledgment

The authors would like to thank the Microfabrication Laboratory staffs of Peking University for their supports in device fabrication. This work is supported by National Natural Science Foundation of China (No. 90207004) and State Key Fundamental Research Project of China.

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Toshiba Develops New NAND Flash Technology

12 June, 2007

New three dimensional cell array increases density with existing process technology

TOKYO--Toshiba Corporation today announced a new three dimensional memory cell array structure that enhances cell density and data capacity without relying on advances in process technology, and with minimal increase in the chip die size. In the new structure, pillars of stacked memory elements pass vertically through multi-stacked layers of electrode material and utilize shared peripheral circuits. The innovative design is a potential candidate technology for meeting future demand for higher density NAND flash memory.

Typically, advances in memory density reflect advances in process technology. Toshiba's new approach is based on innovations in the stacking process. Existing memory stacking technologies simply stack two-dimensional memory array on top of another, repeating the same set of processes. While this achieves increased memory cell density, it makes the manufacturing process longer and more complex. The new array does increase memory cell density, is easier to fabricate, and does not produce much increase in chip area, as peripheral circuits are shared by several silicon pillars.

Toshiba's cutting edge etching technology drives a through-hole down through a stacked substrate, i.e. a multi-layer sandwich of gate electrodes and insulator films. Pillars of silicon lightly doped with impurities are deposited to fill in the holes. The gate electrode wraps around the silicon pillar at even intervals, and a pre-formed nitride film* for data-retention, set in each joint, functions as a NAND cell.

NAND flash memory functions through batch processing of cells, in large numbers of elements connected in series. Toshiba's new array increases density without increasing chip dimension, as the number of connected elements increases in direct proportion to stack height. For example, a 32-layer stack realizes 10 times the integration of a standard chip formed with the same generation of technology.

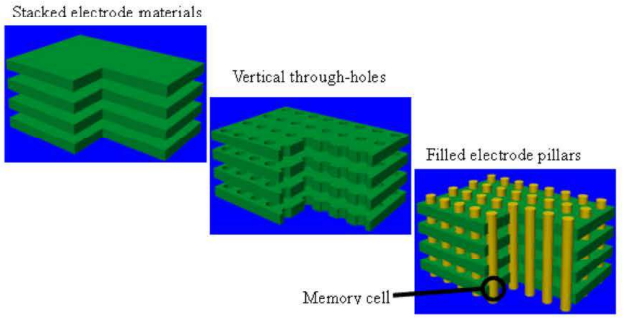
Toshiba will further develop this elemental technology to the level where it matches current structures in terms of security and reliability.

This announcement was presented in the VLSI symposium on June 12.

* Toshiba's new method has a SONOS structure-- silicon-oxide-nitride-oxide- silicon --and the electrical charge is held in the silicon-nitride film, which is formed inside gate holes. Traps are formed to lock the electrical charge inside the silicon-nitride film.

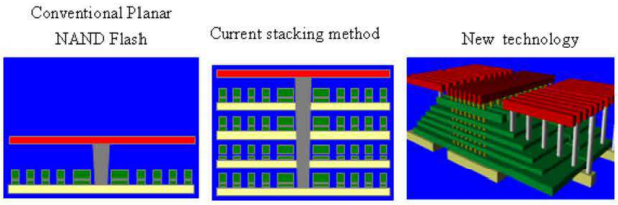
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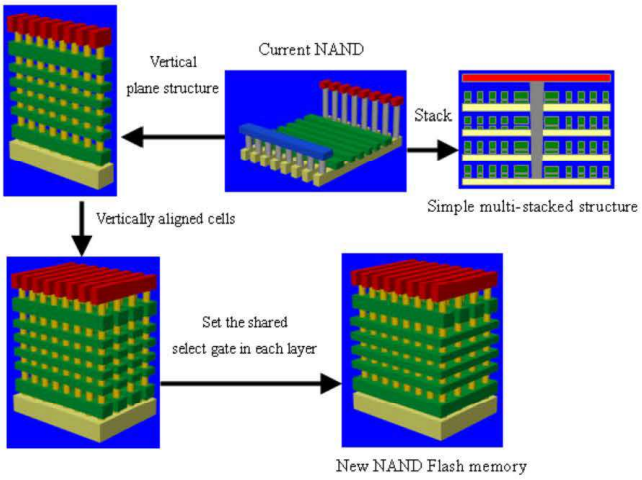


Even if the number of stacks is increased, lithography is only done once, and there is only a small increase in the number of control gate drivers.

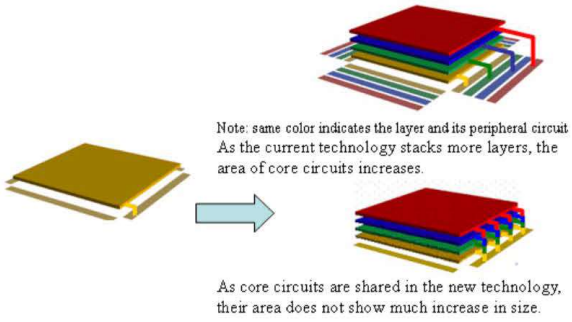
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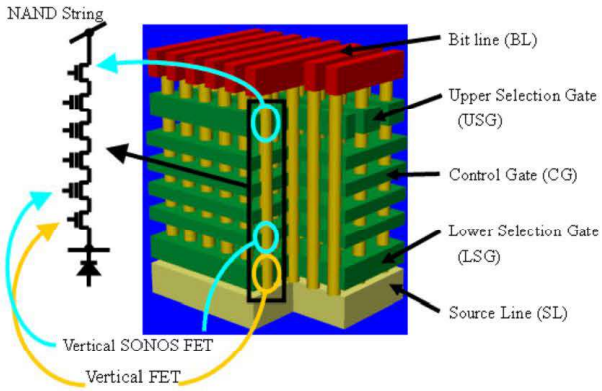
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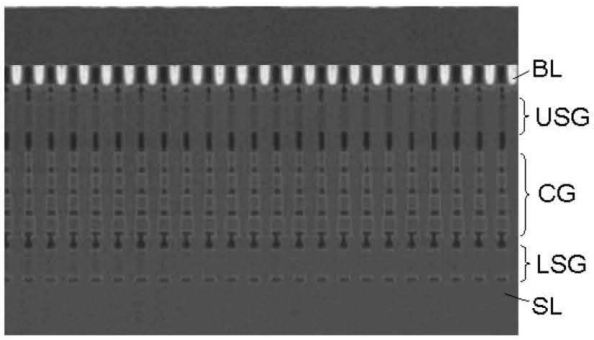


Core Circuitry of Stacked Memory



The structure of the new memory cell





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Appendix KIM02

Mater. Res. Soc. Symp. Proc. Vol. 997 © 2007 Materials Research Society 0997-I03-12

A Comparison of N+ Type and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories

Moon Kyung Kim[1], SooDoo Chae[2], Chung Woo Kim[2], Jo-won Lee[3], and Sandip Tiwari[1]
[1]Electrical and Computer Engineering, Cornell University, Ithaca, NY, 14850
[2]Semiconductor Business, Samsung Electronics Co., Yongin-City, Kyunggi-Do, Korea, Republic of
[3]Tera-level Nano Devices, Seoul, Korea, Republic of

ABSTRACT

The polarity of gates and the threshold voltages are primary parameters that determine the electric fields in the gate stack region of non-volatile memories. This field is central to programming, retention and the other characteristics of the devices. We have investigated the effect of the gate polysilicon polarity, experimentally, for silicon-oxide-nitride-oxide-silicon (SONOS) memory devices on silicon-on-insulator (SOI) wafers. An ultra-thin oxide-nitride-oxide (ONO) film with high trap density and strong localization of the trapping provides the scalability and retention in our structures. The effect of ONO film, grown and deposited and of doping was simulated and characterized. Retention is affected by the electric field between the control gate and the storage node. Our experiments and simulations verify the consequences of different polarity of control gates through the change in electric field that they cause in retention and erase times for n^+ and p^+ polysilicon gate SONOS memories is verified through the characteristic energies of the processes.

INTRODUCTION

There is broad consensus that achieving both the reliability and low voltages of operation is a very difficult challenge for the floating gate type EEPROM as the gate lengths shrink [1]. The floating-gate-type EEPROM requires a thicker tunneling oxide of more than 7-9 nm to guarantee retention characteristics by suppressing tunneling. This gives rise to a high-voltage operation necessitated by a 6 MV/cm of programming/erase electric fields [2]. Use of distributed storage, thus reducing consequences of leakage paths, is one of the ways of addressing these problems. Advanced thin film technology has resulted in a low voltage operation and long retention characteristics in devices based on Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) [3][4]. Silicon nitride and its interface with silicon dioxide provides an alternative for this charge storage where the highly localized storage of charge at increased number of sites may allow a further scaling of the insulator thickness and a trade-off in other attributes. But, SONOS memory has problems in discharging of the electrons from the traps of silicon nitride. When SONOS memory is discharged, the electrons from a gate electrode are injected into silicon nitride through the top oxide stack. To resolve this problem, we have used p^+ polysilicon gate, which has a higher work function than n^+ polysilicon gate. This decreases the amount of back-tunneling electrons from the gate. In our experiments, the effect of doping levels has been simulated and characterized.

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EXPERIMENT

Figure 1 shows schematic views of n^+ type and p^+ type polysilicon gate SONOS structures. 0.5 um gate width/length devices with n^+ polysilicon/ p^+ polysilicon are fabricated on SOI substrates using conventional CMOS processing technology. Active area is defined by optical lithography method and isolation is achieved by separating islands. The oxide-nitride-oxide layers are stacked with the thickness of 3 nm/5.5 nm/7 nm and Figure 2 shows a transmission-electron micrograph of the cross section of this grown and deposited memory stack where the dark region is silicon nitride. The n^+ type and p^+ type polysilicon layers in each device are deposited using LPCVD. N^+/p^+ implants were employed to achieve doping levels around 10^{20} cm^{-3}. Side walls, source/drain implantations and metallization are utilized in fabrication of the completed SONOS devices.

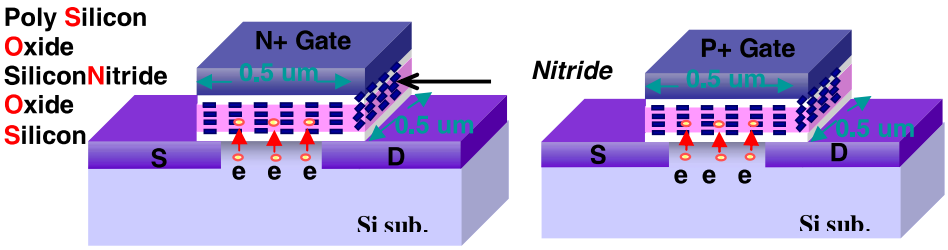


Figure 1. Schematics of n^+ type and p^+ type polysilicon gate SONOS.

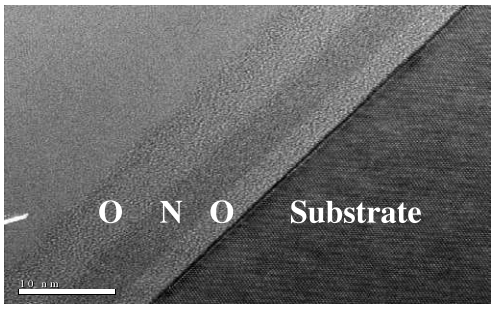


Figure 2. Transmission-electron-micrograph (TEM) of the ONO stack (3 nm / 5.5 nm / 7 nm).

DISCUSSION

Figure 3 shows the energy band diagram of SONOS memory when discharging electrons from the silicon nitride. It has a different energy barrier than for electrons in the polysilicon gate that are tunneling into the silicon nitride through the silicon oxide. The energy barrier between n^+ polysilicon gate and the top oxide is 3.1eV and that of p^+ polysilicon gate with the top oxide is 4.1eV. A higher work function of p^+ polysilicon gate might be expected to improve erase efficiency by reducing electrons back tunneling from the gate. To simulate threshold voltage difference on boron doping concentrations of polysilicon gates in erasure mode, a one-dimensional (1-D) and one band model of charge transport is used, which takes into account Hall-Shockley-Reed statistics for trap population. And the thin oxide between Si and Si_3N_4

facilitates the electron injection because the electric field is amplified in the oxide due to the lower dielectric constant of oxide in comparison to that of nitride [5].

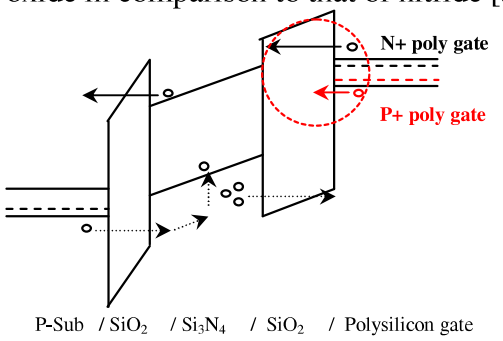


Figure 3. Energy band diagram of n^+ polysilicon and p^+ polysilicon gate SONOS when negative voltage is applied to the gate in erasure process.

Figure 4 shows threshold voltage dependence on boron doping concentrations of polysilicon in erasure mode. As the boron doping level is increased, the erasure speed is faster and the erased threshold voltage of p^+ polysilicon gate with over 10^{20} cm^{-3} doping level is below -2.5 V at the erasure pulse of 1 *m*s.

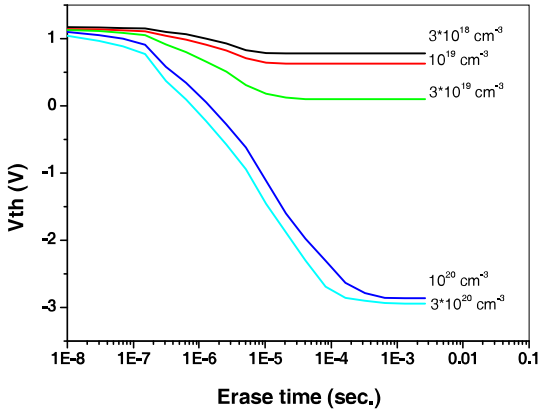


Figure 4. Threshold voltage dependence on boron doping concentrations of polysilicon gates in erasure mode.

Figure 5 shows transfer characteristics with n^+ and p^+ polysilicon gates at 0.5 V drain voltage. The difference of the threshold voltages between devices of n^+ and p^+ polysilicon gates is about 1.1 eV because of the Fermi level difference of n^+ and p^+ polysilicon and the process variance in ONO films in each device. To get high-speed SONOS memory devices, optimization of ONO thickness is very important [6]. The characteristics of ONO layers in these devices are not as good as previous devices. However, it shows clear differences in erasure characteristics. Reducing thicknesses of layers can improve memory speeds but it occurs at the expense of reduced retention time in the limits due to the reduction of tunneling barrier thickness.

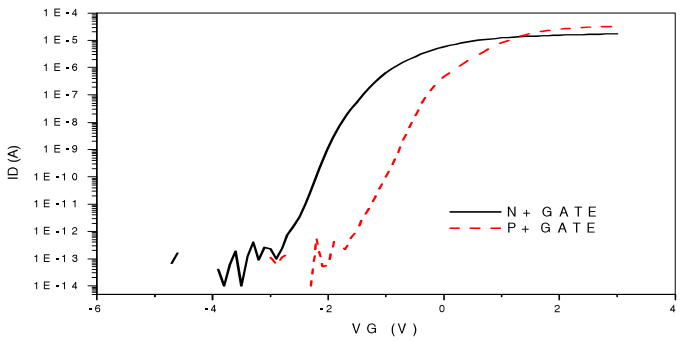


Figure 5. Transfer characteristics of n^+ and p^+ polysilicon gates at 0.5V drain voltage.

Figure 6 shows programming speed characteristics employing field assisted tunneling mechanism. Larger write voltages result in higher tunneling probabilities due to the reduction of the effective barrier. This is observed in these plots as a decrease in writing times with increased applied tunneling voltages. To obtain 4 V of threshold voltage shift, the program time is about 20 us at 16 V program voltage, and this programming time is sufficiently short for usage in semiconductor memories for massive data storage. In Figure 6 we can also see the alteration and differences in program speed behavior for the n^+ and p^+ polysilicon gates near 14 V program voltage.

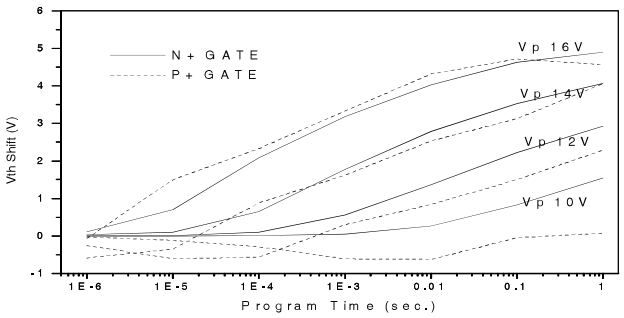


Figure 6. Programming speed characteristics of n^+ and p^+ gate.

The effective field of 14V programming voltage is 10.89 MV/cm and Φ_{os}/X_{ot} is 10.3 MV/cm. Here Φ_{os}, X_{ot} are the energy barrier between silicon and silicon oxide and the thickness of tunneling oxide, respectively. The mechanism of the programming state for $E_{ot}>\Phi_{os}/X_{ot}$ is Fowler-Nordheim (FN) tunneling. In FN tunneling, the programming speed of n^+ and p^+ polysilicon gate memory is almost the same, but in direct tunneling and modified FN tunneling (<14V), the programming speed of n^+ polysilicon gate is faster than that of p^+ polysilicon gate. The erasure time of SONOS memory is somewhat slow because it occurs via the injection of electrons through the top oxide from the gate and because of the heavy effective mass of the hole for hole transport for erasure. To solve this problem, several methods have been introduced recently. The use of high-k material instead of top SiO_2 film would help decrease the number of back-tunneling electrons from the top oxide arising from capacitive coupling. The high-k material has numerous trap charges and the usage of high-k material is significant change from current practice of CMOS processes. We expect that a higher work function of p^+ polysilicon gate will improve the erase speed.

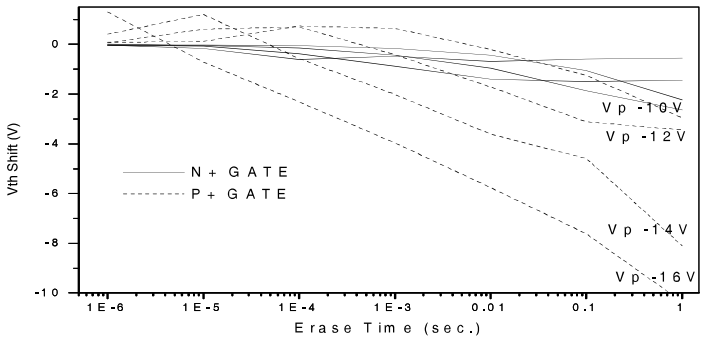


Figure 7. Erasing speed characteristics of n^+ and p^+ gate.

Figure 7 shows erasure speed characteristics by field-assisted tunneling method. The erase speed of p^+ polysilicon gate memory is much faster than that of n^+ polysilicon gate memory. To achieve -4 V threshold voltage shift from a programmed state in p^+ polysilicon gate memory, the erase time is about 1 ms at -16 V erase voltage.

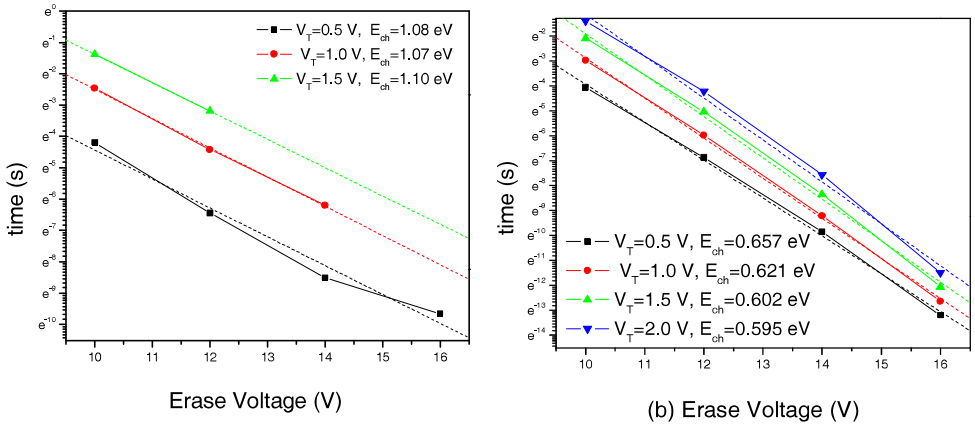


Figure 8. Emission characteristic energy of
(a) n^+ polysilicon gate and (b) p^+ polysilicon gate SONOS.

Figure 8 shows the erasing characteristic energy for various voltages for n^+ type and p^+ type polysilicon gate SONOS memories. The characteristic energy for tunneling for the charging and discharging arises from the tunneling transmission probability, and hence preserves the exponential aspect. Emission process has a higher characteristic energy than a capture process due to the use of a cold mechanism and the erase efficiency of p^+ type polysilicon gate SONOS is improved compared to that of n^+ type polysilicon gate SONOS. The emission characteristic energy of n^+ polysilicon gate SONOS is somewhat larger than that of p^+ polysilicon gate (0.59 ~0.65 eV). Figure 9 shows the endurance characteristics of n^+ and p^+ polysilicon gate memories after various erase and programming cycles. The threshold voltage is changed by 0.3 V in the erasure state of n^+ polysilicon gate memory and by 0.8 V in the program state of n^+ polysilicon gate memory after 10^4 cycles by FN program and erasure. The main reason is that electrons are overcharged into silicon nitride when SONOS memory is programmed. In the case of p^+ polysilicon gate memory, the threshold voltage variance of the program state is 0.35 V and that

of the erase state is over 0.8 V after 10^4 cycles. The different erasure method, i.e. using hot holes, in flash memories causes higher tunnel oxide damage. But it is expected that D_2 annealing treatment may decrease the rate of the degradation of the tunnel oxide.

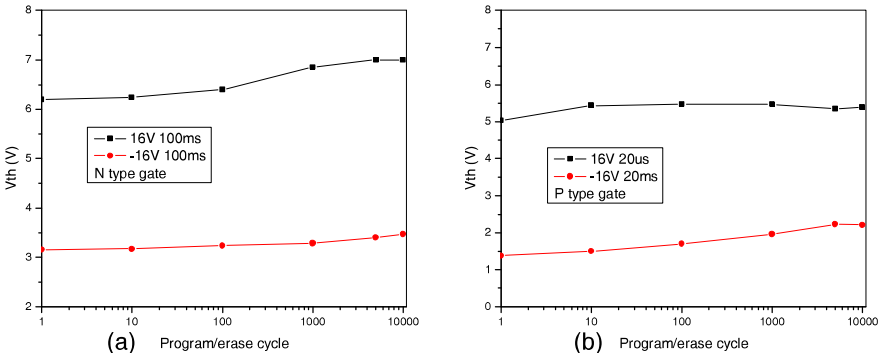


Figure 9. Endurance characteristics of (a) n^+ and (b) p^+ polysilicon gate memories.

CONCLUSIONS

According to our simulation, the erased threshold voltage of p^+ polysilicon gate memory with over 1E20/cm^3 doping level was below -2.5 V at the erase pulse of 1 ms. In our experimental results, considering the program/erase threshold voltage window as 4 V in p^+ polysilicon gate memory, the program time is approximately 20 us at 16 V program voltage and the erase time is about 1 ms at –16V erase voltage using FN tunneling method. In conclusion, this study has helped understand trapping/detrapping process in the presence of different fields that are obtained through different polarity control gates. A higher work function of p^+ polysilicon gate can improve erase speed while satisfying other memory characteristic needs such as of endurance.

ACKNOWLEDGMENTS

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Appendix SZE01

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